

Demonstration of Robust Retention in Band Engineered FEFETs for NAND Storage Applications Using Tunnel Dielectric Layer

Prasanna Venkatesan¹, Graduate Student Member, IEEE,

Lance Fernandes², Graduate Student Member, IEEE,

Priyanka Ravikumar, Graduate Student Member, IEEE, Chinsung Park³, Member, IEEE, Huy Tran,

Zekai Wang, Hari Jayasankar, Amrit Garlapati, Taeyoung Song⁴, Graduate Student Member, IEEE,

Mengkun Tian, Hang Chen, Member, IEEE, Winston Chern, Kijoon Kim, Jongho Woo, Suhwan Lim⁵,

Kwangsoo Kim⁶, Shimeng Yu⁷, Fellow, IEEE, Suman Datta⁸, Fellow, IEEE, Wanki Kim,

Daewon Ha⁹, and Asif Khan, Senior Member, IEEE

Abstract—We perform a comprehensive study of memory retention characteristics in ferroelectric field-effect transistors with different engineered gate stacks designed to achieve a large memory window (MW) for NAND storage applications. Through this study, we show that the widely reported retention loss in these band-engineered FEFETs can be mitigated by optimizing the position of the dielectric insert. Specifically, placing the dielectric insert in the middle of the FE stack (tunnel dielectric layer, TDL) leads to excellent retention while increasing the MW to a quad-level-cell compatible level ($\geq 7.5V$). This enhanced retention is enabled by the potential wells at the TDL-FE interfaces that energetically secure the MW-enhancing charges and prevent their detrapping. In contrast, placing the dielectric insert on the gate side (gate blocking layer, GBL), while maximizing the MW, compromises retention due to the detrapping of the trapped charges at the GBL-FE interface through the GBL.

Index Terms—Ferroelectrics, retention, FEFET, trap dynamics, NAND.

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Prasanna Venkatesan, Lance Fernandes, Priyanka Ravikumar, Chinsung Park, Huy Tran, Zekai Wang, Hari Jayasankar, Amrit Garlapati, Taeyoung Song, Winston Chern, and Shimeng Yu are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: pravindran6@gatech.edu).

Mengkun Tian is with the Institute of Materials, Georgia Institute of Technology, Atlanta, GA 30332 USA.

Hang Chen is with the Institute of Electronics and Nanotechnology, Georgia Institute of Technology, Atlanta, GA 30332 USA.

Kijoon Kim, Jongho Woo, Suhwan Lim, Kwangsoo Kim, Wanki Kim, and Daewon Ha are with the Advanced Device Research Laboratory, Semiconductor Research Center, Samsung Electronics Company Ltd., Suwon-si 16677, South Korea.

Suman Datta and Asif Khan are with the School of Electrical and Computer Engineering and the School of Material Science and Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

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I. INTRODUCTION

BAND engineered ferroelectric field-effect transistors have emerged as a viable solution for continued z-scaling in 3D NAND devices (Fig. 1(a)). By inserting dielectric layers at different positions in the ferroelectric gate stack, these FEFETs have been demonstrated to enable multi-bit operation ($MW \geq 7.5$) at low write voltages (≤ 20 V) while meeting the gate stack thickness requirements for a vertical NAND process flow (≤ 20 nm) [1], [2], [3], [4], [5], [6], [7], [8], [9]. This enhanced MW could be realized through two mechanisms depending on the location of the dielectric insert: (1) Tunnel Dielectric Effect, where the dielectric (tunnel dielectric layer or TDL) is inserted in the middle of the ferroelectric layer and enhances the MW through the trapped charges at FE-TDL interfaces [3], [10], [11]. (2) Gate side injection, where the dielectric (gate blocking layer or GBL) is inserted next to the gate, allowing for charge injection into the FE-GBL interface leading to MW enhancement [2], [5], [9]. The MW of these devices can be described using the below equation:

$$MW = \frac{(P_r - Q_{it})}{C_{FE}} + \frac{(Q'_{it} - Q_{it})}{C_{TDL/GBL}} \quad (1)$$

where P_r is the remanent polarization of the ferroelectric, Q_{it} is the screening charge density at the FE-channel IL interface, Q'_{it} is the trapped charge density at the FE-TDL/GBL interface that leads to the enhanced MW.

While FEFETs, in general, have been known to exhibit robust retention, these devices with large MW have suffered from poor retention characteristics exhibiting retention losses between 25 and 50% after 1e4 s at room temperature [2], [5]. A detailed account of this unstable retention in GBL FEFETs was presented by Kuk et al. [5].

In this work, we perform a comprehensive study of the retention behavior of large MW FEFETs for FE-NAND applications using six gate stacks at 25 - 125°C: two standard FEFET (10 and 19 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO)), two TDL FEFETs (9 nm HZO/ 1 nm Al_2O_3 / 9 nm HZO (9/1/9) and 8 nm HZO/ 3 nm Al_2O_3 / 8 nm HZO (8/3/8)) and two GBL FEFETs (14 nm HZO/ 4 nm SiO_2 (14/4) and 6 nm HZO/

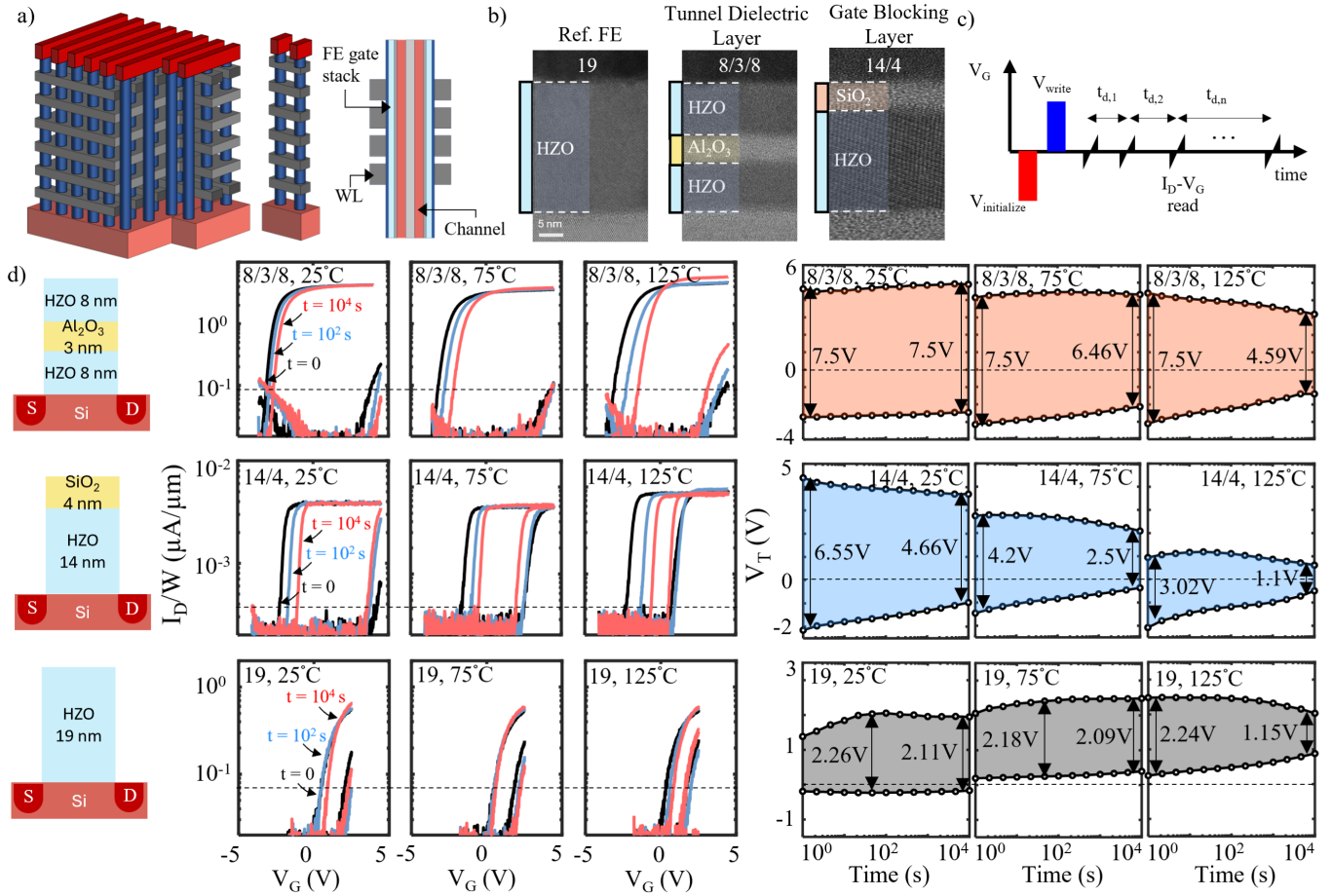


Fig. 1. (a) Schematic of vertical NAND structure (b) TEM of (1) 19 nm standard FE-HZO FEFET, (2) 8 nm HZO / 3 nm Al₂O₃ / 8 nm HZO (8/3/8) TDL FEFET and (3) 14 nm HZO / 4 nm SiO₂ (14/4) GBL FEFET. (c) Measurement scheme for retention characterization. (d) Retention of FEFETs with the three gate stacks for 1e4 s done at RT, 75°C and 125°C. The write voltages for 8/3/8, 14/4 and 19 are 13 V, 14 V and 11 V respectively. GBL FEFETs show significant retention loss (29%) even after 1e4 s at RT. While the standalone at FE and TDL stacks show < 1% retention loss. Further, the MW of the GBL FEFET reduces at higher temperatures.

2 nm Al₂O₃ / 6 nm HZO / 4 nm SiO₂ (6/2/6/4)). Through this analysis, we demonstrate for the first time, that TDL FEFETs where the dielectric layer is placed in the middle of the ferroelectric gate stack enhances retention of the FEFETs significantly, exhibiting minimal to no retention loss while placing the dielectric layer next to the gate leads to significant retention loss resulting from loss of the MW enhancing trapped charges.

II. RETENTION CHARACTERIZATION

The FEFETs are fabricated using the process flow described in [12], [13], and [14]. In this work, Al₂O₃ is used as the TDL and SiO₂ is used as the GBL as they have been shown to be optimum dielectrics for MW enhancement in these positions [10]. The high resolution cross-section of FEFET with standard FE (19 nm), TDL (8/3/8) and GBL (14/4) gate stacks obtained using Transmission Electron Microscopy (TEM) are shown in Fig. 1(b). Retention is characterized by programming the devices to a high (ERS) or a low (PGM) threshold voltage (V_T) state and reading the transfer characteristics (I_D - V_G) over time at different temperatures.

Fig. 1(d) shows the time evolution of the transfer characteristics and V_T of 19, 8/3/8 and 14/4 stack based FEFETs

at RT, 75°C and 125°C. The initial positive shift observed in some of the cases is a result of read-after-write delay caused by screening of the polarization at the FE-IL interface [13], [15]. The initial MW, in these cases, is assumed to be the MW after read-after-write delay. The 19 nm FEFET exhibits a memory window of 2 V, which decreases slightly to 1.9 V after 1e4 s. The band engineered FEFETs, 8/3/8 and 14/4, with a TDL and GBL, demonstrate a large MW of 7.5 V and 6.55 V, respectively. The time evolution of V_T in 8/3/8 FEFET exhibits robust retention, showing less than 1% loss after 1e4 s at RT. In contrast, the MW of GBL-FEFET 14/4 drops to 4.66 V indicating a 29% retention loss under the same conditions. 19 and 8/3/8 FEFETs begin to show retention degradation at 75 and 125°C. However, their retention losses are significantly lower compared to the 14/4 FEFET even at elevated temperatures. At 125°C, the MW of the 14/4 degrades down to that of a standard FEFET, suggesting that the trapped charges responsible for its MW enhancement have fully detrapped.

The retention loss after 1e4 s at RT, 75°C and 125°C for all the samples is summarized in Fig. 2(a). The initial MW of the standard FE and TDL FEFETs remains constant with temperature (upto 125°C). However, the initial MW of FEFETs with a GBL at 75 and 125°C is significantly lower than that at RT,

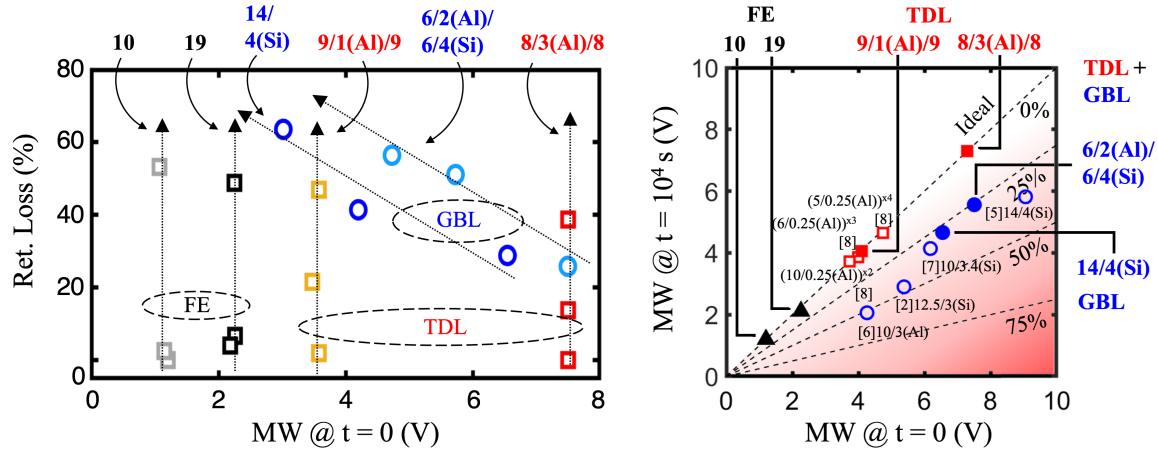


Fig. 2. (a) Retention loss vs initial MW at different temperatures is shown for different gate stacks. The arrow indicates the direction of increasing temperature from 25-125°C. (b) Retention benchmark of GBL, TDL and standalone FE gate stacks shows the MW after 1e4 s against the initial MW at RT. The 1:1 line along the diagonal corresponds to 0% retention loss while the other dashed lines indicate 25, 50 and 75% loss in MW after 1e4 s. The benchmark shows that TDL FEFETs have near perfect retention behavior compared to GBL FEFETs which lose between 25 and 50% of the MW after 1e4 s.

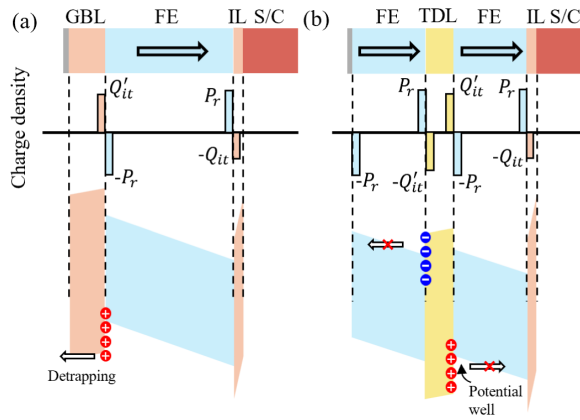


Fig. 3. The band diagrams of the GBL and TDL FEFETs are drawn by solving the Poisson equation [3], [11], [16]. In order to achieve MW enhancement through the insertion of dielectric in the ferroelectric gate stacks, the trapped charge Q'_{it} at the FE-TDL interface should be larger than the screening charge Q_{it} at the channel IL-FE interface. However, in the case of GBL ferroelectric gate stacks, the trapped charge detraps through the GBL resulting in loss of the MW enhancement. On the contrary, in TDL gate stacks, the MW enhancing charges are energetically stable in potential wells at the FE-TDL interfaces, leading to robust retention.

indicating an inherent instability in the MW enhancement. The retention loss increases with temperature across all samples. In a benchmark with several large MW FEFETs from the literature (Fig. 2(b)), it can be seen that TDL FEFETs exhibit robust retention characteristics with retention loss below 3% while the GBL FEFETs show retention losses between 25 and 50% after 1e4 s at RT. The robust retention in the 9/1/9 TDL FEFET also reveals that 1 nm Al_2O_3 is sufficient to separate the positive and negative charges at the FE-DE interfaces that are responsible for the MW enhancement. Similar retention characteristics in laminated FEFET with Al_2O_3 inserts as thin as 2.4 Å has also been reported by Lee et al. [8]

III. MECHANISM

Based on the insights from the above experiments, we propose a mechanism for retention loss. Both TDL and GBL FEFETs rely on the trapped charges at the ferroelectric-dielectric interface for MW enhancement. From eq. [1], the trapped charge Q'_{it} needs to be greater than the screening charge Q_{it} at the channel IL to achieve MW enhancement irrespective of the location of the dielectric. These trapped charges detrapp over time and leak away towards the gate through the leaky GBL (Fig. 3(a)). As $Q'_{it} - Q_{it}$ reduces, the MW enhancement decreases, leading to retention loss. As temperature is increased, the detrapping accelerates resulting in accelerated MW/retention loss. That said, similar temperature accelerated detrapping of trapped screening charges at a FE-IL interface has been observed in FEFETs in the context of the well-known read-after-write delay problem [12], [13], [17], [18].

In the case of TDL, on the contrary, the condition for MW enhancement enables a potential well at the two FE-TDL interfaces (Fig. 3(b)). This energetically confines the trapped charges leading to MW enhancement. And with the other methods of leakage not possible due to the thick ferroelectric layer, TDL FEFETs inherently possess a retention advantage over GBL FEFETs.

IV. CONCLUSION

In summary, we demonstrate best-in-class retention in QLC compatible TDL FEFETs where the dielectric layer is inserted in the middle of the ferroelectric gate stack showing < 1% retention loss after 1e4 s. This robust retention is enabled by the potential wells at the FE-TDL interfaces which energetically protects the MW enhancing charges against detrapping. GBL devices, on the other hand, while showing larger MWs, exhibit large retention losses (25 - 50%) due to the detrapping of MW enhancing trapped charges. While we observe that the retention loss increases with temperature, the initial MW in GBL FEFETs decreases with temperature contrary to standard and TDL FEFETs where it remains constant, further emphasizing the significance of the position of the dielectric for vertical NAND applications.

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