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Breaking the Hydrogen Barrier: BEOL-Safe In_2O_3 Transistor

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Outline of this Talk

- M3D Integration with Oxide Transistors
- BEOL-Safe Oxide Transistor (FGA Immunity)
- Deep Dive into Electrical Characteristics
- Unveiling Defect Dynamics
- Key Takeaway & Conclusion

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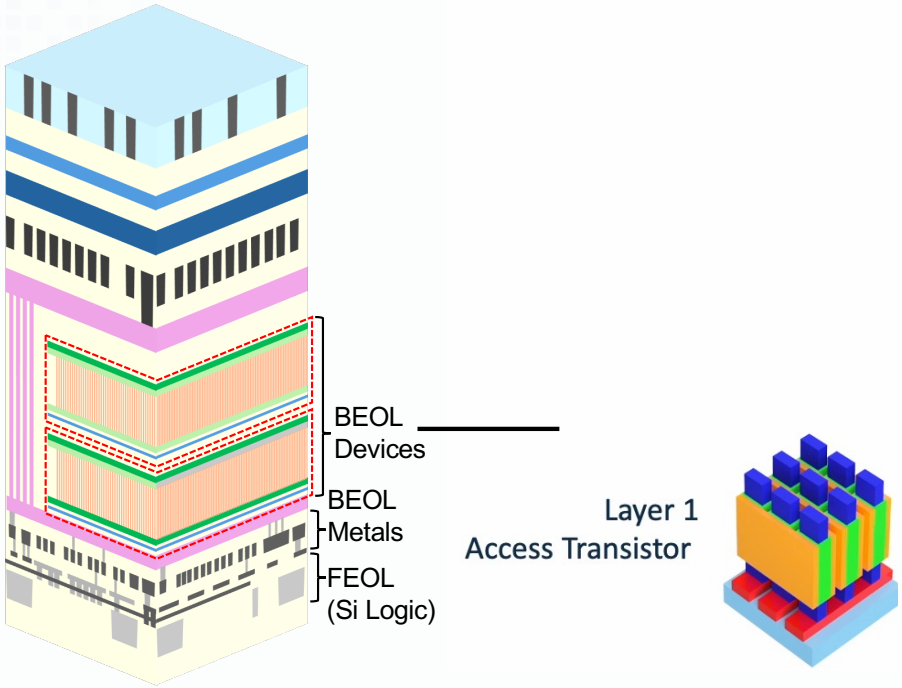
- M3D Integration with Oxide Transistors
  - BEOL-compatibility for monolithic 3-D integration
  - Critical Challenges
  - Recent Approaches
- BEOL-Safe Oxide Transistor (FGA Immunity)
- Deep Dive into Electrical Characteristics
- Unveil Defect Dynamic
- Key Takeaway & Conclusion

BEOL-compatibility for monolithic 3-D integration



- Ultra-low I_{OFF}
- Acceptable μ_{FE}
- Robust Electrostatics

1/ Low temperature processing:

All BEOL steps below 400 ^{0}C.

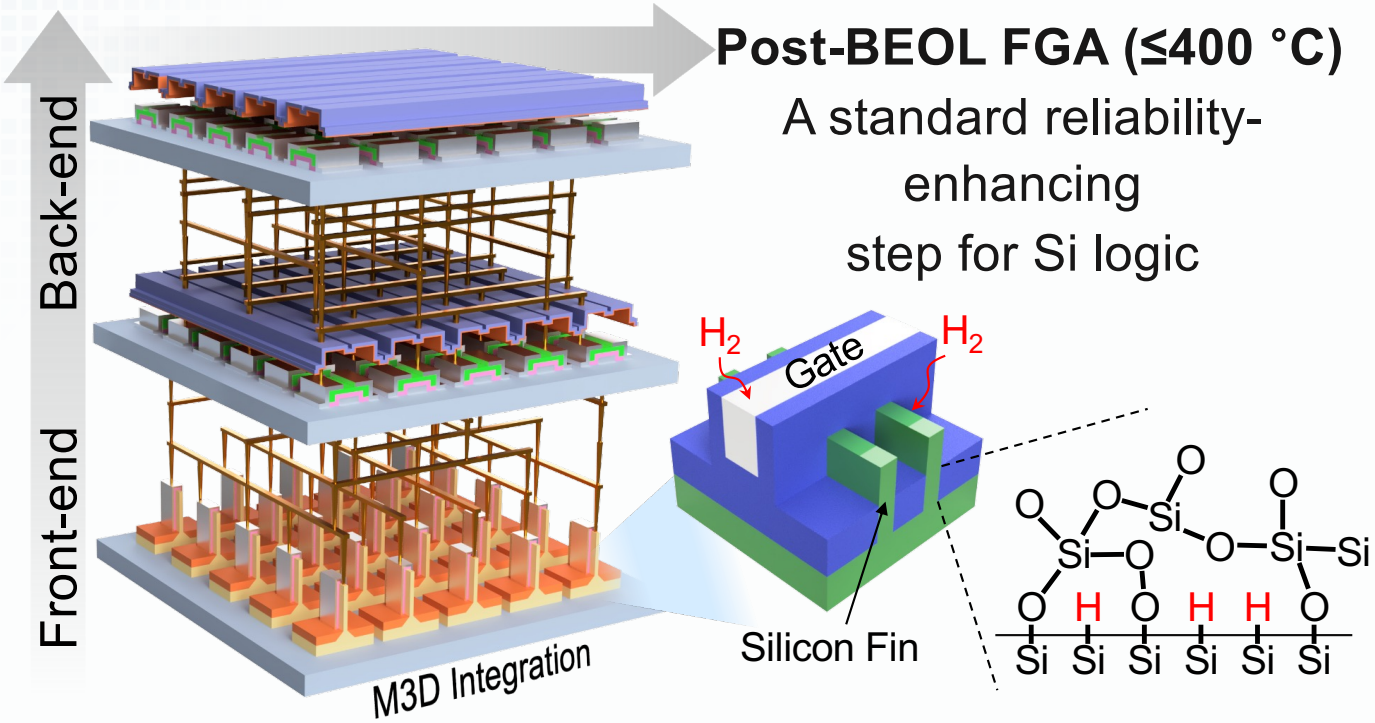
✅ Demonstrated

2/ FGA Immunity:

Resistance to hydrogen at 400 ^{0}C or higher.

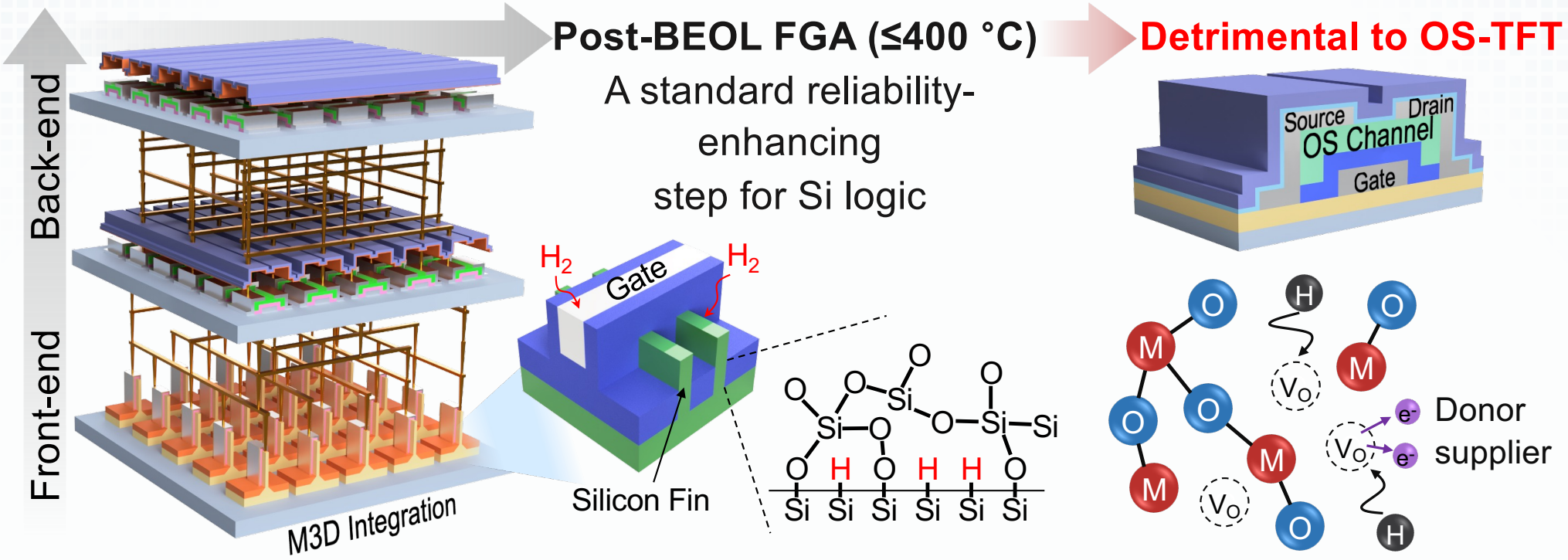
⚠ Under Evaluation

M3D Integration Challenges for OS-TFTs



FGA is a required final BEOL step used to passivate front-end Si logic transistors and improve reliability.

M3D Integration Challenges for OS-TFTs

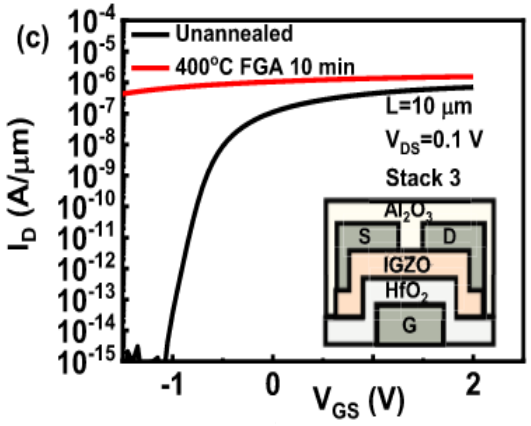


However, post-processing FGA destabilizes OS-TFTs via H incorporation.

M3D Integration Challenges for OS-TFTs

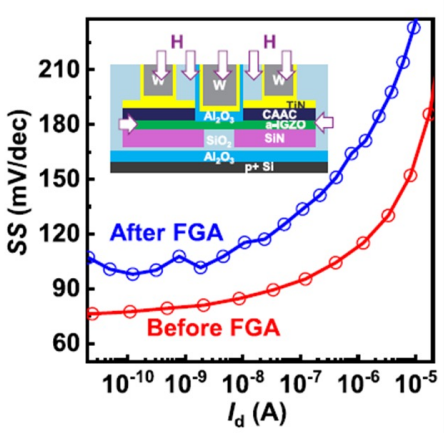
Performance Instability

Large Negative V_{TH} Shift



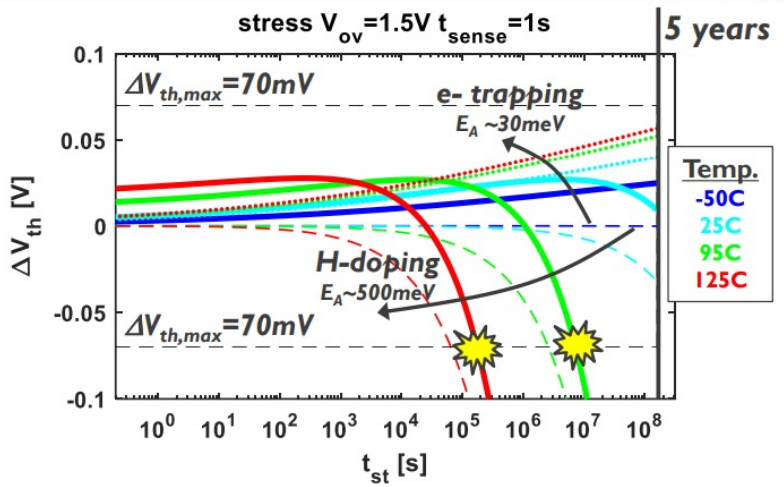
Z. Lin et al., TED, 2025 (SJTU)

SS degradation



H. Tang et al., EDL, 2025 (imec)

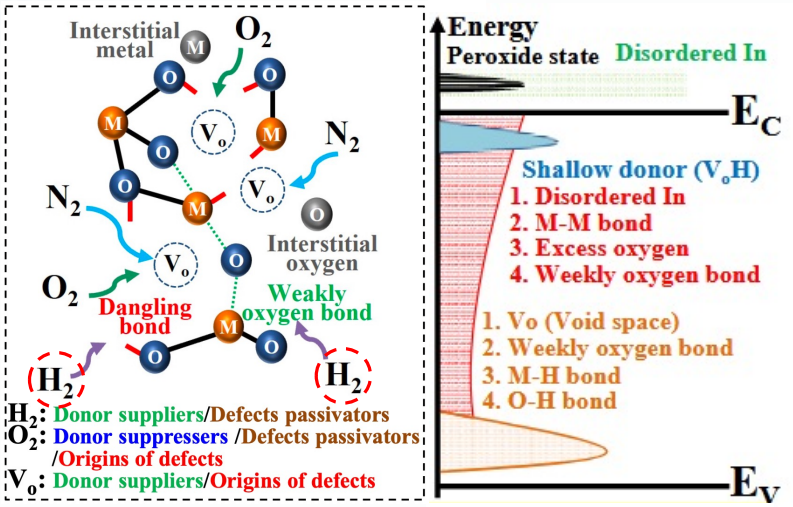
Reliability Degradation



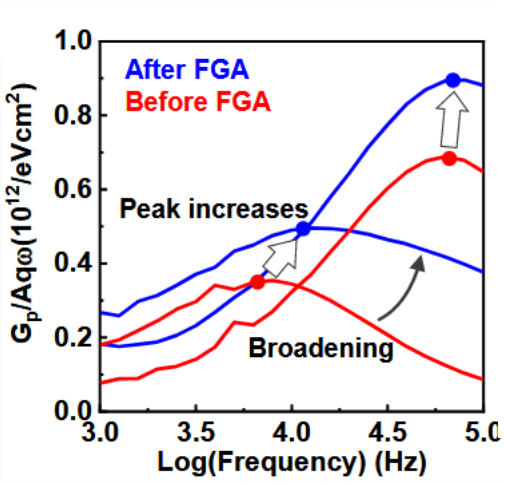
A. Chasin et al., IEDM, 2024 (imec)

H ingress during FGA is a major barrier to BEOL-integrated OS-TFTs, causing negative V_{TH} shift, SS degradation, and reliability loss.

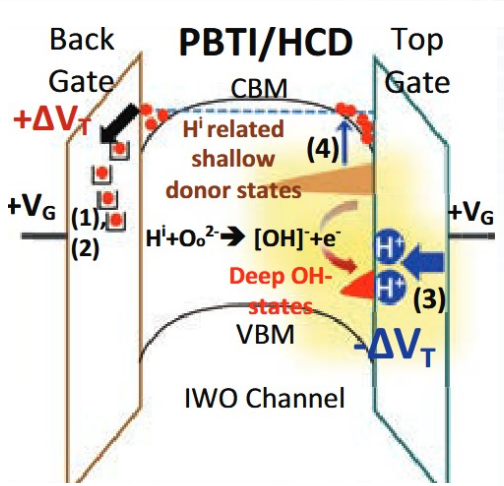
Why Hydrogen Ingress Degrades OS-TFTs



C.-K. Chen et al., IEDM, 2022 (NUS)



H. Tang et al., EDL, 2025 (imec)



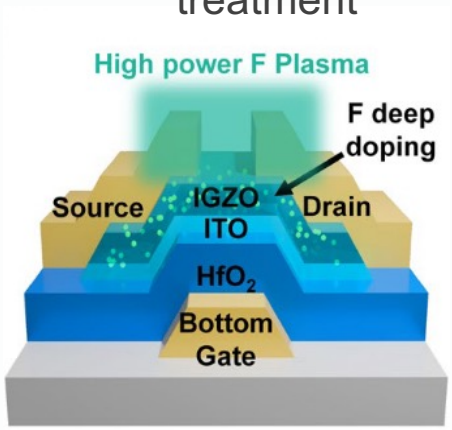
K. A. Aabrar et al., VLSI, 2024 (GT

H incorporation can form M–H or M–OH bonds, introducing additional sub-gap trap states, increasing D_{it}, and shifting V_{TH} under bias stress.

Recent Approaches for Mitigating the H Issue

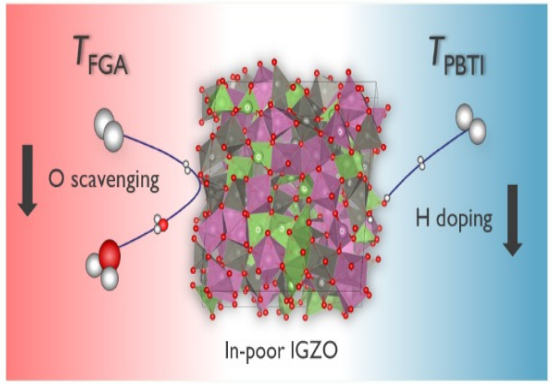
Channel Engineering

Post-dep. Plasma treatment



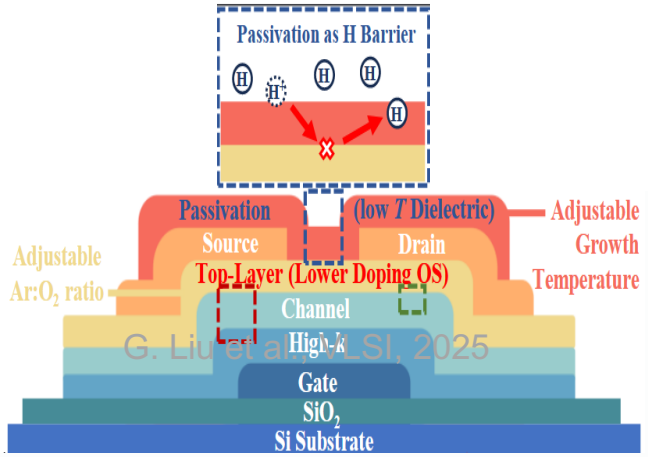
B. Tang et al., VLSI, 2025 (NUS)

Dopant modification



A. Kruv et al., ACS AEM, 2025 (imec)

Barrier Engineering

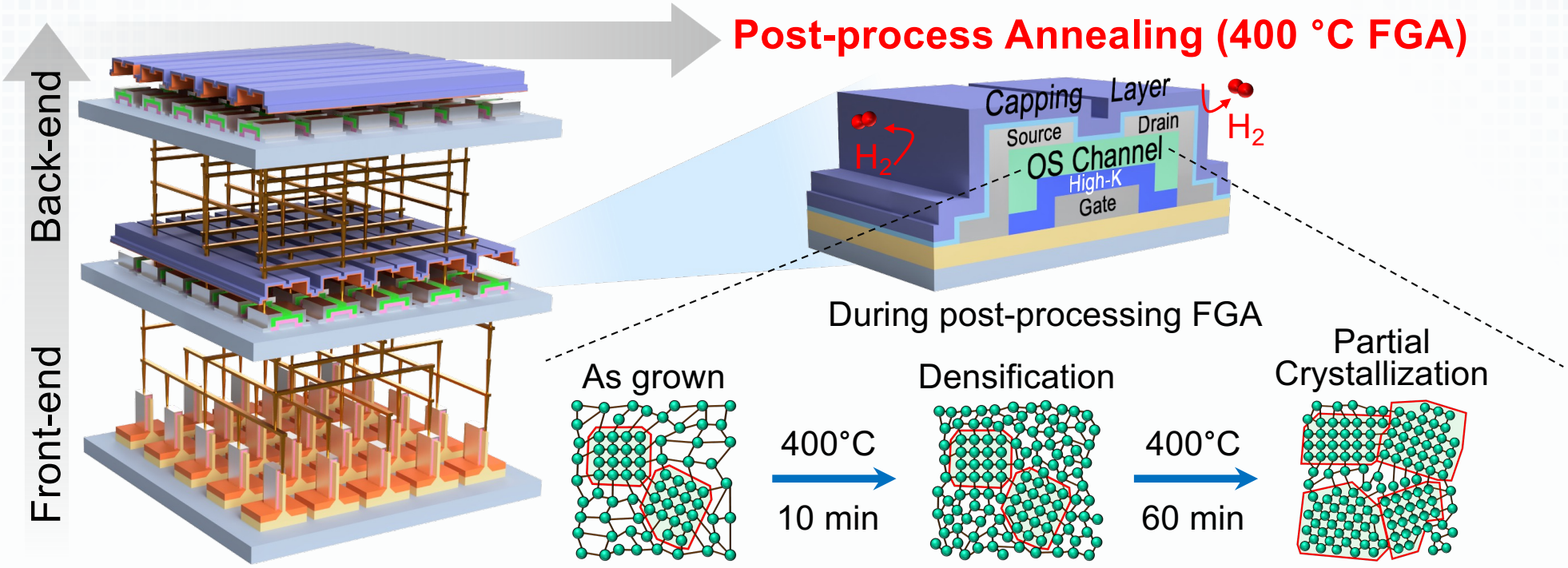


G. Liu et al., VLSI, 2025 (NUS)

Outline of this Talk

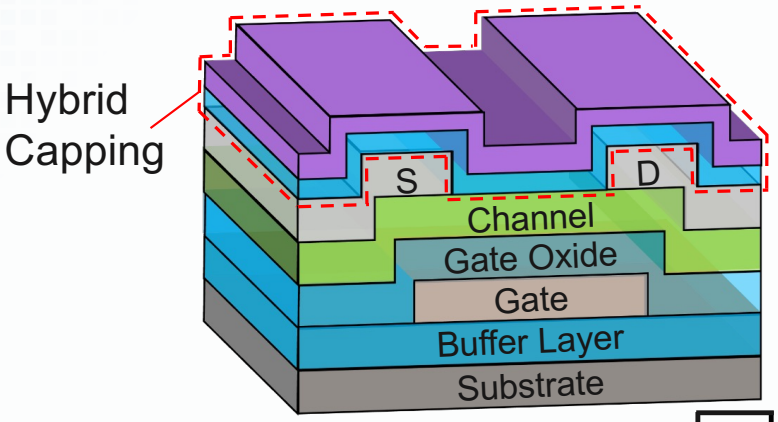
- M3D Integration with Oxide Transistors
- BEOL-Safe Oxide Transistor (FGA Immunity)
  - High-Level Achievement
  - ALD Process OS-TFT Device
  - Hybrid Capping Layer
- Deep Dive into Electrical Characteristics
- Unveil Defect Dynamic
- Key Takeaway & Conclusion

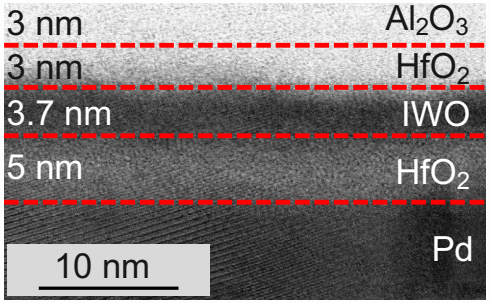
Highlights



- ❑ Hybrid capping maintains OS-TFT stability under 400 °C FGA.
- ❑ Combining experiments and modeling reveals how defects evolve during FGA.

ALD Process OS-TFT Device





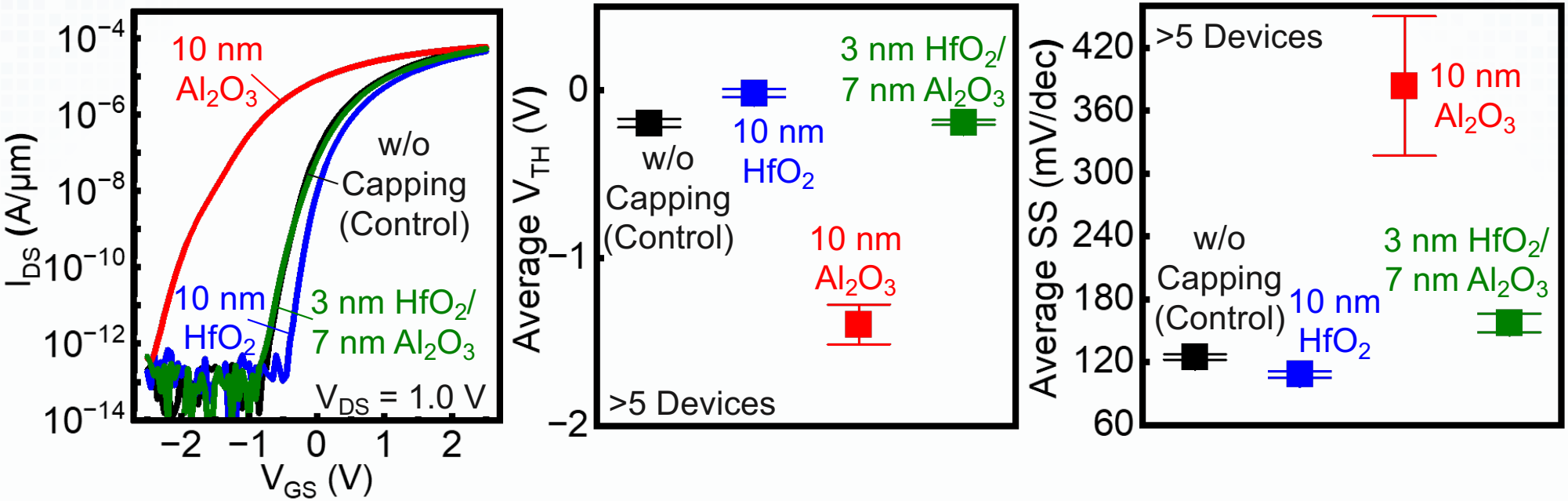
- Ti/Pd Bottom Gate (EBE, RT)
- 5 nm HfO_2 Gate Oxide (ALD, 250 °C)
- 3.7 nm IWO Channel (ALD, 250 °C)
- Channel Etching (ICP, RT)
- PDA (400 °C, O_2, 10 min)

- Pd S&D Contact (EBE, RT)
- PMA (250 °C, O_2, 10 min)
- Hybrid Capping: 3 nm HfO_2/3 nm Al_2O_3 (ALD, 250 °C)
- Post-Processing FGA (400 °C, 10~60 min)

Channel Dimension: W_{ch} = 10 μm/L_{ch} = 1 μm FGA: 4% H_2/96% N_2

Proposed Hybrid Capping Layer

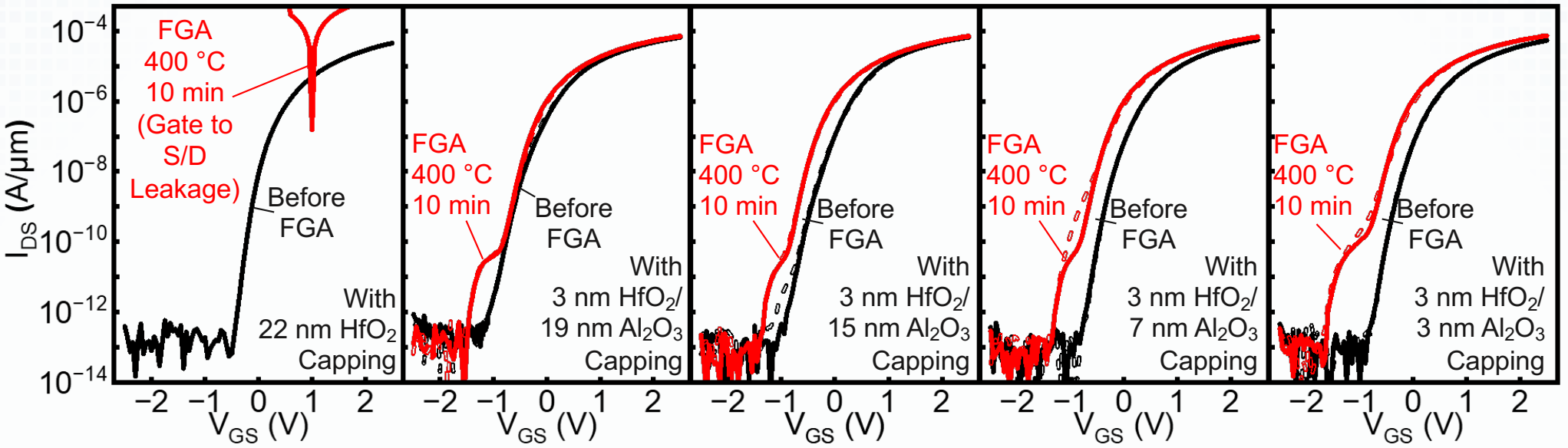
Role of HfO_2 Interlayer: Mitigate Post-Capping Degradation



Direct Al_2O_3 deposition induces severe post-capping degradation, whereas an HfO_2 interlayer prevents V_{TH} shift and SS degradation.

Proposed Hybrid Capping Layer

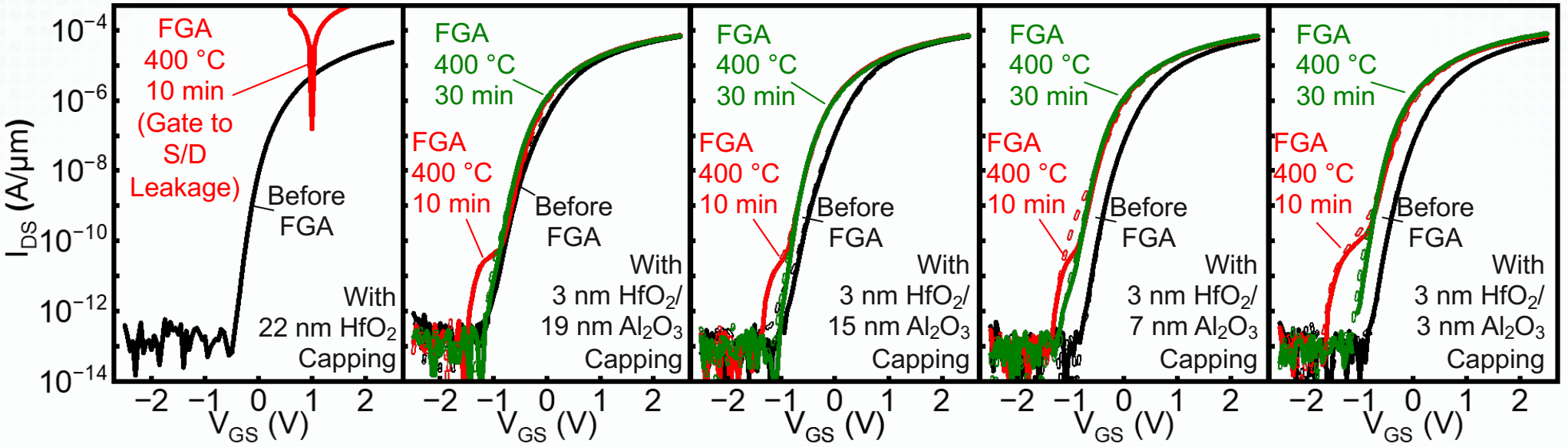
Role of Al_2O_3: Superior H Blocking Capability



HfO_2 alone cannot effectively block H. In contrast, replacing the top layer with Al_2O_3 provides strong H-blocking even at a scaled thickness of 3 nm.

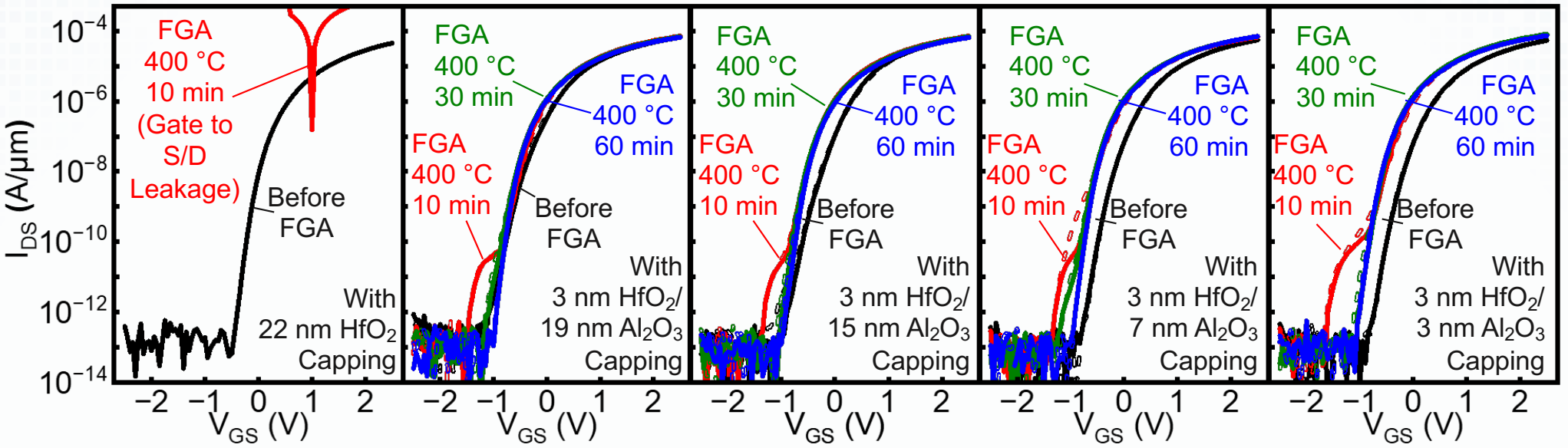
Proposed Hybrid Capping Layer

Role of Al_2O_3: Superior H Blocking Capability



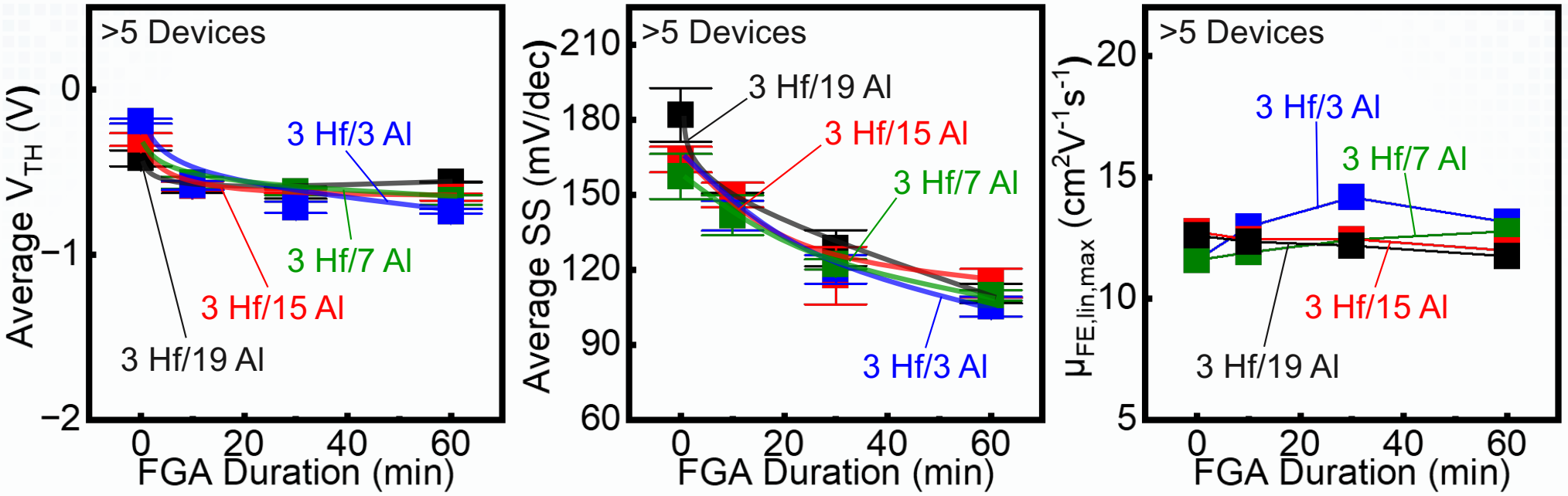
Proposed Hybrid Capping Layer

Role of Al_2O_3: Superior H Blocking Capability



V_{TH} remains stable after up to 60 min of FGA with the optimized 3 nm HfO_2 / 3 nm Al_2O_3 hybrid capping layer.

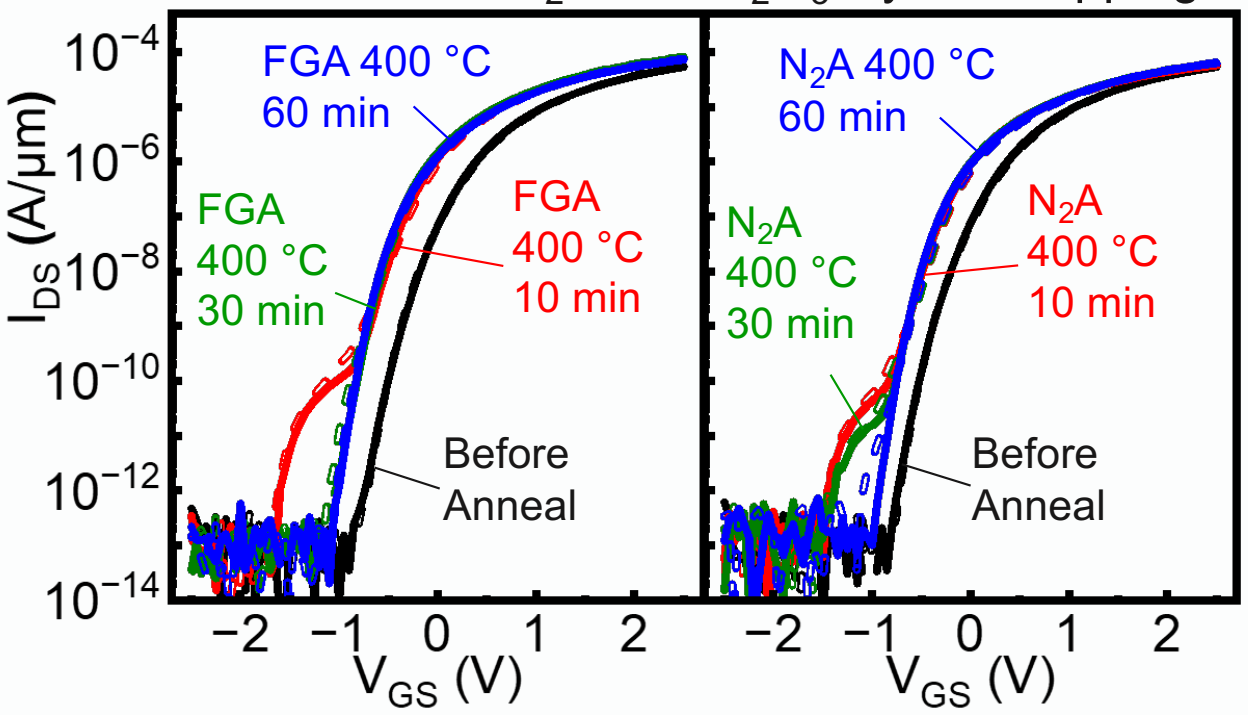
Proposed Hybrid Capping Layer



Stable V_{TH} and consistent SS improvement are observed across different Al_2O_3 thicknesses under prolonged FGA, with minimal impact on carrier scattering.

Proposed Hybrid Capping Layer (H Immunity)

With 3 nm HfO_2/3 nm Al_2O_3 Hybrid Capping



FGA: 4% H_2/96% N_2

N_2A: 100% N_2

H immunity is confirmed by comparing FGA and pure N_2 annealing at the same temperature.

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- Deep Dive into Electrical Characteristics
  - Phenomenon: Origin & Suppression of “Kink”
  - Reliability: Evolution of NBTI & PBTI during FGA
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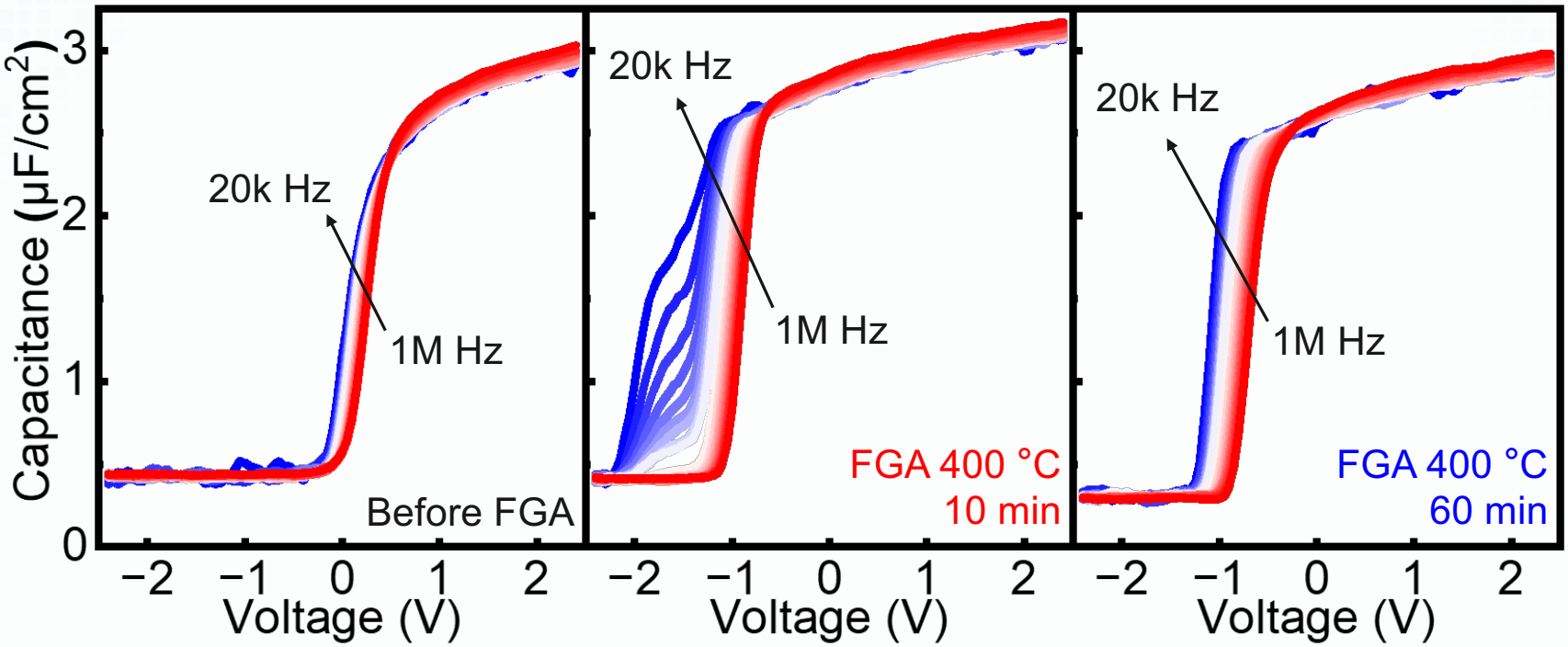
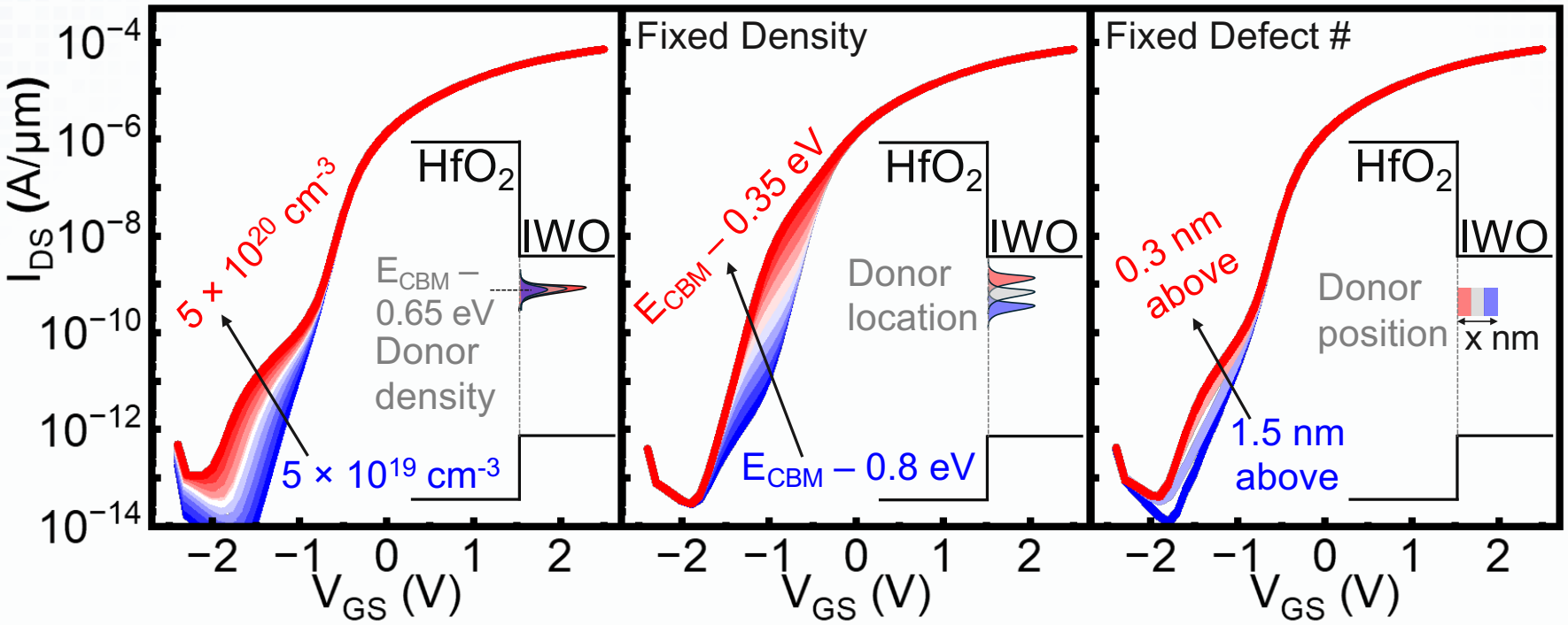
Phenomenon: Origin & Suppression of “Kink”



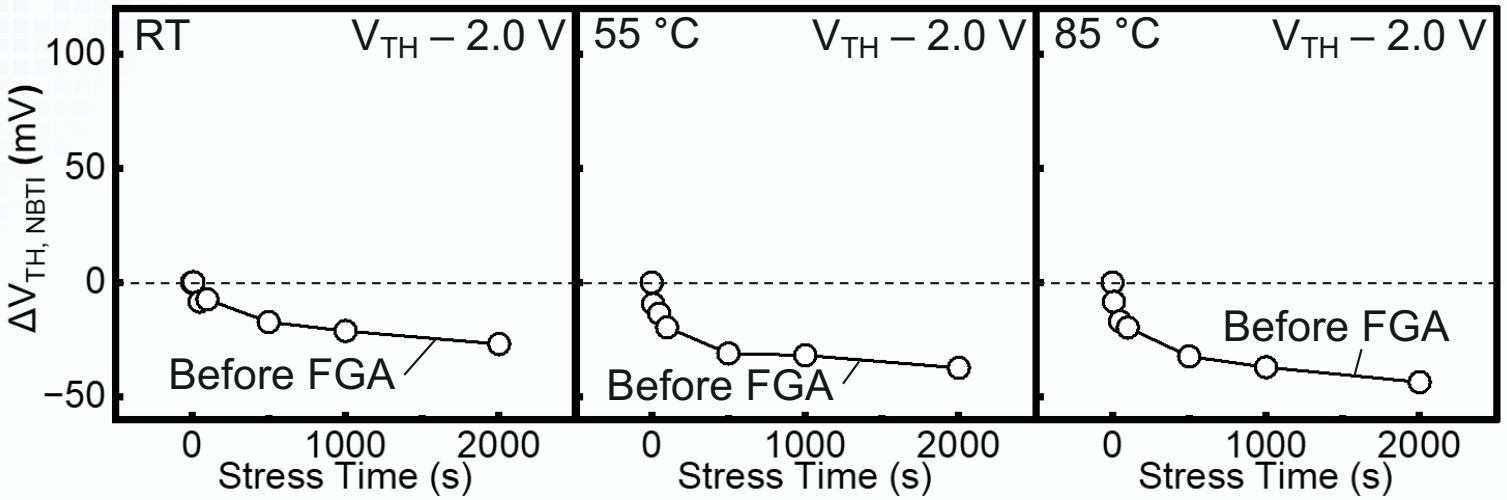
A transient “kink” emerges at 10-min anneal and vanishes with longer annealing → Indicating involvement of intermediate defect states.

TCAD Simulation for “Kink” (Ginestra™)

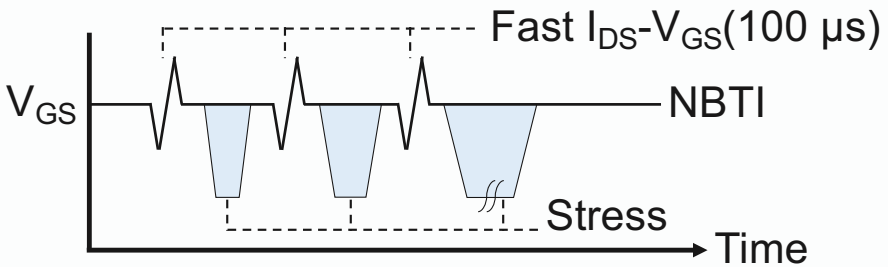


Simulations confirm the 10-min FGA “kink” originates from increased shallow interface traps.

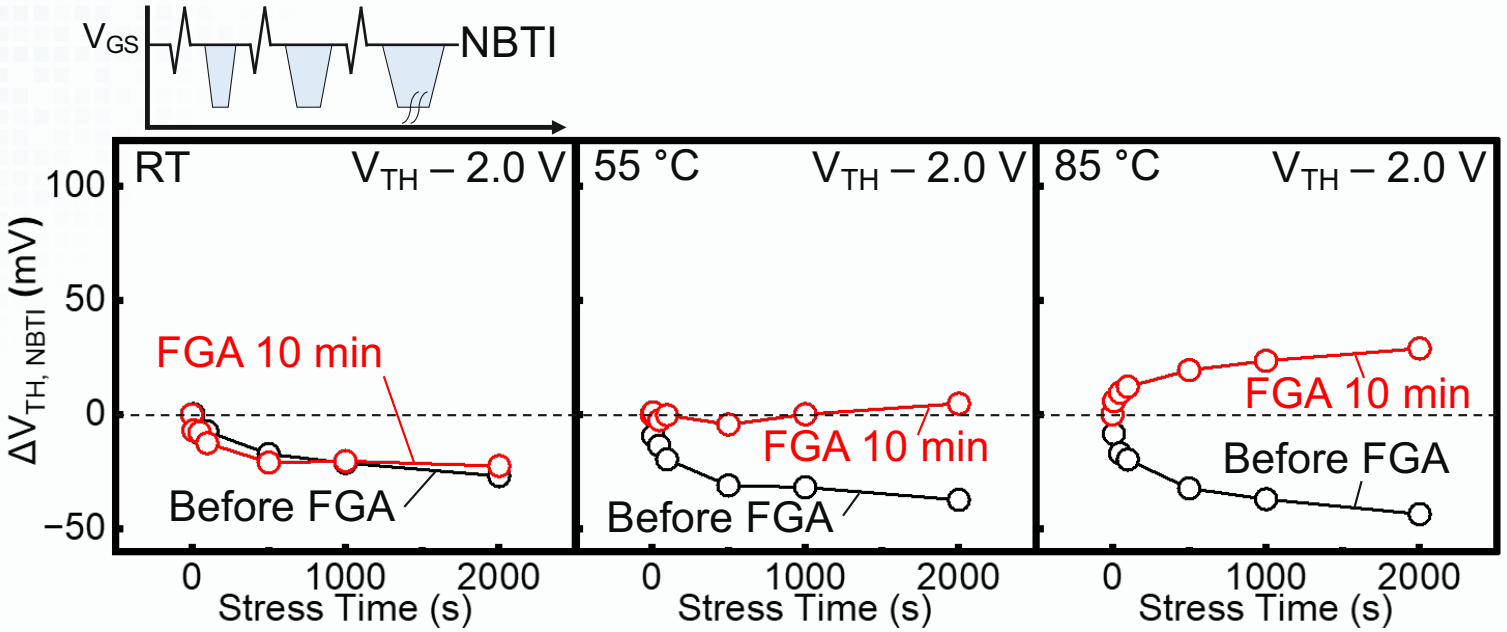
Reliability: Evolution of NBTI during FGA



V_O ionization
$Vo=Vo^{2+}+2e^-$

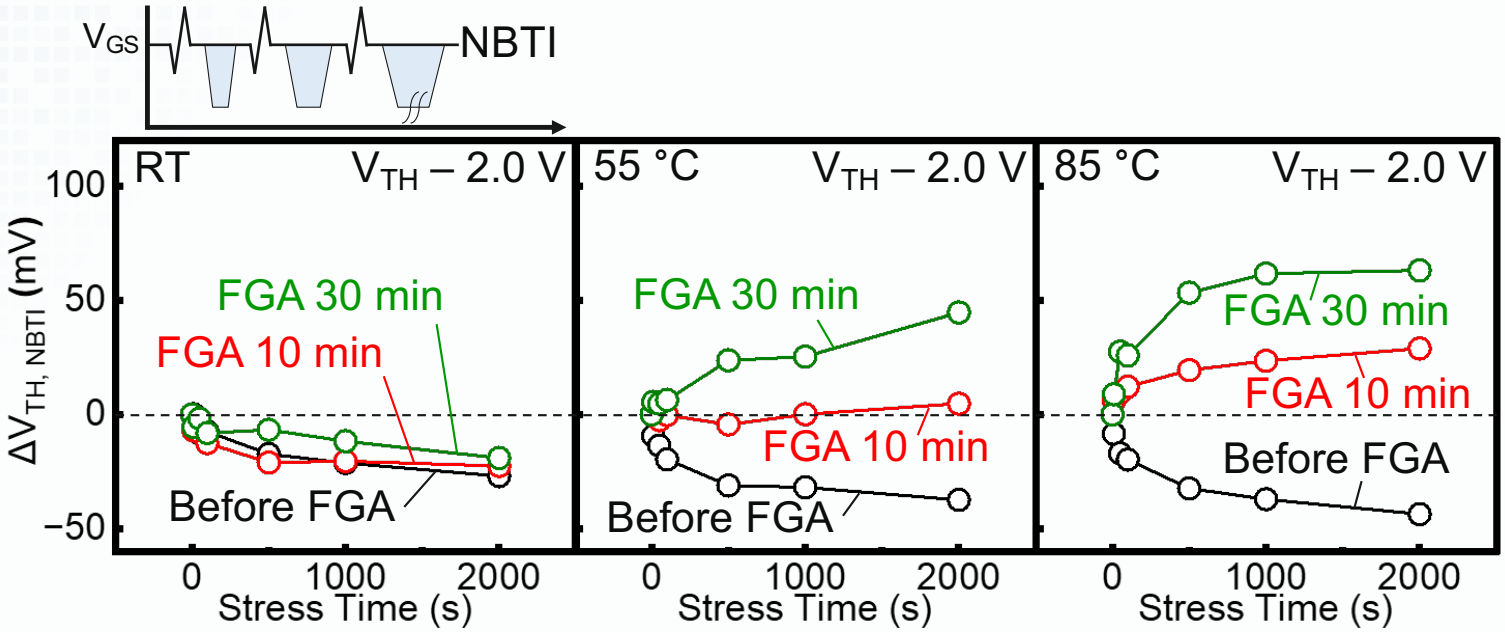


Reliability: Evolution of NBTI during FGA

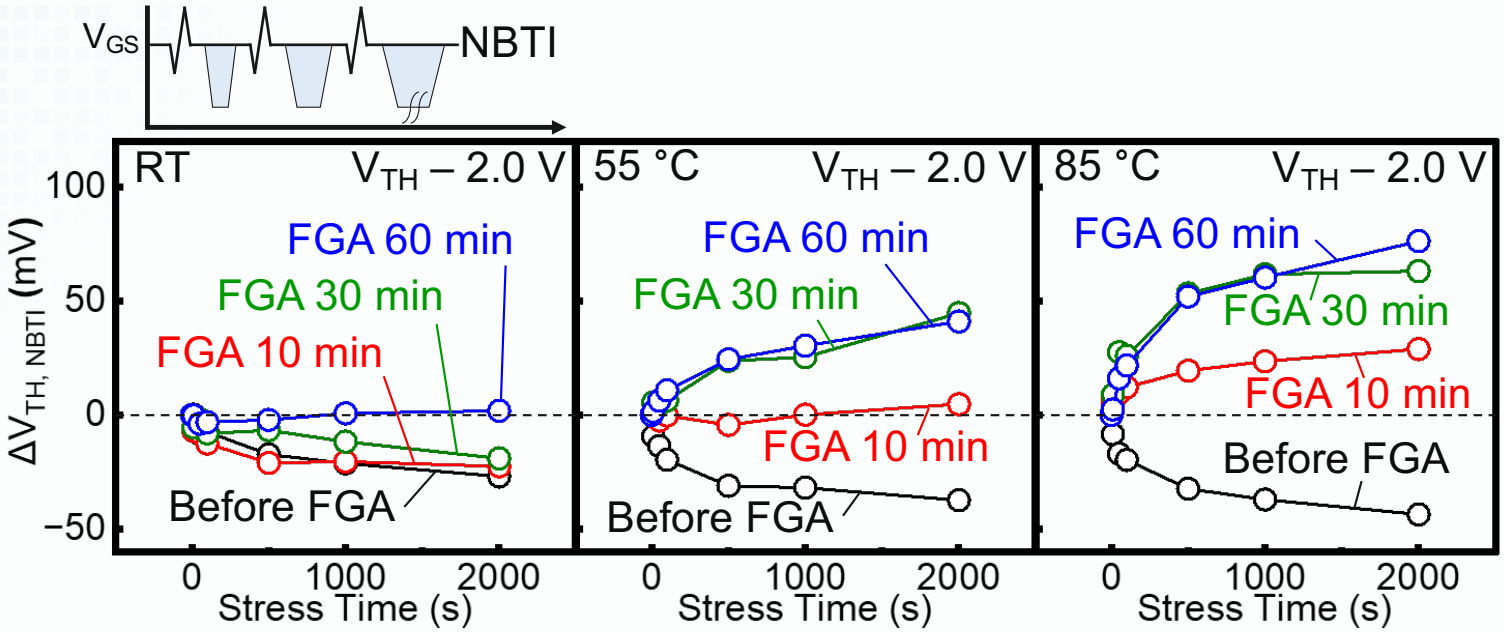


FGA induces a ΔV_{TH} polarity reversal, which becomes more pronounced at elevated temperatures.

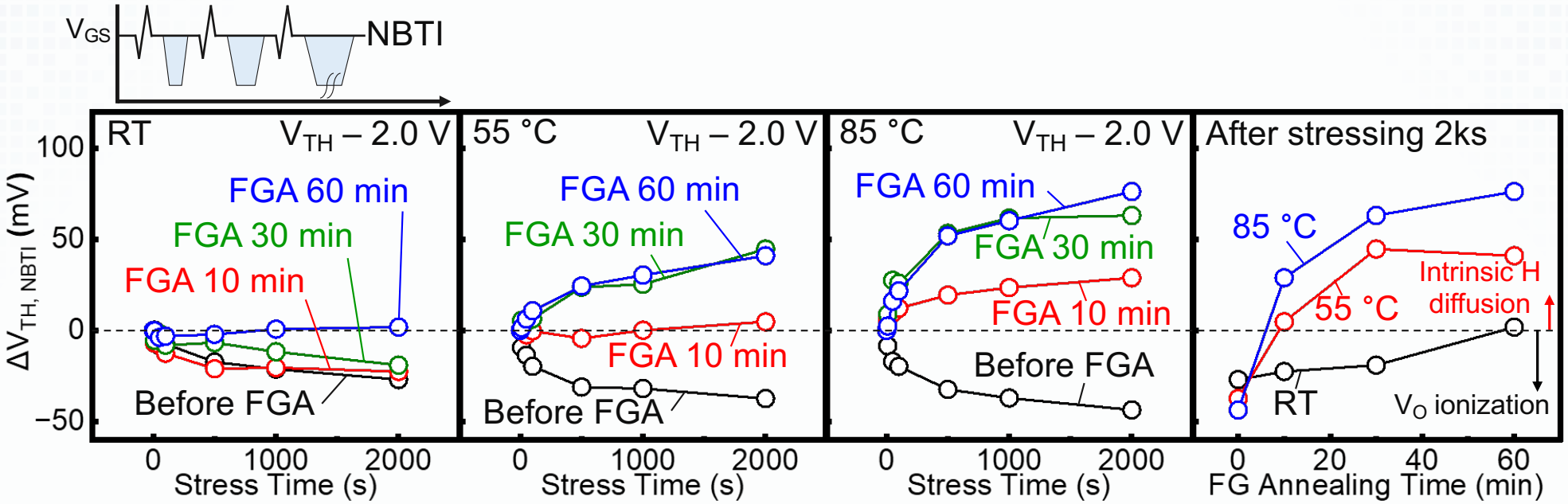
Reliability: Evolution of NBTI during FGA



Reliability: Evolution of NBTI during FGA

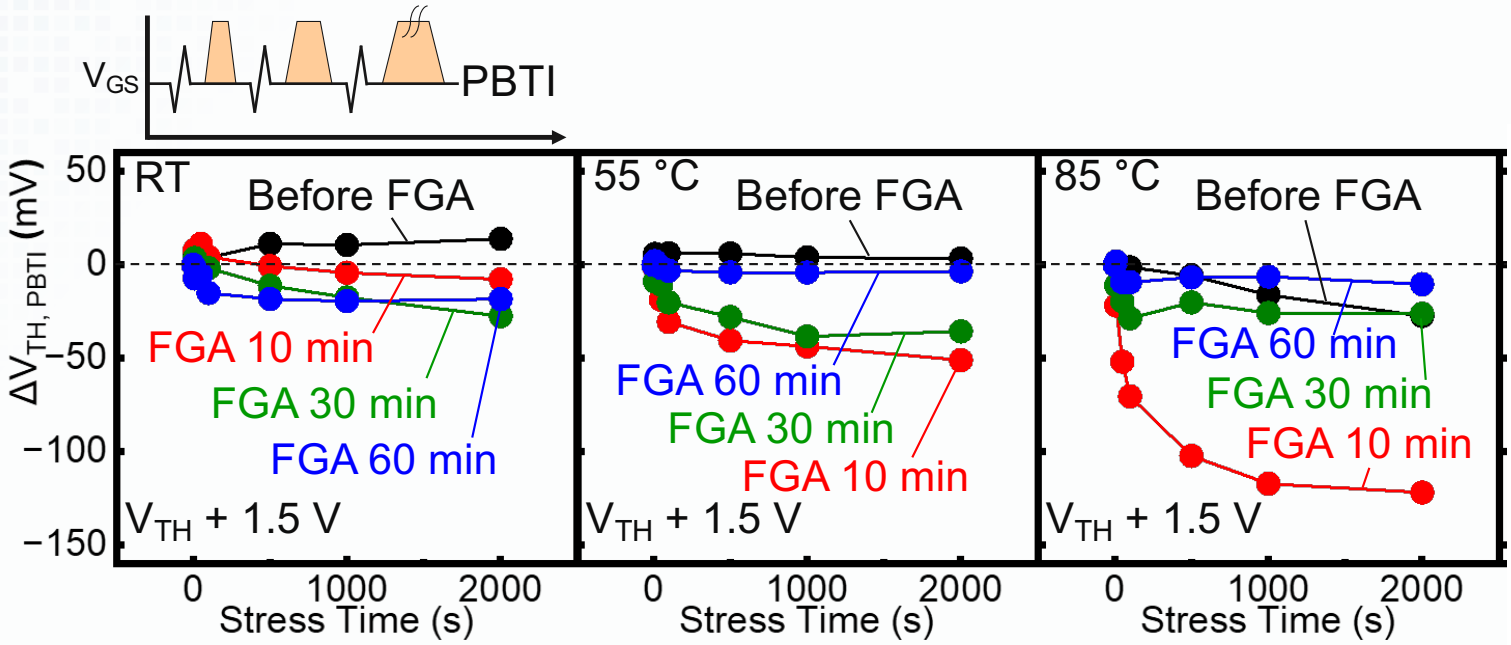


Reliability: Evolution of NBTI during FGA

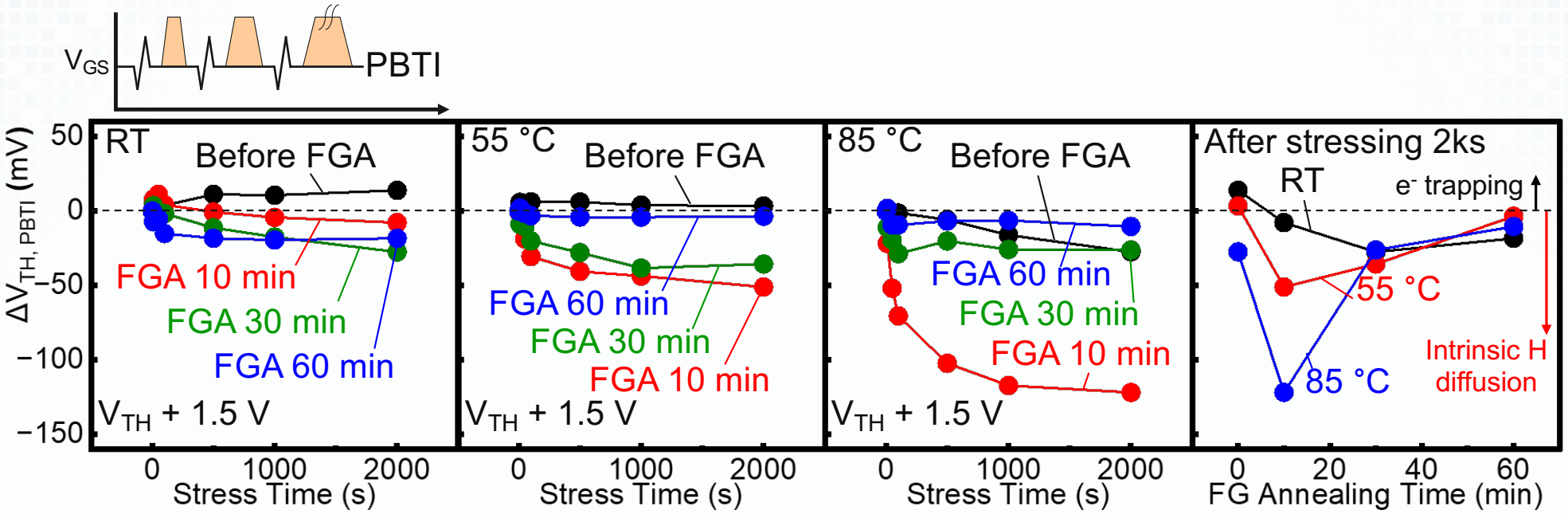


ΔV_{TH} polarity reversal after prolonged FGA originates from intrinsic H diffusion from Pd contacts (high H catalytic activity).

Reliability: Evolution of PBTI during FGA

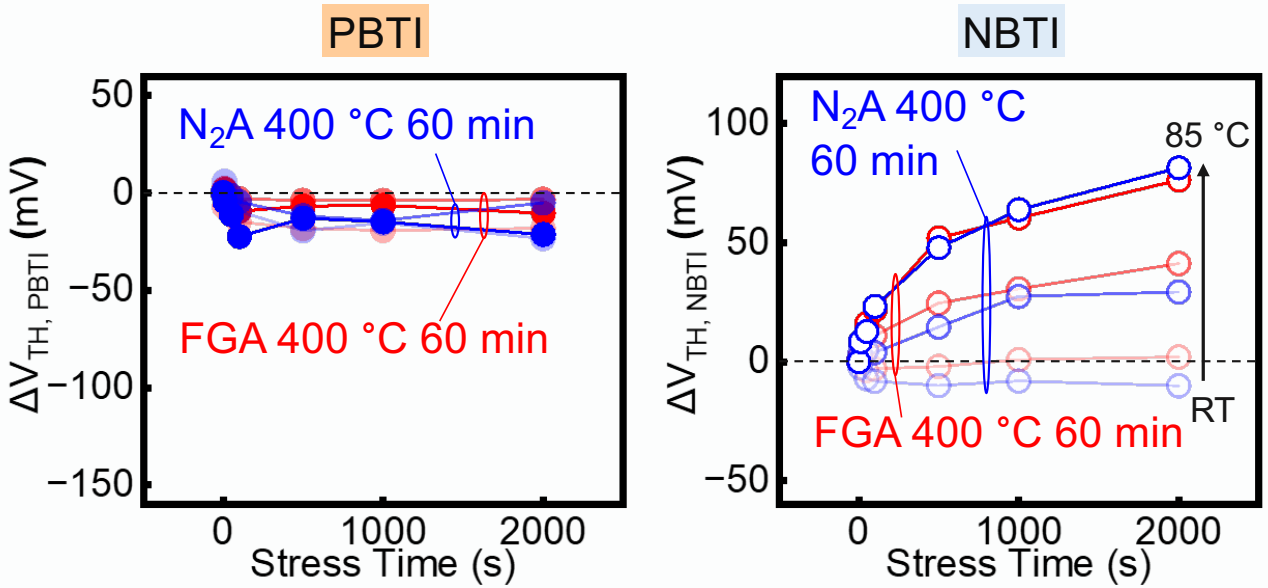


Reliability: Evolution of PBTI during FGA



Reduced $-\Delta V_{TH}$ under PBTI from 10 → 60 min anneal arises as partial crystallization traps H in deep In–OH/In–In complexes, limiting its motion.

Reliability: Comparing FGA & N_2A



BTI trends under FG and pure N_2 anneals confirm limited ambient hydrogen impact.

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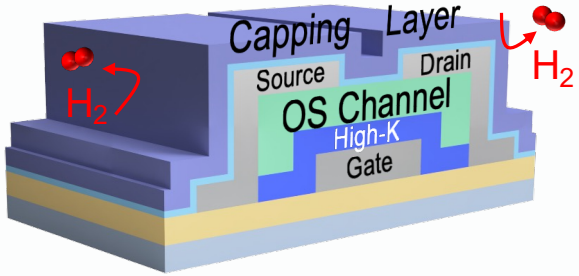
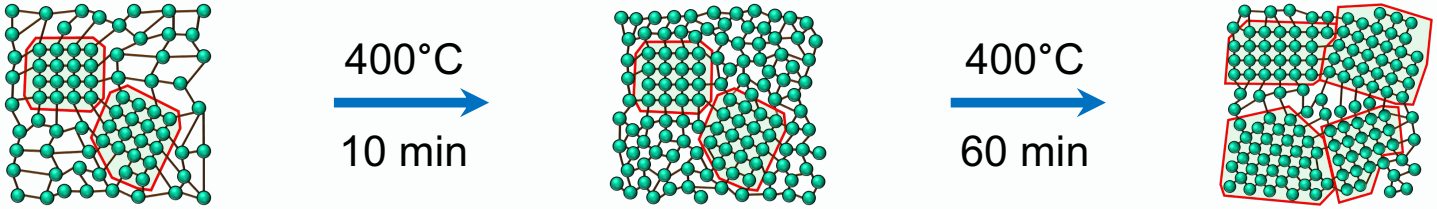
- Unveiling Defect Dynamics
  - 2-Stage of Defect Dynamics
  - Propose BTI Mechanisms During FGA
- Ongoing Progress

2-Stage of Defect Dynamics



During Post-Processing FGA (400 °C)

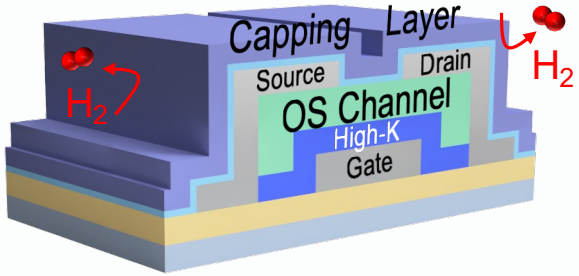


As grown

Stage I: Densification

Stage II: Partial Crystallization

2-Stage of Defect Dynamics



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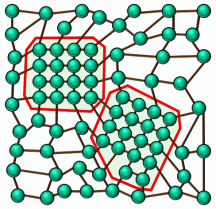
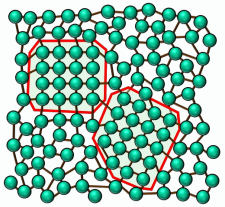


As grown

400°C

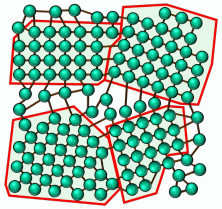
10 min



Stage I:
Densification

400°C

60 min

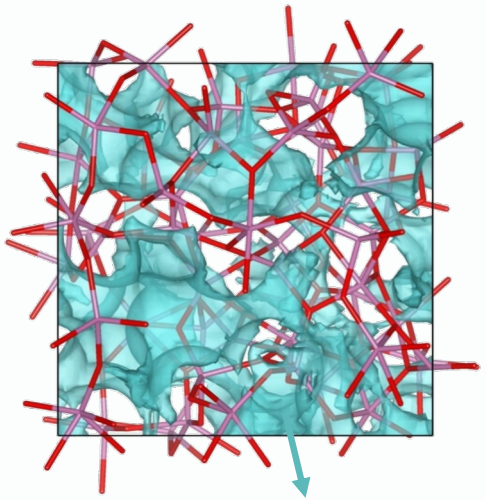


Stage II:
Partial
Crystallization

Stage I: Densification in a-InO

Low density

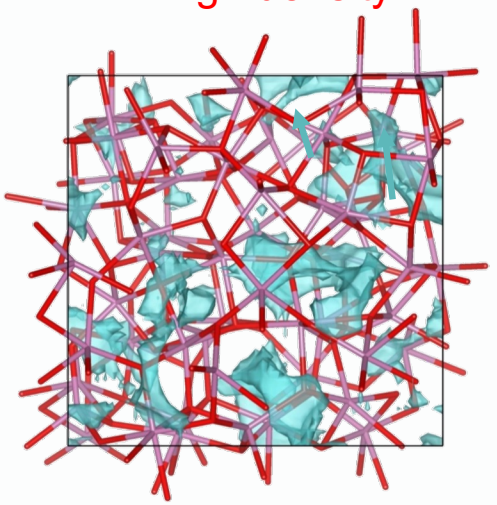
Density:
ρ=6.6 g/cm^3



Void vol. 9.1%
(3-coordinated O atoms)

High density

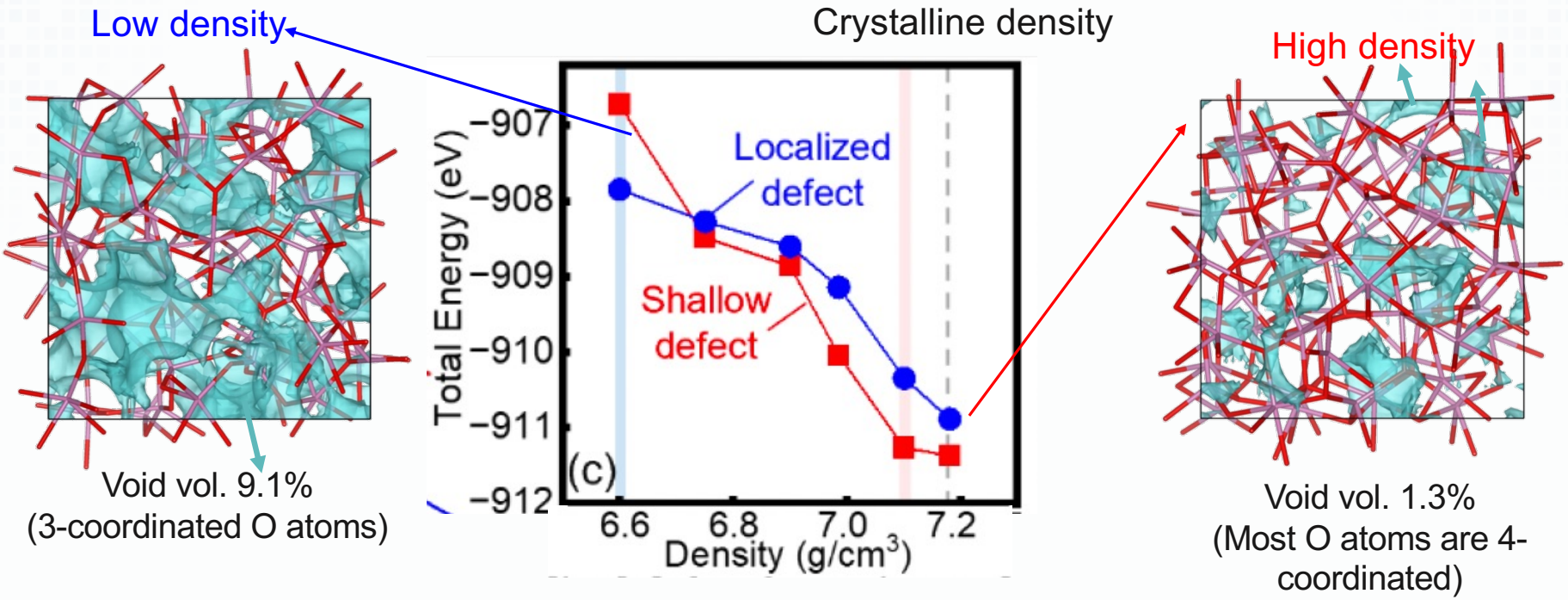
Density:
ρ=7.1 g/cm^3



Void vol. 1.3%
(Most O atoms are 4-coordinated)

Low-density a-InO forms deep/localized trap states; densification yields shallow states and increase carrier.

Stage I: Densification in a-InO

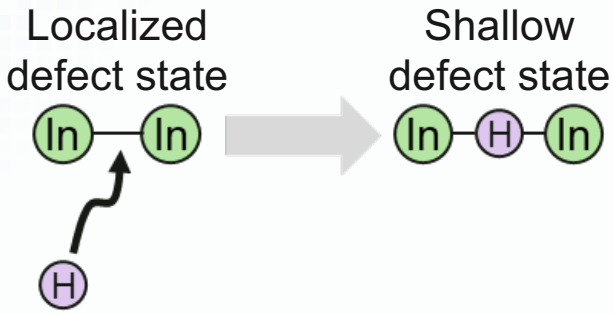


Low-density a-InO forms deep/localized trap states; densification yields shallow states and increase carrier.

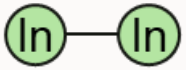
In collaboration with Dr. Julia Medvedeva, Missouri University of Science & Technology, USA

Impact of H: 2 Types of Hydrogen-Related Defects

In–H–In: Intrinsic H passivates In–In pairs, forming shallow In–H–In states.



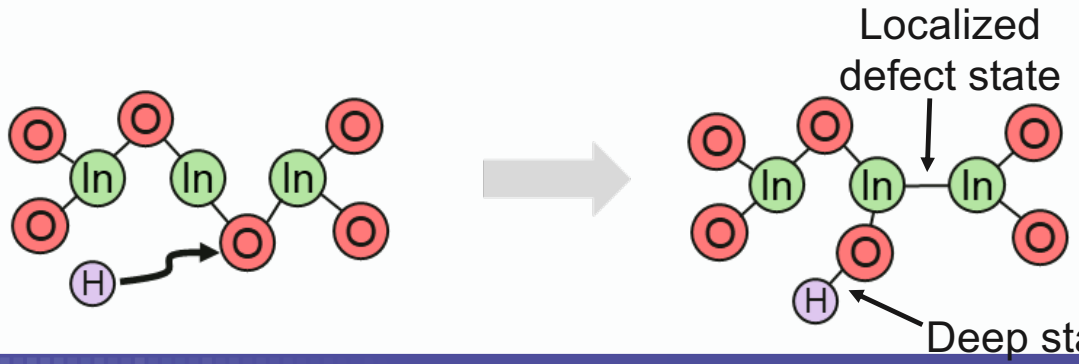
In-In Metallic Bond (localized e⁻ traps):

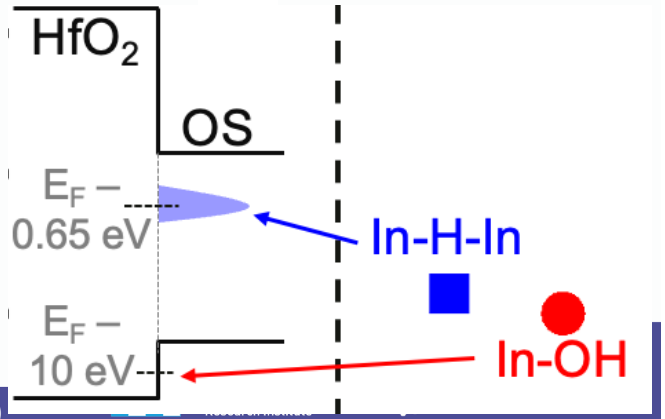


In-H-In (Shallow/Delocalized e⁻ donor):

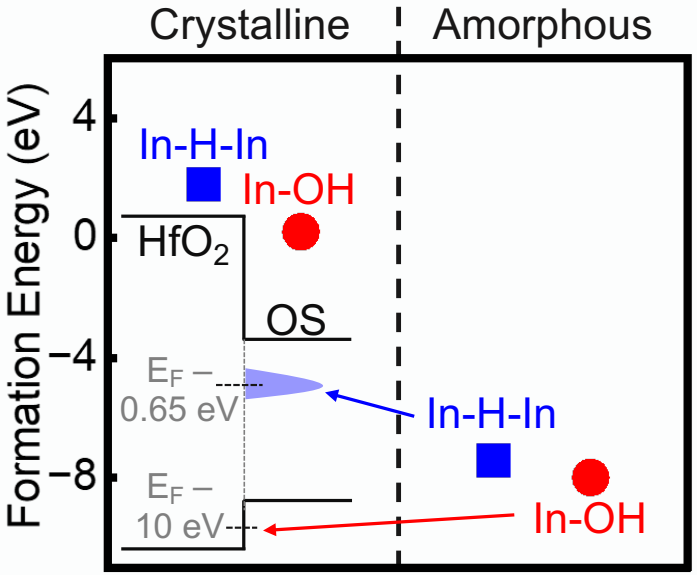
Covalent OH (Very Deep State):

In–OH: H bonds with O, leaving adjacent In–In deep localized traps, preferentially at the c/a interface.



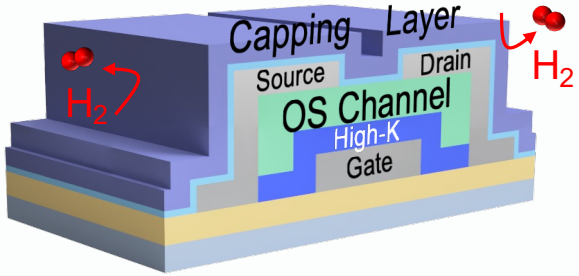


Impact of H: 2 Types of Hydrogen-Related Defects

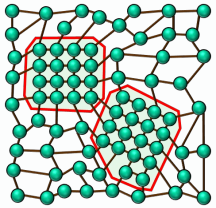


Both types of H-related defects have lower formation energy in the amorphous regions, indicating that hydrogen incorporation is more favorable there.

2-Stage of Defect Dynamics



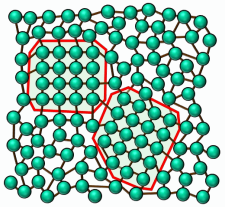
During Post-Processing FGA (400 °C)



As grown

400°C

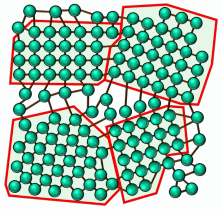
10 min



Stage I:
Densification

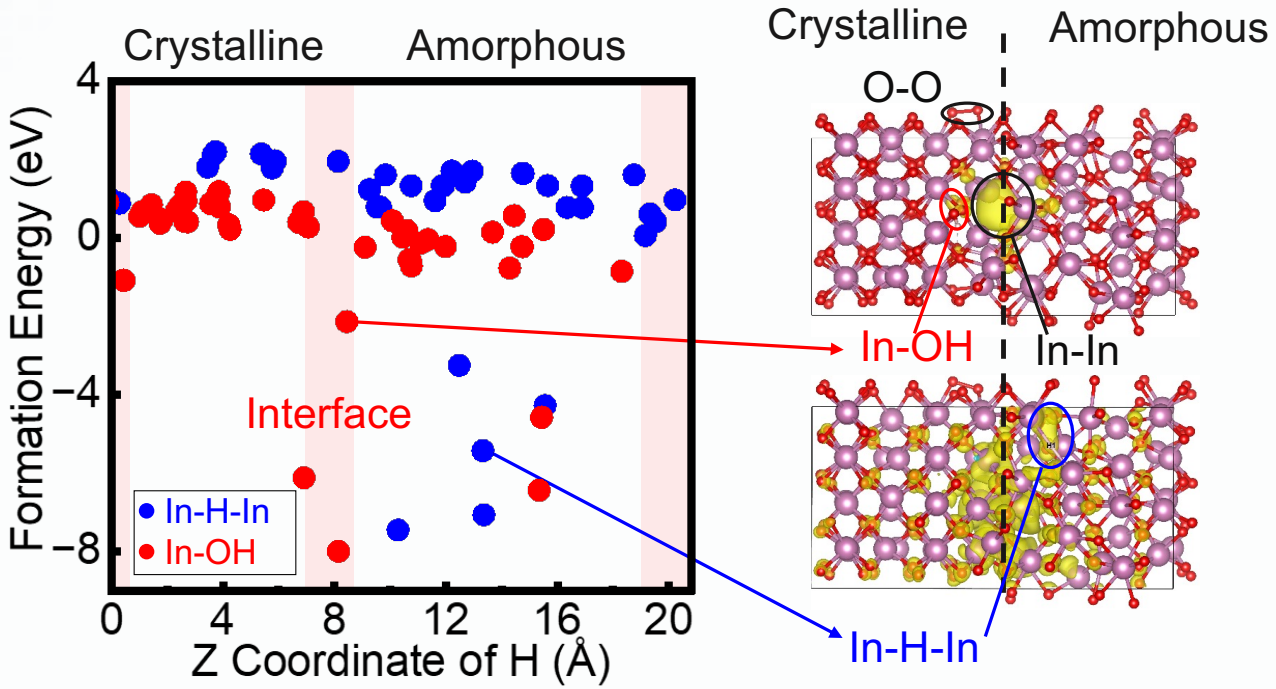
400°C

60 min



Stage II:
Partial
Crystallization

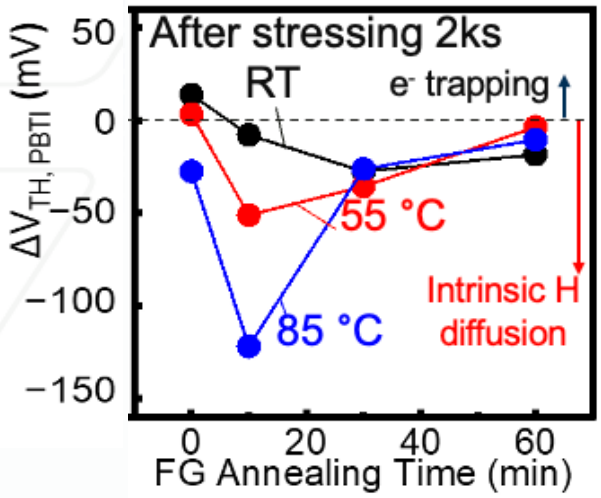
Stage II: Intrinsic H Impact at c/a Interface



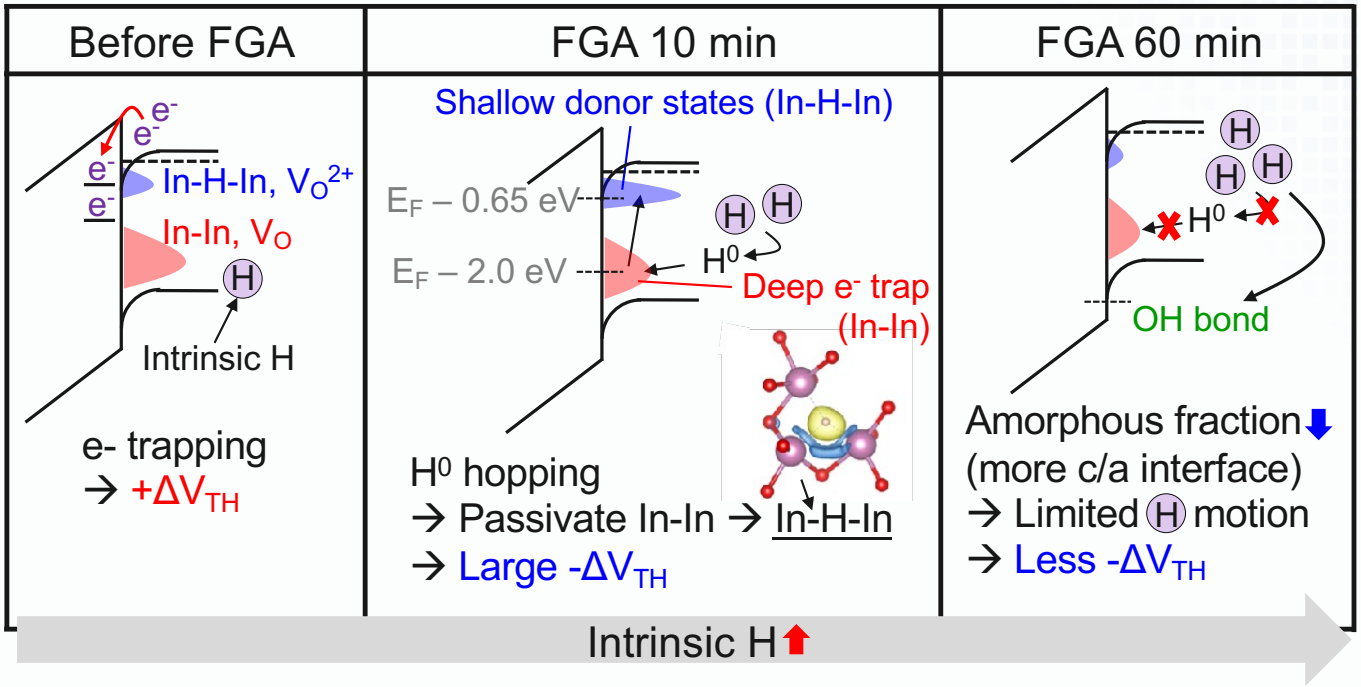
- In–H–In: Intrinsic H passivates In–In pairs, forming shallow In–H–In states.
- In–OH: H bonds with O, leaving adjacent In–In deep localized traps—preferentially at the c/a interface.

In collaboration with Dr. Julia Medvedeva, Missouri University of Science & Technology, USA

Propose BTI Mechanisms During FGA (PBTI)

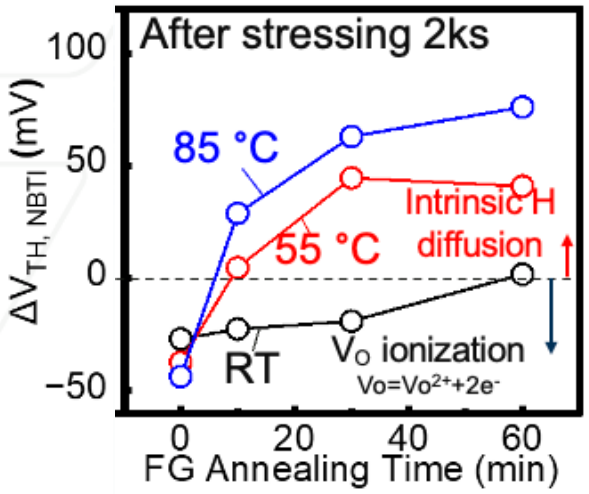


BG Charge State		-	0	+
Fraction of stable In-OH		2 %	27 %	35 %
# of H hops during 2ps at 300 K	In ←→ In	7742	2765	766
	In → O	267	77	6
	O → O	562	792	884



During PBS, H^-/H^0 passivates deep In–In traps, forming shallow In–H–In donors that increase carrier density and cause $-\Delta V_{TH}$.

Propose BTI Mechanisms During FGA (NBTI)



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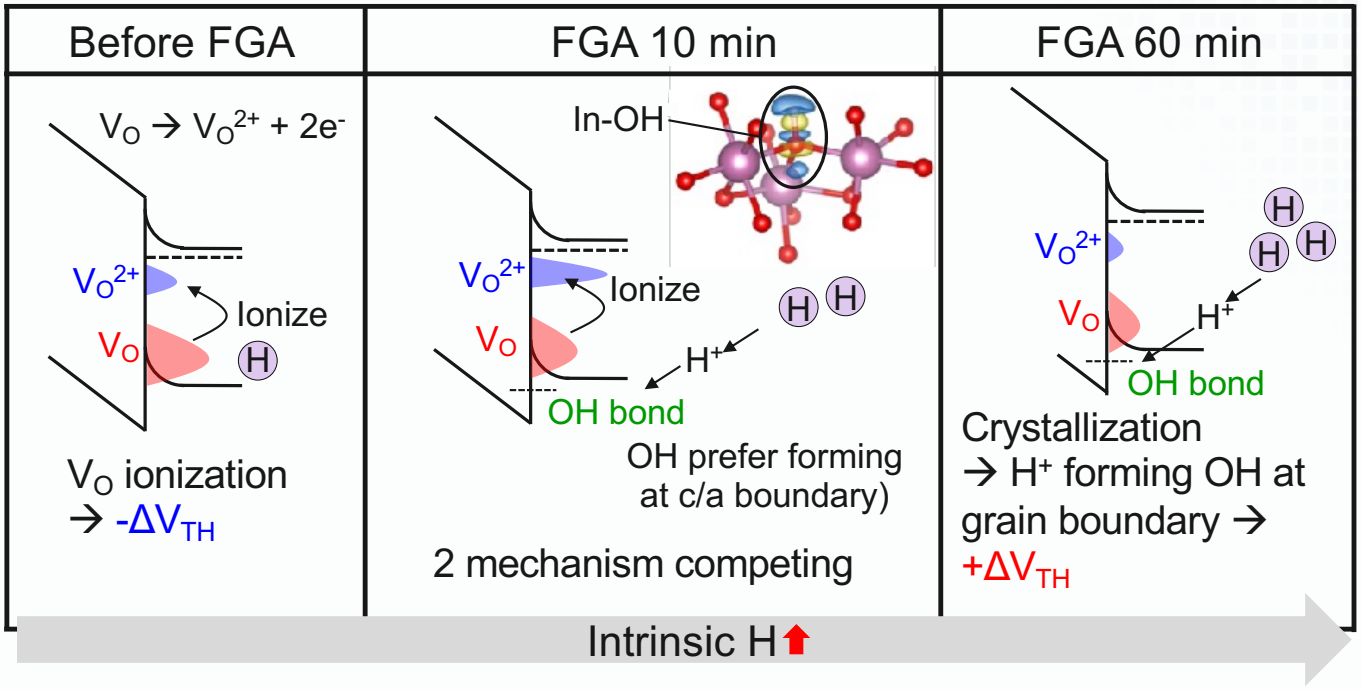


During NBS, H^+ forms covalent O–H bonds, creating new In–In traps, reducing carrier density, and inducing $+\Delta V_{TH}$.

Outline of this Talk

- M3D Integration with Oxide Transistors
- BEOL-Safe Oxide Transistor (FGA Immunity)
- Deep Dive into Electrical Characteristics
- Unveil Defect Dynamic
- Key Takeaway & Conclusion

Key Takeaway & Conclusion

1. A robust strategy (hybrid capping) for maintaining oxide TFTs performance under 400 °C post-processing FGA up to 60 mins.

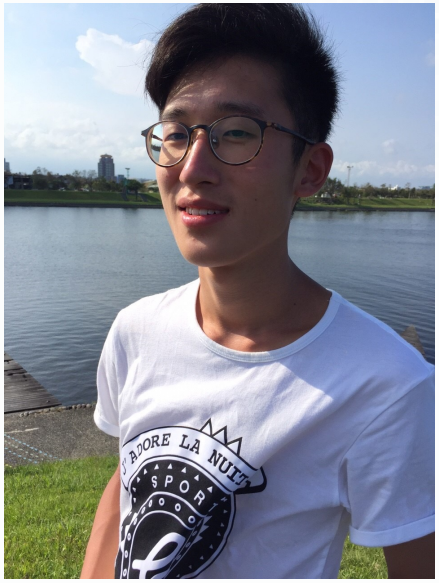
2. Deep insights into the resulting electrical characteristics under 400 °C post-processing FGA:
(1) “Kink” evolution and (2) BTI trend.

3. A 2-stage defect transformation process through DFT modeling (densification and partial crystallization).

4. Comprehensive BTI mechanism revealed through combined experimental and theoretical analysis during post-FGA.

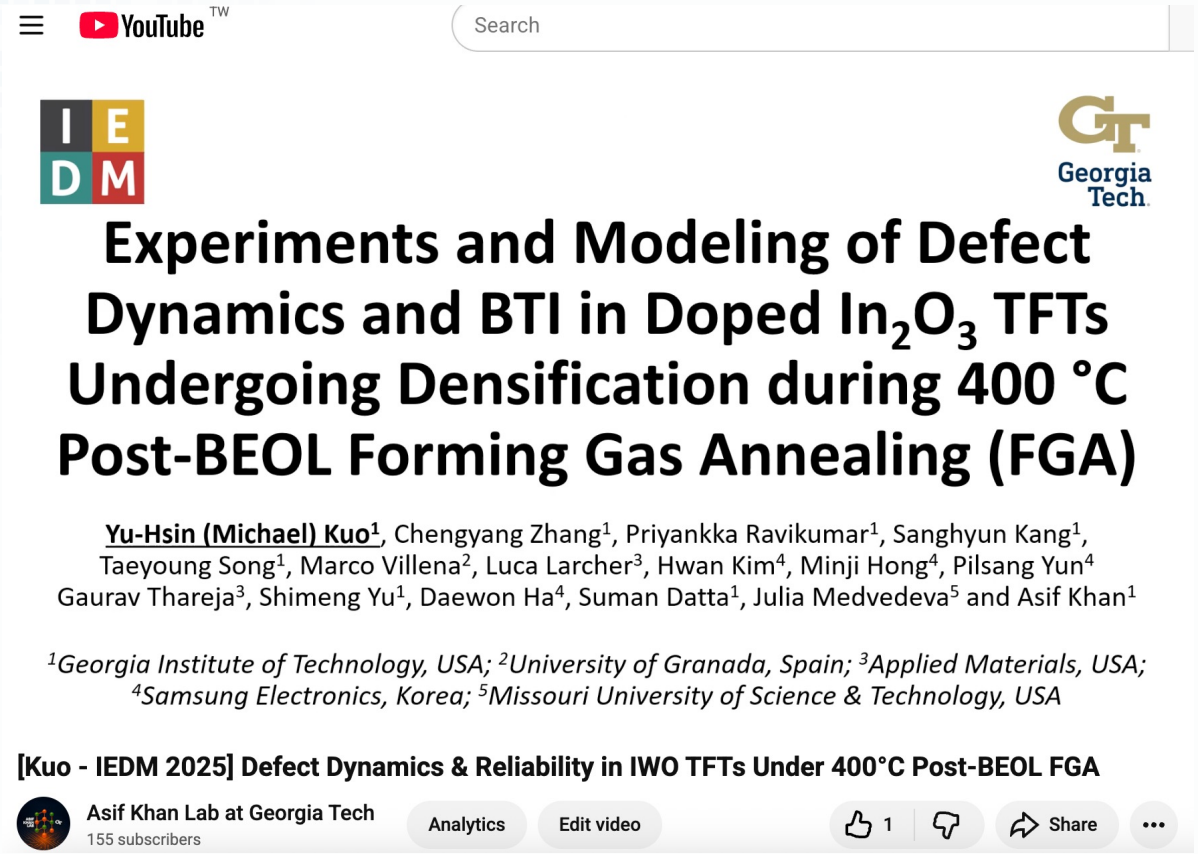
Summary

- Kuo, Y-H., et al. "Experiments and Modeling of Defect Dynamics and BTI in Doped In 2 O 3 TFTs Undergoing Densification during 400° C Post-BEOL Forming Gas Annealing (FGA)." *2025 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2025.
- Kuo, Yu-Hsin, et al. "Experiments and Modeling of Defect Dynamics and BTI Behavior in Doped InO TFTs During 400° C Postprocessing Forming Gas Annealing." *IEEE Transactions on Electron Devices* (2026).



Yu-Hsin (Michael) Kuo
3rd Year PhD Student

Summary



https://www.youtube.com/watch?v=Fkx-8-vo5zY

Acknowledgment

Thanks to SRC-GRC-NMP program, Samsung Electronics, DOE, & NSF.

Thank you for your attention