Ferroelectric NAND Flash: Scaling Storage for AI era

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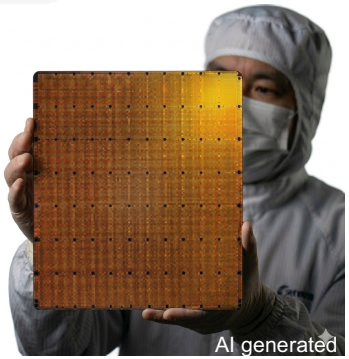
Foundational Memory & Storage Technologies

1 SRAM



Cerebras WSE-3

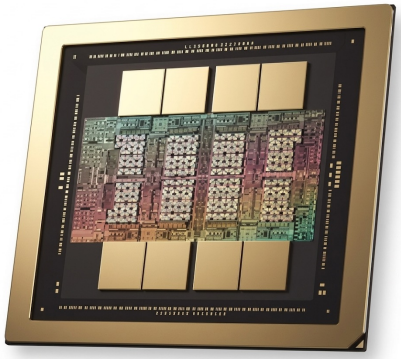
CAPACITY

44 GB

BANDWIDTH

21 PB/s

2 DRAM and High Bandwidth Memory



NVIDIA Rubin

CAPACITY

288 GB

BANDWIDTH

22 TB/s

3 NAND Flash Storage

CAPACITY

30 – 245 TB

BANDWIDTH

~14 GB/s

4 Magnetic Hard Drives

CAPACITY

24 – 44 TB

BANDWIDTH

~300 MB/s

← faster, smaller | larger, slower →

Every AI system rides on this hierarchy.

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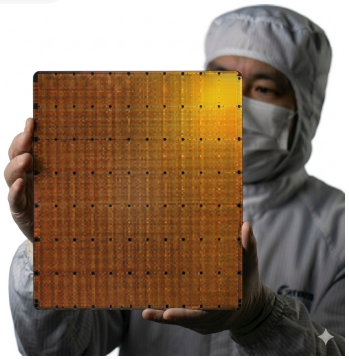

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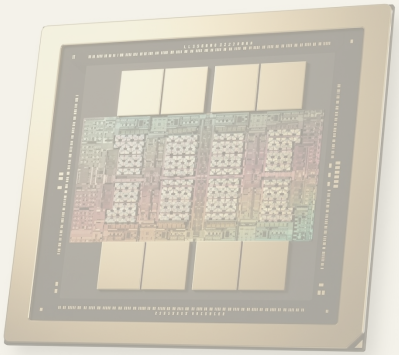

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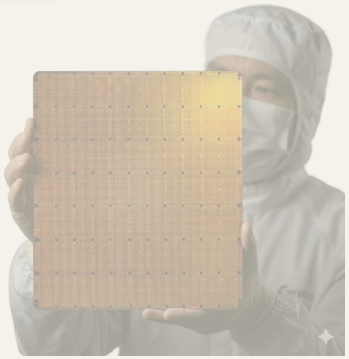

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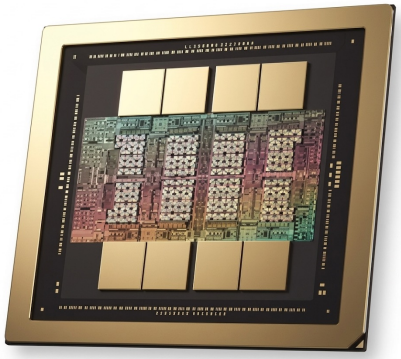

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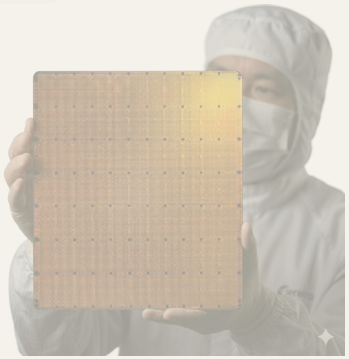

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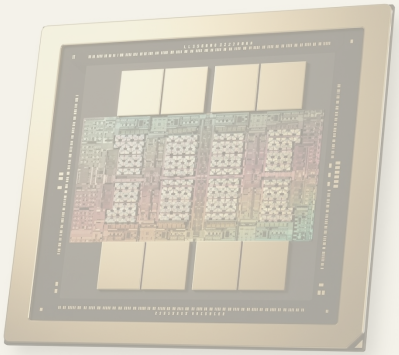

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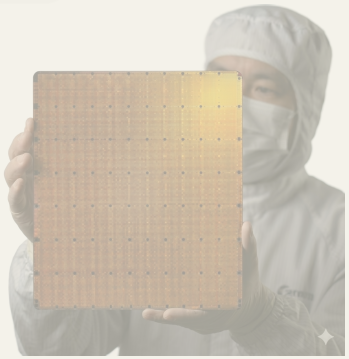

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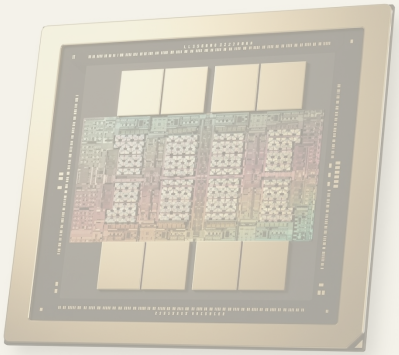

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Why NAND Flash Matters for AI

1

AI's appetite for data is exploding

10s of PB

TRAINING DATA

- Training datasets: PB-scale per frontier model
- Checkpoints: TBs written every few hours
- RAG vector databases: billions of embeddings

Storage demand ~doubling per year

2

NAND has overtaken HDD on every metric

~50×

BANDWIDTH vs HDD

- Capacity: 245 TB SSD vs 44 TB HDD
- Bandwidth: 14 GB/s vs 300 MB/s
- Density: 2.5 PB/2U vs ~30 TB/2U

One SSD replaces eight HDDs

3

NAND is climbing the memory hierarchy

Active

MEMORY TIER

- KV cache offload for long-context inference
- Parameter streaming during training
- Disaggregated memory tiers via CXL: CXL-attached SSD pools sit between HBM and bulk storage, creating an entirely new memory tier

From cold storage to working memory

NAND is no longer where the data sleeps.
It's increasingly part of where the AI thinks.

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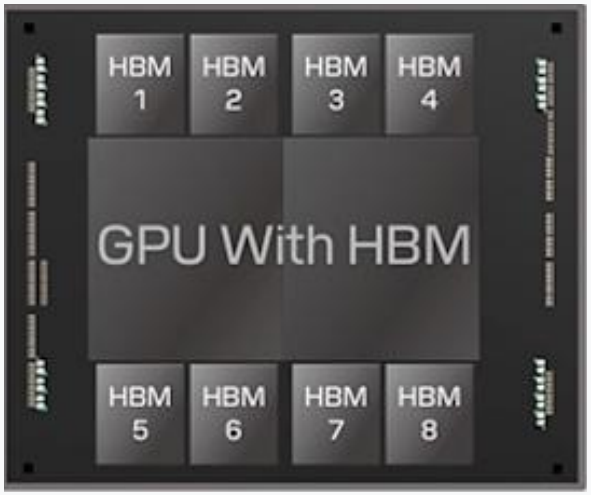
What if NAND moved on Package?

High Bandwidth Flash (HBF) stacks NAND in the HBM form factor — bulk capacity, right next to compute

GPU + HBM



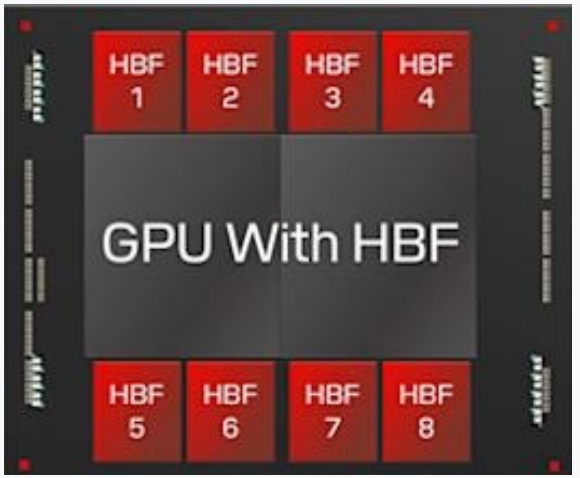
192 GB

TOTAL ON-PACKAGE MEMORY

~8 TB/s · Shipping today (B200)

~21×

GPU + HBF



4,096 GB

TOTAL ON-PACKAGE MEMORY

TB/s class · In development

Concept and figure inspired by SanDisk High Bandwidth Flash (HBF). KV caches, mixture-of-experts weights, long-context attention, large embedding tables

21× more memory, on package, at HBM-class bandwidth — *if* NAND can scale to deliver it

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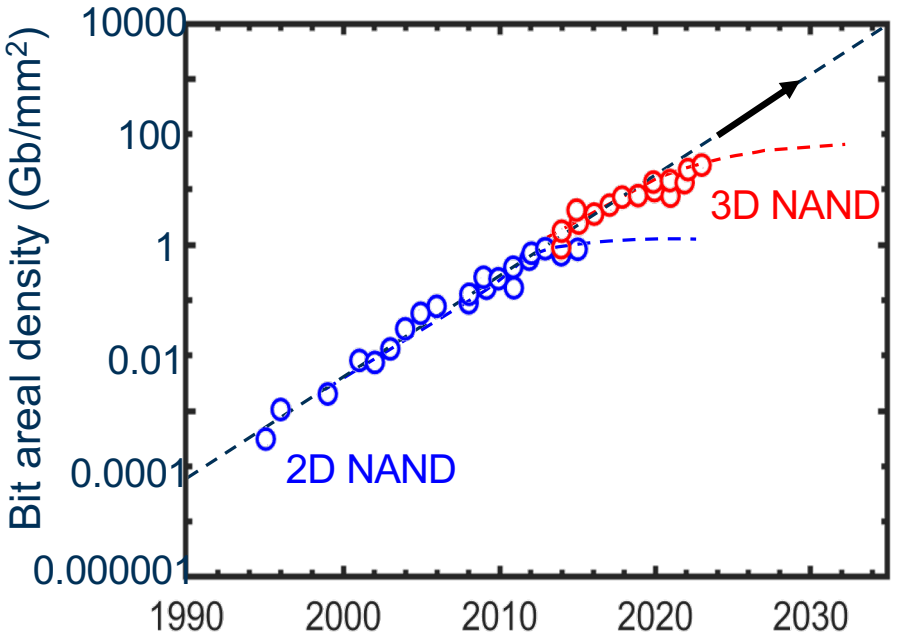
https://documents.sandisk.com/content/dam/asset-library/en_us/assets/public/sandisk/collateral/company/Sandisk-HBF-Fact-Sheet.pdf#page=1.00

Vertical NAND Scaling

NAND Flash Storage



A. Goda, IEDM 2024

Vertical scaling has delivered 50× density per decade — and the climb continues

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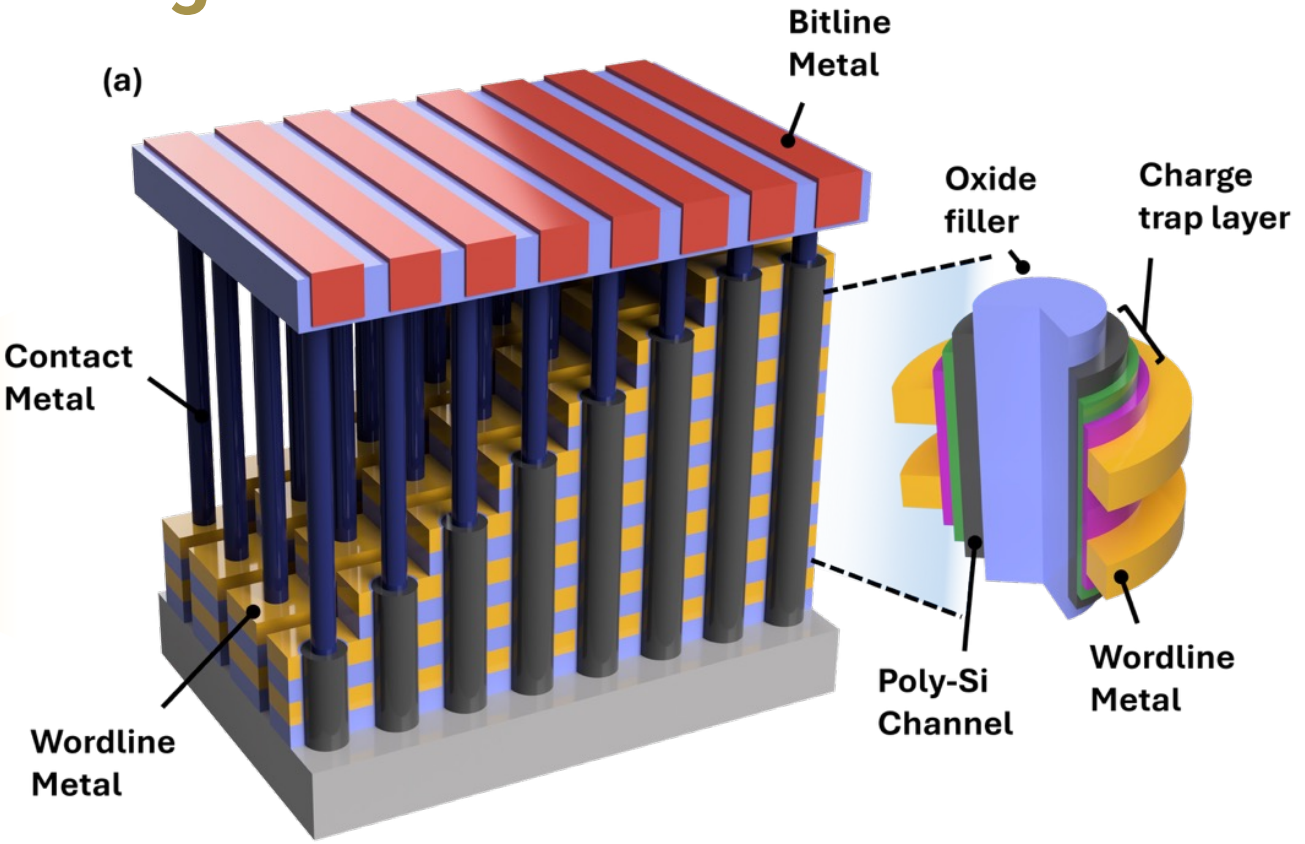
Vertical NAND Scaling



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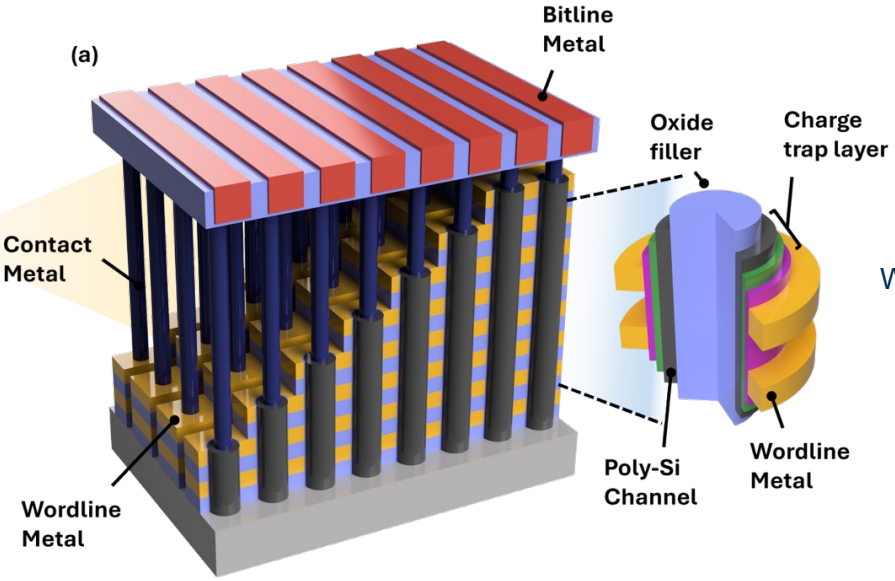
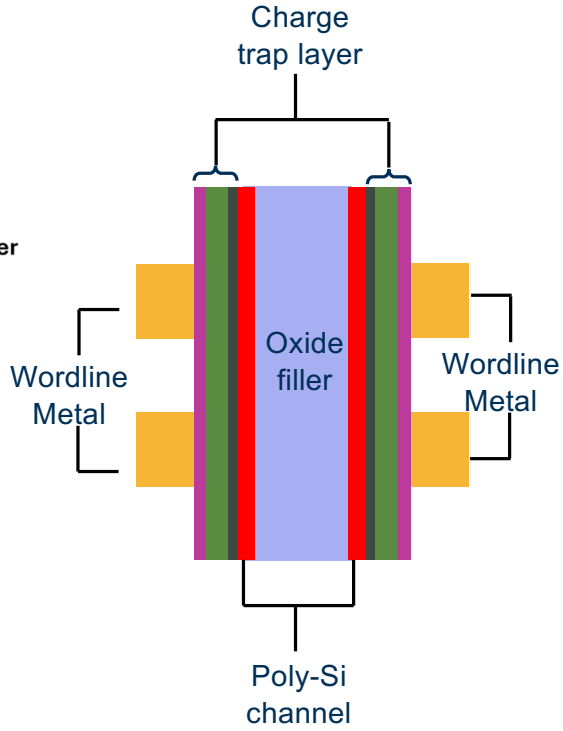
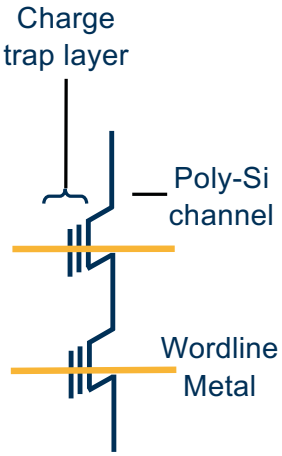
Vertical NAND Scaling

NAND Flash Storage







Relentless innovations have led to a 50x improvement in bit arial density per decade.

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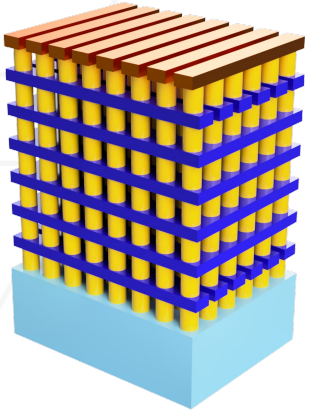
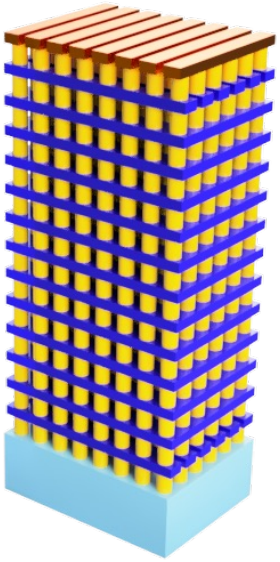
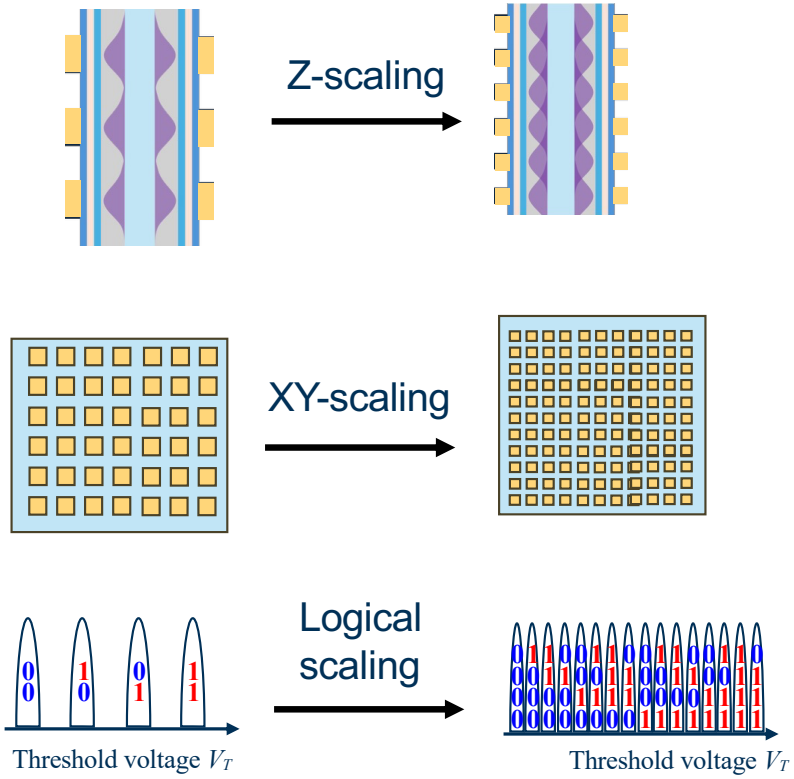
Vertical NAND Scaling



2014
First 3D NAND, Samsung
24 Layers, MLC



2022-2026
Production
Samsung 236L TLC
SK hynix 238L TLC → 321L (ramping 1H25)
Micron 276L TLC
Prototype / R&D demos:
SK hynix 321L sample (FMS 2023)
SK hynix 300+L demo (ISSCC 2023)
Kioxia / WD >300L demo (VLSI 2023)
Kioxia / Sandisk 1000L using wafer-to-wafer Cu direct bonding (2026)



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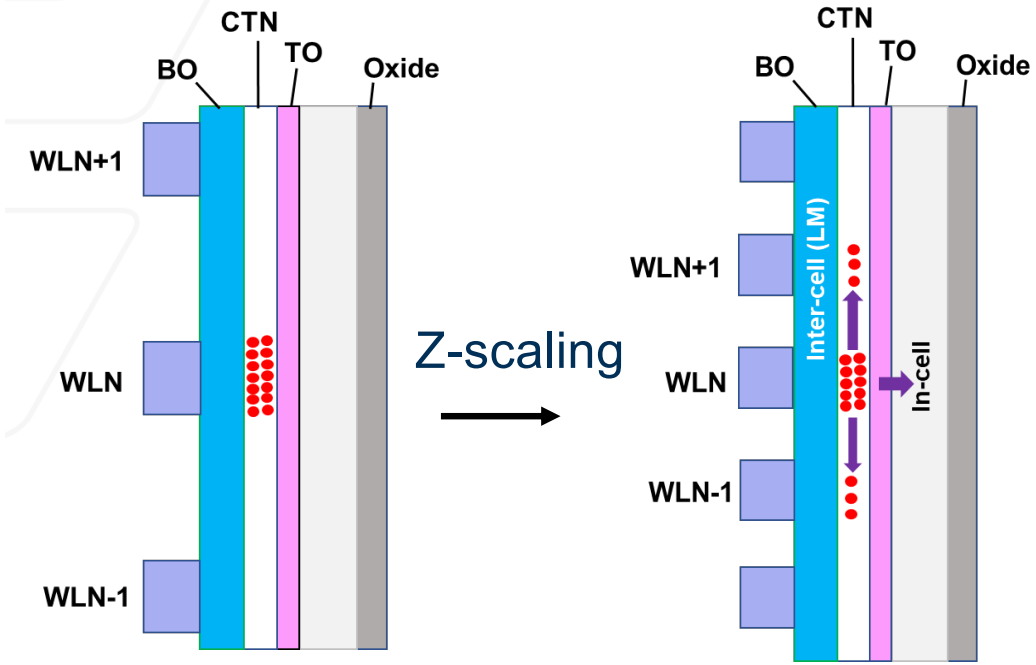
Challenges of vertical NAND flash scaling



1 Lateral charge migration

Continuous SiN trap layer lets stored charge migrate between cells via diffusion and trap-to-trap transport.

2 High write voltage

Fowler–Nordheim programming demands ~20 V every cycle — large on-die charge pumps and accelerated tunnel-oxide wear-out. Increased power,

3 Coupling and disturb

Electrostatic fringing fields perturb adjacent cells; pass-voltage stress accumulates with each read.

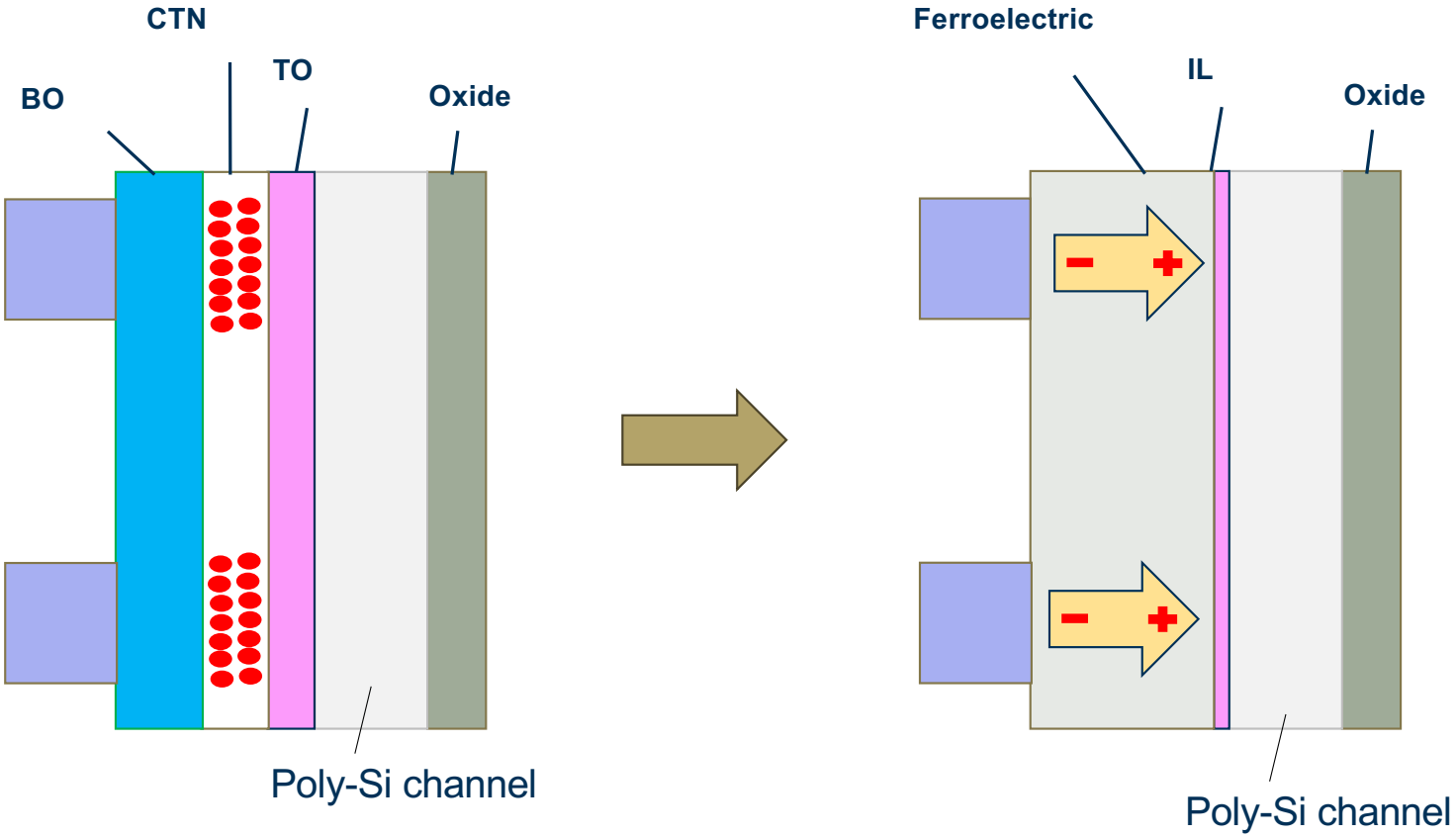
4 Variability and read margin

RTN, poly-Si grain variability, and channel taper compress threshold-voltage state distributions. Poly-Si channel resistance grows with cell count; grain boundaries limit mobility and uniformity.

Read sensing margin shrinks

13

Can ferroelectricity enable next generation NAND flash?



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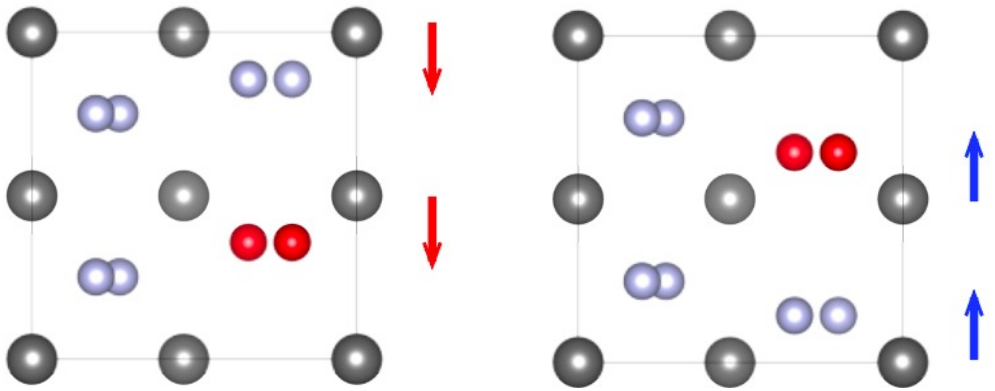
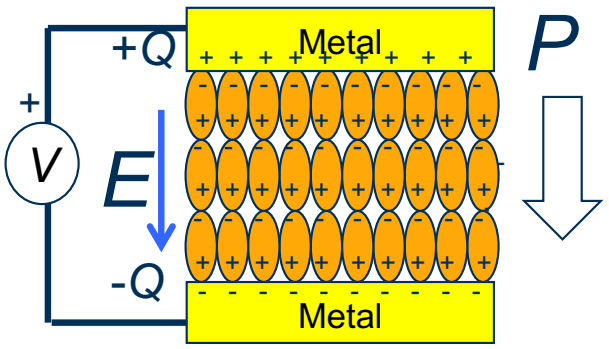
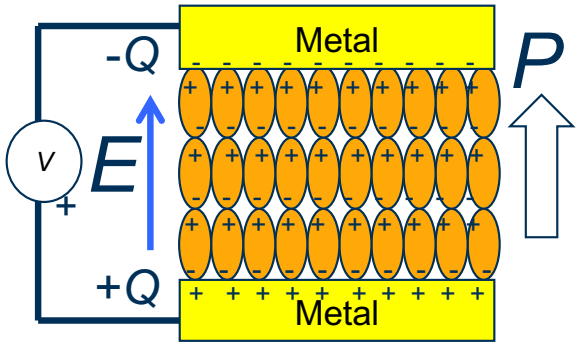
Ferroelectricity

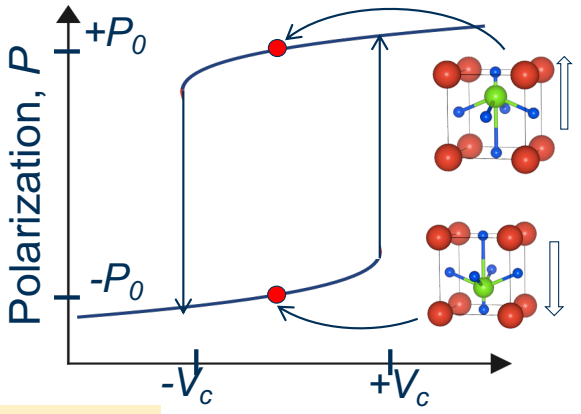
CMOS compatible HfO_2-based fluorite-structure ferroelectric

Orthorhombic *Pca2₁* structure



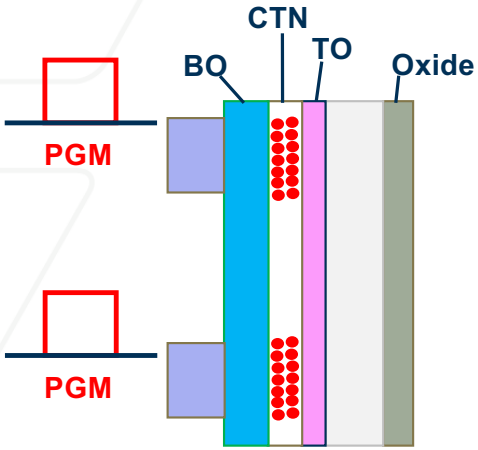


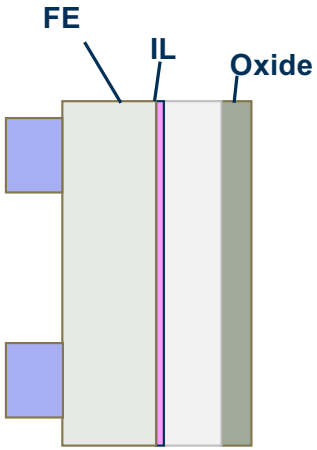




A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

Charge trap flash vs. ferroelectric flash





CTF that stores data in the form of charge.

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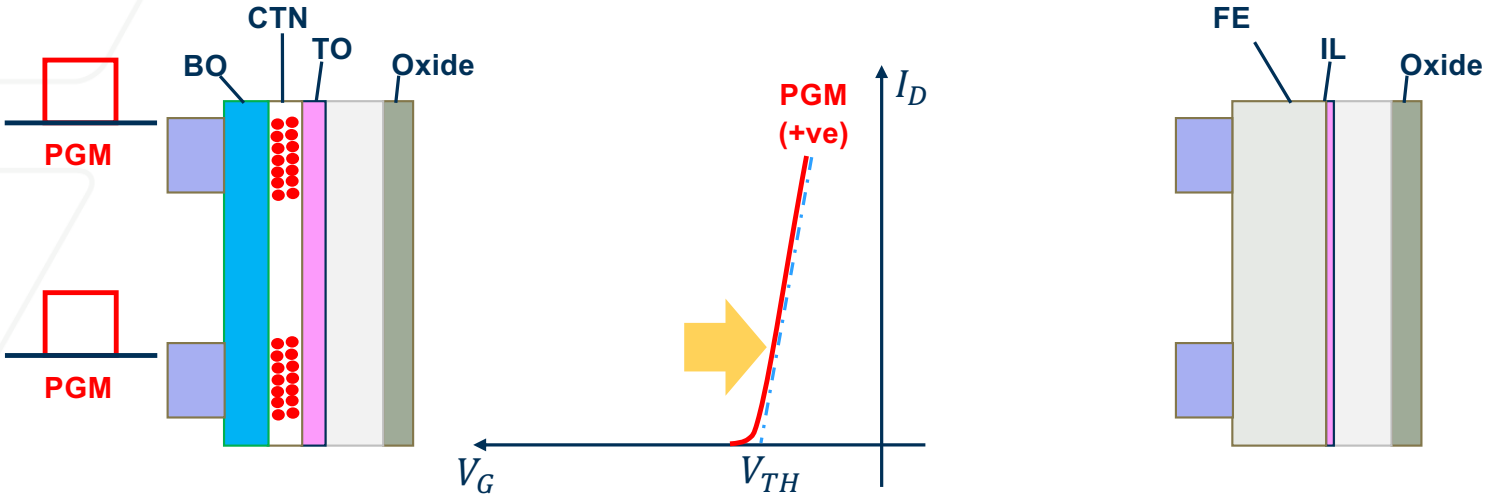

A Positive PGM pulse sets the Vt to high Vt state in CTF NAND.

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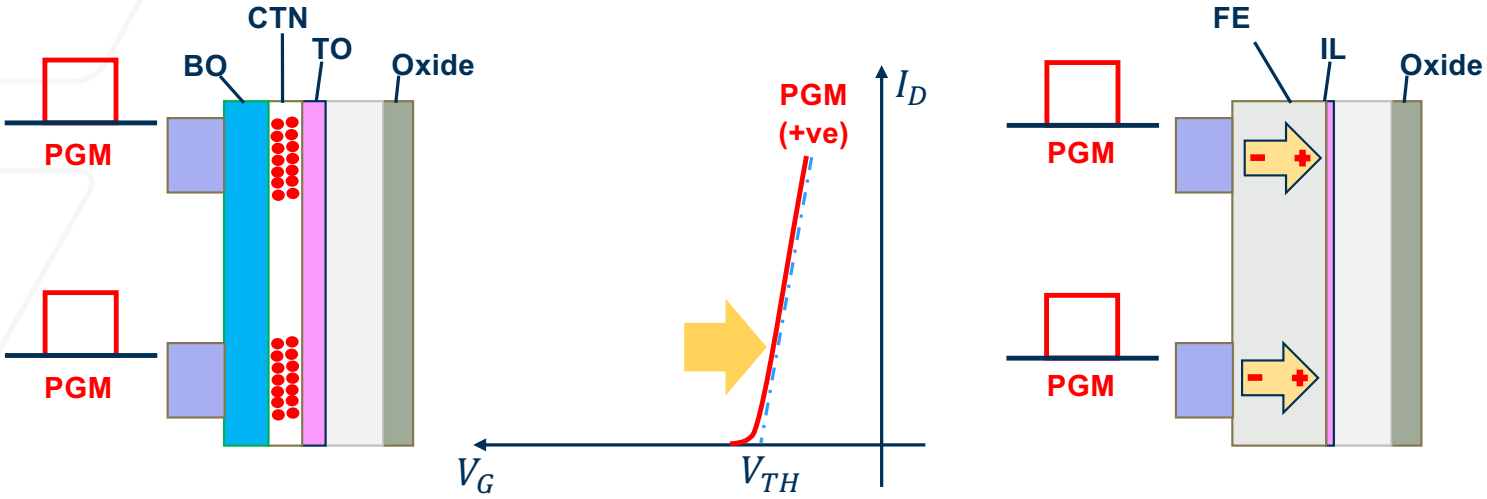

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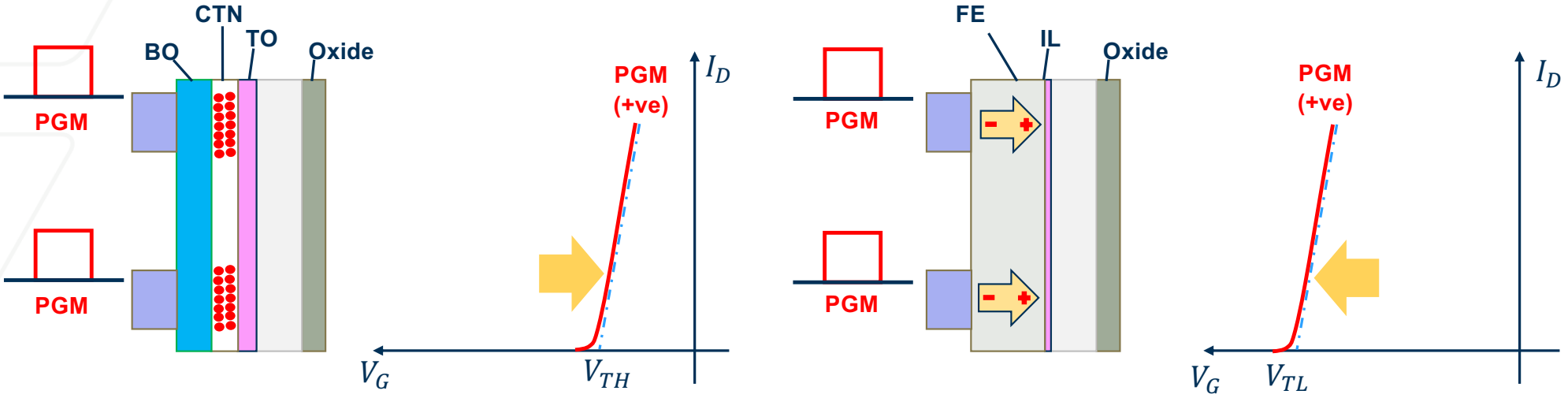

A Positive PGM pulse sets the Vt to high Vt state in CTF NAND.

On the contrary, a Positive PGM pulse sets the Vt to low Vt state in a FEFET.

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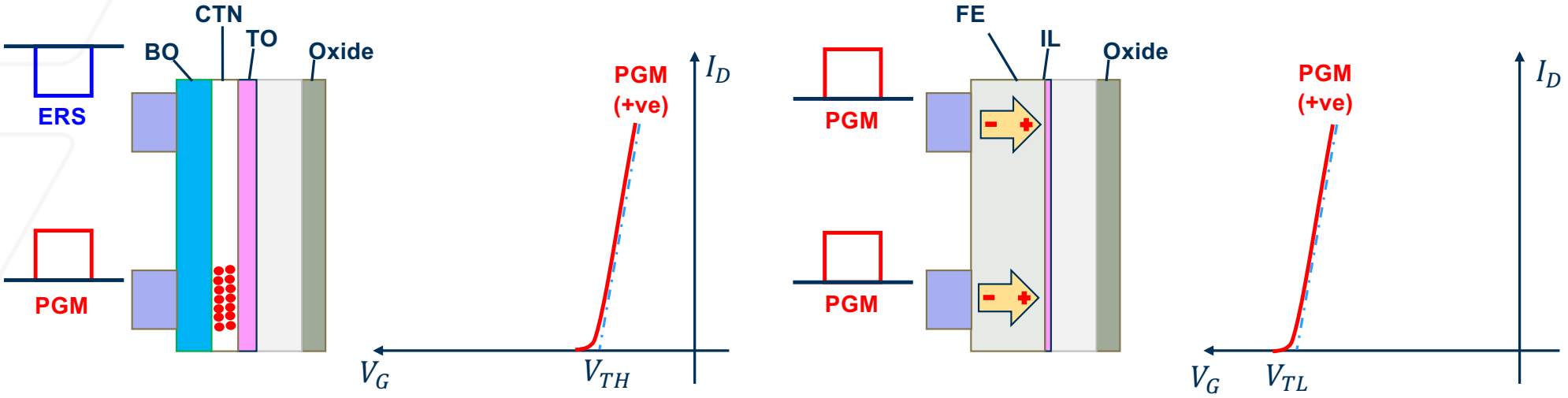

A Negative ERS pulse sets the Vt to low Vt state in CTF NAND.

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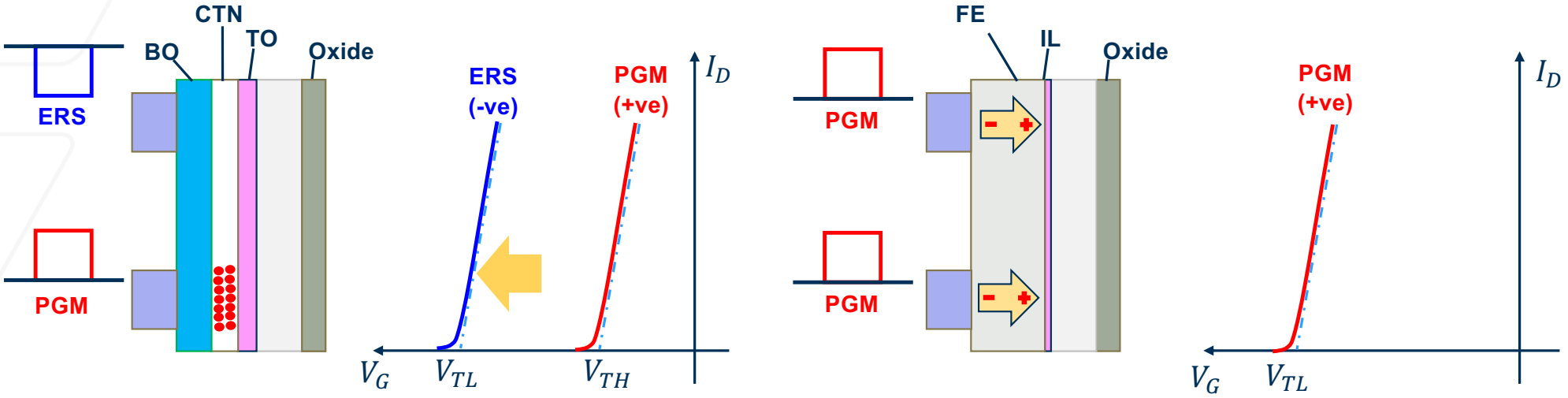

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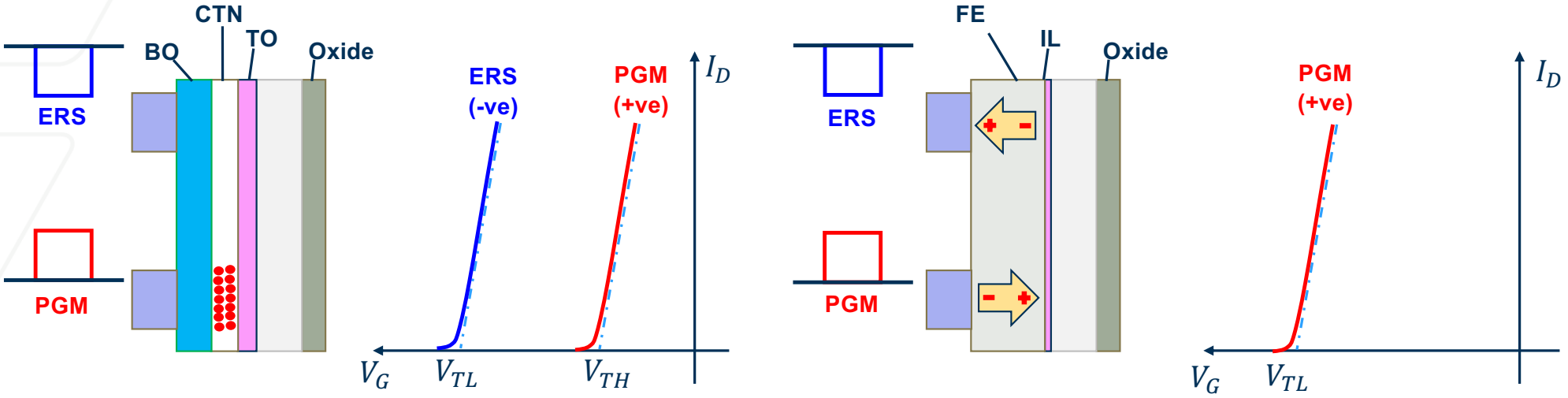

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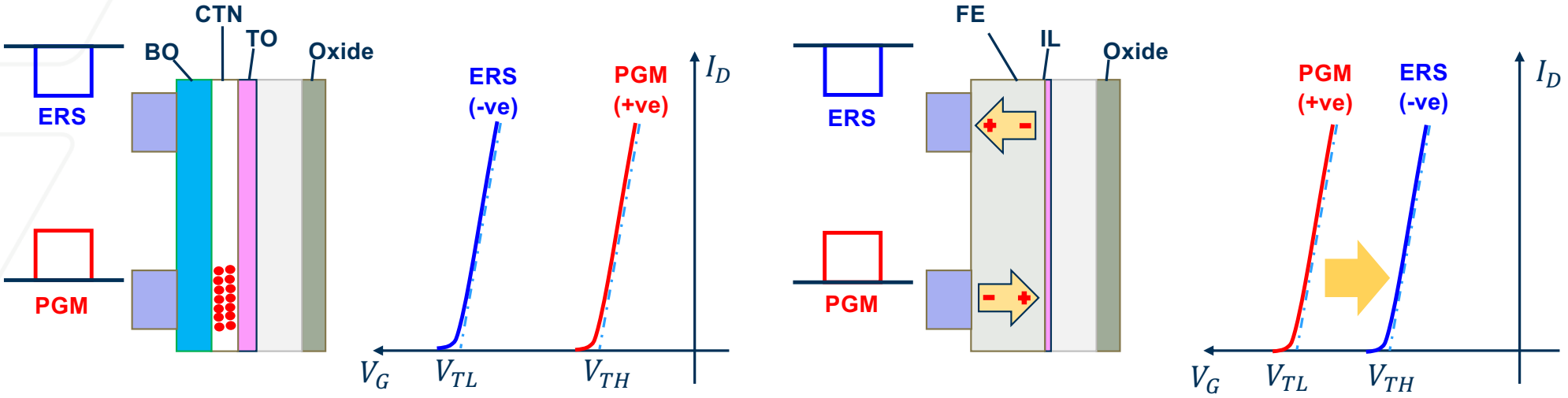

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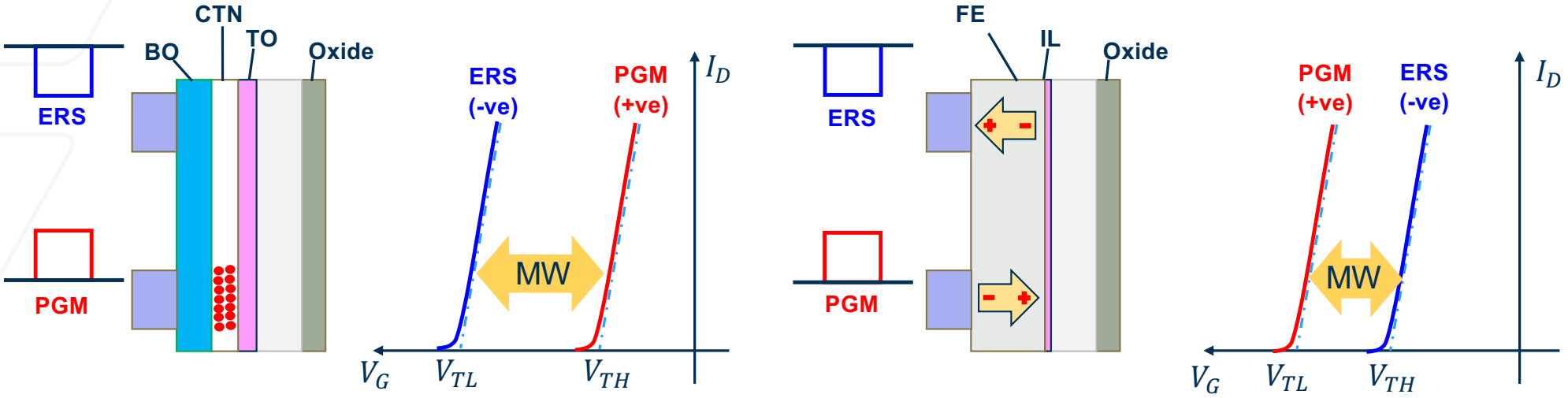

$$MW = V_{TH} - V_{TL}$$

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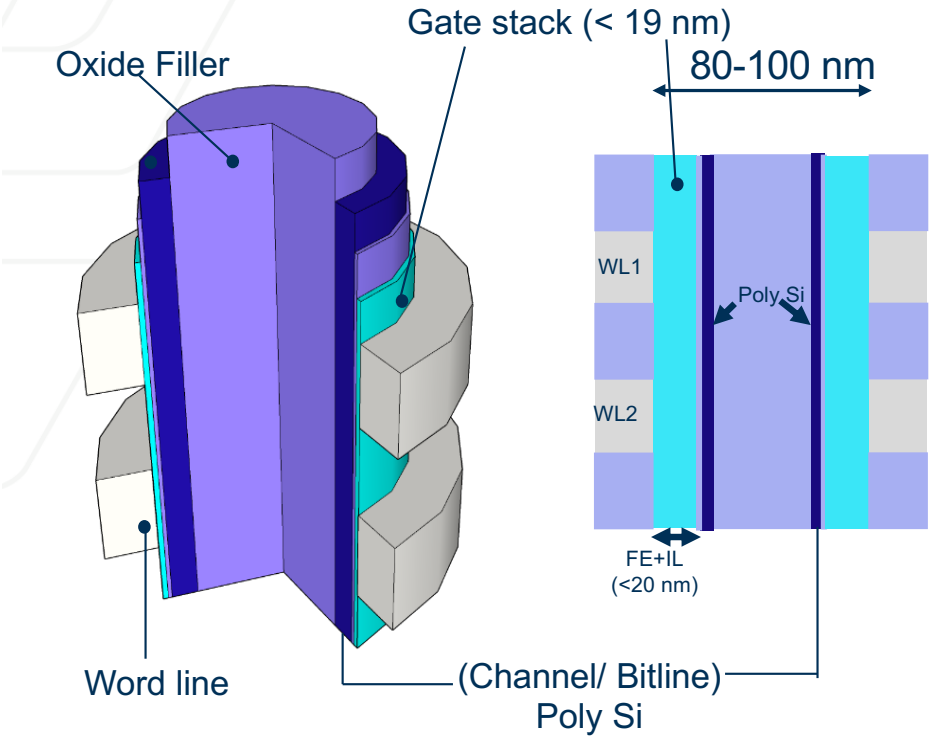
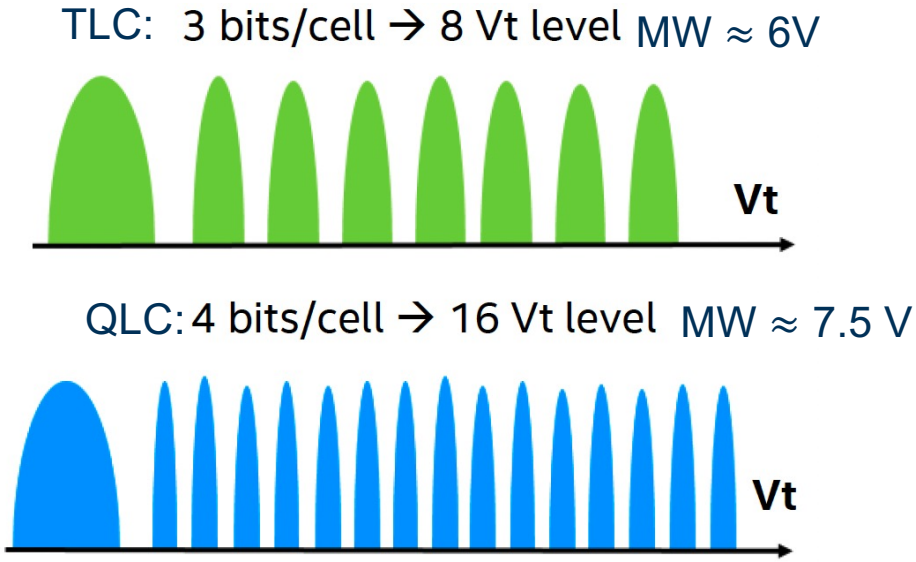
Target metrics for ferroelectric NAND flash





To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm

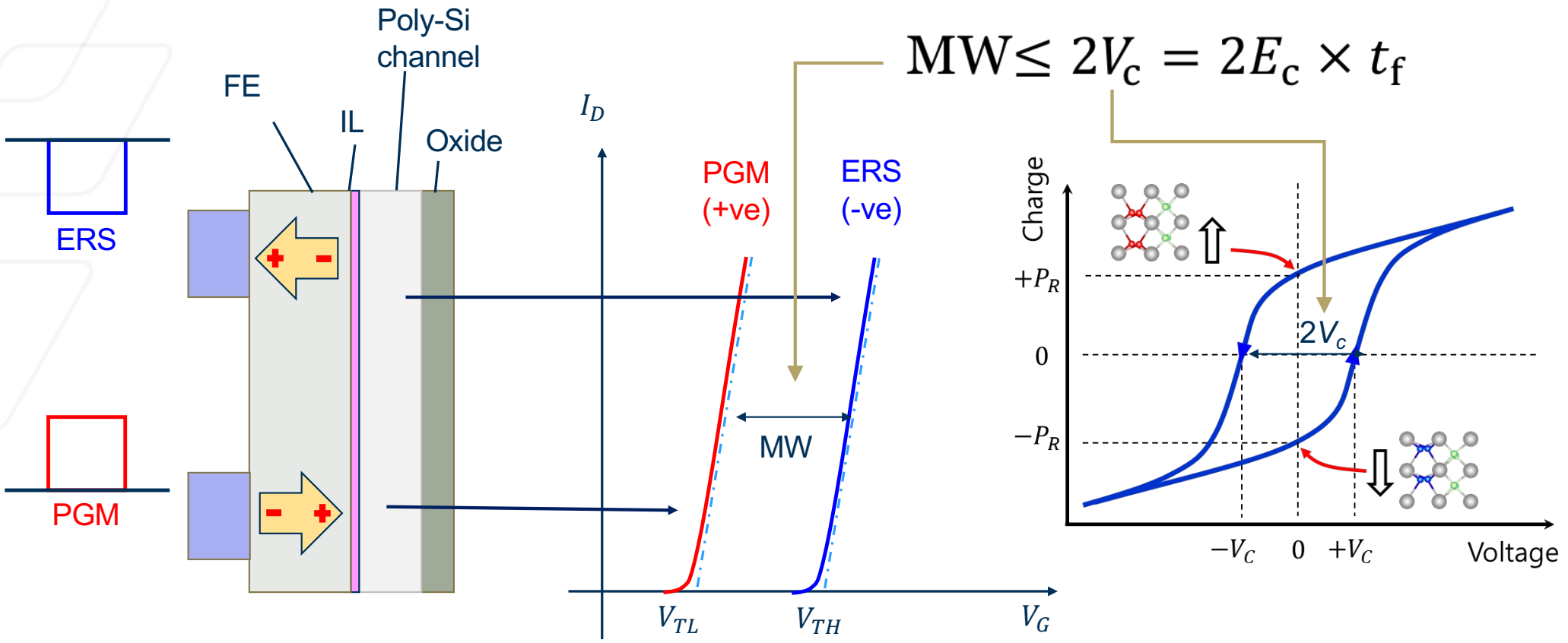
Design constraints

Gate stack thickness, $t \leq 19$ nm

Write voltage ≤ 15 V

Memory window, MW ≥ 6.5 V

Ferroelectric flash



The maximum memory window of a FeFET is theoretically limited by the memory window of the ferroelectric layer.

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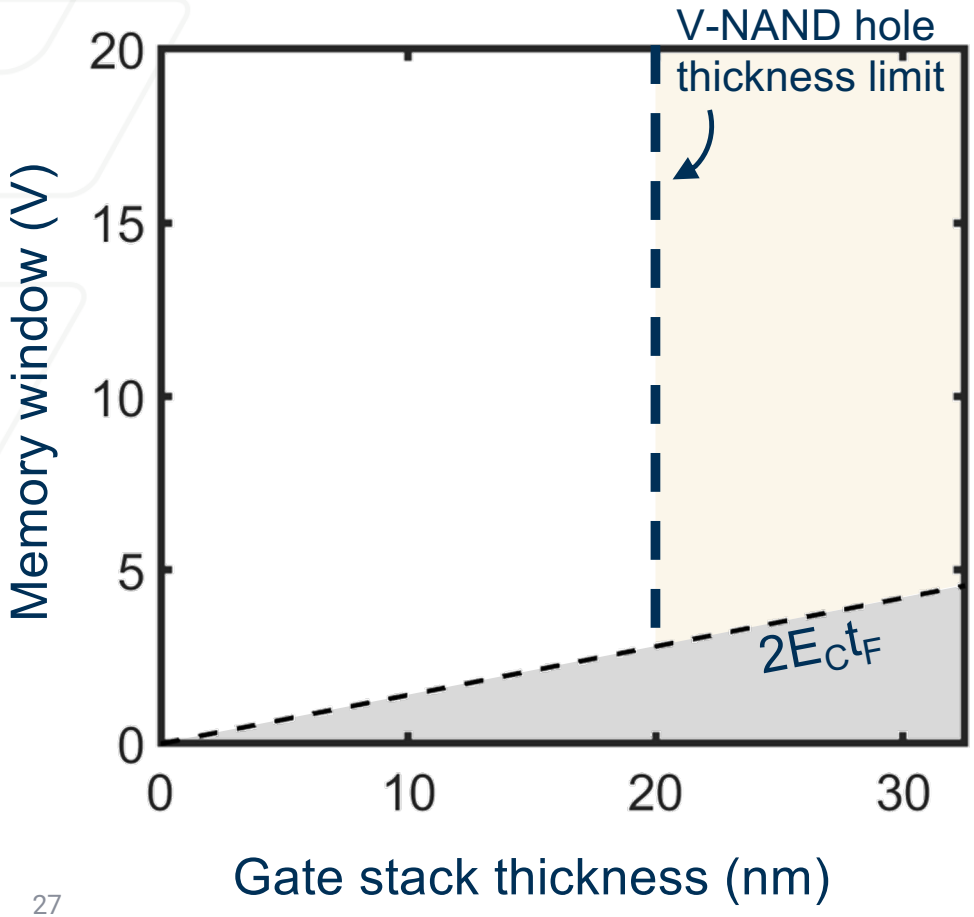
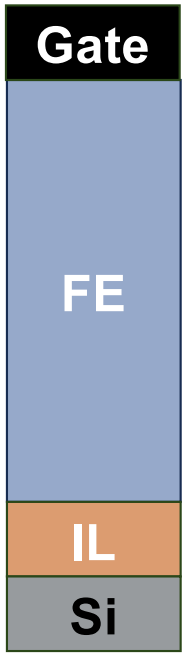
Memory window of FEFETs is limited by V_C





$$\mathrm{MW} \leq 2V_c = 2E_c \times t_f$$

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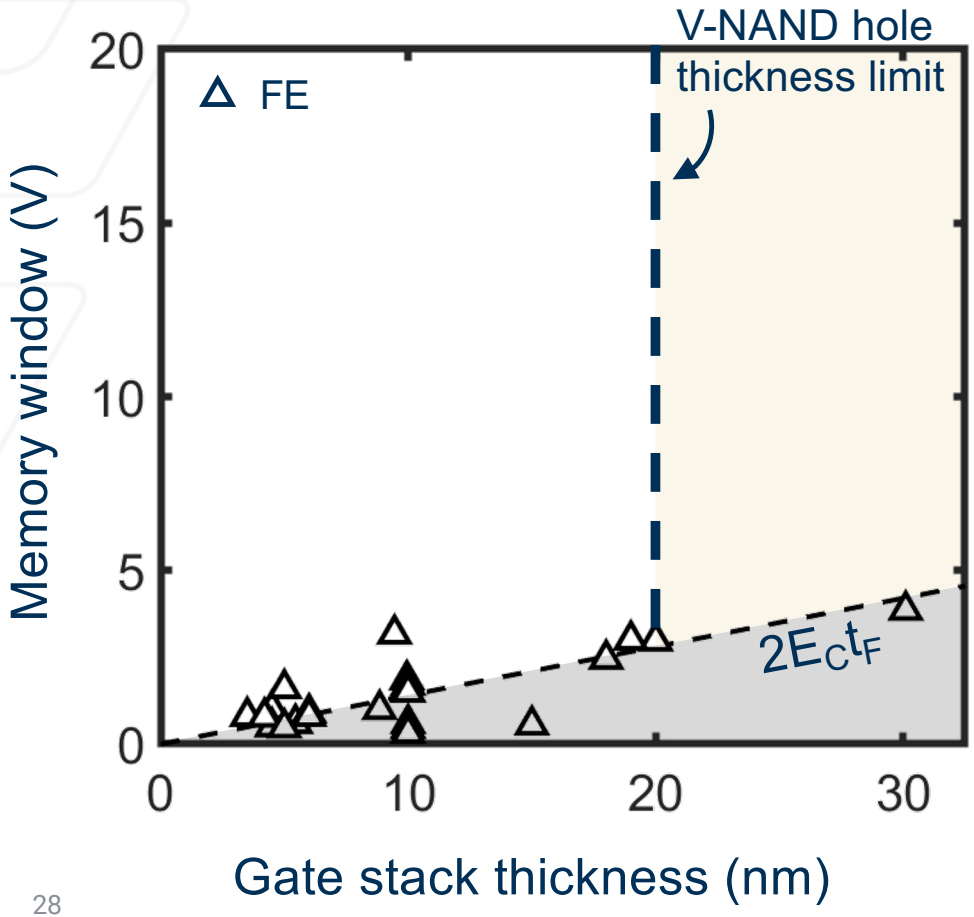
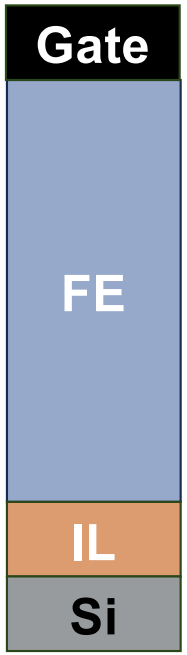
Memory window of FEFETs is limited by V_C





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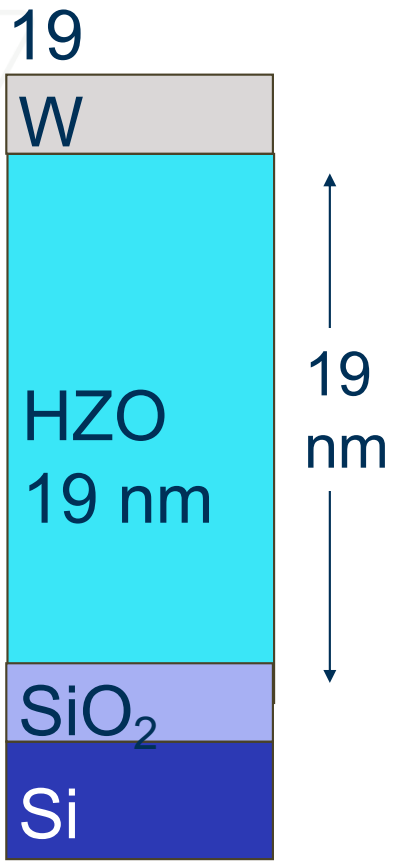
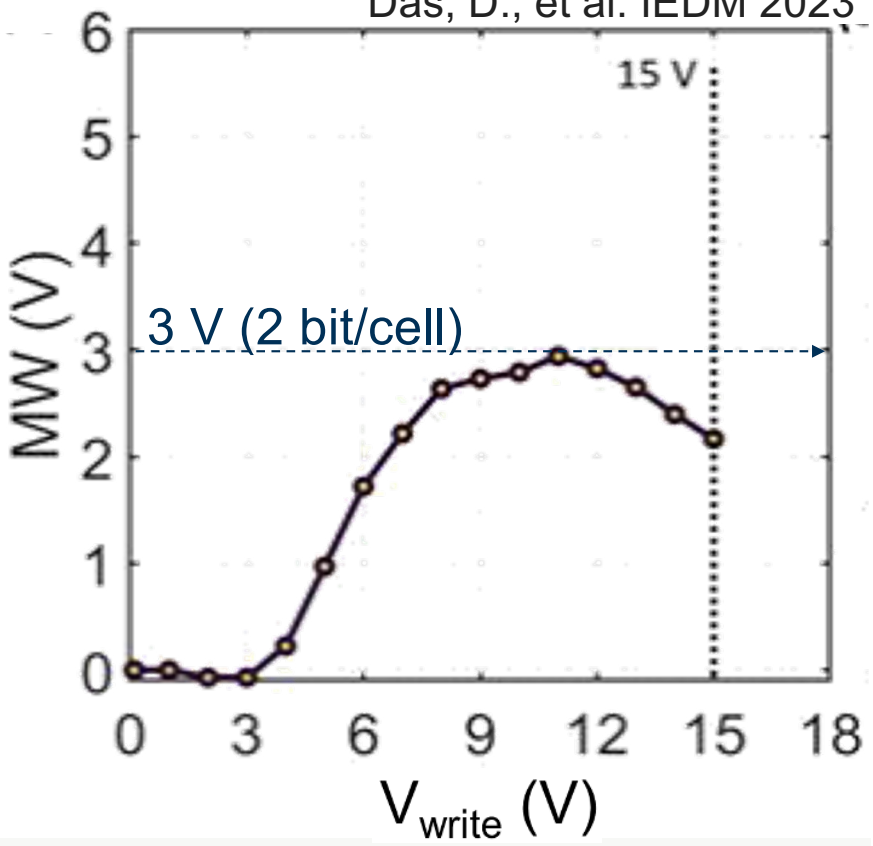
The maximum memory window of an FeFET is theoretically limited by the memory window of the ferroelectric layer.

Increasing the MW by dielectric insertion



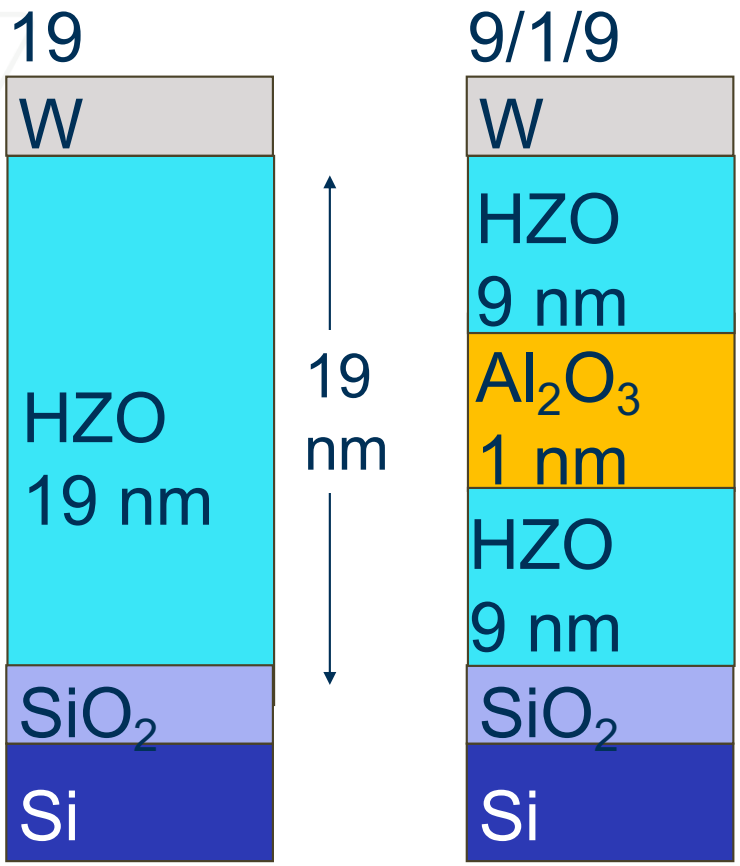
Das, D., et al. IEDM 2023

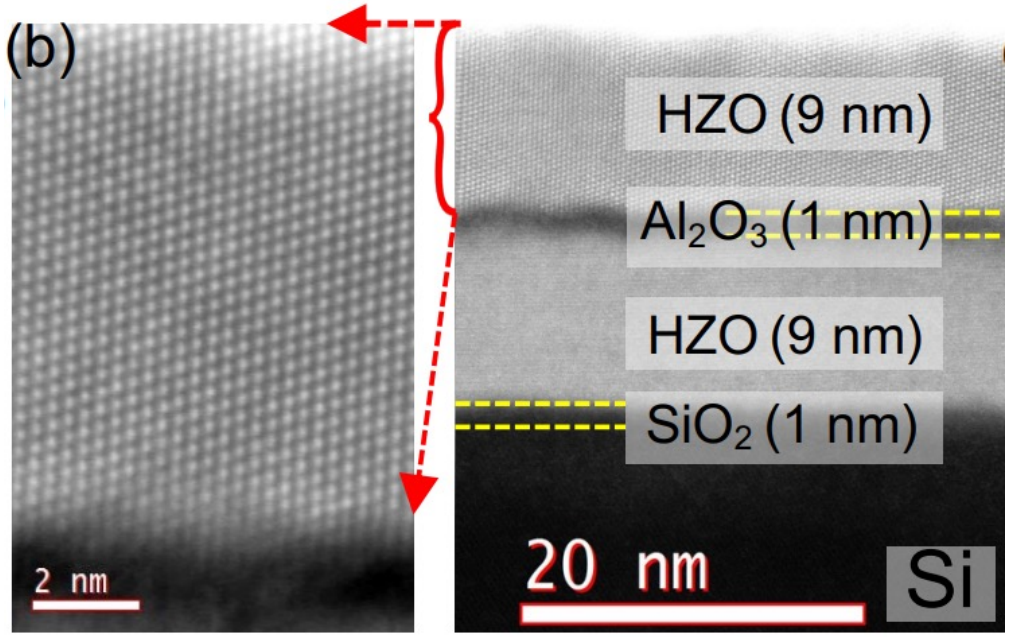


10 nm HZO layer leads to maximum memory window of 2.9 V.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion





Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

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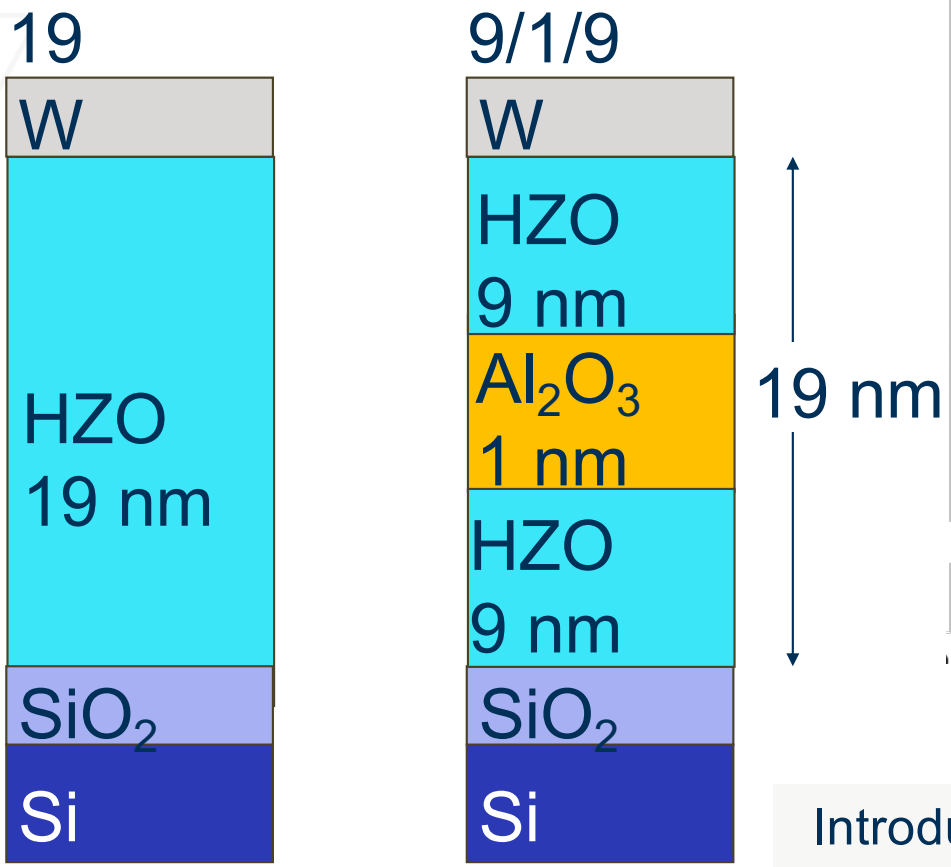
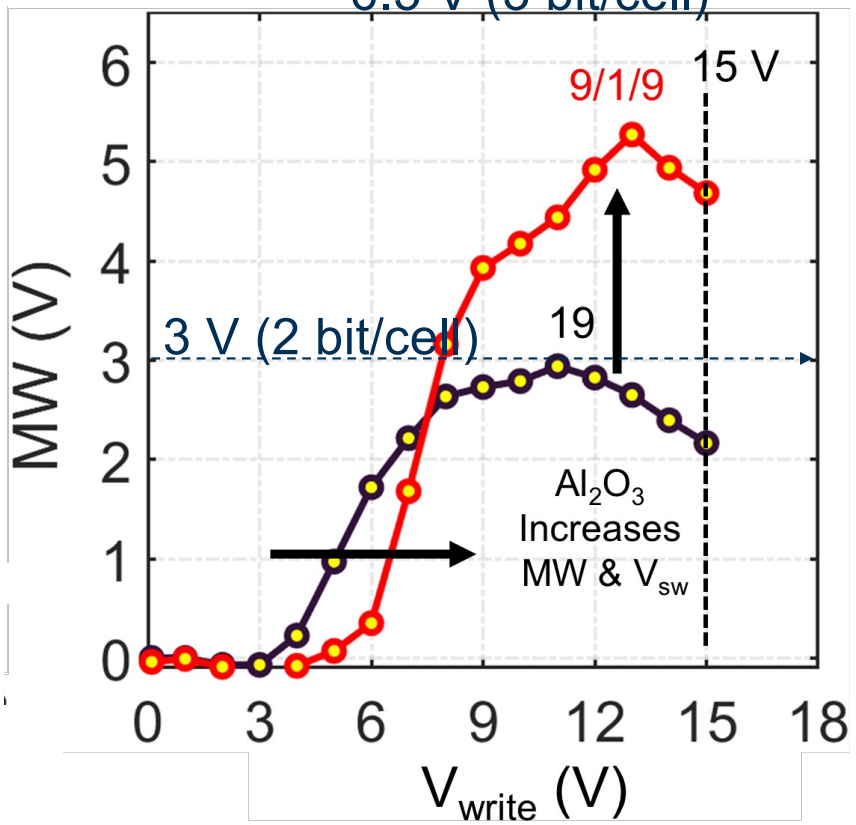
Increasing the MW by dielectric insertion





Introducing 1 nm Al_2O_3 intermediate layer dramatically memory window to 5.3 V.

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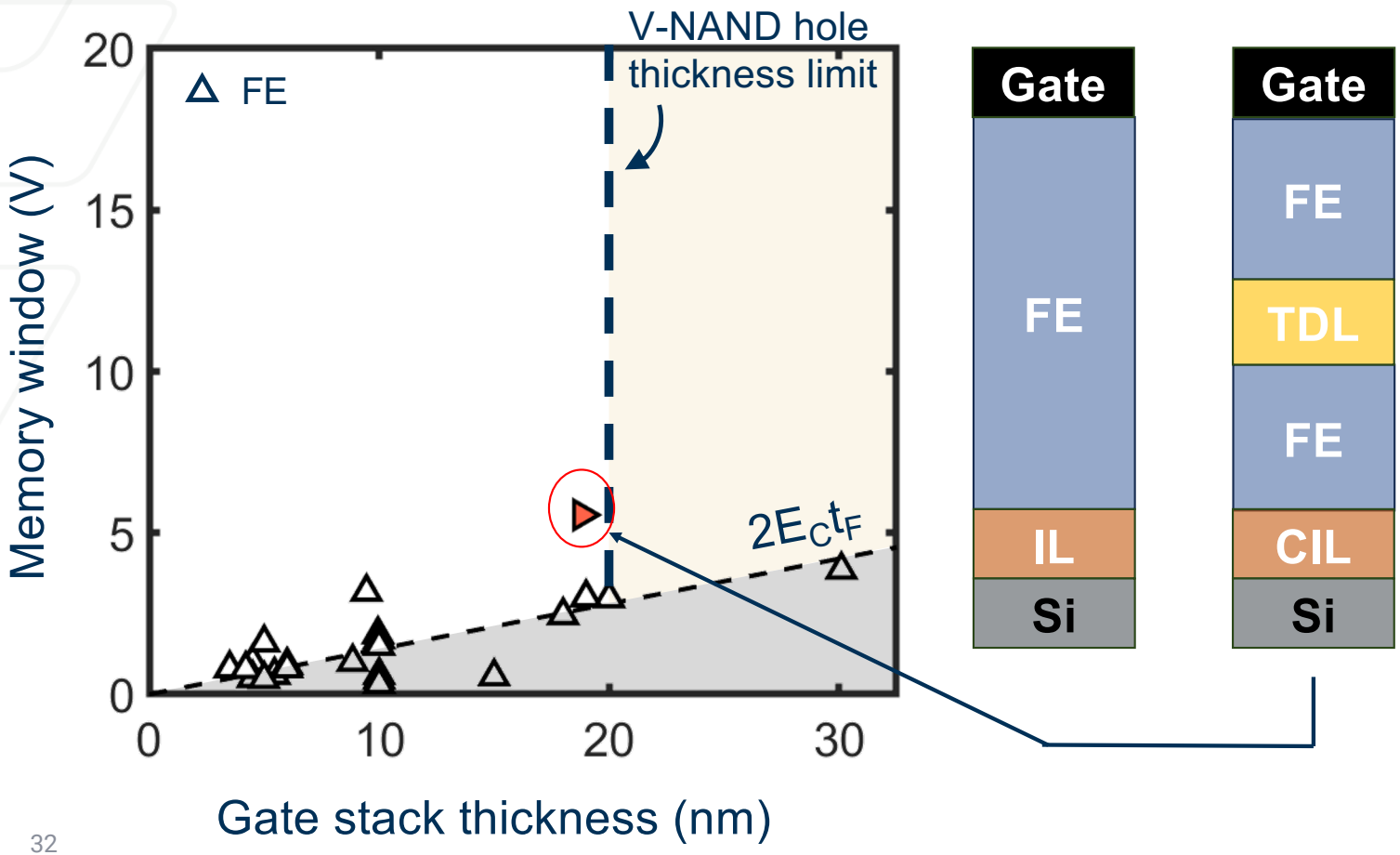
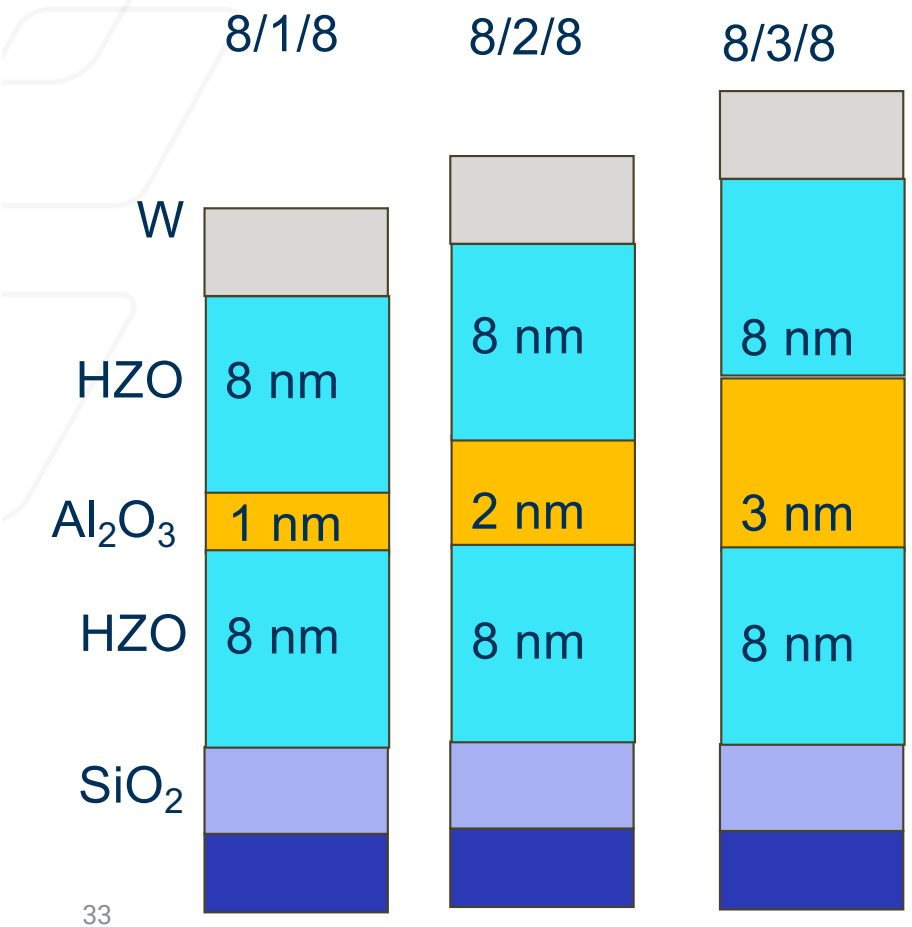
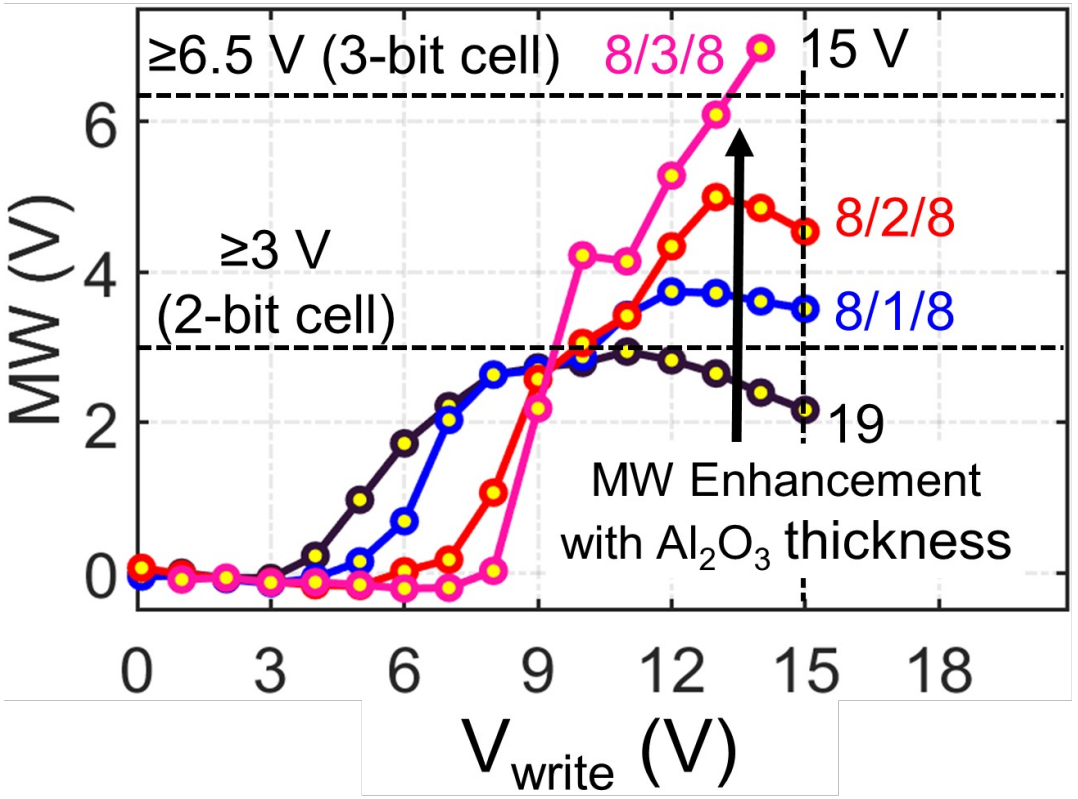
Memory window of FEFETs is limited by V_C



Georgia Tech

Increasing the MW by dielectric insertion

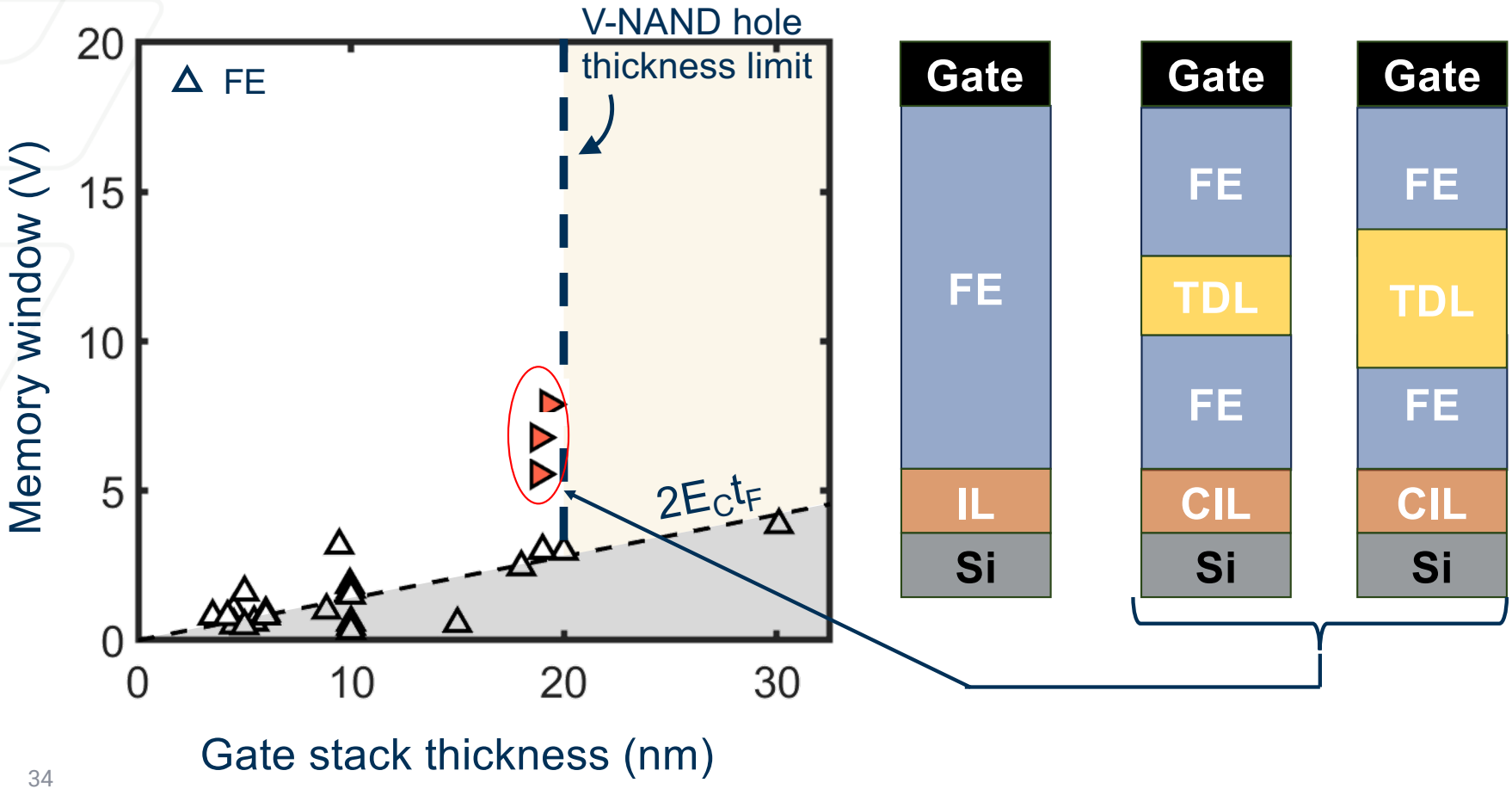




FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

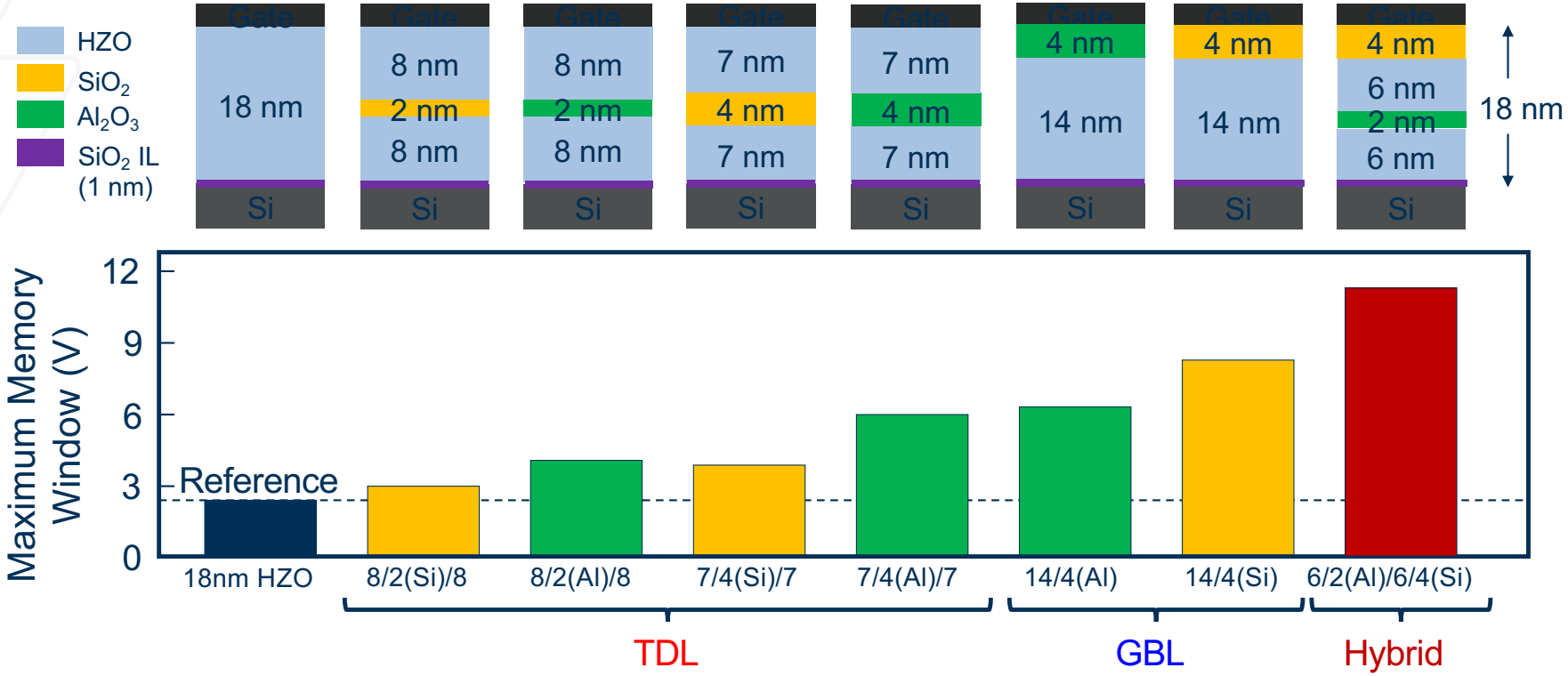
Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion



Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

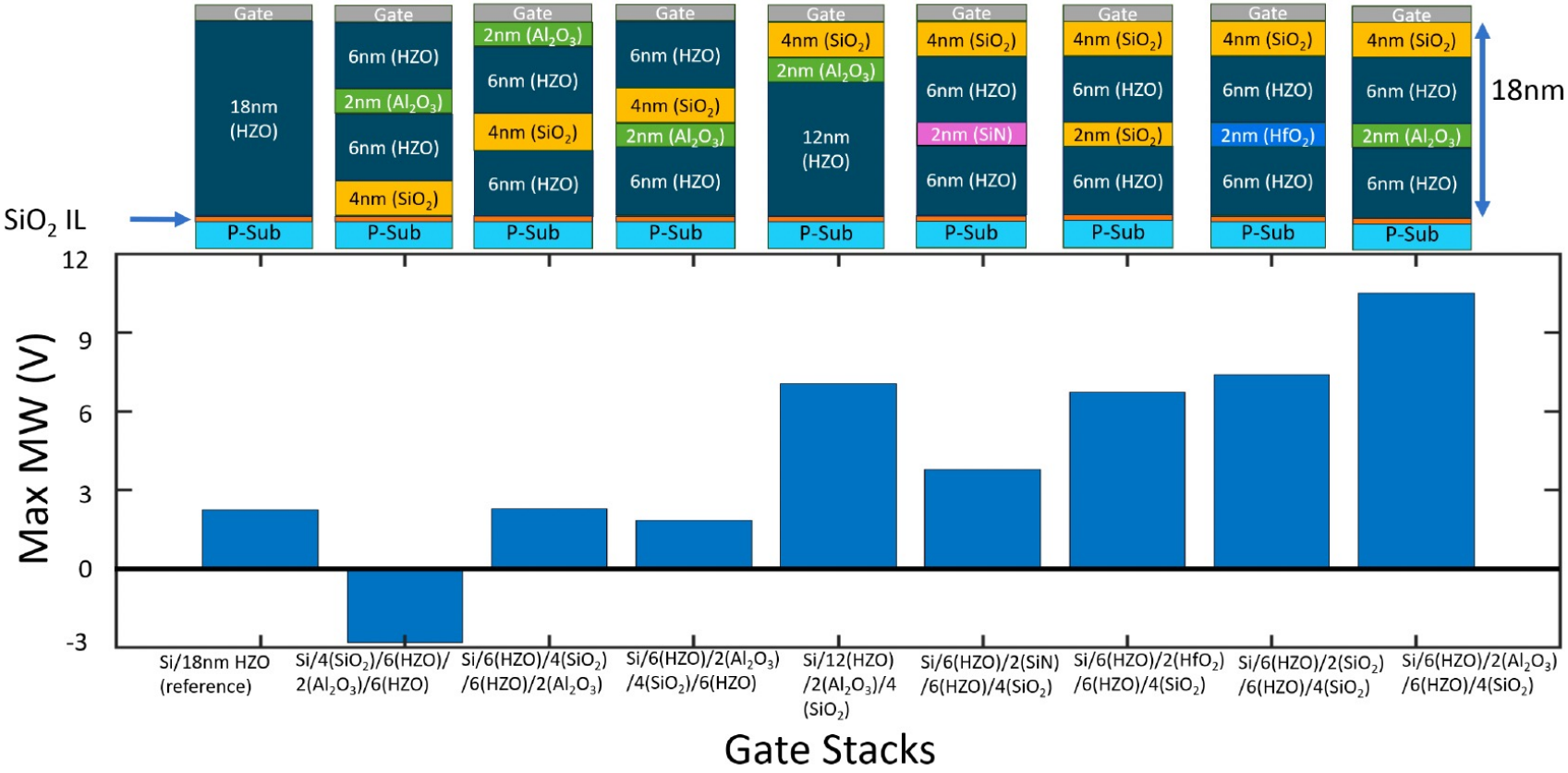
Position and choice of the dielectric



- GBL stacks have higher MW than TDL stacks for similar thickness and material.
- SiO_2 in GBL and Al_2O_3 in TDL gives higher MW for similar dielectric thickness

Hernandez-Chacon, J. *Material choices for charge trapping layer and blocking layer for ferroelectric NAND applications*. IEEE Electron Device Letter 45, 1776 - 1779 (2024). https://doi.org/10.1109/LED.2024.3437239

Position and choice of the dielectric



Fernandes, Khan et al. *Optimizing Memory Window for Ferroelectric Nand Applications: An Experimental Study on Dielectric Material Selection and Layer Positioning*. IEEE Transactions on Electron Devices 72, 234 - 239 (2024). https://doi.org/10.1109/TED.2024.3504475

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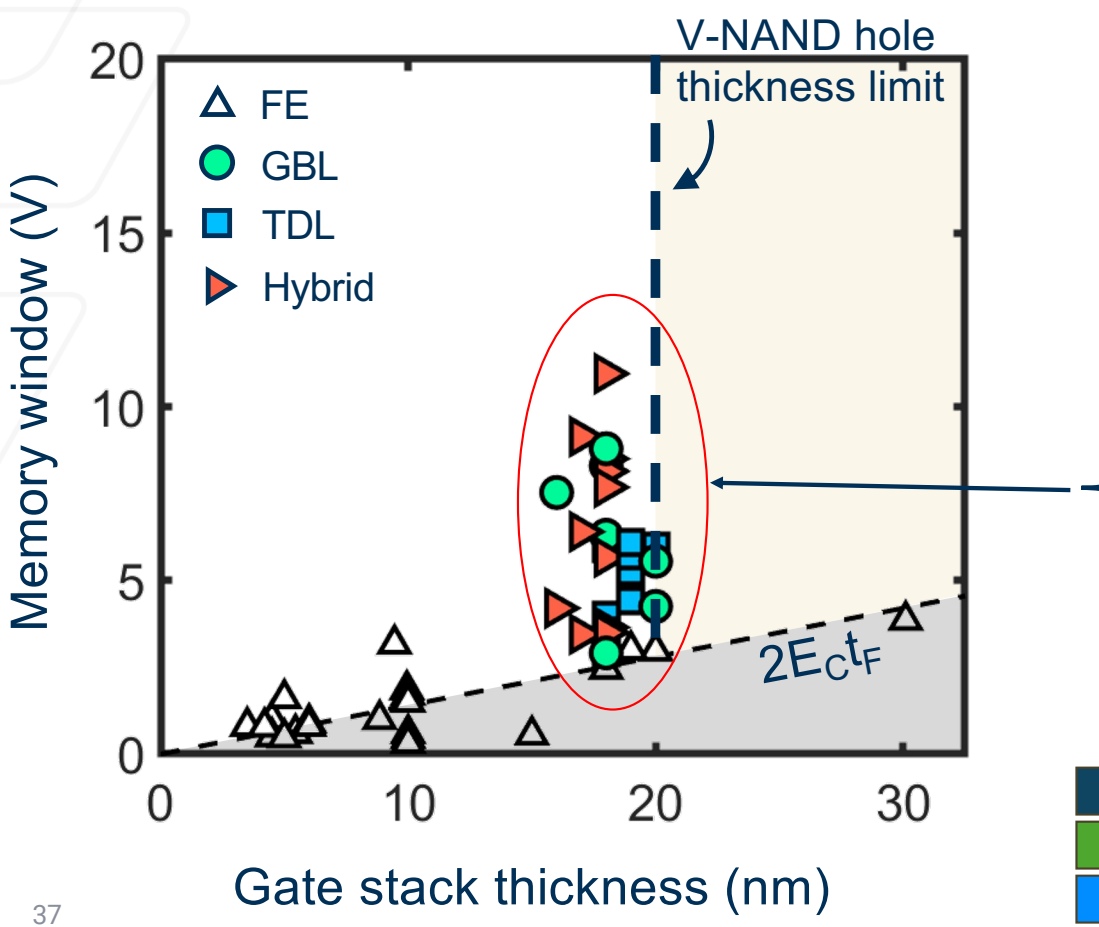
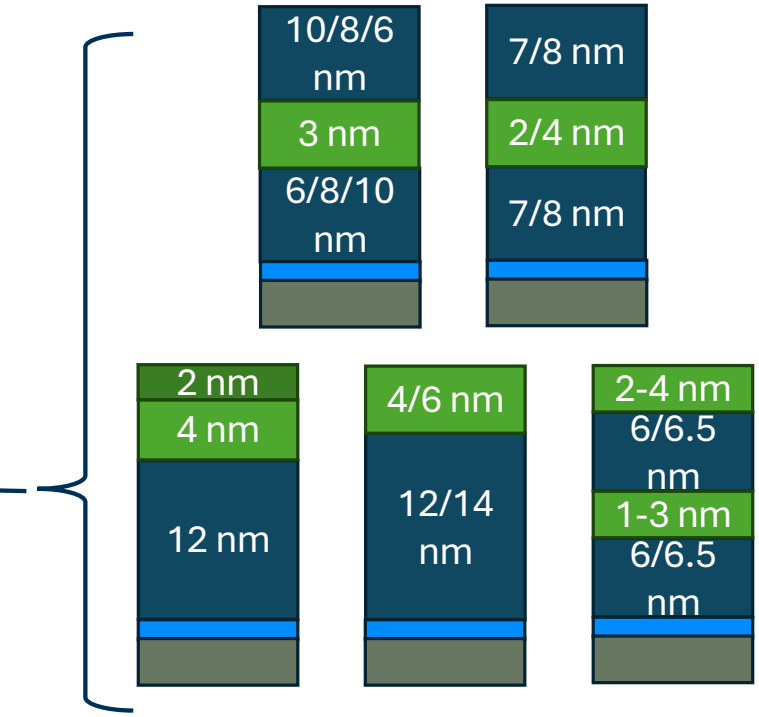
Increasing the MW by dielectric insertion

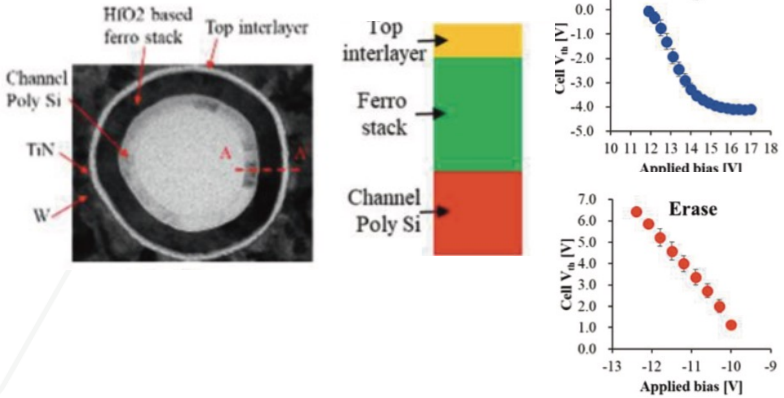




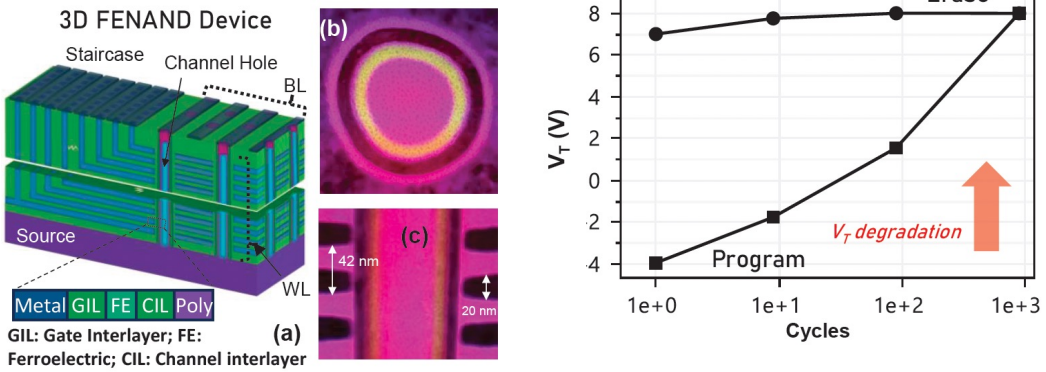
Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$
Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4
Channel IL: SiO_2
Semiconductor: Bulk Si, Poly Si, SOI, IWO

Increasing the MW by dielectric insertion

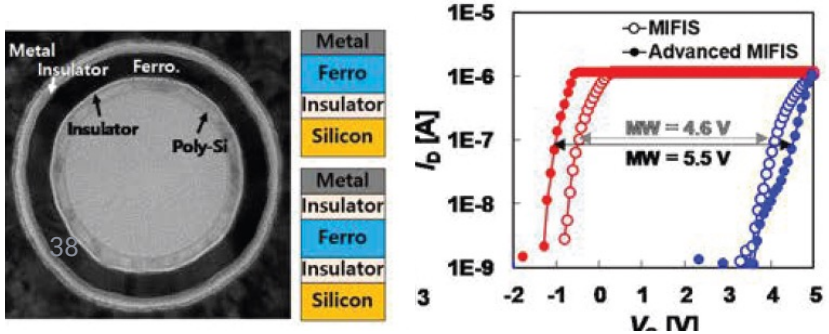
SK Hynix
Yoon et al. VLSI 2023



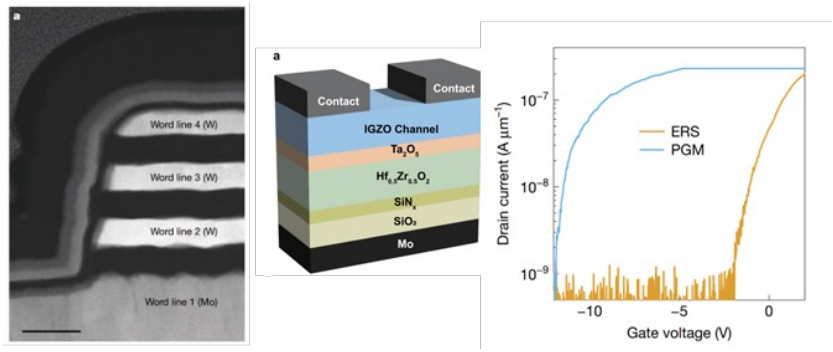
Micron
Sharma et al. VLSI 2025



Samsung
Lim et al. IEDM 2023



Samsung
Sharma et al. Science 2025

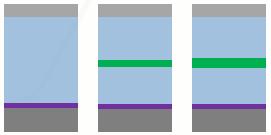


Increasing the MW by dielectric insertion

Results from Georgia Tech

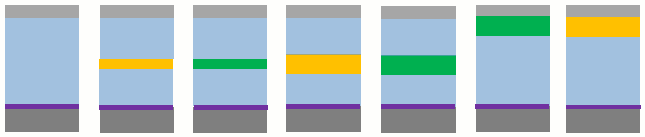
Batch 1: Tunnel Dielectric Layer

Das et al., IEDM 2023:



Batch 2: Choice and position of dielectric insert

Fernandes et al., EDL 2024:

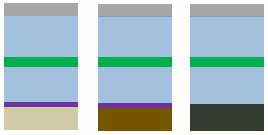


Batch 3: Hybrid structures

Fernandes et al., TED 2024:

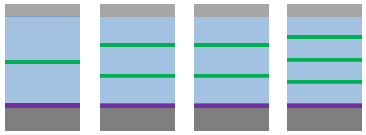
Batch 4: Channel materials

Fernandes et al., IMW 2025:



0.5 nm TDL inserts

Lee et al., TED 2024:



AOS channels

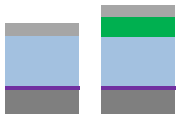
Yoo et al., VLSI 2024:

Joh et al., IEDM 2024:

Gate blocking layer

Lim et al., IEDM 2023:

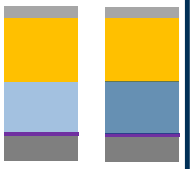
Hu et al., EDL 2024:



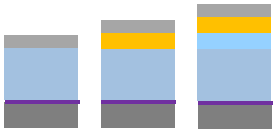
Yang et al., ICSIST 2024:

Hu et al., EDL 2024:

Chu et al., EDL 2024:

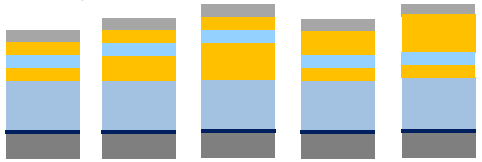


Kuk et al., IEDM 2024:

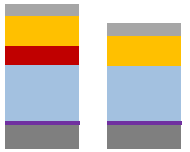


Qin et al., IEDM 2024:

Han et al., IRPS 2025:



G. Kim et al., IEDM 2024:



Ferroelectrics:

- 39 HZO
- HAO

Dielectrics:

- SiO_2
- Al_2O_3
- Si_3N_4
- HfO_2
- TiO_2

Channel IL:

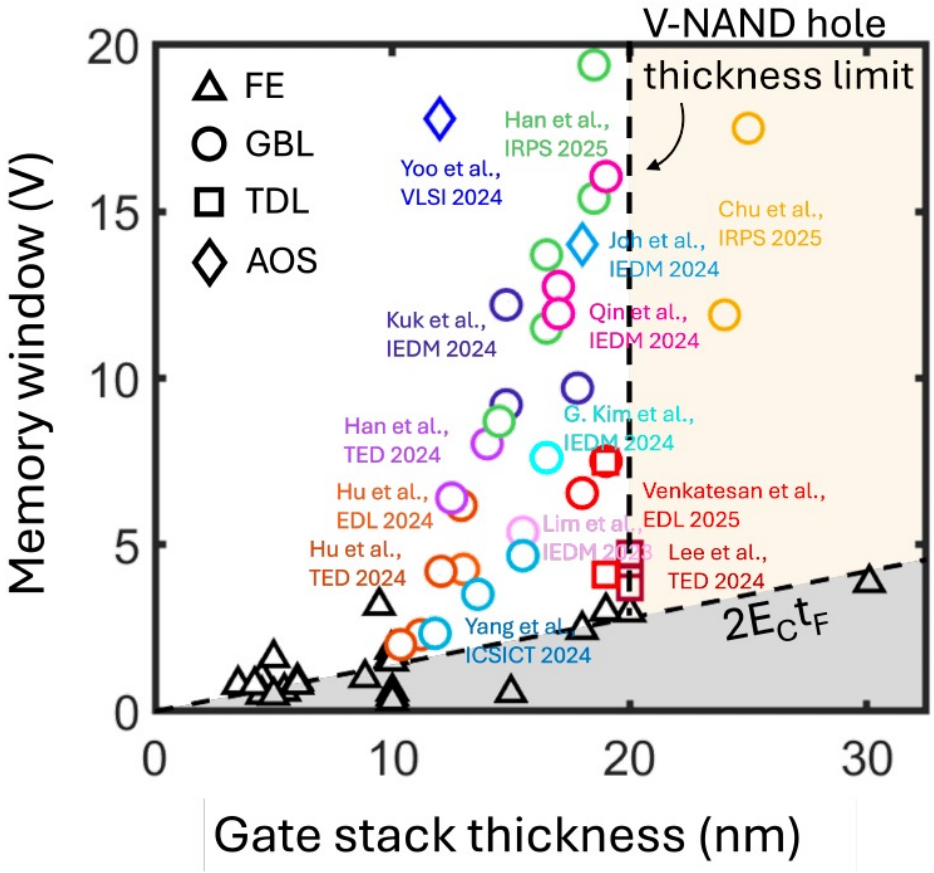
- SiO_2 IL (1 nm)
- Al_2O_3/AlON IL (1 nm)

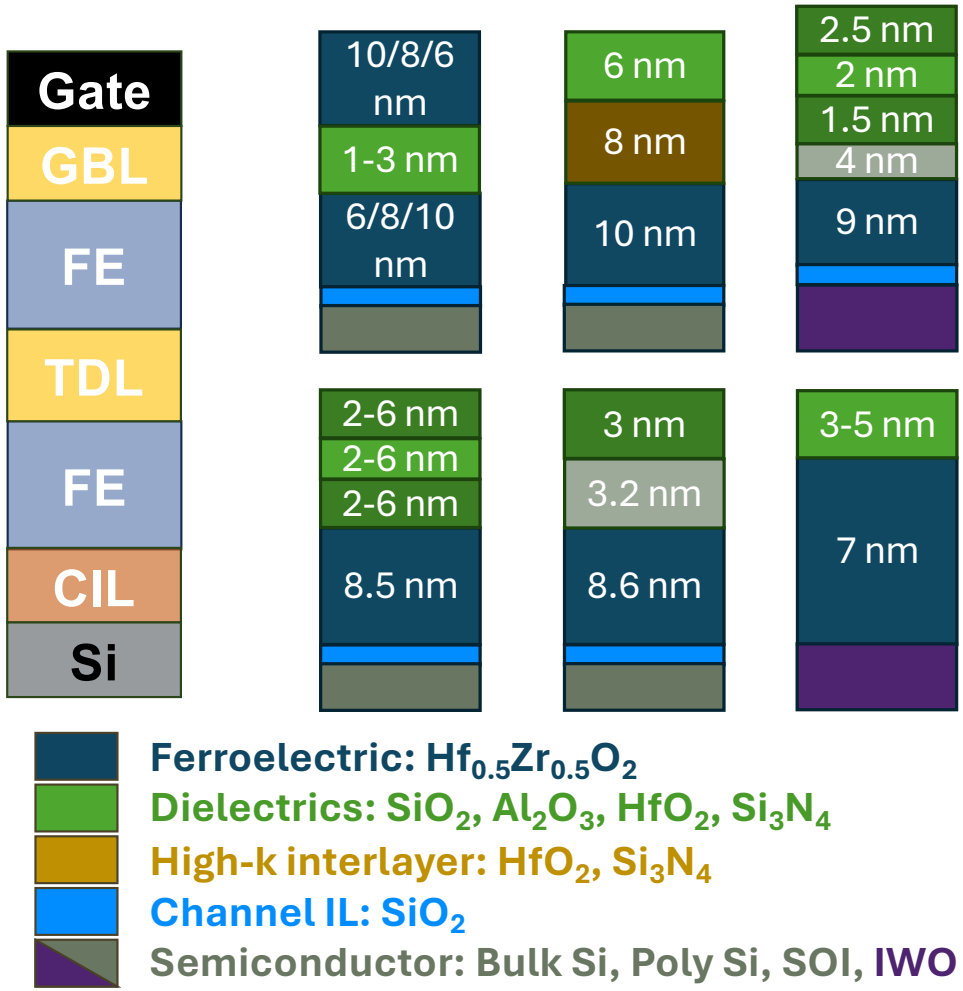
Semiconductor:

- Si
- AOS
- SOI
- Poly-Si

Georgia Tech

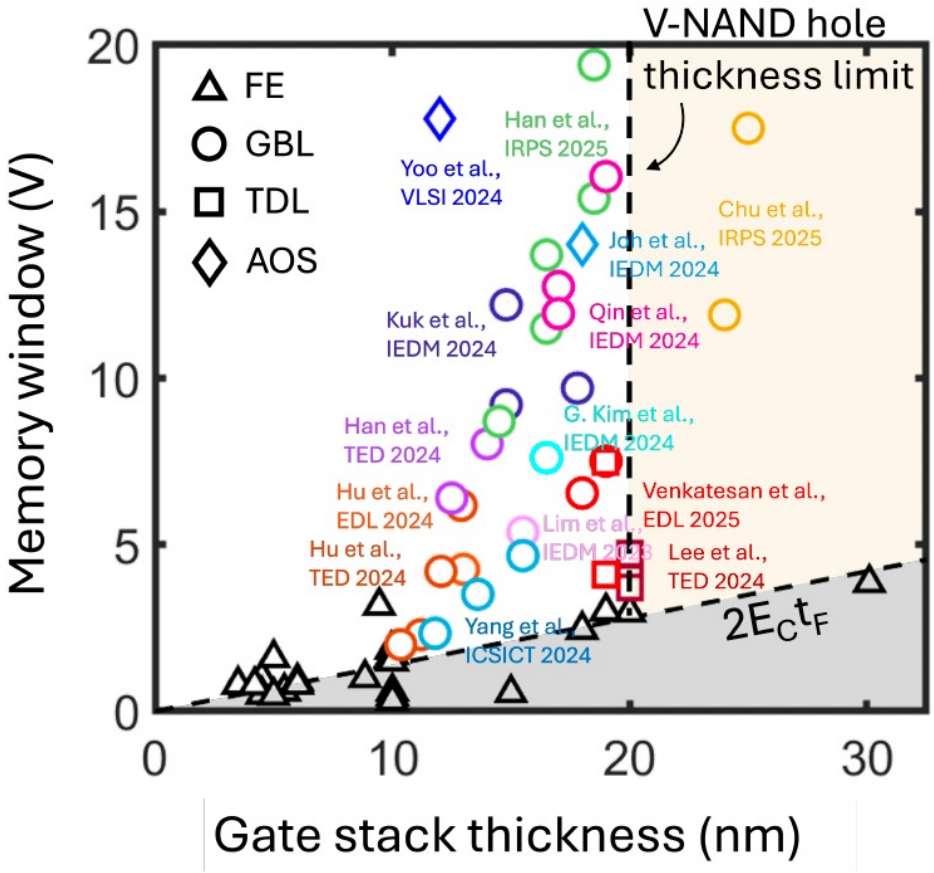
Increasing the MW by dielectric insertion

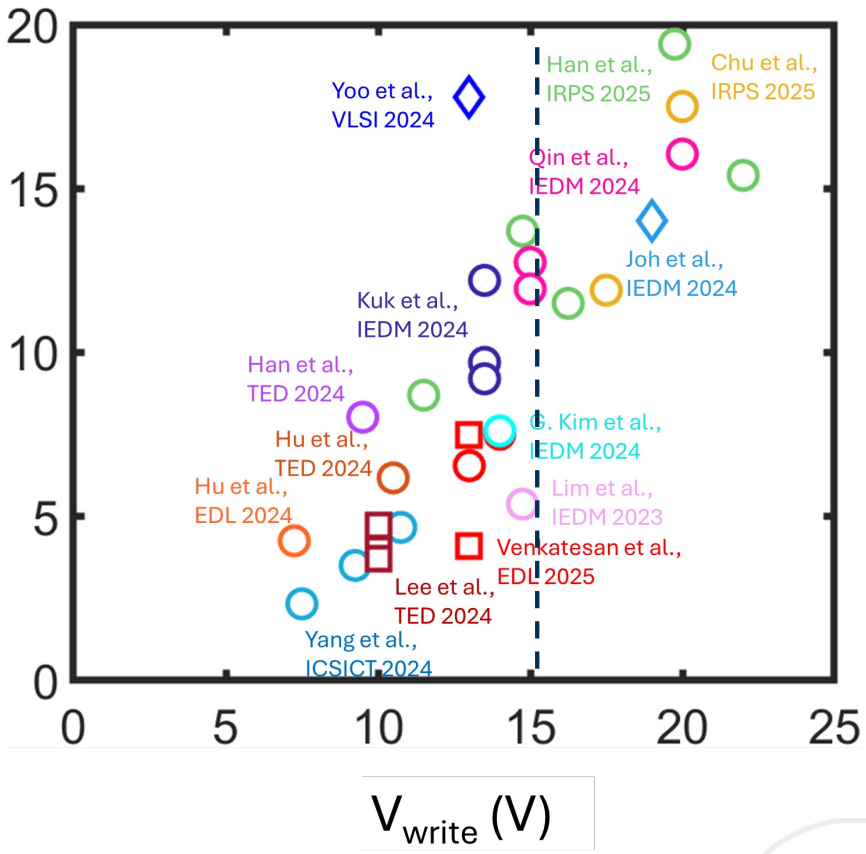




Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$
Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4
High-k interlayer: HfO_2, Si_3N_4
Channel IL: SiO_2
Semiconductor: Bulk Si, Poly Si, SOI, IWO

Increasing the MW by dielectric insertion





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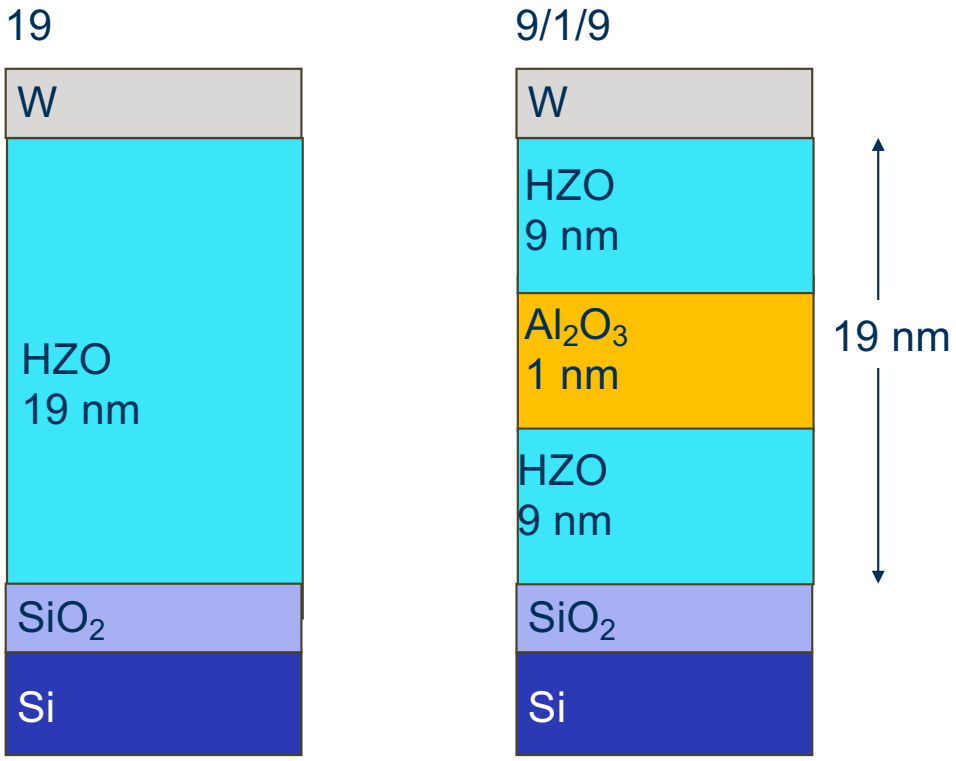
Where is the MW enhancement coming from?



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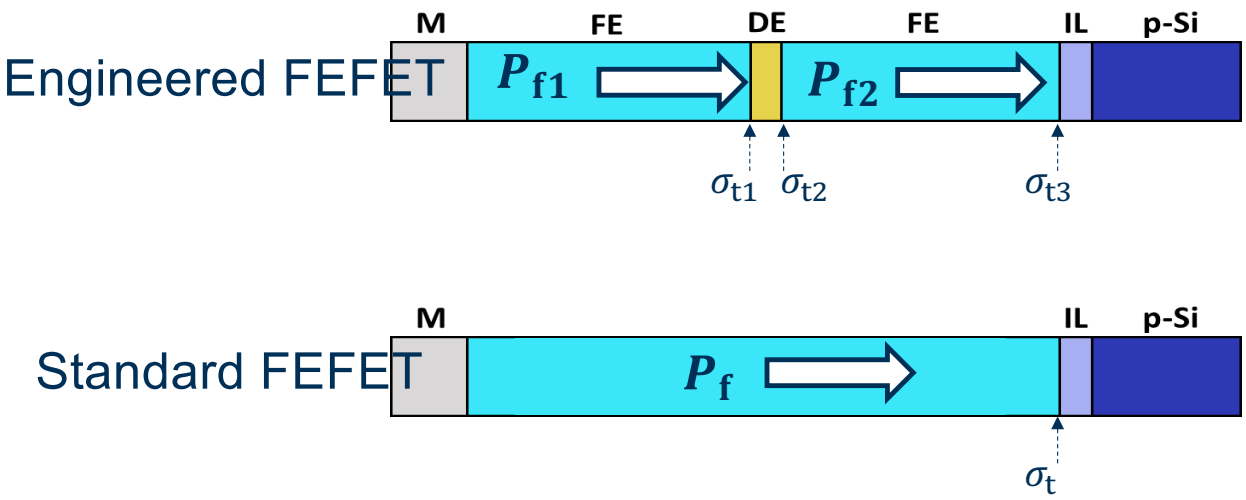
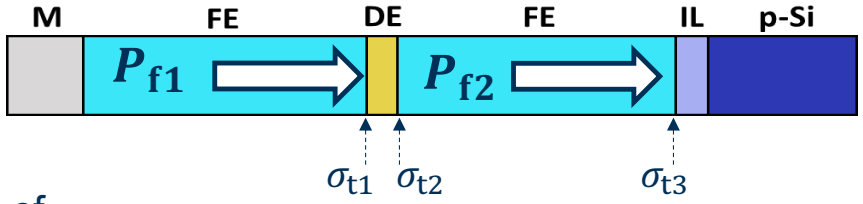
Where is the MW enhancement coming from?



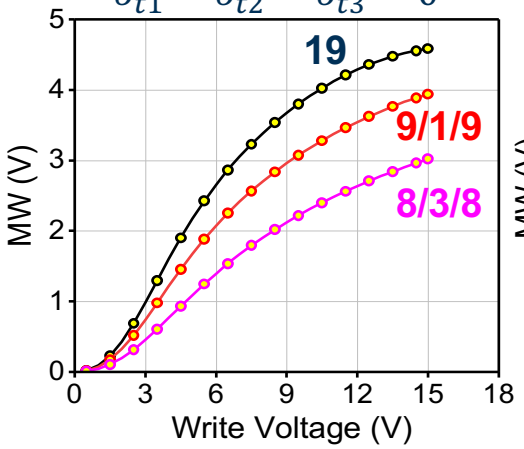
Trapped charges are the key differentiator.

Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

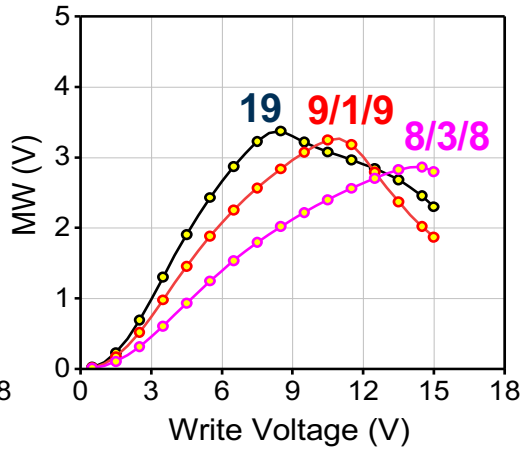
Decoupling the impacts of different trapping mechanisms



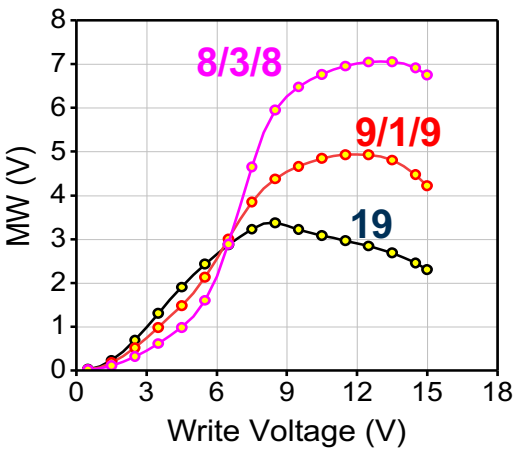
Absence of screening trap charges
$\sigma_{t1} = \sigma_{t2} = \sigma_{t3} = 0$



HZO/SiO_2 Traps only
$\sigma_{t1} = \sigma_{t2} = 0;\ \sigma_{t3} \neq 0$



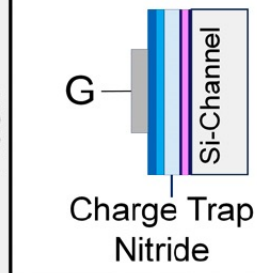
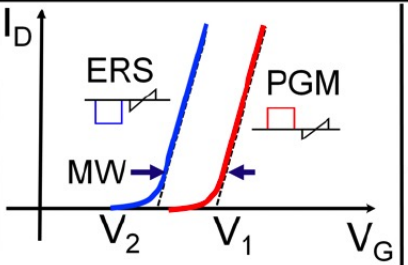
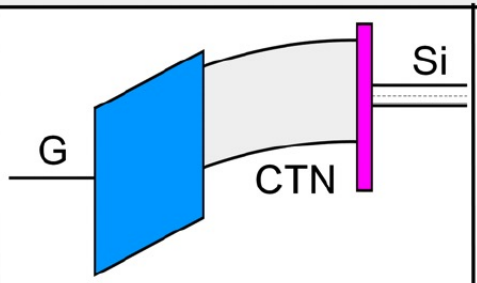
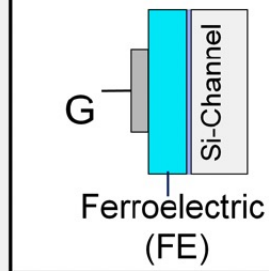
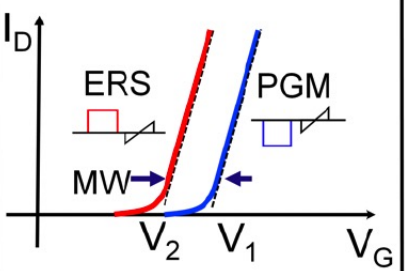
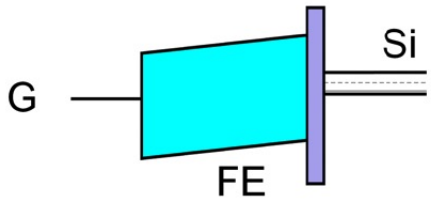
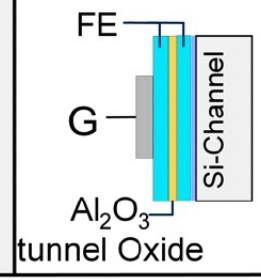
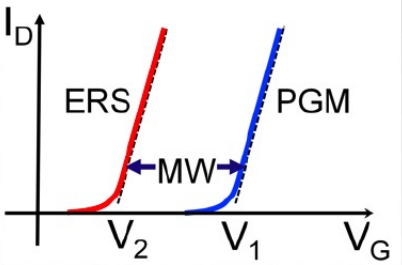
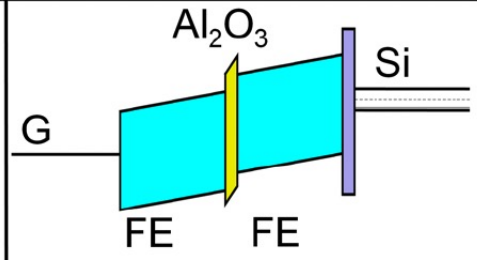
Al_2O_3/HZO + HZO/SiO_2 Traps
$\sigma_{t1} \neq 0;\ \sigma_{t2} \neq 0;\ \sigma_{t3} \neq 0$



Trap effects are responsible for the observed MW trend
(MW: 8/3/8 >9/1/9>19)

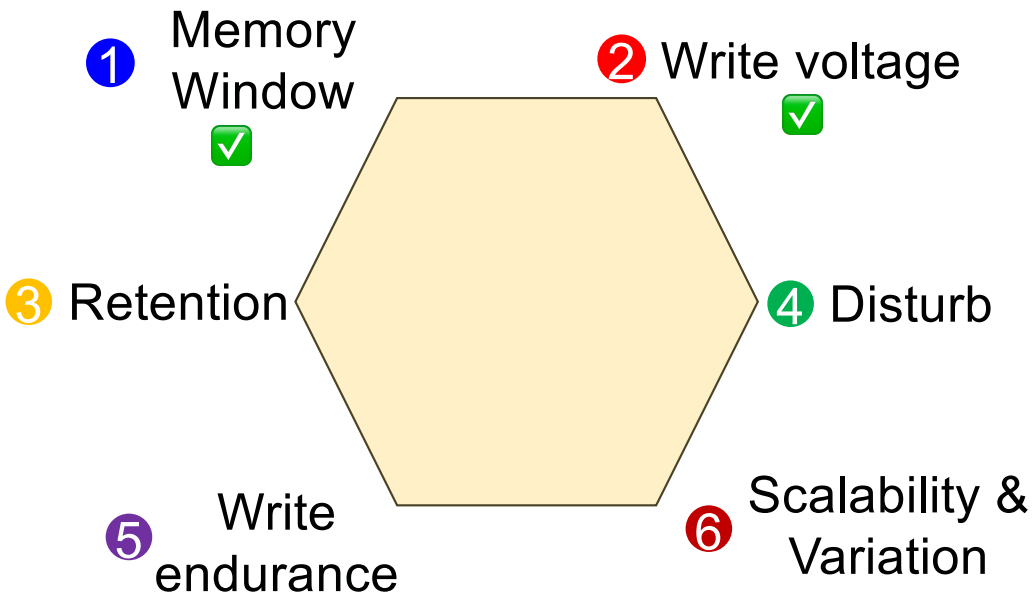
Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

Charge trap flash vs ferroelectric flash

	Structure	Characteristics	Band diagram at FB condition	Attributes
Charge Trap Flash				✓ Large MW × Large Write Voltage Mechanism: Trapping
Conventional FEFET				× Low MW ✓ Low Write Voltage Mechanism: Polarization Switching
Proposed FEFET				✓ Large MW ✓ Moderate Write Voltage Mechanism: Polarization Switching + Trapping + Tunneling

Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

Evaluating ferroelectric NAND Flash



Venkatesan, Khan, et al. "Pushing the limits of NAND technology scaling with ferroelectrics: P. Venkatesan et al." *MRS Bulletin* 50.9 (2025): 1094-1107.

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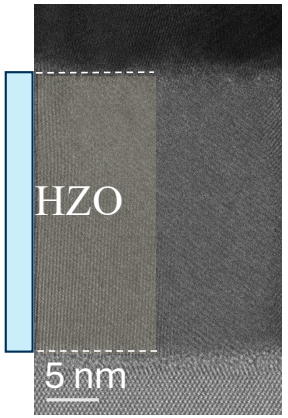
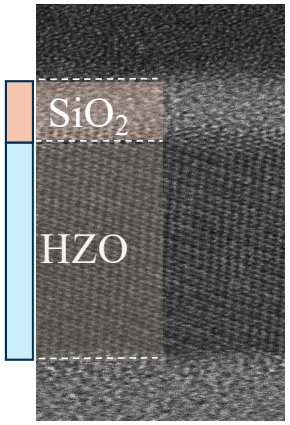
Ferroelectric NAND gate stacks

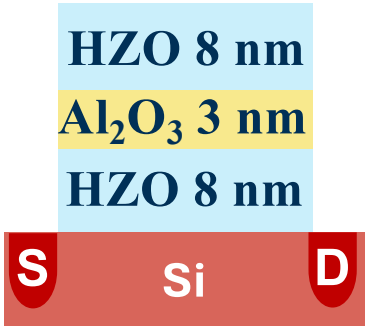
FE (reference)

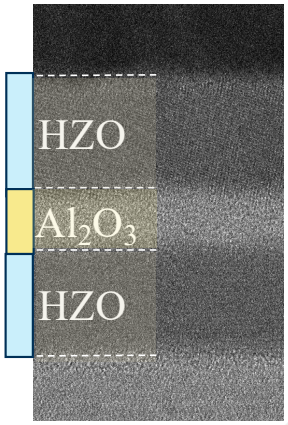


Gate blocking layer (GBL) 14/4(Si)



Tunnel dielectric layer (TDL) 8/3(Al)/8





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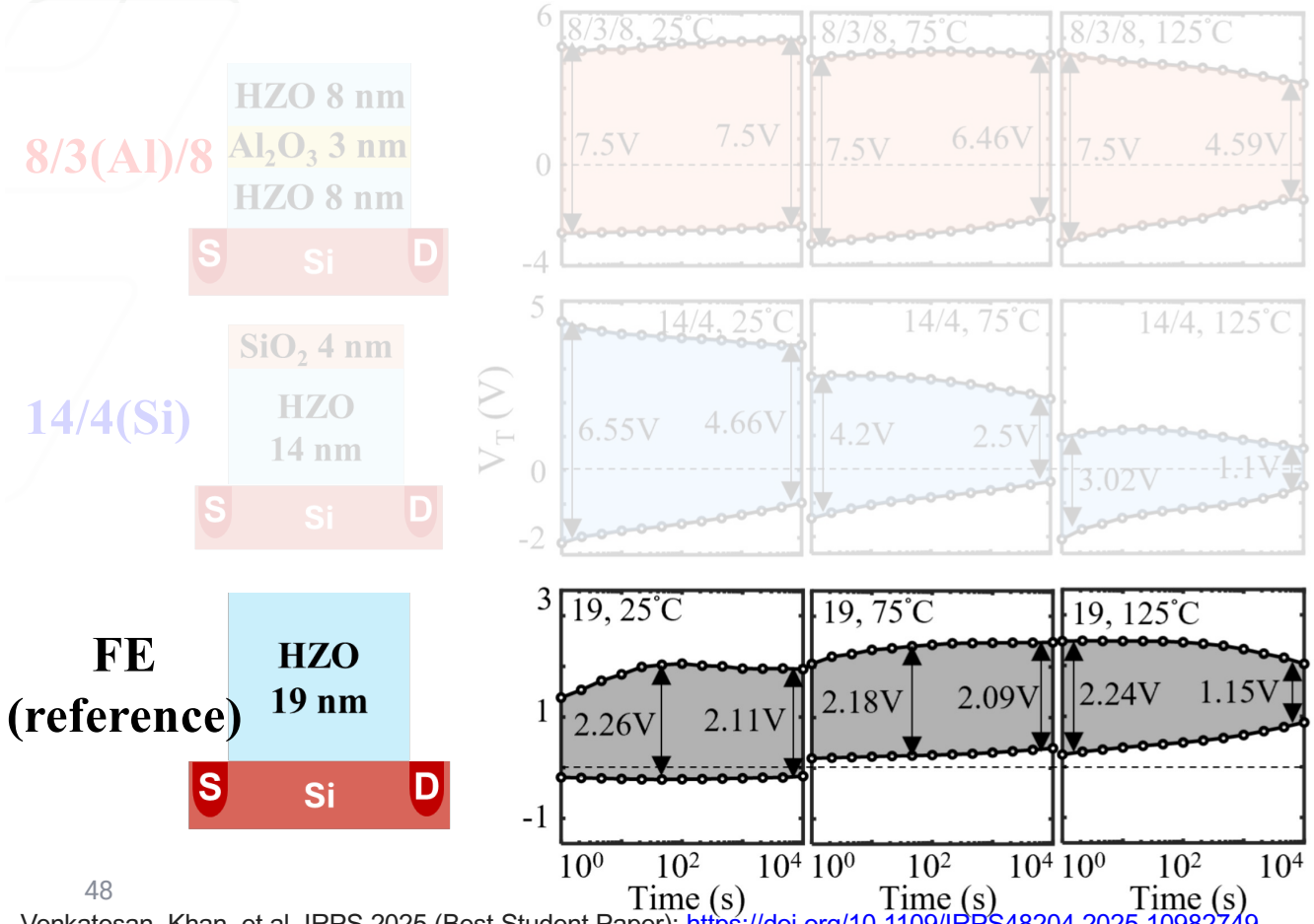
Temperature Dependent Retention for Fe-NAND stacks



Reference stack shows slight degradation at Higher temperature

Venkatesan, Khan, et al. IRPS 2025 (Best Student Paper): https://doi.org/10.1109/IRPS48204.2025.10982749
Venkatesan, Khan, et al. EDL 2025 (Editor's Pick): 10.1109/LED.2024.3523235

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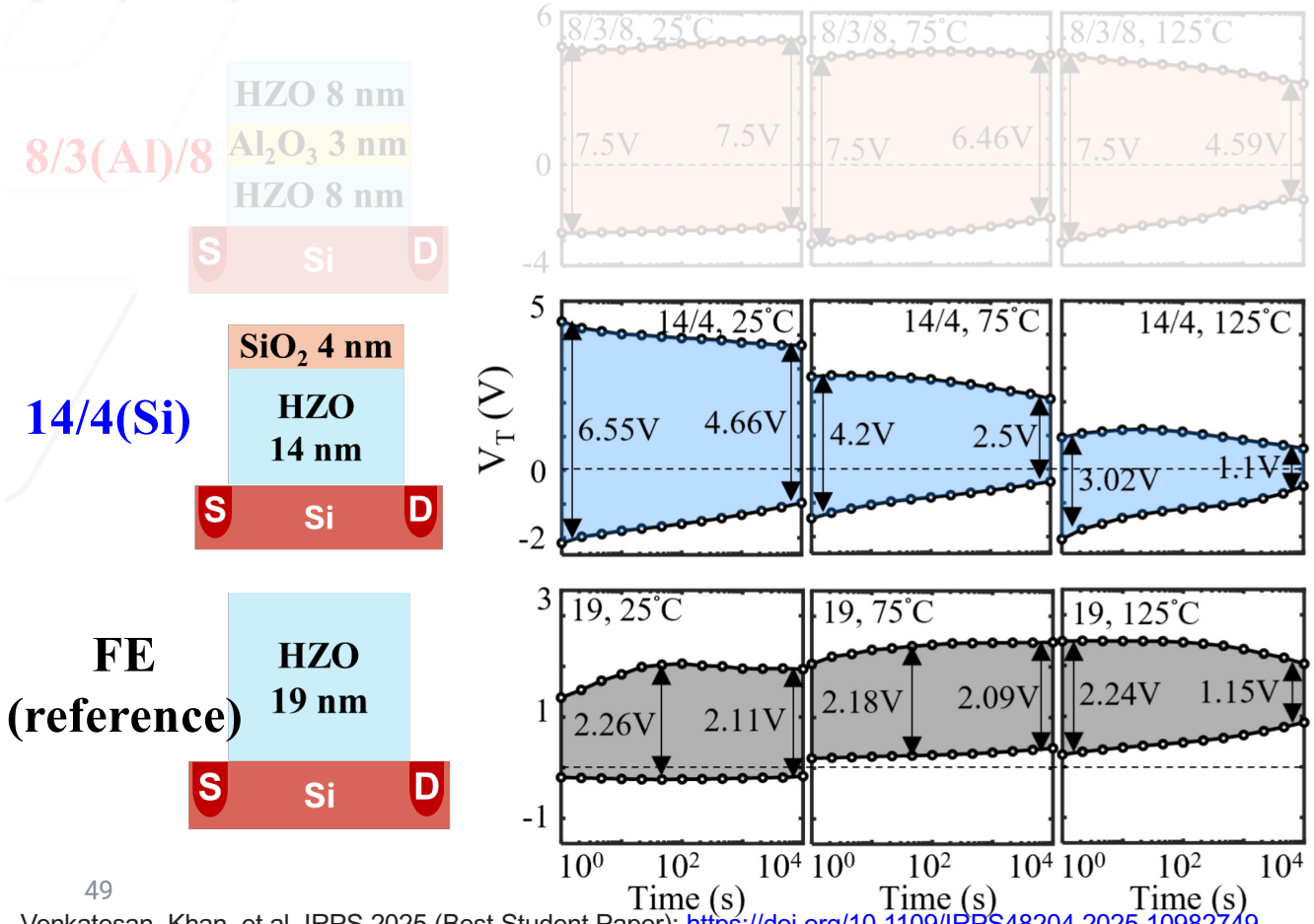
Temperature Dependent Retention for Fe-NAND stacks



GBL stack has lower initial MW at high temperature, but MW loss remain the same

Reference stack shows slight degradation at Higher temperature

Venkatesan, Khan, et al. IRPS 2025 (Best Student Paper): https://doi.org/10.1109/IRPS48204.2025.10982749
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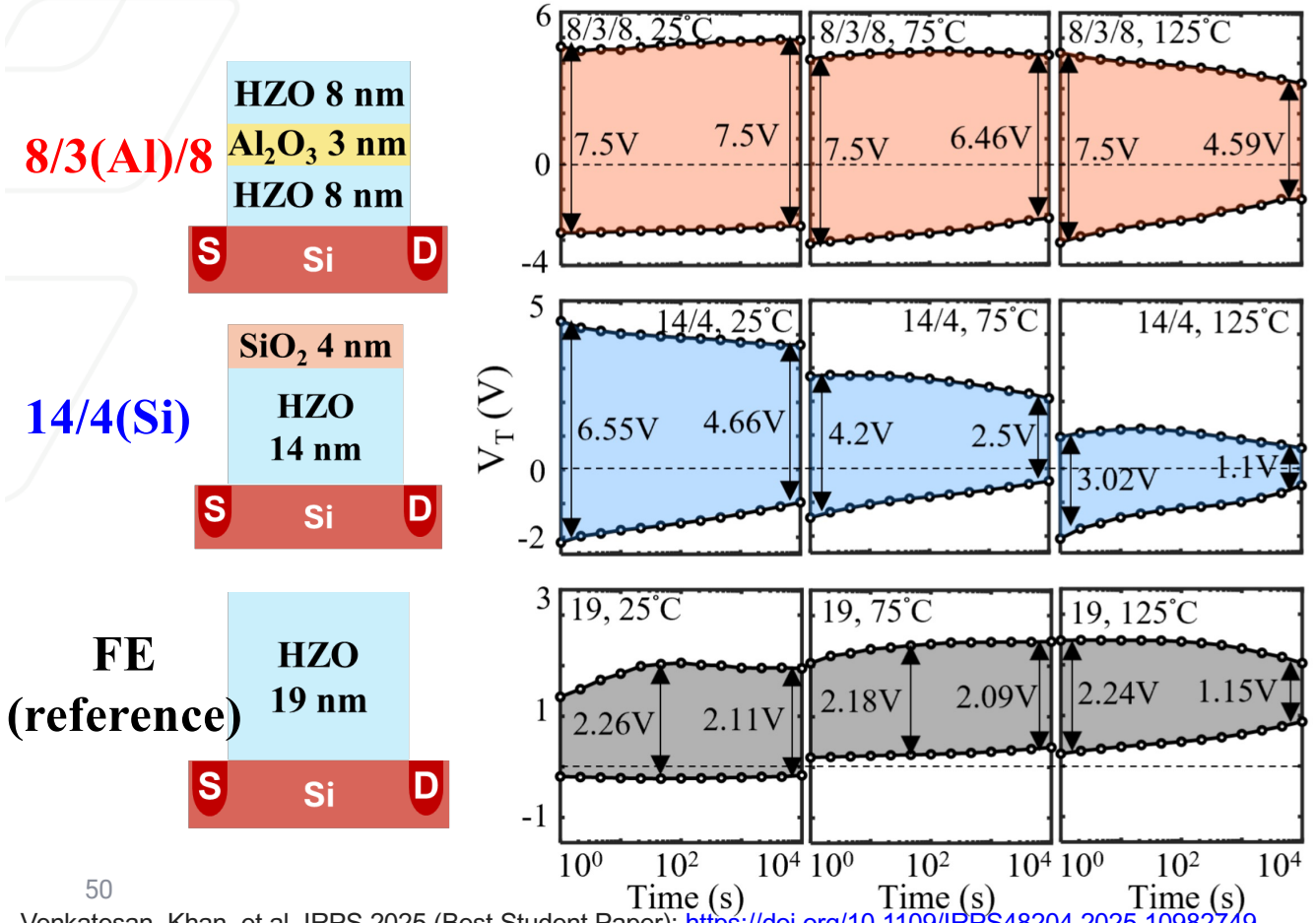
Temperature Dependent Retention for Fe-NAND stacks



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Venkatesan, Khan, et al. EDL 2025 (Editor's Pick): 10.1109/LED.2024.3523235

YouTube Link: https://youtu.be/wYLvvmKorGQ?si=wLm34Tboy9SmMhXQ

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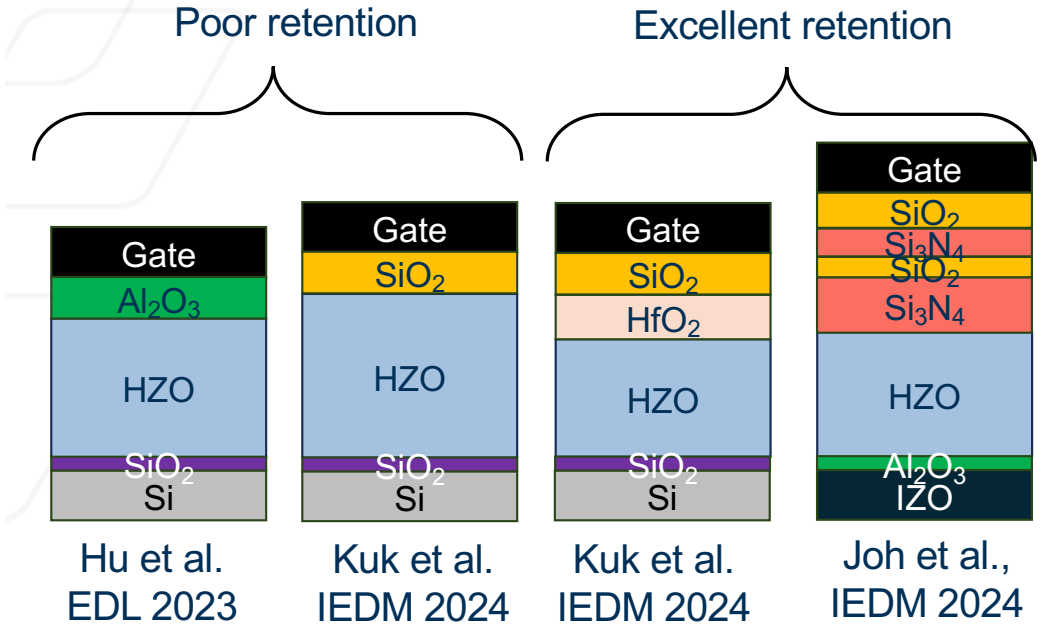
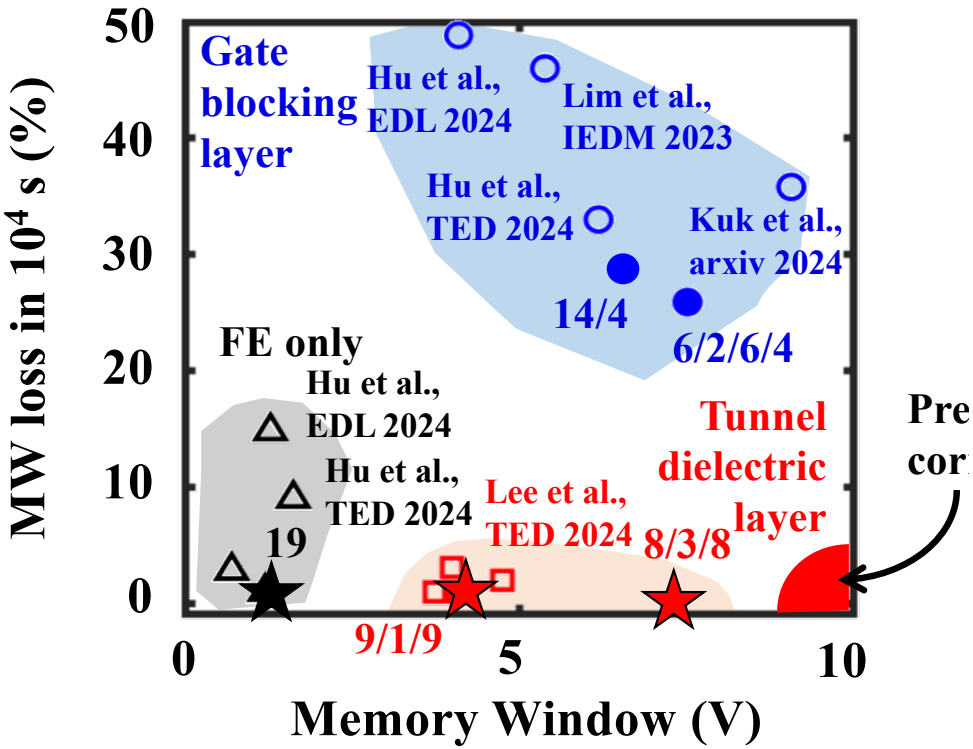
Retention benchmark





Kuk et al.
IEDM 2024

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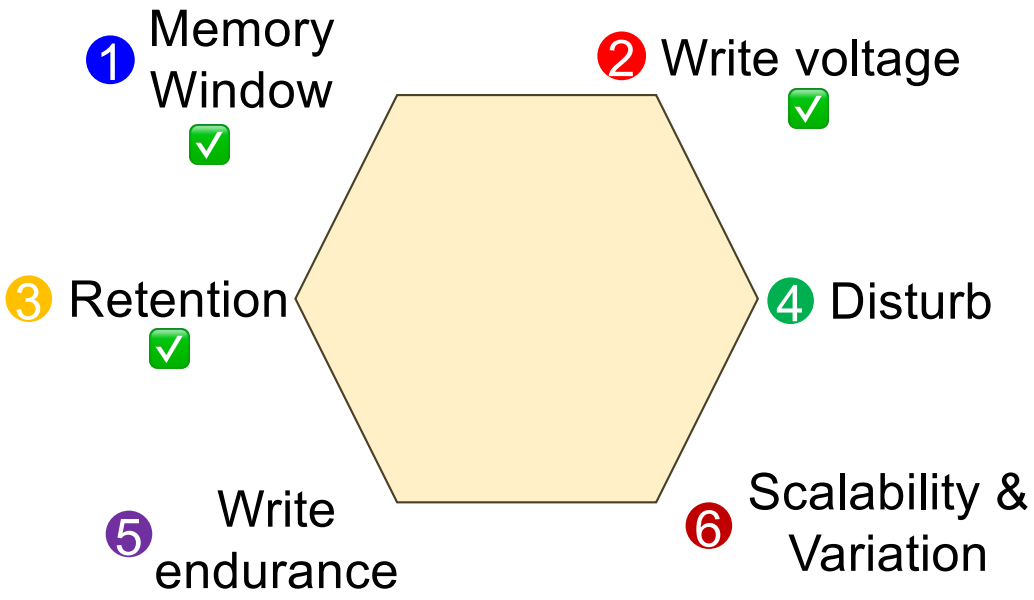
Evaluating ferroelectric NAND Flash



Venkatesan, Khan, et al. "Pushing the limits of NAND technology scaling with ferroelectrics: P. Venkatesan et al." *MRS Bulletin* 50.9 (2025): 1094-1107.

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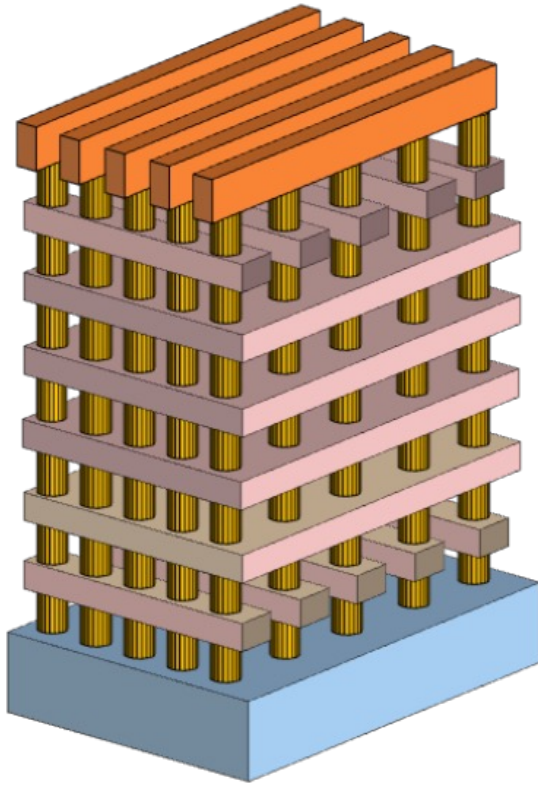
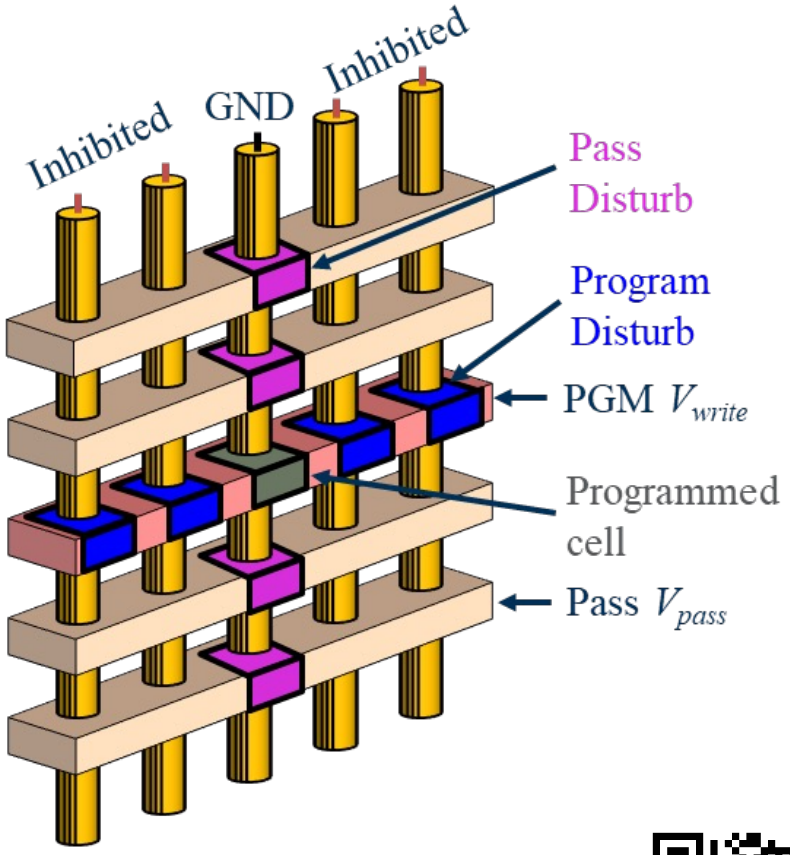
Disturb in Ferroelectric NAND

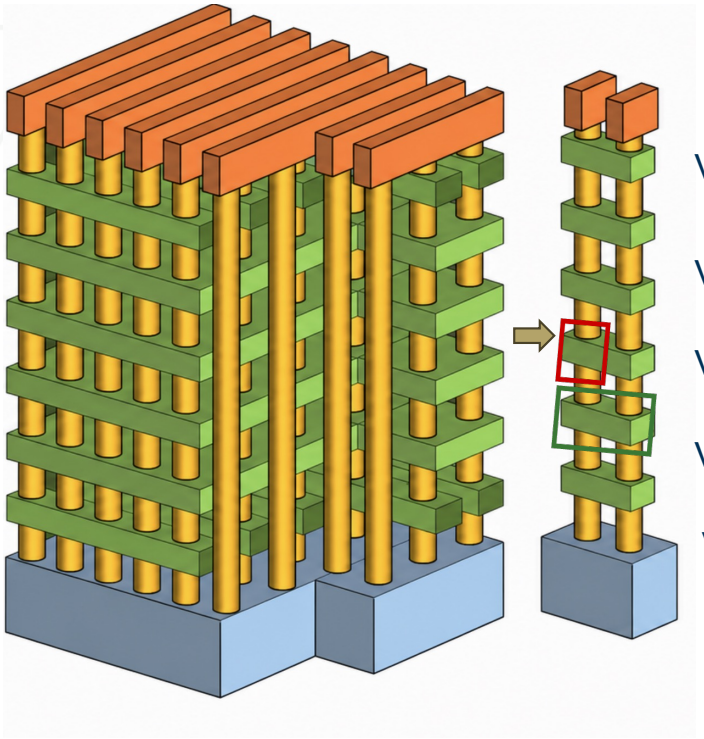


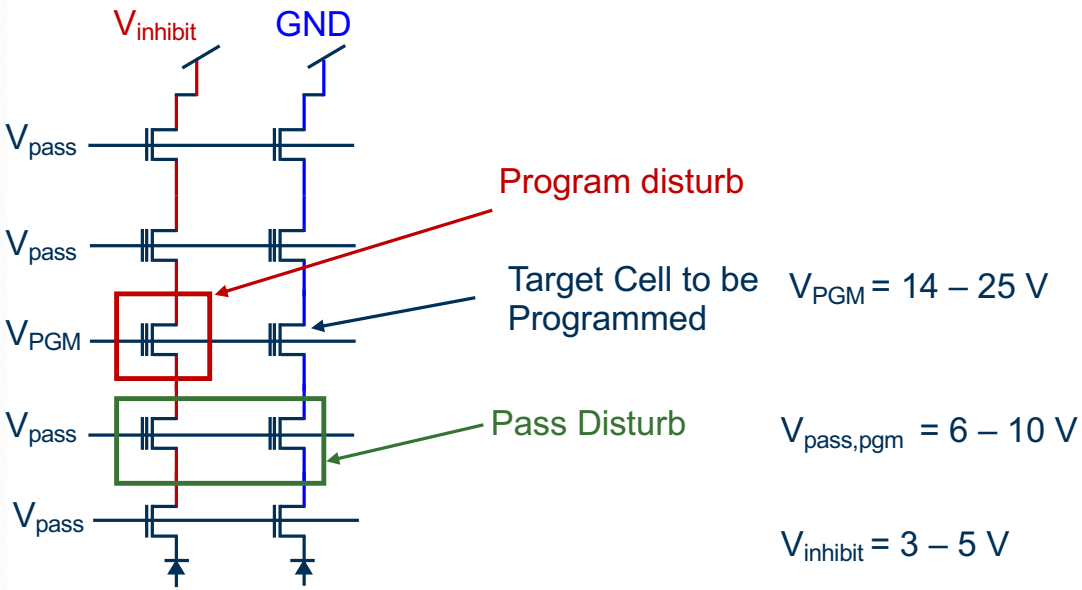


A pass voltage is applied to unaddressed cells while accessing a different cell along the bit line. This pass voltage could disturb the V_T of the cell either due to electron trapping or polarization back switching.

Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

Program and Pass Disturb





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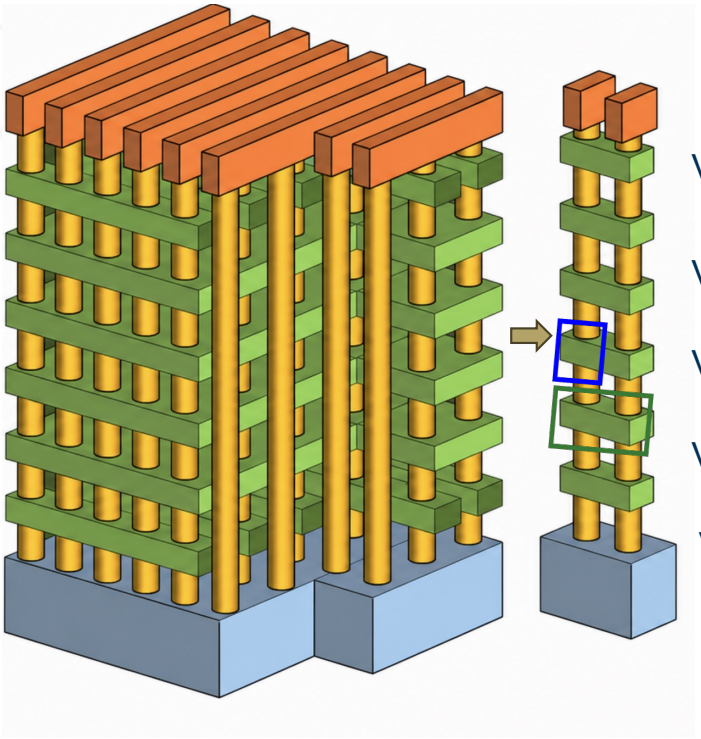
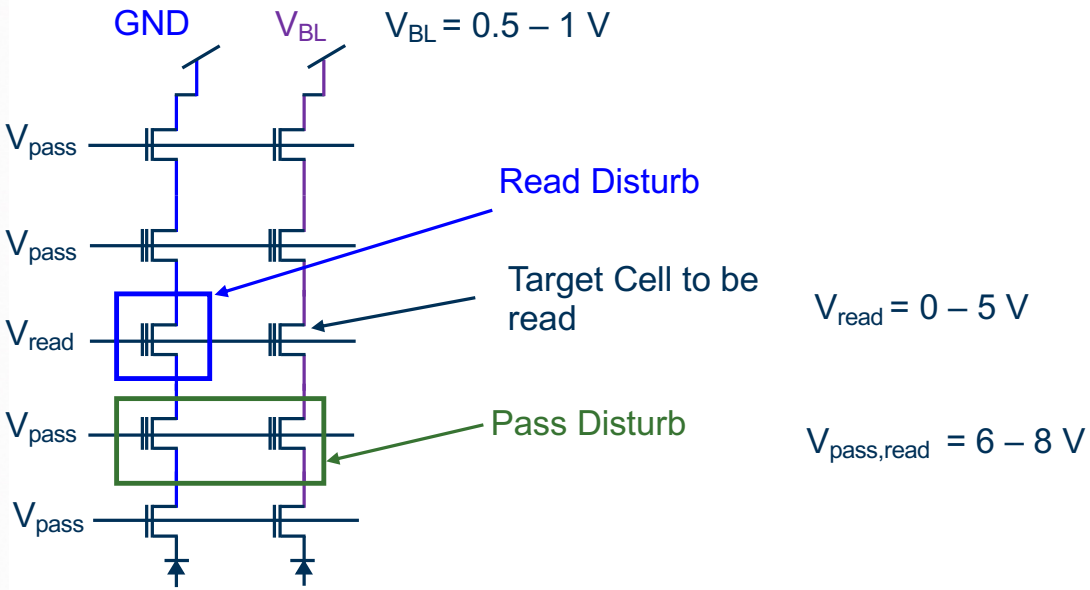
Read and Pass Disturb





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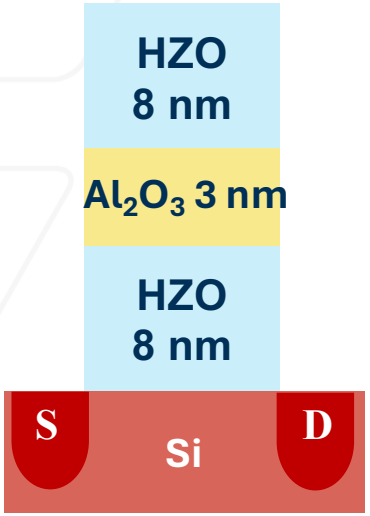
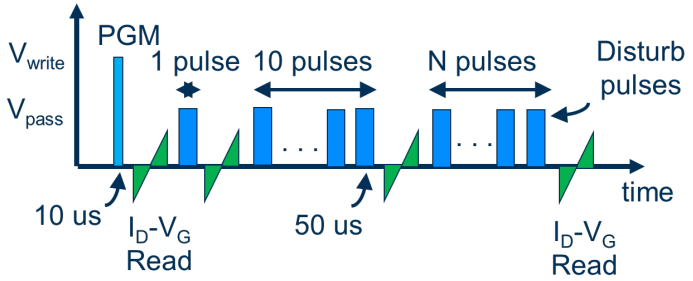
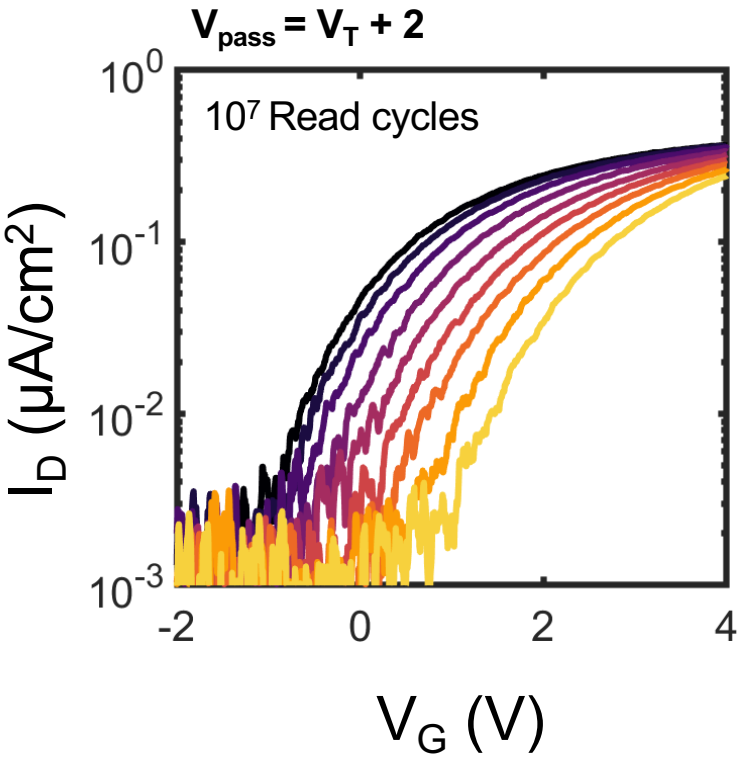
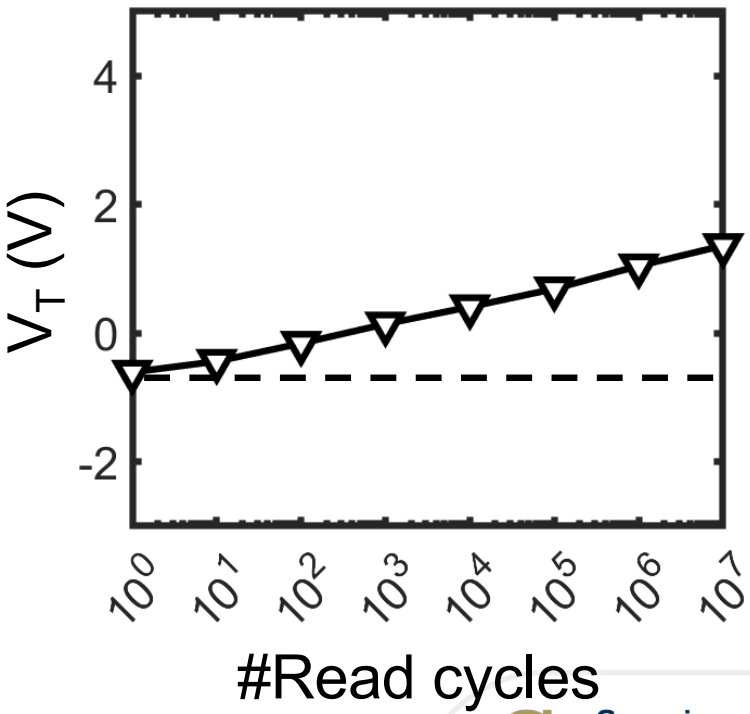
Disturb characterization









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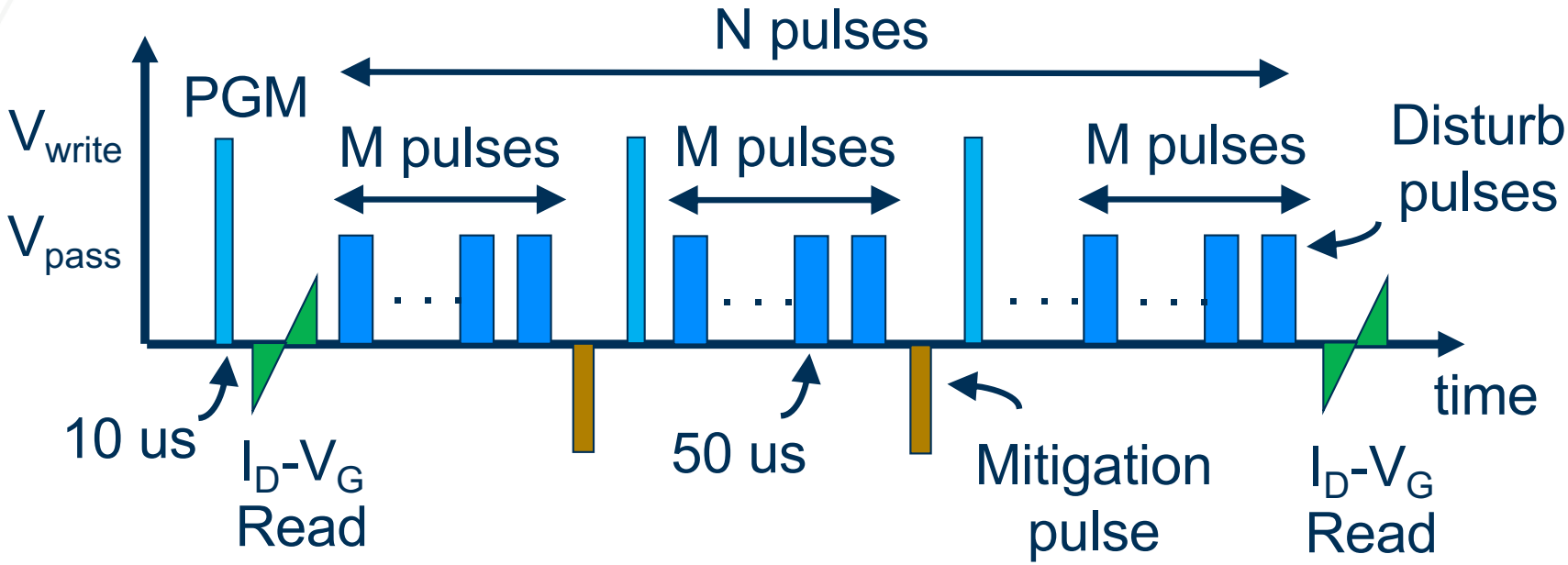
P. Venkatesan *et al*., "Disturb and its Mitigation in Ferroelectric Field-Effect Transistors With Large Memory Window for NAND Flash Applications," in *IEEE Electron Device Letters*, vol. 45, no. 12, pp. 2367-2370, Dec. 2024, doi: 10.1109/LED.2024.3467210

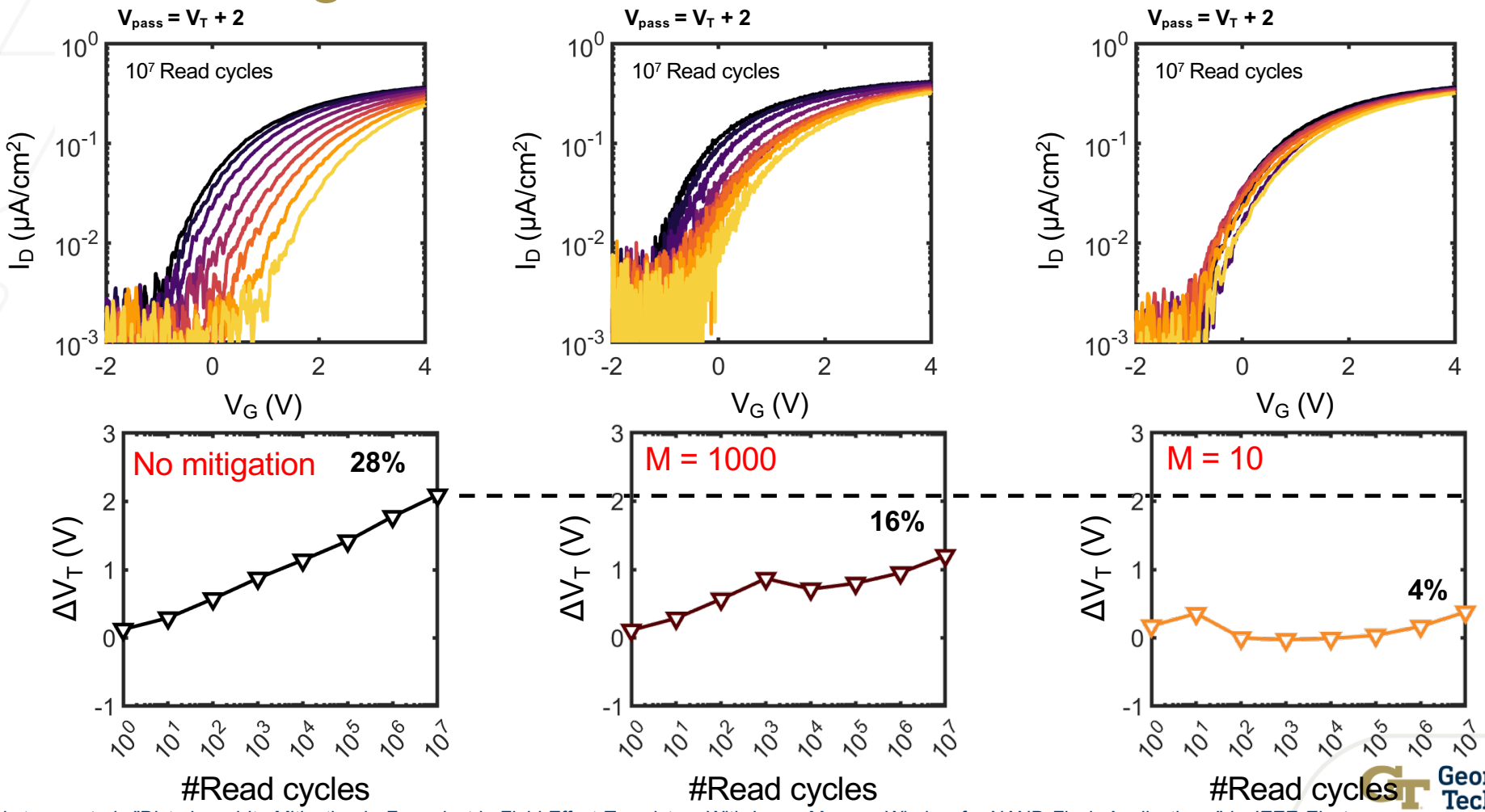
A Disturb Mitigation Scheme for ferroelectric NAND



We introduce a mitigation pulse to detrap the electrons trapped due to the disturb pulses

P. Venkatesan *et al*., "Disturb and its Mitigation in Ferroelectric Field-Effect Transistors With Large Memory Window for NAND Flash Applications," in *IEEE Electron Device Letters*, vol. 45, no. 12, pp. 2367-2370, Dec. 2024, doi: 10.1109/LED.2024.3467210

A Disturb Mitigation Scheme for ferroelectric NAND



P. Venkatesan *et al*., "Disturb and its Mitigation in Ferroelectric Field-Effect Transistors With Large Memory Window for NAND Flash Applications," in *IEEE Electron Device Letters*, vol. 45, no. 12, pp. 2367-2370, Dec. 2024, doi: 10.1109/LED.2024.3467210

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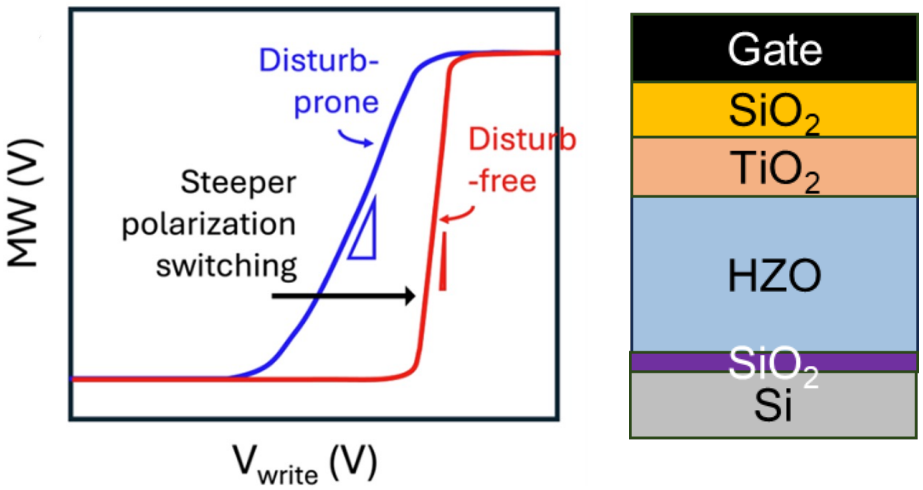
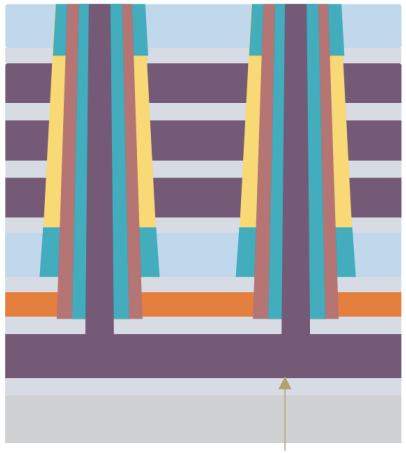
Techniques to mitigate disturb



Inserting a TiO2 layer in GBL can reduce disturb.

G. Kim, et. al., IEDM 2024,
doi: 10.1109/IEDM50854.2024.10873411



Oxide filler replaced by a metallic filler.

Pass operation is performed by a separate non-ferroelectric gate stack so that the ferroelectric state is not disturbed

X. Niu, et. al., IEDM 2025,
doi: doi: 10.1109/IEDM50572.2025.11353563

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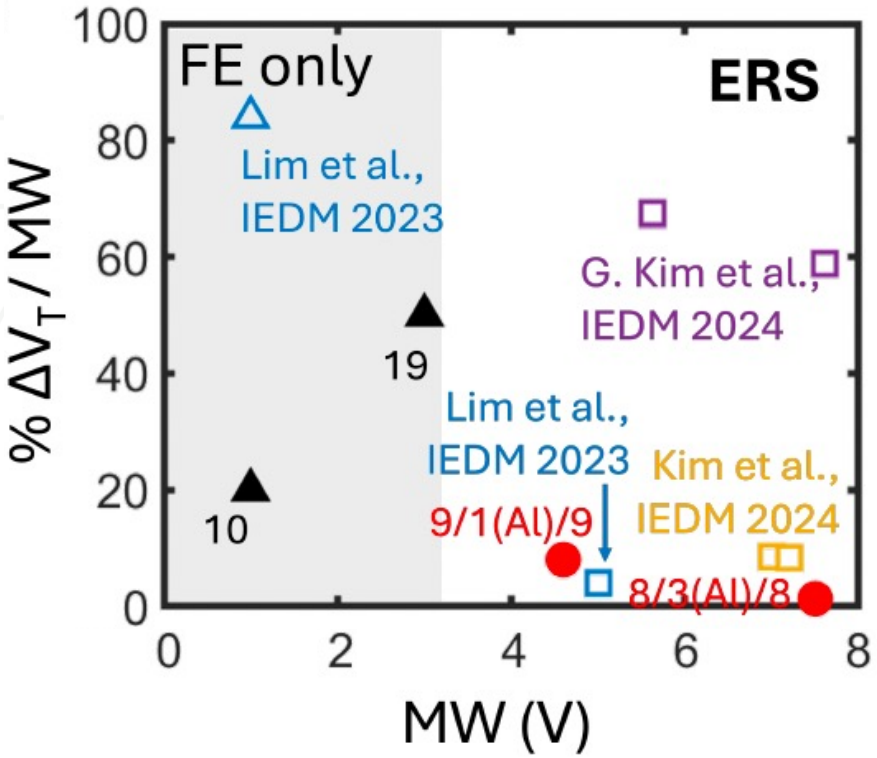
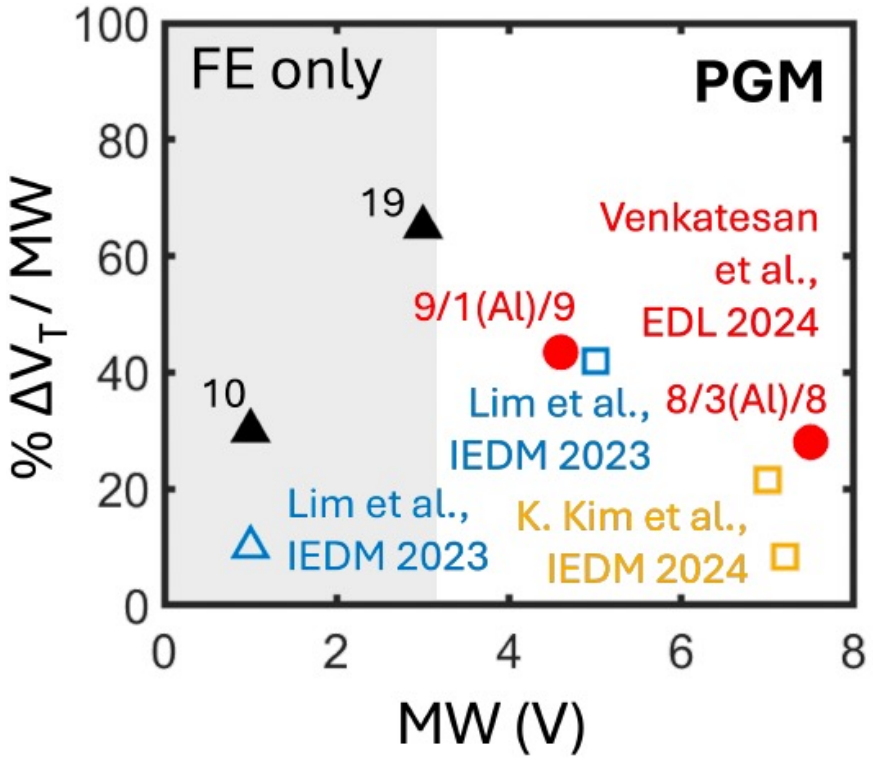
Pass disturb





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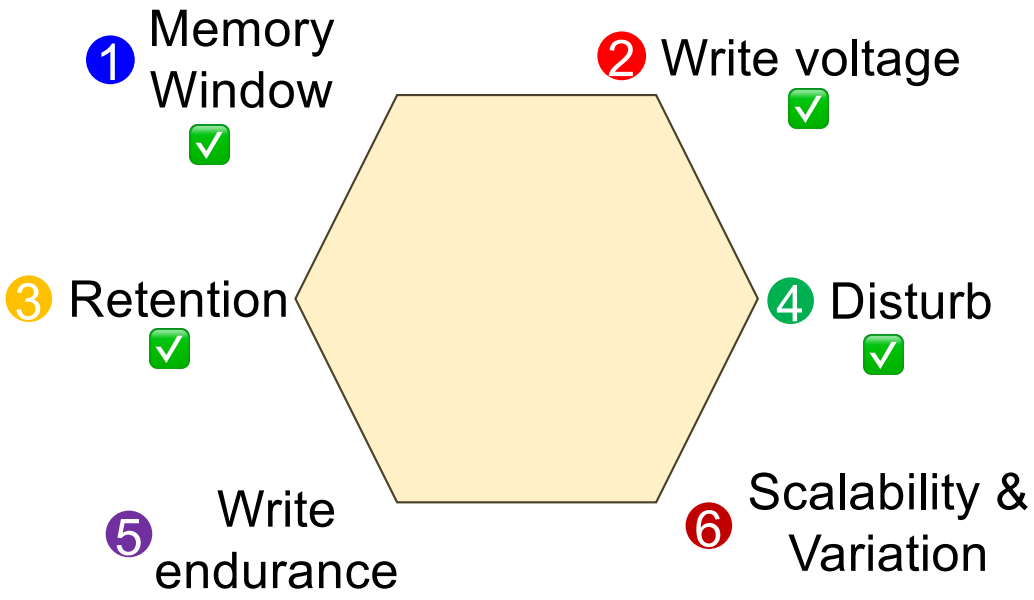
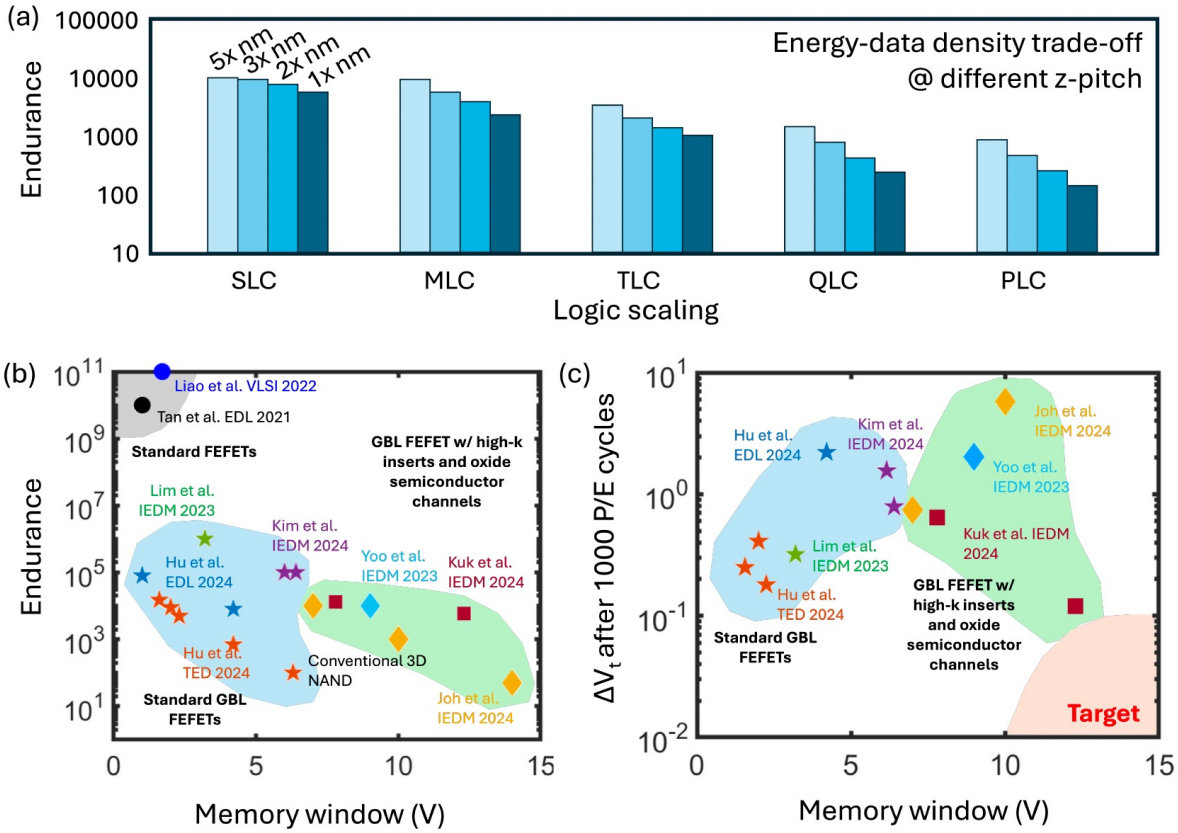
Evaluating ferroelectric NAND Flash



Venkatesan, Khan, et al. "Pushing the limits of NAND technology scaling with ferroelectrics: P. Venkatesan et al." *MRS Bulletin* 50.9 (2025): 1094-1107.

Write Endurance



Venkatesan, P., et al. IMW 2025

Endurance decreases with increasing MW

IL degradation drives V_t shift in FEFETs

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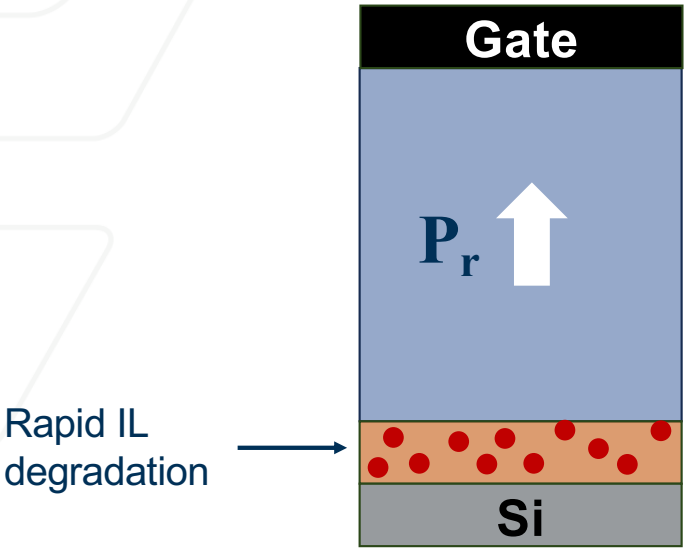
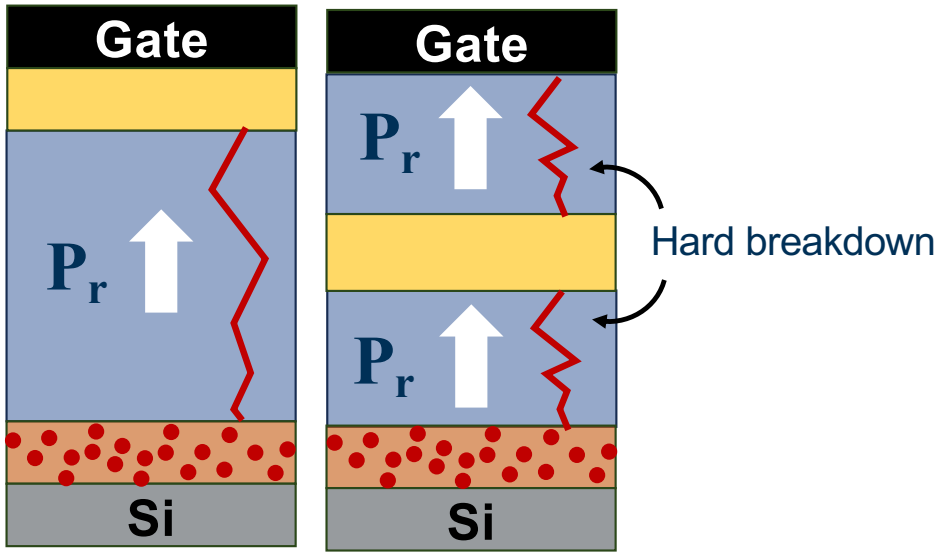
Write Endurance

Standard FEFETs



- Small MW
- V_{write} / V_{BD} lower than 1
- IL degradation dominates
- MW closure
- Minimal FE degradation

Engineered FEFETs



- Large MW
- V_{write} / V_{BD} close to 1
- Rapid IL degradation
- Increased risk of hard breakdown

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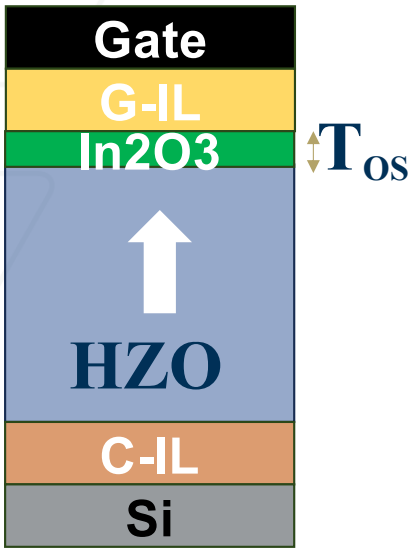
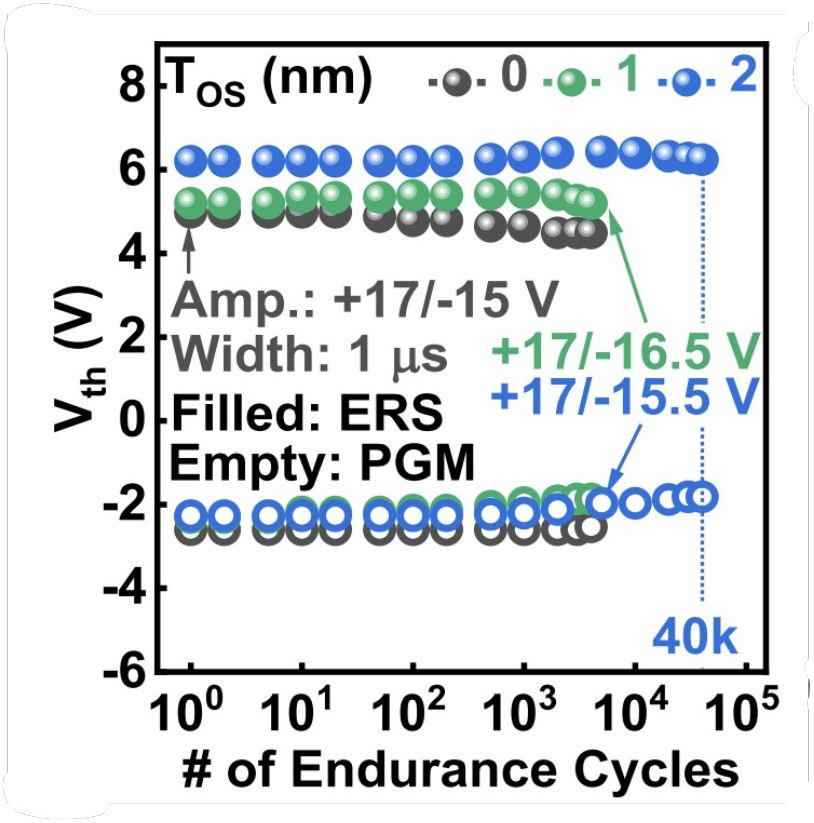
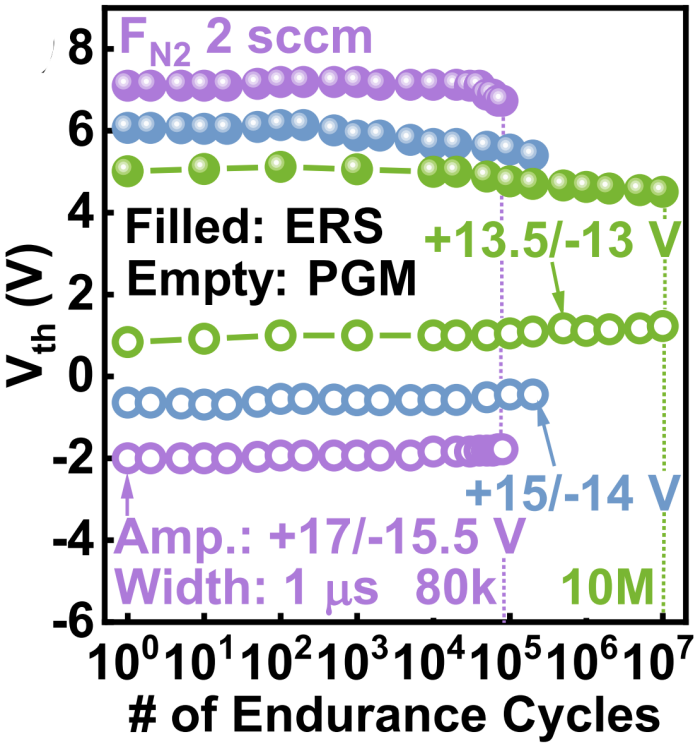
Insertion of Oxygen Resorvior Layer to improve Fe-NAND endurance







Introducing In2O3 layer acts as oxygen reservoir layer for HZO layer to enable larger MW and high endurance by optimizing the thickness and deposition parameters of the ORL layer

H. Kang, et, al., IEDM 2025, TED 2026

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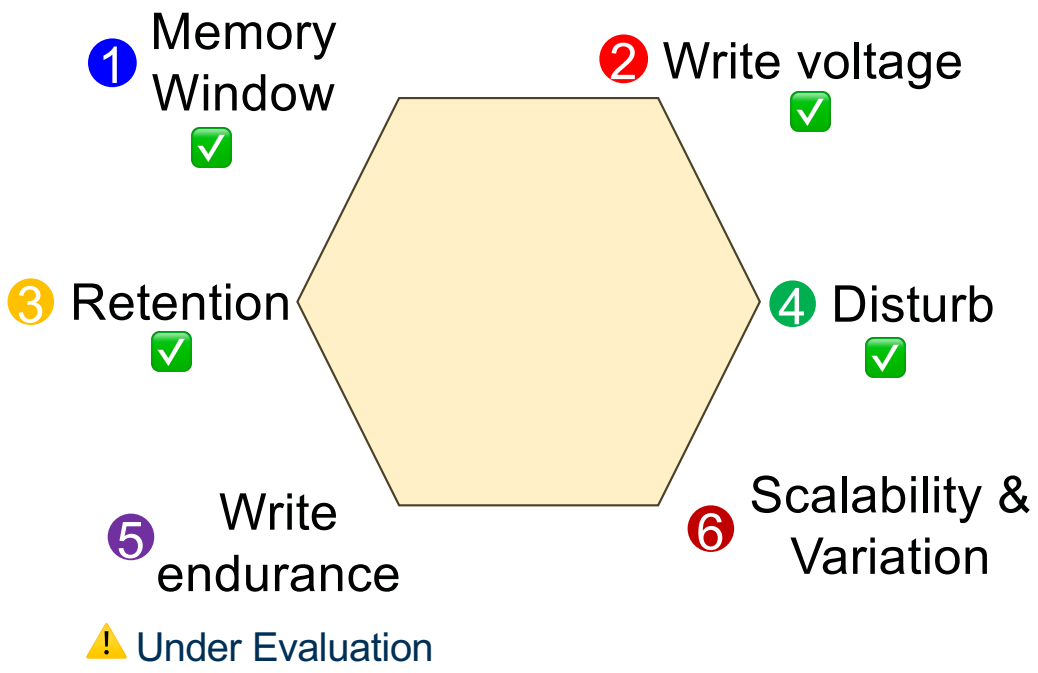
Evaluating ferroelectric NAND Flash



Venkatesan, Khan, et al. "Pushing the limits of NAND technology scaling with ferroelectrics: P. Venkatesan et al." *MRS Bulletin* 50.9 (2025): 1094-1107.

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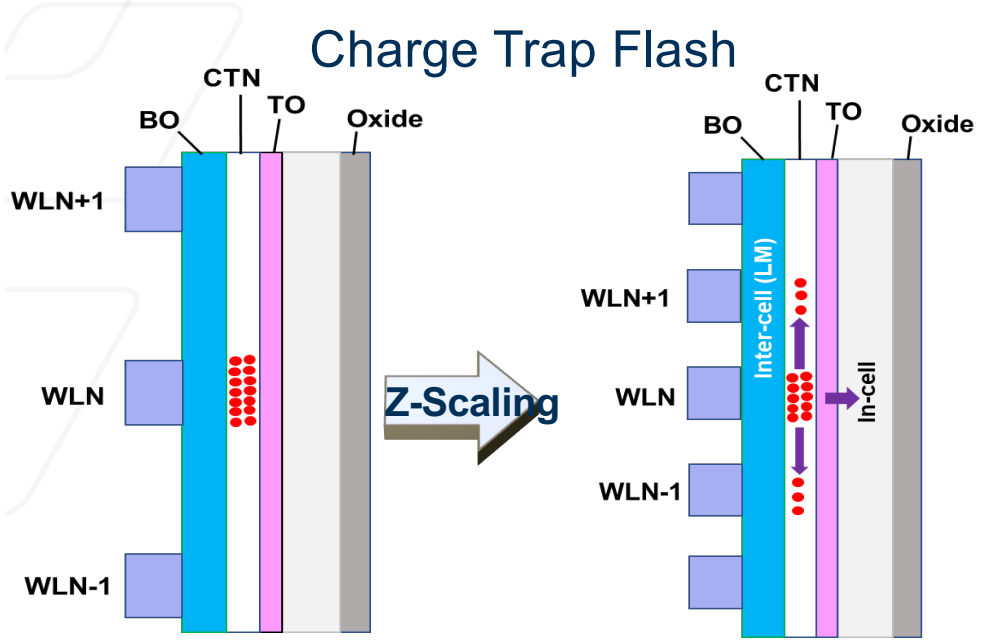
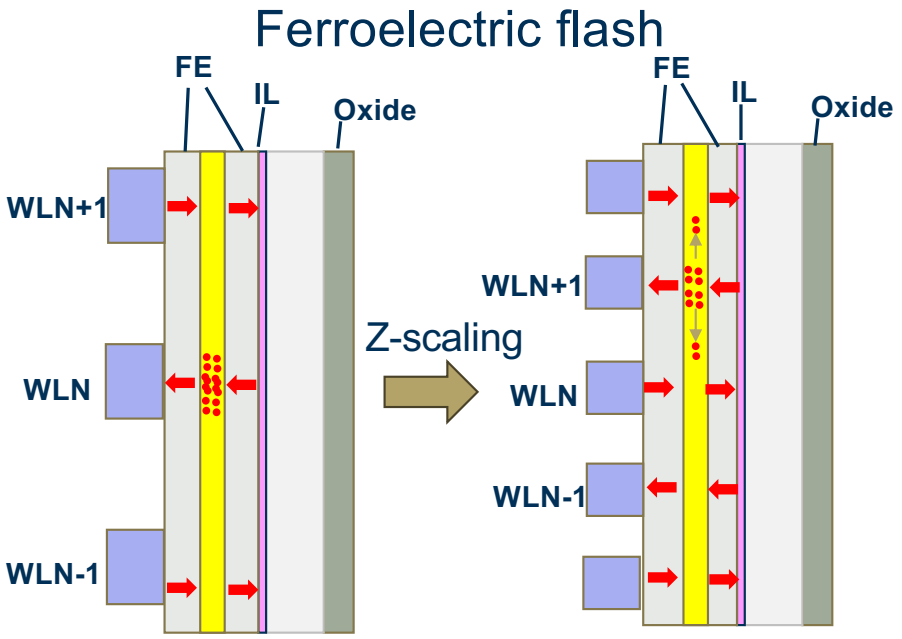
Lateral charge migration



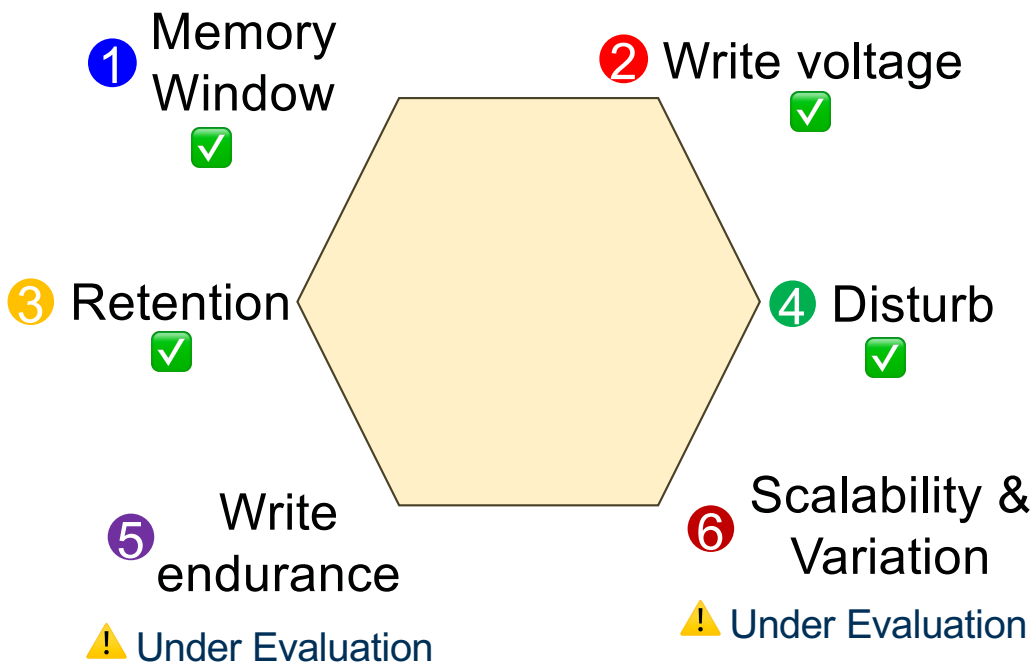
Lateral charge migration prevents aggressive Z-scaling for 3D NAND.



The nature of trapped charges at the ferroelectric—interlayer interface will determine the scaling potential of ferroelectric 3D NAND technology.

66

Evaluating ferroelectric NAND Flash



Venkatesan, Khan, et al. "Pushing the limits of NAND technology scaling with ferroelectrics: P. Venkatesan et al." *MRS Bulletin* 50.9 (2025): 1094-1107.

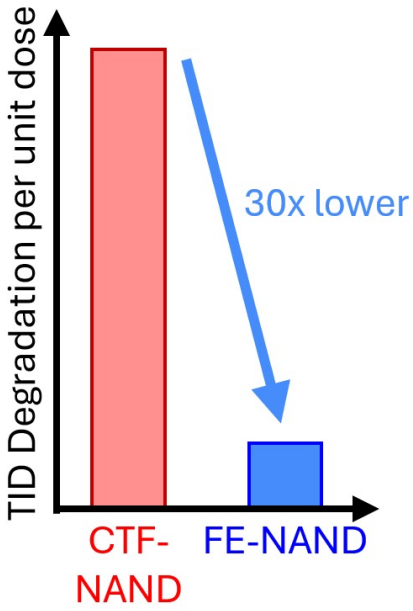
Space applications and ferroelectric NAND flash

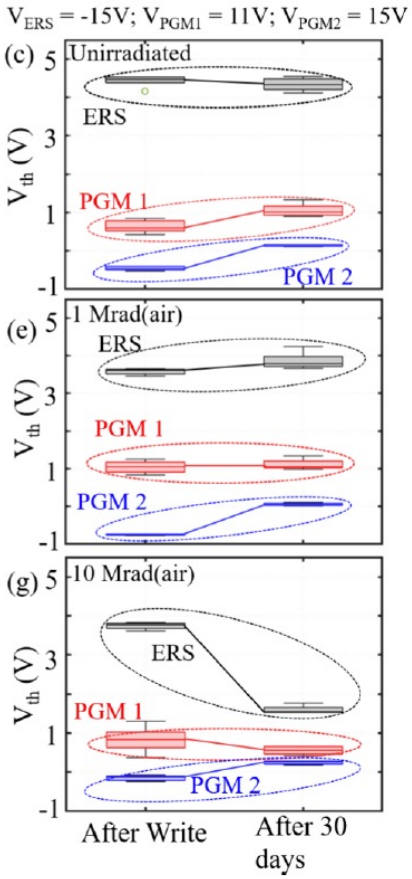
- Space is becoming a key infrastructure layer for **AI, sensing, communication, navigation, and defense**.
- **Spacecraft memories must retain data under extreme radiation.**
  - Radiation dose increases sharply with mission orbit:
    LEO satellites: **5–30 krad**
    GEO missions: **100–300 krad**
    Jupiter/Europa missions: approaching **1 Mrad**
- **CTF-NAND can show retention loss even at relatively low doses** of approximately **50 krad**, creating risk for long-duration missions.
- **Magnetic storage remains impractical for many spacecraft systems** because of mass, volume, power, and mechanical constraints.

Ferroelectric NAND flash may provide a solution.

Space applications and ferroelectric NAND flash

All properties of ferroelectric NAND transistors, including retention, disturb, and write endurance remain intact up to 1 Mrad TID.





Fernandes, Lance, et al. "Enabling Radiation Hardness in Solid-State NAND Storage Utilizing a Laminated Ferroelectric Stack." *Nano Letters* 26.10 (2026): 3390-3397.

Future work: SEE, displacement damage, retention/endurance after irradiation, disturb behavior, and thermal recovery

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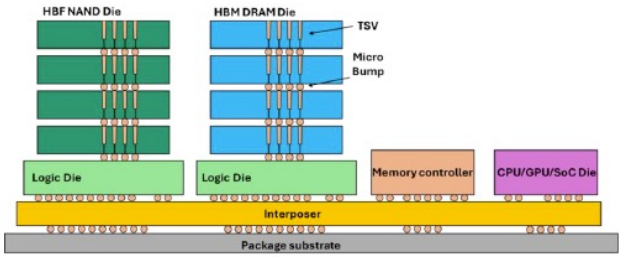
Where NAND is Going Next

1

ACTIVE MEMORY TIER



Workload-tuned NAND

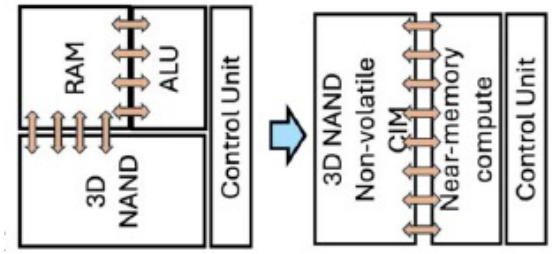
- QLC for cold archival
- SLC-like for inference buffers for AI

One NAND no longer fits all

the right cell for the right job

2

COMPUTE SUBSTRATE



Compute-in-Memory (CIM)

- MAC inside the NAND array
- In-storage vector search for RAG

The array becomes the computer

10–100× lower energy for memory-bound AI

3

RAD-HARD STORAGE

Orbital Infrastructure for AI

- Petabyte storage on satellites
- Deep space missions

NAND leaves the data center

rad-hardness for orbital AI

From a single technology to a portfolio — NAND, tuned to the workload

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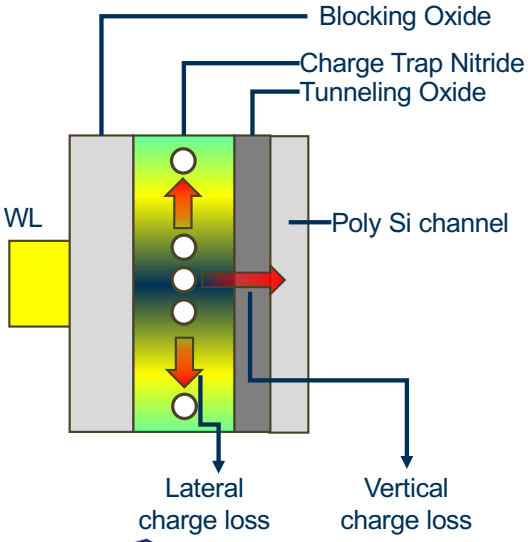
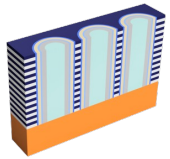
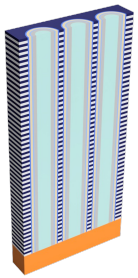
Ferroelectrics for Future NAND Storage Technology

Ferroelectric augmentation can provide enable NAND scaling in future generations

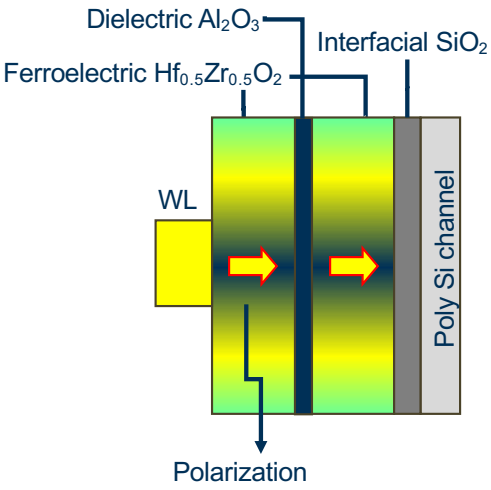


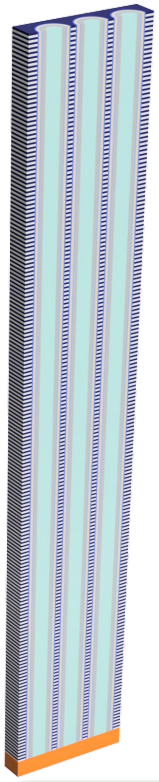


2014:
First 3D NAND
24 Layers, MLC



2025:
300+ Layers, QLC
5 Trillion+ transistors





2030 and
beyond

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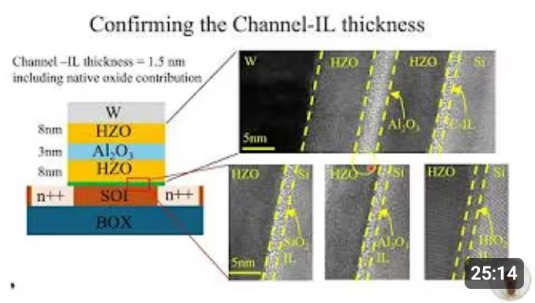

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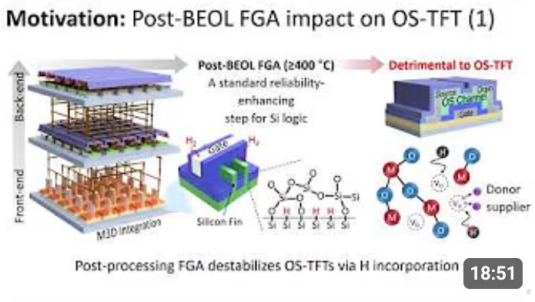

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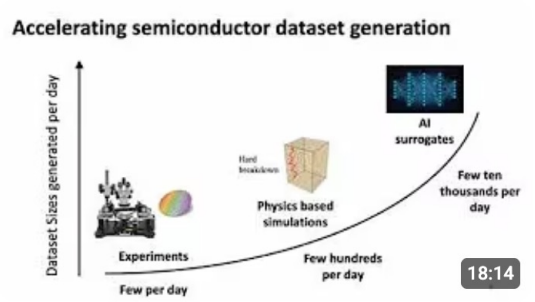

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