

Negative Capacitance FETs: Physics, Materials and Devices

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MRS Spring 2018 Tutorial



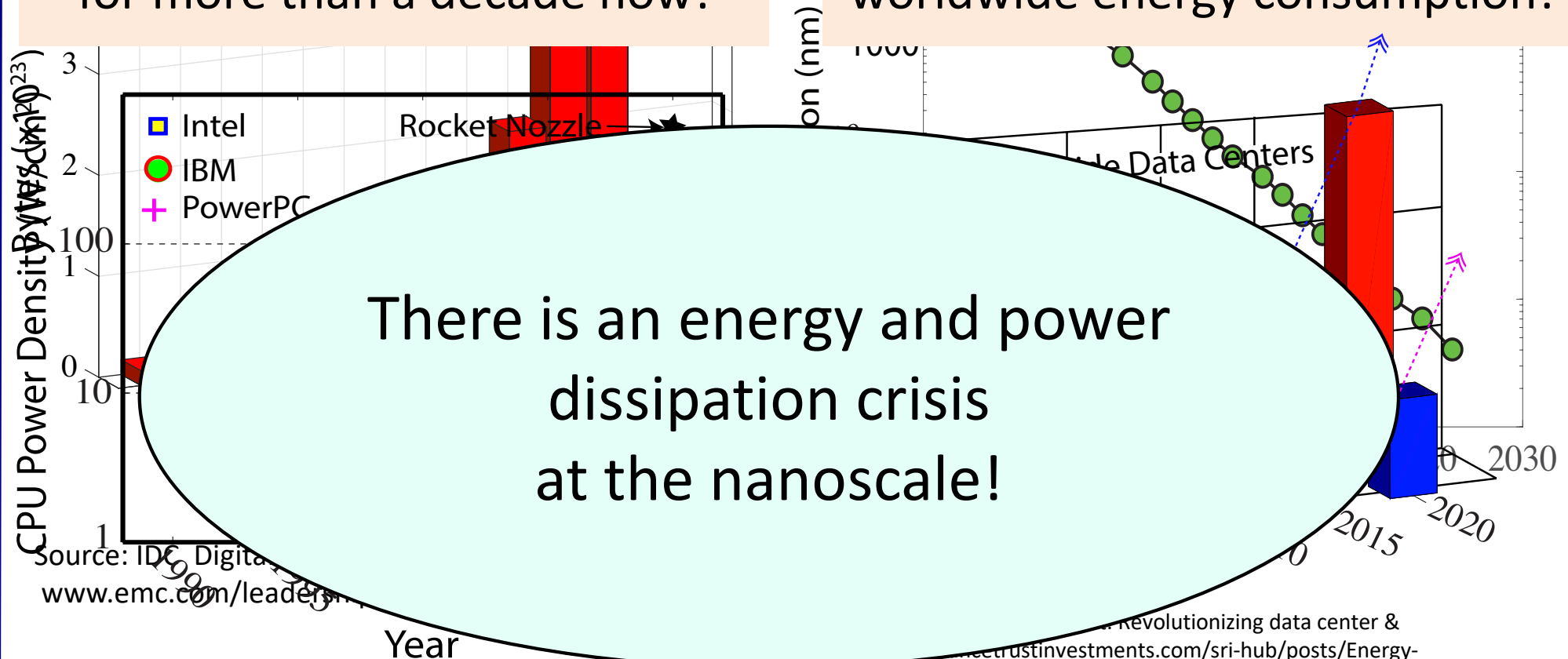
Computing and Global Challenges

Computable data grows 50x every ten year!

Extreme scaling has been the driver!

Clock frequency stuck at 3 GHz for more than a decade now!

Computing constitutes 2-5% of worldwide energy consumption!

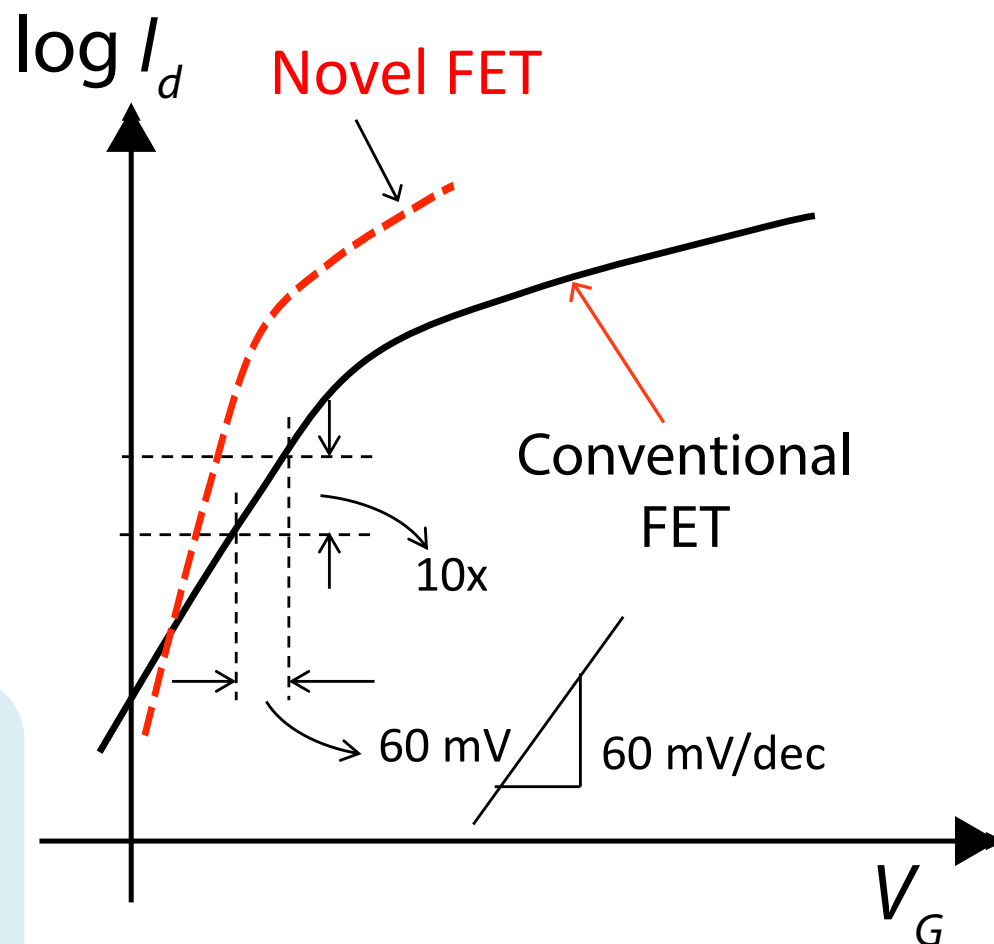
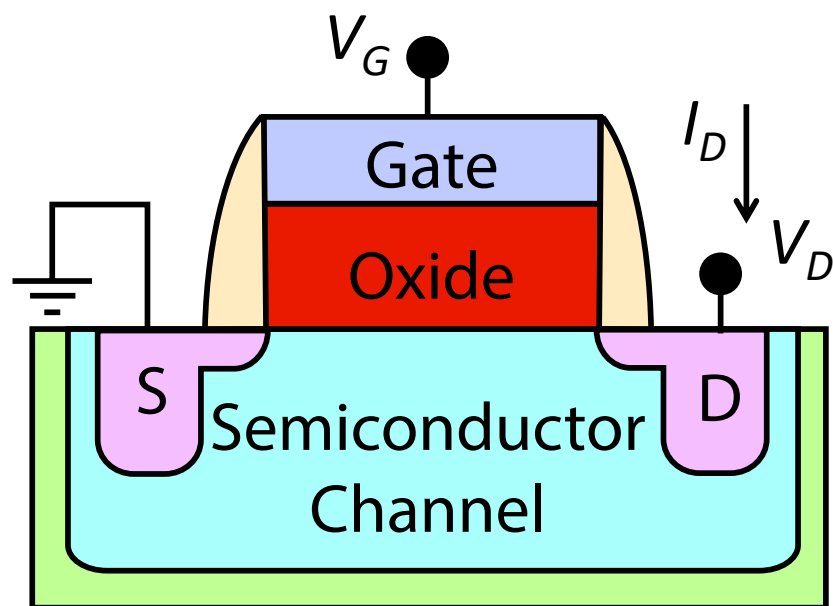


Adapted from: Danowitz et al. Comm. of ACM 55.1 (2012).

efficient-data-centres

revolutionizing data center &
investments.com/sri-hub/posts/Energy-

Energy Challenge in Computing



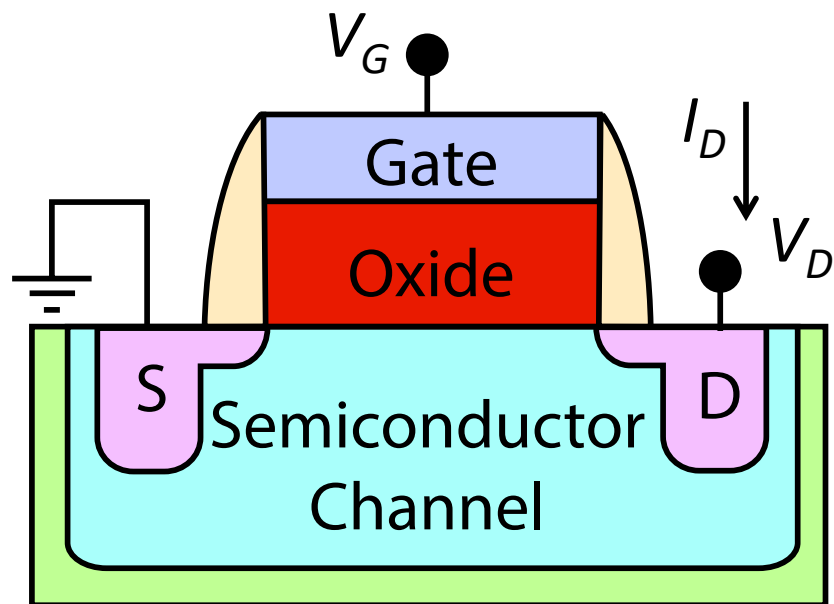
Boltzmann distribution
dictates that

Channel charge, $Q \propto e^{\frac{q\psi_s}{k_B T}}$

Minimum Subthreshold Swing $S_{\min} = \frac{k_B T}{q} \log_e(10) = 60 \text{ mV} / \text{dec}$

We are in search of an Ultra-low Power MOSFET!

The Negative Capacitance Approach



Subthreshold Swing

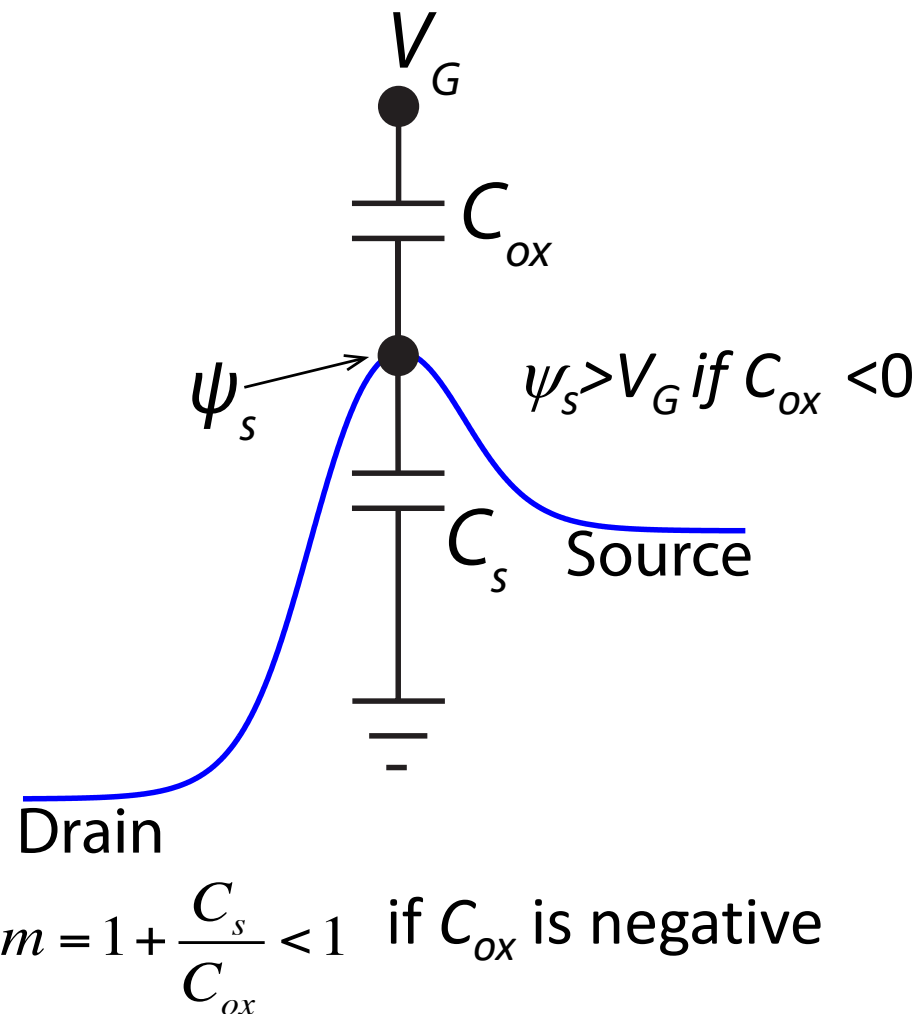
$$S = \frac{\partial V_G}{\partial (\log_{10} I_D)}$$

$$= \underbrace{\frac{\partial V_G}{\partial \psi_s}}_{\equiv m} \frac{\partial \psi_s}{\partial (\log_{10} I_D)}$$

$$= m \times 60 \text{ mV/decade}$$

Body Factor

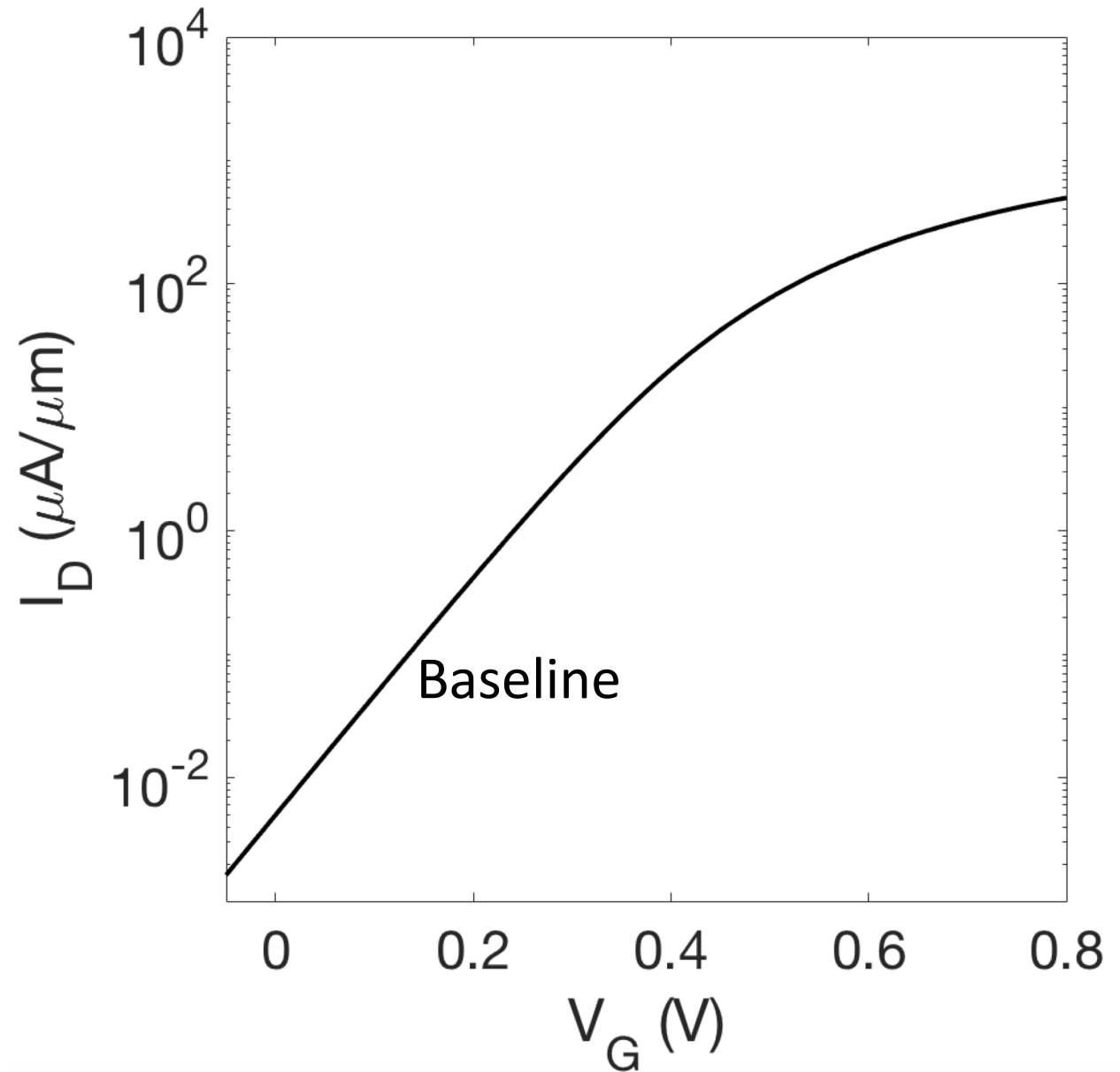
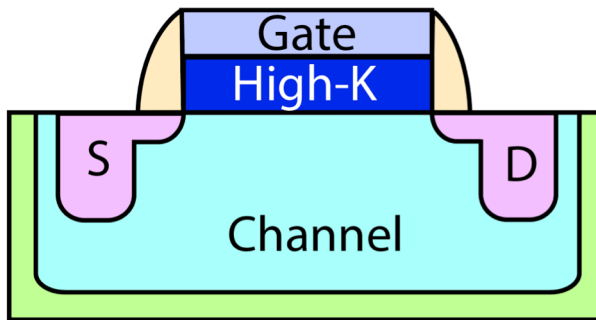
$$m = \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_s}{C_{ox}}$$



Negative capacitance can result
in a $S < 60 \text{ mV/decade}$

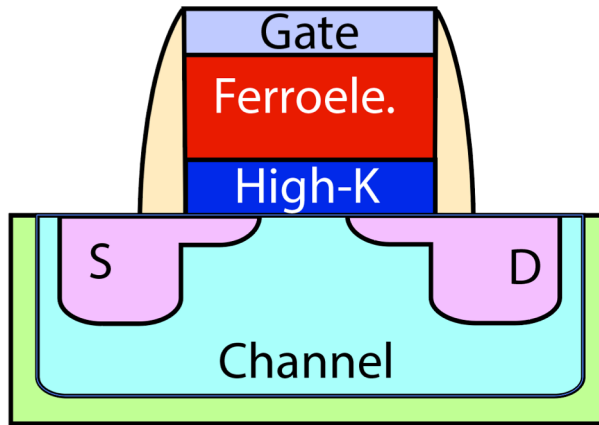
NCFET: What do we expect?

Baseline FET



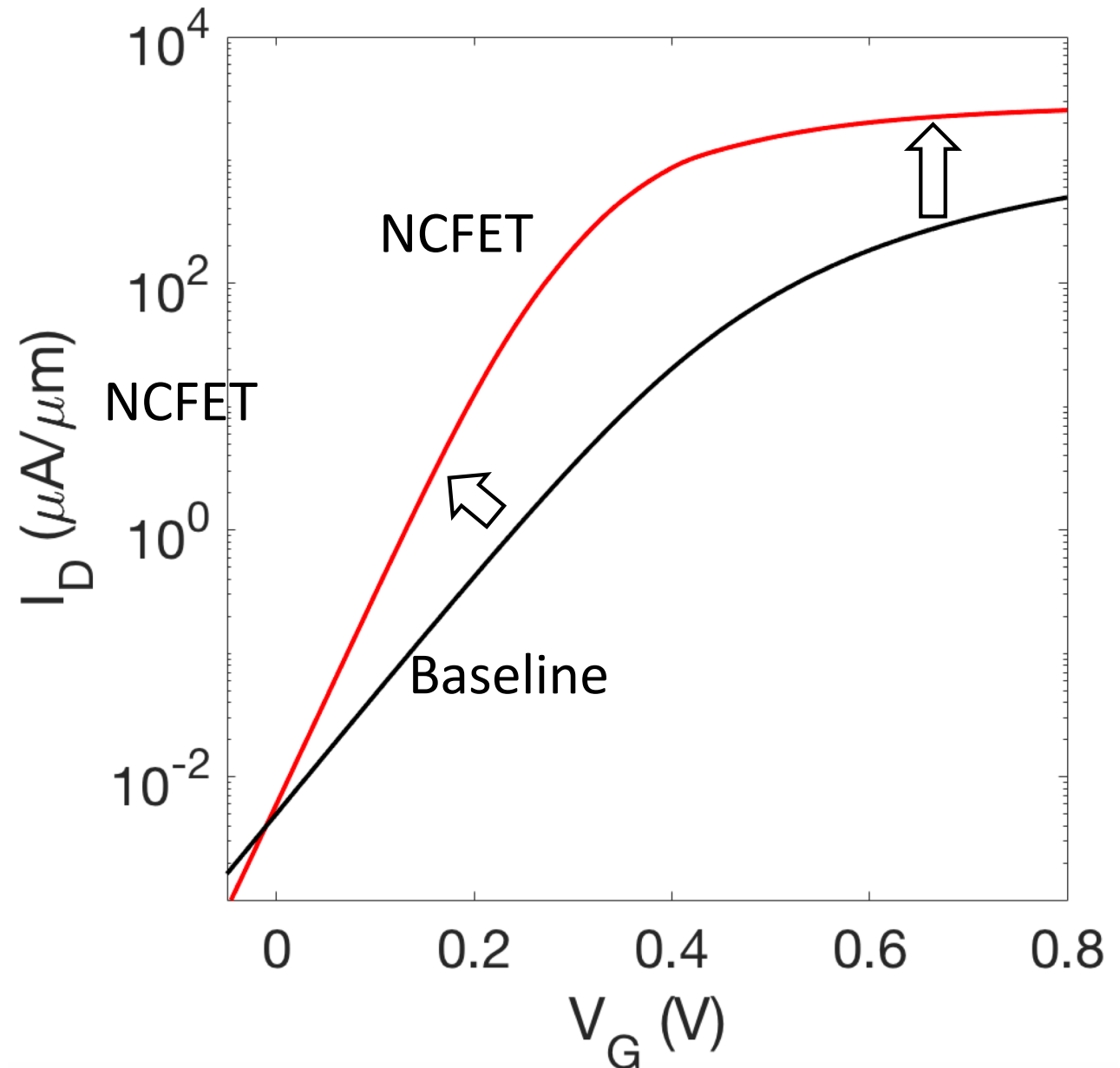
NCFET: What do we expect?

NCFET (Baseline+FE)



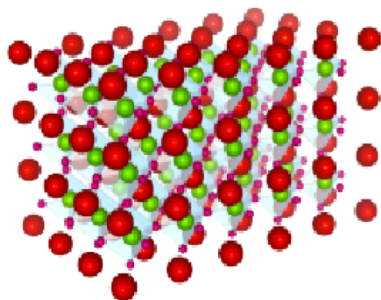
We expect:

1. Improvement of subthreshold swing.
2. Boost in on-current.

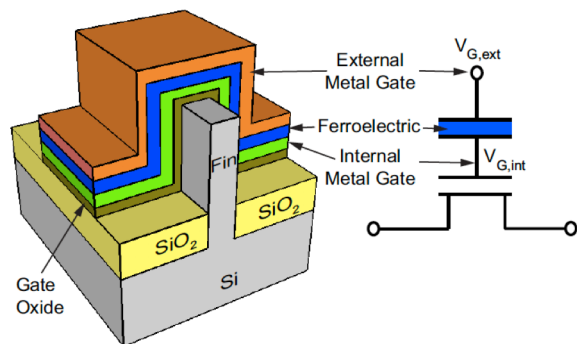


What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors

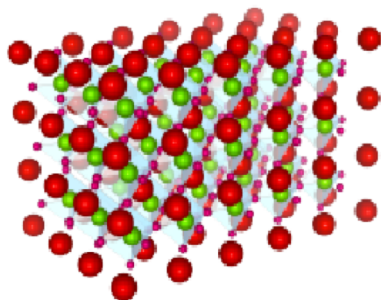


What do we need to know?

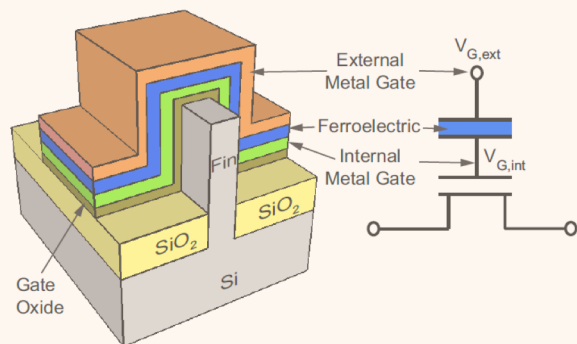


What am I going to do today?

Physics of Negative Capacitance in Materials



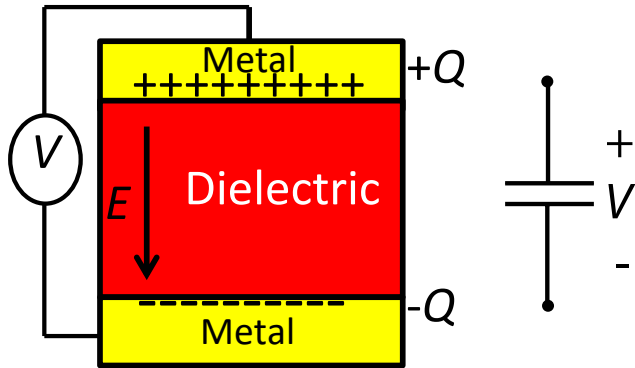
Physics of Negative Capacitance Transistors



What do we need to know?



Capacitance: Positive and Negative

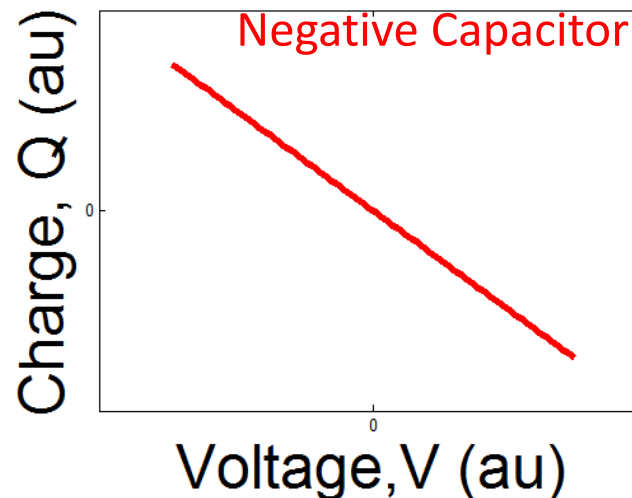
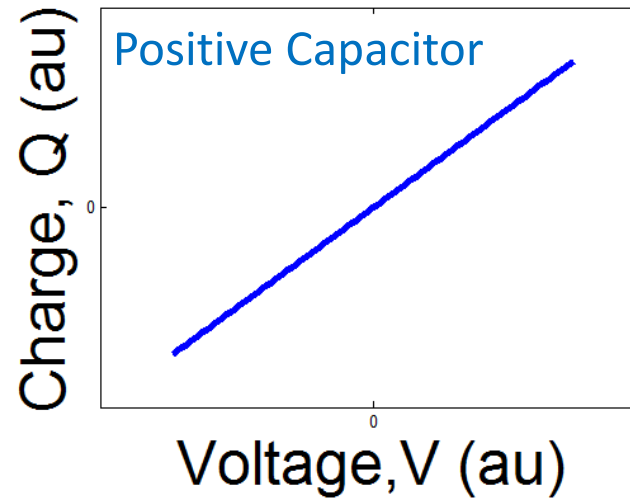


Capacitance $C = \frac{dQ}{dV}$

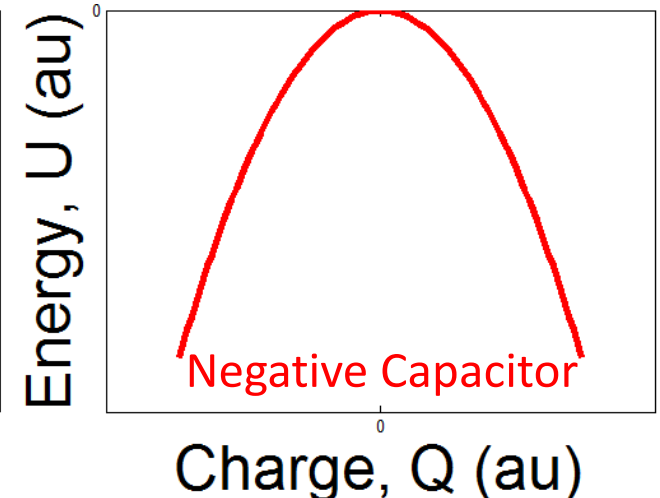
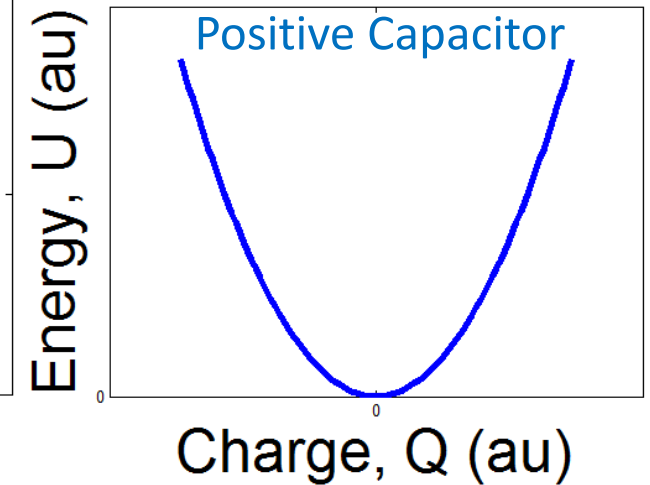
Stored Energy $U = \frac{Q^2}{2C}$

$$C = \left[\frac{d^2 U}{dQ^2} \right]^{-1}$$

Q-V Characteristics



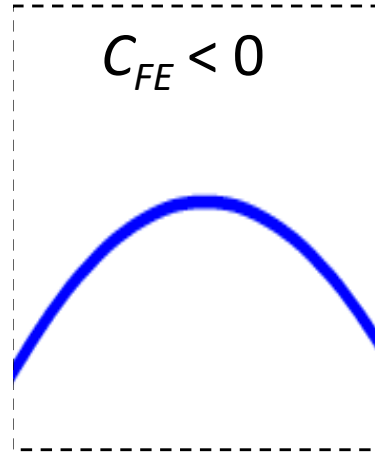
Q-U Characteristics
(Energy Landscape)



C is inverse of radius of curvature of energy landscape

How to get Negative Capacitance Material

U ↑



Q →

Landau Theory of Ferroelectrics

Free energy of a ferroelectric

$$U = \alpha Q^2 + \beta Q^4 + \gamma Q^6; \alpha < 0$$

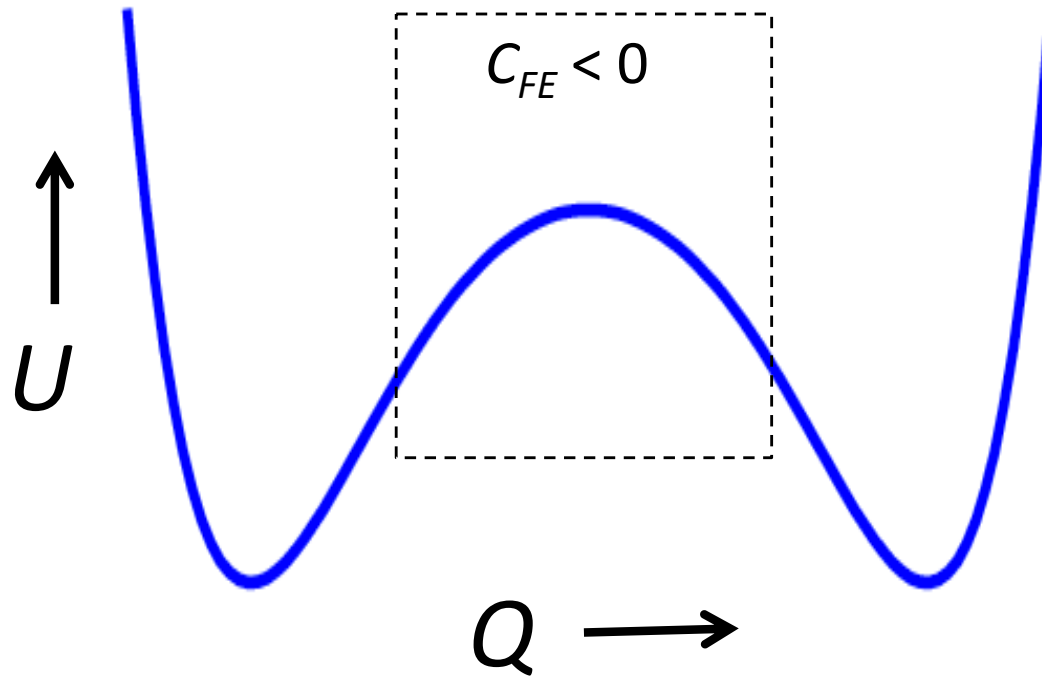
α, β, γ = Anisotropy Constants

Q = Charge

According to the Landau theory of ferroelectric, ferroelectric oxides could give an effective negative capacitance

Landau & Khalatnikov. Dokl. Akad. Nauk 96, 85
469472 (1954).

How to get Negative Capacitance Material



Landau Theory of Ferroelectrics

Free energy of a ferroelectric

$$U = \alpha Q^2 + \beta Q^4 + \gamma Q^6; \alpha < 0$$

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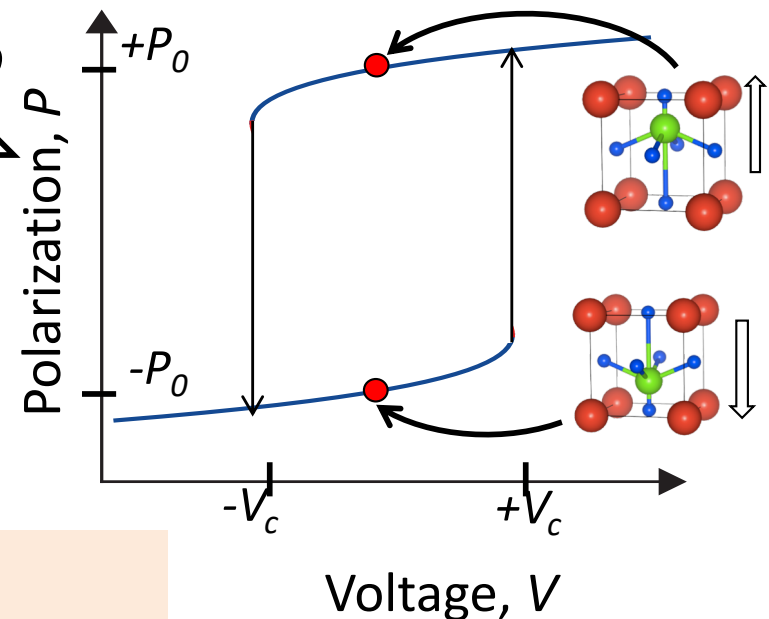
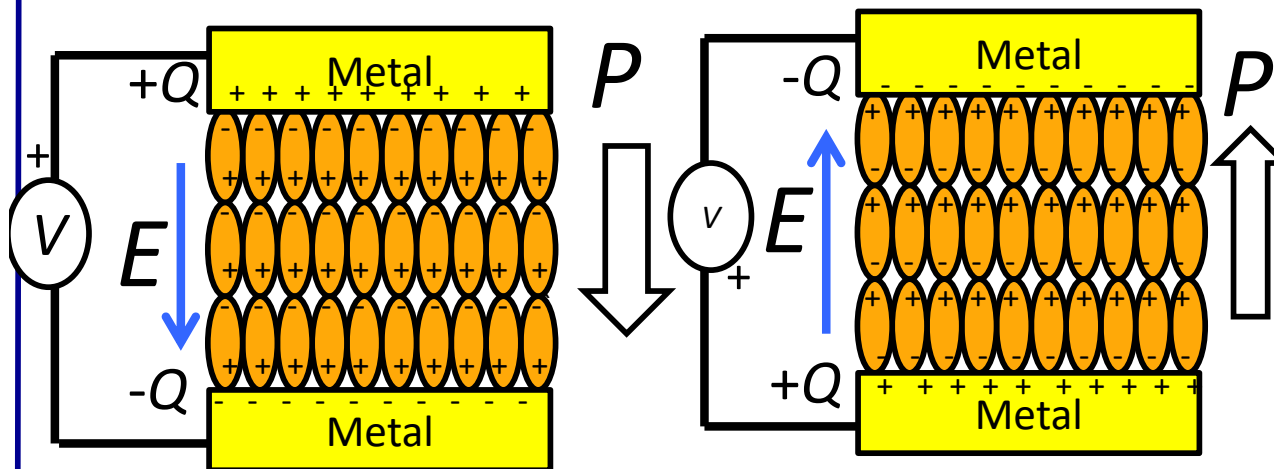
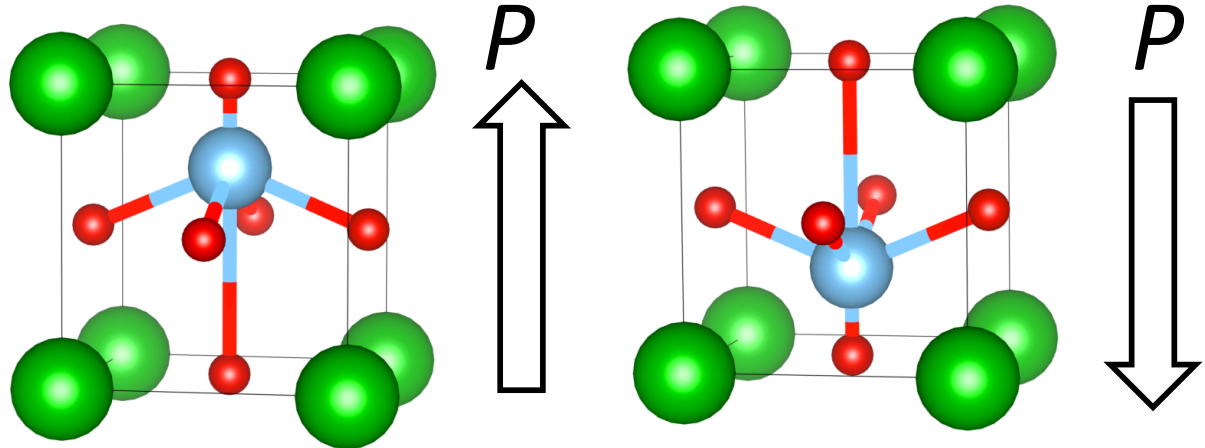
Q = Charge

According to the Landau theory of ferroelectric, ferroelectric oxides could give an effective negative capacitance

Landau & Khalatnikov. Dokl. Akad. Nauk 96, 85
469472 (1954).

Ferroelectric Oxides: Perovskites

Classical Ferroelectric
 PbTiO_3 ($\text{Pb}^{2+}\text{Ti}^{4+}\text{O}_3^{6-}$)



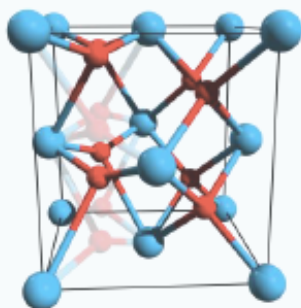
A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercivity voltage .

New CMOS Compatible Ferroelectrics

HfO₂ and its doped variants can become ferroelectric under certain growth and/or processing condition

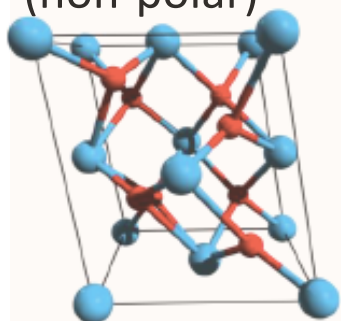
Orthorhombic (Pbc2₁)
(polar)

Ferroelectric

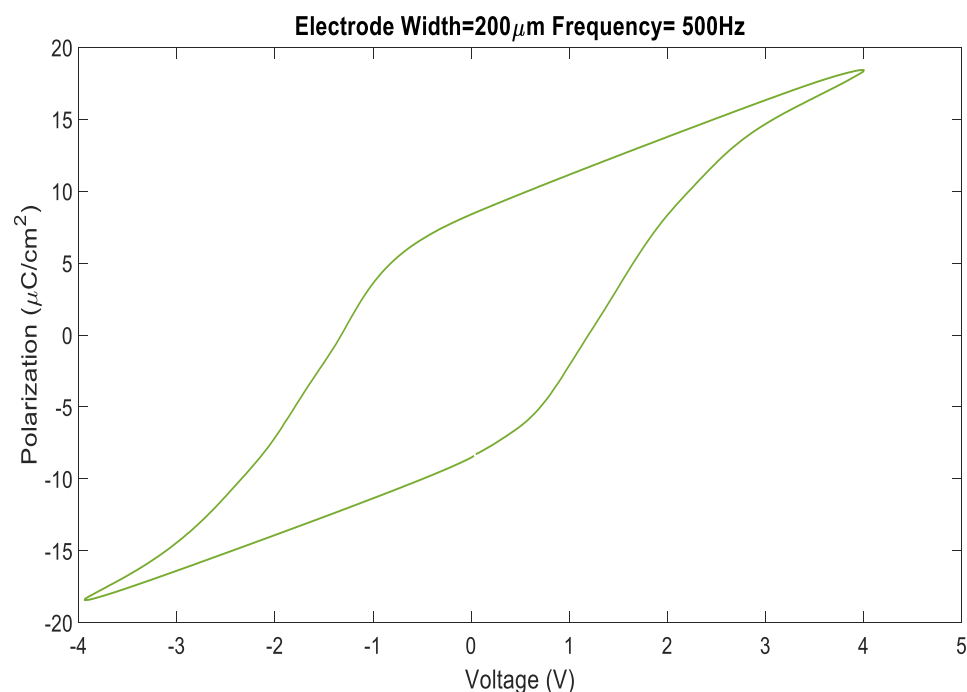
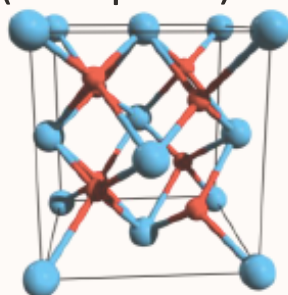


Non-Ferroelectric

Monoclinic
(non-polar)

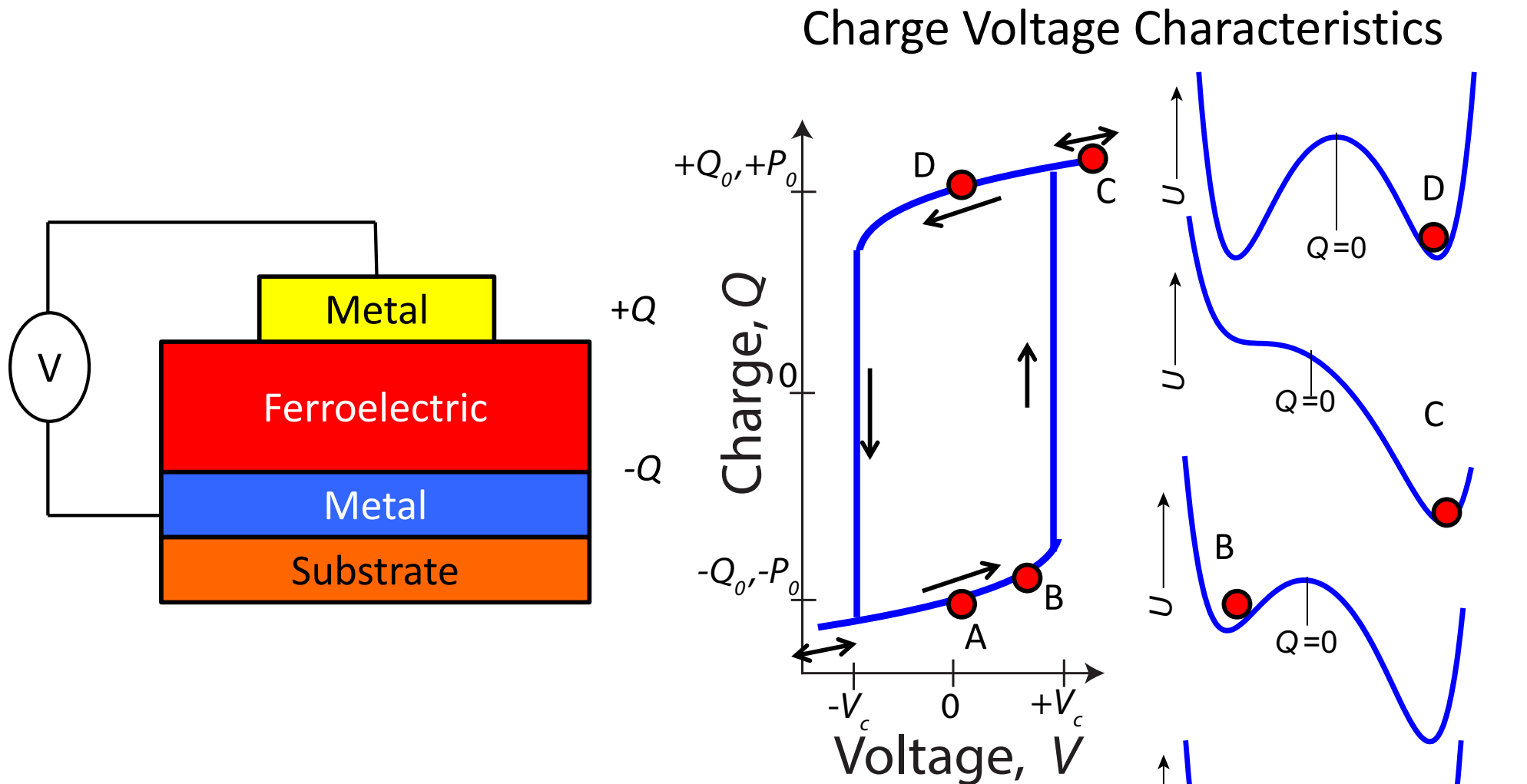


Tetragonal
(non-polar)



Boscke *et.al.*, Appl. Phys. Lett., **99**, 102903 (2011)
Mikolajick *et.al.*, Adv. Sci. Tech., **95**, 136 (2014)

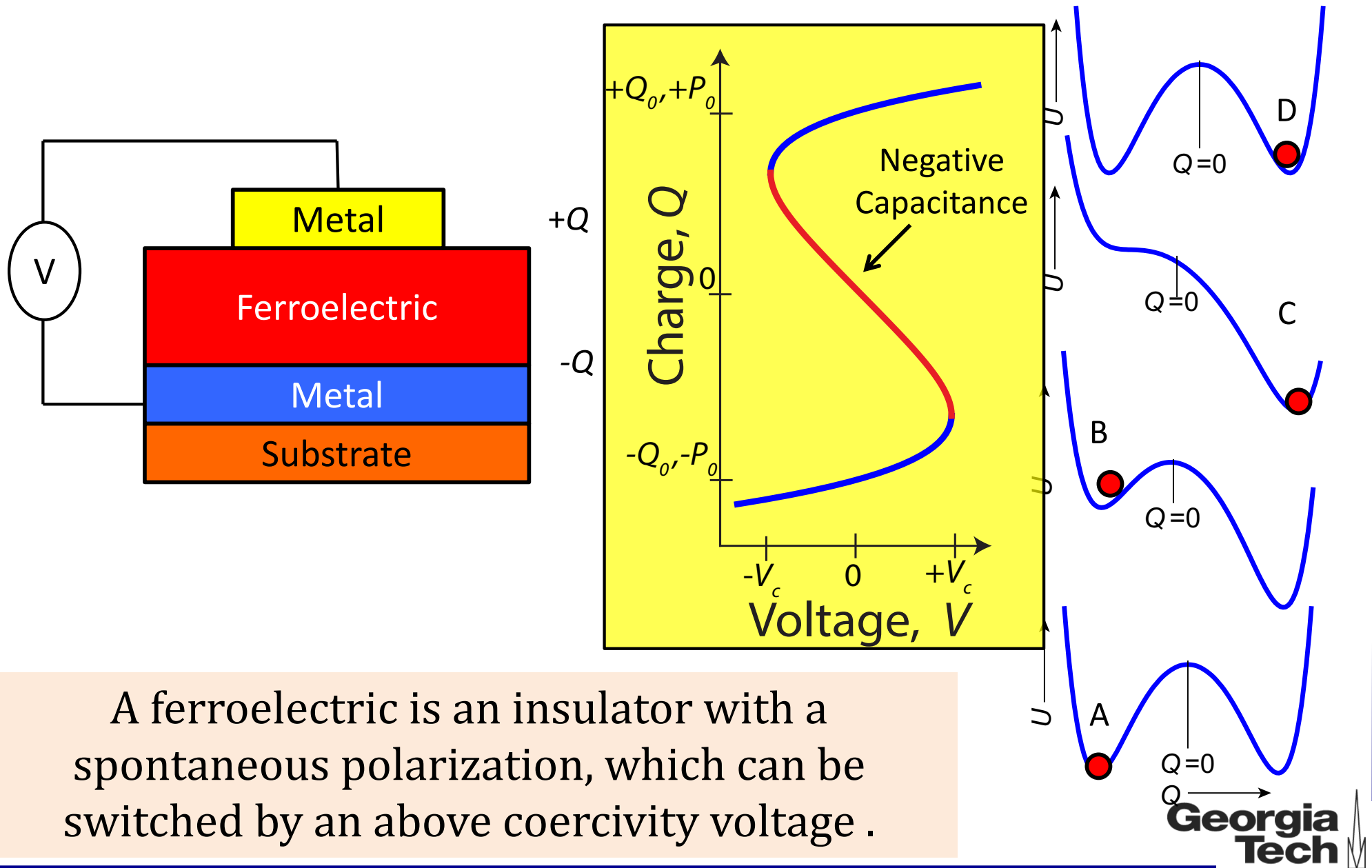
Ferroelectric Oxides



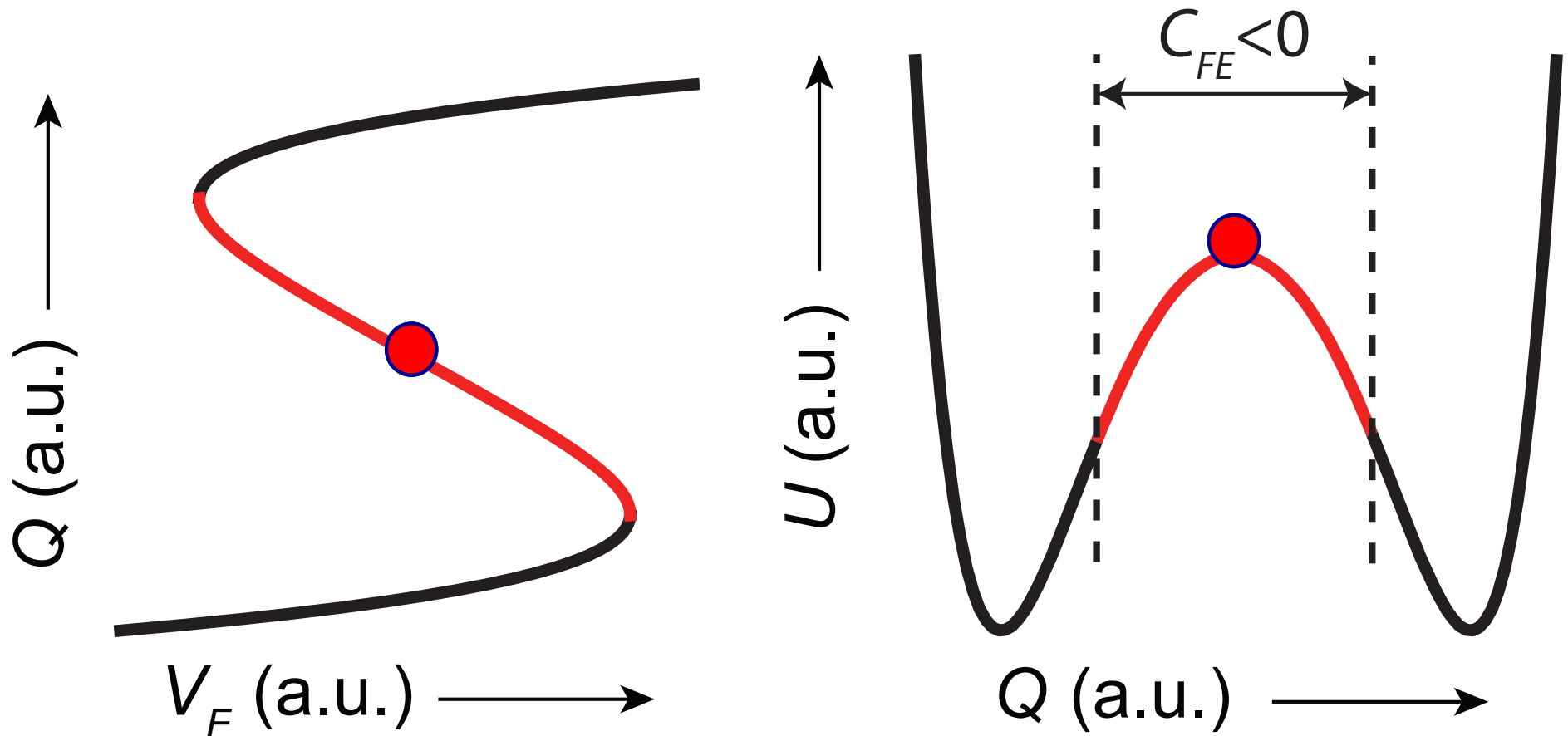
A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercivity voltage.

Ferroelectric Oxides

Charge Voltage Characteristics

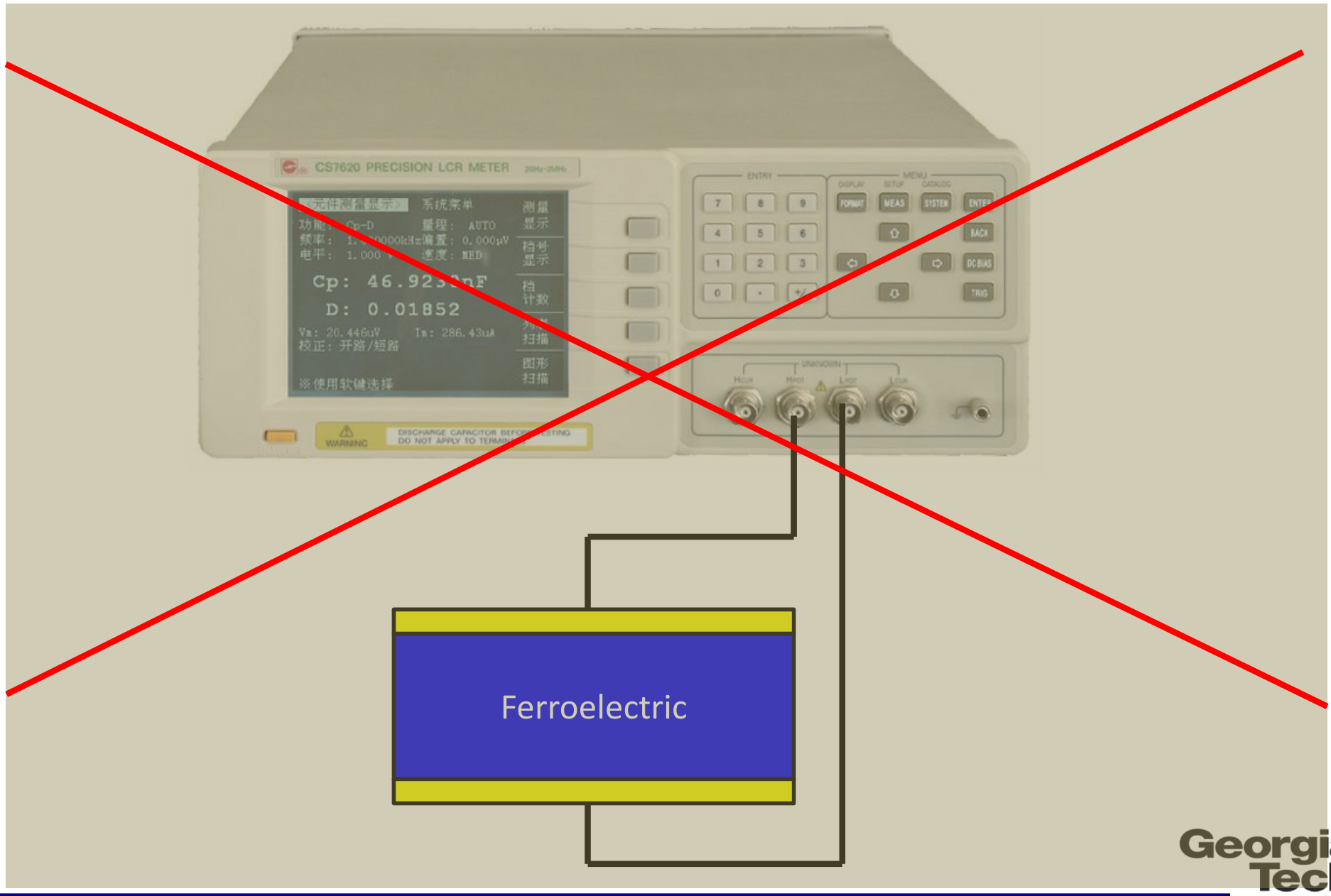


Why is it difficult to measure?

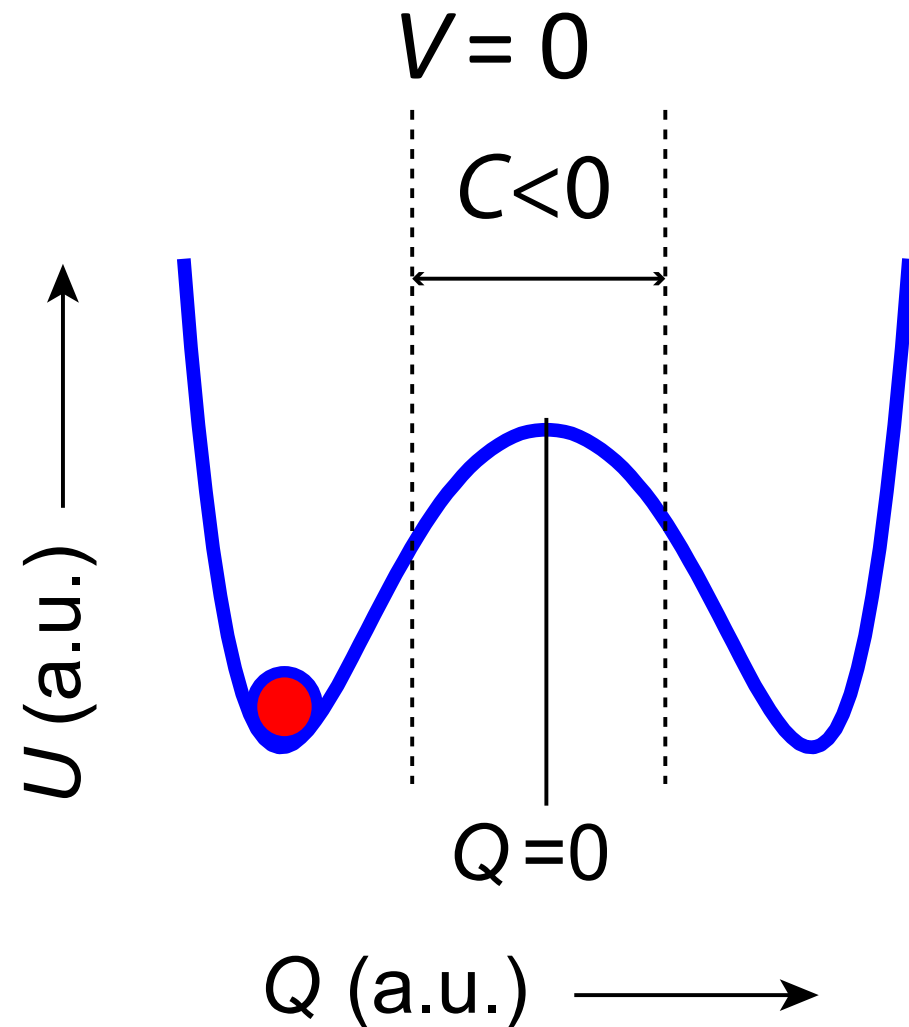
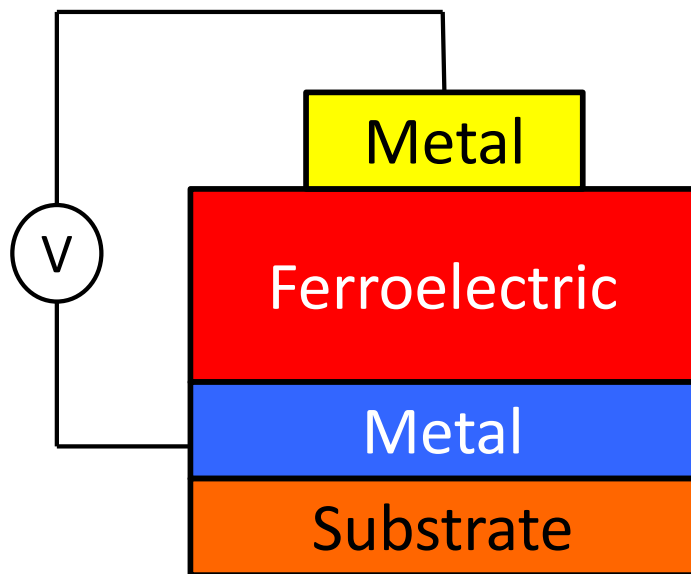


Ferroelectric Negative Capacitance is unstable and cannot be accessed in a time independent equilibrium measurement.

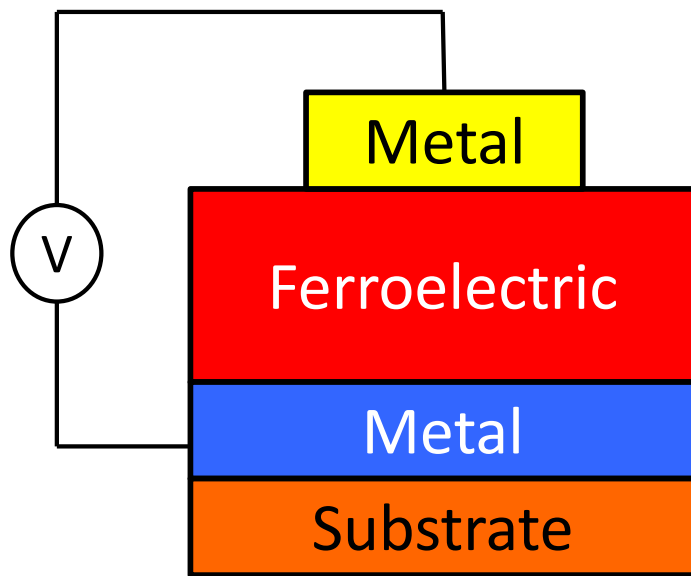
Why is it difficult to measure?



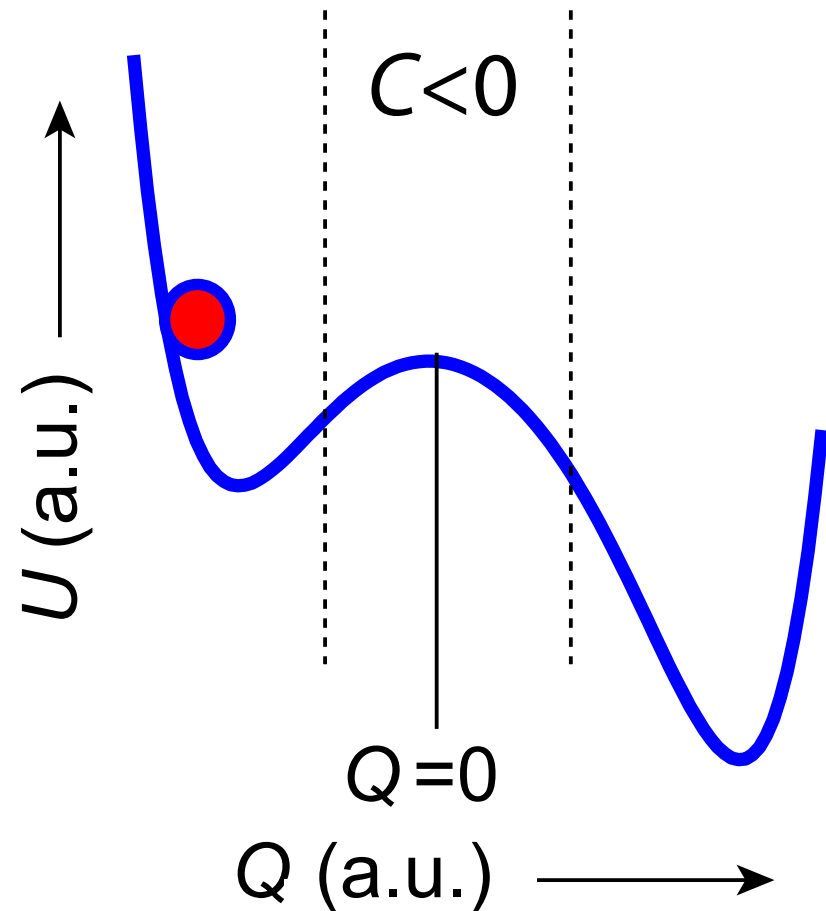
Direct Measurement of Negative Capacitance



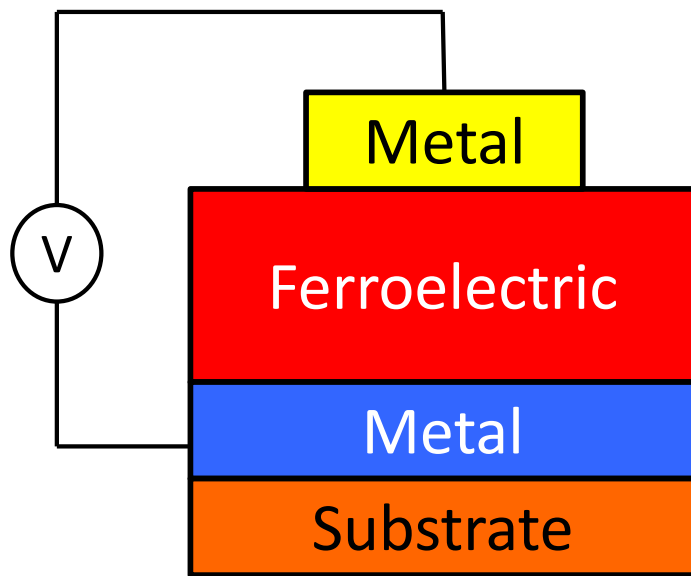
Direct Measurement of Negative Capacitance



$V < \text{Coercive Voltage}$

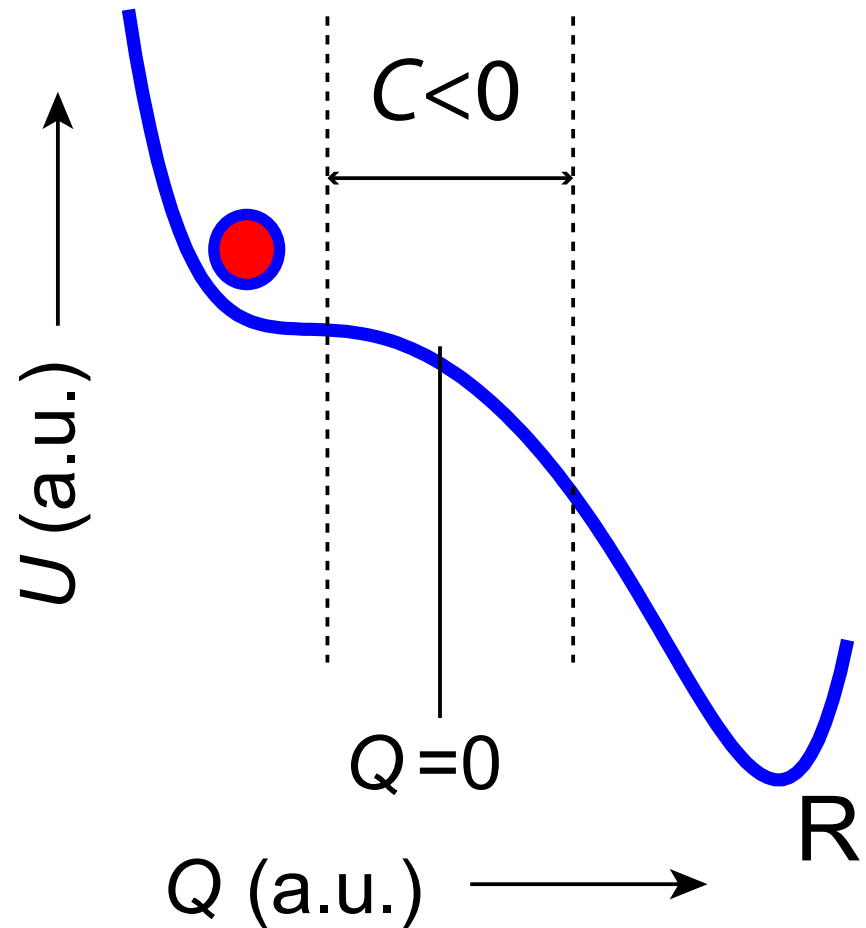


Direct Measurement of Negative Capacitance

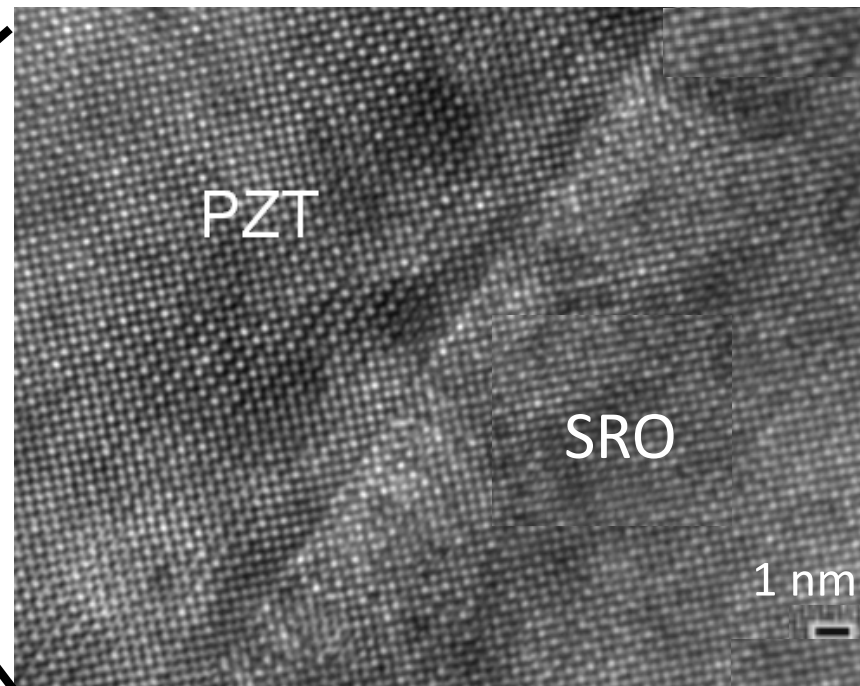
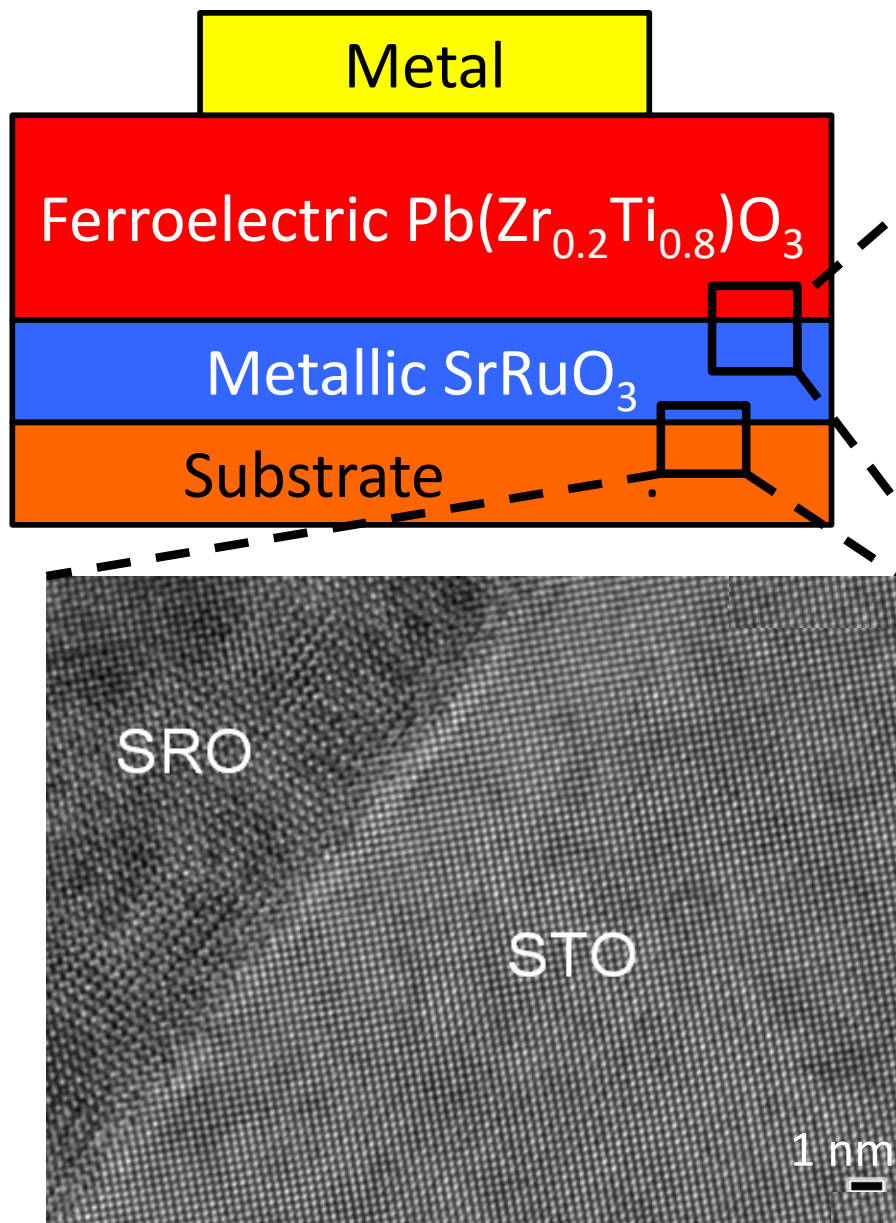


A ferroelectric capacitor goes through the unstable negative capacitance states during switching.

$V > \text{Coercive Voltage}$



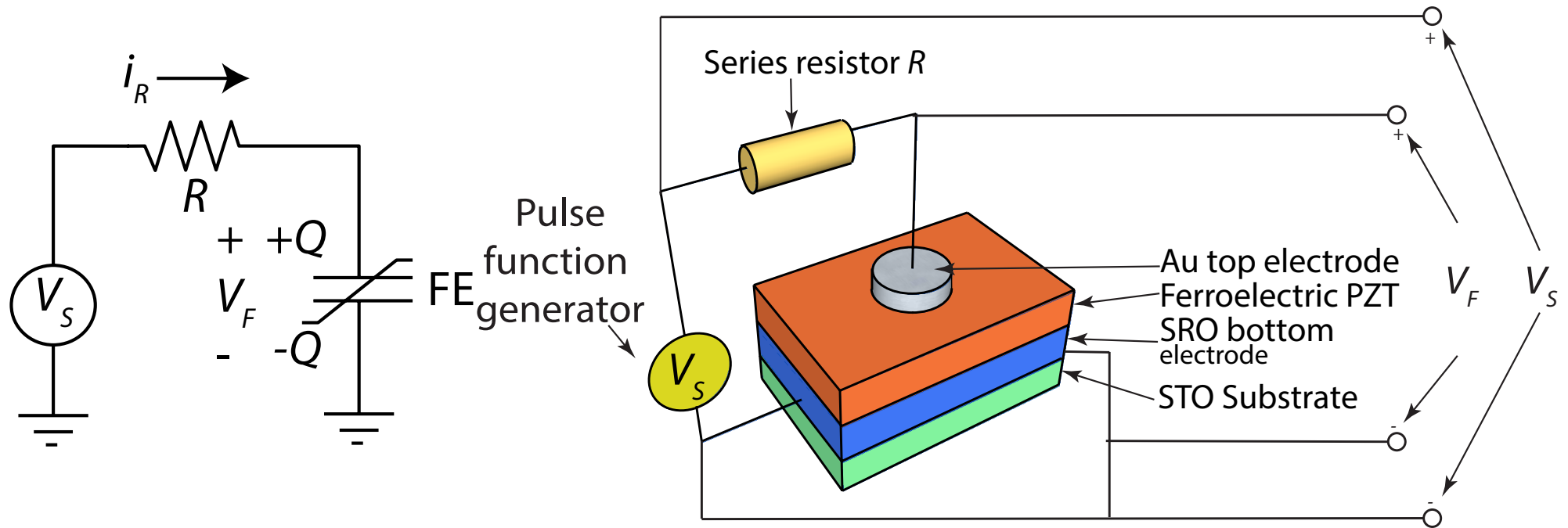
Ferroelectric $\text{Pb}(\text{Zr}_{0.2}\text{Ti}_{0.8})\text{O}_3$



Courtesy: Pan group, U. Mich.

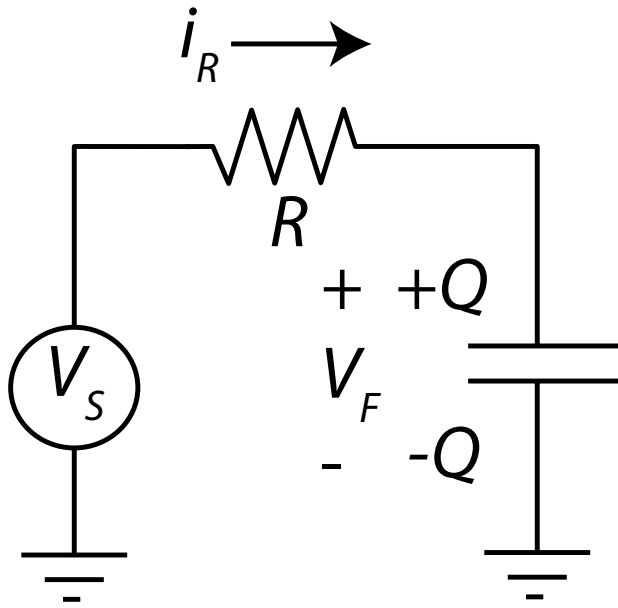
Excellent epitaxial quality!

Direct Measurement of Negative Capacitance



A ferroelectric capacitor connected in series with an external resistor.

What happens in an R - C Series circuit?

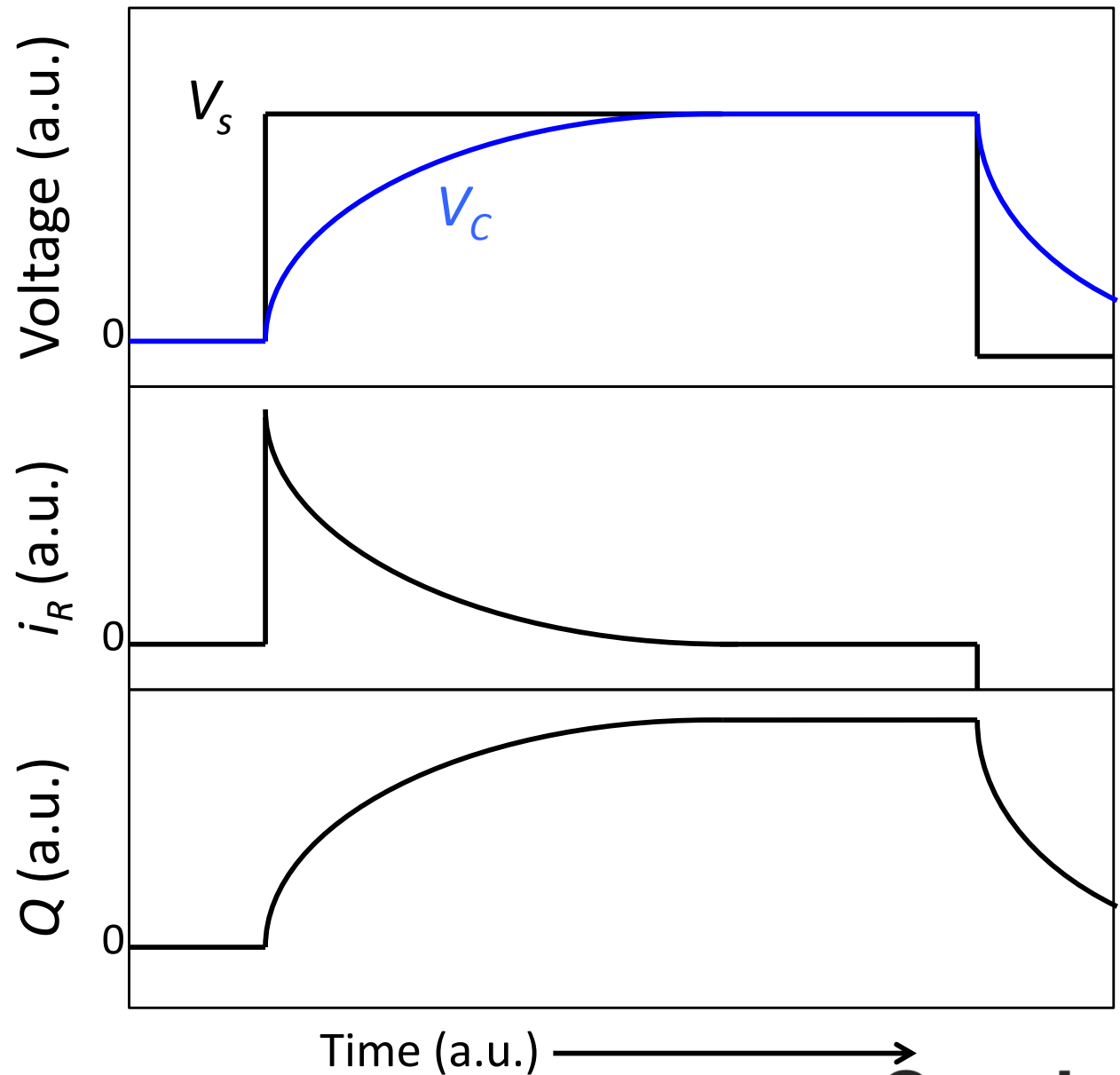


Voltage: $V_C = V_S(1 - e^{-t/RC})$

Current: $i_R = V_S e^{-t/RC} / R$

Charge: $Q = CV_S(1 - e^{-t/RC})$

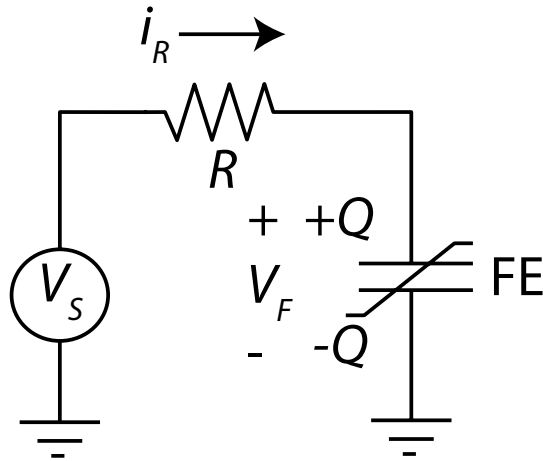
At any time t ,
 $dQ/dV_C = C > 0$.



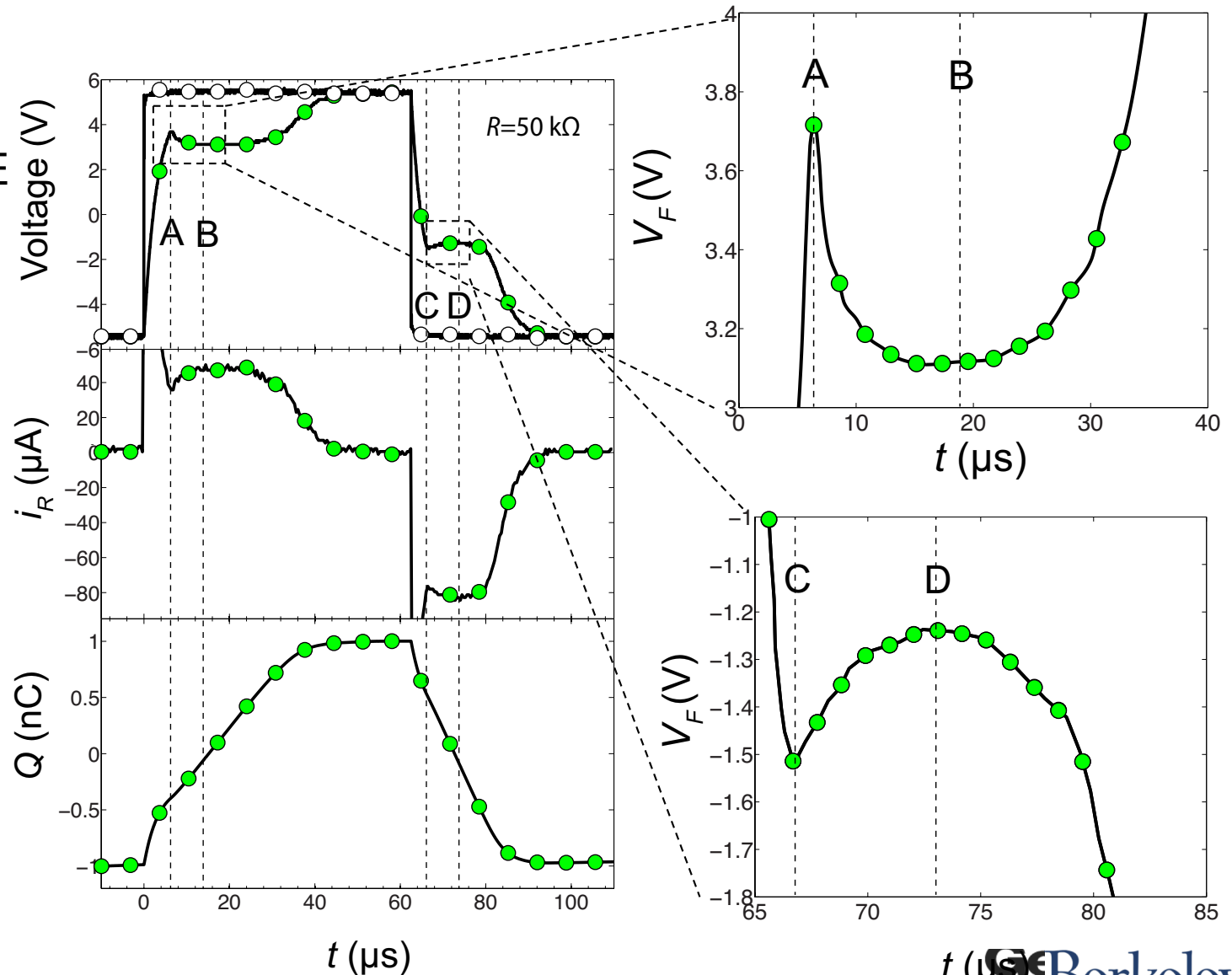
Direct Measurement of Negative Capacitance

60 nm $\text{Pb}(\text{Zr}_{0.2}\text{Ti}_{0.8})\text{O}_3$ (Coercive voltage ≈ 2.5 V)

$V_s: -5.4 \text{ V} \rightarrow +5.4 \text{ V} \rightarrow -5.4 \text{ V}$



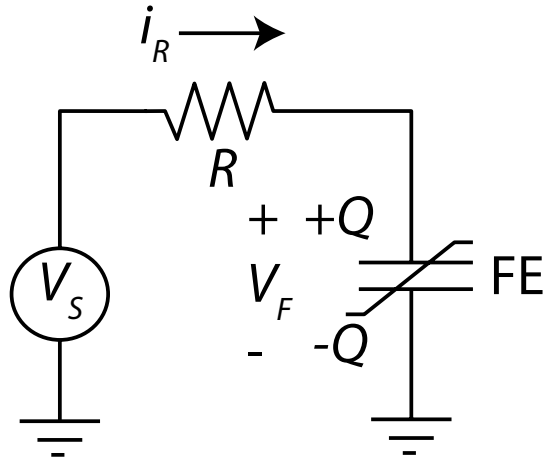
During AB & CD,
 dQ & dV_F has
opposite signs
indicating
 $dQ/dV_F < 0$.



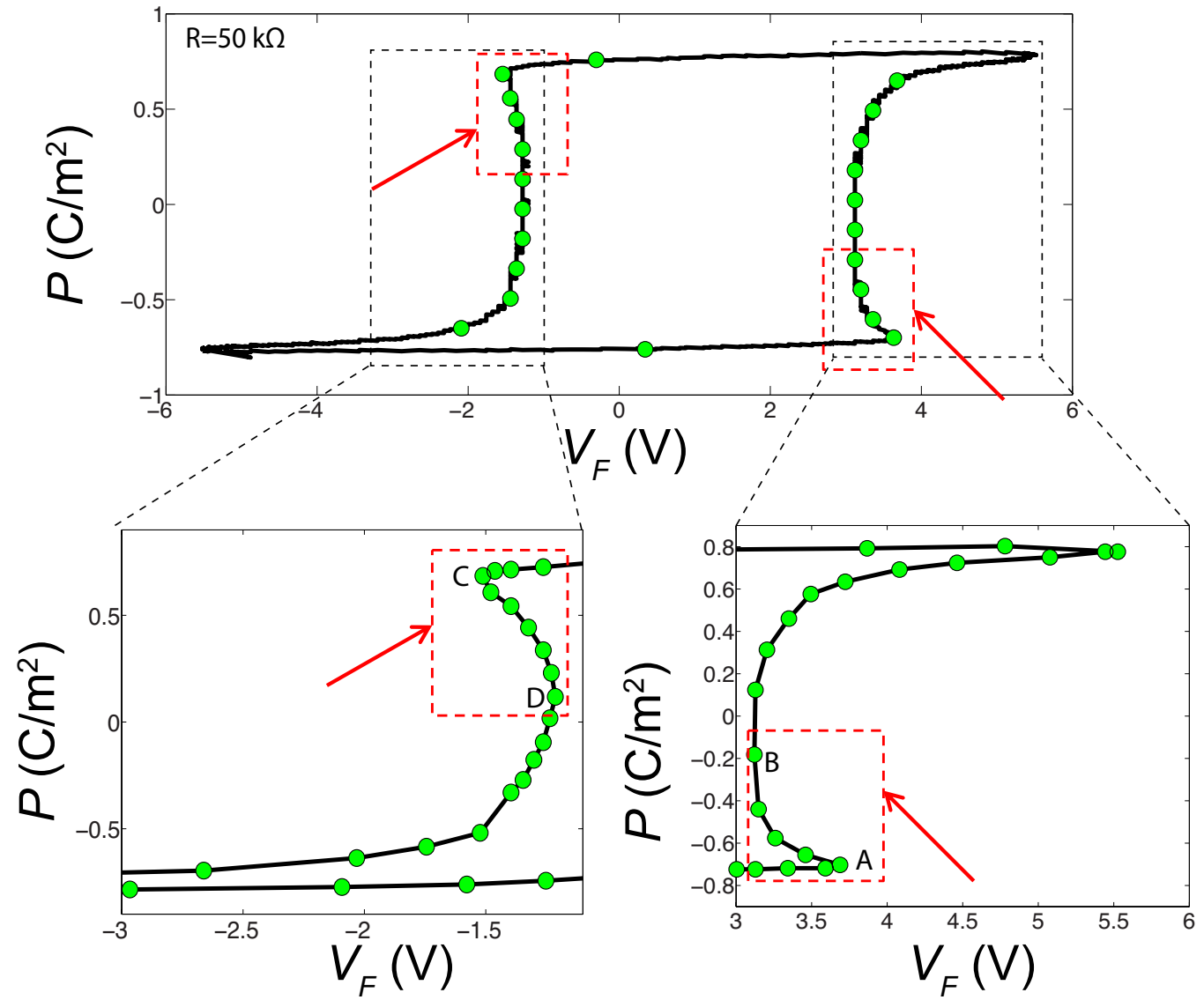
Khan et al. Nature Mater. 14,
182 (2015)

Direct Measurement of Negative Capacitance

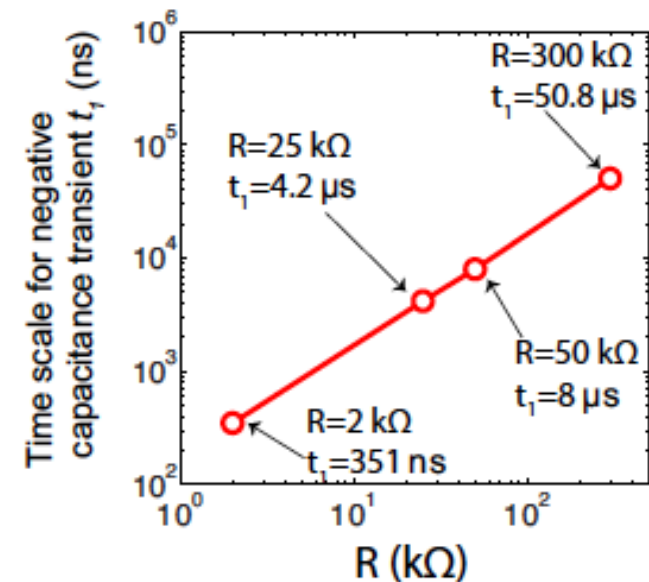
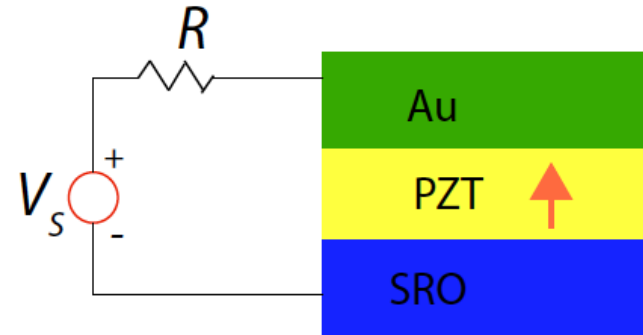
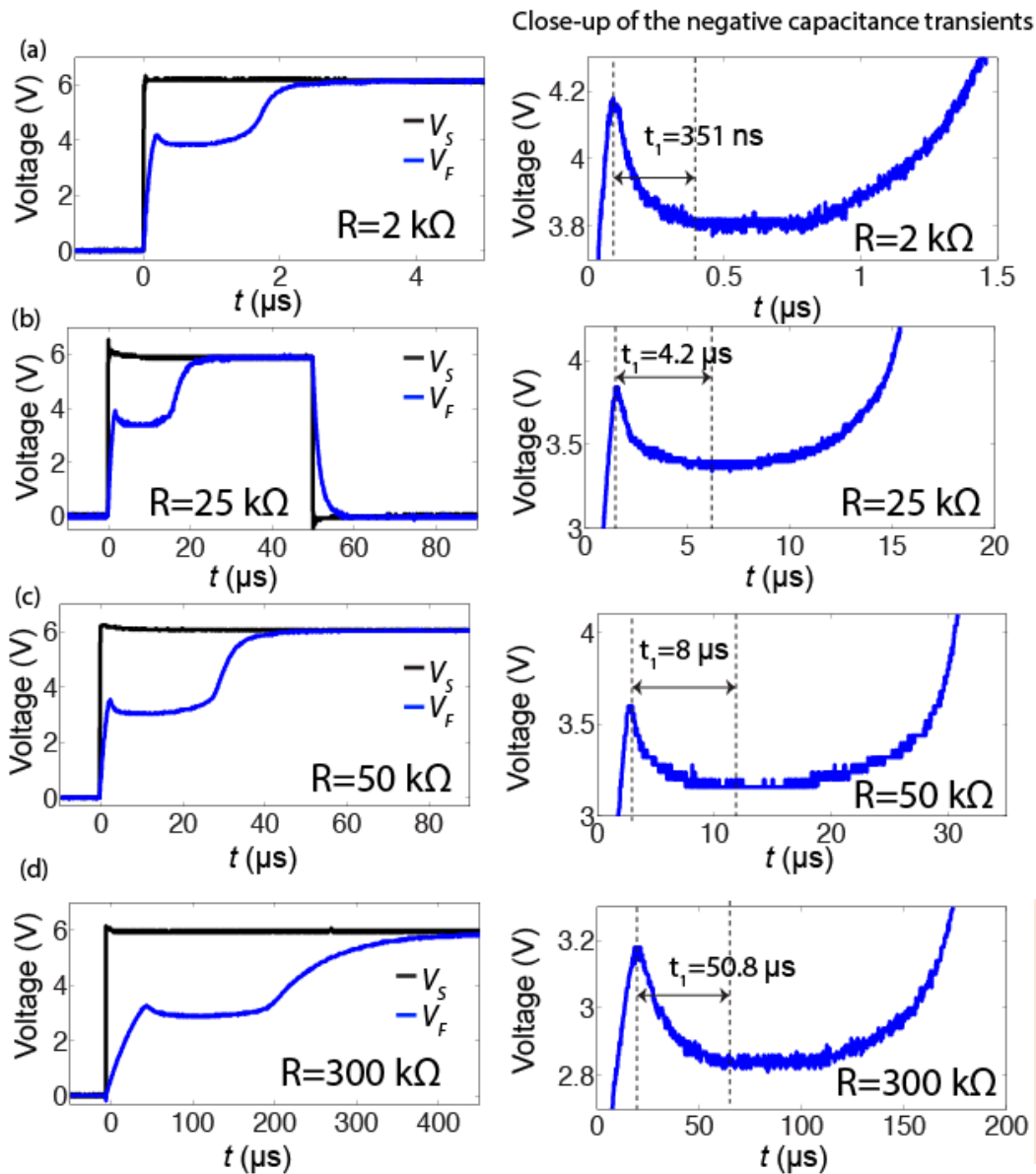
60 nm $\text{Pb}(\text{Zr}_{0.2}\text{Ti}_{0.8})\text{O}_3$ (Coercive voltage ~ 2.5 V)



A negative dQ/dV_F directly observed in an isolated ferroelectric.



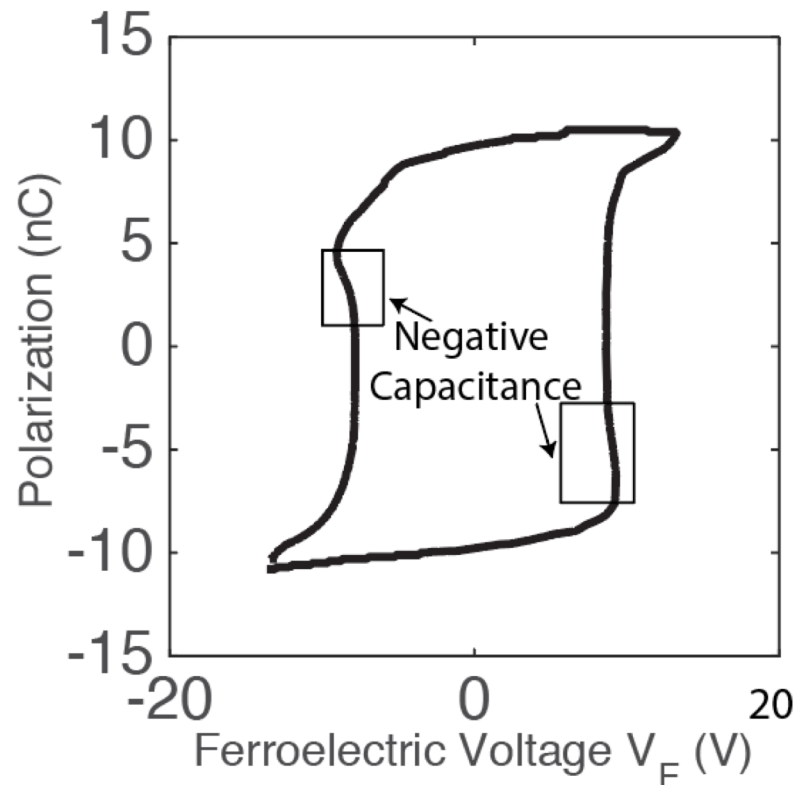
Time Scale of Negative Capacitance



The intrinsic time scale of Negative Capacitance transient could be very small.

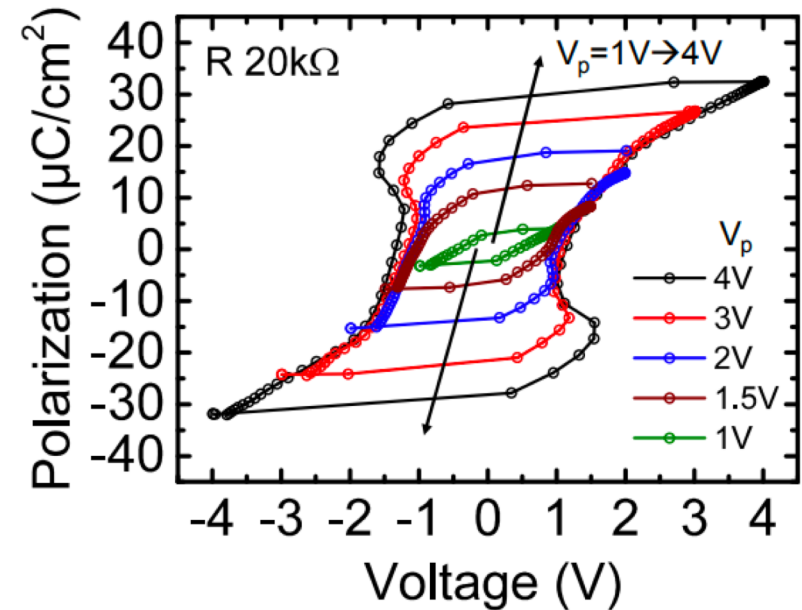
Negative Cap. in Doped HfO_2 Ferroelectrics

Ferroelectric Gd-doped HfO_2 (27 nm)



Hoffmann et al. Direct Observation of Negative Capacitance in Polycrystalline Ferroelectric HfO_2 . Advanced Functional Materials 2016.

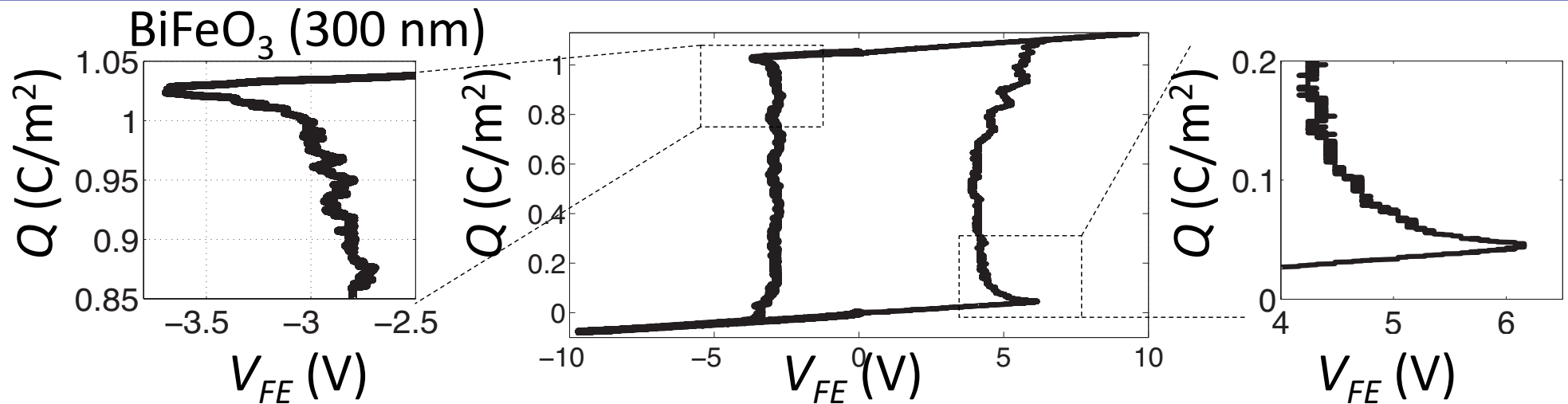
Ferroelectric HfZrO_2 (10 nm)



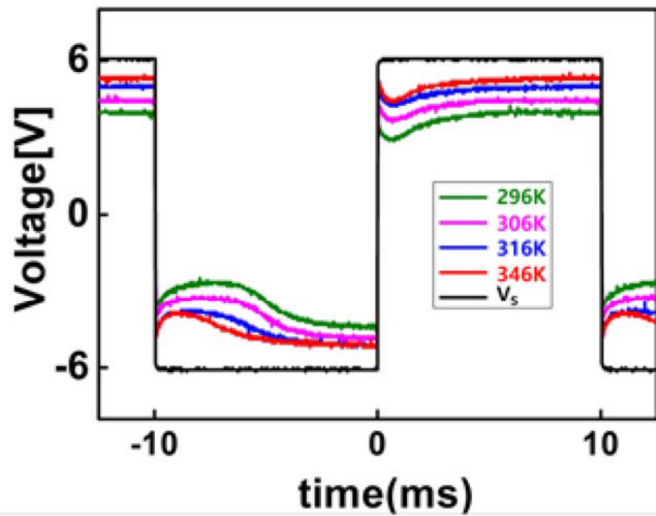
Kobayashi et al. Experimental study on polarization-limited operation speed of negative capacitance FET with ferroelectric HfO_2 . IEDM 2016

Negative capacitance is a general phenomenon in ferroelectrics!

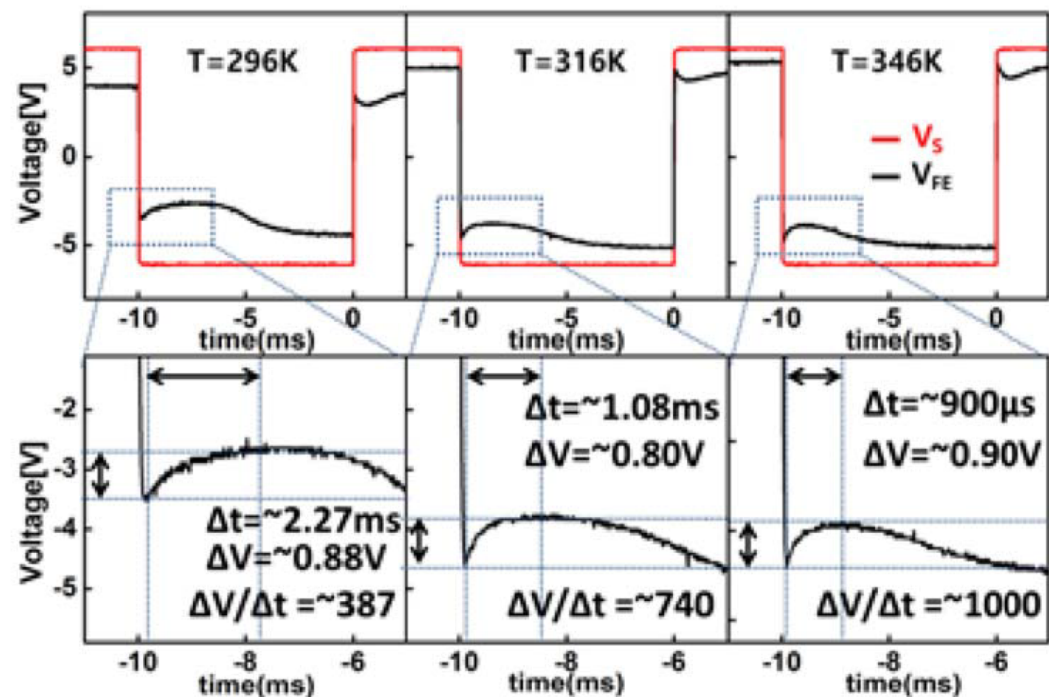
Negative Cap. in Other Ferroelectrics



Organic Ferroelectric
PVDF_{0.75}-TrFE_{0.25} (20 nm)



Ku et al. JEDS 5, 232 (2017)



Negative Capacitance in 1956!

Landauer et al. Polarization reversal in the Barium Titanate hysteresis loops.

J. Appl. Phys. 27, 752 (1956)

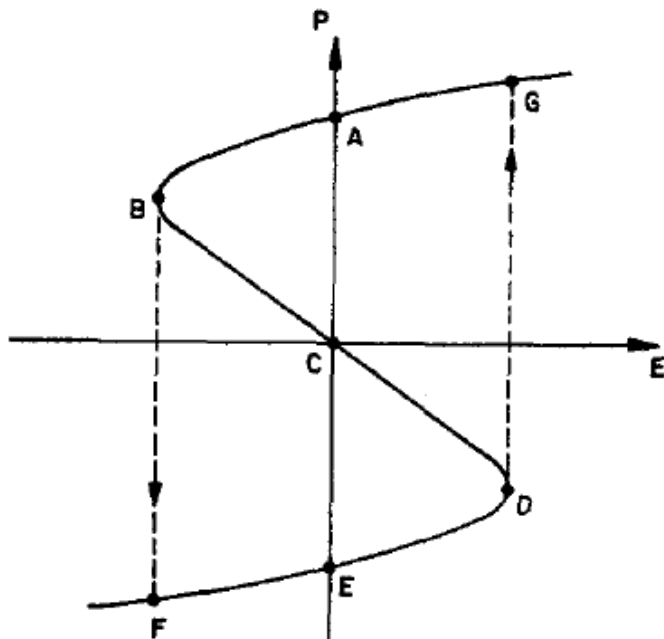


FIG. 1. Plot of polarization against field, at room temperature, as given by Devonshire's theory. P = polarization, E = field. Direction of field and polarization are taken to be the same, and parallel to the "c" axis of a single domain crystal. The solid line $GAB CDEF$ gives the theoretical relationship.

Merz. Switching time in BaTiO₃ and its dependence on its crystal thickness. **J. Appl. Phys.** 27, 938 (1956)

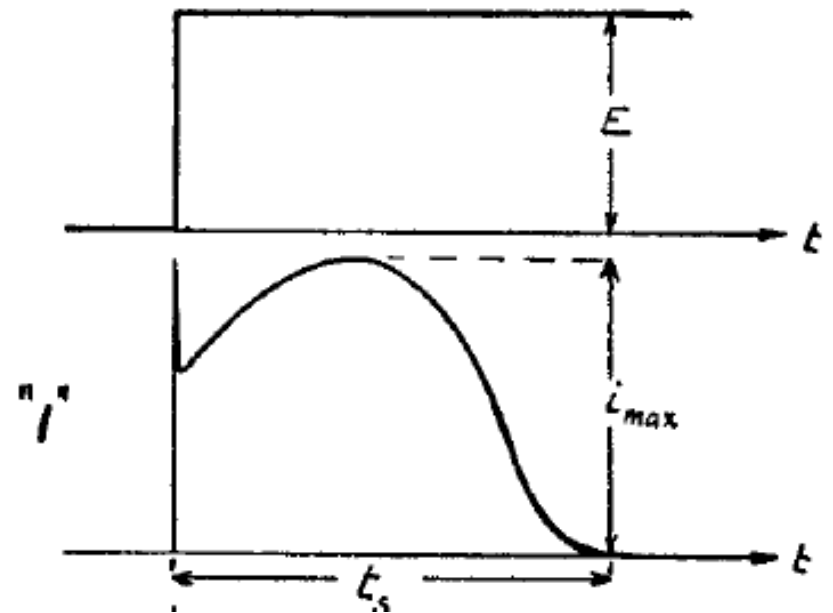
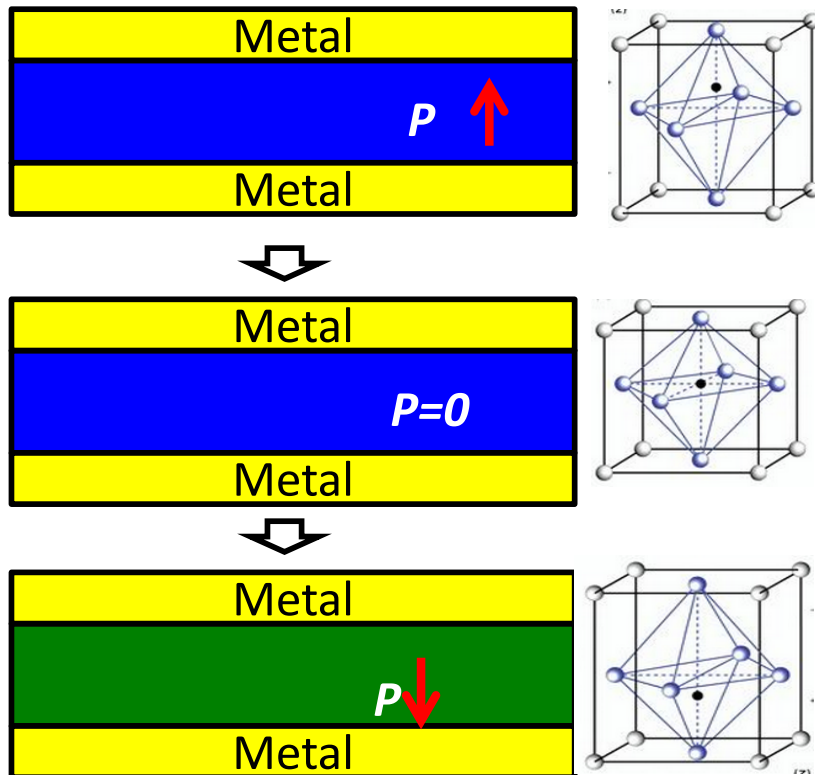


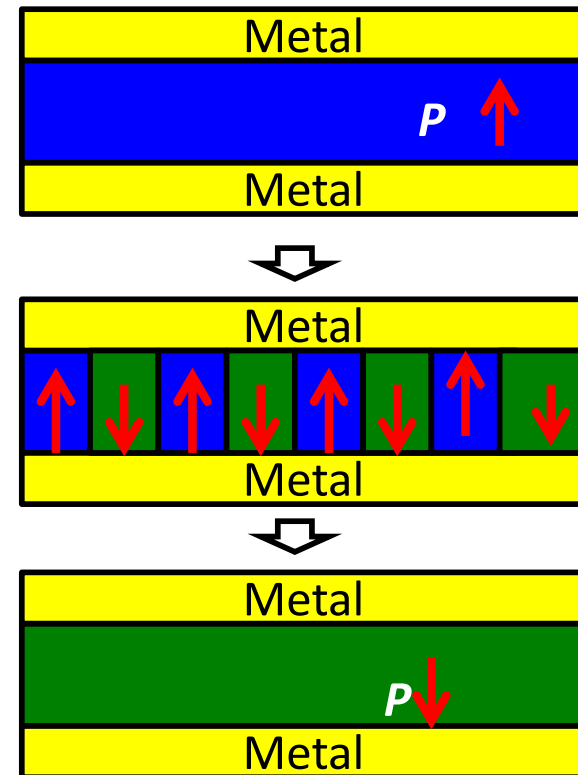
FIG. 1. Pulsing field and pulsing current *versus* time.

Effects of Domain Mechanisms on NC

Landau-Khalatnikov Dynamics



Domain Mediated Dynamics



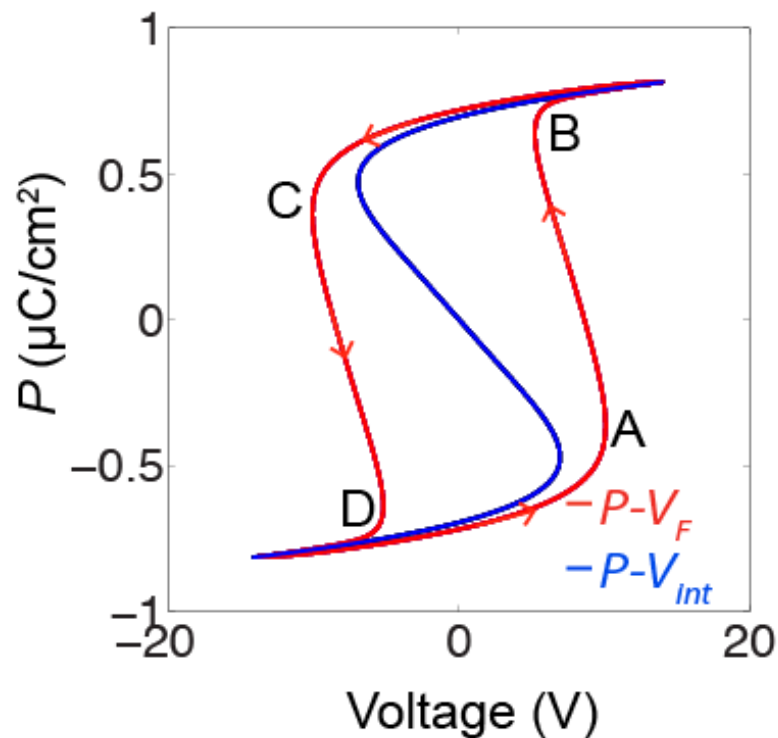
The Negative Capacitance effect is present even though the ferroelectric does not switch in a single domain fashion.

Effects of Domain Mechanisms on NC

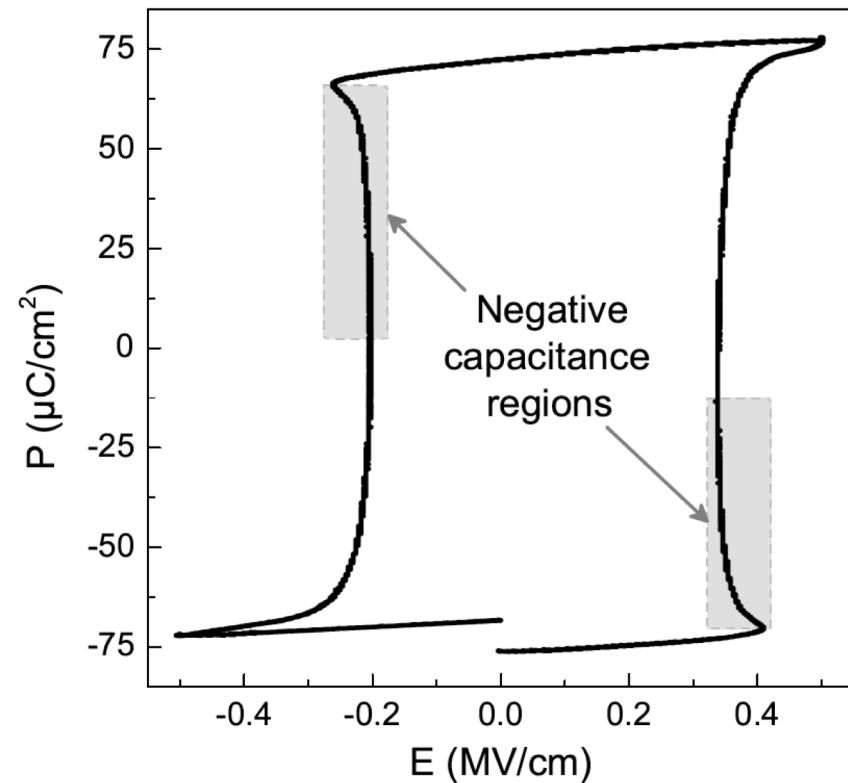
1-D Landau Simulations

Landau-Khalatnikov
Equation:

$$\rho \frac{dP}{dt} = - \frac{dU}{dP}$$



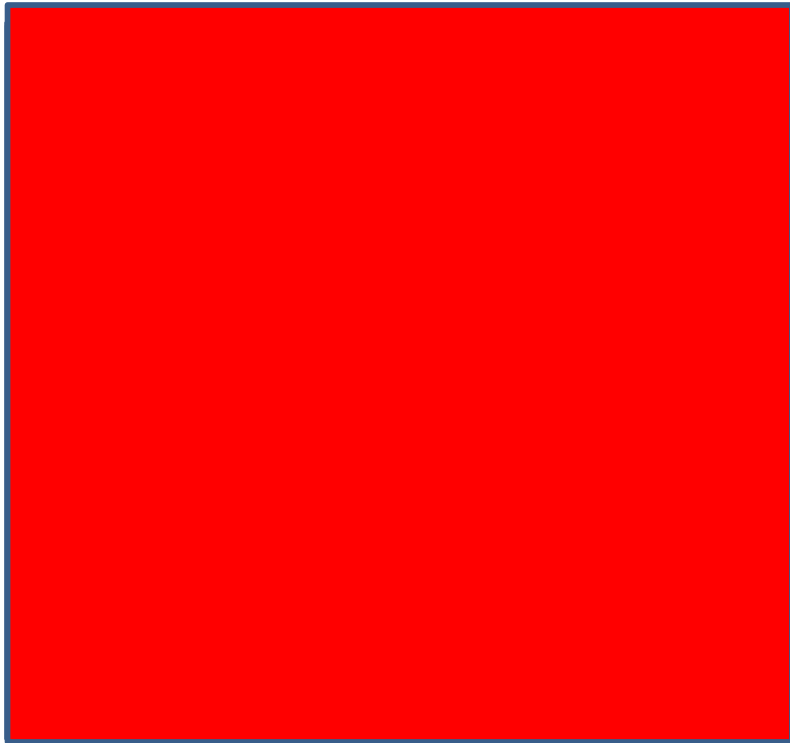
Experimental Charge-Field Hysteresis



Discrepancy between shape of experimental hysteresis curve and the prediction from 1-D L-K simulations

Effects of Domain Mechanisms on NC

Domain mediated
Polarization switching

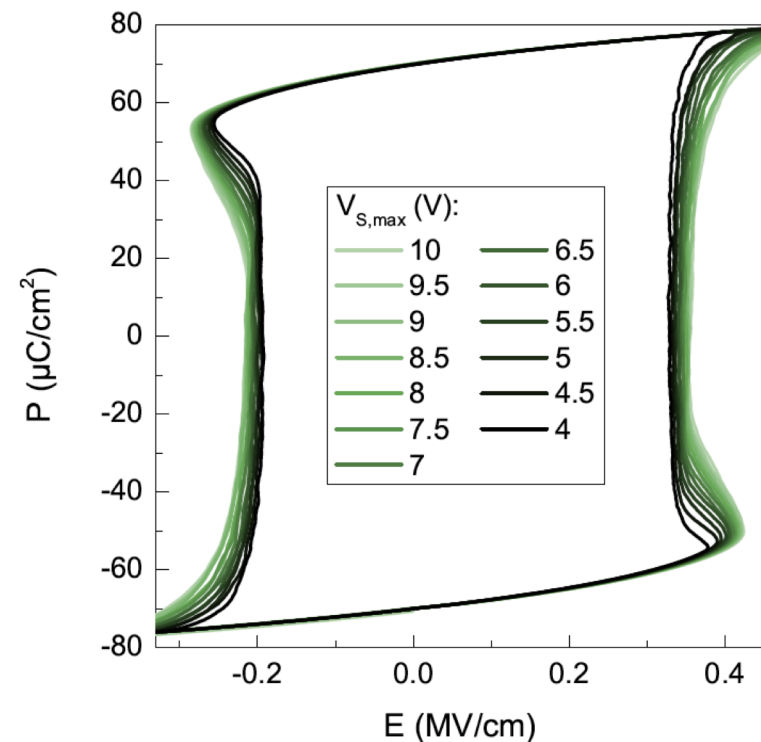


Hoffmann, Khan et al. (under review)
Preprint: <https://arxiv.org/abs/1711.07070>

Simulation based on Time
dependent Ginzburg-Landau
formalism

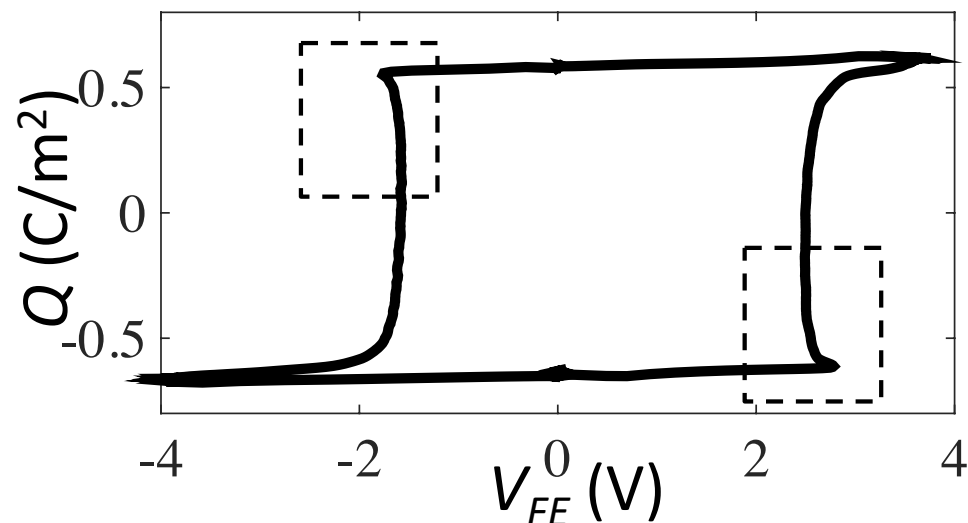
$$-\frac{\partial u_i}{\partial P_i} = \rho_i \frac{\partial P_i}{\partial t}$$

$$u_i = \alpha_i P_i^2 + \beta_i P_i^4 + \gamma_i P_i^6 - EP_i + k \sum_j \left(\frac{P_i - P_j}{\Delta x} \right)^2$$



What's next?

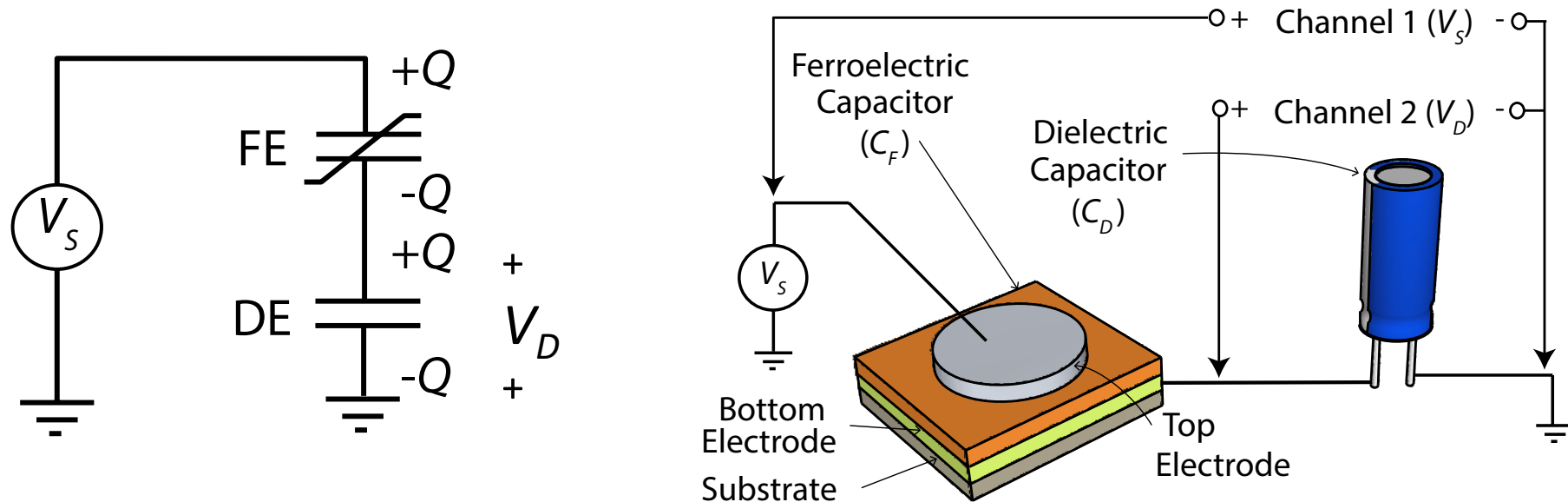
Now that negative capacitance has been detected...



How to achieve voltage amplification from negative capacitance?

How to stabilize negative capacitance?

Ferroelectric+Dielectric Capacitor

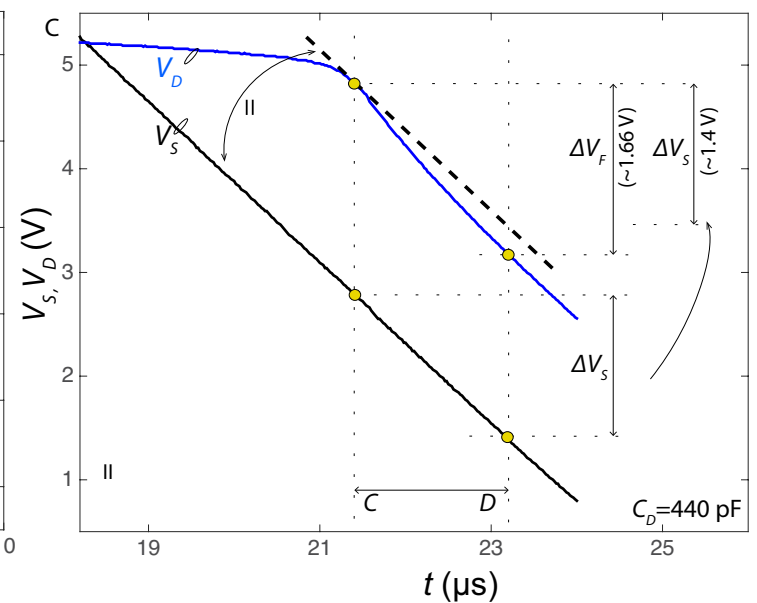
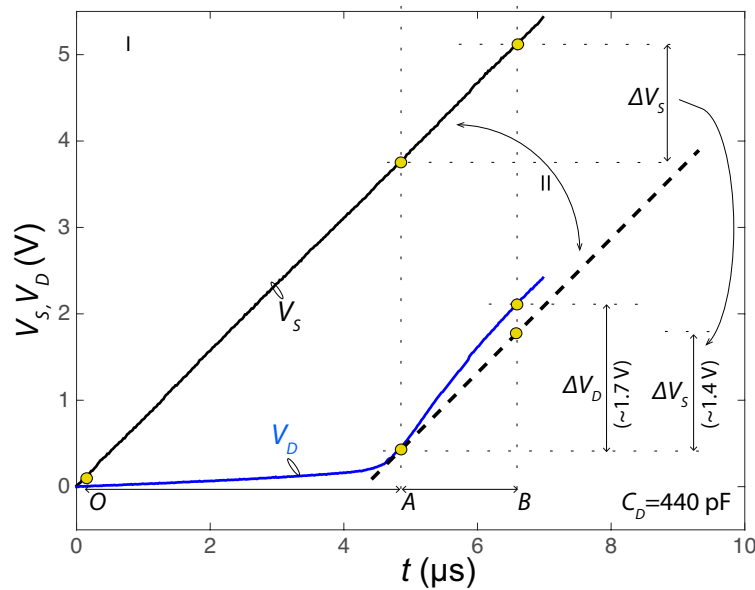
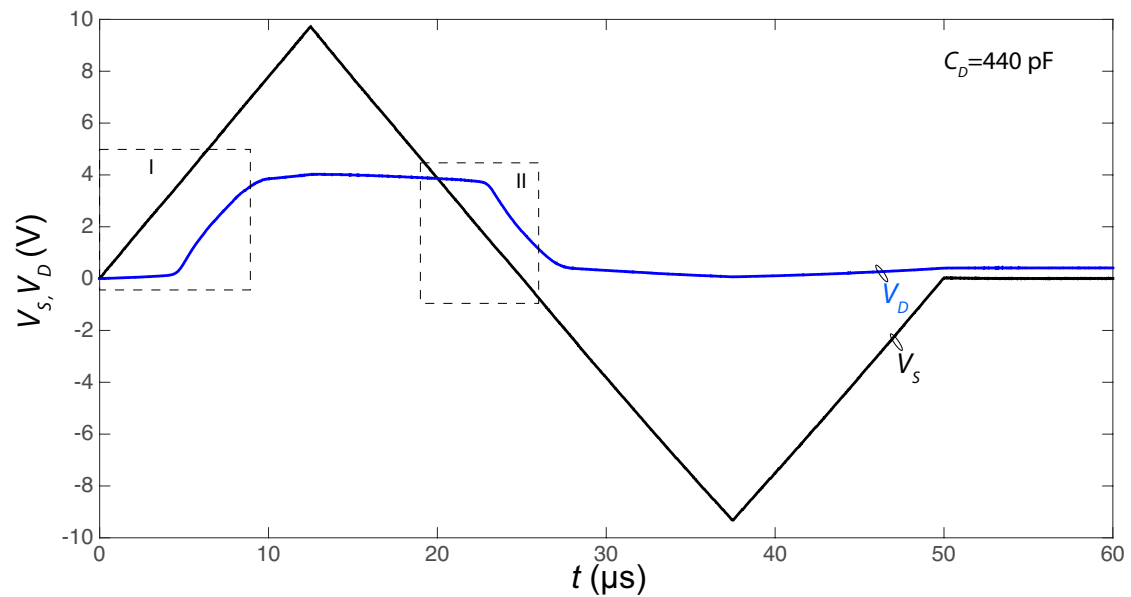
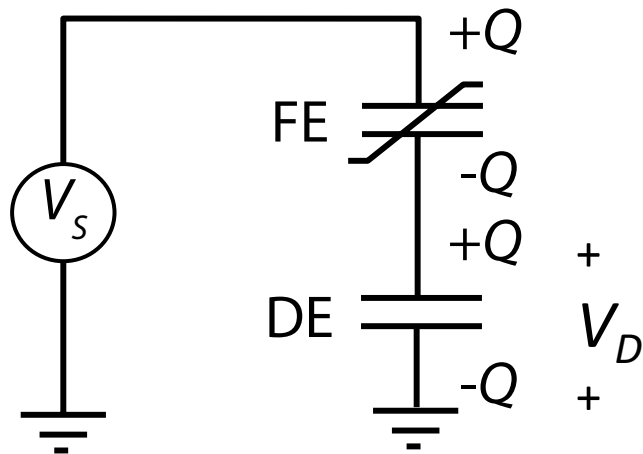


Voltage amplification:
$$\frac{dV_D}{dV_S} = \frac{C_F}{C_F + C_D} = \frac{|C_F|}{|C_F| - C_D} \quad \text{If } |C_F| > C_D, \quad \frac{dV_D}{dV_S} > 1$$

Equivalent Capacitance
$$C_{F+D} = \left[\frac{1}{C_D} + \frac{1}{C_F} \right]^{-1} \quad \text{If } |C_F| > C_D, \quad C_{D+F} > C_D$$

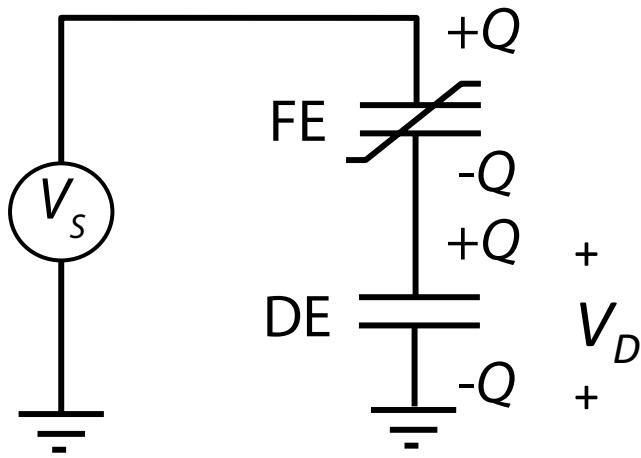
Khan, Hoffmann et al. (under review)

Ferroelectric+Dielectric Capacitor



Khan et al. Appl. Phys. Lett. 111, 253501 (2017)

Ferroelectric+Dielectric Capacitor

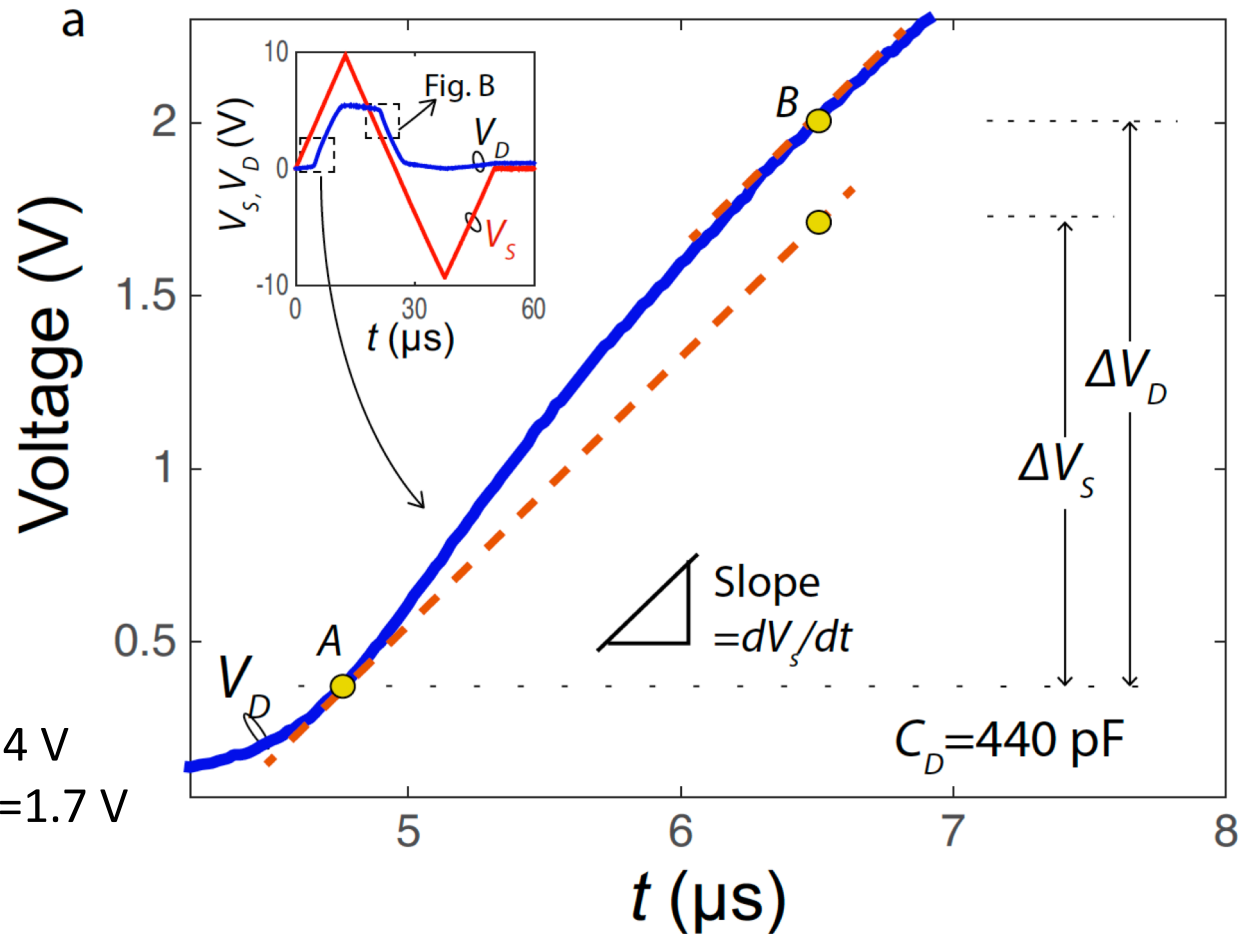


Khan, Hoffmann et al. (under review)

Change in source voltage $\Delta V_S = 1.4 \text{ V}$
 Change in dielectric voltage $\Delta V_D = 1.7 \text{ V}$

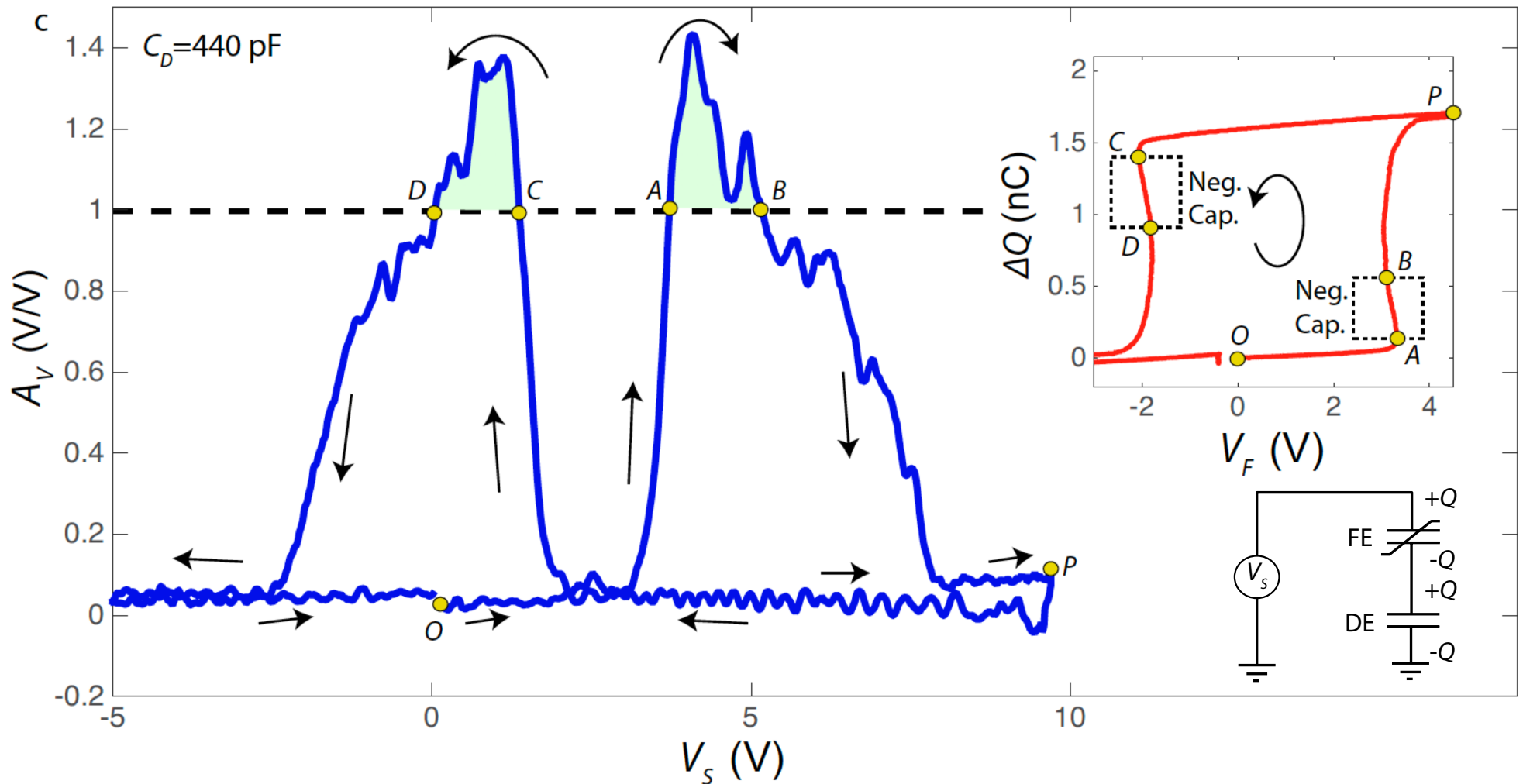
$$\frac{\Delta V_D}{\Delta V_S} = \frac{1.7 \text{ V}}{1.4 \text{ V}} \approx 1.21 = \frac{|C_F|}{|C_F| - C_D}$$

Khan et al. Appl.
 Phys. Lett. 111,
 253501 (2017)



Voltage amplification in a FE-DE
 series network experimentally
 observed!

Ferroelectric+Dielectric Capacitor

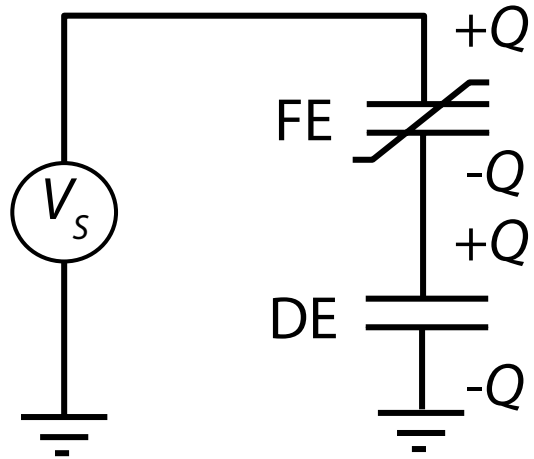


Khan et al. Appl. Phys. Lett. 111, 253501 (2017)

Voltage amplification in a FE-DE series network experimentally observed!

Stabilization and capacitance enhancement

Ferroelectric-Dielectric
Series Combination

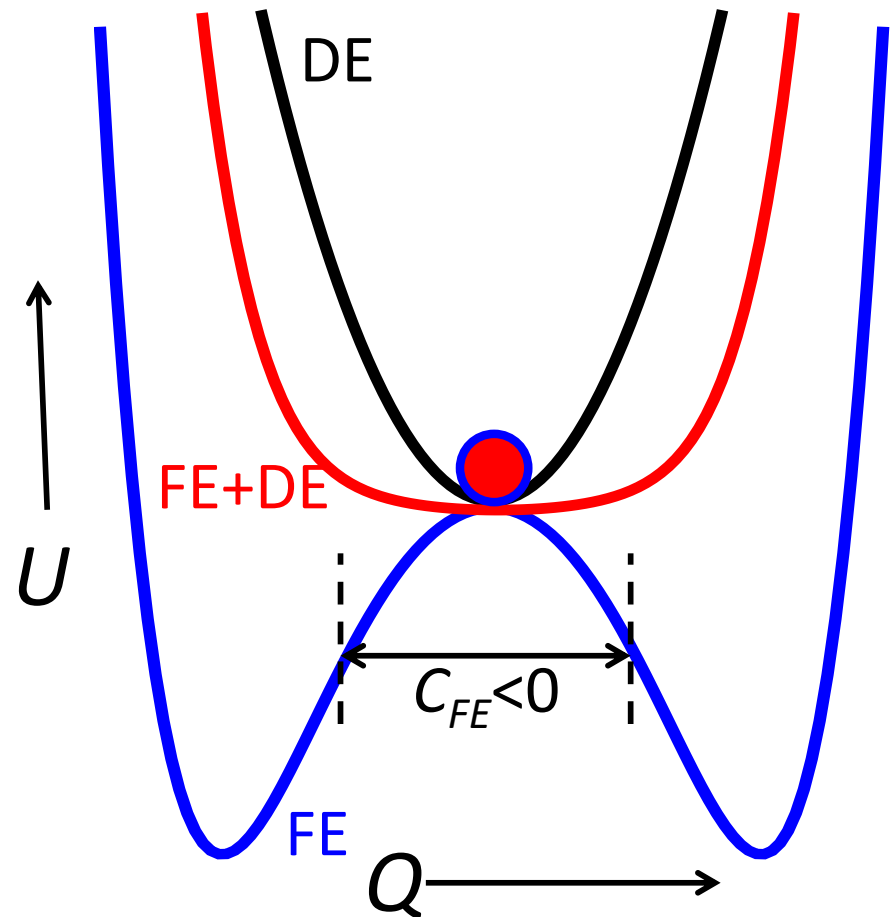


$$C = \left[\frac{d^2 U}{dQ^2} \right]^{-1}$$

Equivalent Capacitance $C_{FE+DE} = \left[\frac{1}{C_{FE}} + \frac{1}{C_{DE}} \right]^{-1}$

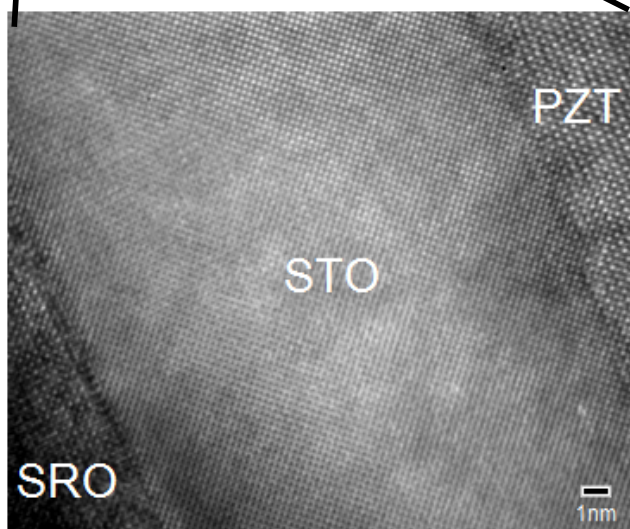
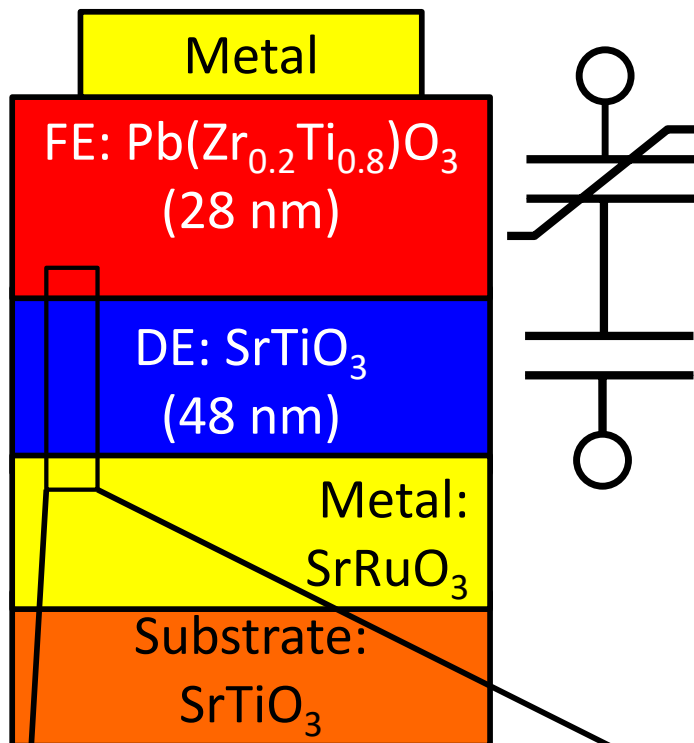
$$C_{FE+DE} > C_{DE} \quad \text{if} \quad C_{FE} < 0$$

Energy Landscapes

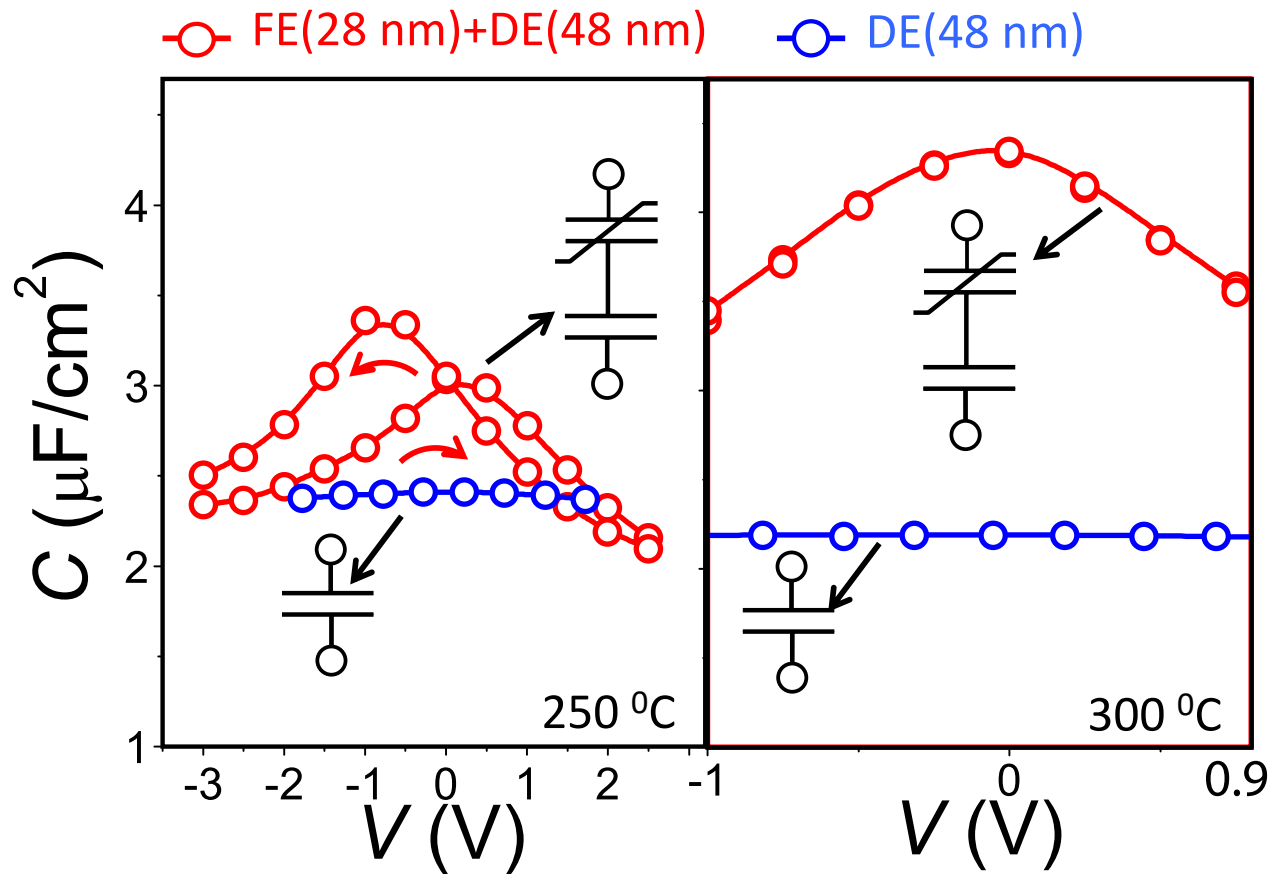


Enhancement of capacitance in a FE-DE Series combination!

Capacitance Enhancement due to Neg. Cap.



C-V Characteristics

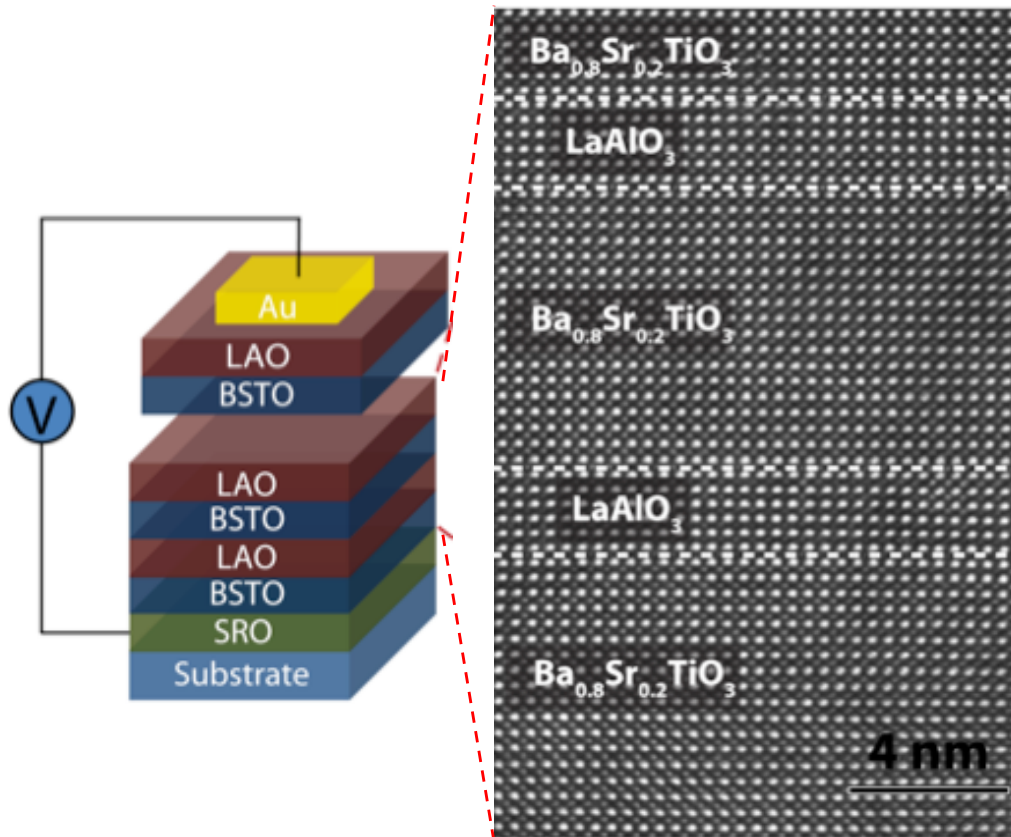


Capacitance Enhancement in a FE-DE heterostructure experimentally observed!

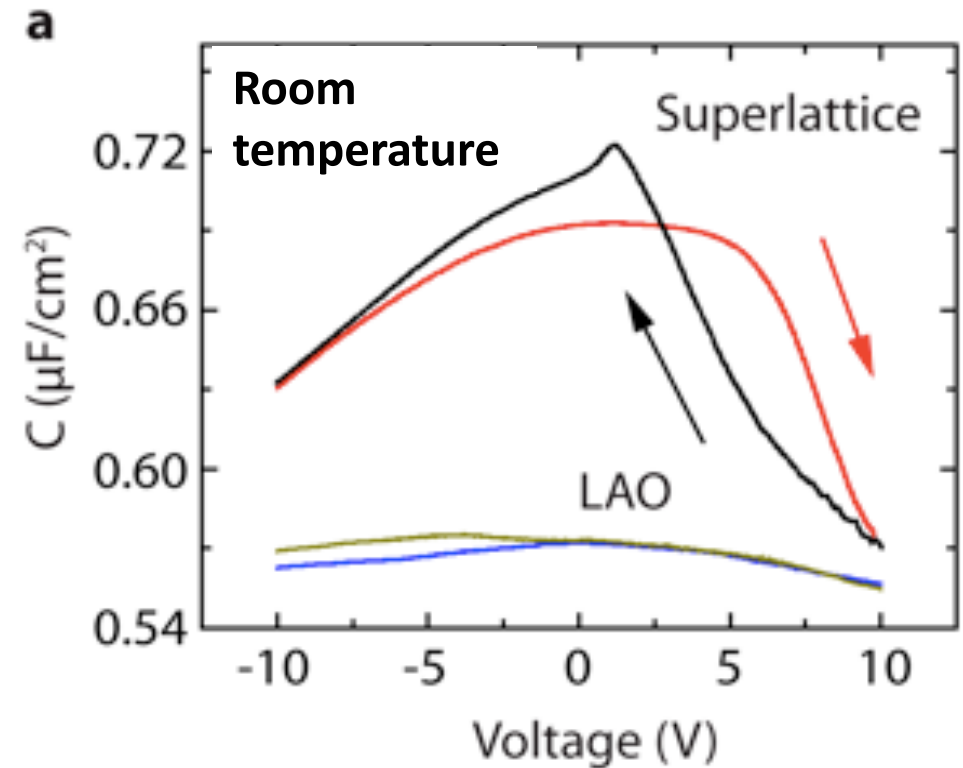
Khan et al. Appl. Phys. Lett. 100, 113501 (2011)
(cover article, most downloaded Aug/Sep 2011).
Gao, Khan et al. Nano Lett. 14, 5814 (2014)

Negative Capacitance in $(\text{Ba}_{0.8}\text{Sr}_{0.2})\text{TiO}_3$

$(\text{Ba}_{0.8}\text{Sr}_{0.2})\text{TiO}_3$ bulk Curie Temperature: $<110^\circ\text{C}$



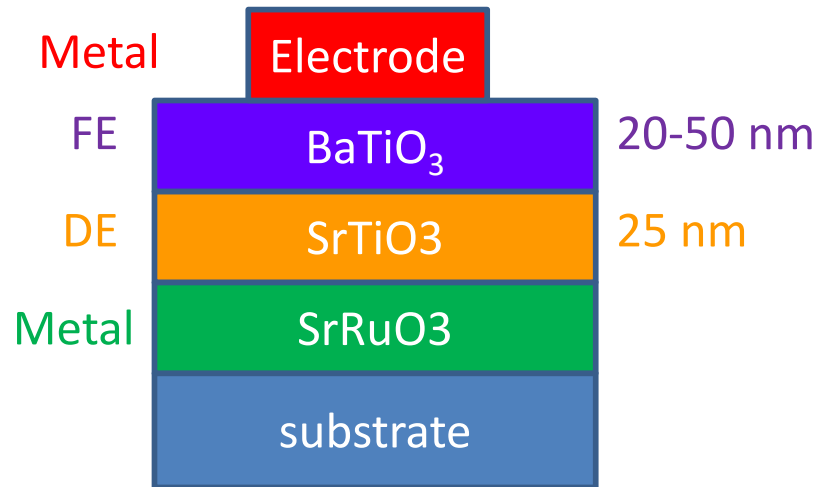
Superlattice: LAO(6 monolayer (ML))/BSTO(18 ML) repeated 11 times on GSO.



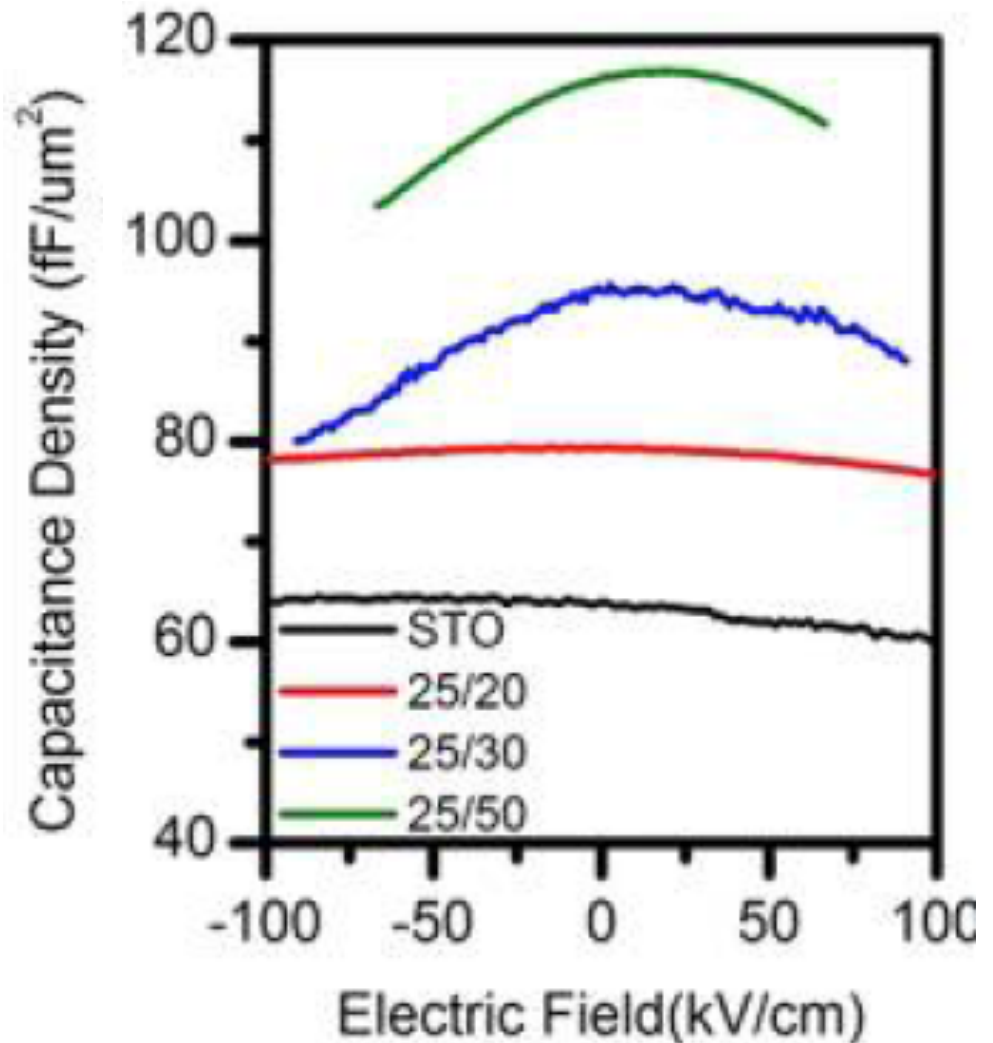
W. Gao, A. Khan et al. Nano Lett. 14, 5814 (2014).

Capacitance enhancement at room temperature

Negative Capacitance in BaTiO₃

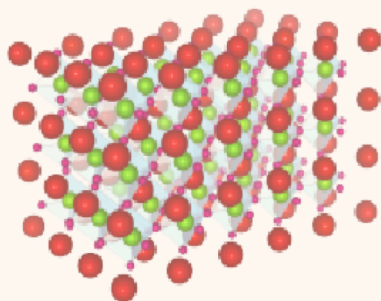


Room temperature Negative Capacitance observed in BaTiO₃ owing to its low Curie temperature.

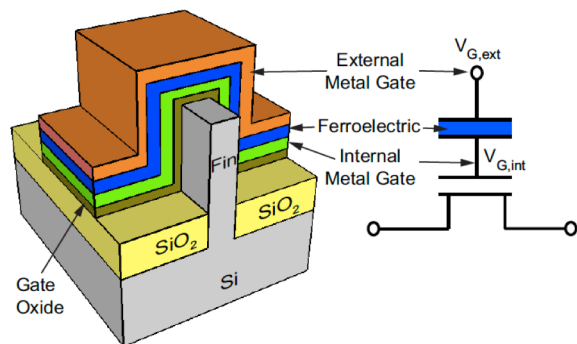


What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors

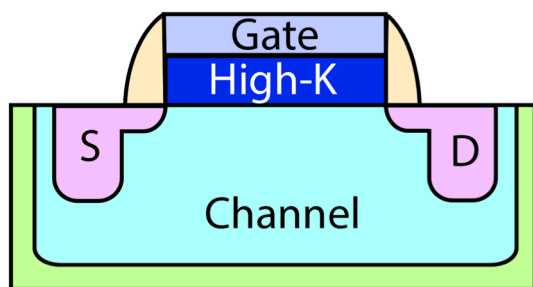


What do we need to know?

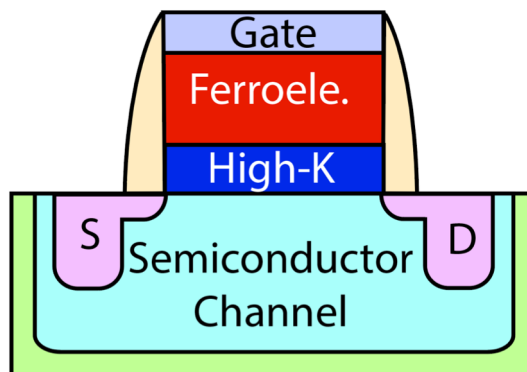


Physics of Negative Capacitance FET

Baseline FET



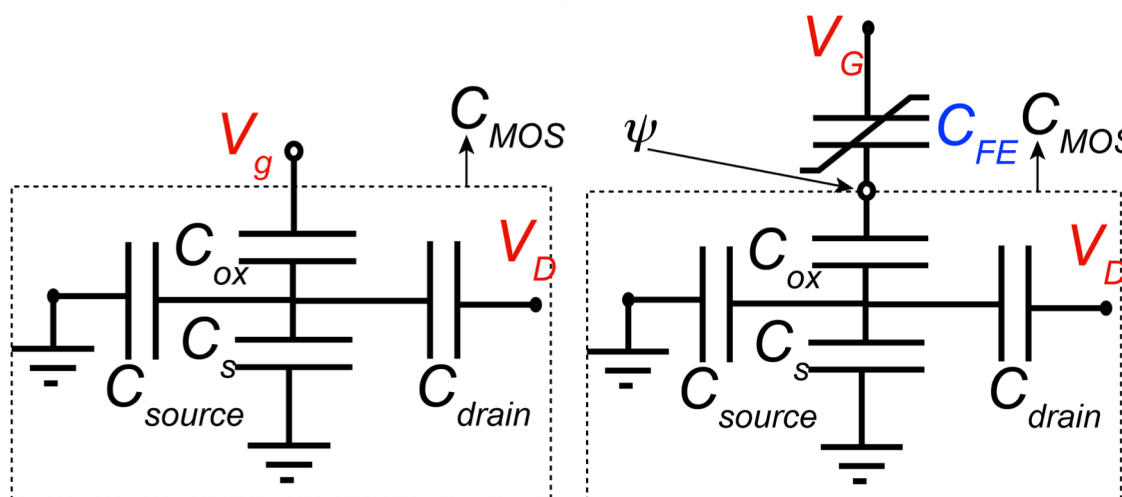
NCFET



Amplification Factor

$$\frac{d\psi}{dV_G} = \frac{C_{FE}}{C_{FE} + C_{MOS}} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}}$$

Modified Body Factor $m^o = \frac{dV_G}{d\psi} = 1 - \frac{C_{MOS}}{|C_{FE}|}$



Subthreshold Swing $S^{NC} = S^{original} \times (1 - \frac{C_{MOS}}{|C_{FE}|})$

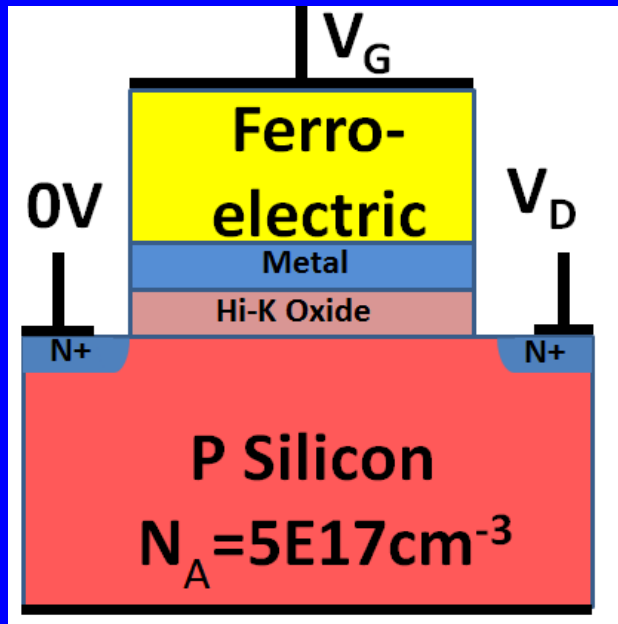
Ideal Switch: ~ 0 mV/decade $\Leftarrow$
 $|C_{FE}| \approx C_{MOS}, |C_{FE}| > C_{MOS}$

Condition	Characteristics	Mode
$C_{FE} < 0, C_{FE} > C_{MOS}$	$0 < m^o < 1, S^{NC} < S^{original}$	Logic
$C_{FE} < 0, C_{FE} < C_{MOS}$	$m^o < 0, S^{NC} < 0$	Memory

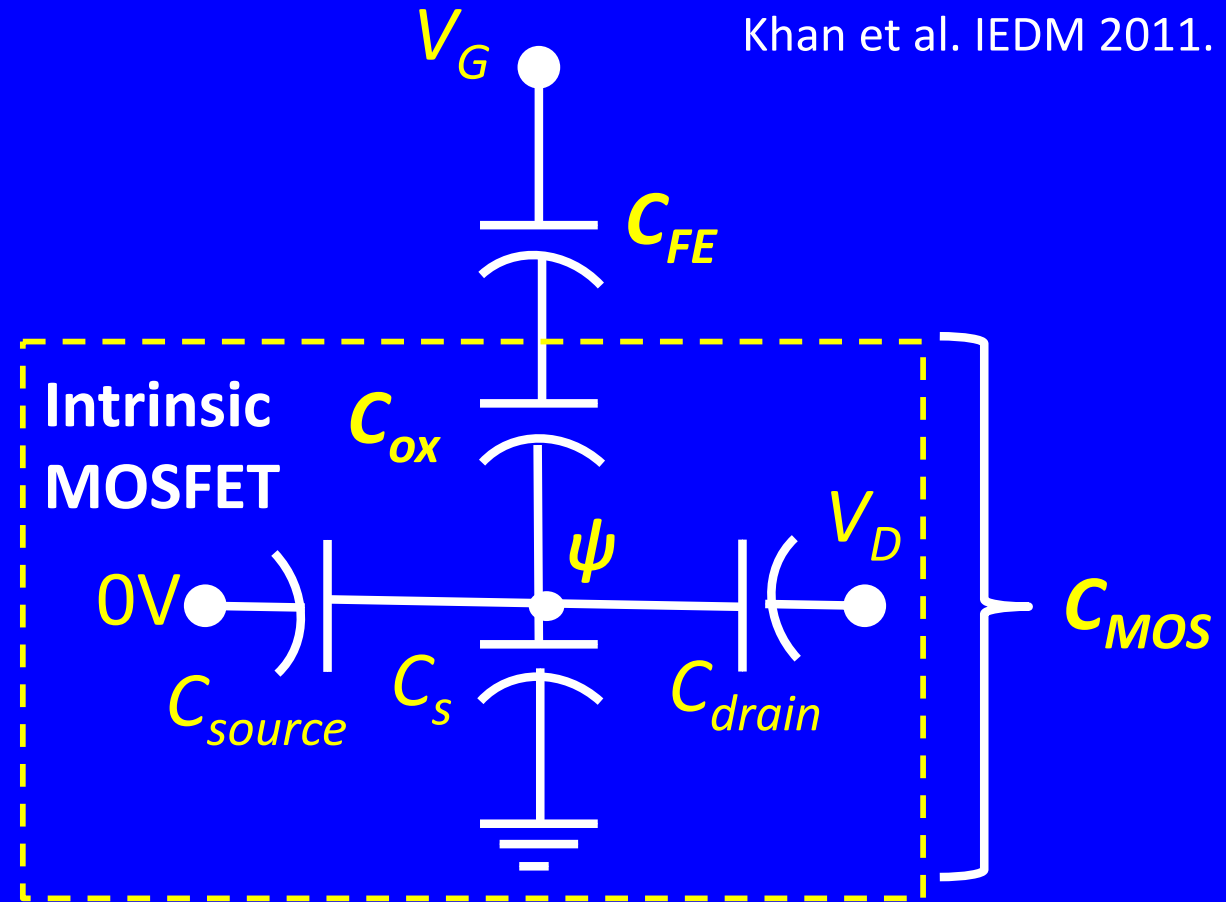
Khan et al. IEDM 2011

Sub 60mV/dec Negative Capacitance FET: Capacitance Tuning Perspective

Negative Capacitance FET



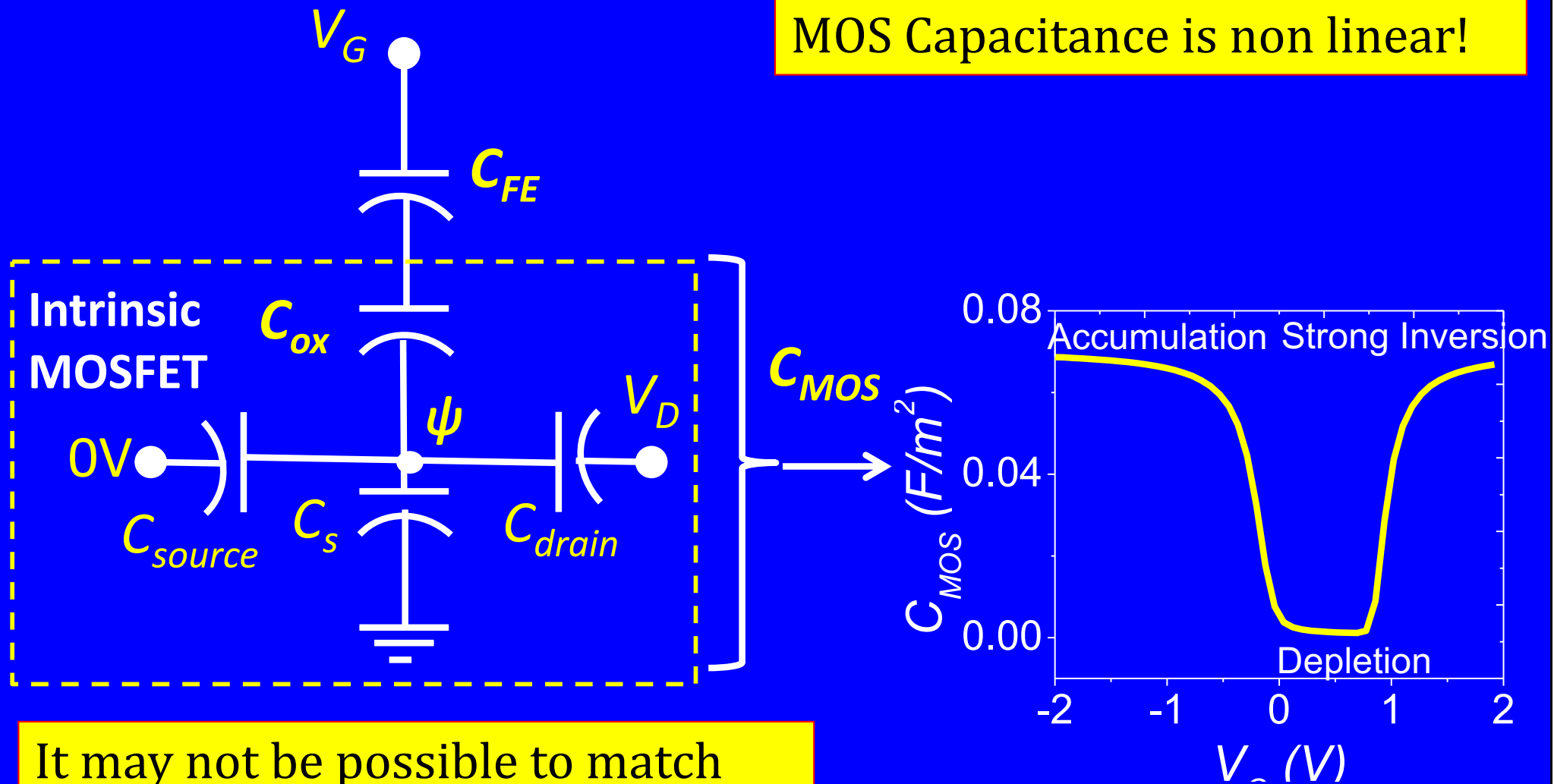
Khan et al. IEDM 2011.



Ideal Switch: $\sim 0 \text{ mV/decade} \Leftrightarrow |C_{FE}| \approx C_{MOS}, |C_{FE}| > C_{MOS}$
 Is it possible to match C_{FE} and C_{MOS} over a large range of charge densities and voltages?

Capacitance Matching in an NCFET

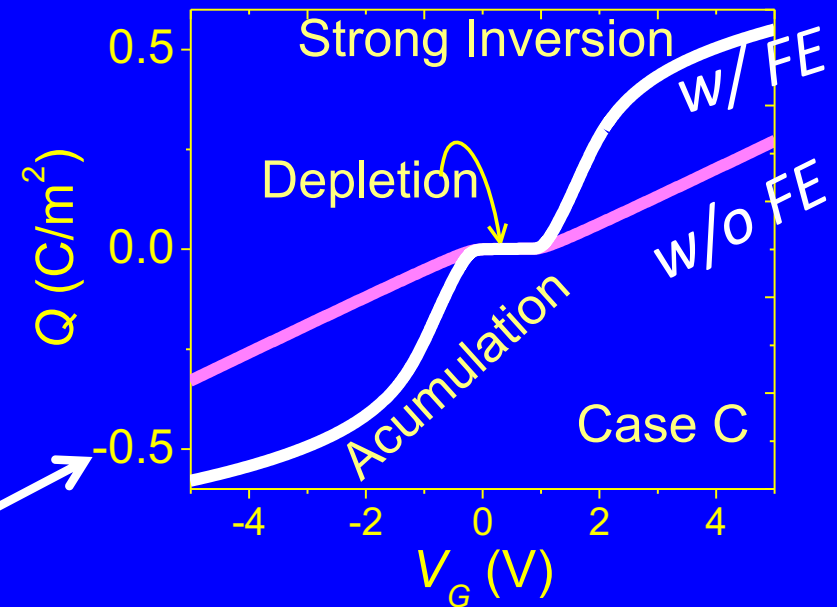
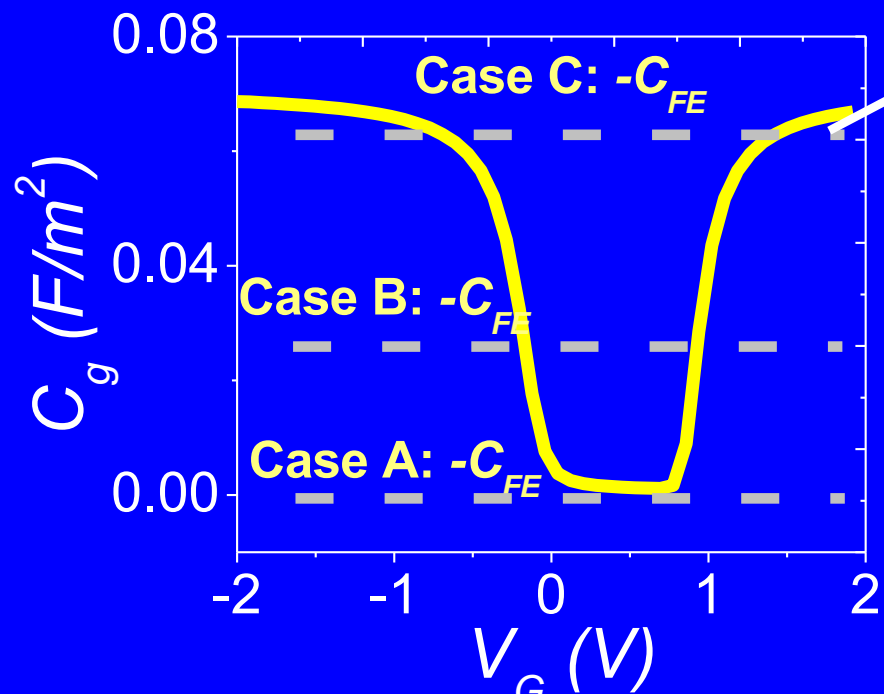
MOS Capacitance is non linear!



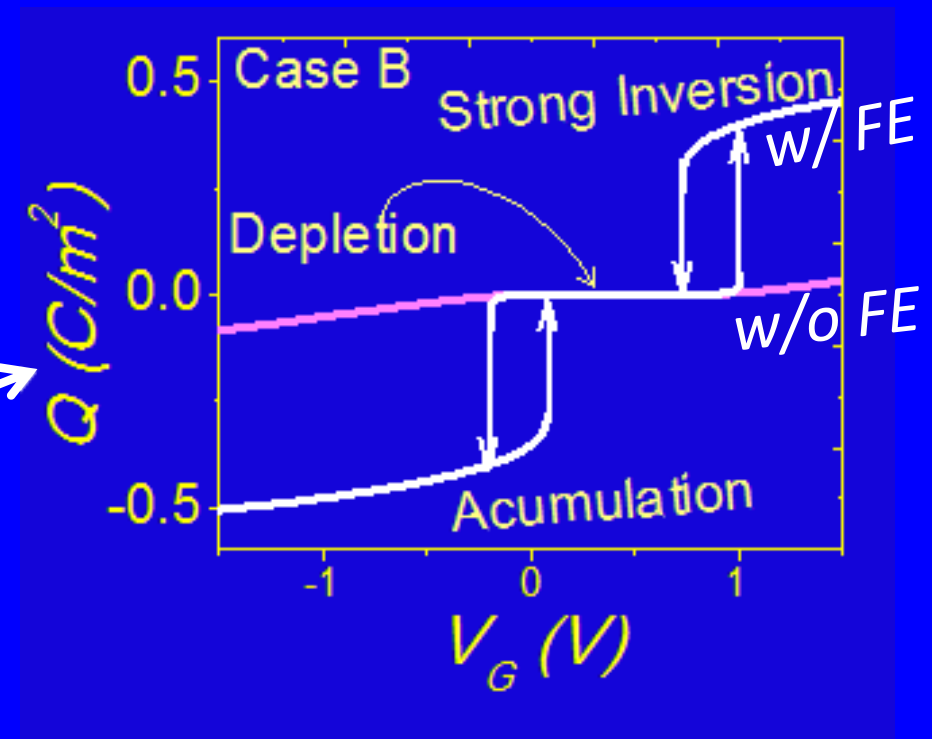
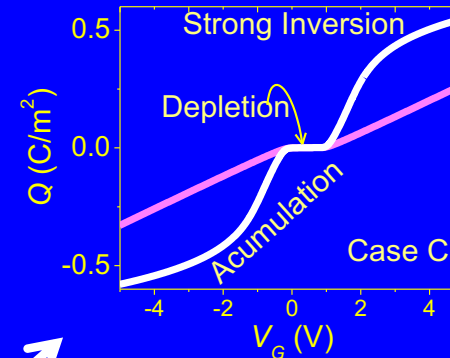
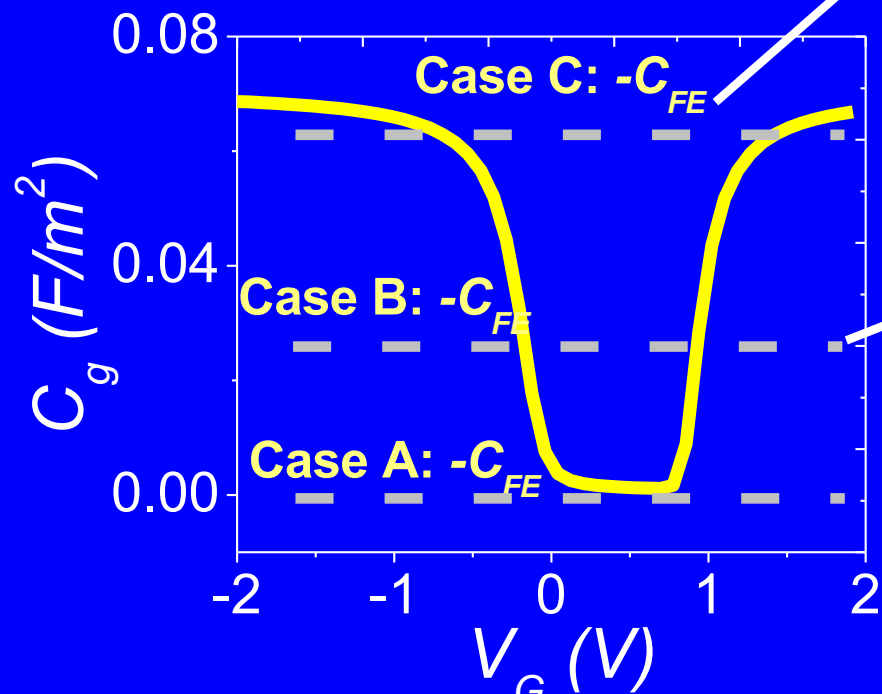
It may not be possible to match C_{FE} and C_{MOS} within the operational charge densities.

Khan et al. IEDM 2011.

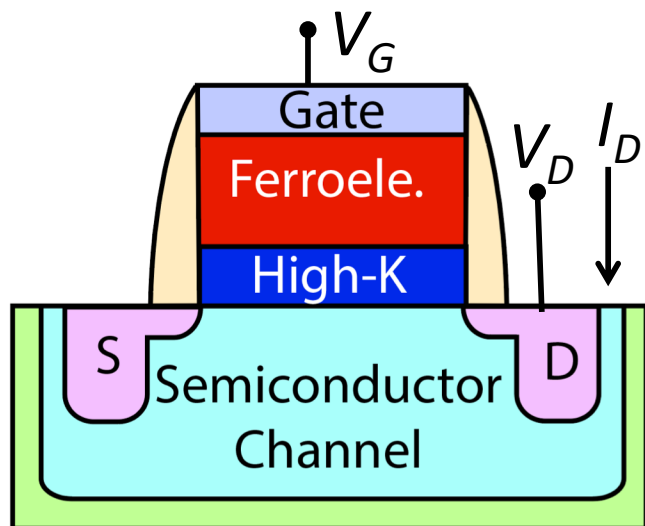
Capacitance Matching in a NCFET



Capacitance Matching in a NCFET



Physics of Negative Capacitance FET

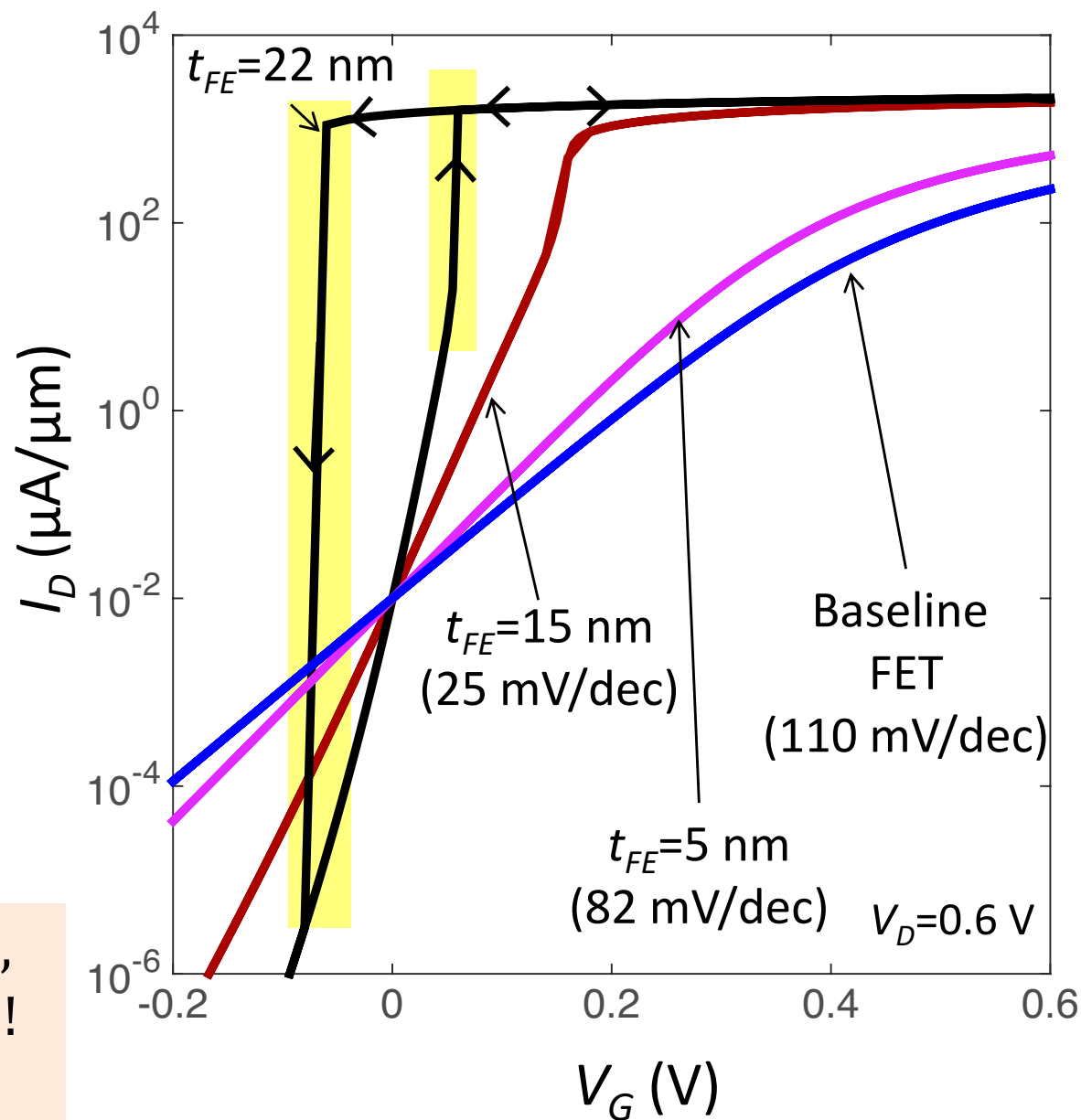


Ferroelectric Capacitance

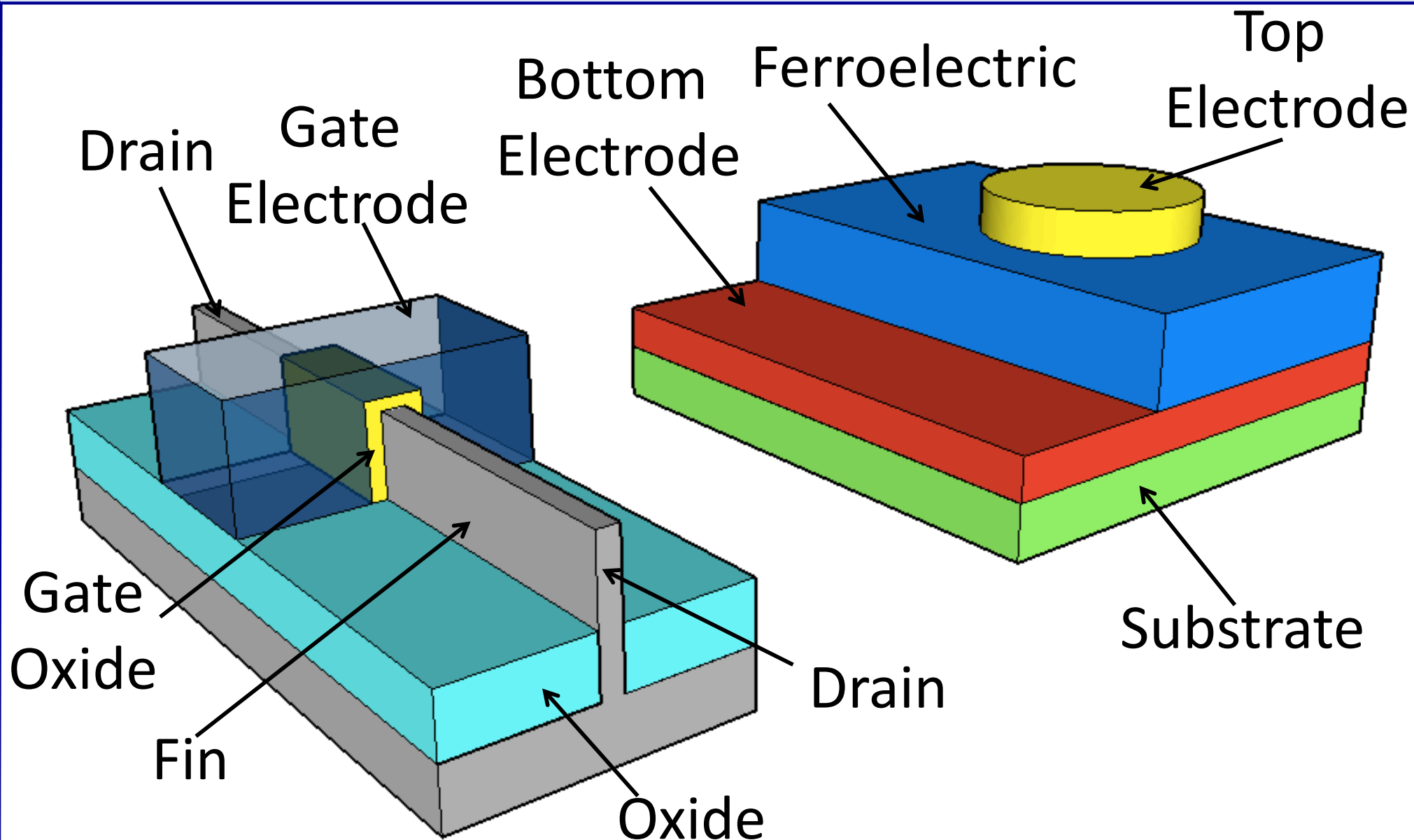
$$|C_{FE}| \approx \frac{P_o}{E_{FE} t_{FE}}$$

Intel 45 nm node, MIT MVS Model
Collaboration with
Dimitri Antoniadis, MIT

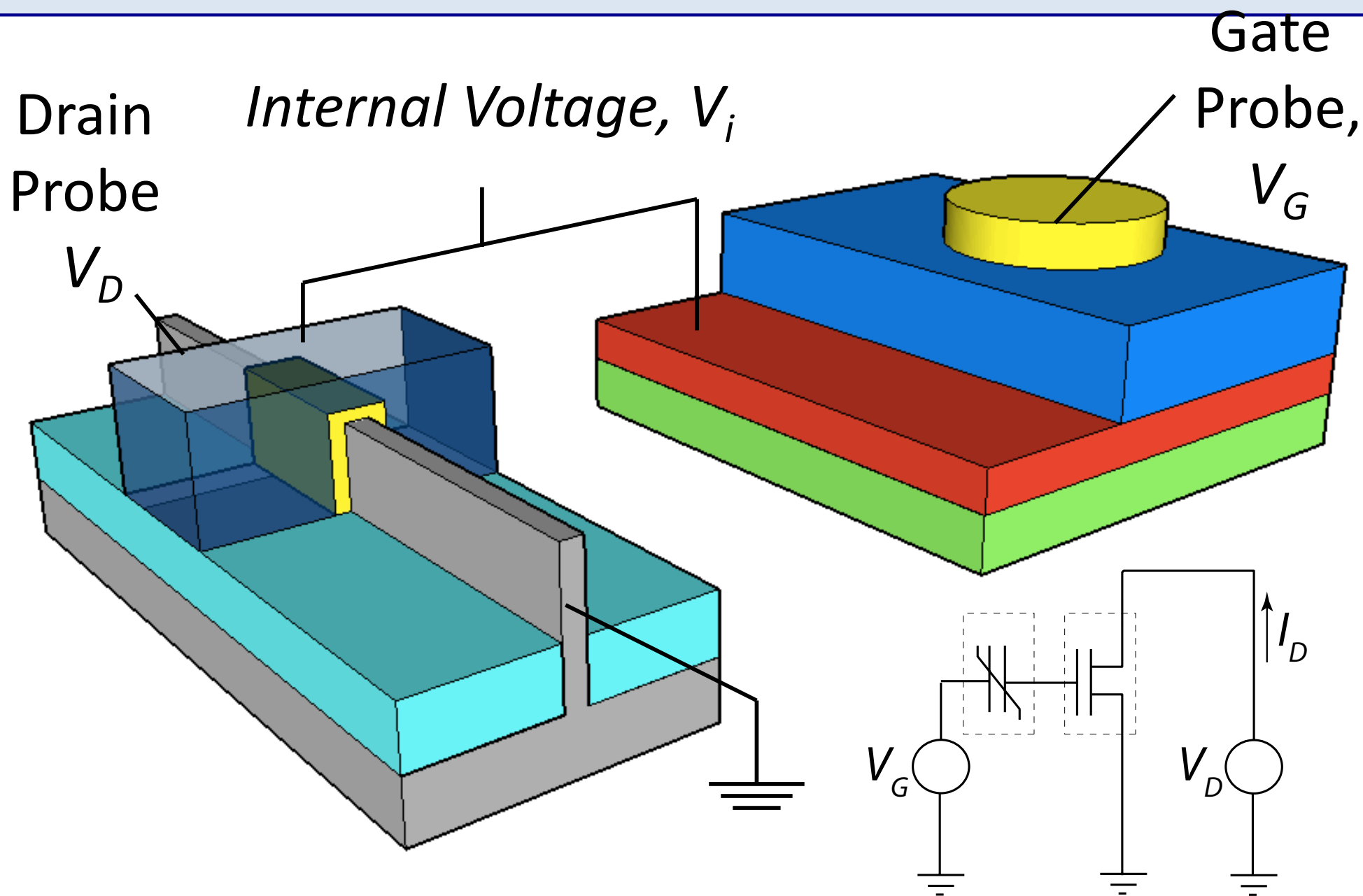
Below a critical FE thickness,
NCFET is a steep logic device!
Above that it's a memory
device!



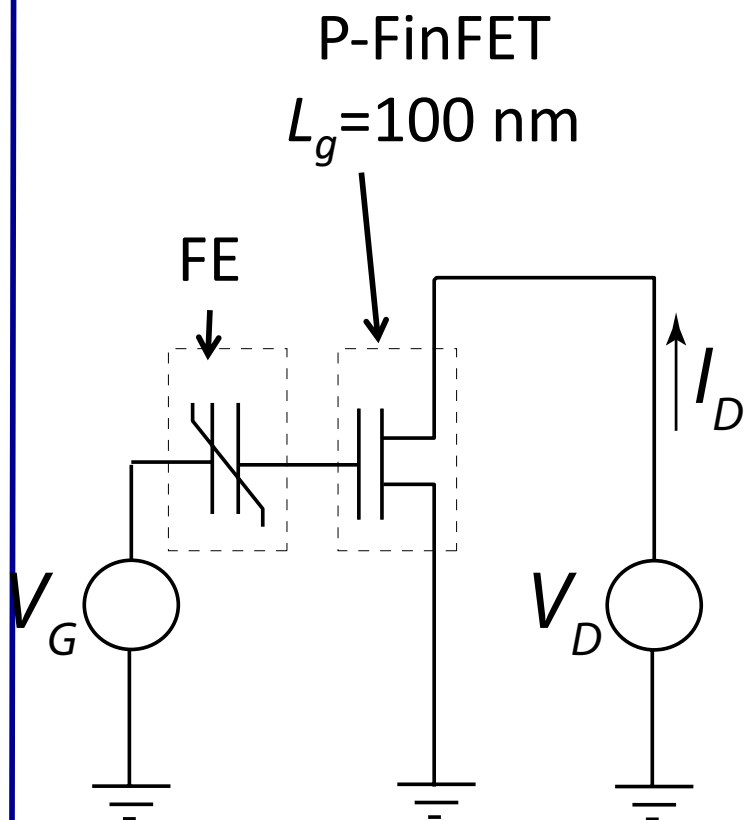
Externally Connected NC-FET



Externally Connected NC-FET

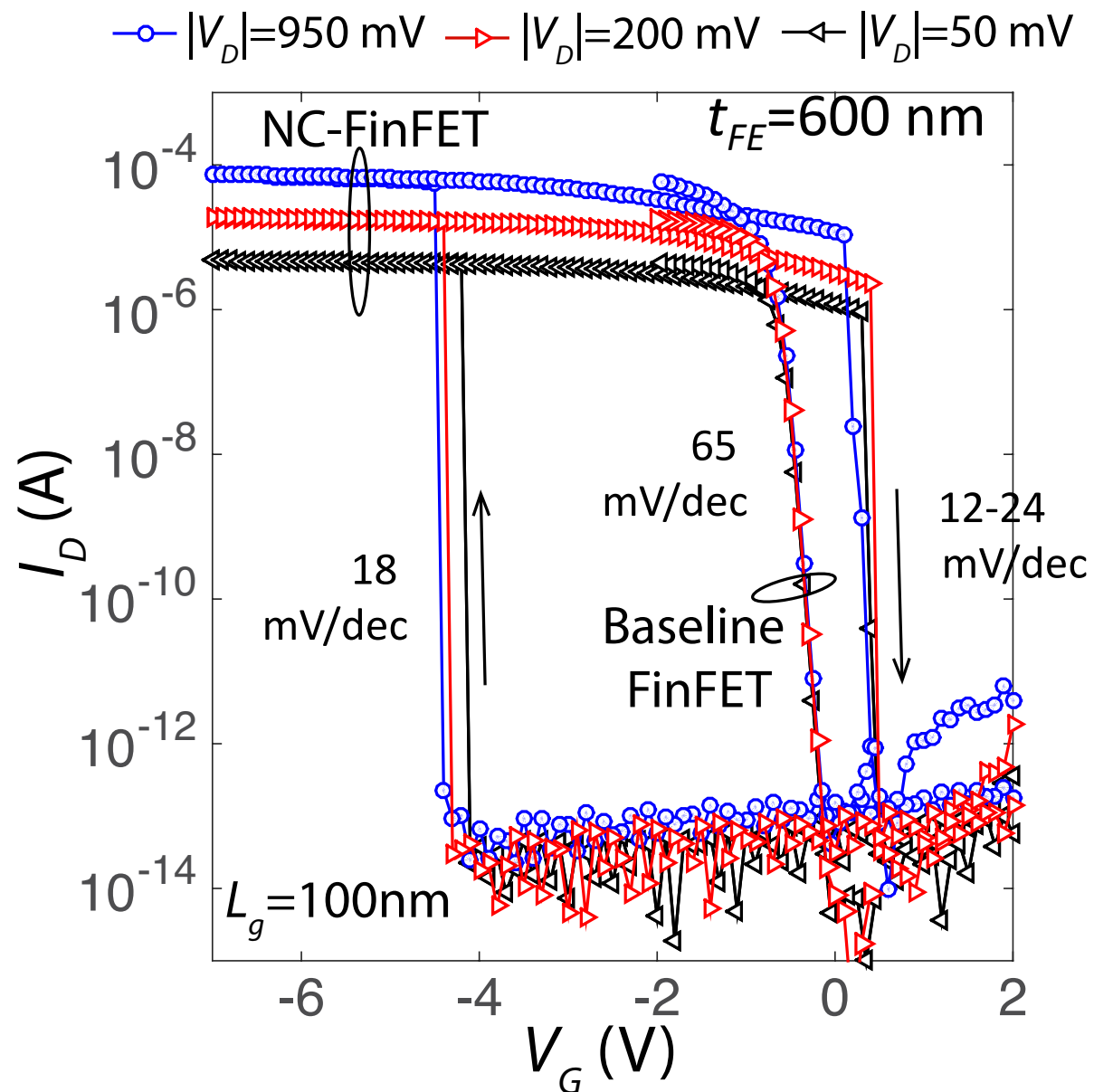


Externally Connected NC-FET

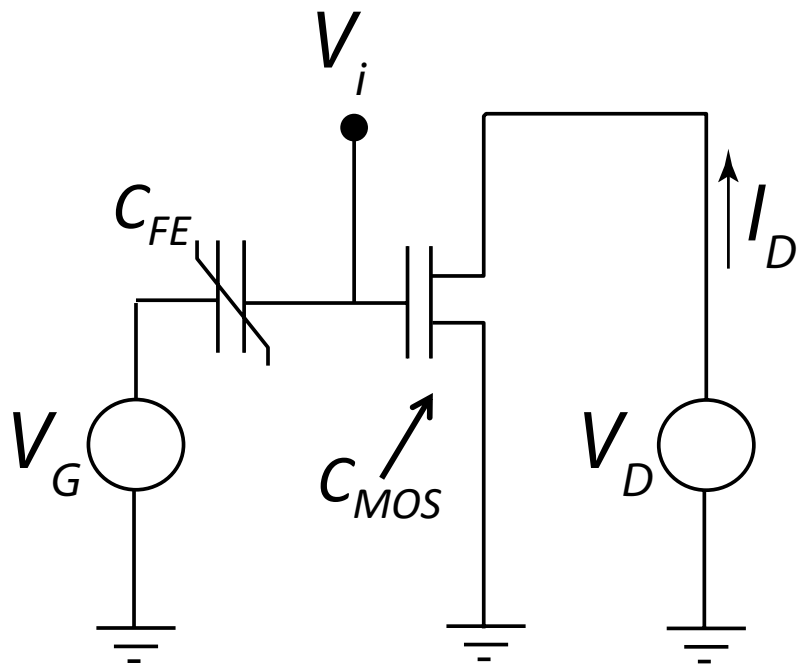


FinFET $L_G = 100 \text{ nm}$
 Fin width = 35 nm
 Fin height = 25 nm
 EOT = 1.4 nm

Khan et al. IEEE EDL 37, 111 (2016)

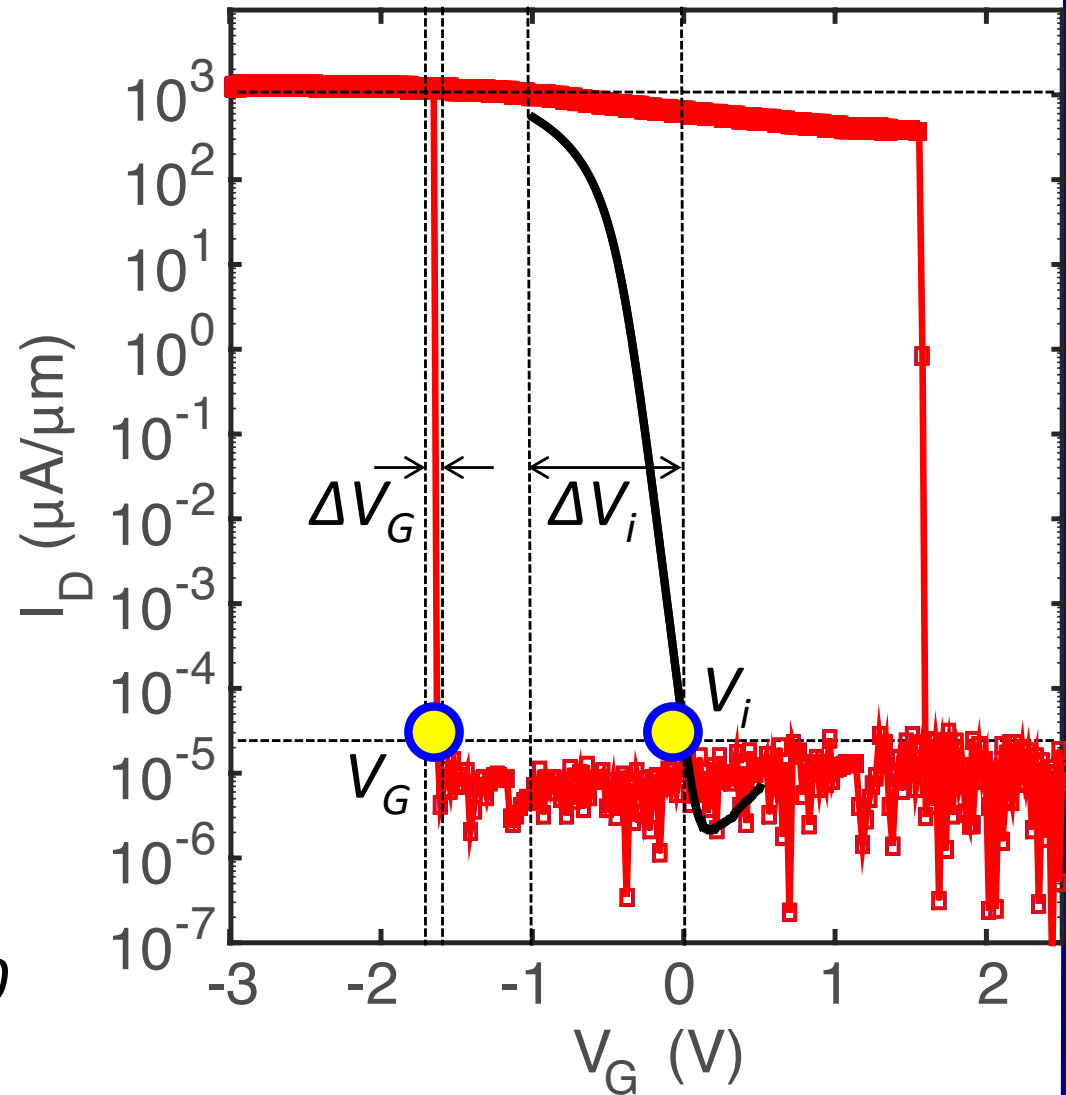


Negative Capacitance Transistors: Experiment



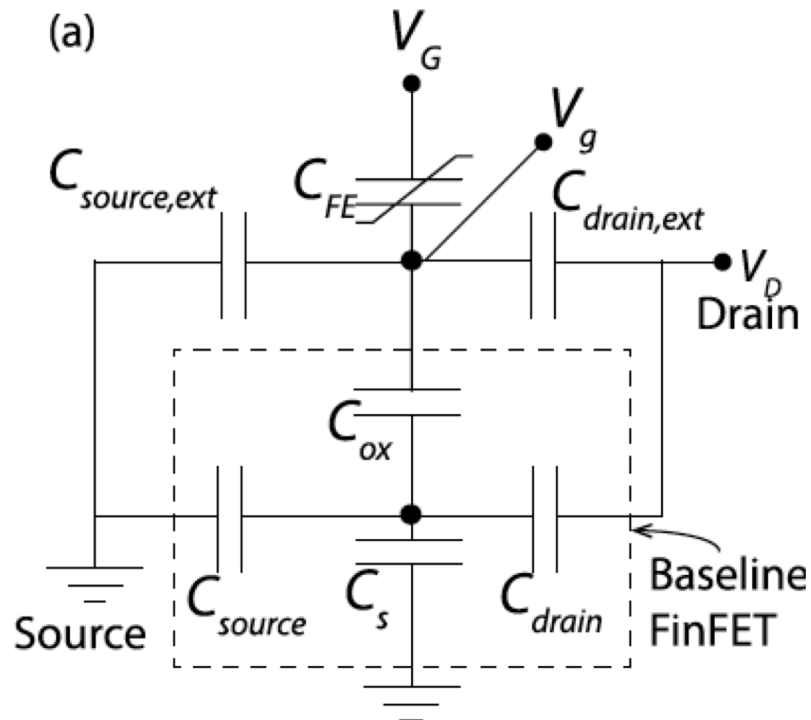
$$\frac{\Delta V_i}{\Delta V_G} > 1$$

$$\frac{\Delta V_i}{\Delta V_G} = \frac{C_{FE}}{C_{MOS} + C_{FE}} > 1 \text{ only if } C_{FE} < 0$$

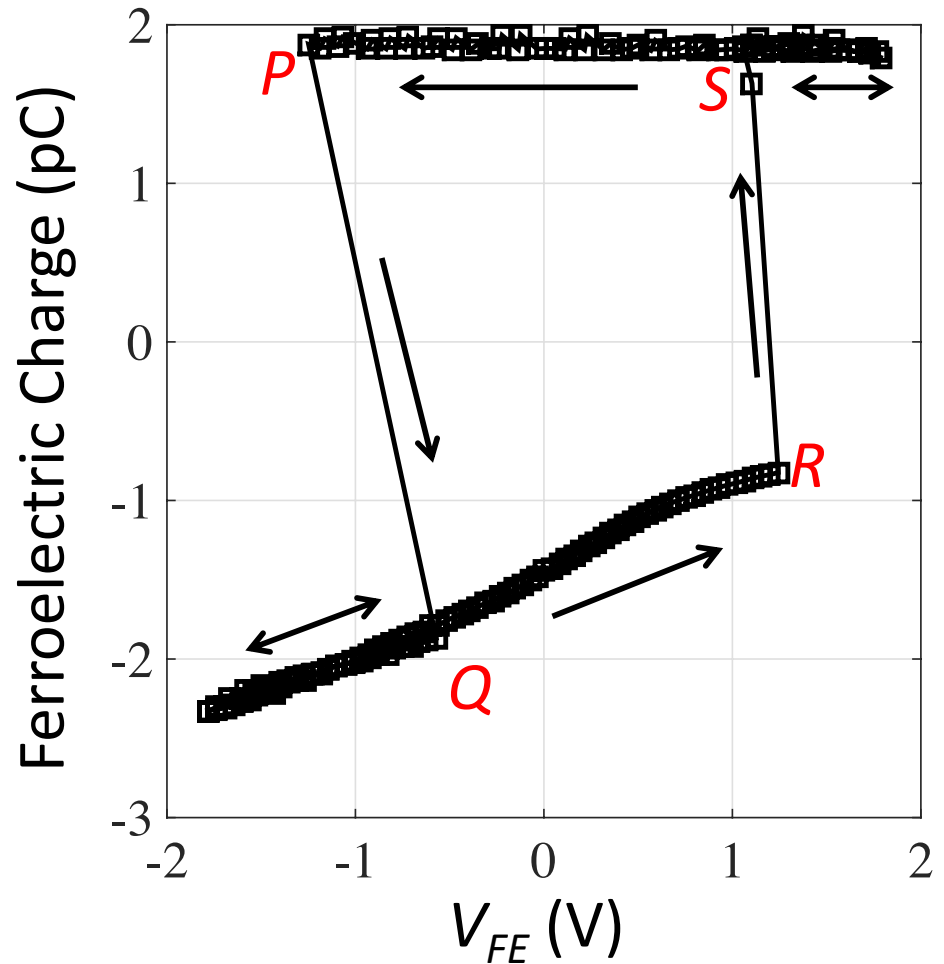


Sharp switching occurs due to ferroelectric negative capacitance!

Externally Connected NC-FET

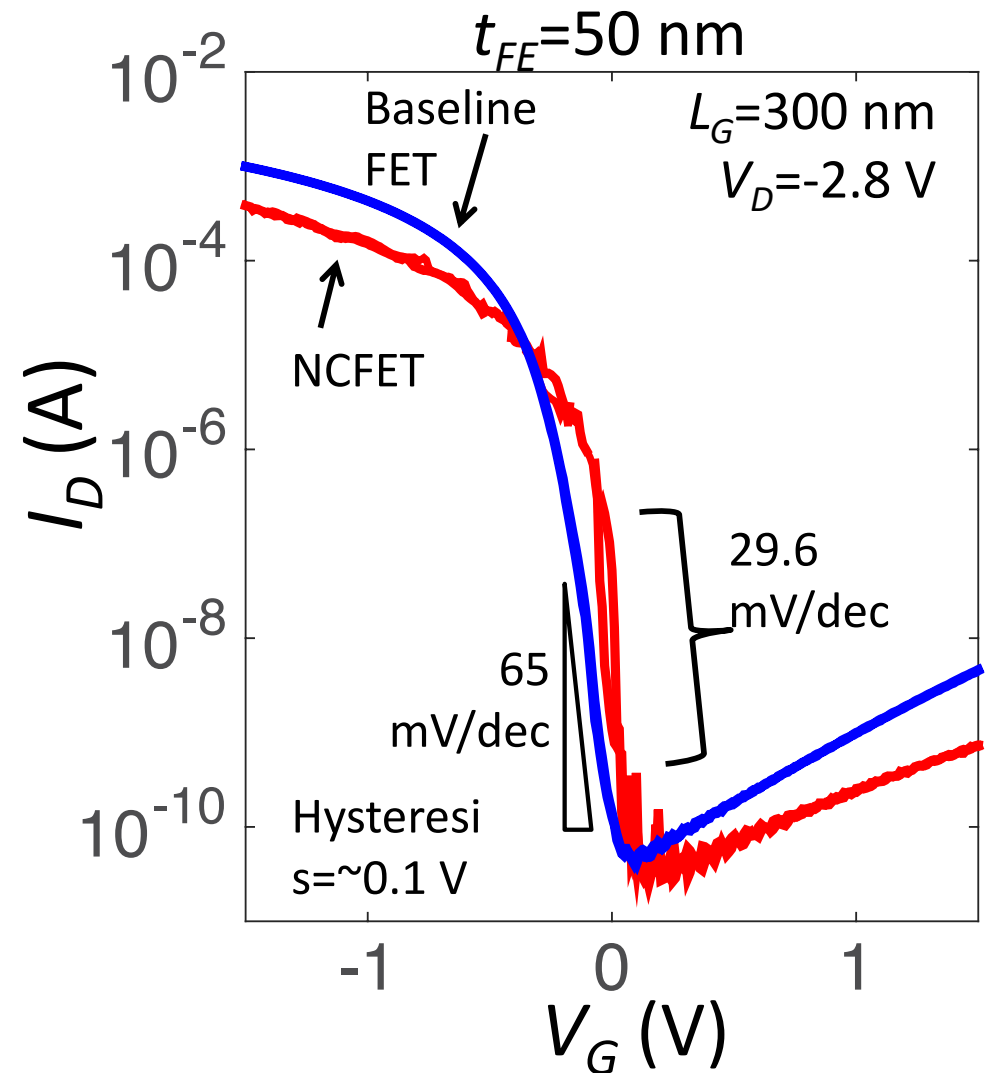
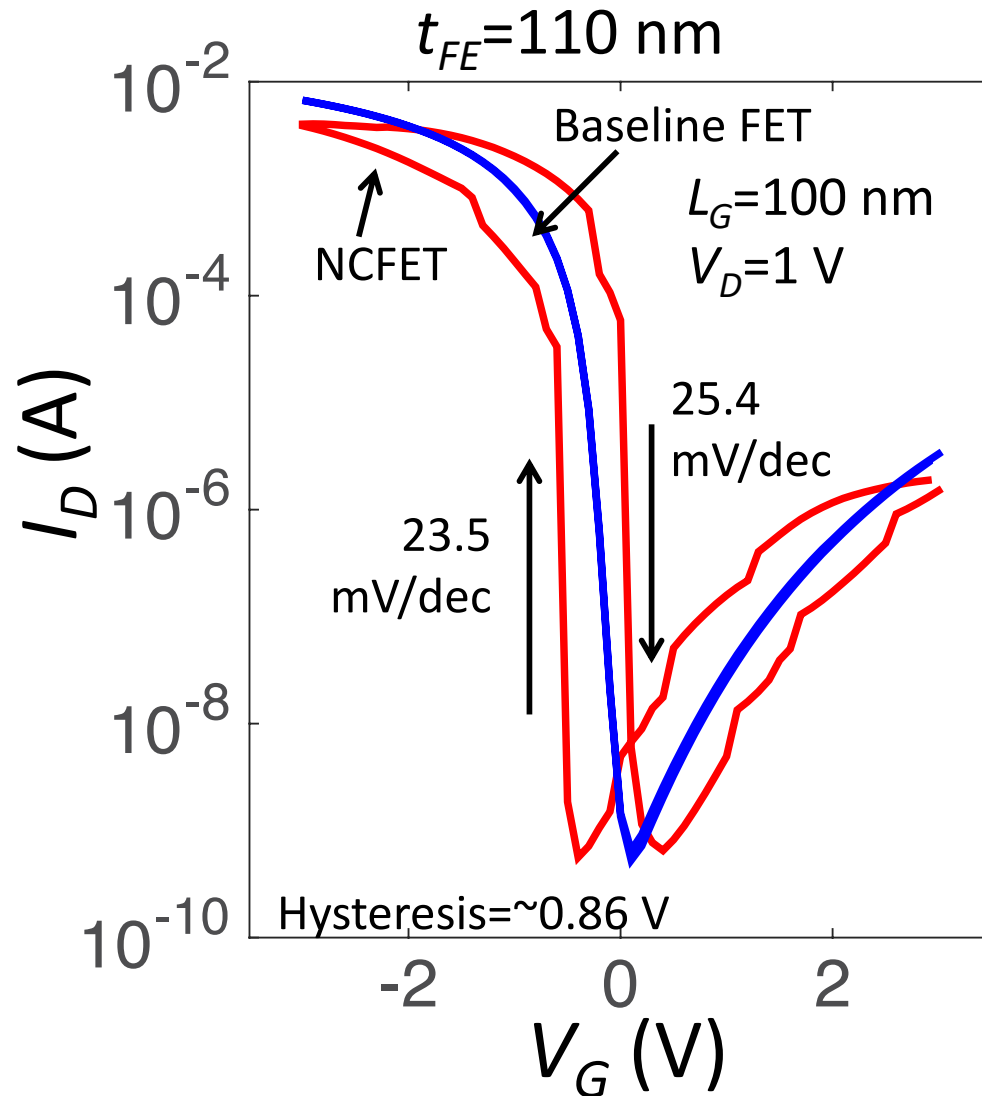


Sharp switching occurs
due to ferroelectric
negative capacitance!



Negative Capacitance
Regions: PQ and RS

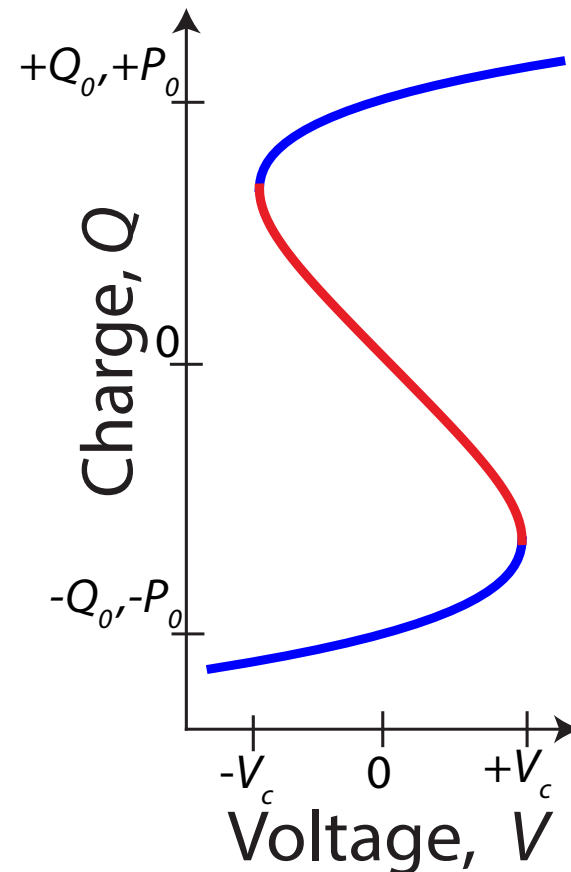
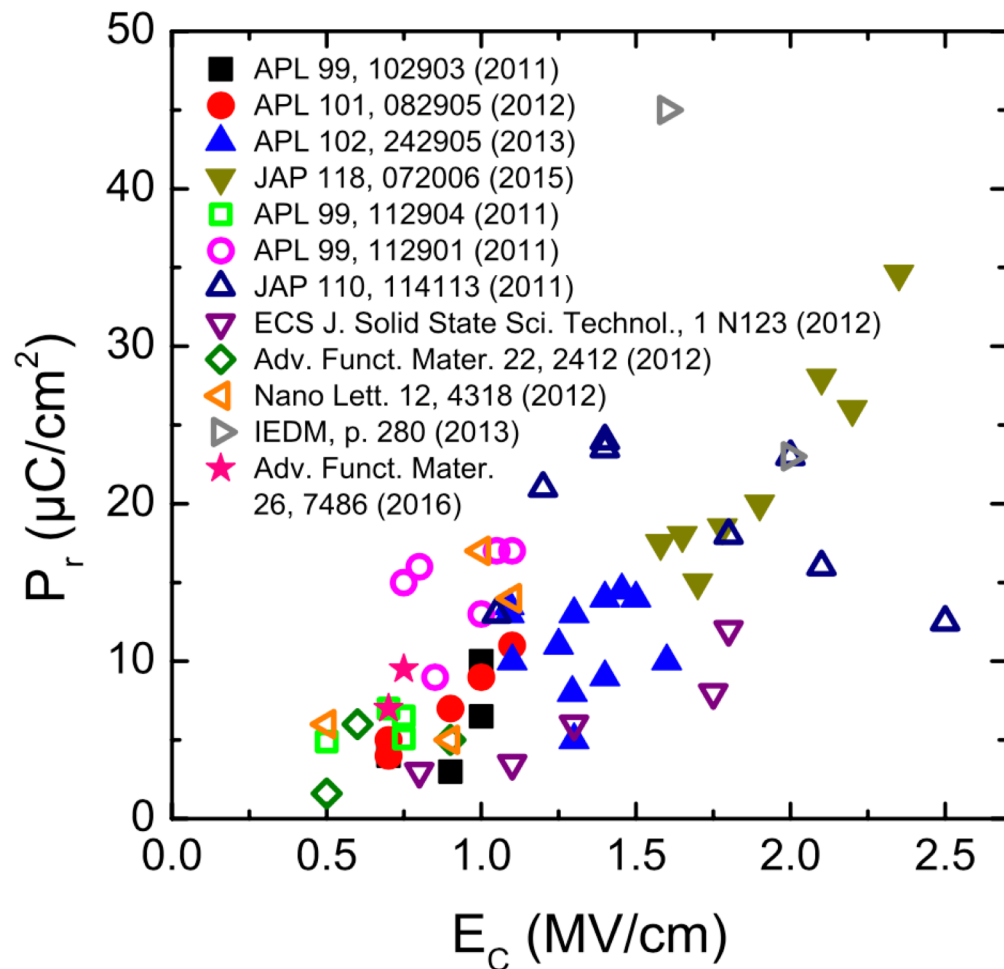
Externally Connected NC-FET



Khan, Jo et al.
(unpublished)

Negative capacitance can reduce subthreshold swing below 60 mV/dec!

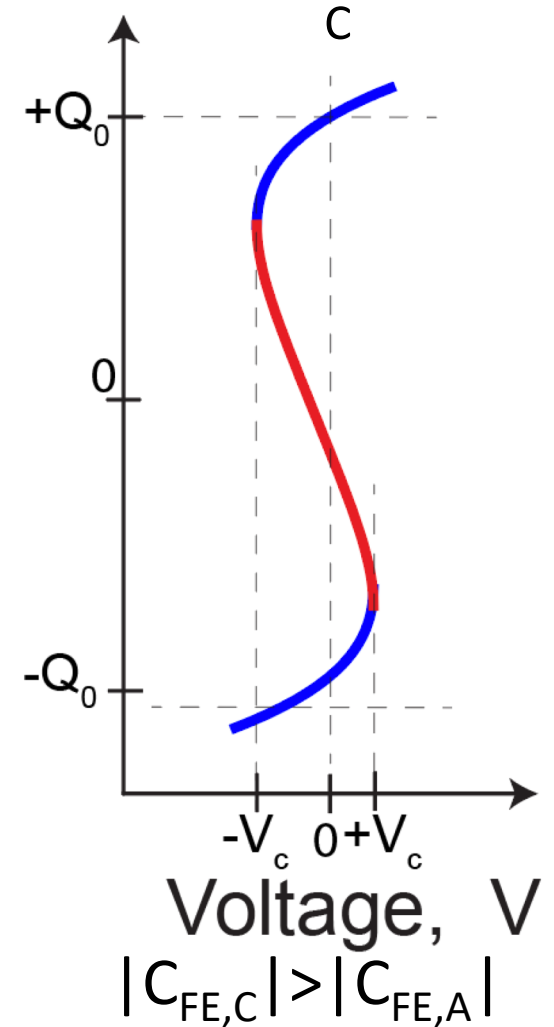
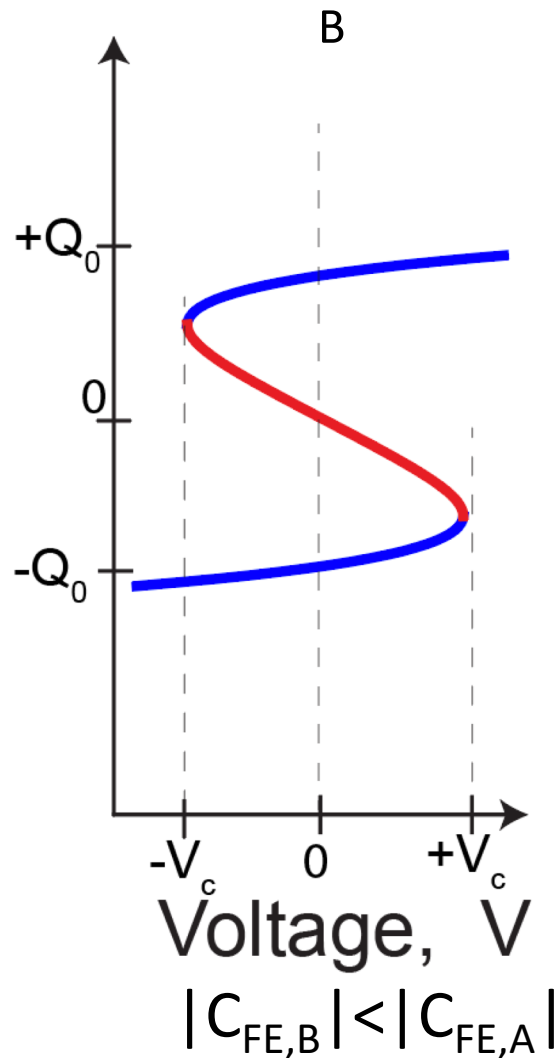
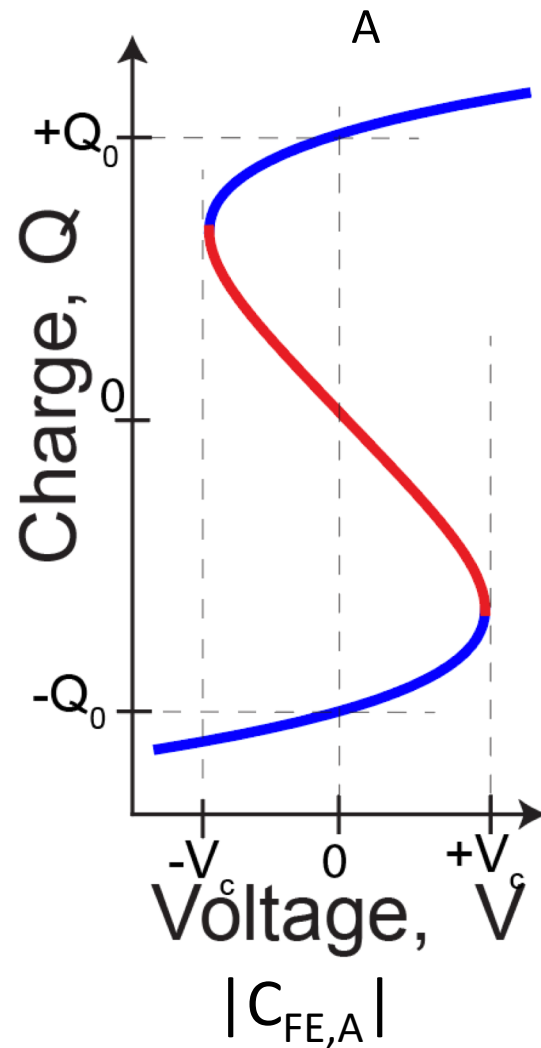
Ferroelectric Negative Capacitance



$$C_{FE} = \frac{dQ}{dV} \approx -\frac{Q_0}{V_c}$$

There are plenty of materials to try out!

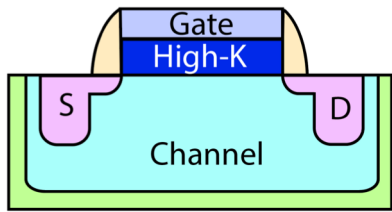
Ferroelectric Negative Capacitance



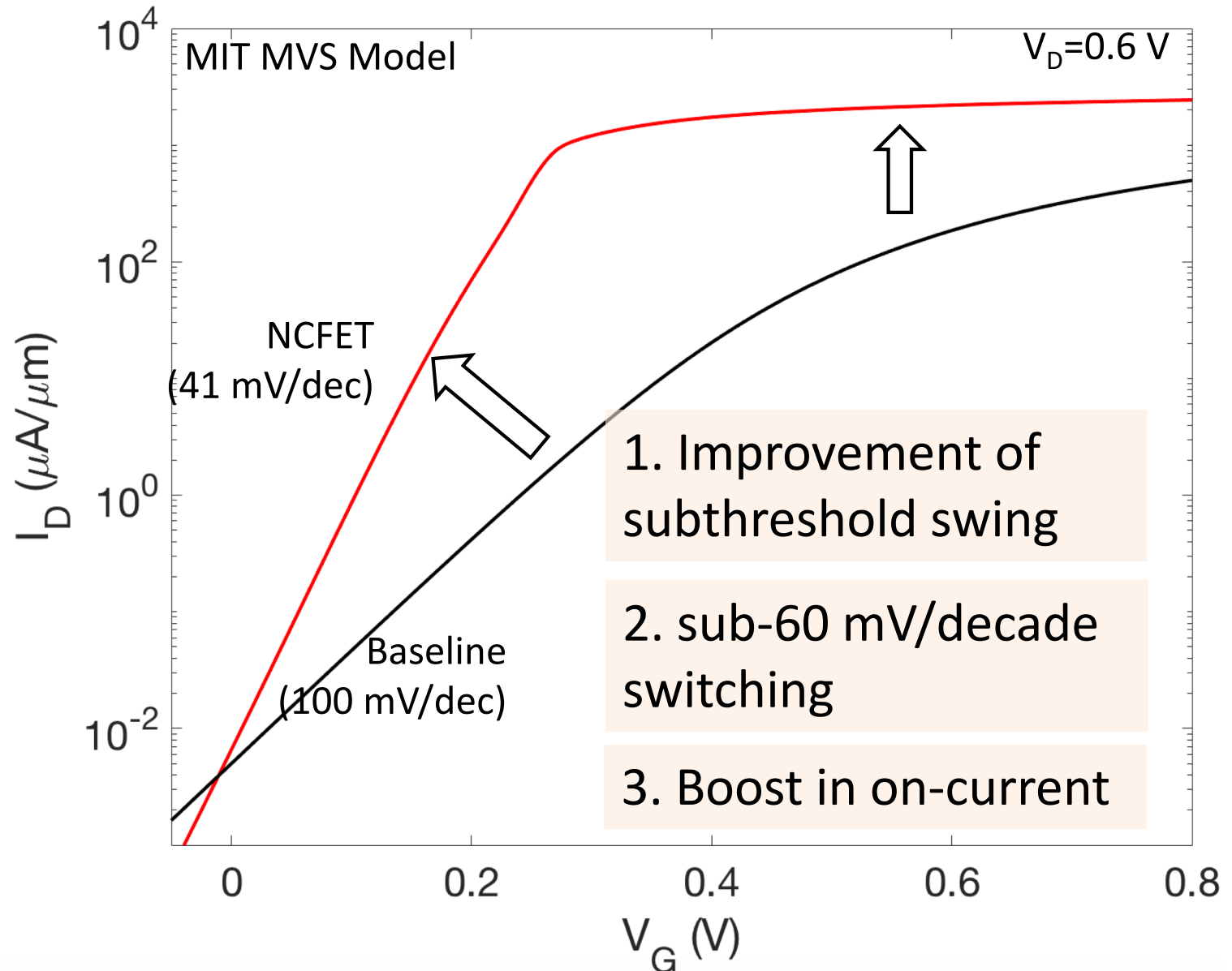
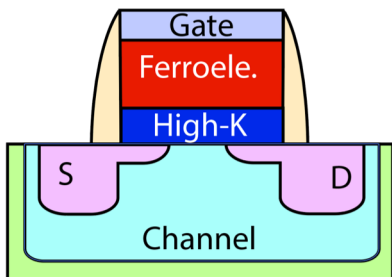
$$C_{FE} = \frac{dQ}{dV} \approx -\frac{Q_0}{V_c}$$

NCFET Expectation

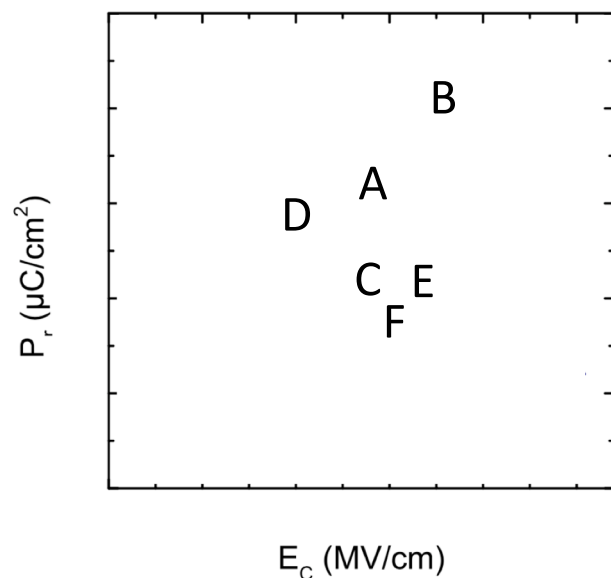
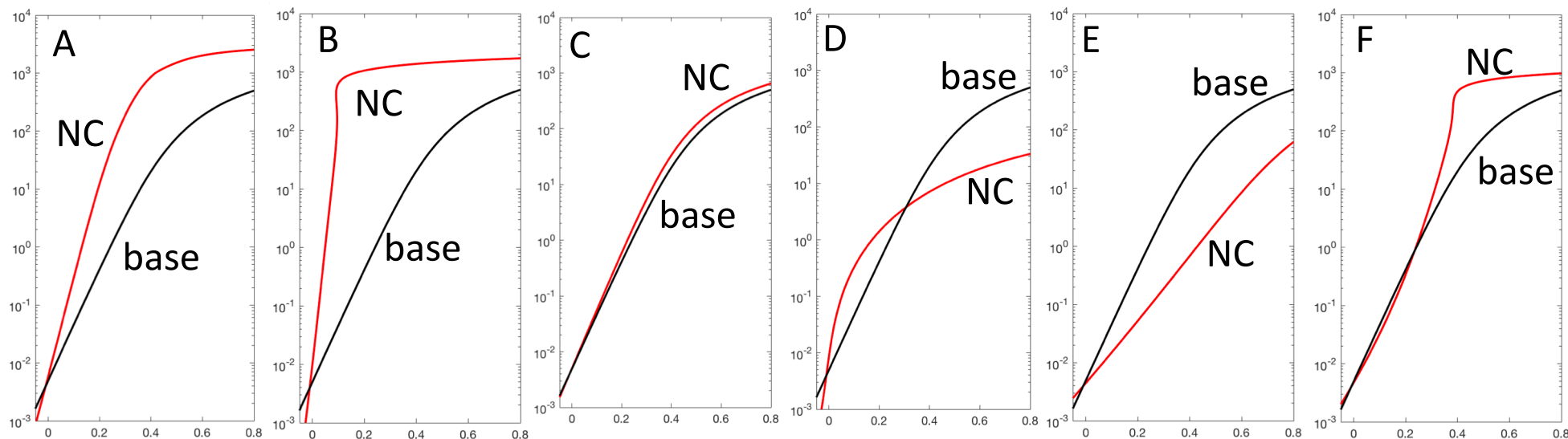
Baseline FET
(Intel 45 nm)



NCFET
(Baseline+FE)



Zoo of NCFET behavior (from best to worst)



A: SS ↓ ↓ (<60 mV/dec) $I_{on} ↑ ↑$

B: SS ↓ ↓ (<<60 mV/dec), $I_{on} ↑ ↑ ↑$

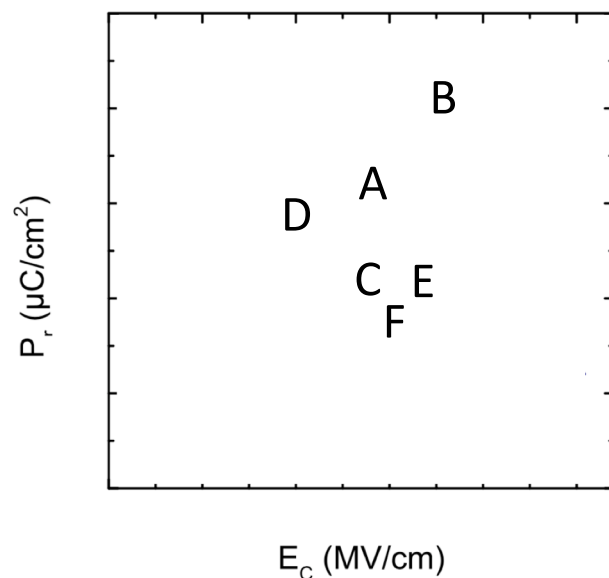
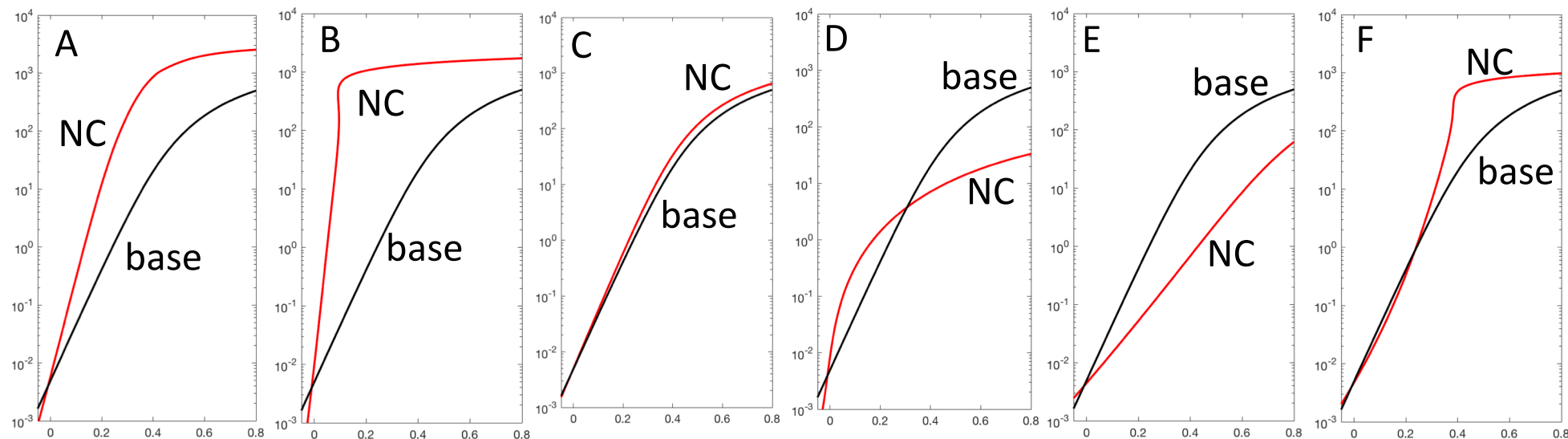
C: SS ↓ (~60 mV/dec) $I_{on} ↑$

D: SS ↓ ↓ (<<60 mV/dec) $I_{on} ↓$

E: SS ↑ ↑ (>>60 mV/dec) $I_{on} ↓ ↓$

F: SS ↑ (>60 mV/dec) $I_{on} ↑ ↑$

Zoo of NCFET behavior (from best to worst)



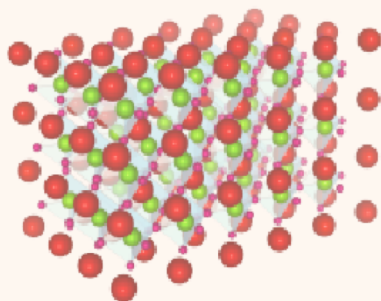
If designed properly, great performance can be obtained!

Otherwise, very poor performance can also be obtained from NCFETs!

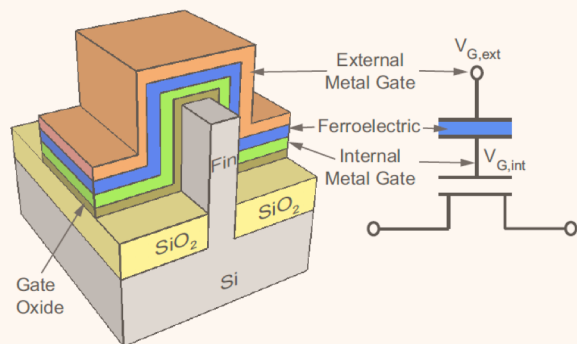
Experiments need to go hand-in-hand with simulations and also structural characterization!

What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors

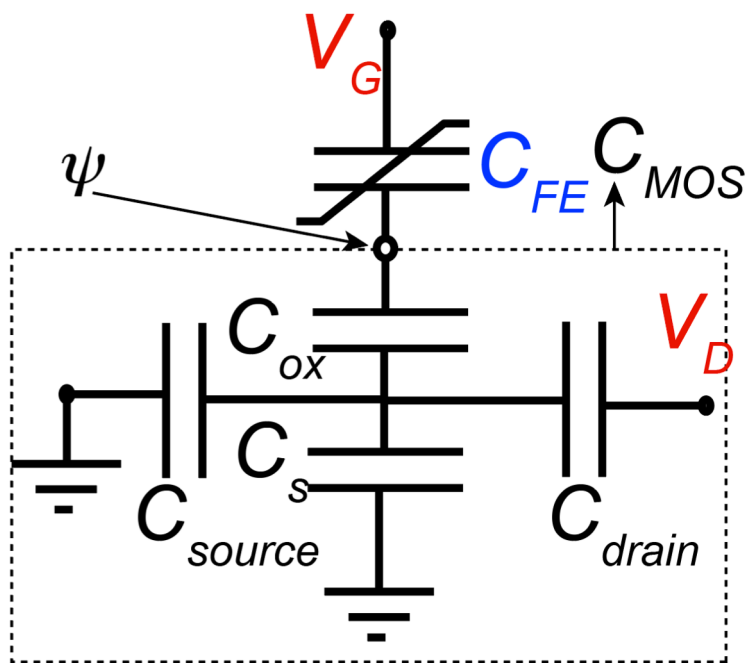


What do we need to know?

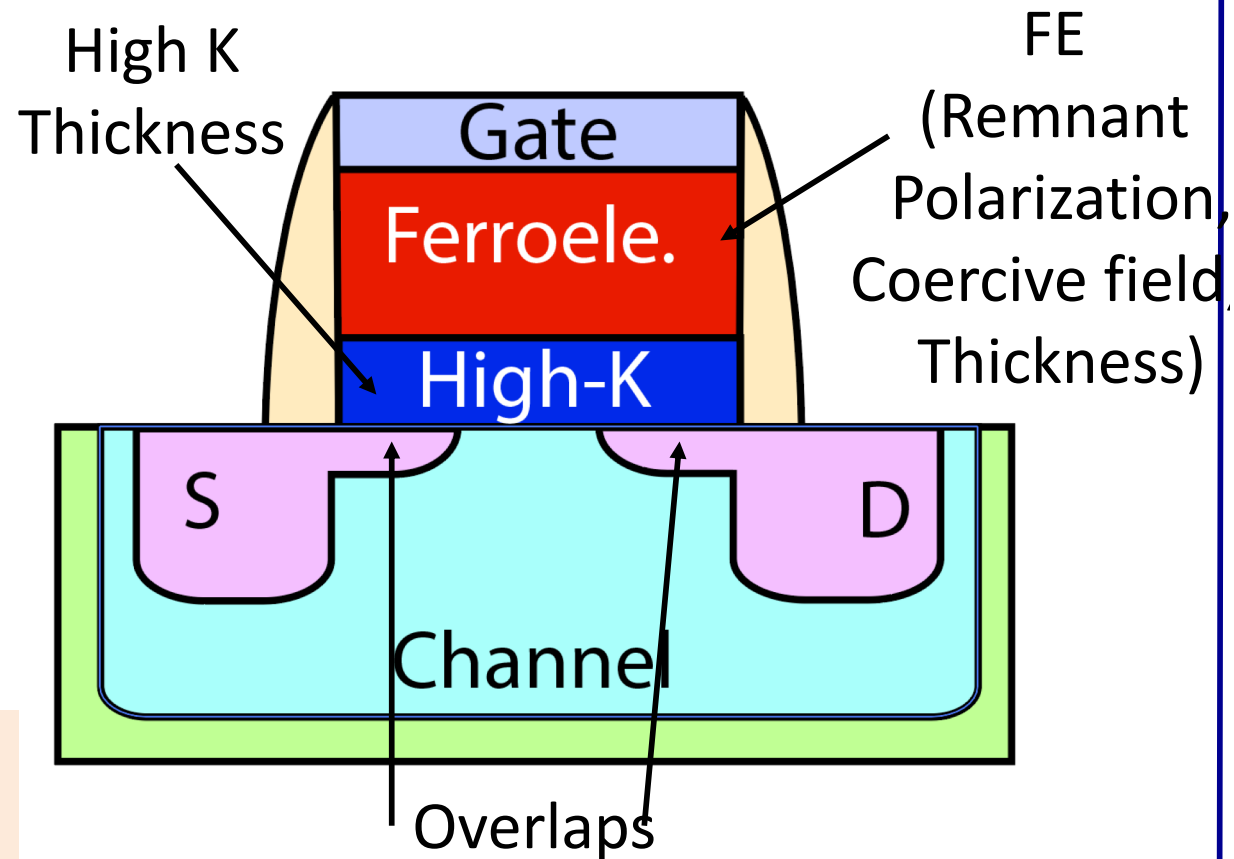


Design of NCFETs

How to design an NCFET?
~0 mV/decade swing?



Ideal Switch: ~0 mV/decade
 $|C_{FE}| \approx C_{MOS}, |C_{FE}| > C_{MOS}$



Khan et al. IEDM 2011

Yeung, Khan et al. VLSI-TSA 2013

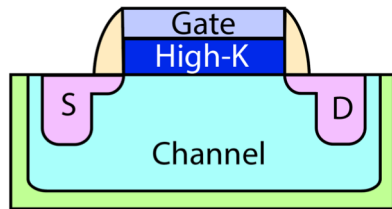
Hu, Khan et al. DRC 2015

Cheng-I, Khan et al. IEEE T-ED 2016

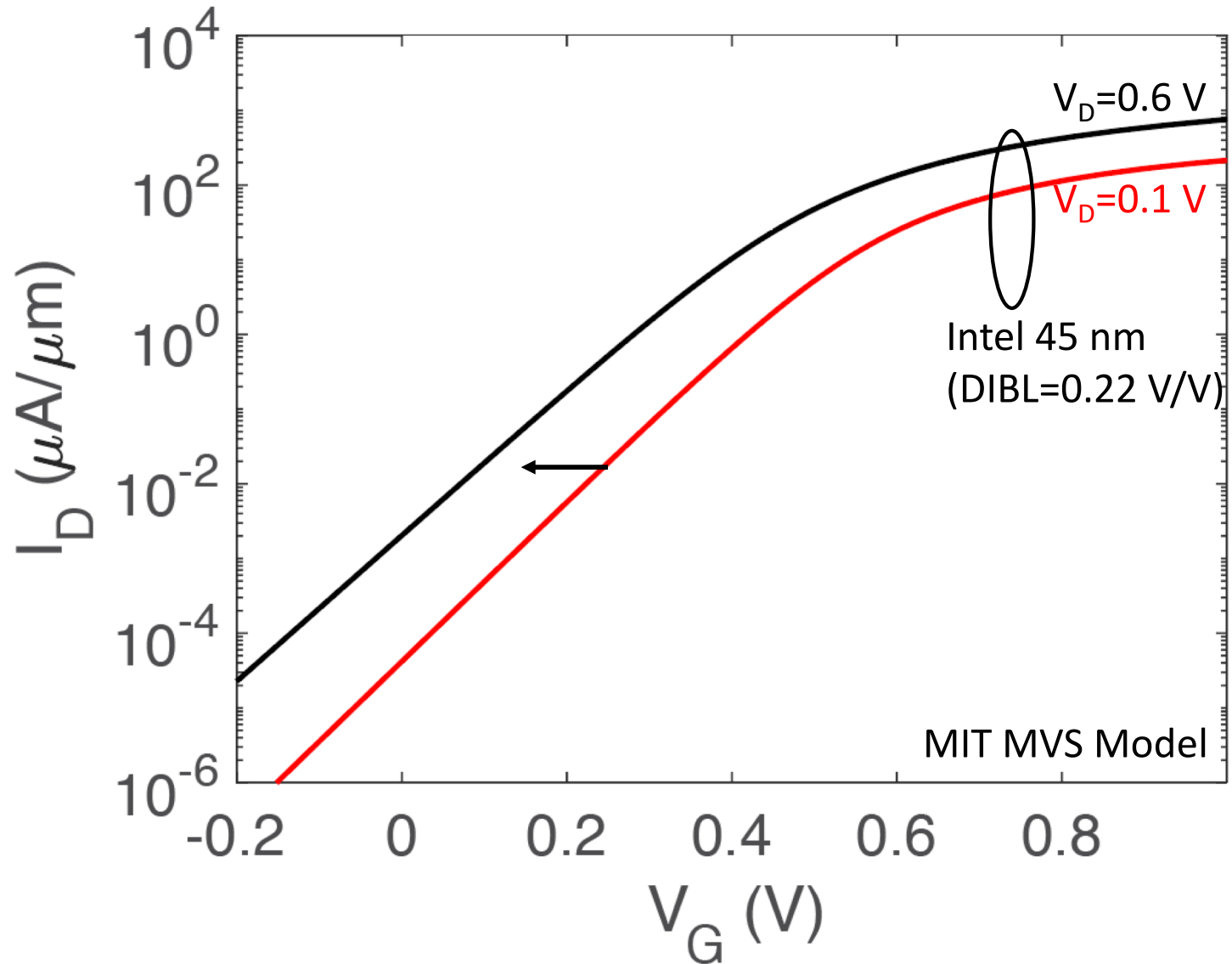
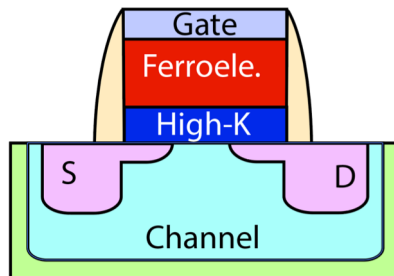
Subthreshold
Swing $S^{NC} = S^{original} \times (1 - \frac{C_{MOS}}{|C_{FE}|})$

Reverse DIBL in NCFETs

Baseline FET
(Intel 45 nm)

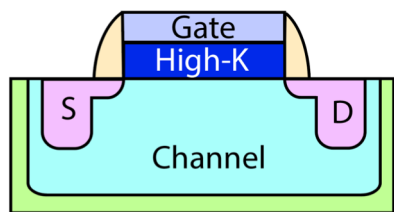


Baseline FET
(Intel 45 nm
+9 nm FE)

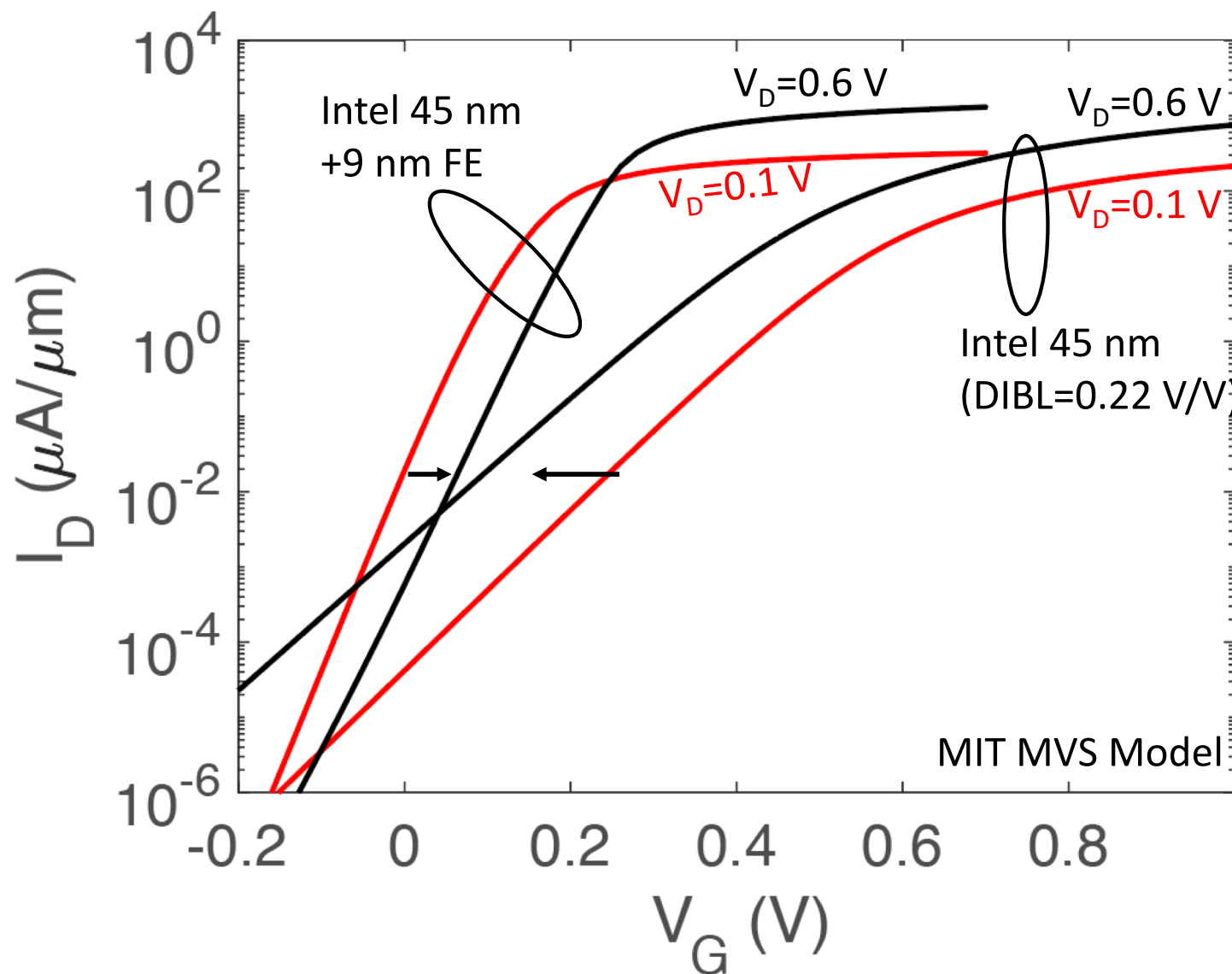
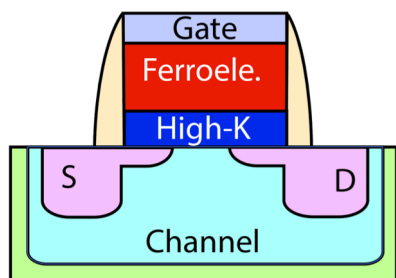


Reverse DIBL in NCFETs

Baseline FET
(Intel 45 nm)



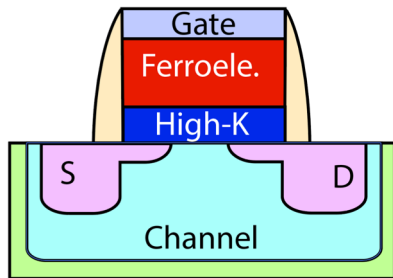
Baseline FET
(Intel 45 nm
+9 nm FE)



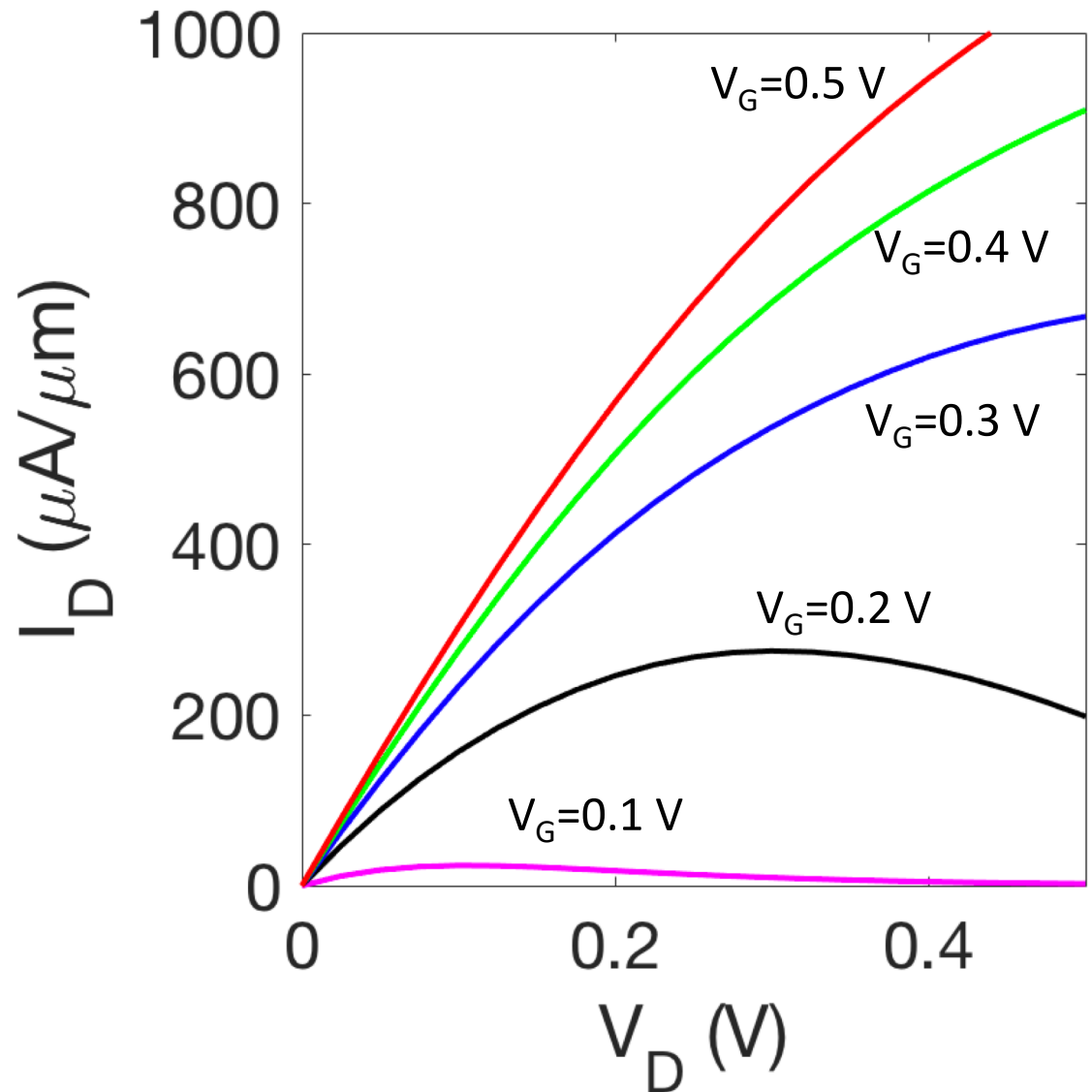
NCFET might show reverse DIBL effects!

Reverse DIBL in NCFETs: NDR

Baseline FET
(Intel 45 nm
+9 nm FE)

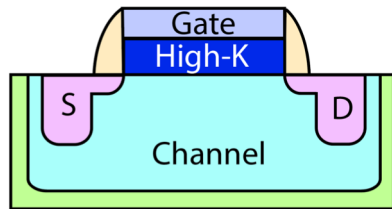


Reverse DIBL
effects may lead to
Output Negative
Differential
Resistance (NDR)

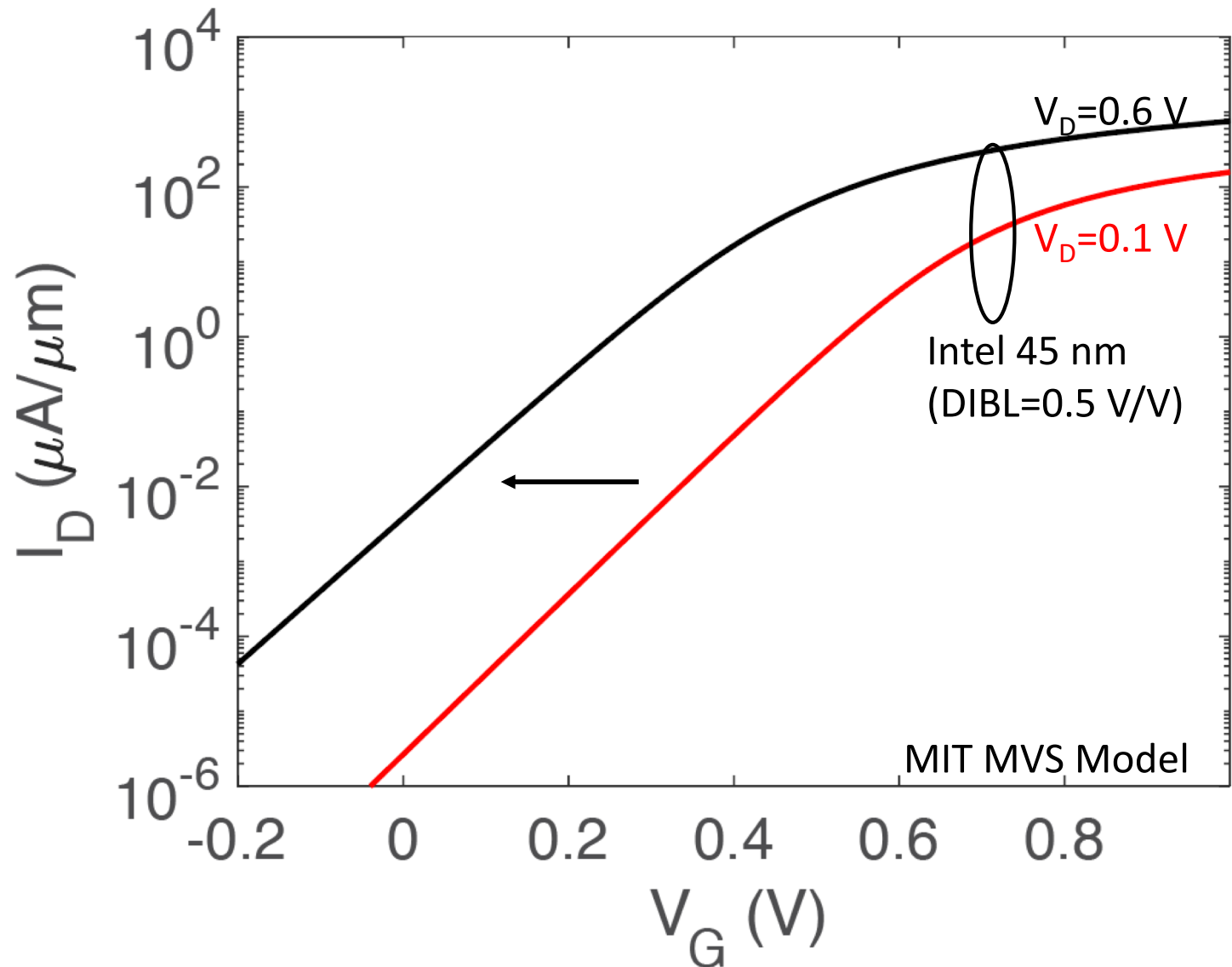
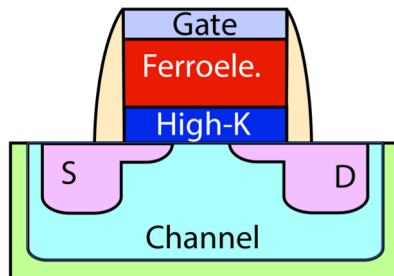


Reverse DIBL in NCFETs

Baseline FET
(Intel 45 nm)

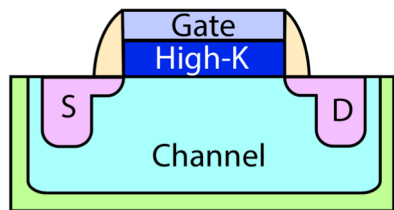


Baseline FET
(Intel 45 nm
+9 nm FE)

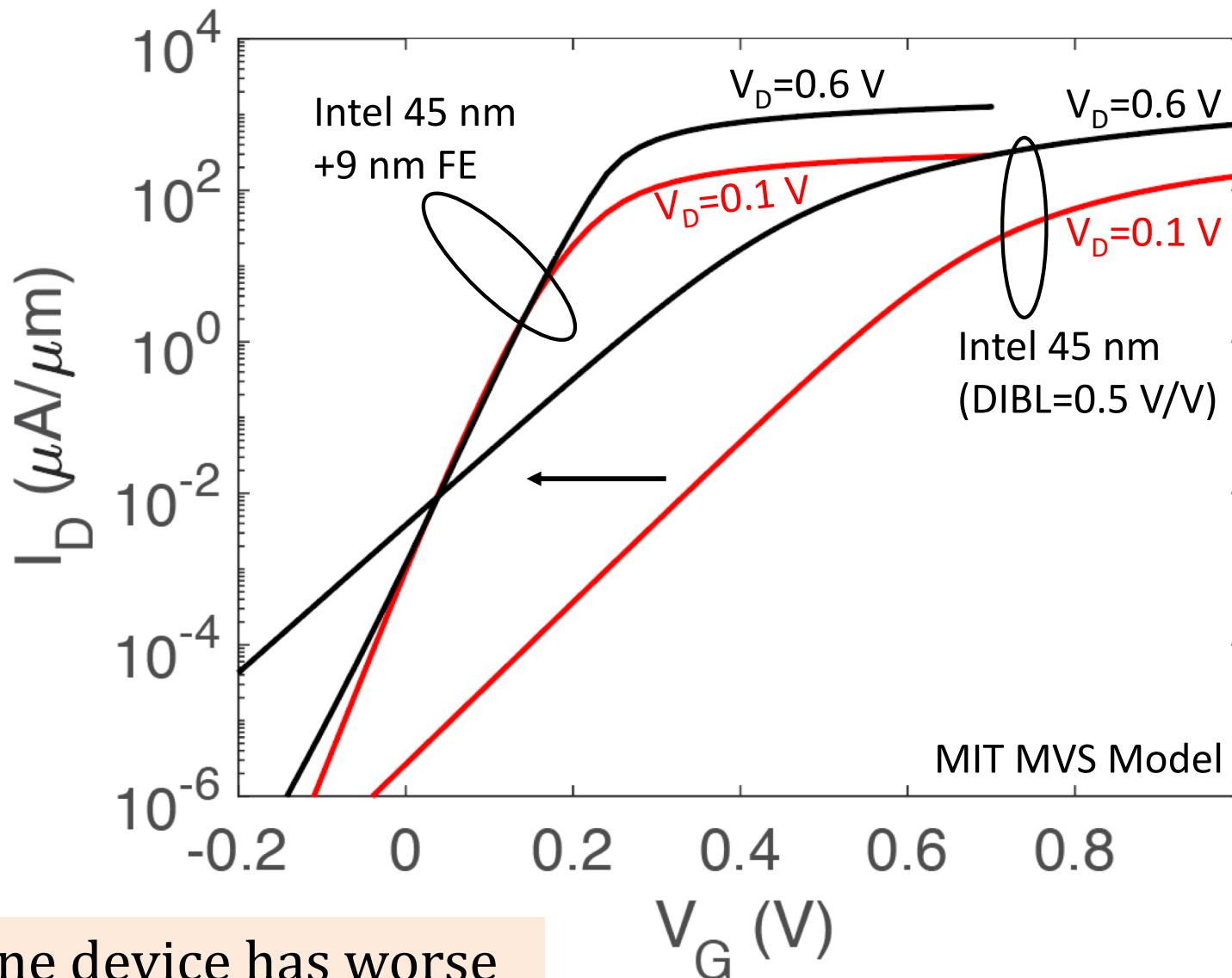
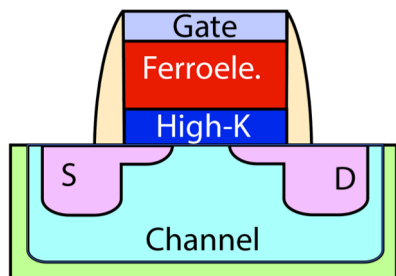


Reverse DIBL in NCFETs

Baseline FET
(Intel 45 nm)

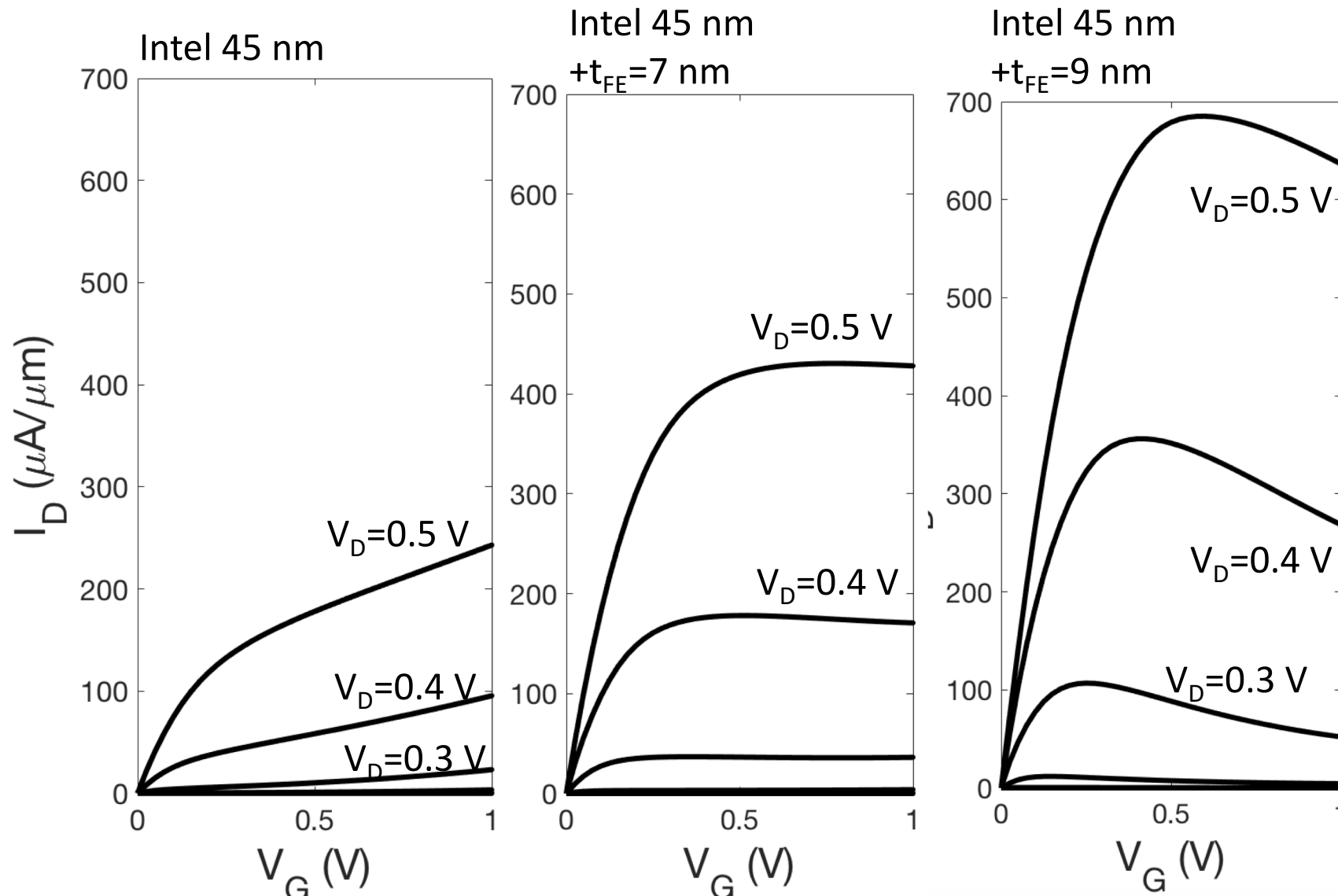


Baseline FET
(Intel 45 nm
+9 nm FE)



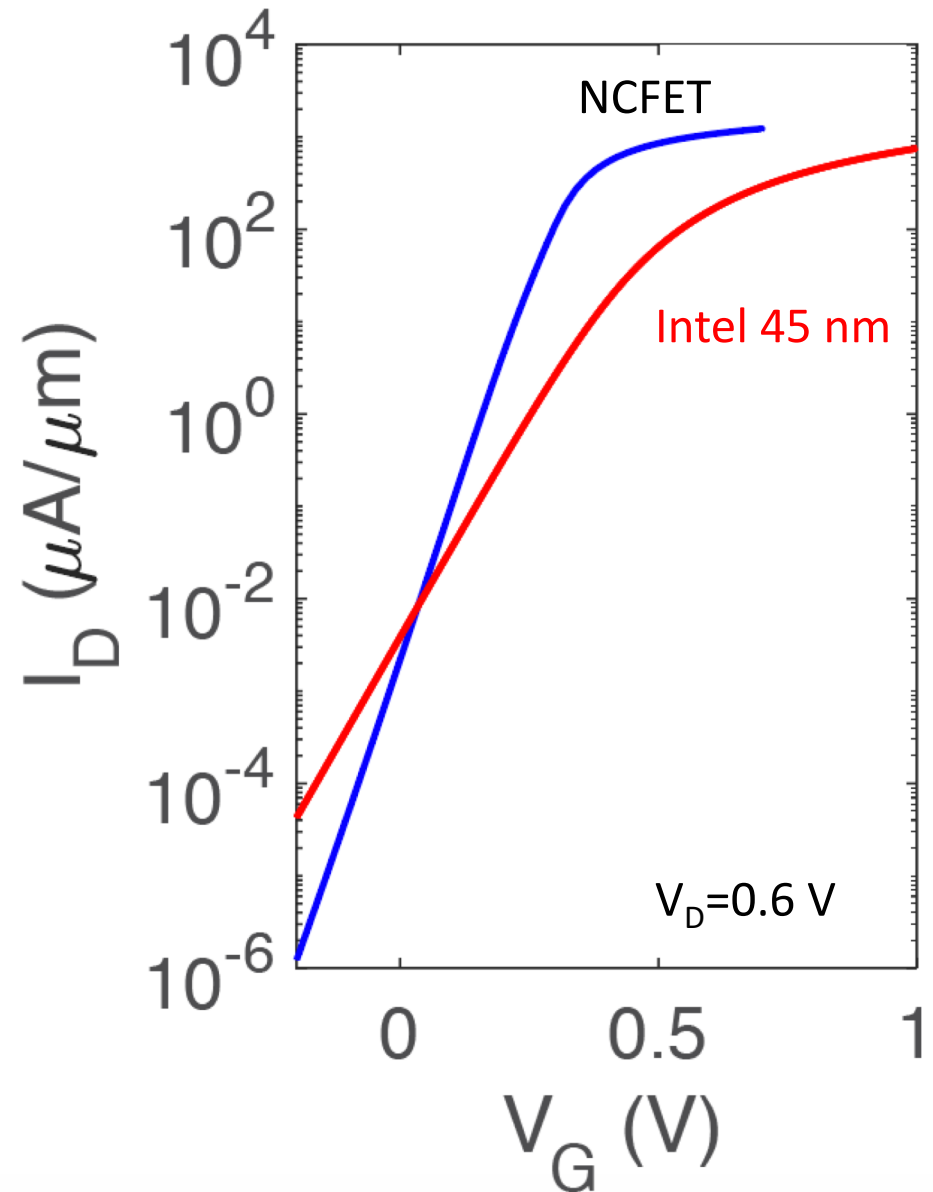
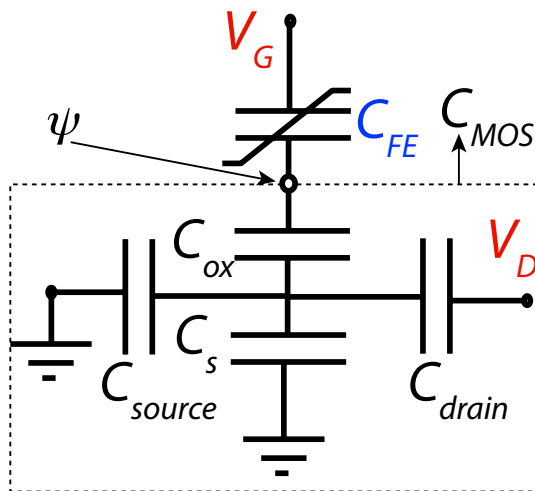
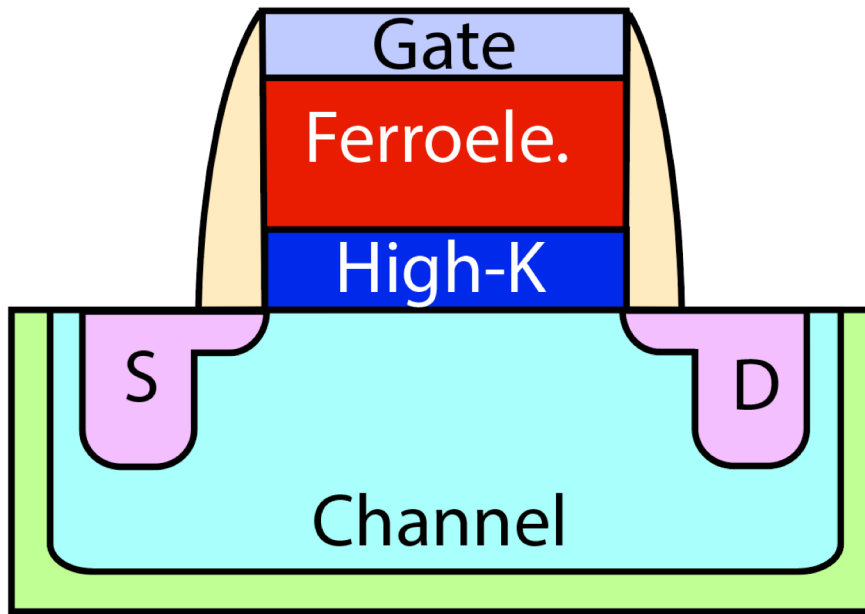
If the baseline device has worse DIBL, it is beneficial for NCFET!

Engineering DIBL in NCFETs

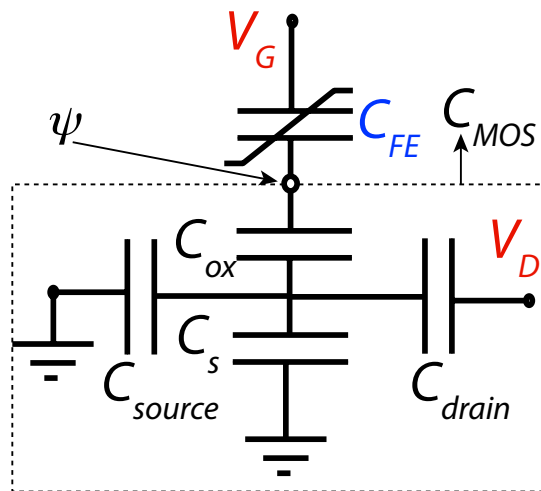
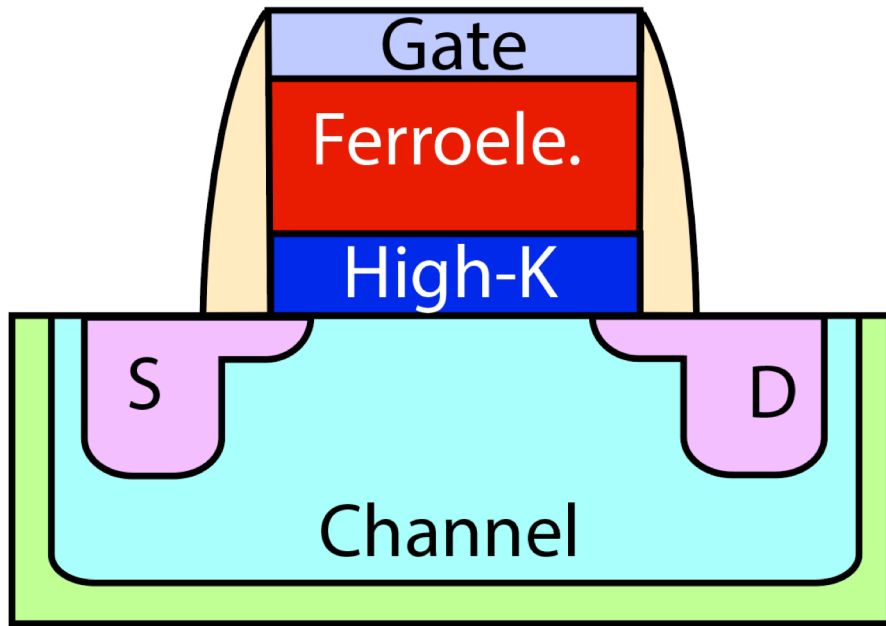


Well designed NCFET can show flat I_D - V_D saturation!
Great for Analog applications!

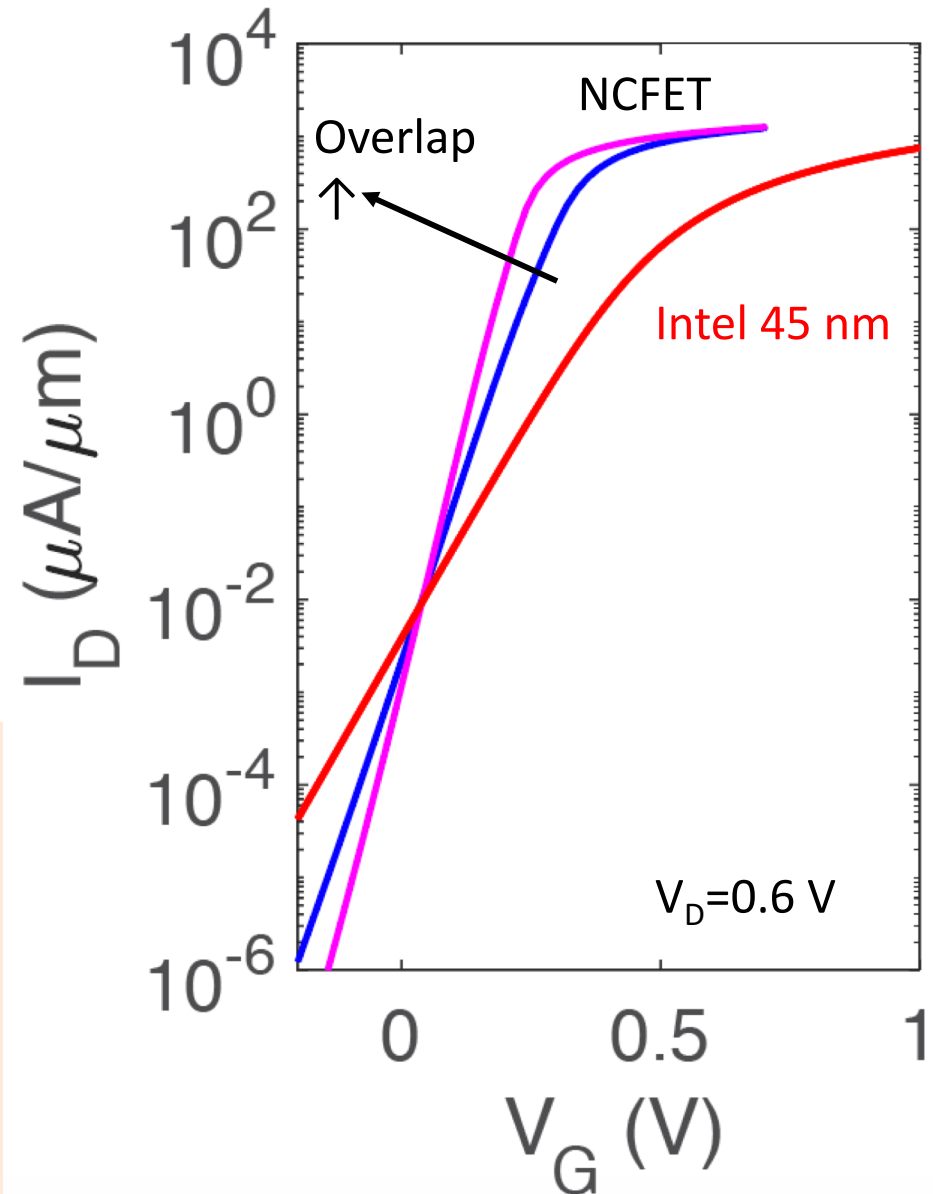
Overlap Capacitance



Overlap Capacitance

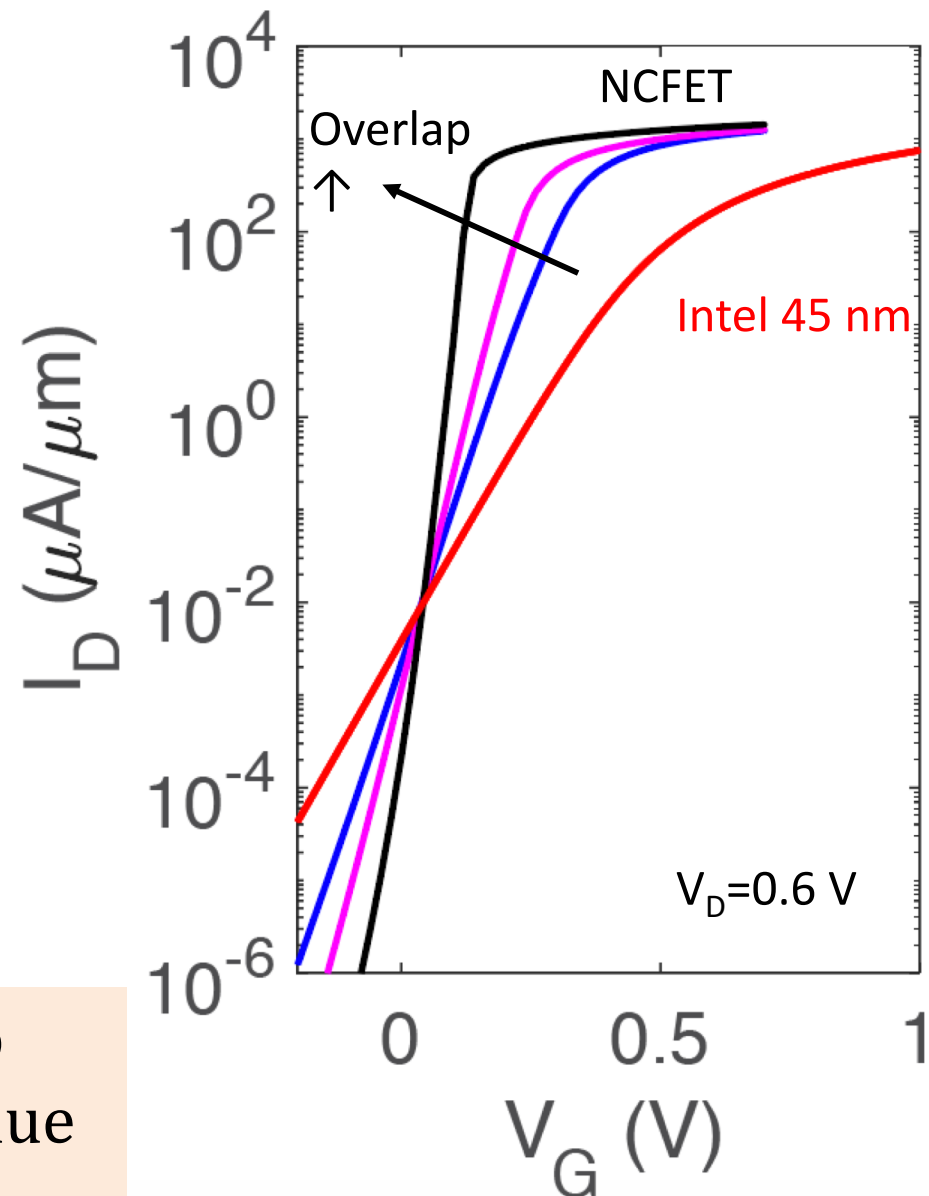
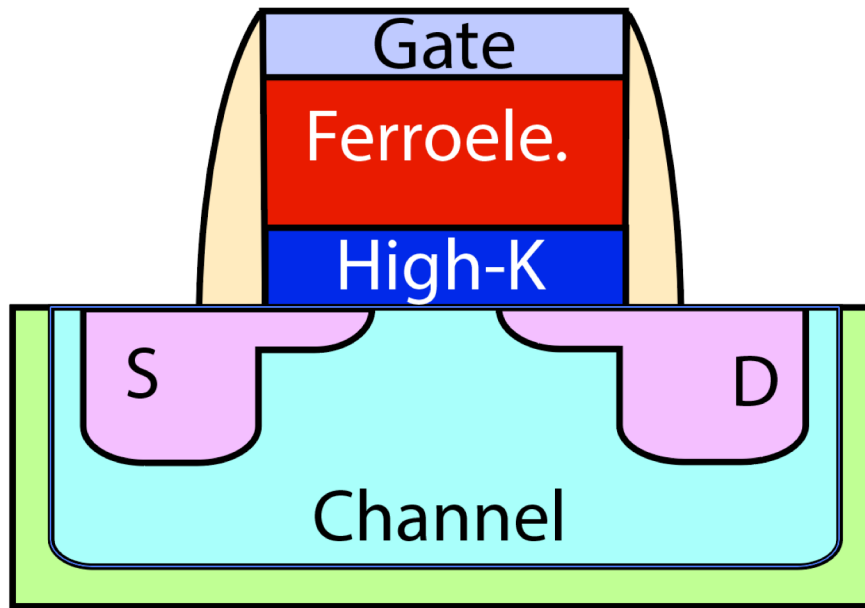


C_{drain}
increases!
 C_{MOS}
comes
closer to
 C_{FE} !



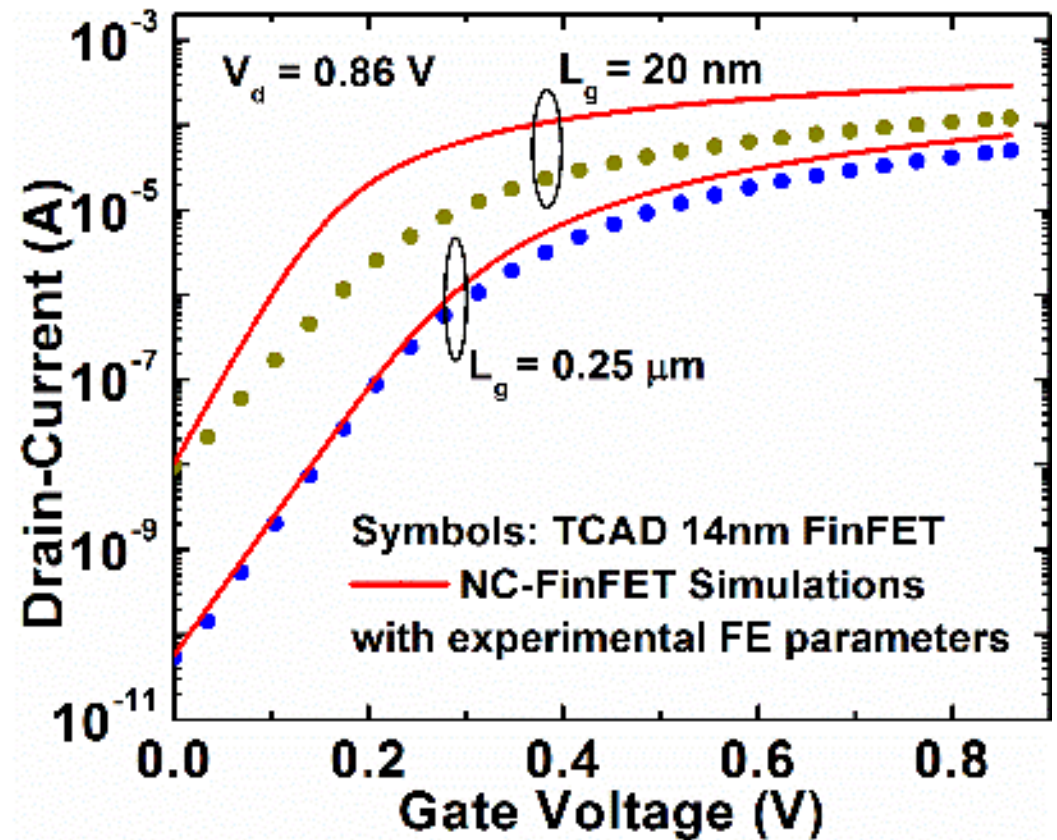
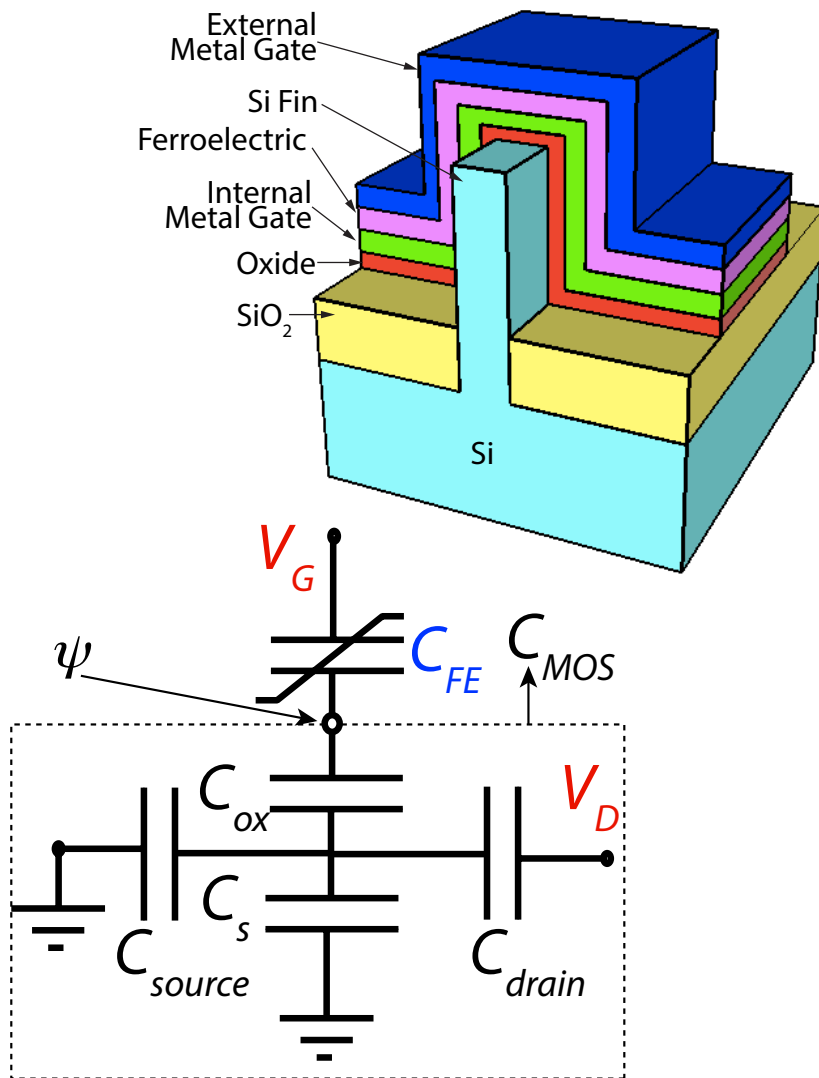
MIT MVS Model

Overlap Capacitance



Overlap capacitance helps to improve NCFET performance due to capacitance matching!

Short L_g Negative Capacitance Transistors



BSIM

Improvement of Subthreshold Swing is higher in short channel transistors!

Design of NCFETs

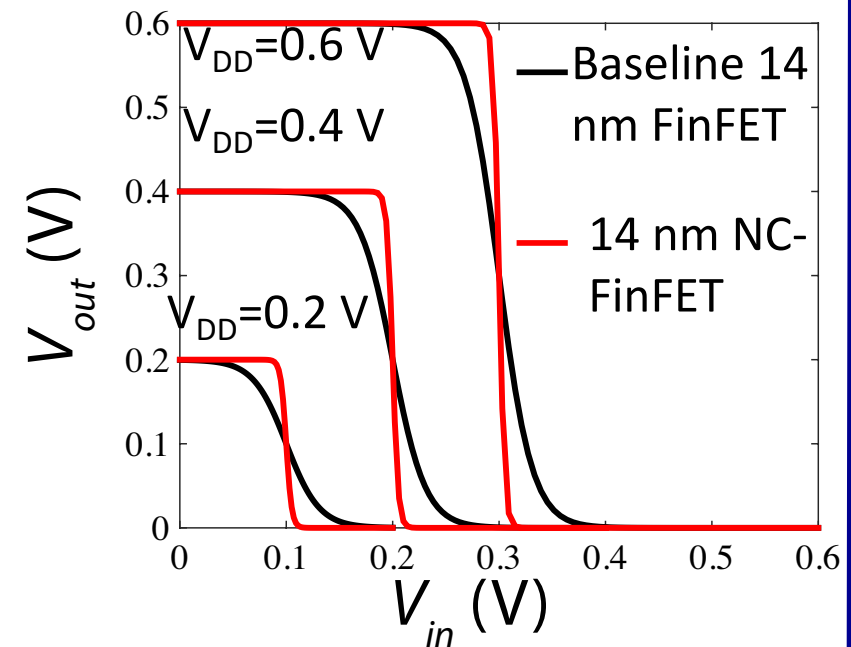
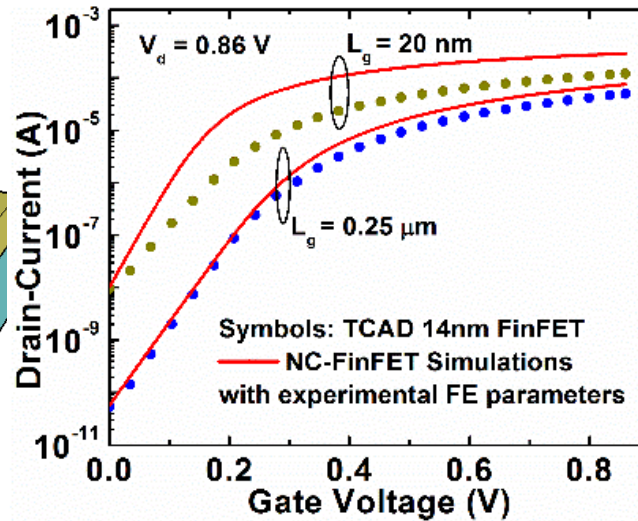
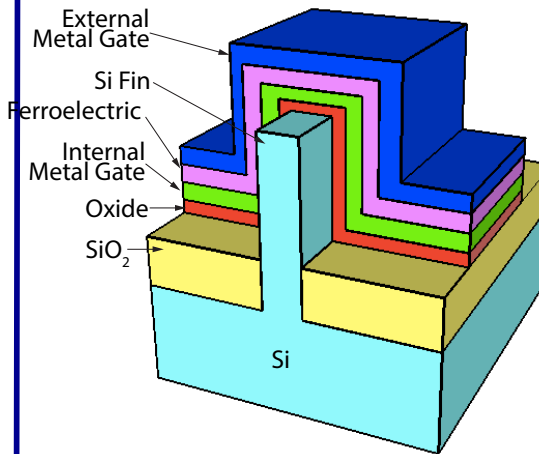
How to design an NCFET?
 ~ 0 mV/decade swing?

1. A baseline device with large DIBL can result in good DIBL characteristics of NCFETs!
2. Don't reduce high-K dielectric thickness to zero! You need it to reduce non-linearity of MOS capacitance!
3. You may see NDR in ID-VD characteristics! In short channel NCFET that will allow you to get flat saturation characteristics!
4. NCFET becomes better at short channel lengths!

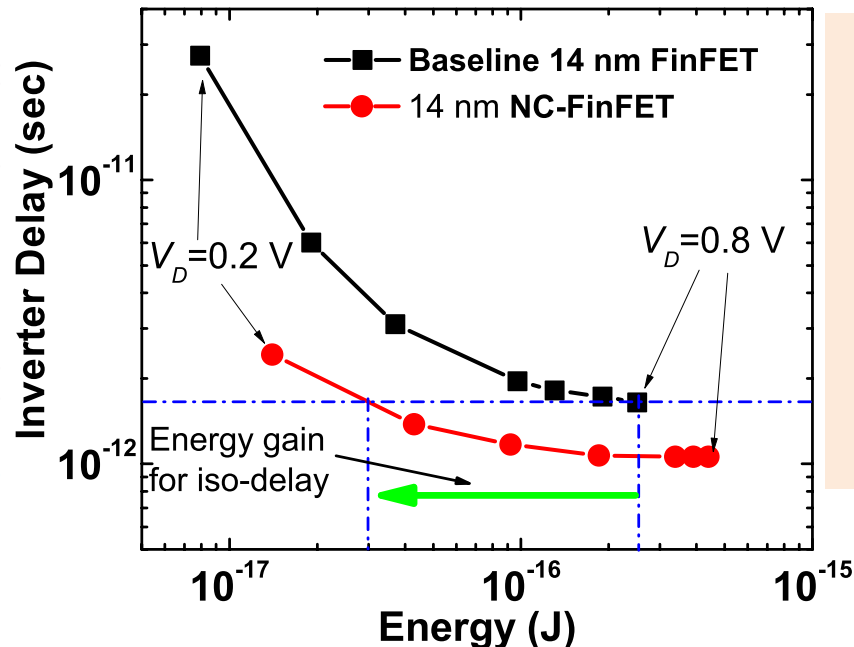
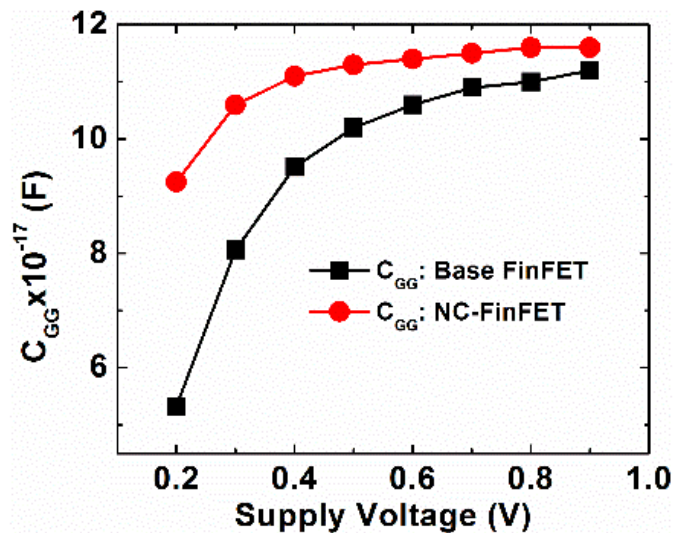
The effects that tend to degrade MOSFET performance improve the performance of NCFETs!

Performance Projection of NCFETs

14 nm NC-FinFET Model



Experiments: Li et al. IEDM 2015

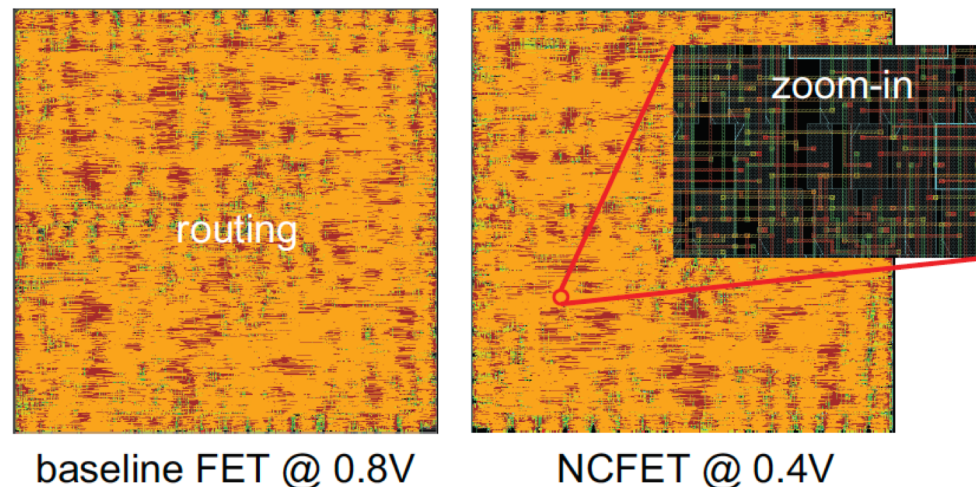


Energy
dissipation due
to
short circuit
current also
decreases!

Khandelwal VLSI Symp 2016

Full Chip Power Benefits of NCFETs

- Advanced Encryption Core (AES) Engine: ~120,000 cells, ~800,000 devices
- Iso-performance analysis (2 GHz)
- Steps:
 - 14 nm NCFET BSIM models based on experimental results (Li et al. IEDM 2015)
 - NCFET-based standard-cell library characterization
 - Full-chip NCFET-based GDSII-level design implementations



Samal, Khandelwal, Khan, Hu,
Salahuddin, Lim. ISLPED 2017

Device	VDD	# Cells	Cell Area (mm ²)	Wirelength (m)	Total Cap (pF)	WNS (ps)	Power (mW)			
							Switching	Internal	Leakage	Total
baseline FET	0.8V	127,757	0.043	1.02	686.8	6.3	57.3	91.4	6.2	154.9
NCFET	0.5V	128,438	0.043	1.03	992.3 (+44%)	19.2	33.6	40.4	0.9	74.9 (-52%)
	0.4V	135,235	0.047	1.01	933.6 (+36%)	0.9	20.1	23.9	0.9	44.9 (-71%)
	0.3V	152,328	0.053	1.02	927.4 (+35%)	-77.5	10.5	12.9	0.8	24.2 (-84%)

ISO-PERFORMANCE (2GHZ) AES DESIGNS USING NCFET AT VARIOUS VDD LEVELS.

Speed

What is the speed of negative capacitance mechanisms?

~220 ps in micron size PNZT capacitors: << Don't get confused!

Li et al. Ultrafast polarization switching in thin-film ferroelectrics. Applied Physics Letters 84, 1175 (2004).

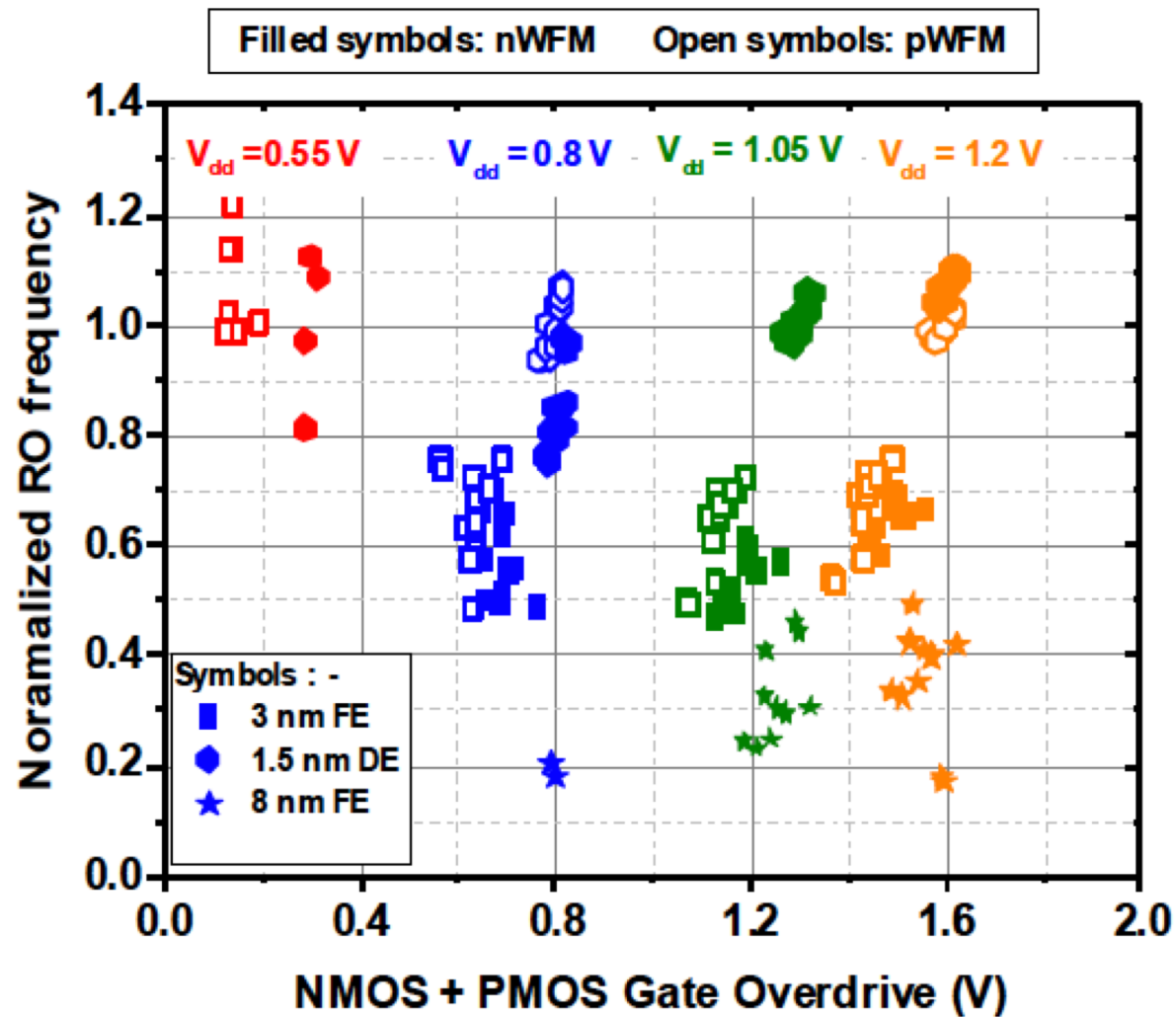
The PNZT capacitor was 5 μm x 5 μm x thickness=200 nm. Switching speed scales with area when limited by domain wall velocity.

With relevant FinFET dimensions ($<\sim 20\text{ nm} \times \sim 100\text{ nm} \times <4\text{ nm} = L_g \times (2 \times \text{fin height} + \text{fin width}) \times \text{FE thickness}$), you would get a switching speed of 16 fs.

With extracted damping and mass terms from spectroscopic measurements for HfO_2 , the characteristics time scale for ferroelectric switching in the domain nucleation limit should be around 220 fs.

Chatterjee et al. Intrinsic Speed Limit of Negative Capacitance Transistors EDL 2017 <http://ieeexplore.ieee.org/abstract/document/7990241/>.

Speed



Krivokapic et al. IEDM 2017

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Office of
Naval Research



STARNET LEAST



NSF E3S Center



FCRP MSD Center



THANKS

Negative Capacitance:

What do we know and
What do we need to know?

QUESTIONS
&
COMMENTS

