Negative Capacitance FETs: Physics, Materials and Devices

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Beyond CMOS Tutorial, ESSDERC 2017
11 September 2017, Leuven, Belgium

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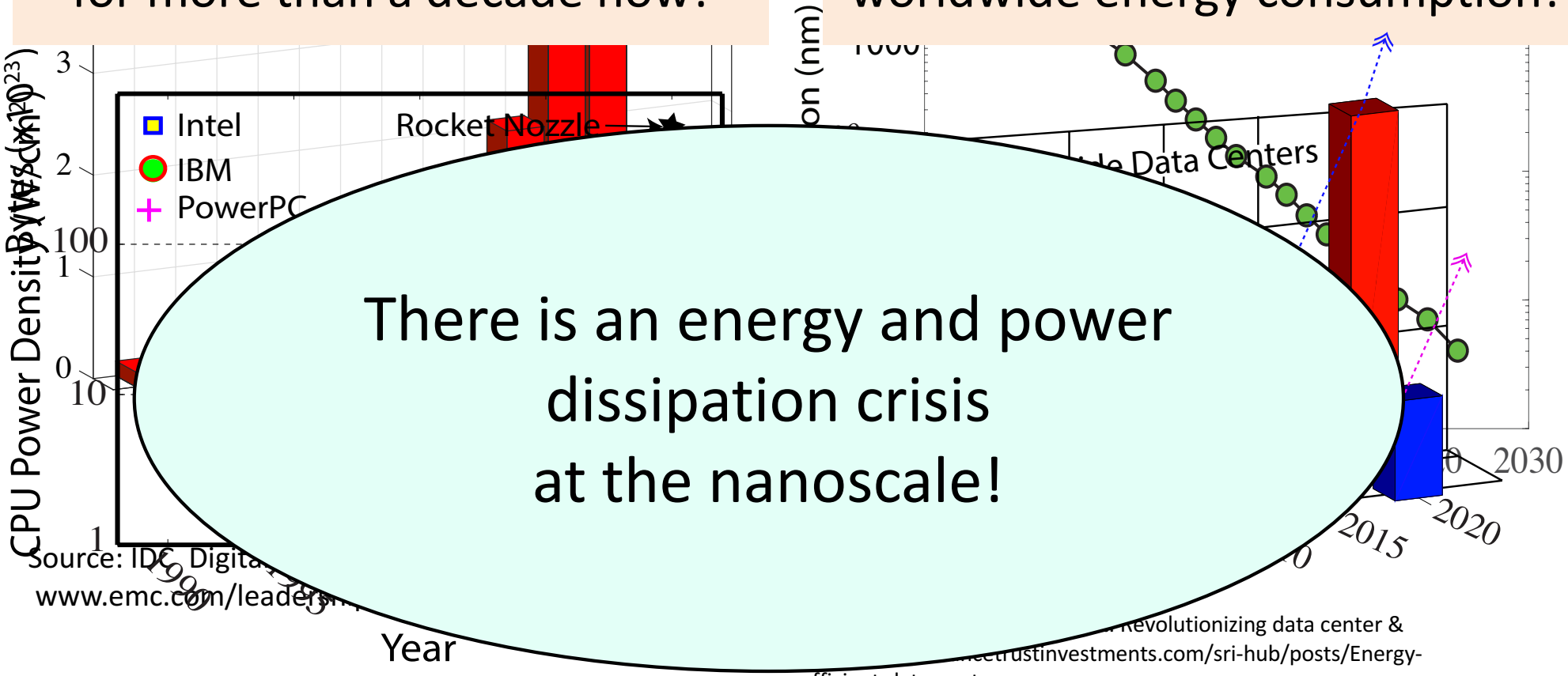
Computing and Global Challenges

Computable data grows 50x every ten year!

Extreme scaling has been the driver!

Clock frequency stuck at 3 GHz for more than a decade now!

Computing constitutes 2-5% of worldwide energy consumption!



There is an energy and power dissipation crisis at the nanoscale!

Source: IDC, Digita… www.emc.com/leader…

Adapted from: Danowitz et al. Comm. of ACM 55.1 (2012).

…Revolutionizing data center & …trustinvestments.com/sri-hub/posts/Energy-efficient-data-centres

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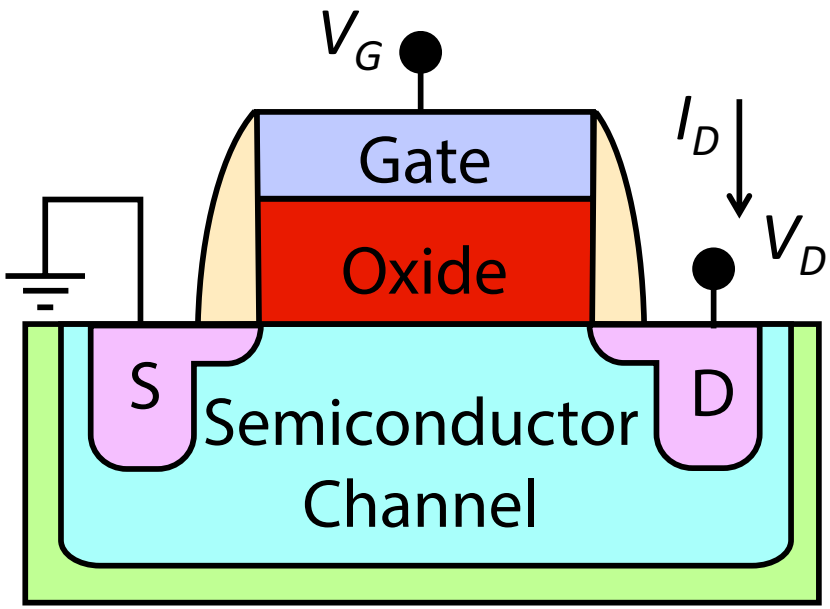
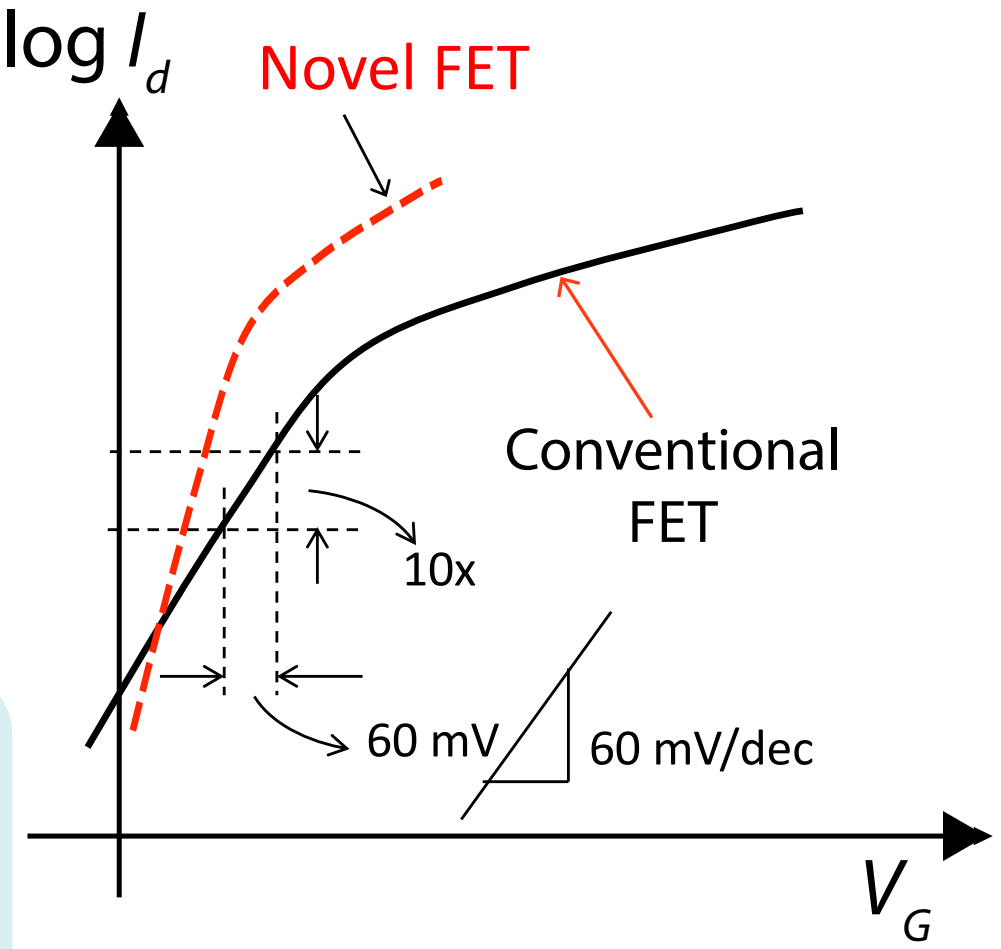
Energy Challenge in Computing





Boltzmann distribution dictates that Channel charge, $Q \alpha e^{\frac{q\psi_s}{k_B T}}$

Minimum Subthreshold Swing

$$S_{\min} = \frac{k_B T}{q}\log_e(10) = 60mV/dec$$

We are in search of an Ultra-low Power MOSFET!

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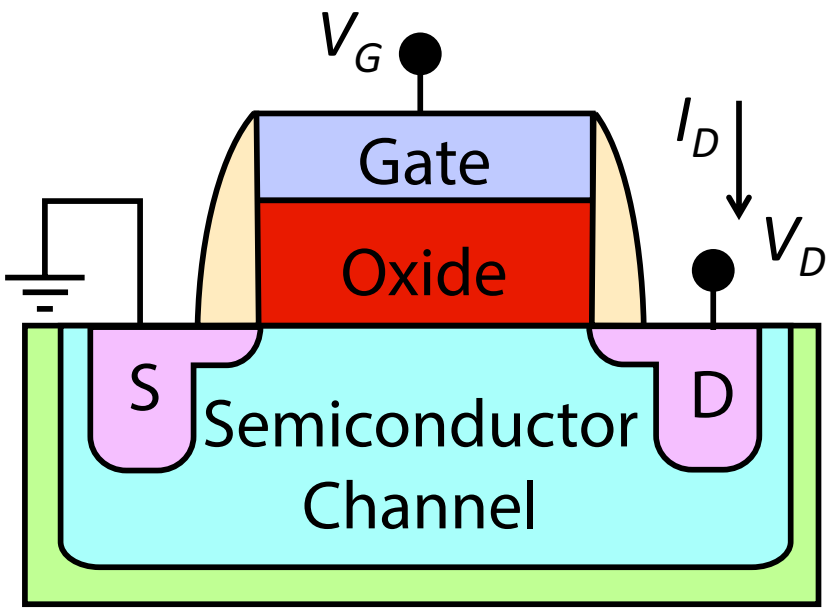
The Negative Capacitance Approach

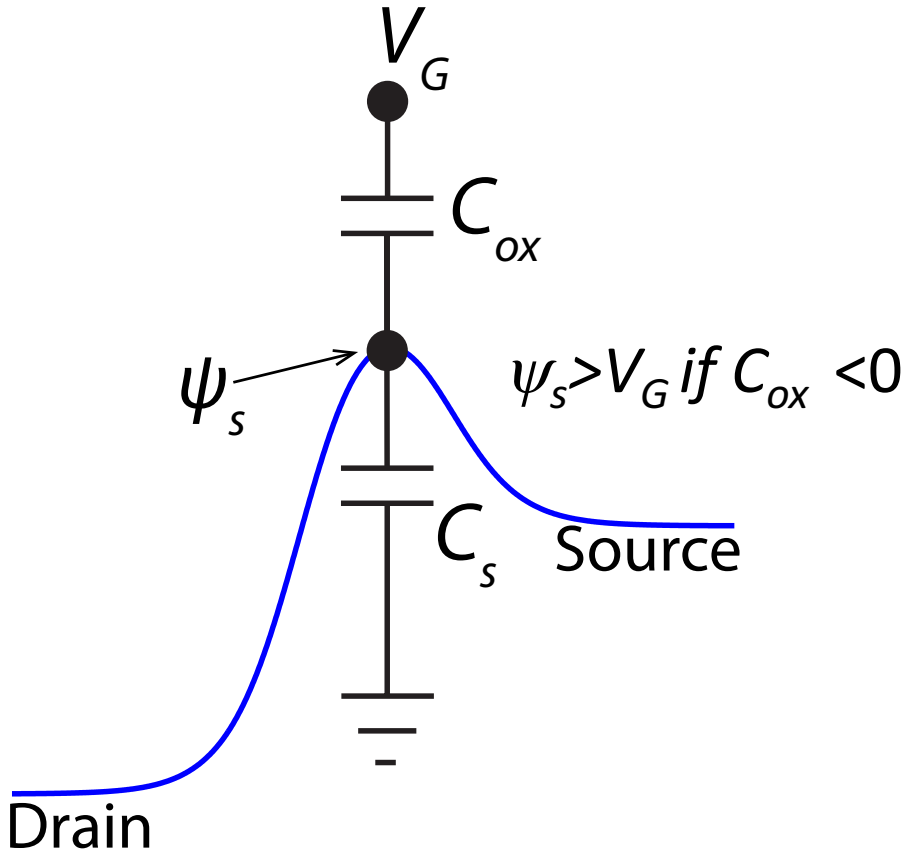


Subthreshold Swing

$$S = \frac{\partial V_G}{\partial(\log_{10} I_D)} = \frac{\partial V_G}{\underbrace{\partial \psi_s}_{\equiv m}} \frac{\partial \psi_s}{\partial(\log_{10} I_D)} = m \times 60 \text{ mV/decade}$$

Body Factor

$$m = \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_s}{C_{ox}}$$



$$m = 1 + \frac{C_s}{C_{ox}} < 1 \quad \text{if } C_{ox} \text{ is negative}$$

Negative capacitance can result in a $S < 60$ mV/decade

Salahuddin et al. Nano Lett. 8, 405 (2008)

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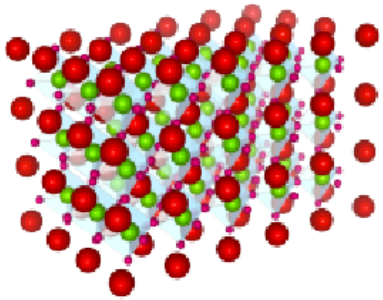
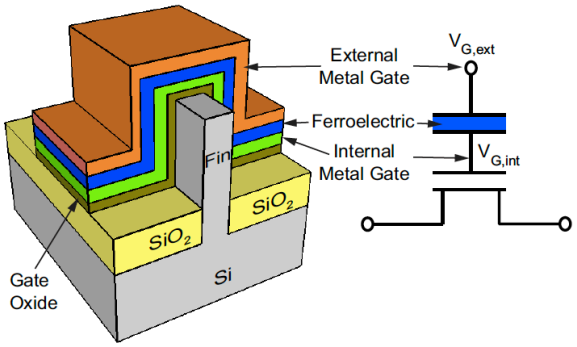
What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors



What do we need to know?

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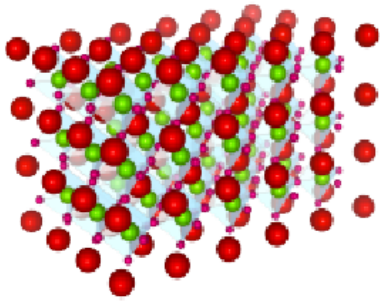
What am I going to do today?

Physics of Negative Capacitance in Materials



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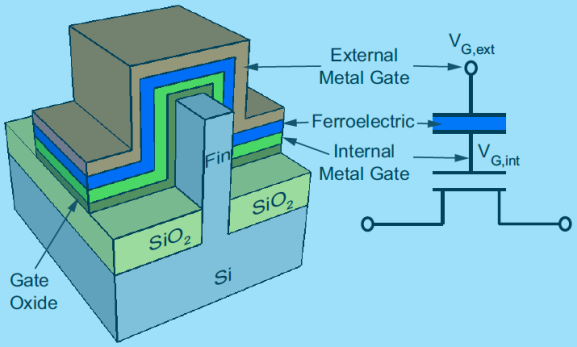

What do we need to know?

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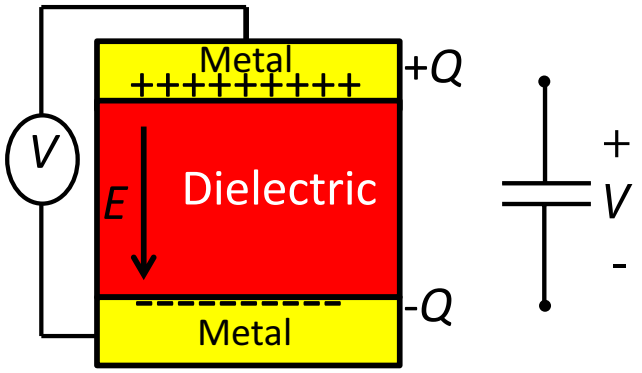
Capacitance: Positive and Negative

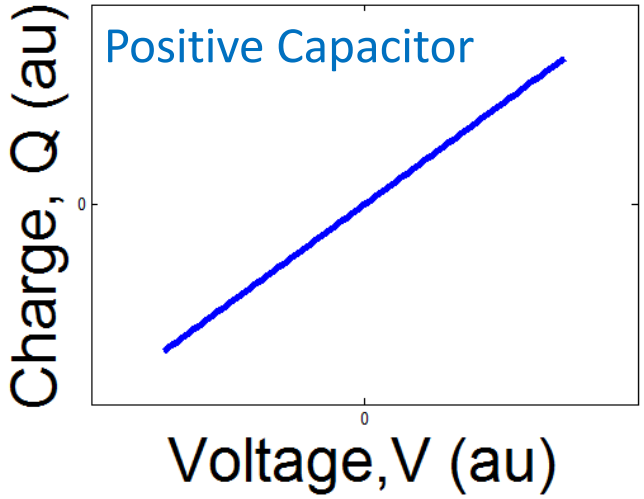


Capacitance $C = \frac{dQ}{dV}$

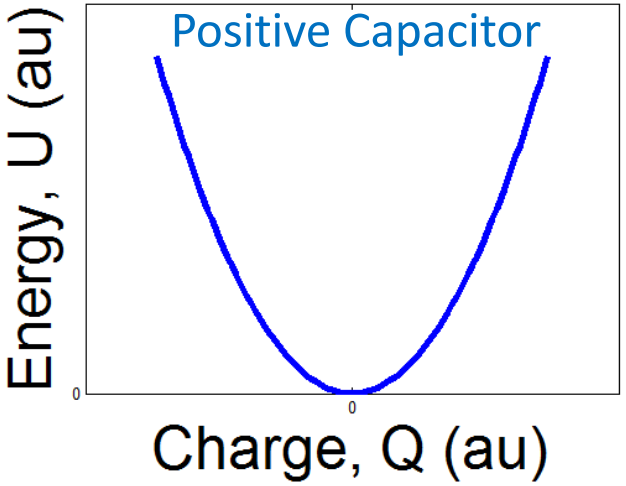
Stored Energy $U = \frac{Q^2}{2C}$

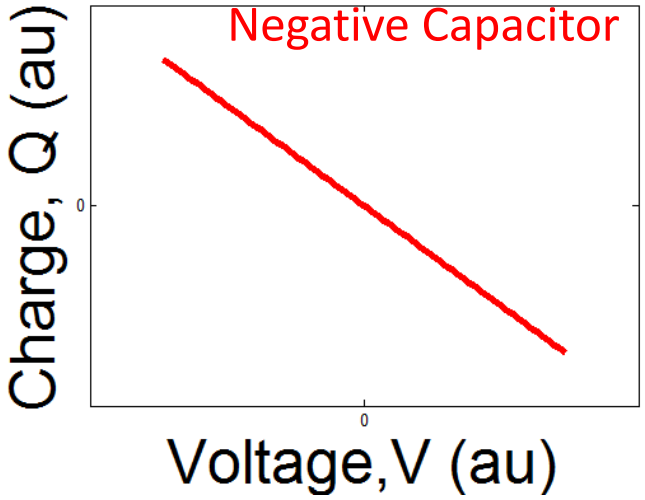
$$C = \left[\frac{d^2U}{dQ^2}\right]^{-1}$$

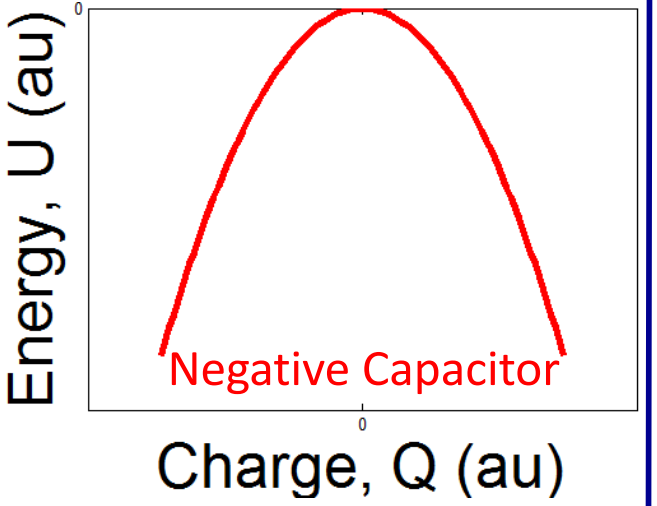
Q-V Characteristics



Q-U Characteristics (Energy Landscape)







C is inverse of radius of curvature of energy landscape

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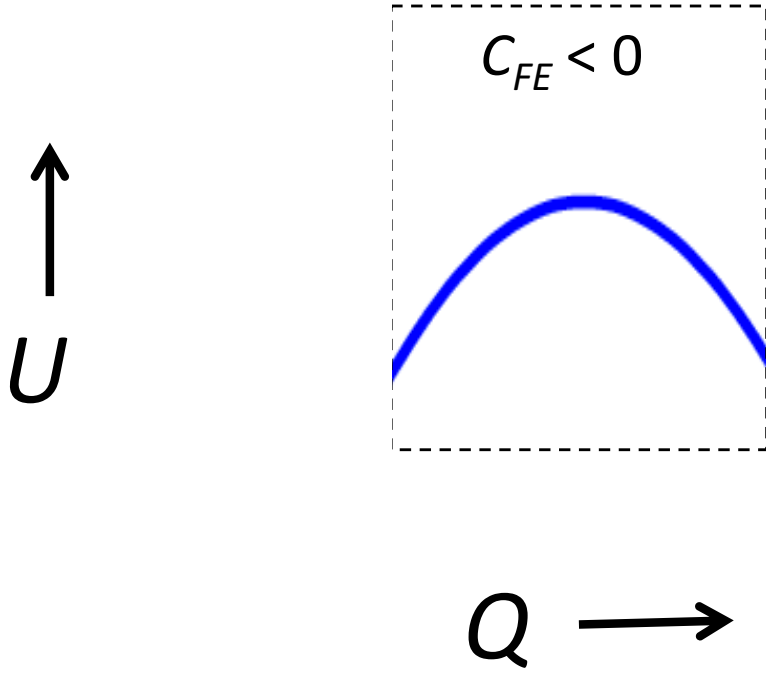
How to get Negative Capacitance Material



Landau Theory of Ferroelectrics

Free energy of a ferroelectric

$$U = \alpha Q^2 + \beta Q^4 + \gamma Q^6; \alpha < 0$$

α, β, γ = Anisotropy Constants
Q = Charge

According to the Landau theory of ferroelectric, ferroelectric oxides could give an effective negative capacitance

Landau & Khalatnikov. Dokl. Akad. Nauk 96, 85 469472 (1954).

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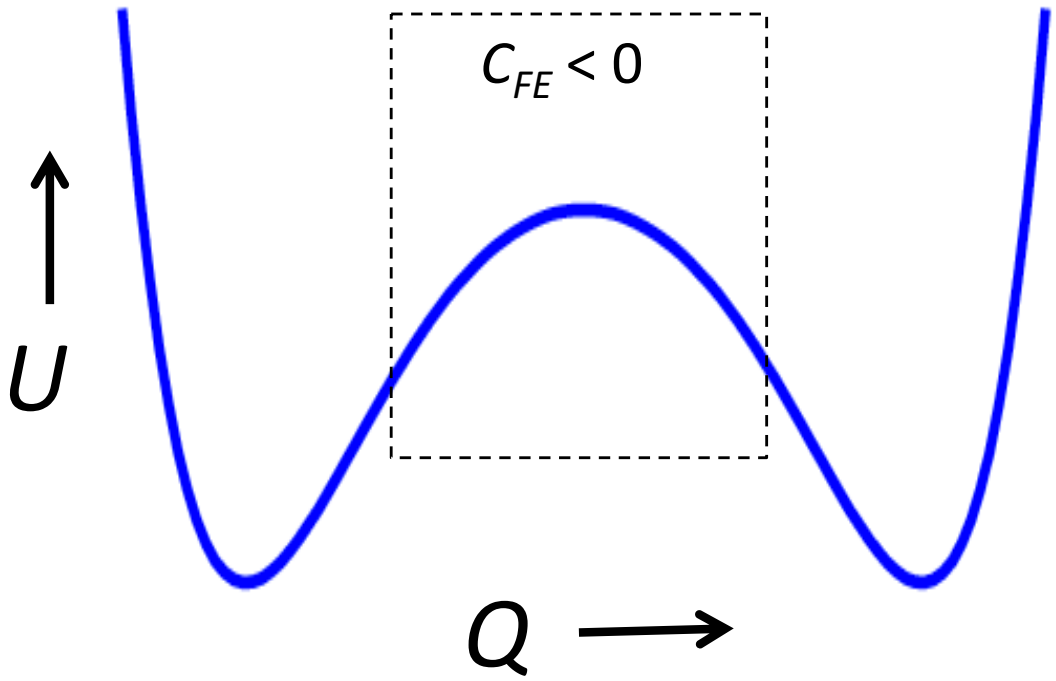
How to get Negative Capacitance Material



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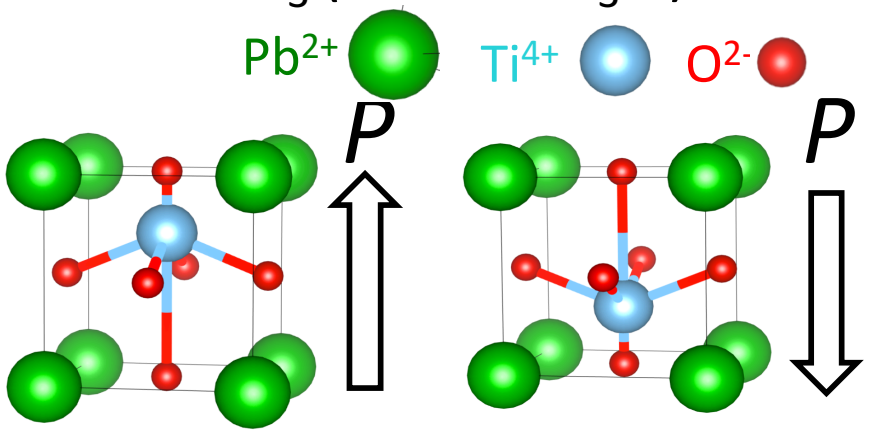
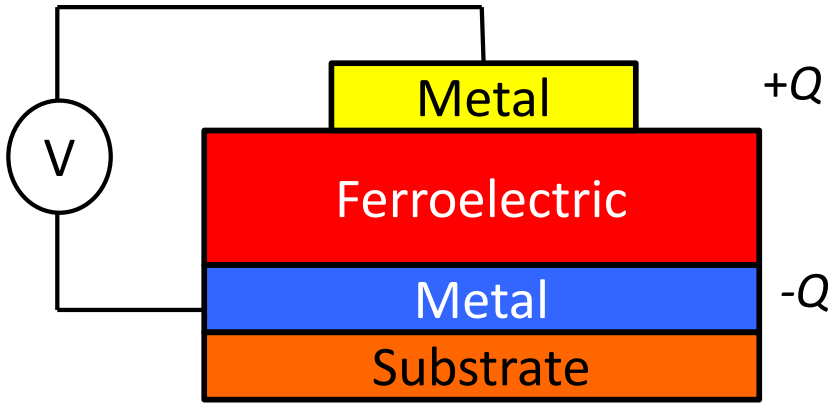
Ferroelectric Oxides

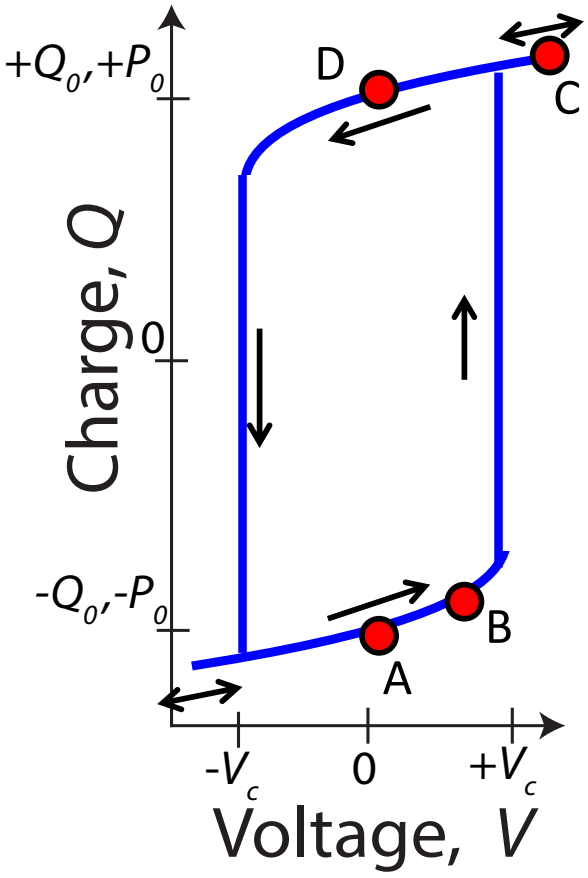
Classical Ferroelectric

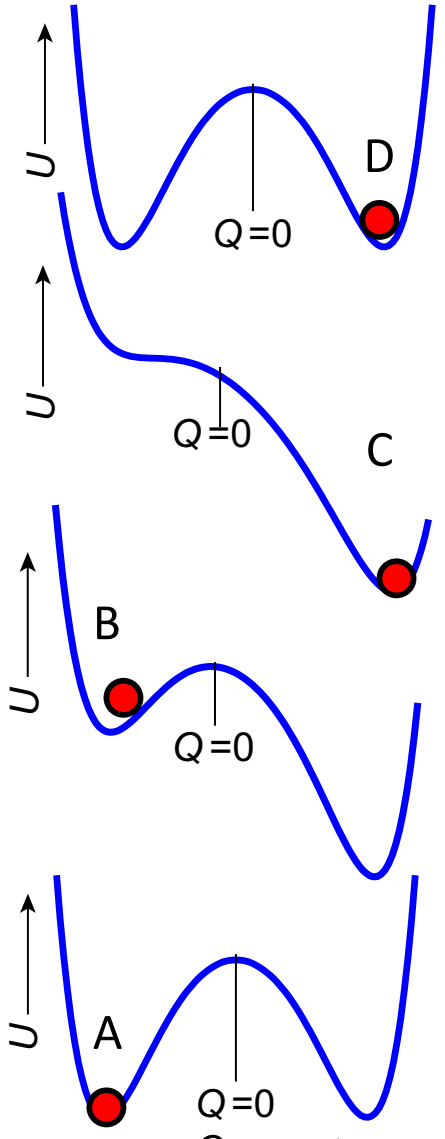
$PbTiO_3$ ($Pb^{2+}Ti^{4+}O_3^{6-}$)





Charge Voltage Characteristics





A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercivity voltage .

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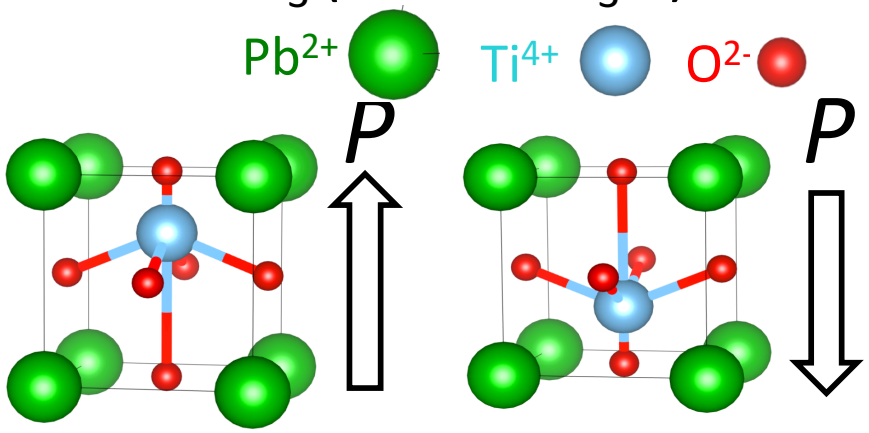
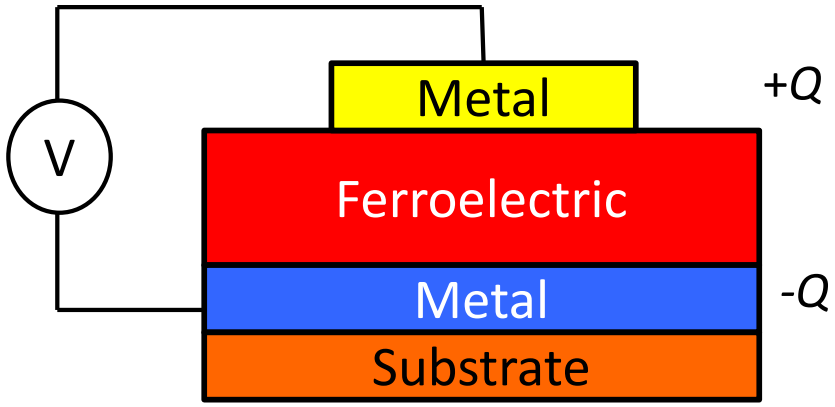
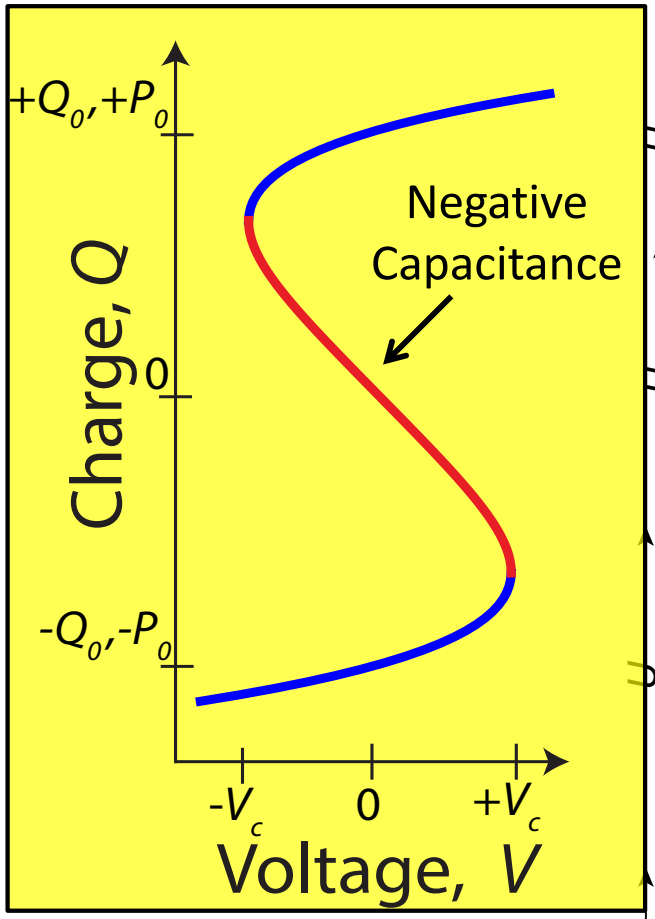
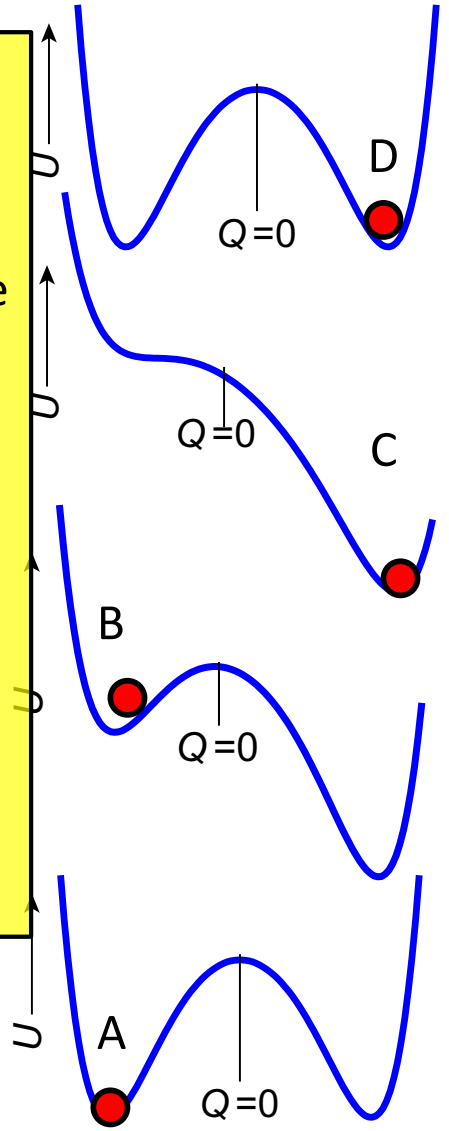




Charge Voltage Characteristics





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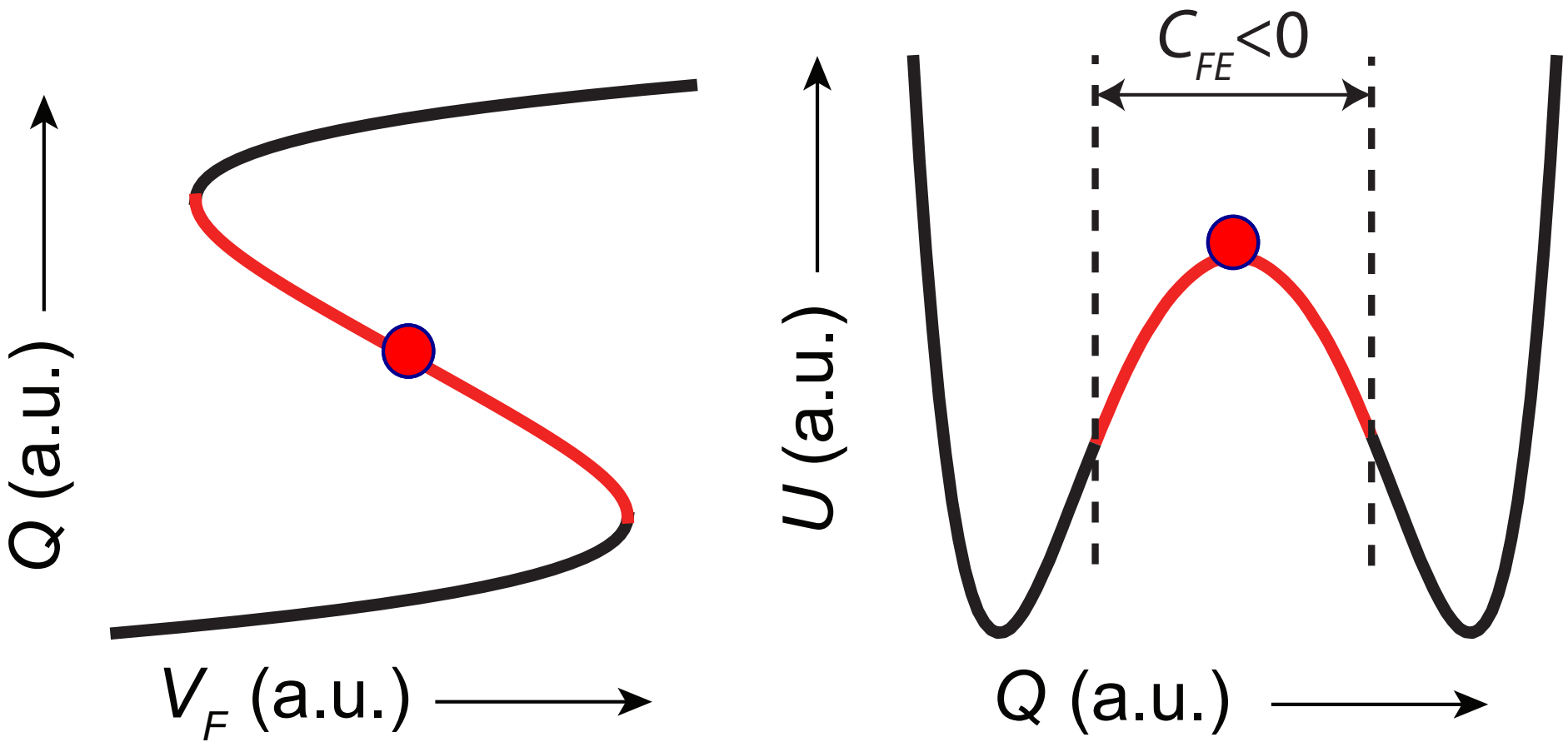
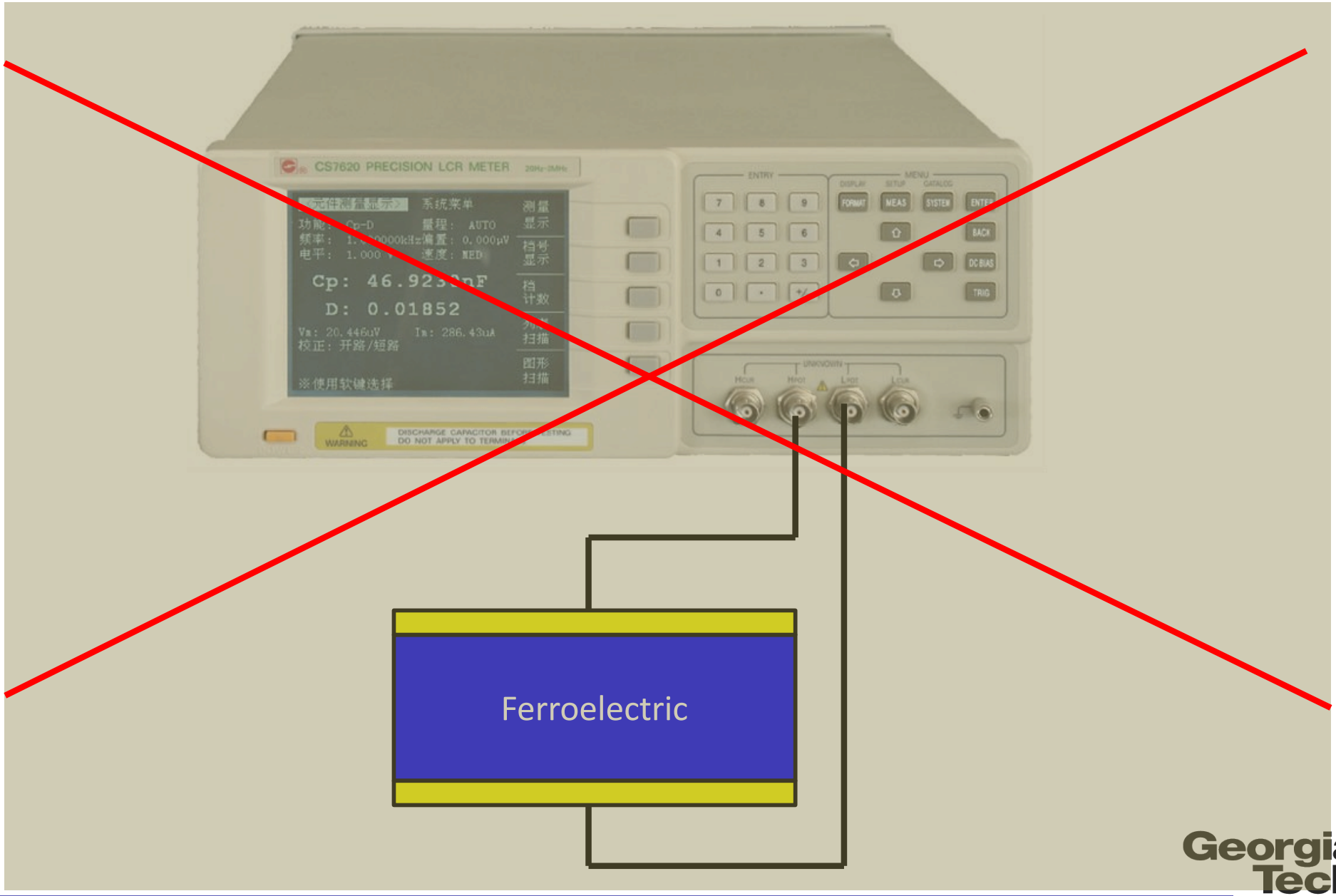
Why is it difficult to measure?

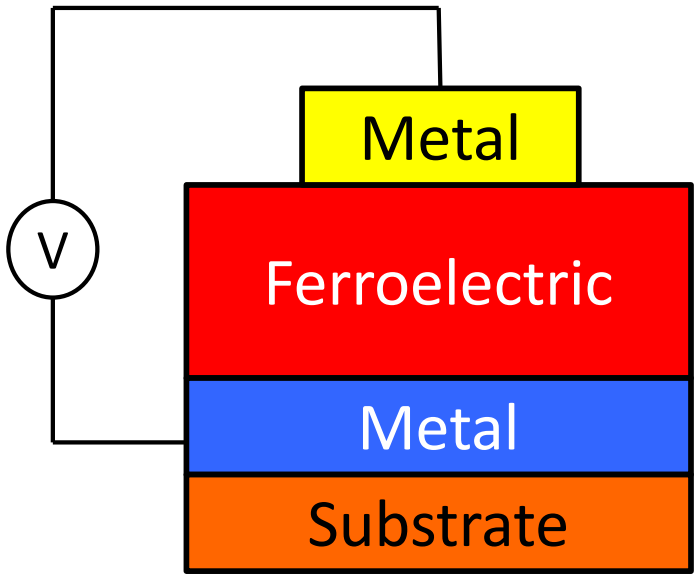


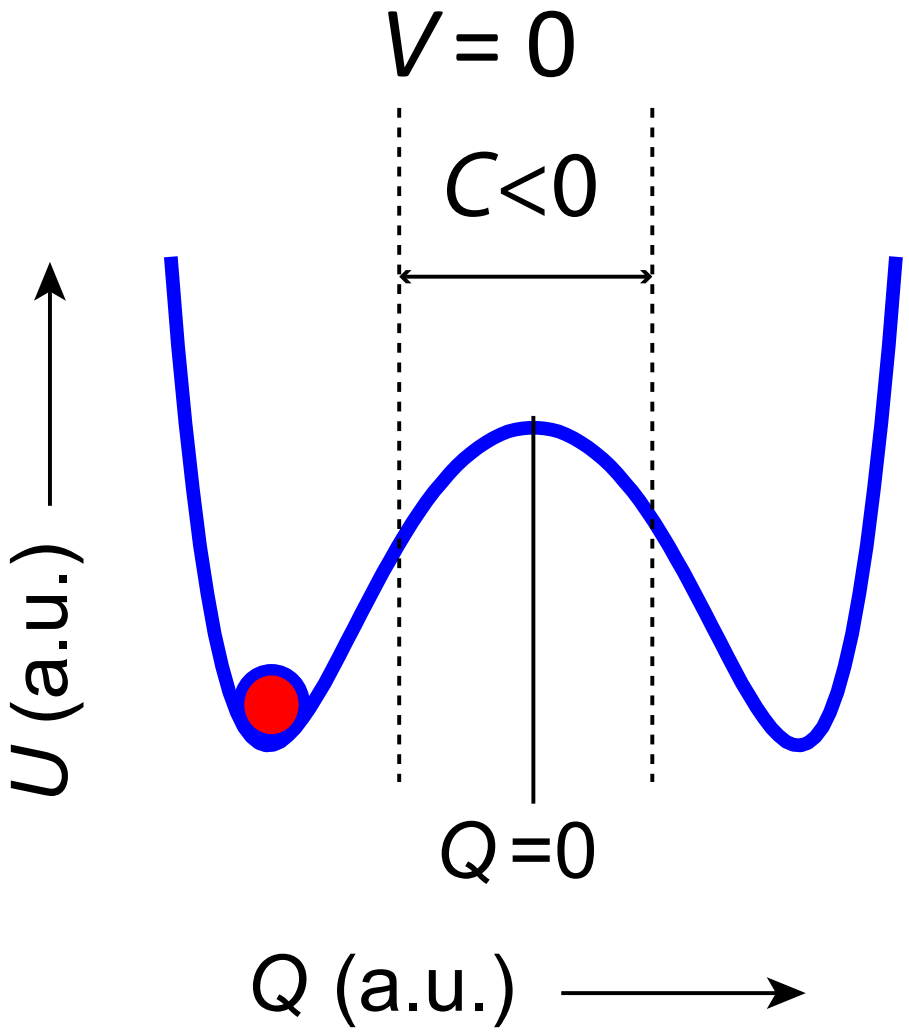
Ferroelectric Negative Capacitance is unstable and cannot be accessed in a time independent equilibrium measurement.

Why is it difficult to measure?



Direct Measurement of Negative Capacitance





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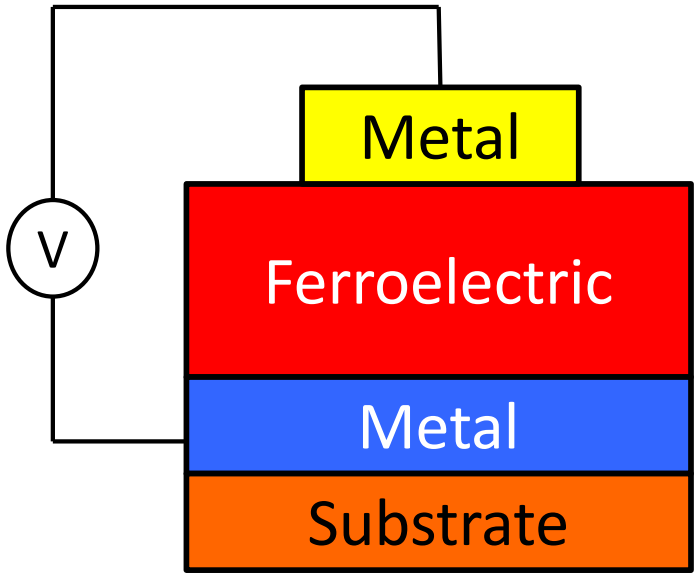
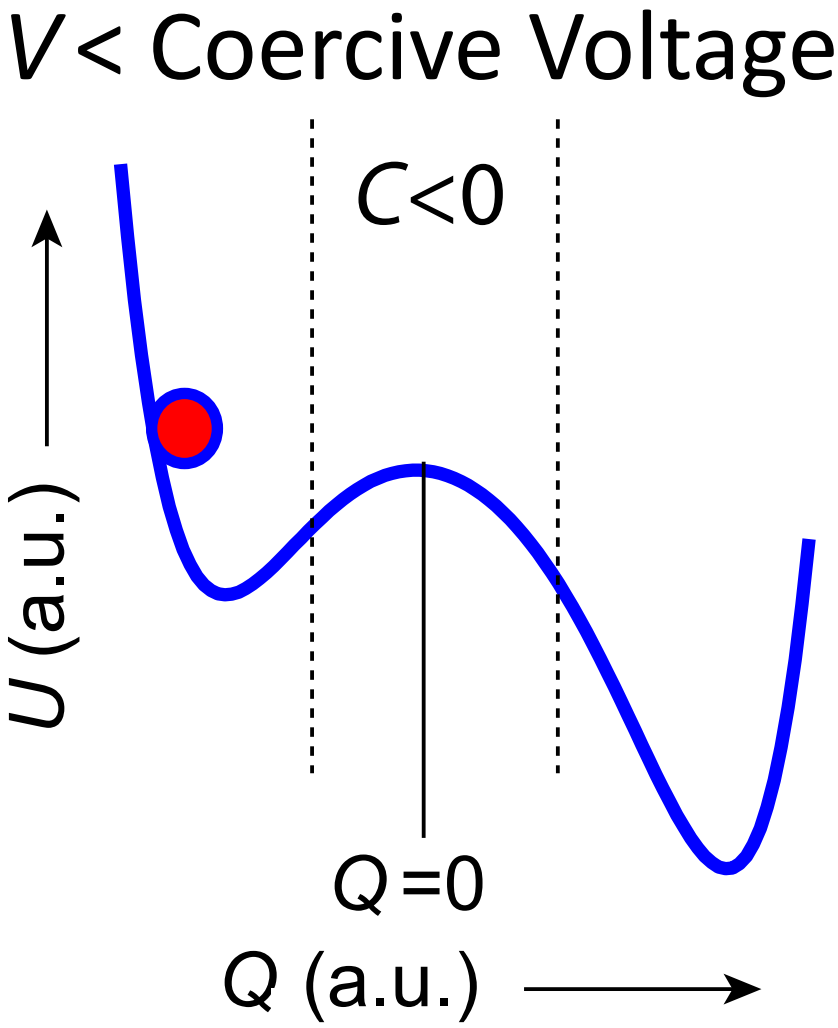
Direct Measurement of Negative Capacitance





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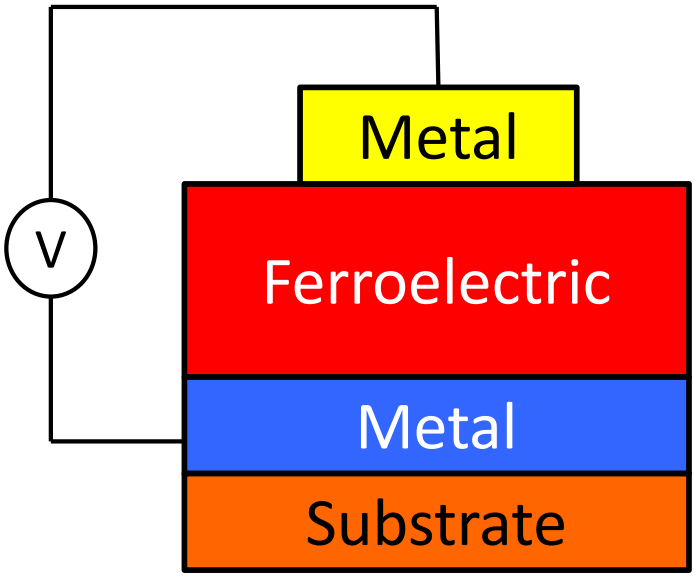
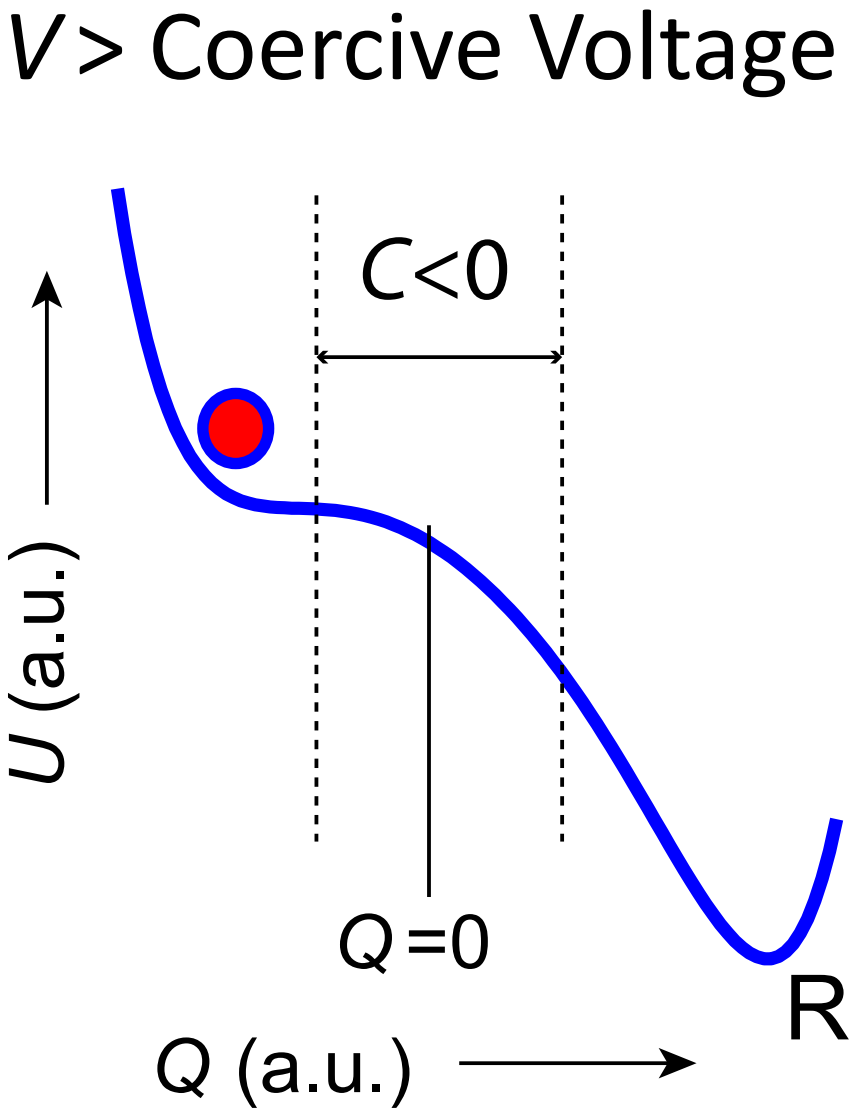
Direct Measurement of Negative Capacitance



A ferroelectric capacitor goes through the unstable negative capacitance states during switching.



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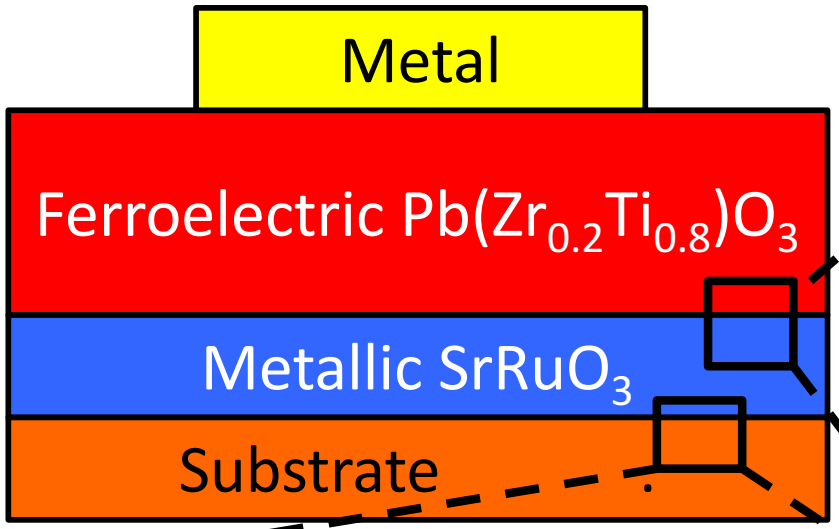
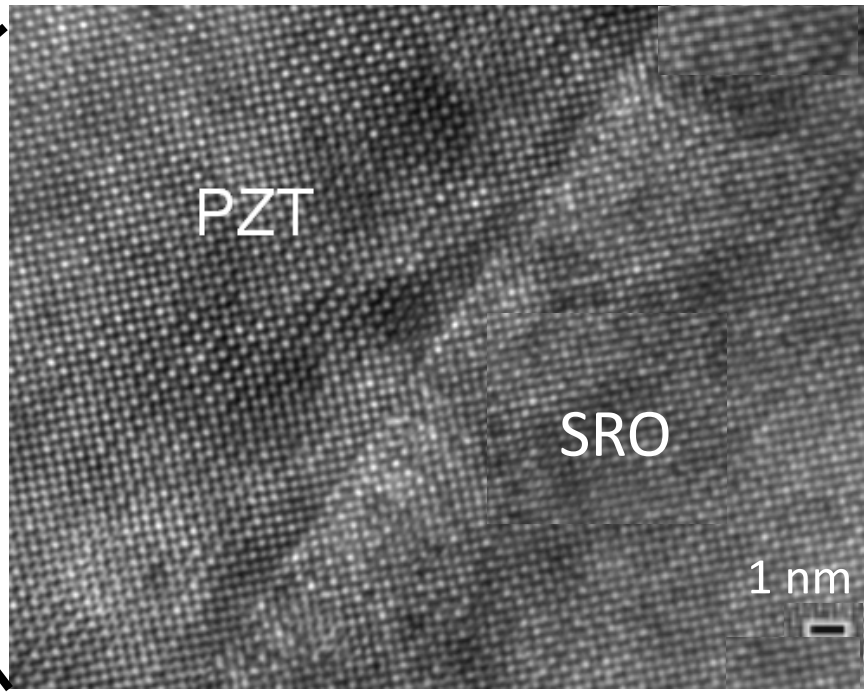
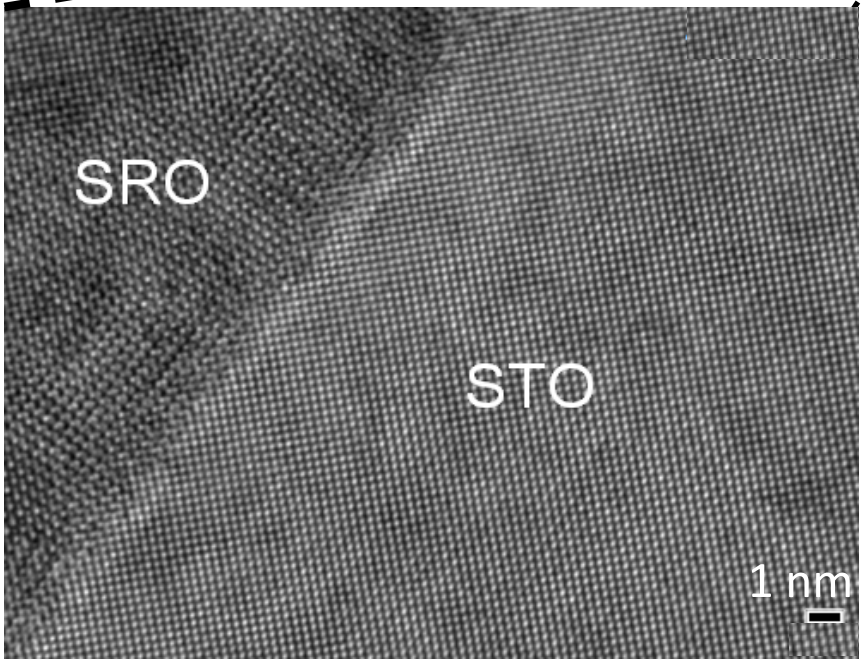
Ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$







Courtesy: Pan group, U. Mich.

Excellent epitaxial quality!

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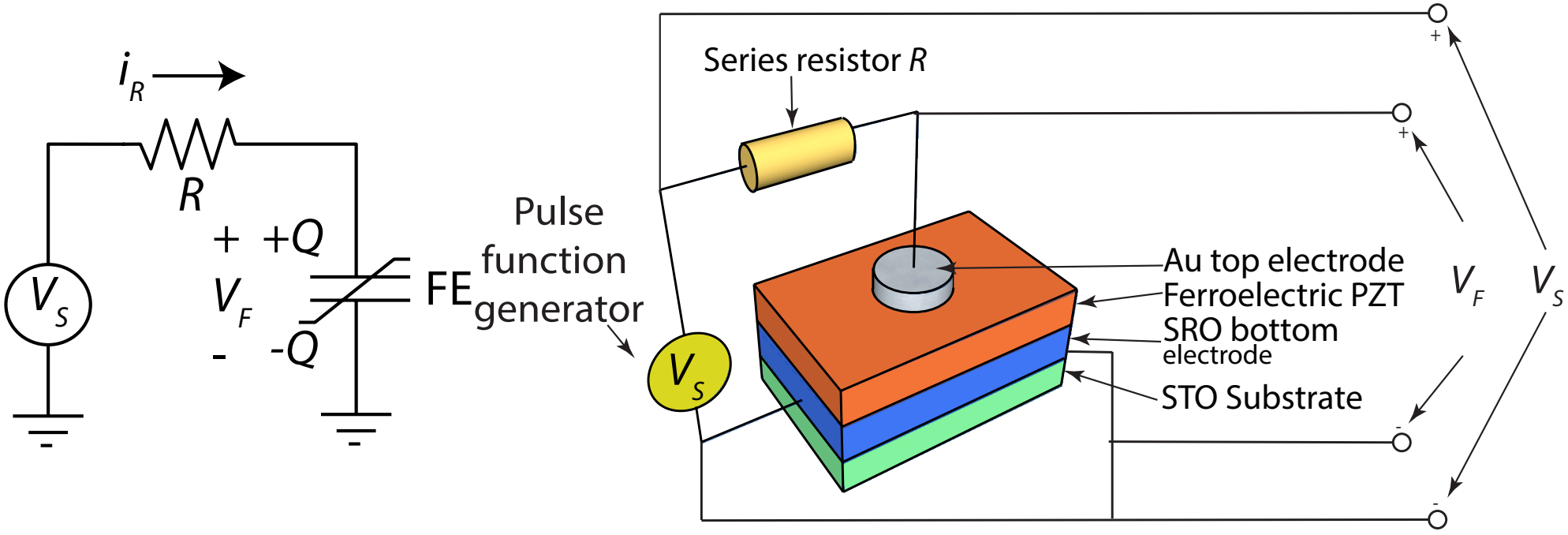
Direct Measurement of Negative Capacitance



A ferroelectric capacitor connected in series with an external resistor.

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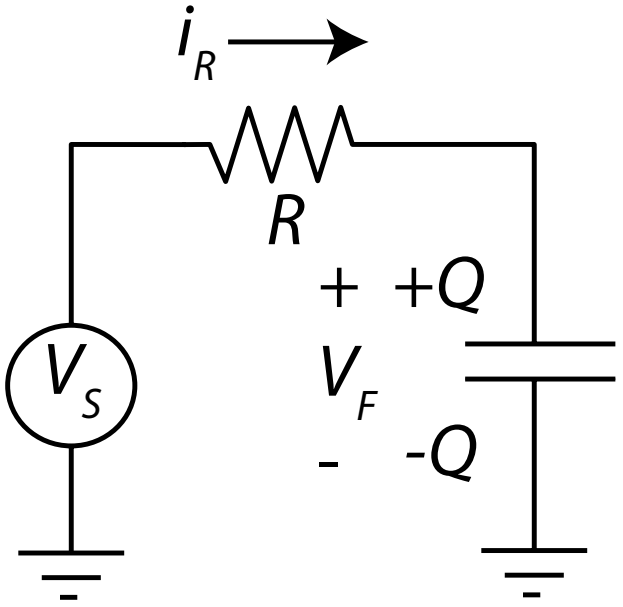
What happens in an *R-C* Series circuit?

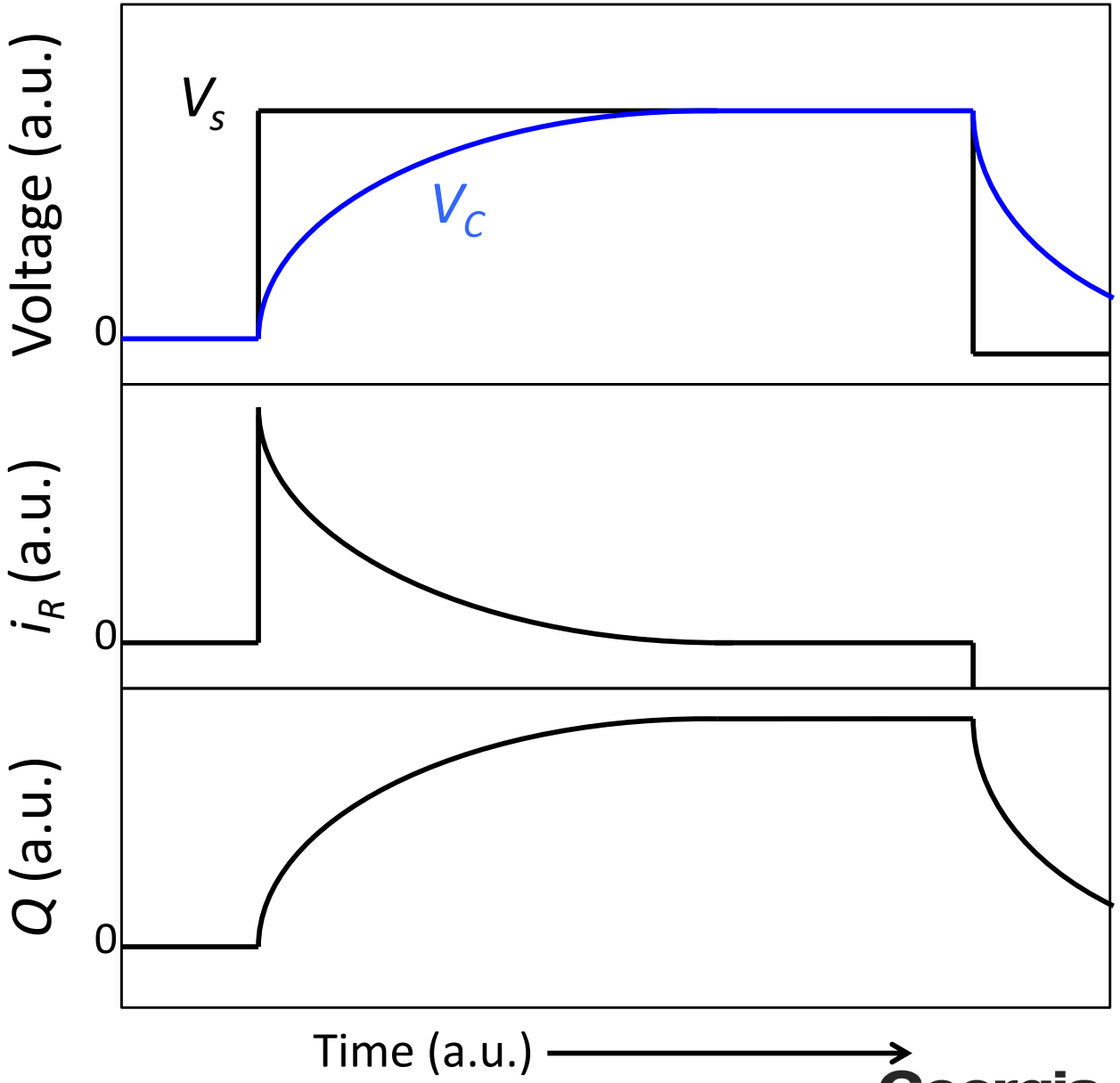


Voltage: $V_C=V_S(1-e^{-t/RC})$

Current: $i_R=V_S e^{-t/RC}/R$

Charge: $Q=CV_S(1-e^{-t/RC})$

At any time t,
$dQ/dV_C=C>0$.



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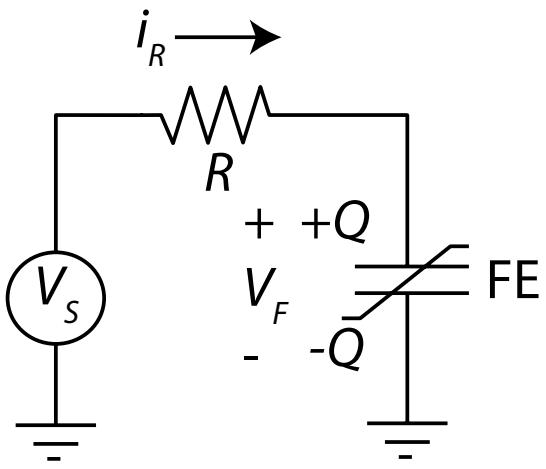
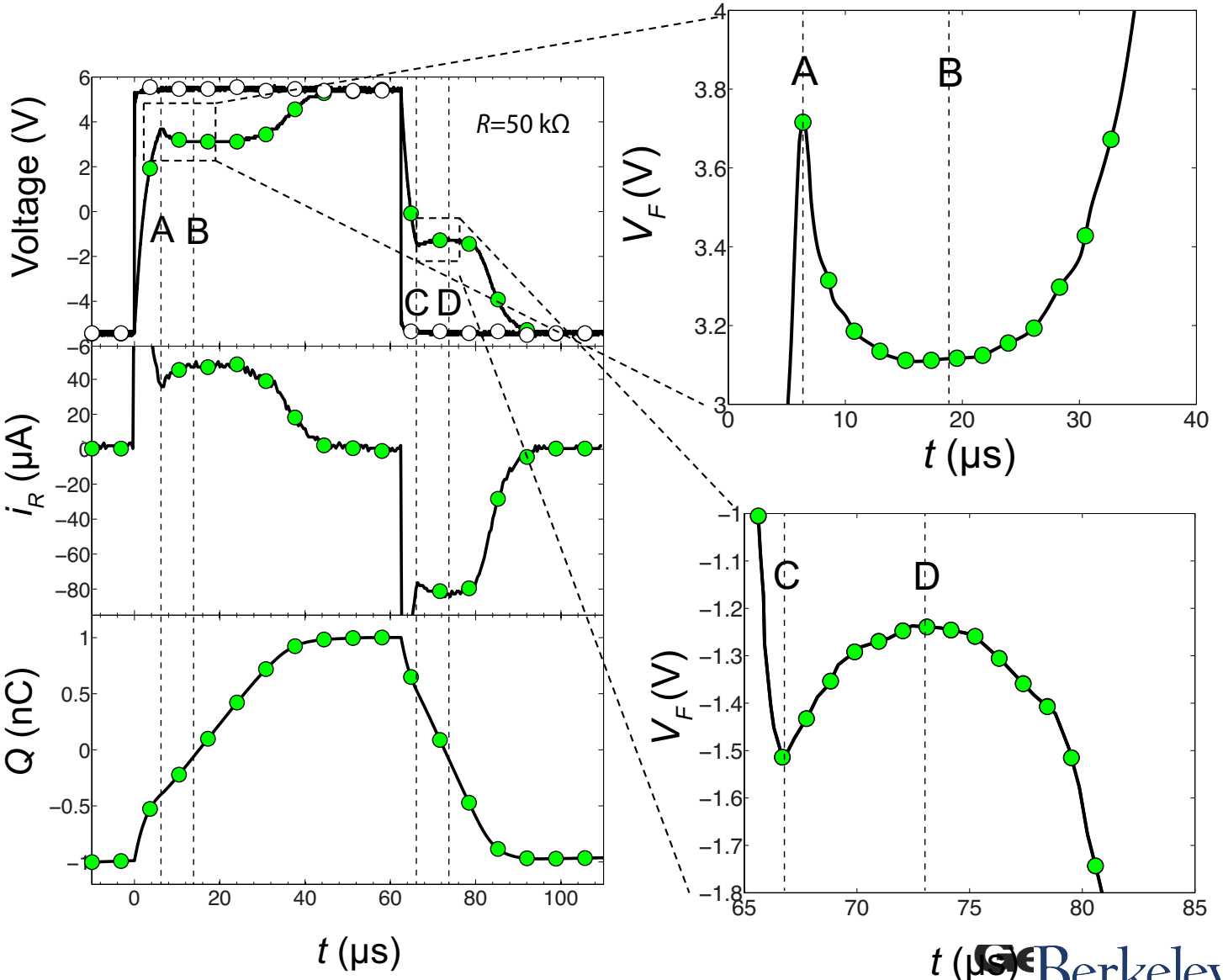
Direct Measurement of Negative Capacitance

60 nm $Pb(Zr_{0.2}Ti_{0.8})O_3$) (Coercive voltage=~2.5 V)

V_s: -5.4 V → +5.4 V → -5.4 V





During AB & CD, dQ & dV_F has opposite signs indicating $dQ/dV_F < 0$.

Khan et al. Nature Mater. 14, 182 (2015)

Direct Measurement of Negative Capacitance

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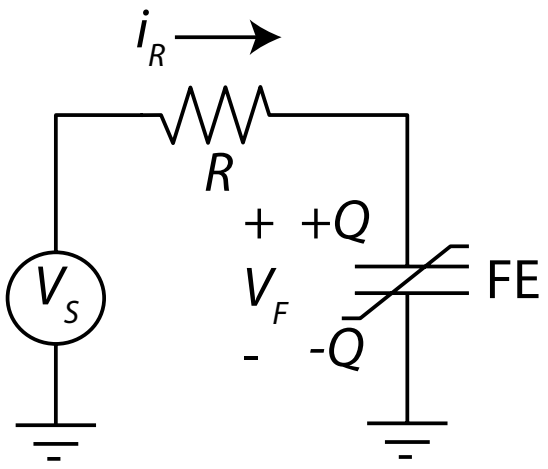

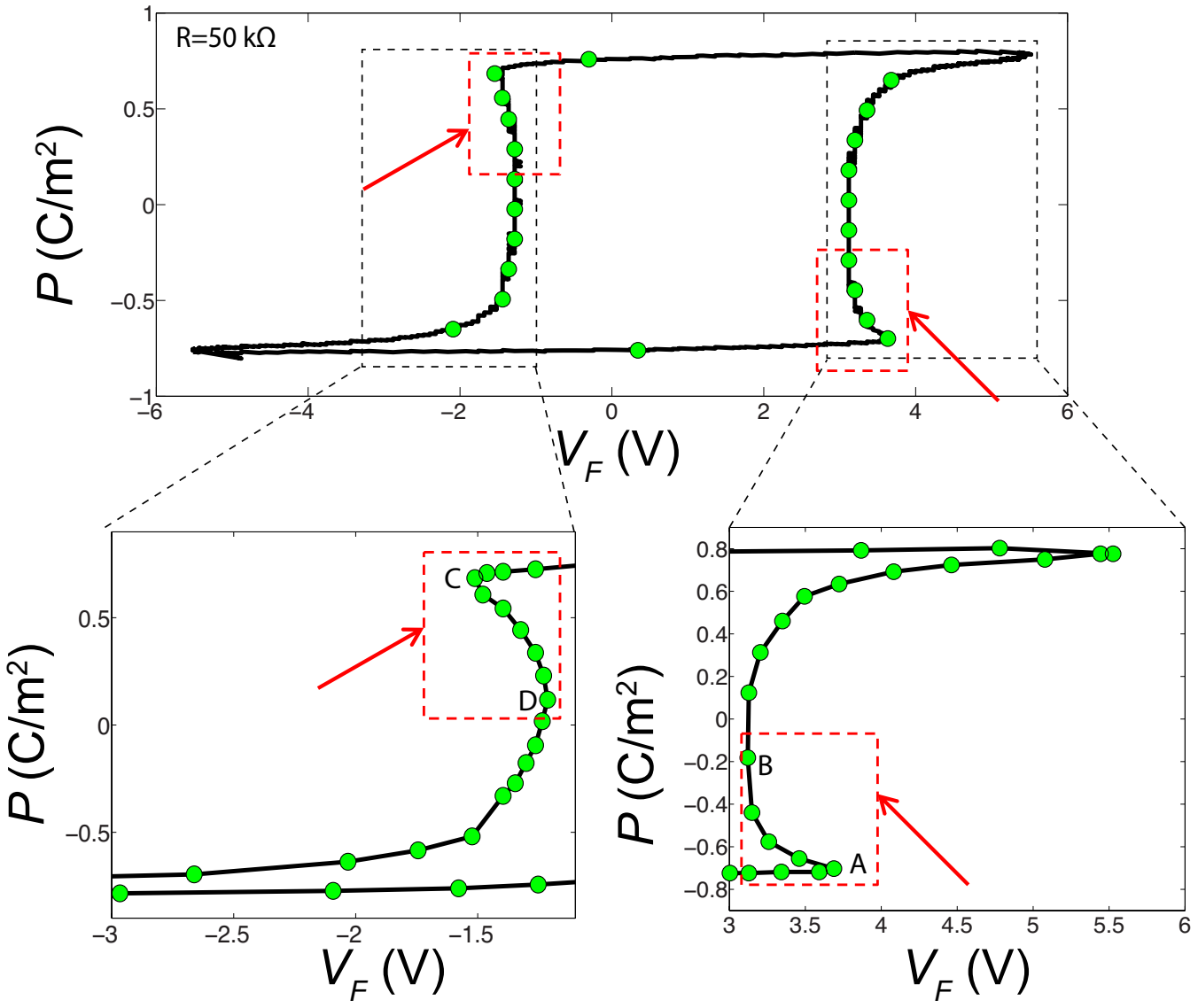

A negative dQ/dV_F directly observed in an isolated ferroelectric.

Khan et al. Nature Mater. 14, 182 (2015)

Perspective

Nature Nanotech. 3, 77 (2008)

NEWS & VIEWS

NANOELECTRONICS

Negative capacitance to the rescue?

Victor V. Zhirnov* and Ralph K. Cavin
are at the Semiconductor Research Corporation, Research Triangle Park, North Carolina 27709, USA.
*e-mail: Victor.Zhirnov@src.org

At this point the proposed negative capacitance mechanism has not been observed in experiments, and it remains

Nature Materials 14, 137 (2015)

news & views

FERROELECTRICS

Negative capacitance detected

The experimental detection of negative capacitance in ferroelectrics rekindles hopes that the phenomenon could be used to further push the miniaturization of conventional transistors.

Gustau Catalan, David Jiménez and Alexei Gruverman

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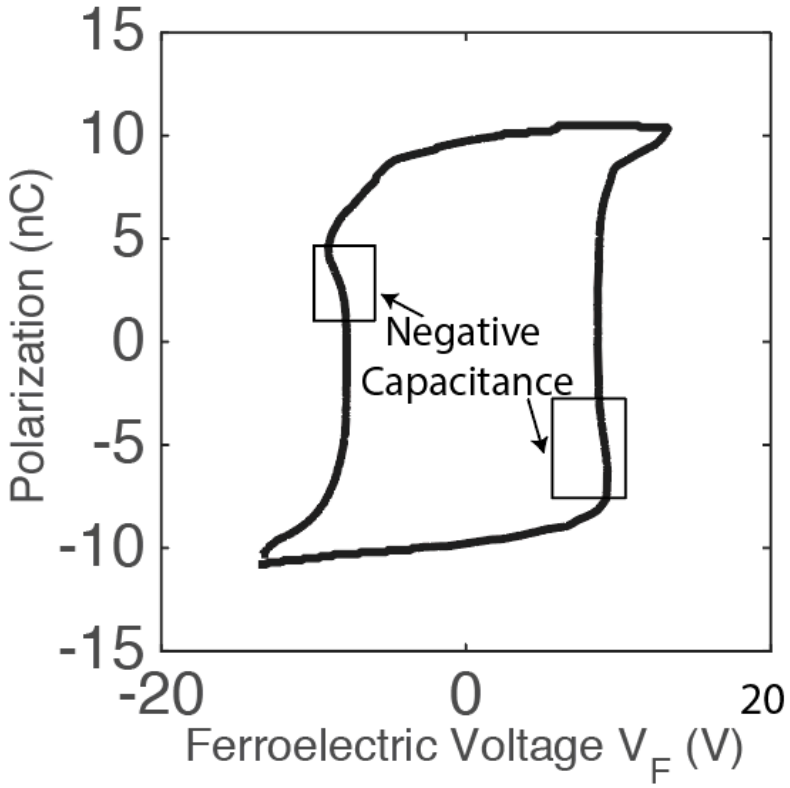
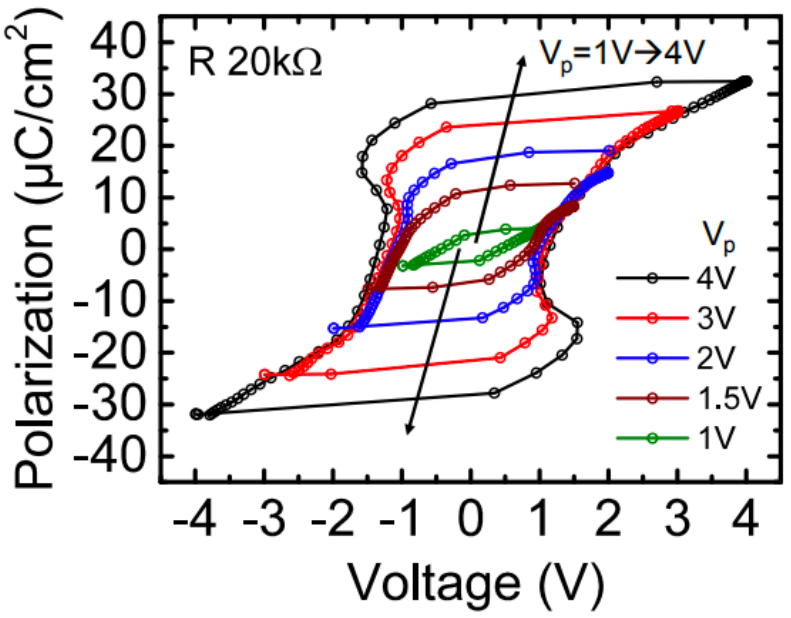
Negative Cap. in Doped HfO_2 Ferroelectrics

Ferroelectric Gd-doped HfO_2 (27 nm)



Hoffmann et al. Direct Observation of Negative Capacitance in Polycrystalline Ferroelectric HfO_2. Advanced Functional Materials 2016.

Ferroelectric $HfZrO_2$ (10 nm)



Kobayashi et al. Experimental study on polarization-limited operation speed of negative capacitance FET with ferroelectric HfO_2. IEDM 2016

Negative capacitance is a general phenomenon in ferroelectrics!

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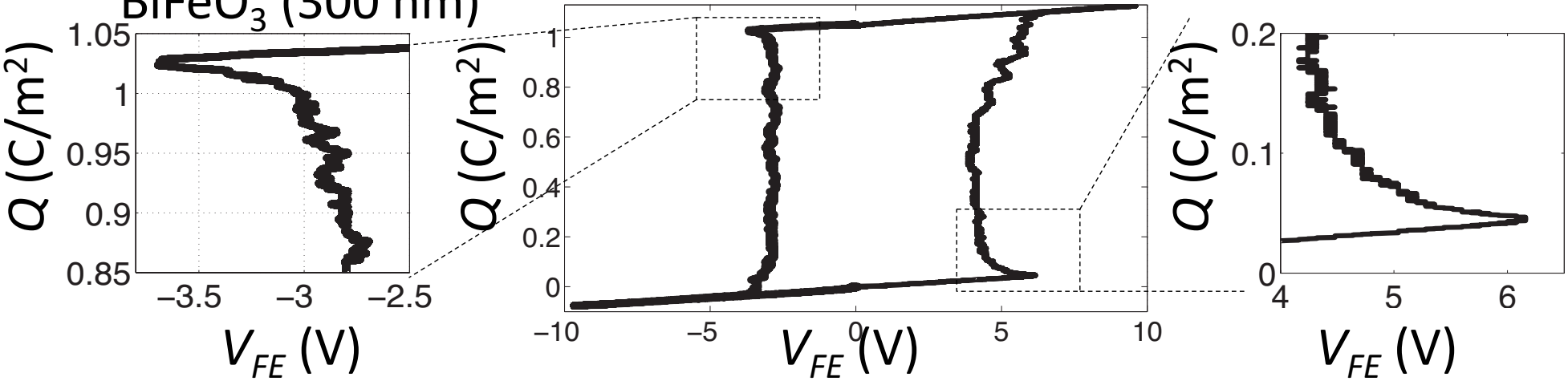
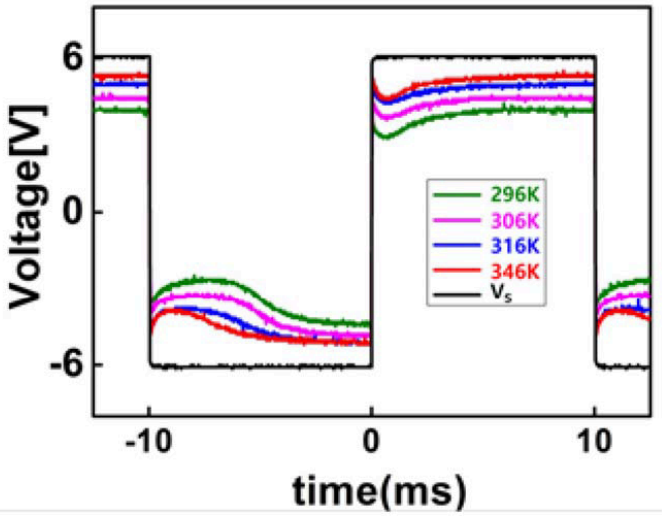
Negative Cap. in Other Ferroelectrics

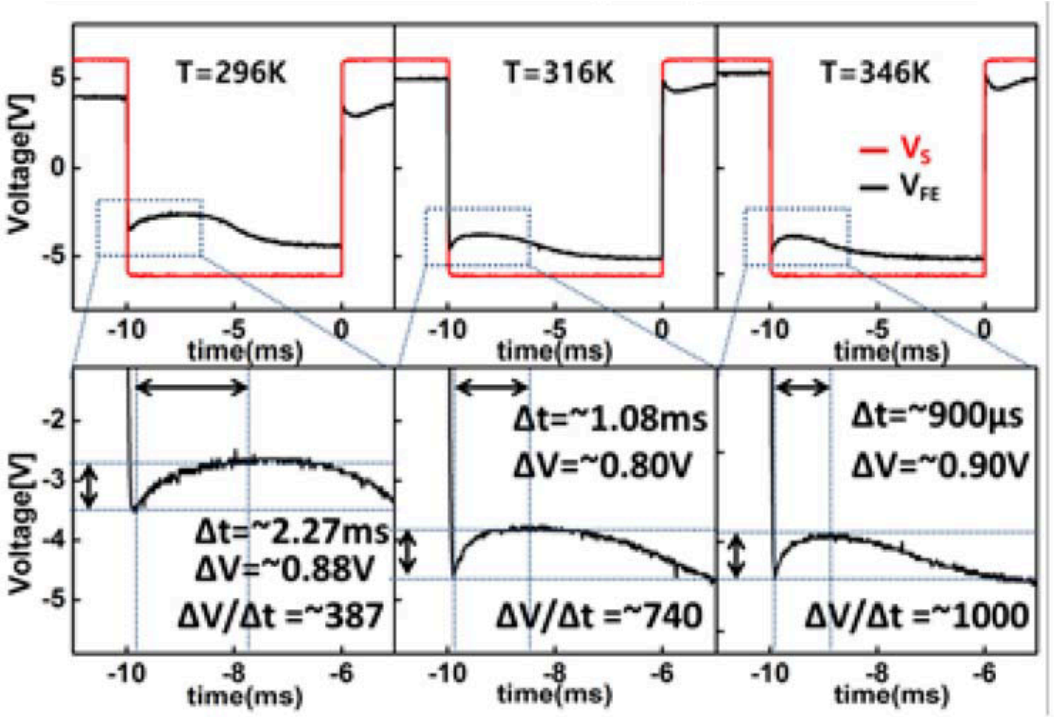
$BiFeO_3$ (300 nm)



Organic Ferroelectric

$PVDF_{0.75}$-$TrFE_{0.25}$ (20 nm)





Ku et al. JEDS 5, 232 (2017)

Negative Capacitance in 1956!

Landauer et al. Polarization reversal in the Barium Titanate hysteresis loops.
J. Appl. Phys. 27, 752 (1956)

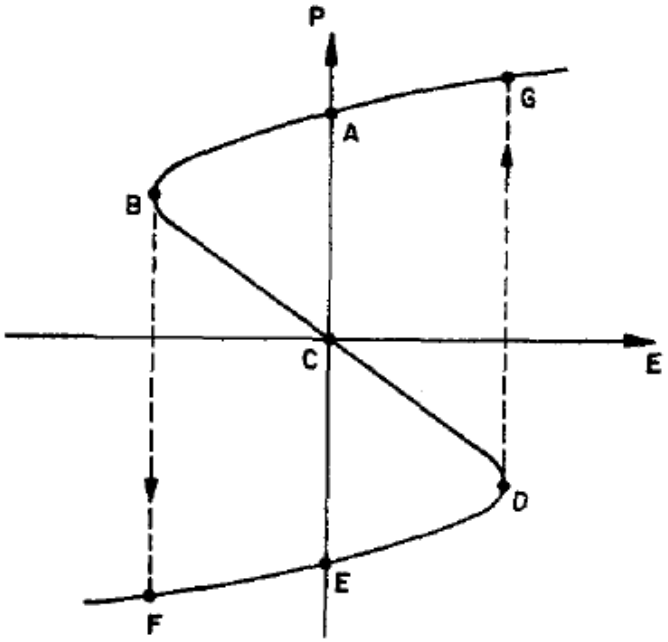


FIG. 1. Plot of polarization against field, at room temperature, as given by Devonshire's theory. P = polarization, E = field. Direction of field and polarization are taken to be the same, and parallel to the "c" axis of a single domain crystal. The solid line $GABCDEF$ gives the theoretical relationship.

Merz. Switching time in BaTiO3 and its dependence on its crystal thickness. **J. Appl. Phys.** 27, 938 (1956)

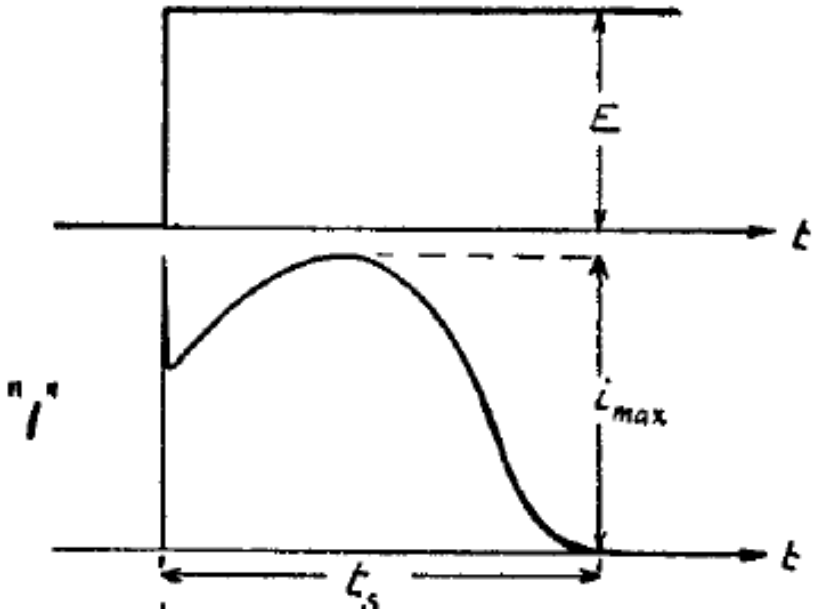


FIG. 1. Pulsing field and pulsing current *versus* time.

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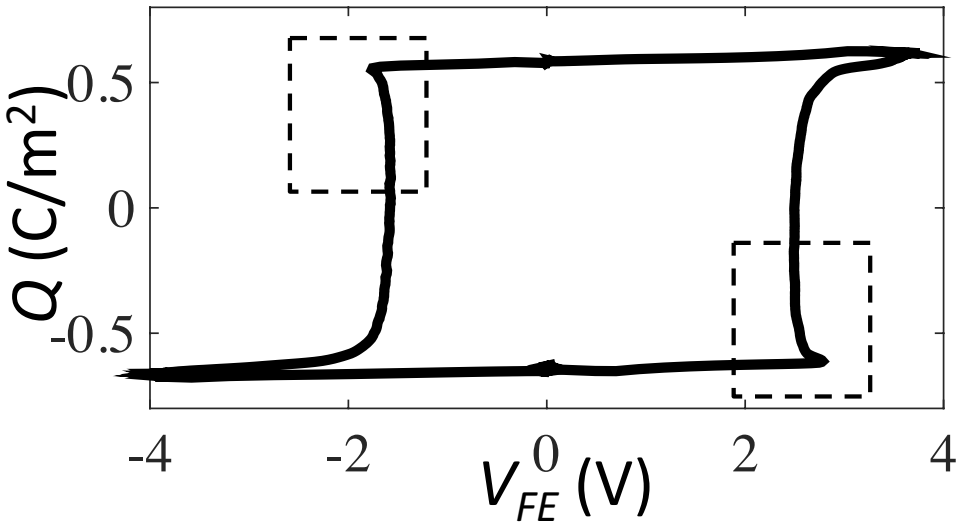
What's next? Stabilize it!

Now that negative capacitance has been detected…



How to stabilize negative capacitance?

1. Can we see capacitance enhancement?

2. Can we see voltage amplification in a ferroelectric-dielectric network?

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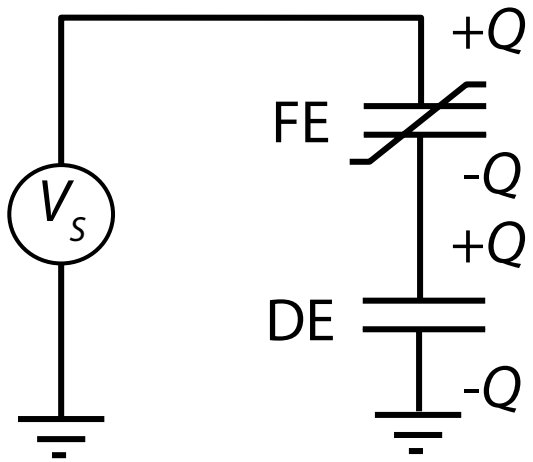
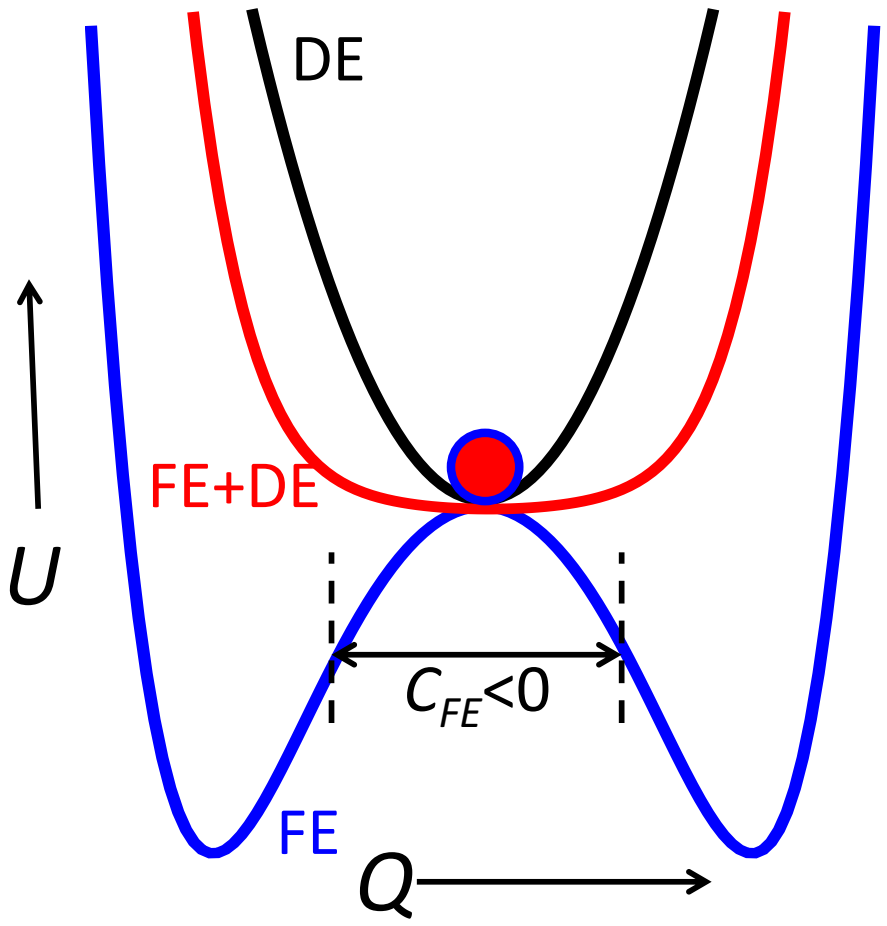
Capacitance Enhancement due to Neg. Cap

Ferroelectric-Dielectric Series Combination



$$C = \left[\frac{d^2U}{dQ^2}\right]^{-1}$$

Energy Landscapes



Equivalent Capacitance $C_{FE+DE} = \left[\frac{1}{C_{FE}} + \frac{1}{C_{DE}}\right]^{-1}$

$C_{FE+DE} > C_{DE}$ If $C_{FE} < 0$

Enhancement of capacitance in a FE-DE Series combination!

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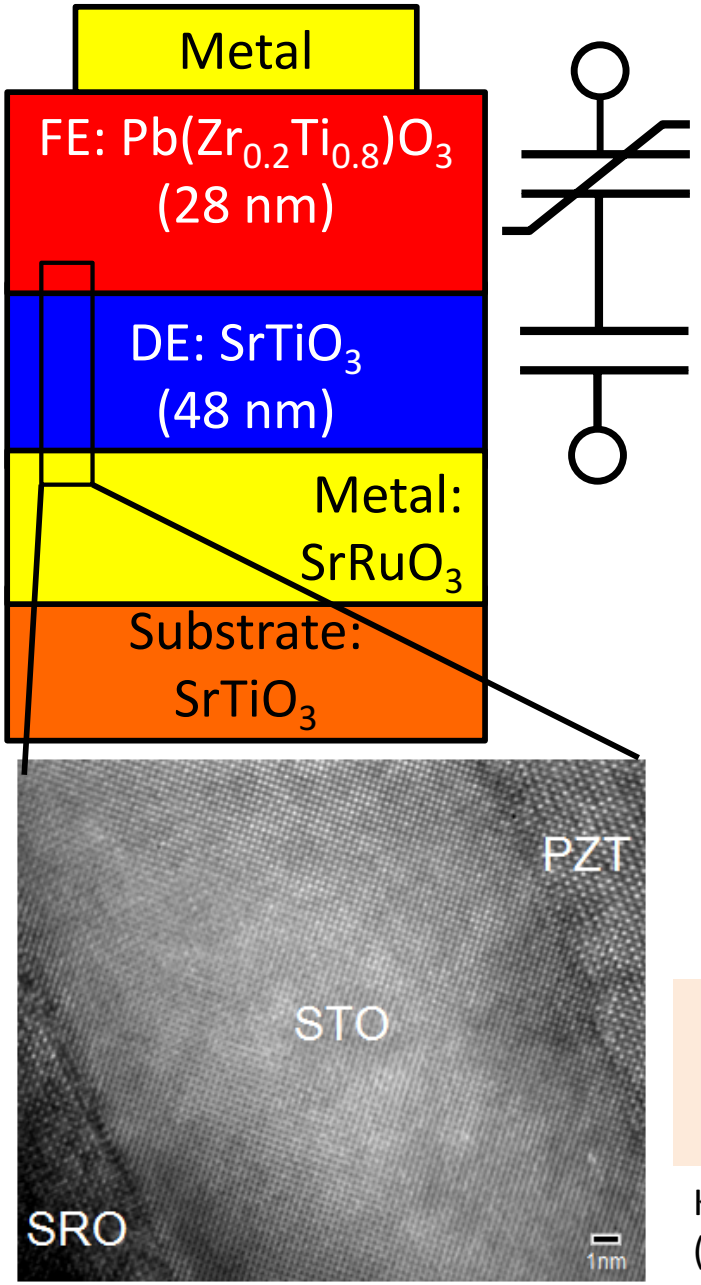
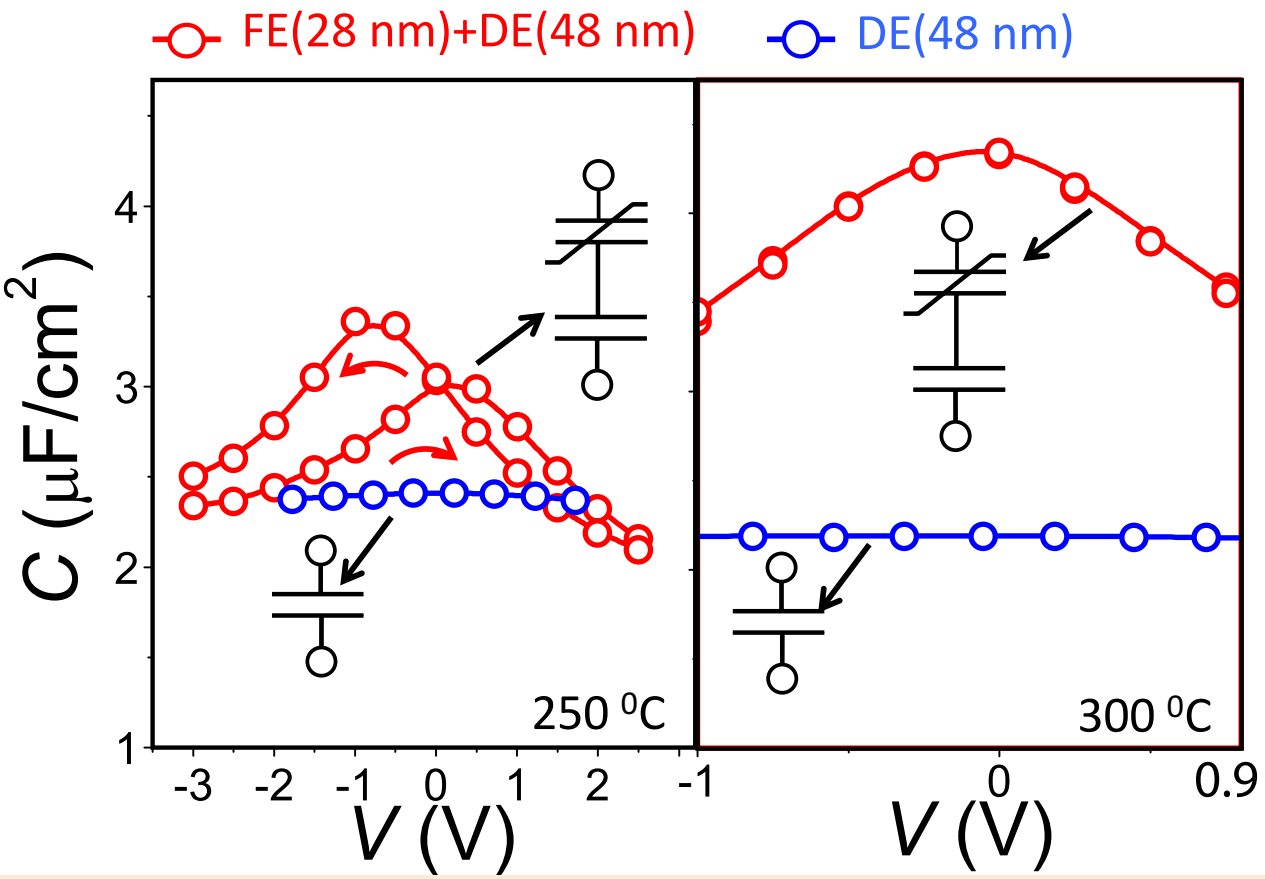
Capacitance Enhancement due to Neg. Cap.



C-V Characteristics



Capacitance Enhancement in a FE-DE heterostructure experimentally observed!

Khan et al. Appl. Phys. Lett. 100, 113501 (2011) (cover article, most downloaded Aug/Sep 2011).
Gao, Khan et al. Nano Lett. 14, 5814 (2014)

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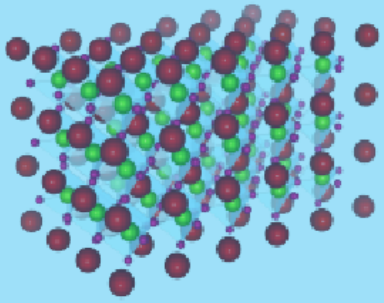
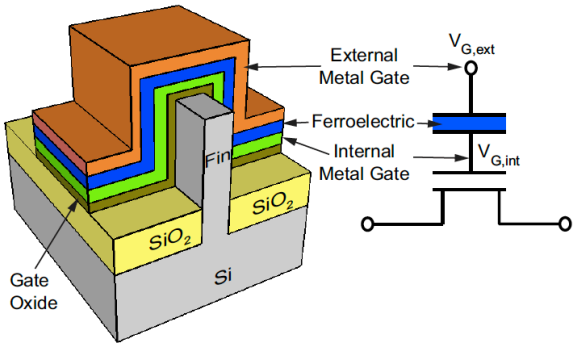
What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors



What do we need to know?

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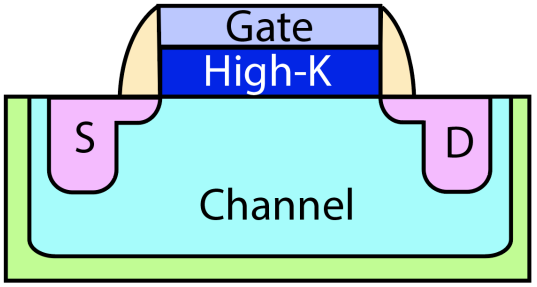
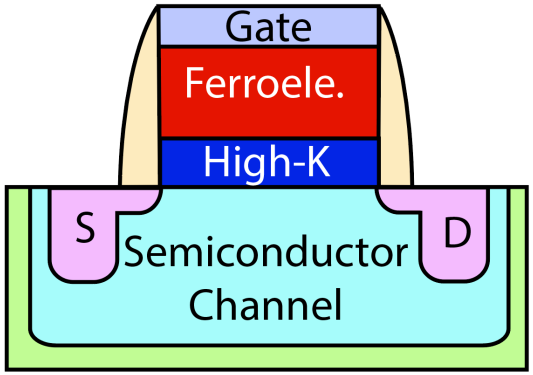
Physics of Negative Capacitance FET

Baseline FET



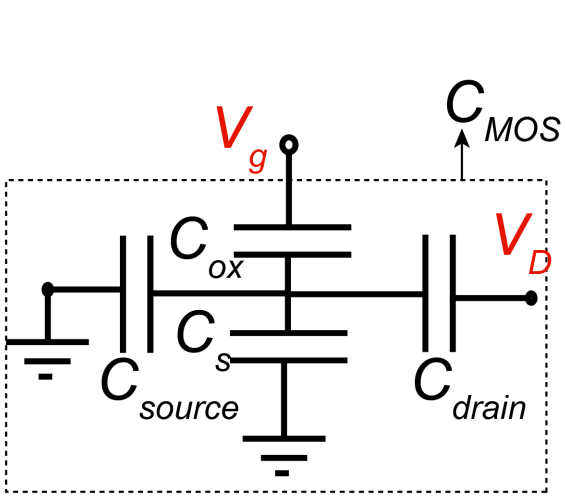
NCFET

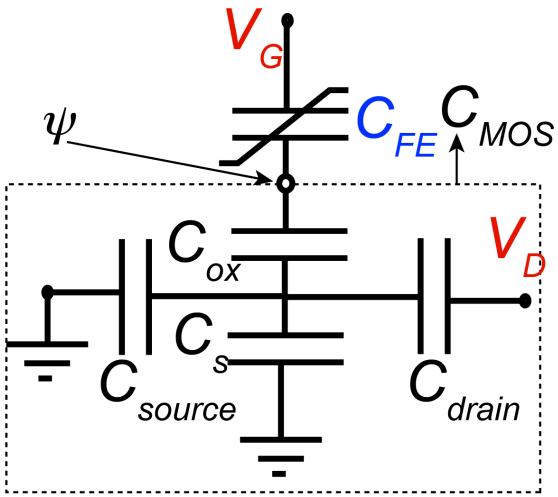


Amplification Factor

$$\frac{d\psi}{dV_G} = \frac{C_{FE}}{C_{FE} + C_{MOS}} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}}$$

Modified Body Factor $m^o = \frac{dV_G}{d\psi} = 1 - \frac{C_{MOS}}{|C_{FE}|}$





Subthreshold Swing $S^{NC} = S^{original} \times (1 - \frac{C_{MOS}}{|C_{FE}|})$

Ideal Switch: ~0 mV/decade ⇐ $|C_{FE}| \approx C_{MOS}$, $|C_{FE}| > C_{MOS}$

Condition	Characteristics	Mode
$C_{FE}<0$, $\|C_{FE}\|>C_{MOS}$	$0<m^o<1$, $S^{NC}<S^{original}$	Logic
$C_{FE}<0$, $\|C_{FE}\|<C_{MOS}$	$m^o<0$, $S^{NC}<0$	Memory

Khan et al. IEDM 2011

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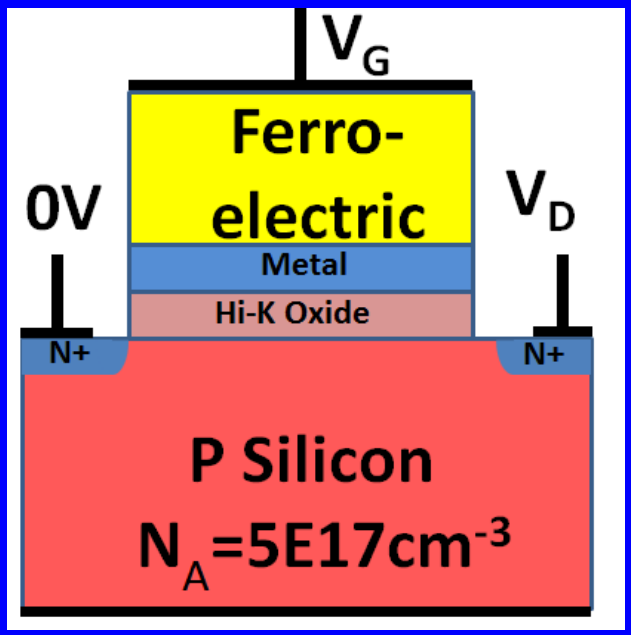
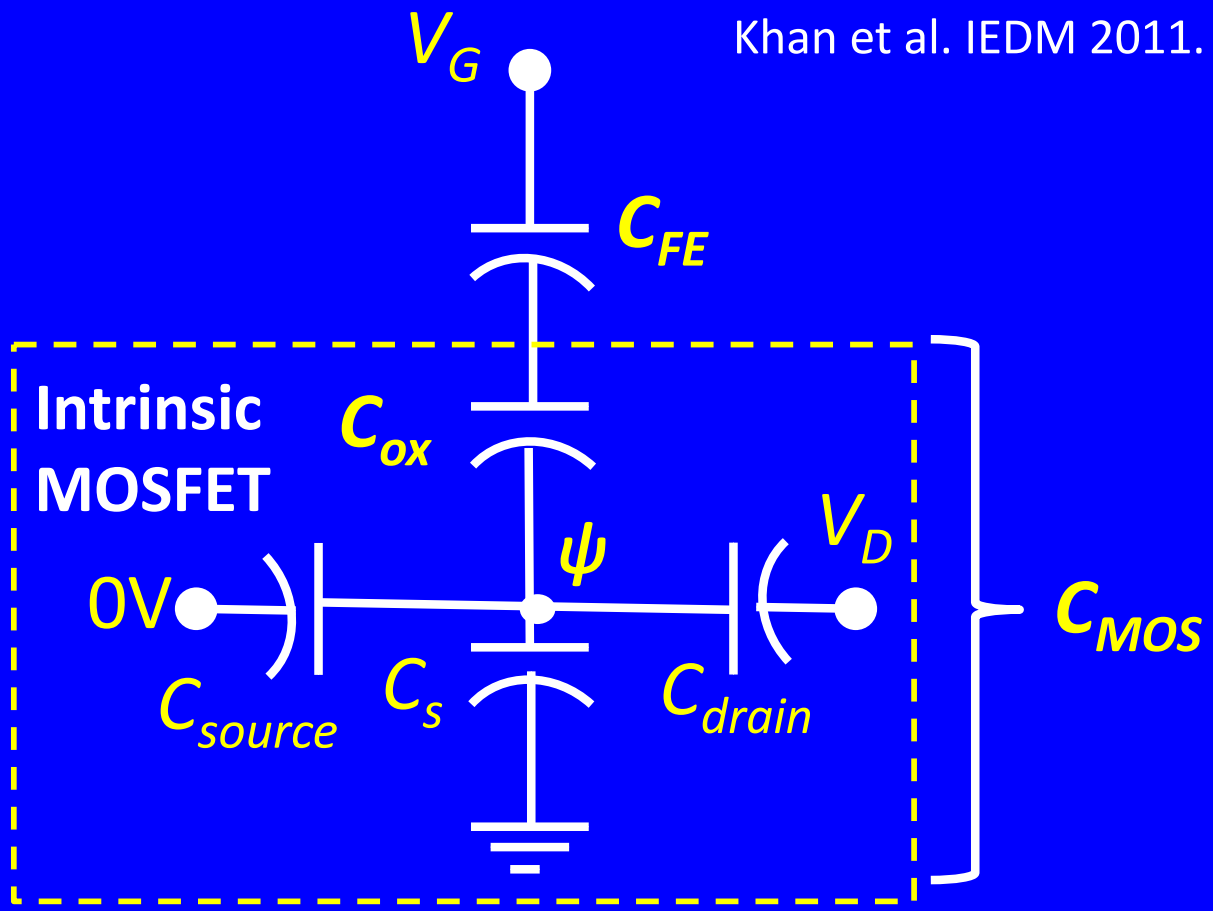
Sub 60mV/dec Negative Capacitance FET: Capacitance Tuning Perspective

Khan et al. IEDM 2011.

Negative Capacitance FET



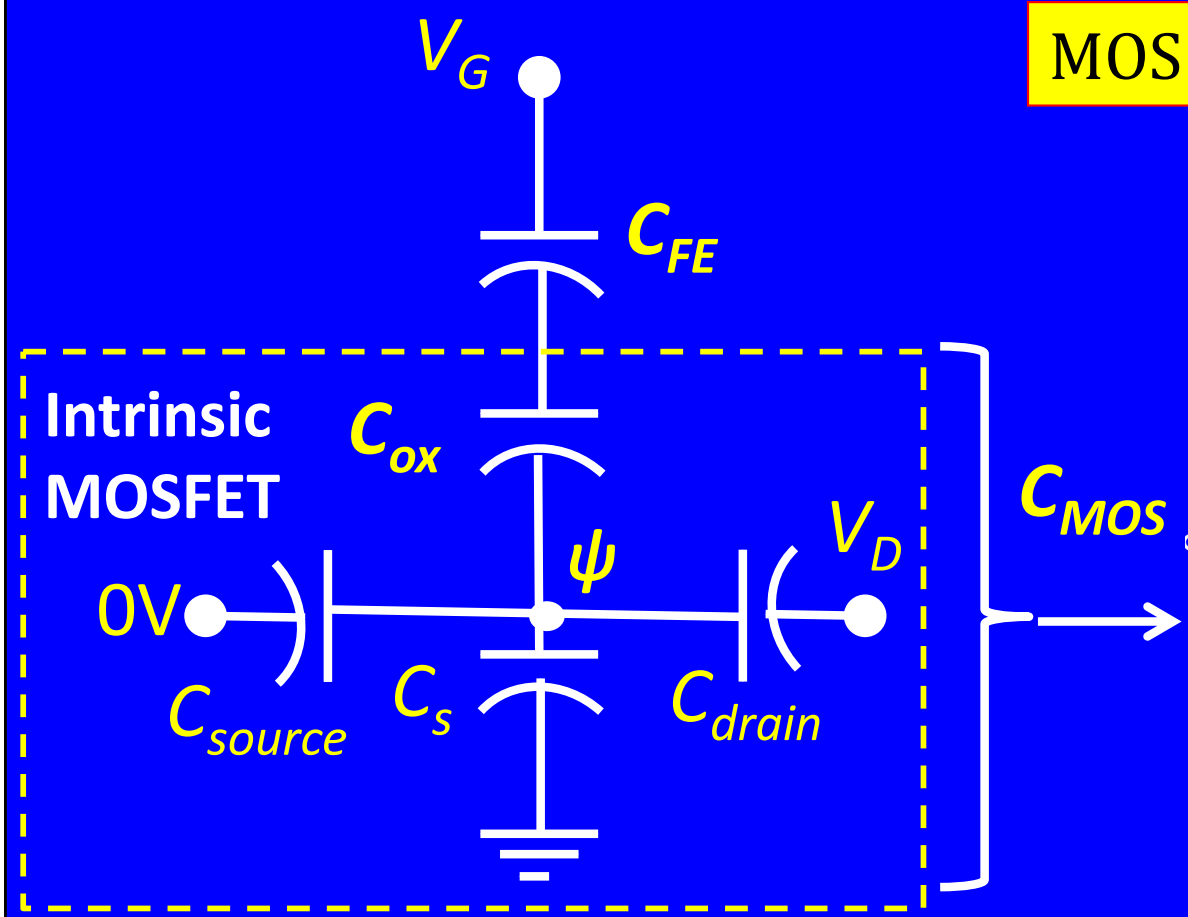


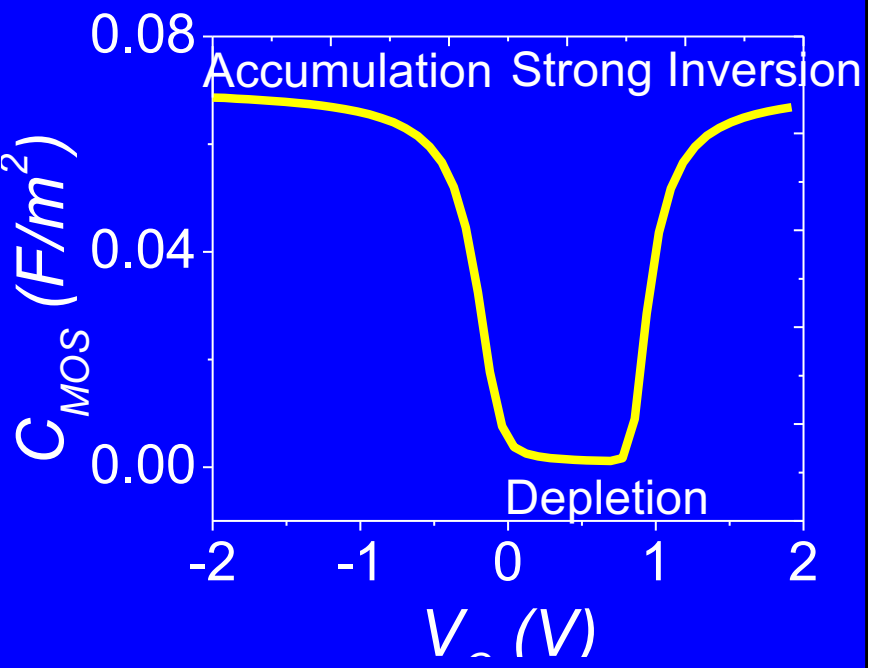
Ideal Switch: ~0 mV/decade $\Leftarrow |C_{FE}| \approx C_{MOS}, |C_{FE}| > C_{MOS}$

Is it possible to match C_{FE} and C_{MOS} over a large range of charge densities and voltages ?

Capacitance Matching in an NCFET

MOS Capacitance is non linear!

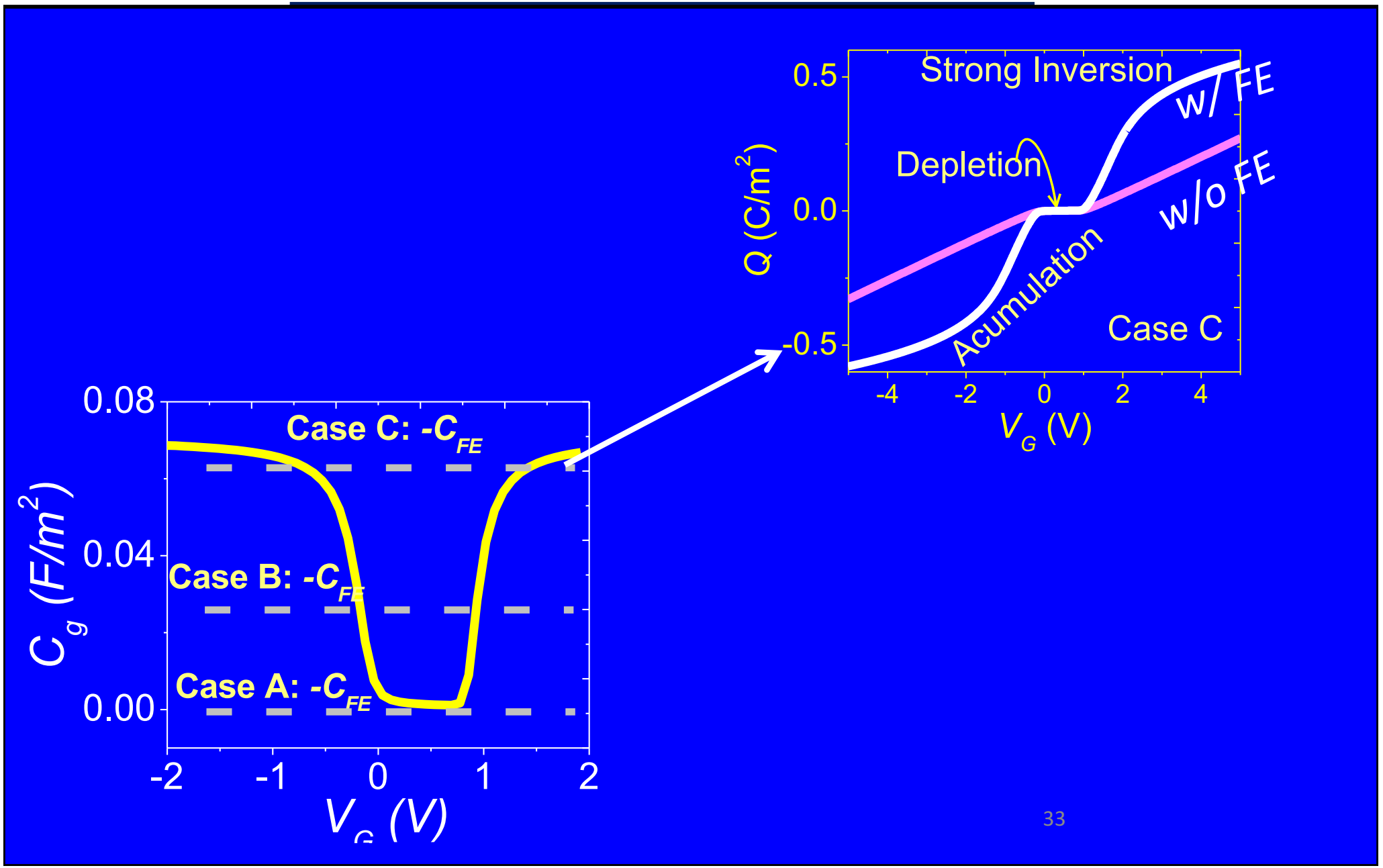




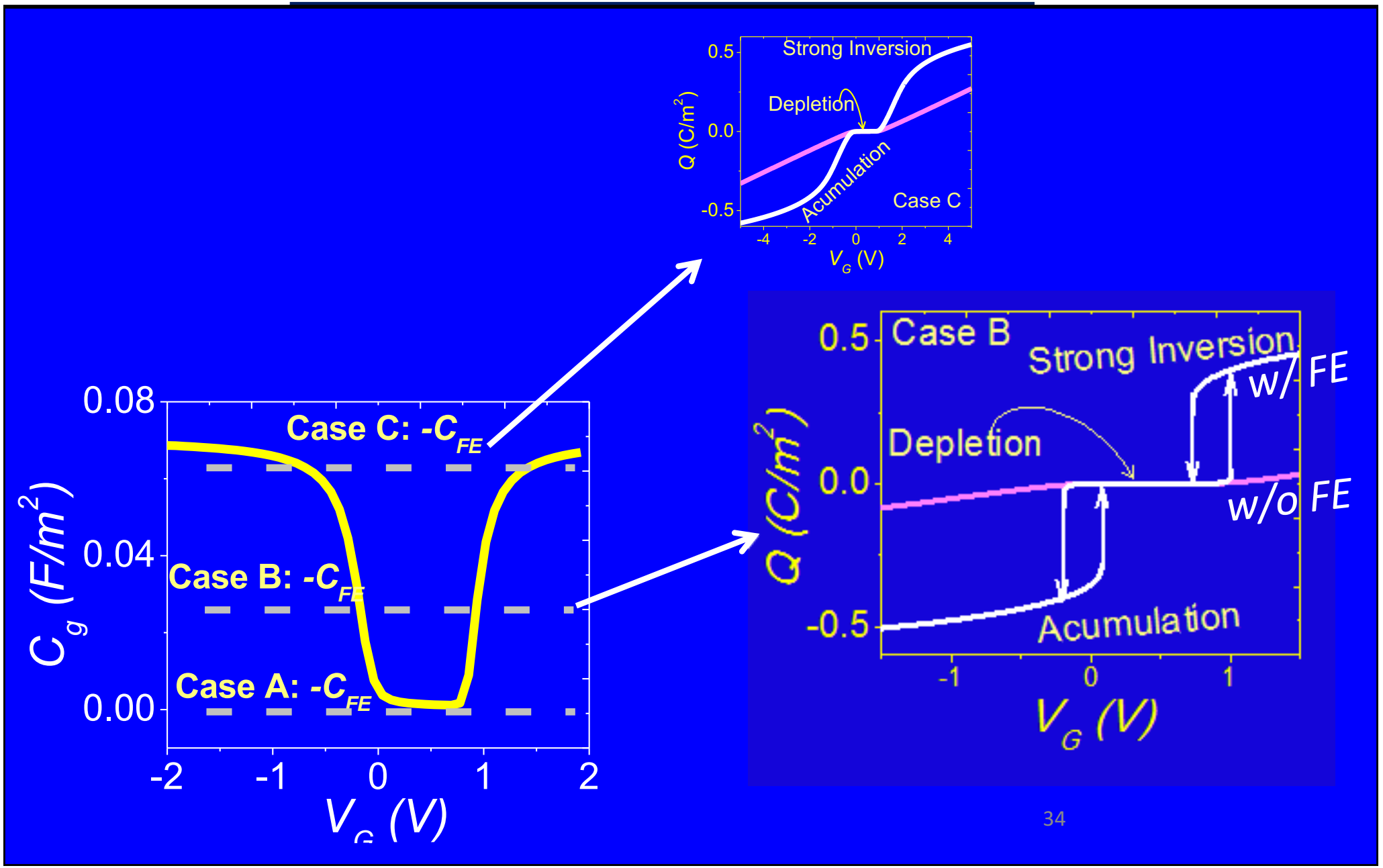
It may not be possible to match C_{FE} and C_{MOS} within the operational charge densities.

Khan et al. IEDM 2011.

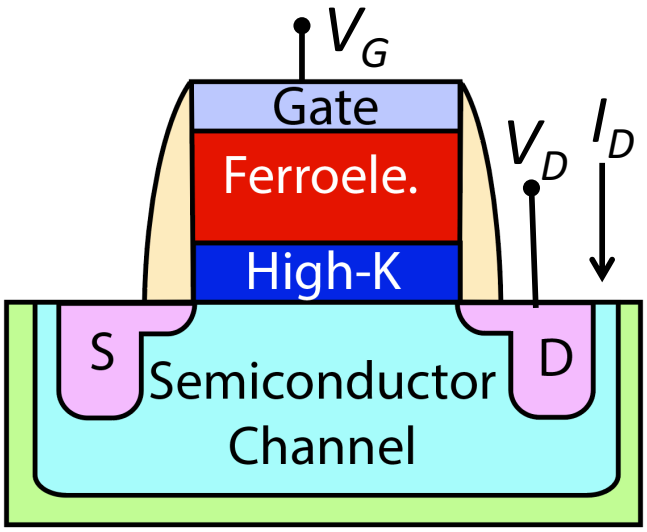
Capacitance Matching in a NCFET



Capacitance Matching in a NCFET



Physics of Negative Capacitance FET



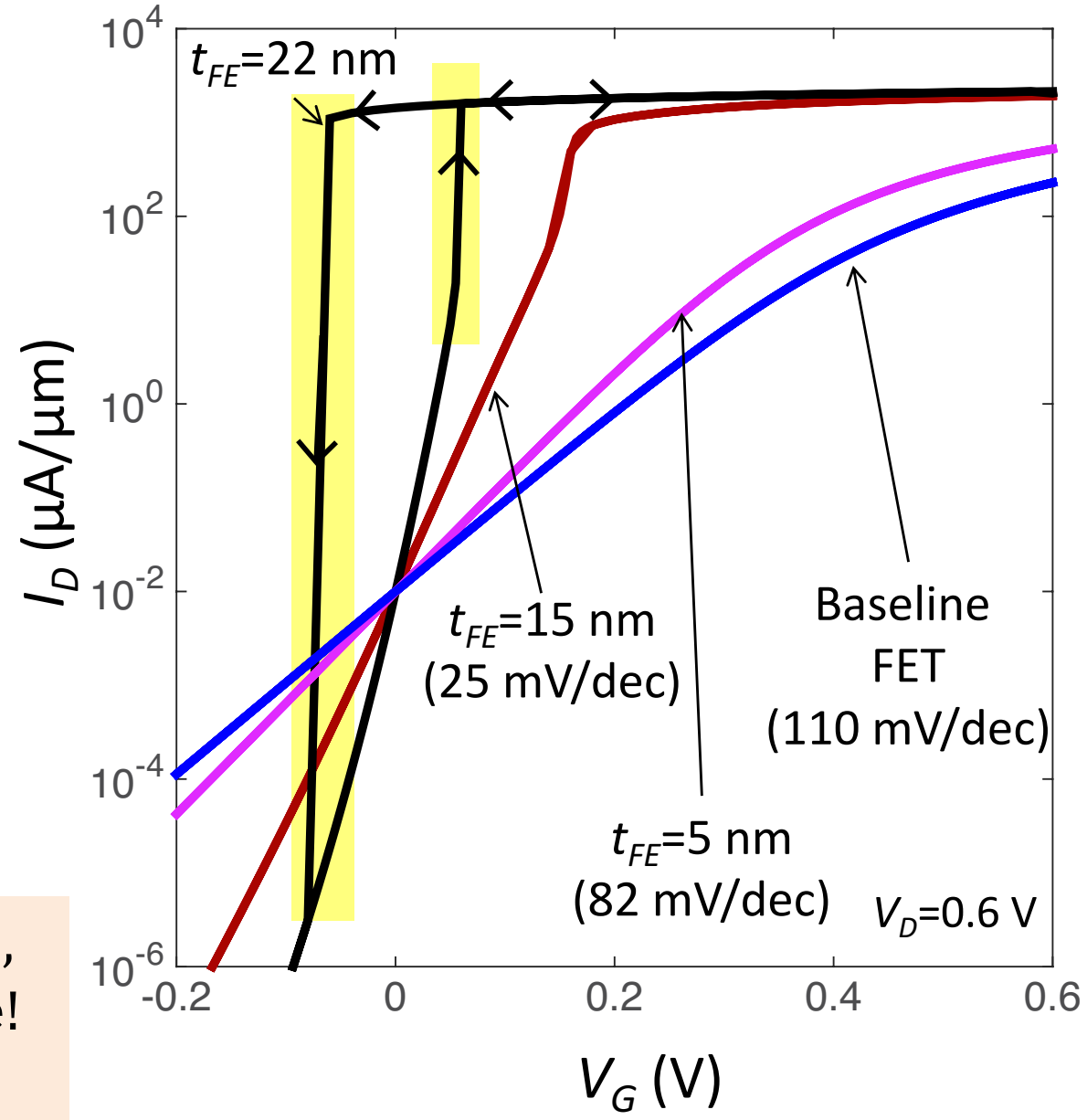
Ferroelectric Capacitance $|C_{FE}| = \sim \dfrac{P_o}{E_{FE} t_{FE}}$

Intel 45 nm node, MIT MVS Model

Collaboration with

Dimitri Antoniadis, MIT

Below a critical FE thickness, NCFET is a steep logic device! Above that it's a memory device!



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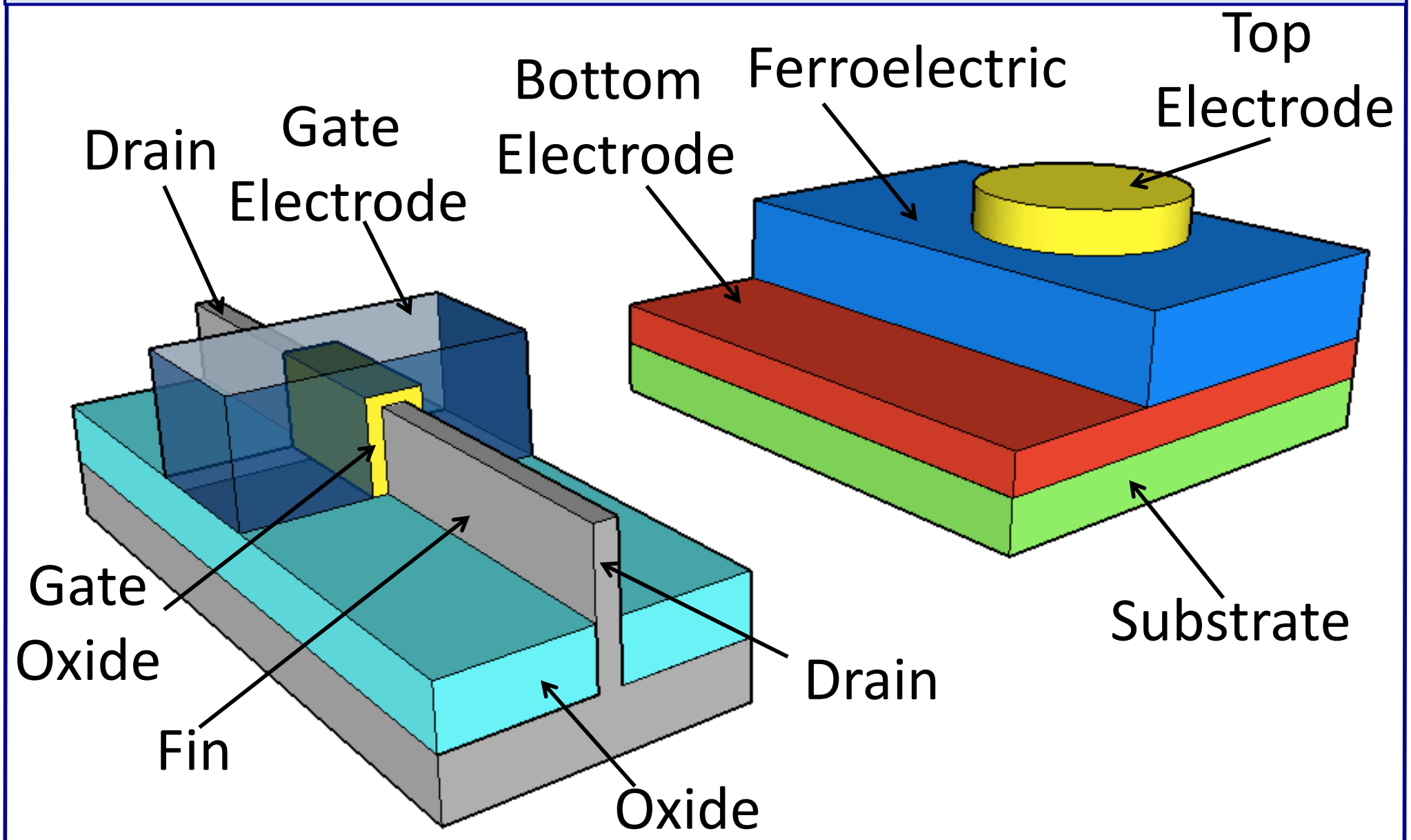
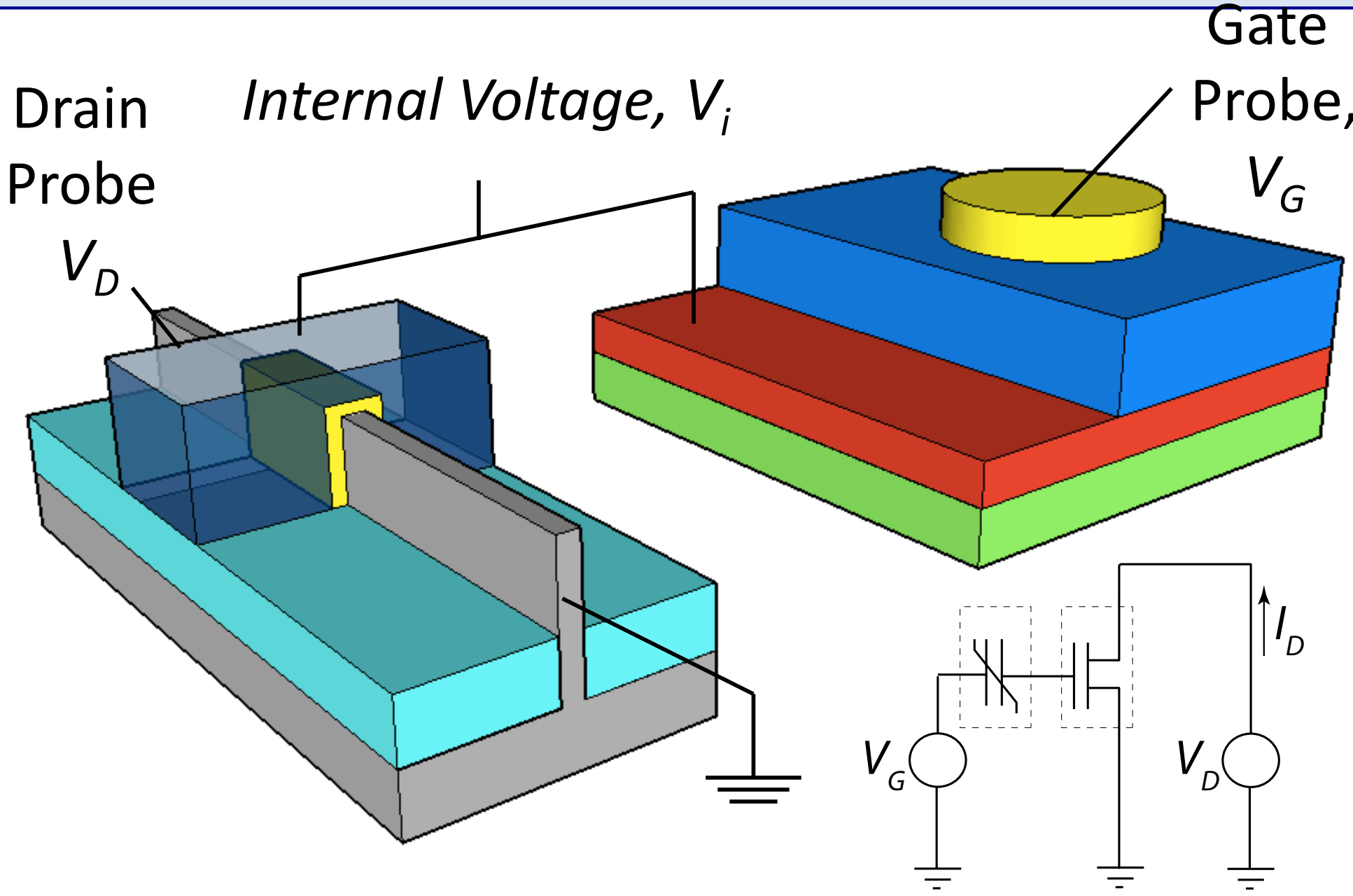
Externally Connected NC-FET



Georgia Tech

Externally Connected NC-FET



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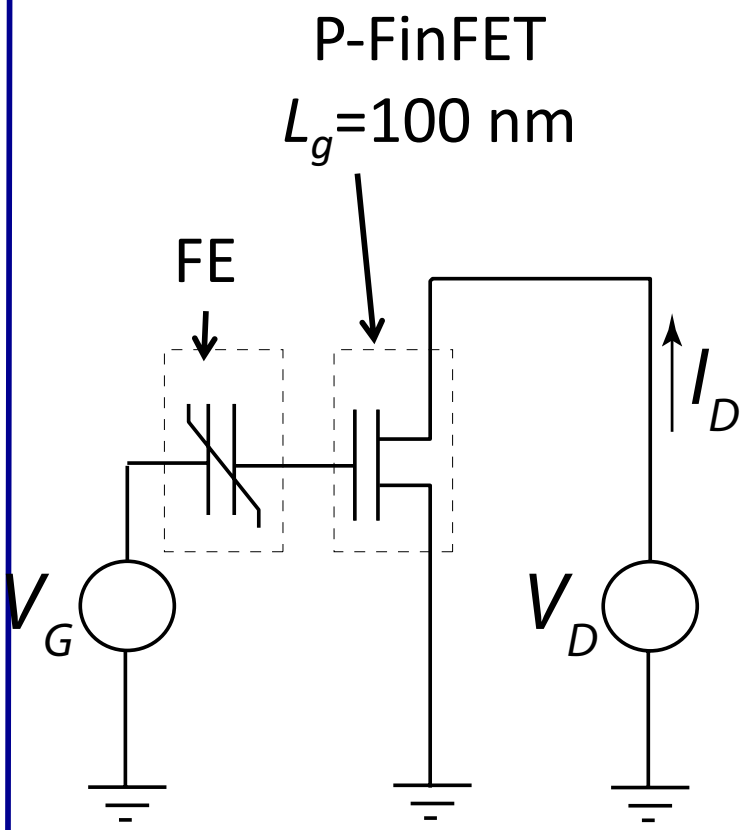
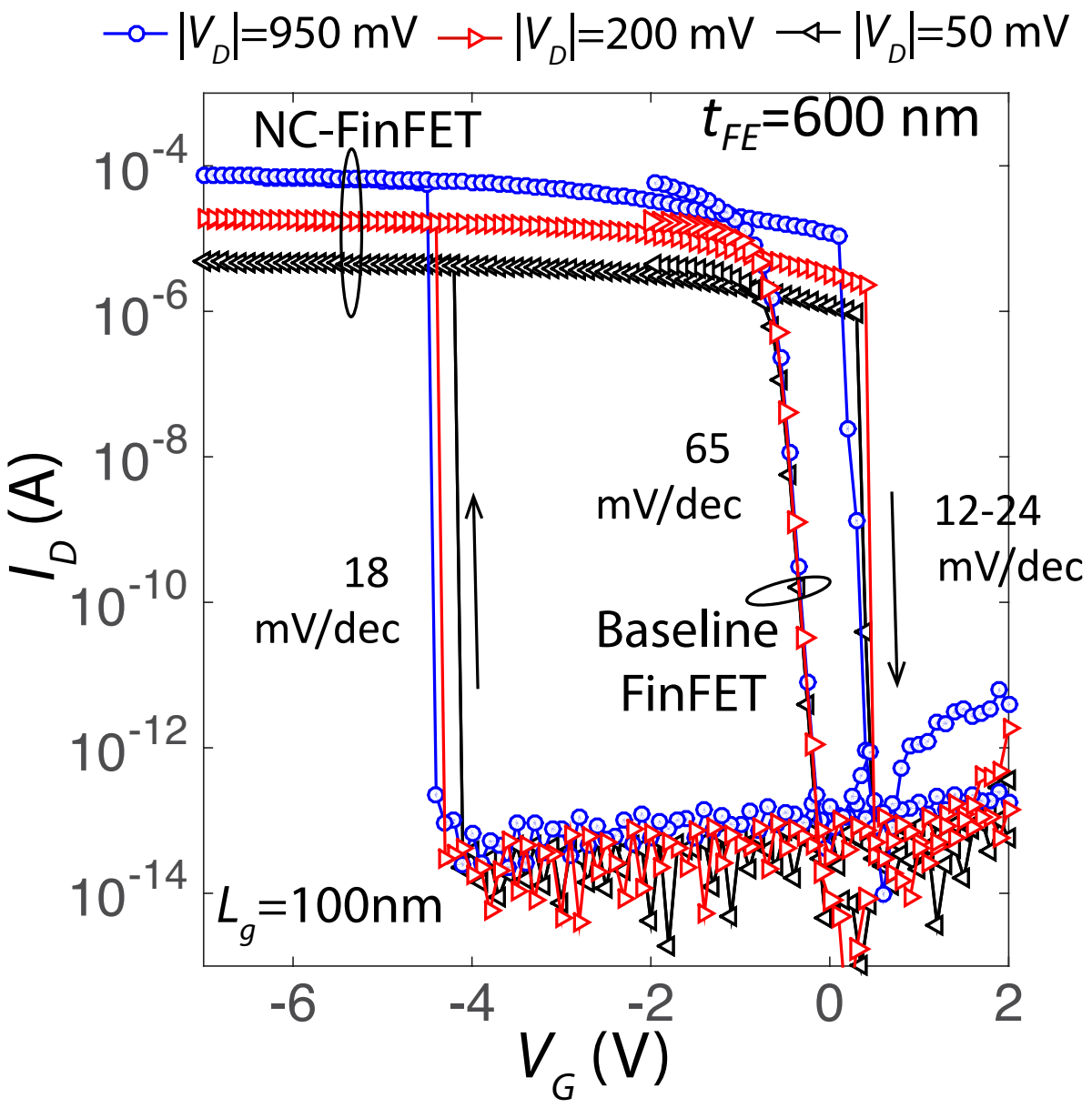
Externally Connected NC-FET





FinFET L_G=100 nm
Fin width=35 nm
Fin height=25 nm
EOT=1.4 nm

Khan et al. IEEE EDL 37, 111 (2016)

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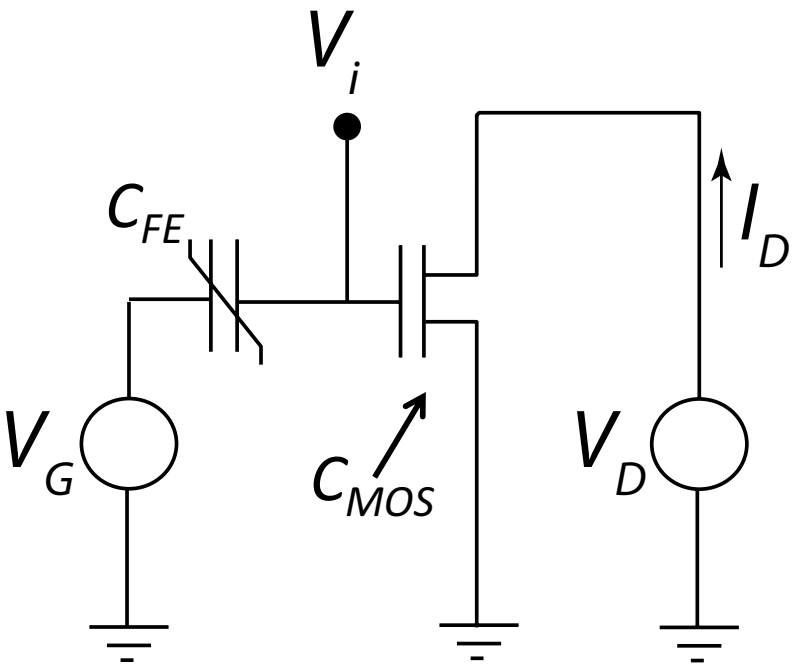
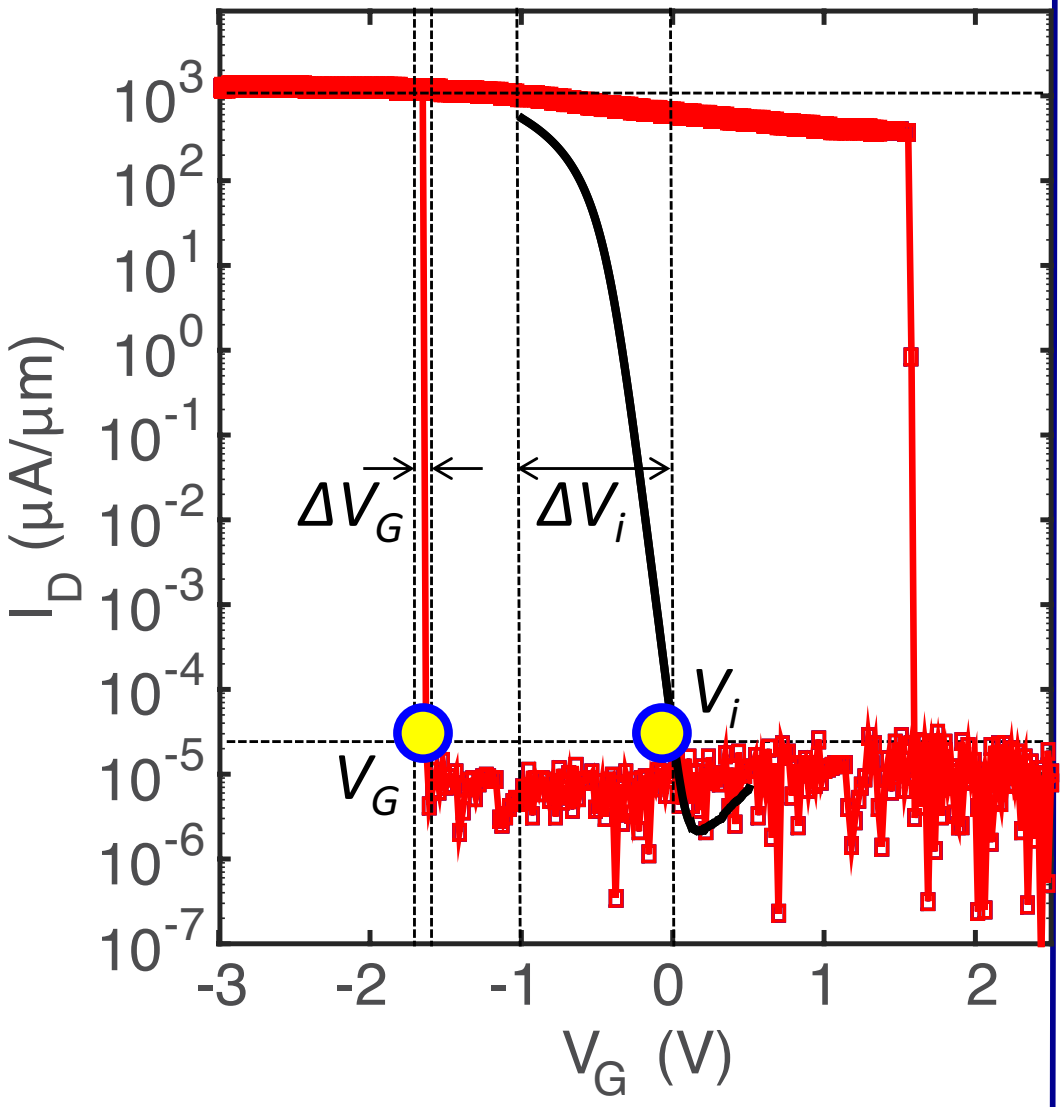
Negative Capacitance Transistors: Experiment



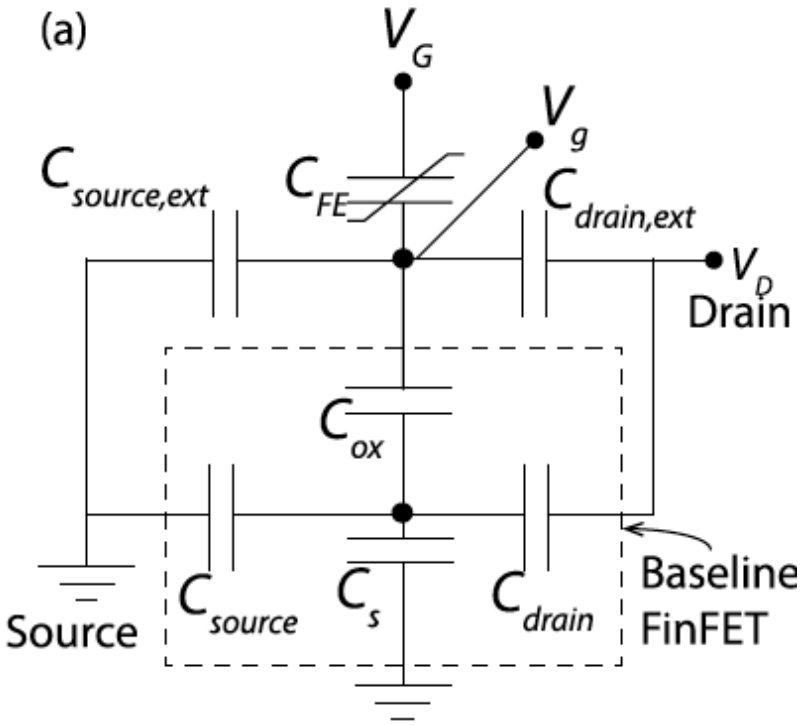
$$\frac{\Delta V_i}{\Delta V_G} > 1$$

$$\frac{\Delta V_i}{\Delta V_G} = \frac{C_{FE}}{C_{MOS}+C_{FE}} \quad > 1 \text{ only if } C_{FE}<0$$

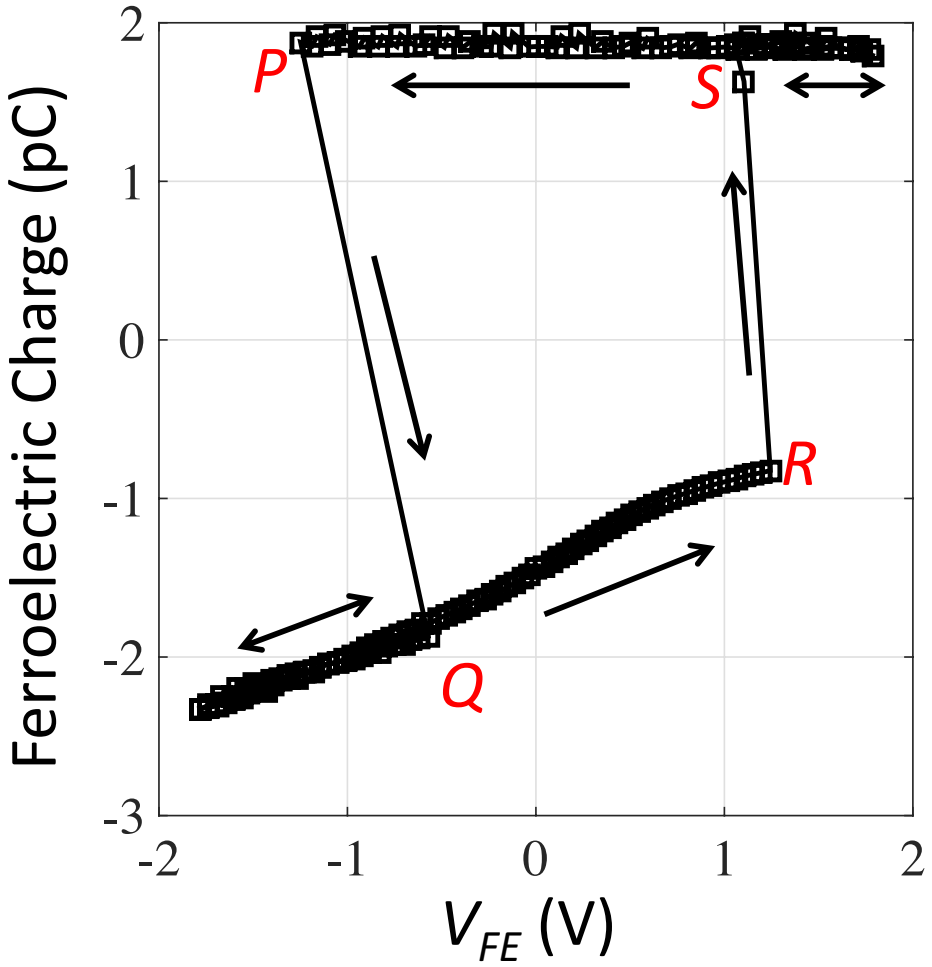


Sharp switching occurs due to ferroelectric negative capacitance!

Externally Connected NC-FET



Sharp switching occurs due to ferroelectric negative capacitance!



Negative Capacitance Regions: PQ and RS

Khan et al. IEEE EDL 37, 111 (2016)

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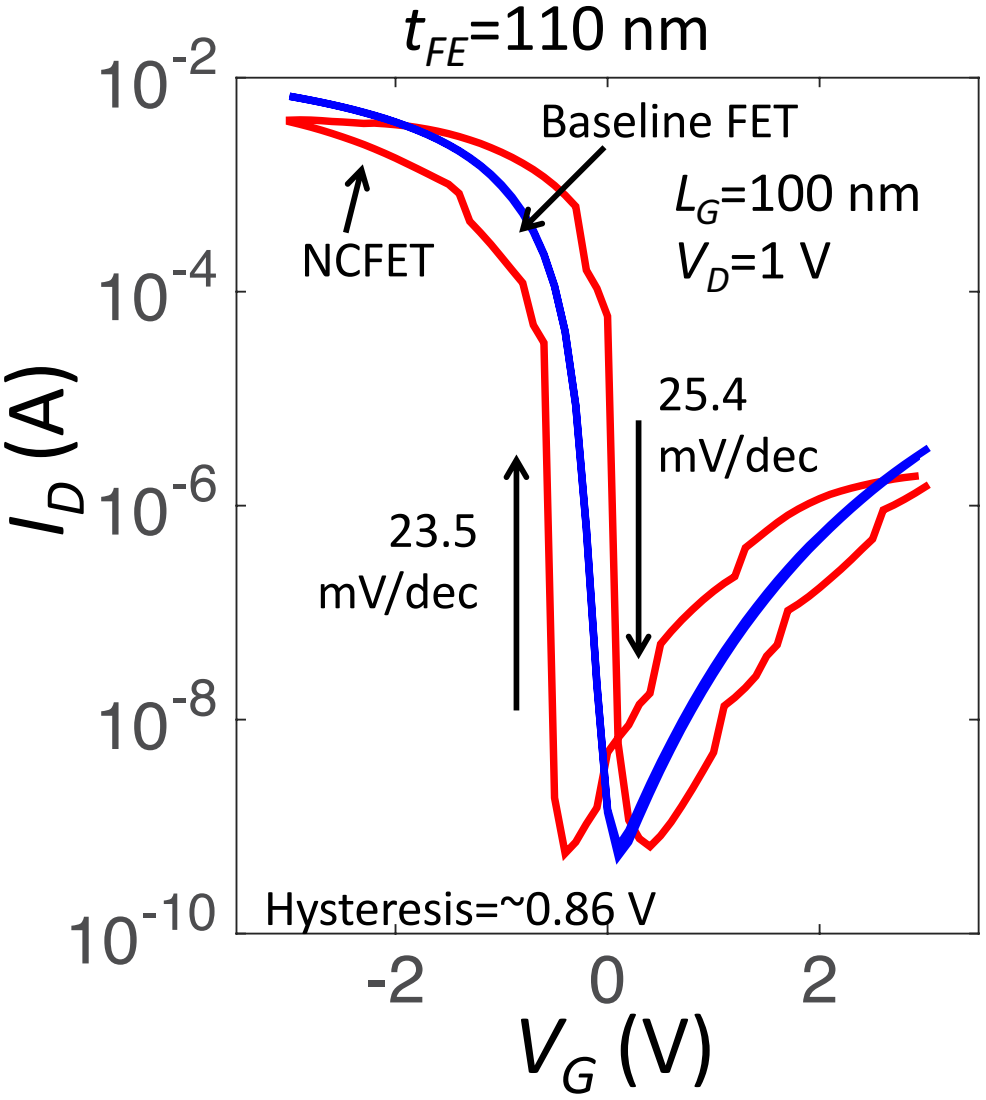
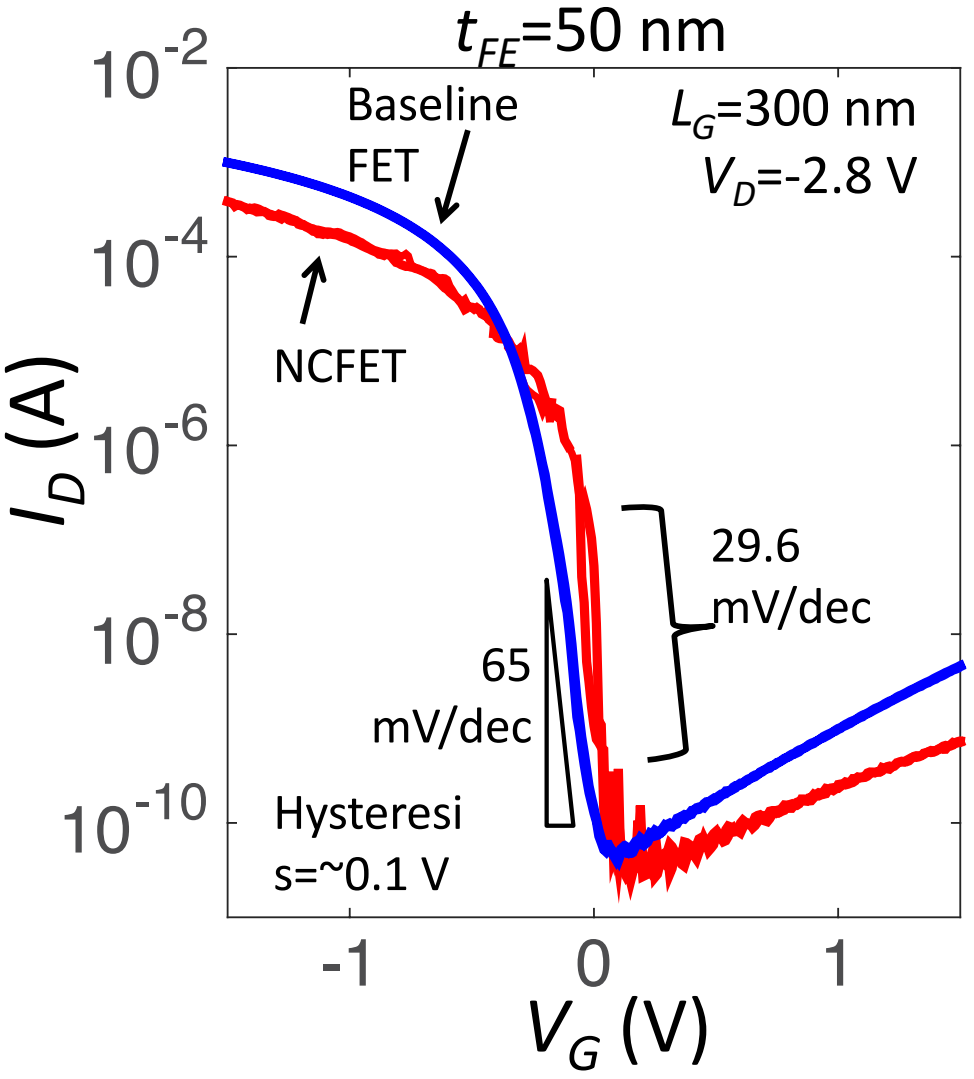
Externally Connected NC-FET





Negative capacitance can reduce subthreshold swing below 60 mV/dec!

Khan, Jo et al. (unpublished)

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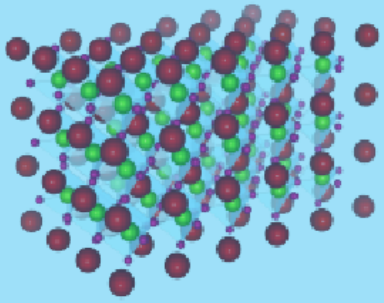
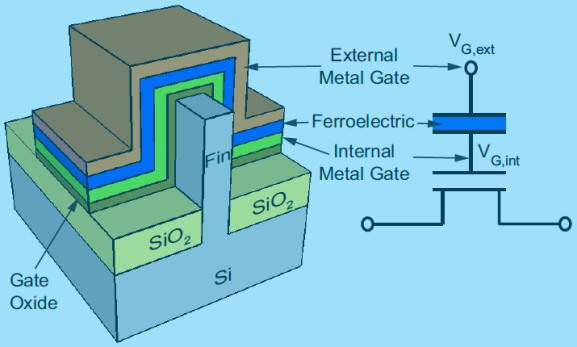
What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors



What do we need to know?

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Why am I excited
And
Why everyone can/should be excited?

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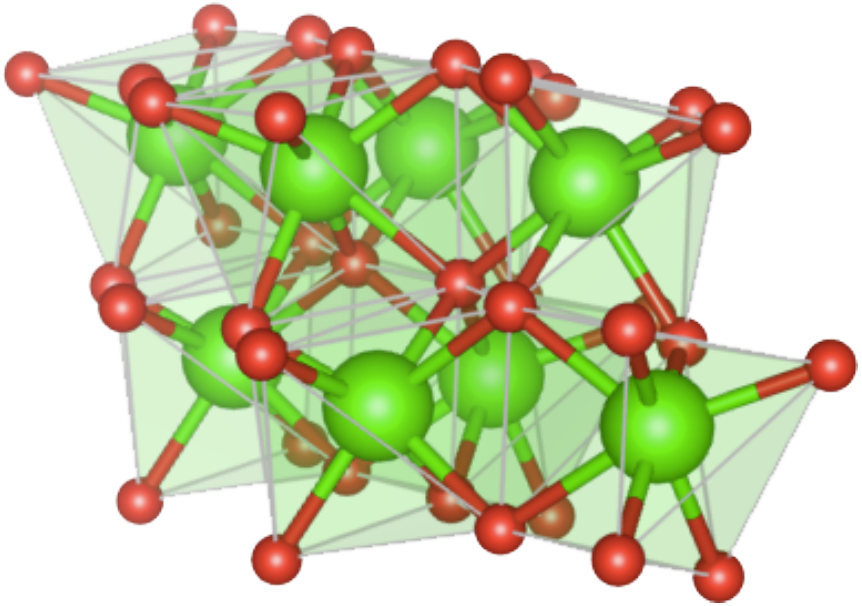
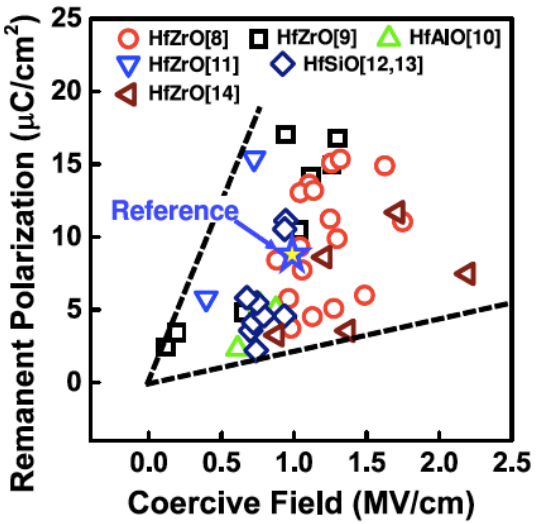
New CMOS Compatible Ferroelectrics

New class of ferroelectric materials have emerged which can be introduced in commercial fabs!



Controlled annealing in HfO_2 doped with Zr, Al, Si, Sr, Ti, La etc. induces a ferroelectric orthorhombic phase!

Thanks to NaMLab!



Negative Capacitance

$$|C_{FE}| = \sim \frac{P_o}{E_{FE} t_{FE}}$$

Kobayashi et al. AIP Adv. **6**, 025113 (2016)

Georgia Tech

Recent Demonstrations of NCFETs

Earliest:

1. A. Rusu et al. “Metal-ferroelectric-meta-oxide-semiconductor field effect transistor with sub-60mv/decade subthreshold swing and internal voltage amplification” IEDM 2010.

HfO_2 and Binary oxide based Ferroelectric:

1. Lee, et al., “Prospects for ferroelectric hfzrox fets with experimentally cet= 0.98 nm, ssfor= 42mv/dec, ssrev= 28mv/dec, switch-off 0.2 v, and hysteresis-free strategies,” IEDM 2015.
2. Li et al., “Sub-60mv-swing negative-capacitance finfet without hysteresis,” IEDM 2015.
3. Lee et al. “Physical thickness 1. x nm ferroelectric HfZrOx negative capacitance FETs,” IEDM 2016
4. Chang et al. “Impact of La2O3/InGaAs MOS interface on InGaAs mosfet performance and its application to InGaAs negative capacitance FET,” IEDM 2016

Perovskite ferroelectrics:

S. Dasgupta et al. “Sub-kT/q switching in strong inversion in PbZr0:52Ti0:48O3 gated negative capacitance FETs,” IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, vol. 1, pp. 43–48, 2015.

Georgia Tech

Recent Demonstrations of NCFETs

Externally connected NCFET:

1. J. Jo et al. “Negative capacitance in organic/ferroelectric capacitor to implement steep switching mos devices,” Nano letters, 15, 4553, 2015.
2. J. Jo and C. Shin, “Negative capacitance field effect transistor with hysteresis-free sub-60-mv/decade switching,” IEEE Electron Device Letters, vol. 37, no. 3, pp. 245–248, 2016.
3. E. Ko, J. W. Lee, and C. Shin, “Negative capacitance finfet with sub-20-mv/decade subthreshold slope and minimal hysteresis of 0.48 v,” IEEE Electron Device Letters, vol. 38, no. 4, pp. 418–421, 2017.
4. A. Khan, et al. , “Negative capacitance in short channel finfets externally connected to an epitaxial ferroelectric capacitor,” IEEE Electron Device Letters, vol. 37, no. 1, pp. 111–114, 2016.

Recent-2-D NCFET:

1. Nourbakhsh et al. , “Subthreshold swing improvement in mos_2 transistors by the negative-capacitance effect in a ferroelectric al-doped-hfo_2/hfo_2 gate dielectric stack,” Nanoscale, vol. 9, no. 18, pp. 6122–6127, 2017
2. McGuire et al. , “Sub-60 mv/decade switching in 2d negative capacitance field effect transistors with integrated ferroelectric polymer,” Applied Physics Letters, vol. 109, no. 9, p. 093101, 2016.
3. McGuire, et al. “Sustained sub-60 mv/decade switching via the negative capacitance effect in MoS2 transistors,” Nano Letters, 2017.
4. Si et al. “Steep Slope MoS2 2D Transistors: Negative Capacitance and Negative Differential Resistance.” https://arxiv.org/abs/1704.06865

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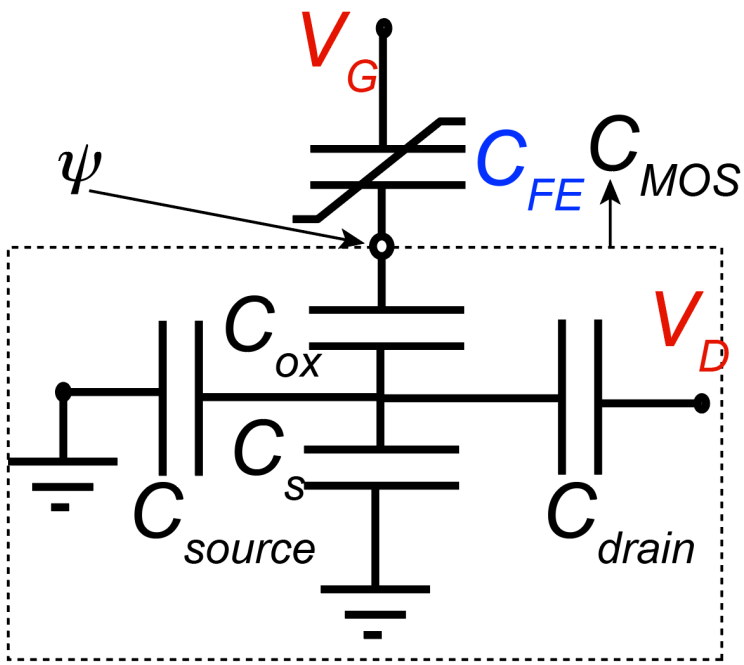
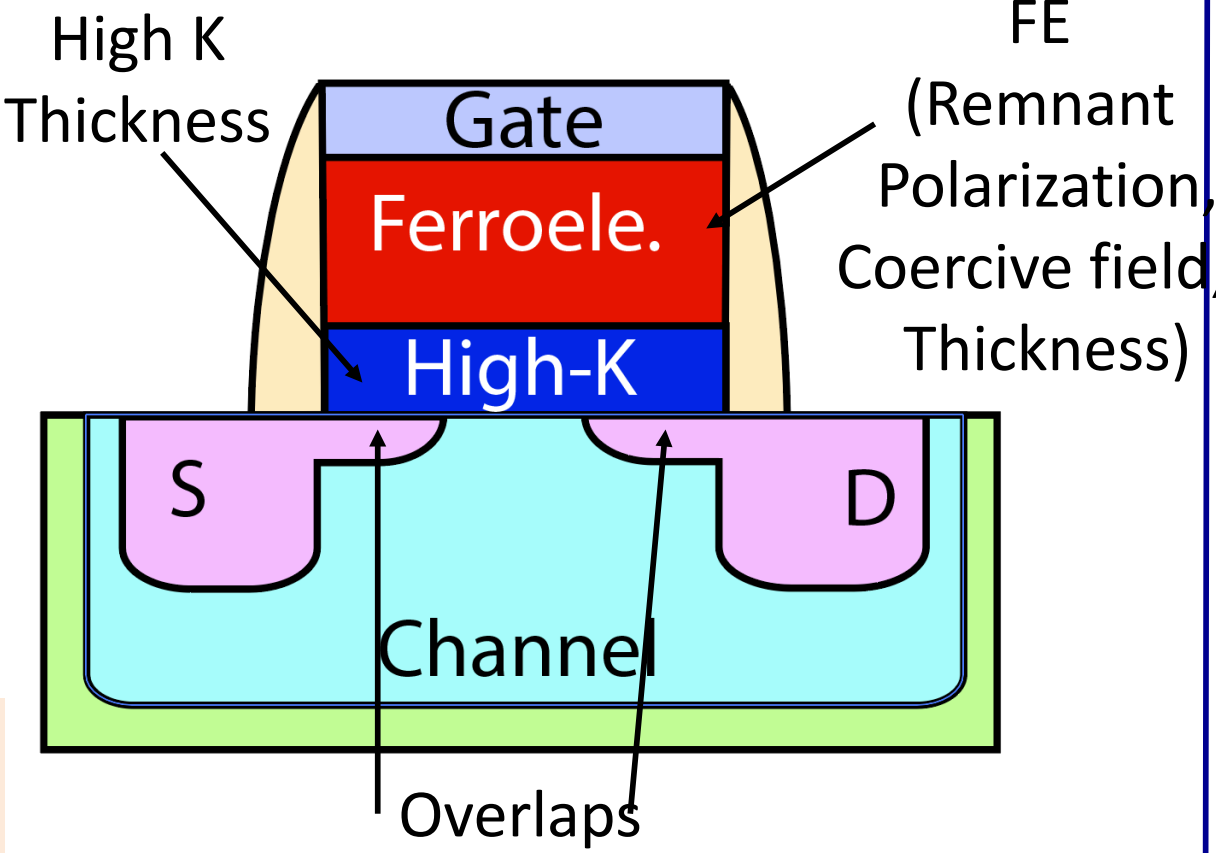
Design of NCFETs

How to design an NCFET?
~0 mV/decade swing?





Ideal Switch: ~0 mV/decade

$|C_{FE}| \approx C_{MOS}, |C_{FE}| > C_{MOS}$

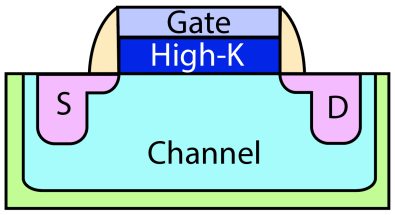
Subthreshold Swing $S^{NC} = S^{original} \times (1 - \frac{C_{MOS}}{|C_{FE}|})$

Khan et al. IEDM 2011
Yeung, Khan et al. VLSI-TSA 2013
Hu, Khan et al. DRC 2015
Cheng-I, Khan et al. IEEE T-ED 2016

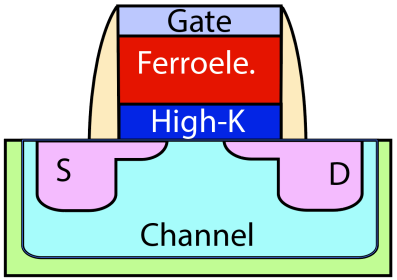
Georgia Tech

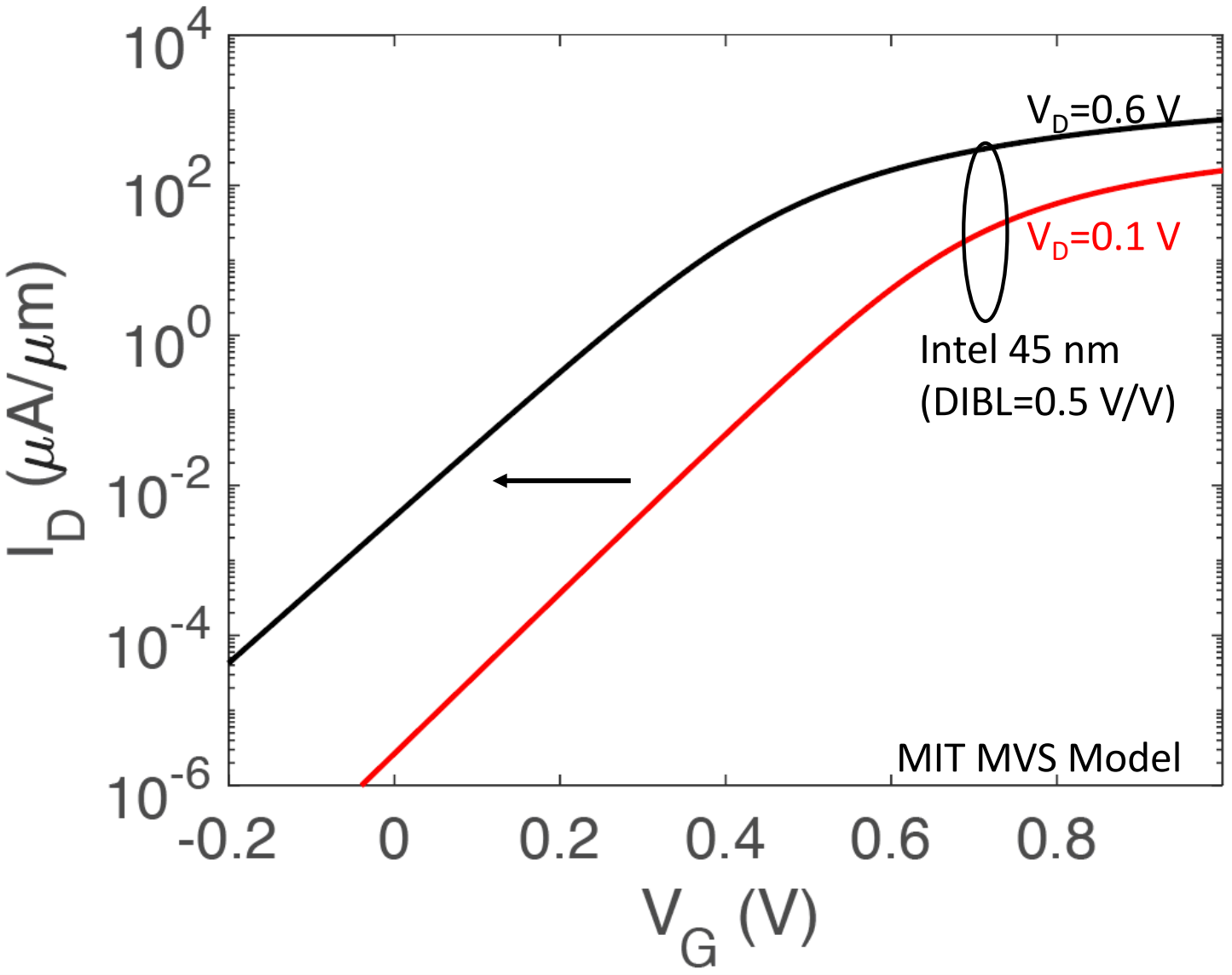
Reverse DIBL in NCFETs

Baseline FET
(Intel 45 nm)



Baseline FET
(Intel 45 nm
+9 nm FE)





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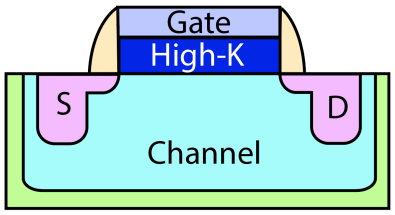
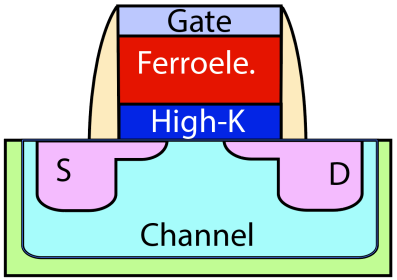
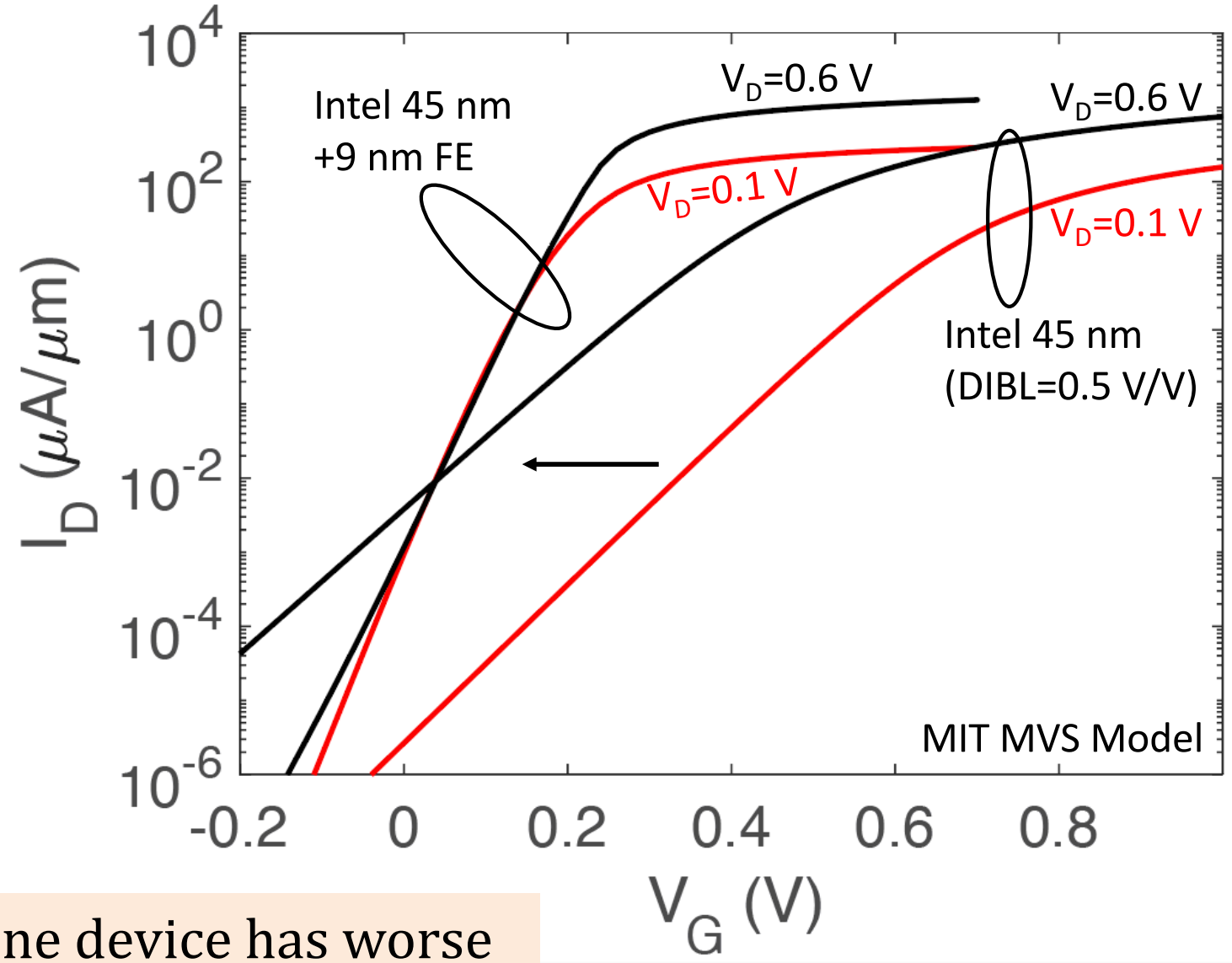
Reverse DIBL in NCFETs

Baseline FET
(Intel 45 nm)



Baseline FET
(Intel 45 nm
+9 nm FE)





If the baseline device has worse DIBL, it is beneficial for NCFET!

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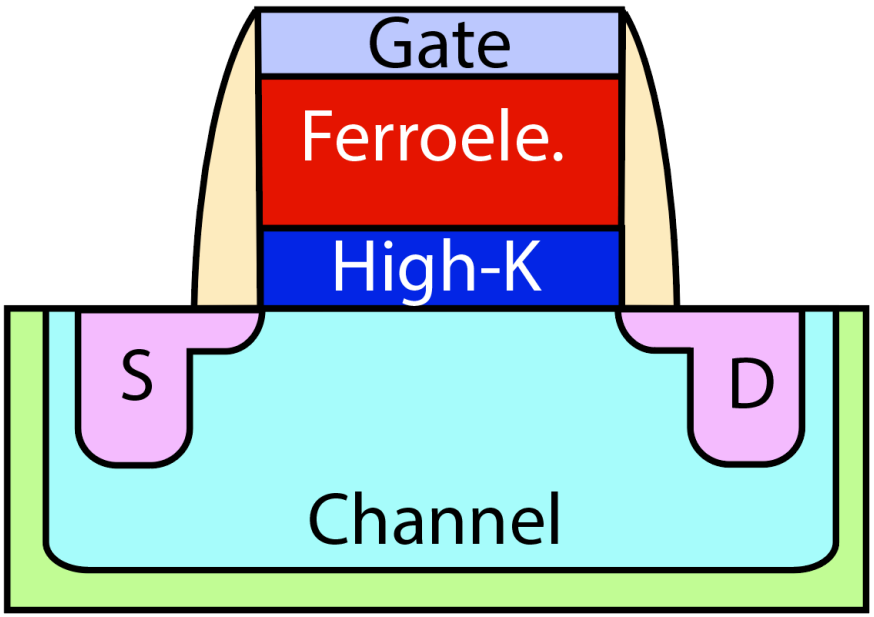
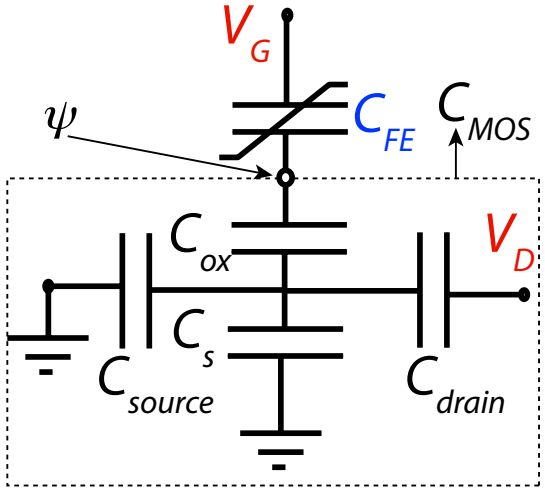
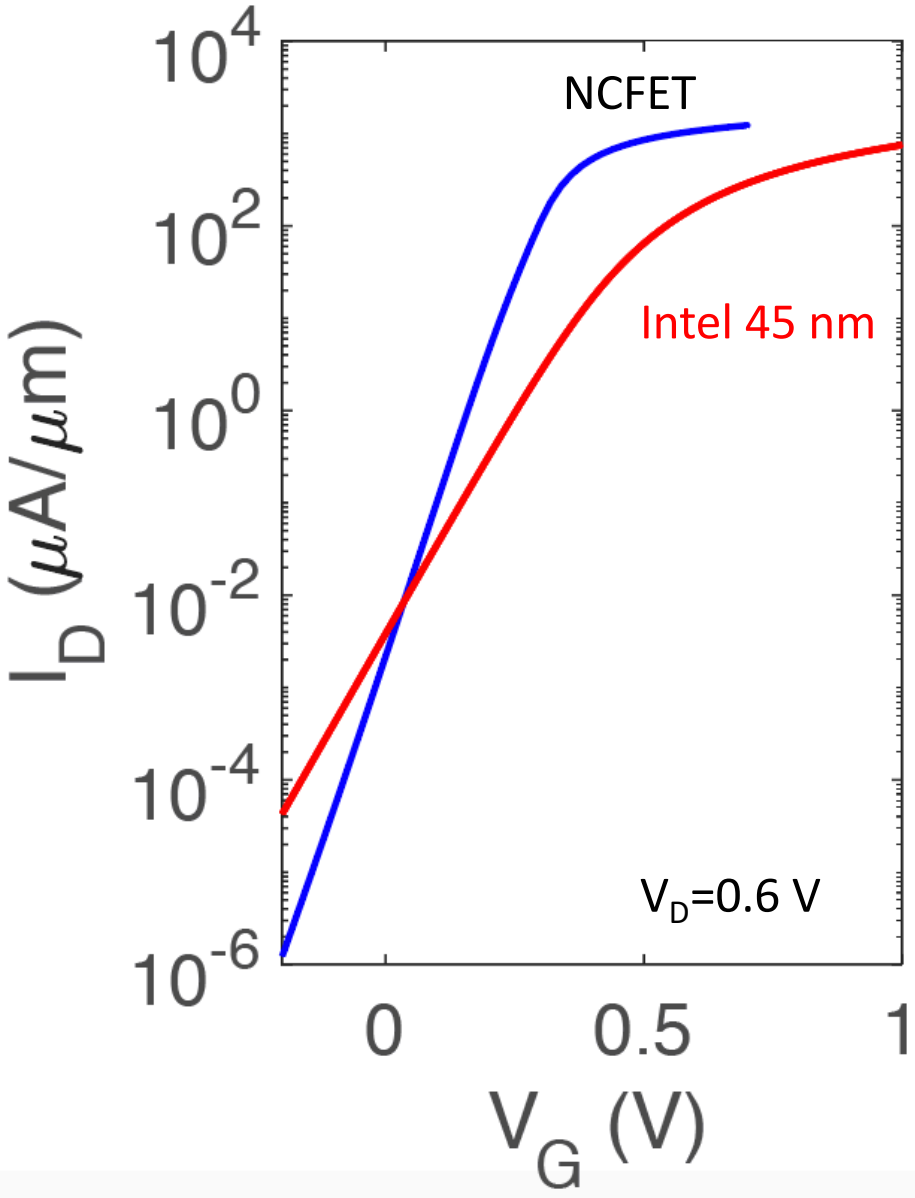
Overlap Capacitance







MIT MVS Model

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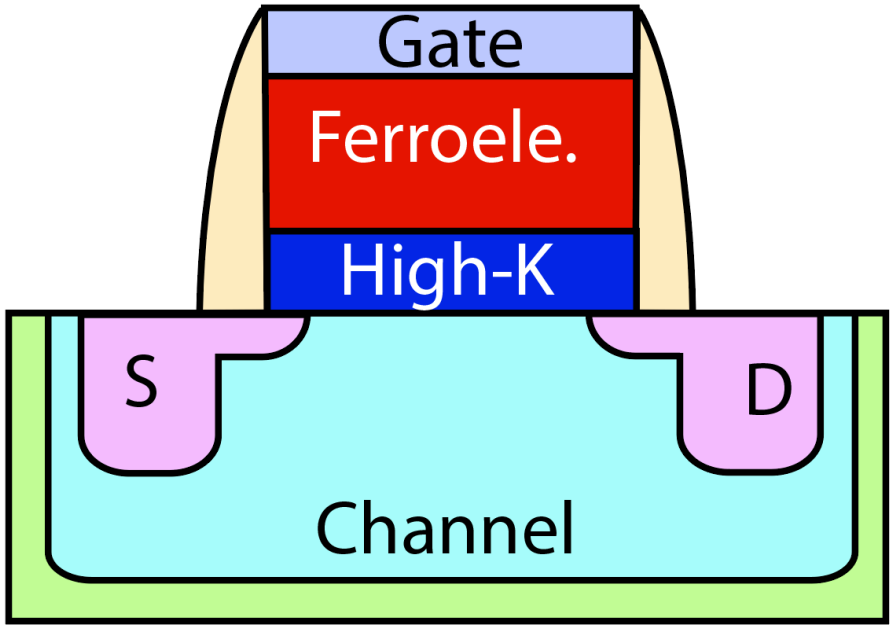
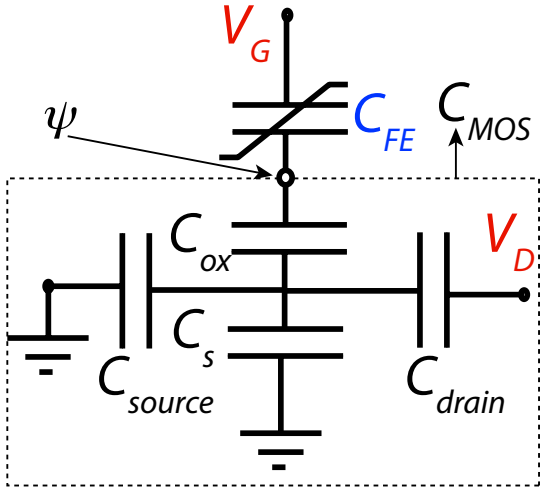
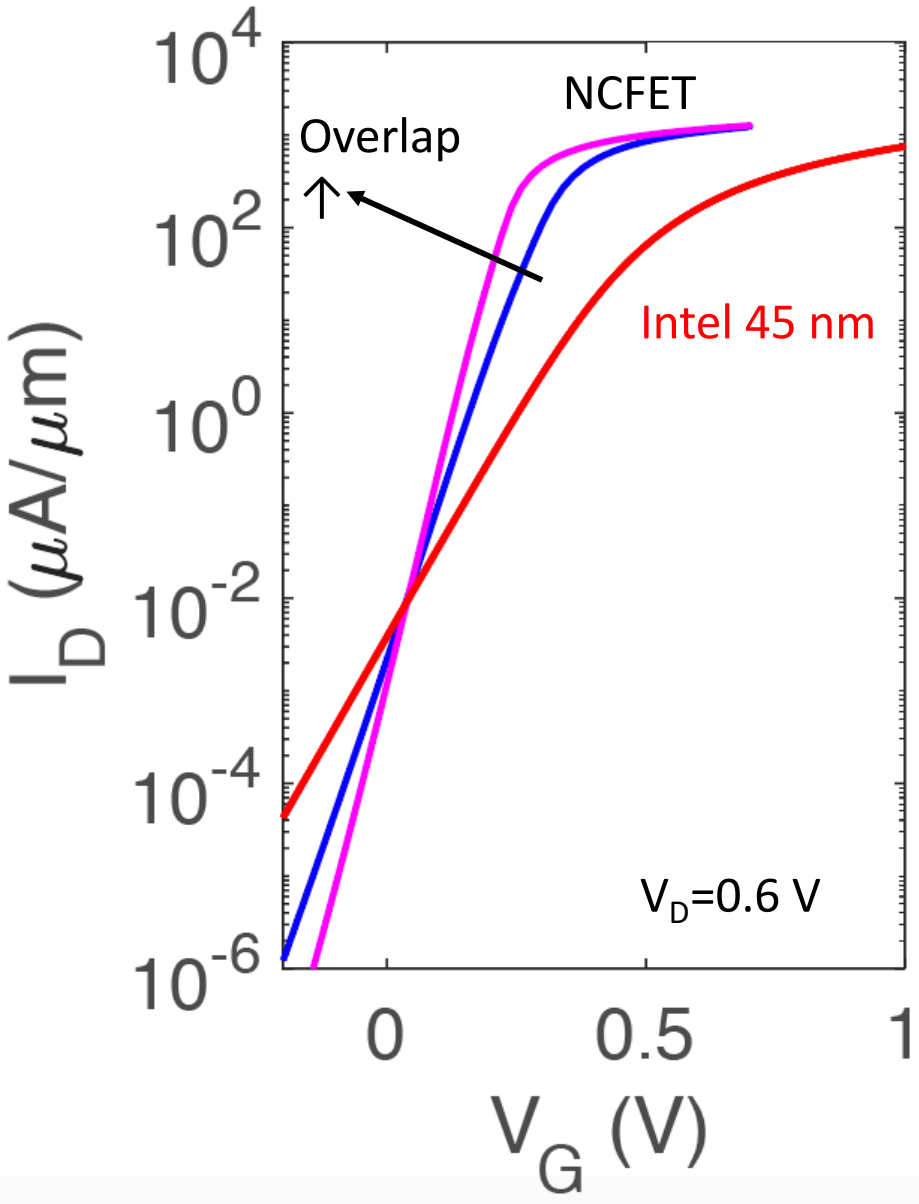
Overlap Capacitance





C_{drain} increases! C_{MOS} comes closer to C_{FE}!



MIT MVS Model

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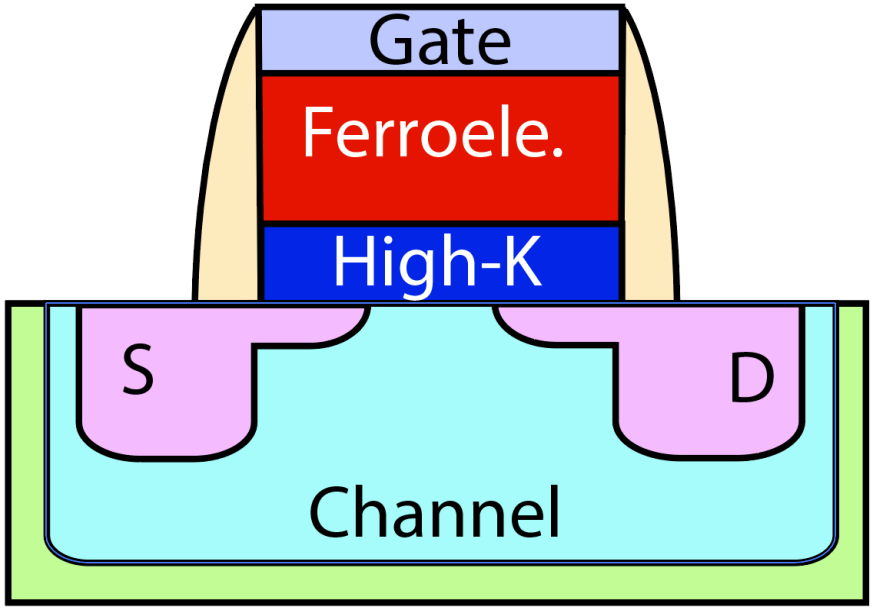
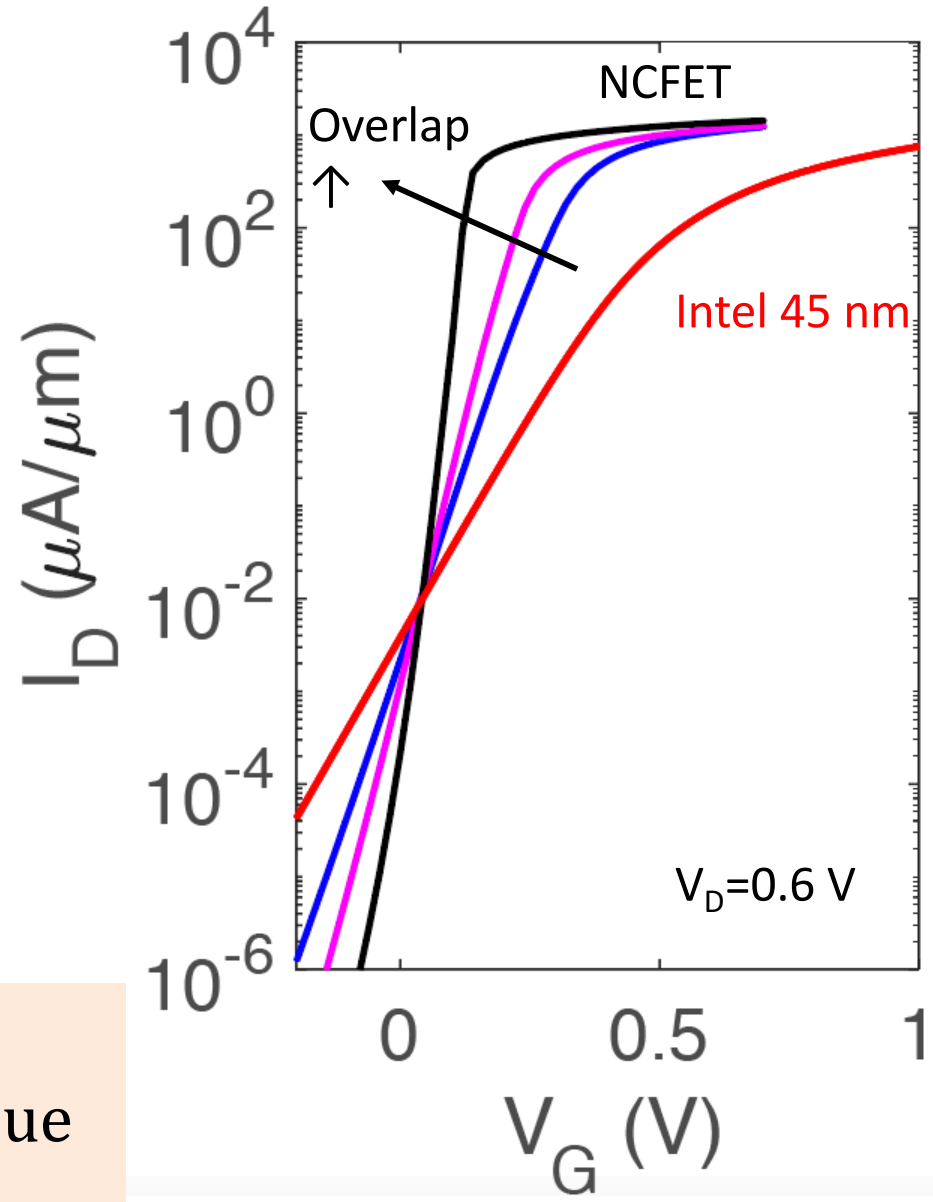
Overlap Capacitance





Overlap capacitance helps to improve NCFET performance due to capacitance matching!

MIT MVS Model

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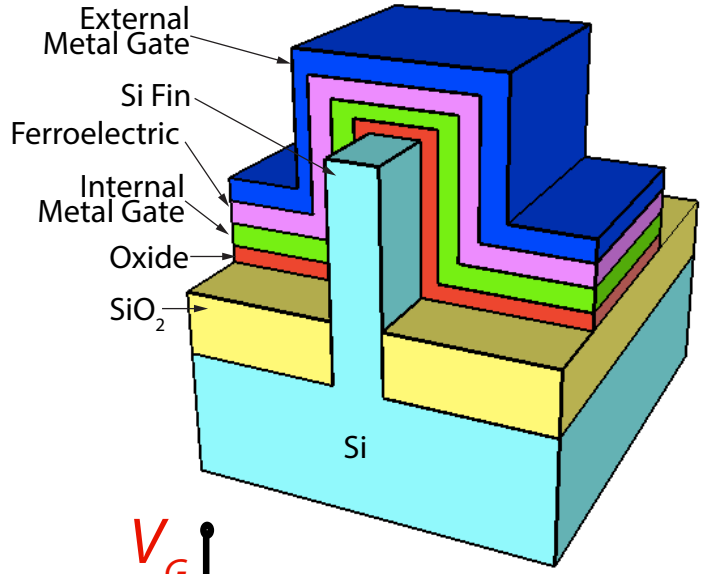
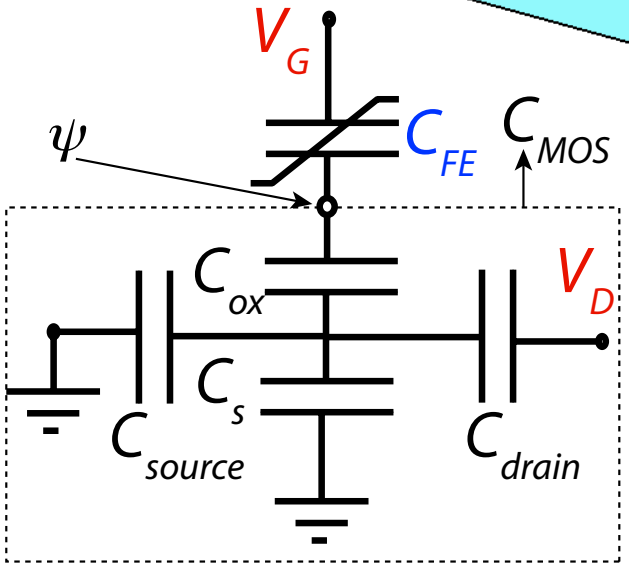
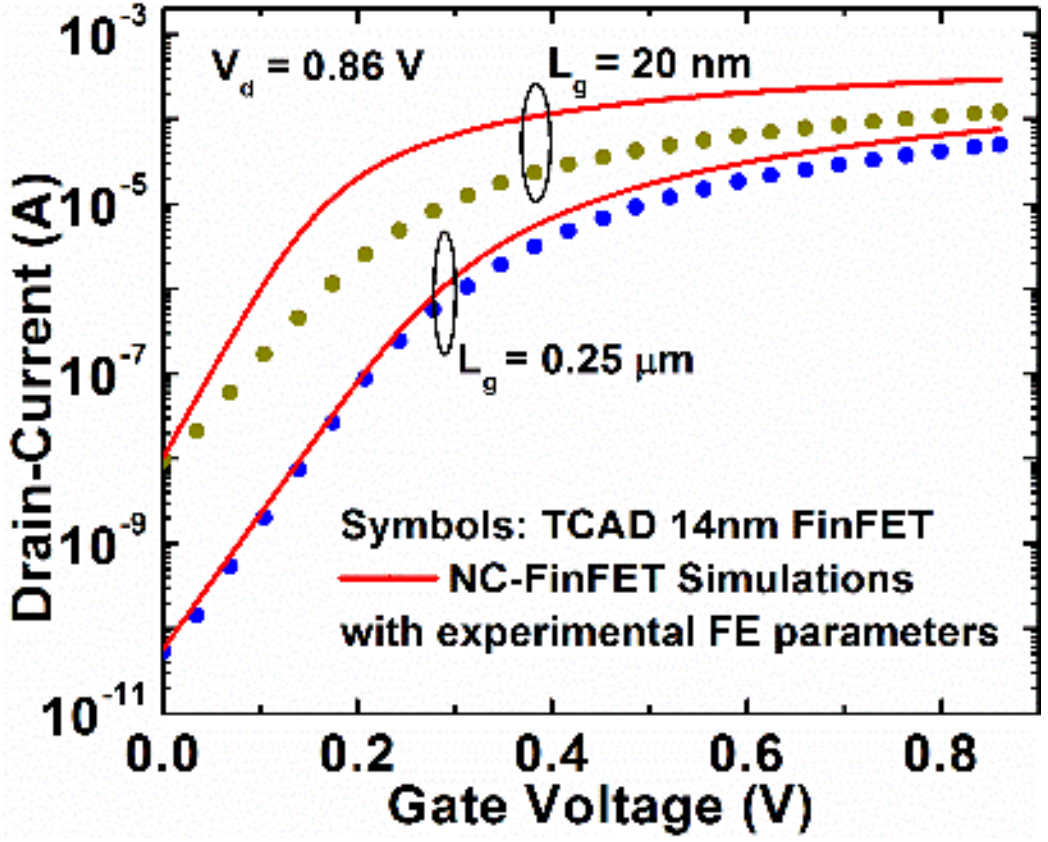
Short L_g Negative Capacitance Transistors







BSIM

Improvement of Subthreshold Swing is higher in short channel transistors!

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Design of NCFETs

How to design an NCFET?
~0 mV/decade swing?

1. A baseline device with large DIBL can result in good DIBL characteristics of NCFETs!
2. Don't reduce high-K dielectric thickness to zero! You need it to reduce non-linearity of MOS capacitance!
3. You may see NDR in ID-VD characteristics! In short channel NCFET that will allow you to get flat saturation characteristics!
4. NCFET becomes better at short channel lengths!

The effects that tend to degrade MOSFET performance improve the performance of NCFETs!

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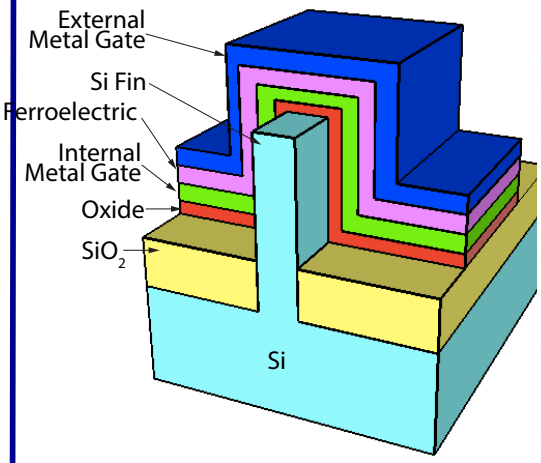
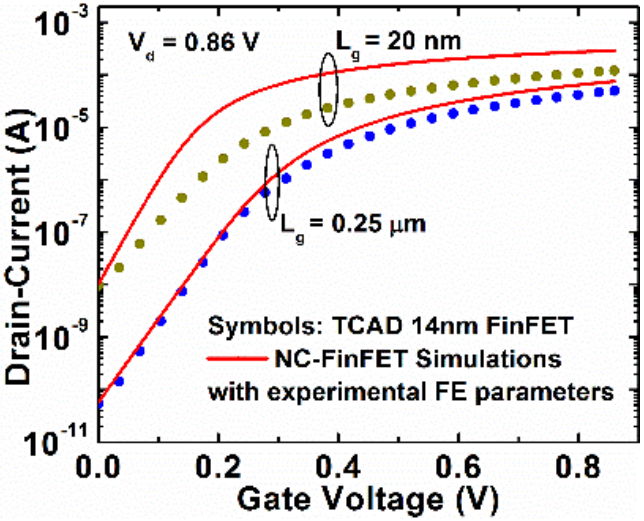
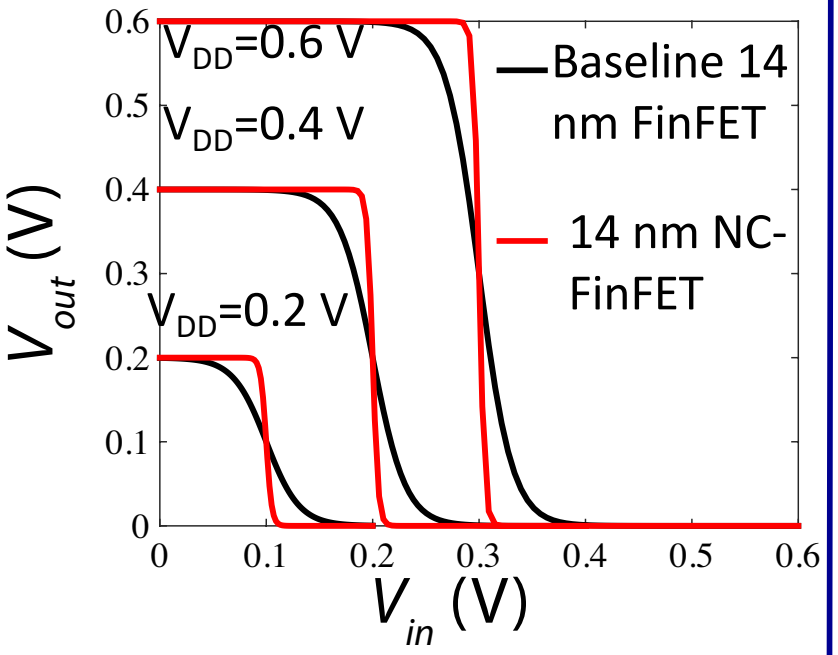
Performance Projection of NCFETs

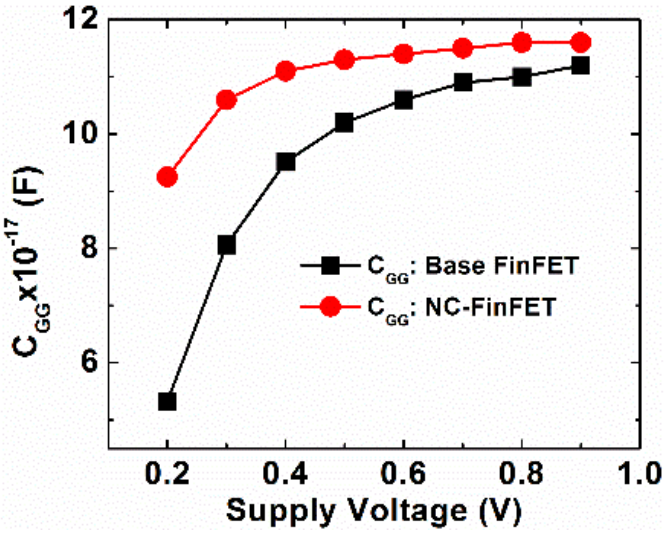
14 nm NC-FinFET Model



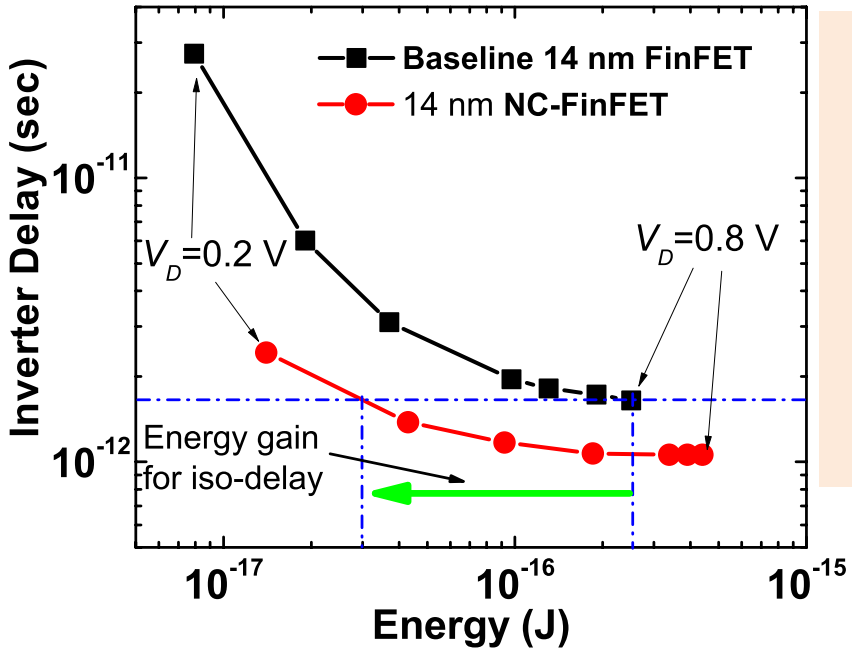




Experiments: Li et al. IEDM 2015



Khandelwal VLSI Symp 2016



Energy dissipation due to short circuit current also decreases!

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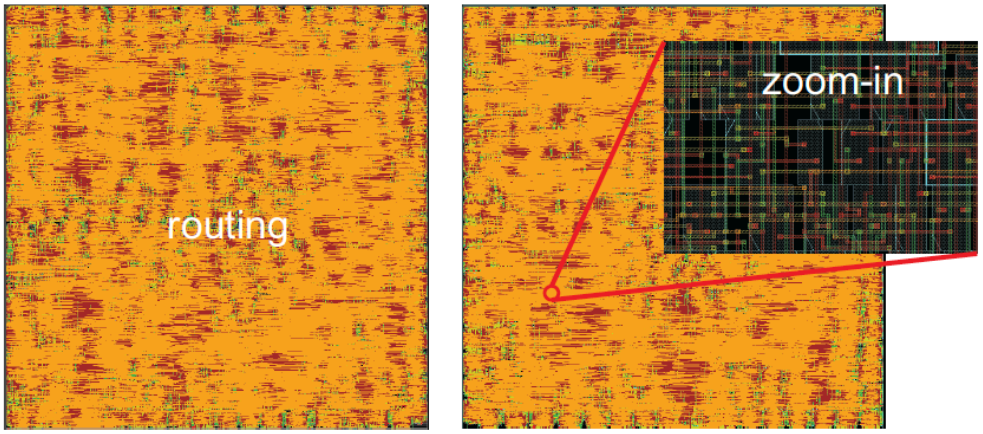
Full Chip Power Benefits of NCFETs

- Advanced Encryption Core (AES) Engine: ~120,000 cells, ~800,000 devices
- Iso-performance analysis (2 GHz)
- Steps:
  - 14 nm NCFET BSIM models based on experimental results (Li et al. IEDM 2015)
  - NCFET-based standard-cell library characterization
  - Full-chip NCFET-based GDSII-level design implementations



baseline FET @ 0.8V NCFET @ 0.4V

Samal, Khandelwal, Khan, Hu, Salahuddin, Lim. ISLPED 2017

Device	VDD	# Cells	Cell Area (mm^2)	Wirelength (m)	Total Cap (pF)	WNS (ps)	Power (mW)			
							Switching	Internal	Leakage	Total
baseline FET	**0.8V**	127,757	0.043	1.02	686.8	6.3	57.3	91.4	6.2	154.9
NCFET	**0.5V**	128,438	0.043	1.03	992.3 (+44%)	19.2	33.6	40.4	0.9	74.9 (-52%)
	0.4V	135,235	0.047	1.01	933.6 (+36%)	0.9	20.1	23.9	0.9	44.9 **(-71%)**
	0.3V	152,328	0.053	1.02	927.4 (+35%)	**-77.5**	10.5	12.9	0.8	24.2 (-84%)

ISO-PERFORMANCE (2GHZ) AES DESIGNS USING NCFET AT VARIOUS VDD LEVELS.

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Speed

What is the speed of negative capacitance mechanisms?

~220 ps in micron size PNZT capacitors: << Don't get confused!
Li et al. Ultrafast polarization switching in thin-film ferroelectrics. Applied Physics Letters 84, 1175 (2004).

The PNZT capacitor was 5 um x 5 um x thickness=200 nm. Switching speed scales with area when limited by domain wall velocity.
With relevant FinFET dimensions (<~20 nm x ~100 nm x <4 nm=Lg x (2*fin height+fin width) x FE thickness), you would get a switching speed of 16 fs.

With extracted damping and mass terms from spectroscopic measurements for HfO2, the characteristics time scale for ferroelectric switching in the domain nucleation limit should be around 220 fs.

Chatterjee et al. Intrinsic Speed Limit of Negative Capacitance Transistors EDL 2017http://ieeexplore.ieee.org/abstract/document/7990241/**.**

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Acknowledgements

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FCRP MSD Center

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Negative Capacitance:

What do we know and

What do we need to know?

QUESTIONS

&

COMMENTS

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