Ferroelectric NAND Flash for Radiation-Tolerant Semiconductor Storage

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Georgia Tech

ELON MUSK

WORLD ECONOMIC FORUM • JAN 2026

“THE LOWEST-COST PLACE TO PUT AI WILL BE IN SPACE.

“...and that will be true within two years, maybe three at the latest.”

SPACEX

1,000,000

SATELLITES — FCC APPLICATION

Proposed orbital data-center system

STARCLOUD

88,000

PROPOSED SATELLITES

1 × NVIDIA H100 already flown

GRID INDEPENDENCE • NEAR-CONTINUOUS SOLAR • PROCESS AT THE SOURCE • LATENCY • AUTONOMY • SOVEREIGNTY

IEEE SPECTRUM • JULY 2026

AT ELON SCALE, AI IN SPACE HITS PHYSICS AND LOGISTICS.

A million-satellite cloud is not the same problem as useful AI at the orbital edge.

KEY CHALLENGES AT 1,000,000-SATELLITE SCALE

THERMAL	No convection; one 700 W H100 needs ~1.4 m^2 of radiator.
SCALE-UP	~16,666 Starship launches—plus million-unit manufacturing.
RELIABILITY	Radiation, debris and degradation demand shielding and servicing.

WHAT SPECTRUM SAYS IS REAL NOW

01 EARTH-OBSERVATION INTELLIGENCE

Process SAR and hyperspectral data onboard; downlink only actionable detections for reconnaissance, maritime tracking and disaster response.

02 AUTONOMOUS COLLISION AVOIDANCE

Move the OODA loop onboard—detect risk and decide maneuvers in milliseconds instead of waiting for ground processing.

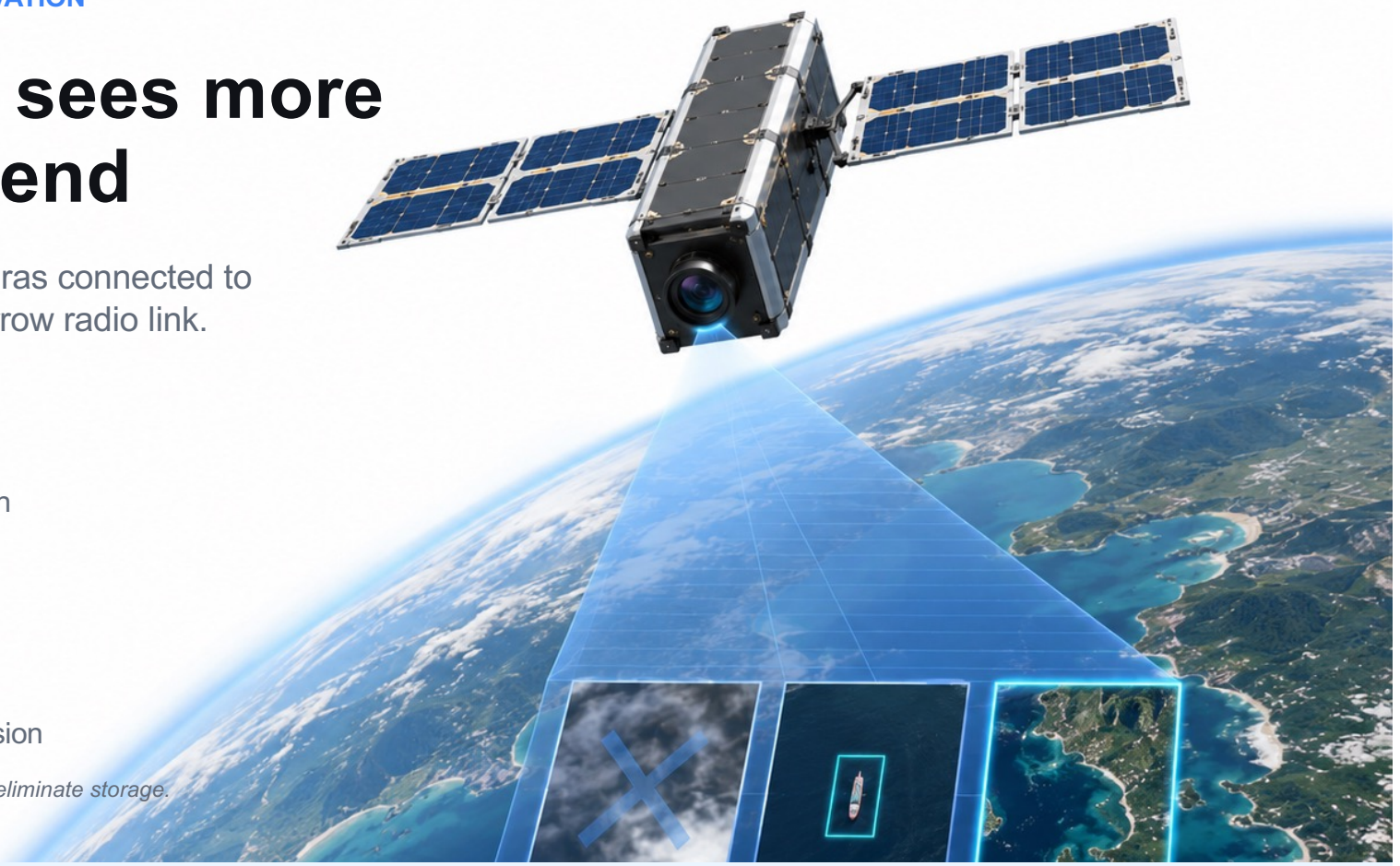
NOT ORBITAL HYPERSCALE YET. SPACE EDGE AI NOW.

Source: IEEE Spectrum, July 2026

REAL CASE 01 | EARTH OBSERVATION

The satellite sees more than it can send

They are very powerful cameras connected to Earth through a relatively narrow radio link.



3.25 TB/day

NISAR: NASA–ISRO radar mission
1.1 TB onboard recorder

96%

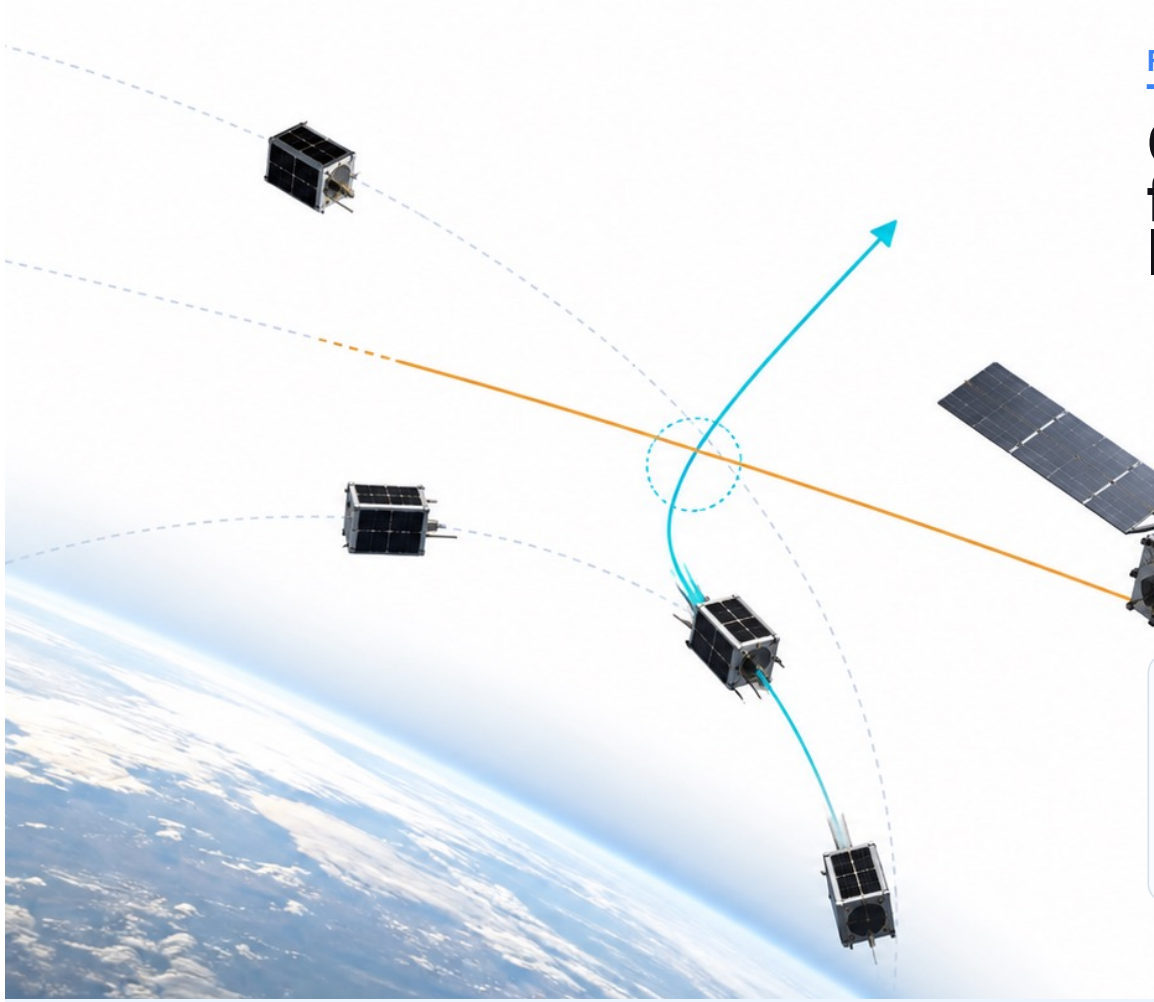
Φsat-1: cloud filtering
Φsat-2: cloud + vessel + compression

AI reduces downlink volume—but does not eliminate storage.

STORAGE CONSEQUENCE

Buffer raw data → run models locally → queue only useful products

Sources: science.nasa.gov/mission/nisar • esa.int/Phsat-2 • doi.org/10.1109/TGRS.2021.3125567



REAL CASE 02 | ORBITAL AUTONOMY

Orbital traffic cannot wait for a ground-only control loop

46,200
tracked orbital objects

1.2M
estimated debris objects 1–10 cm

DEMONSTRATED IN ORBIT

NASA Starling accepted maneuver responsibility, then autonomously planned and executed the avoidance.

GROUND TEAMS: DAYS → ONBOARD ACTION: HOURS
Autonomous reasoning—not necessarily neural-network control

STORAGE CONSEQUENCE

Trusted state, trajectories and maneuver history—available without silent corruption

Sources: nasa.gov (Starling 1.5) • sdup.esoc.esa.int/discosweb/statistics

REAL CASE 03 | MISSILE WARNING

Missile tracks cannot wait for a ground loop

100+
Tracking Layer spacecraft in the planned constellation

2D
track formation processed onboard

SENSOR TO TACTICAL USER

Infrared sensing → onboard track formation → low-latency optical and tactical links

ONBOARD: DETECT → FORM TRACK → RELAY
Public sources do not specify neural-network control

STORAGE CONSEQUENCE

Rolling sensor buffer → track state → authenticated event log

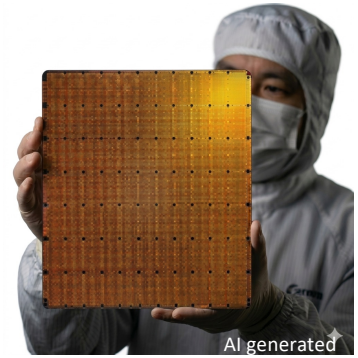
Sources: sda.mil/tracking • SDA Tracking Layer fact sheet

FOUNDATIONAL MEMORY AND STORAGE TECHNOLOGIES FOR AI

AI and Compute Is Nothing Without Storage

1

SRAM



Cerebras WSE-3

CAPACITY

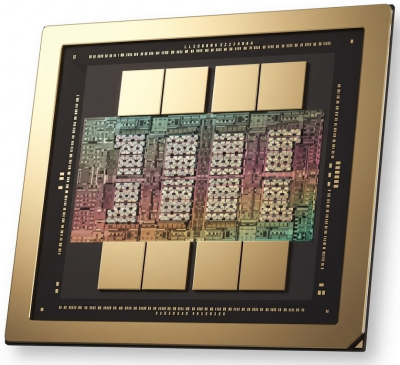
44 GB

BANDWIDTH

21 PB/s

2

DRAM and High Bandwidth Memory



NVIDIA Rubin

CAPACITY

288 GB

BANDWIDTH

22 TB/s

3

NAND Flash Storage

CAPACITY

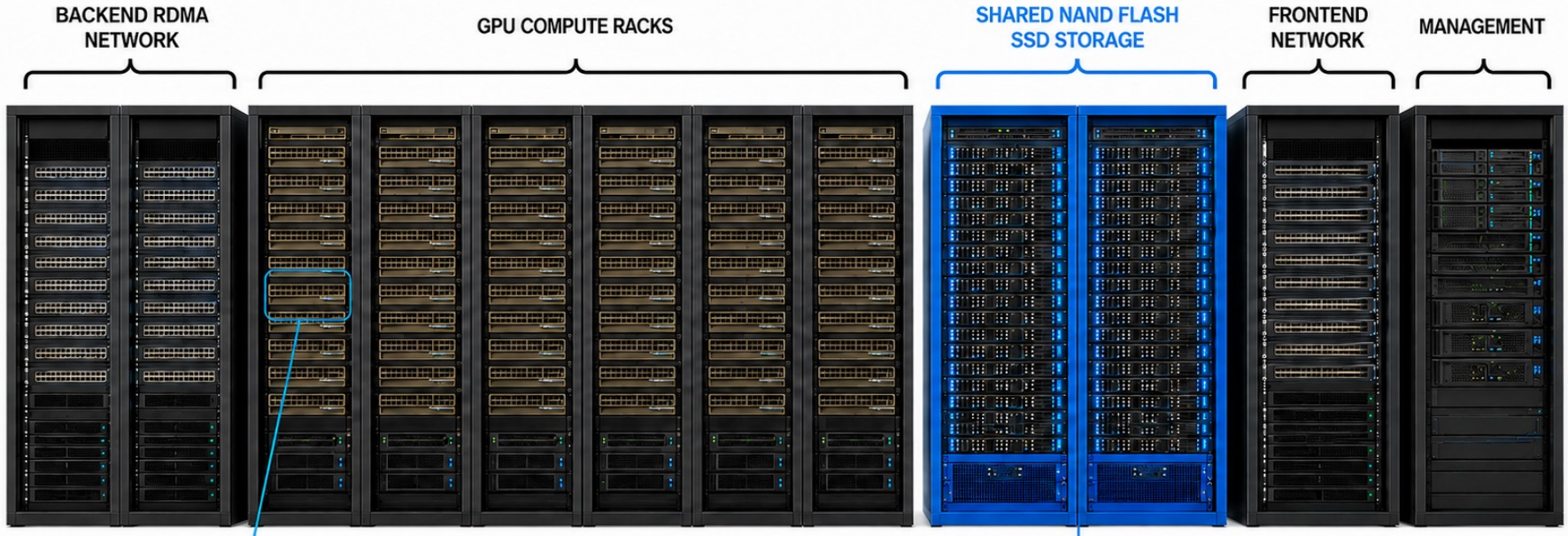
30 – 245 TB

BANDWIDTH

~14 GB/s

DATA STORAGE ON TERESTRIAL DATA CENTERS

AI Data Centers feature Exabytes of Storage



NVIDIA GB200 NVL72 compute rack contains 72 Blackwell GPUs and 13.4 terabytes of HBM3E

This pod would contain 432 GPUs and approximately 80 terabytes of HBM.

NVIDIA Eos supercomputer: 12 petabytes of all-flash storage in fewer than three racks

HBM is attached to the GPUs. NAND flash provides shared persistent capacity.

THE STORAGE CONSEQUENCE

Each gigawatt drives ≈3–4 EB of NAND Storage

A 5-GW Hyperion-scale campus approaches 15–21 EB of installed flash

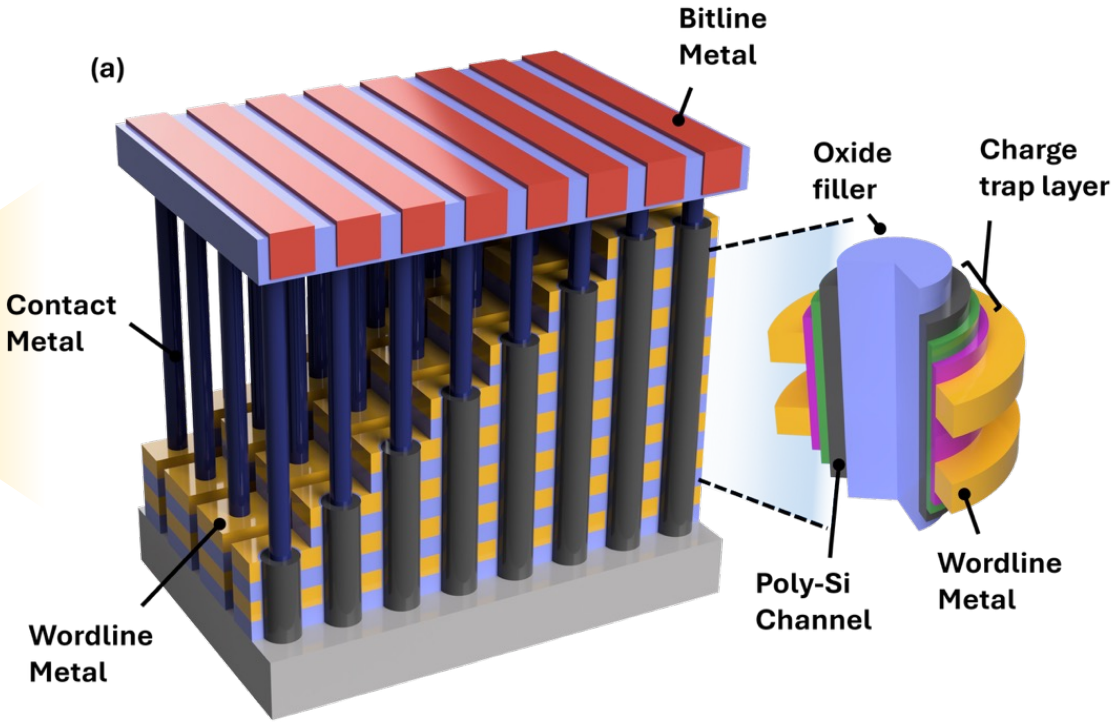
FULL-BUILDOUT ESTIMATE

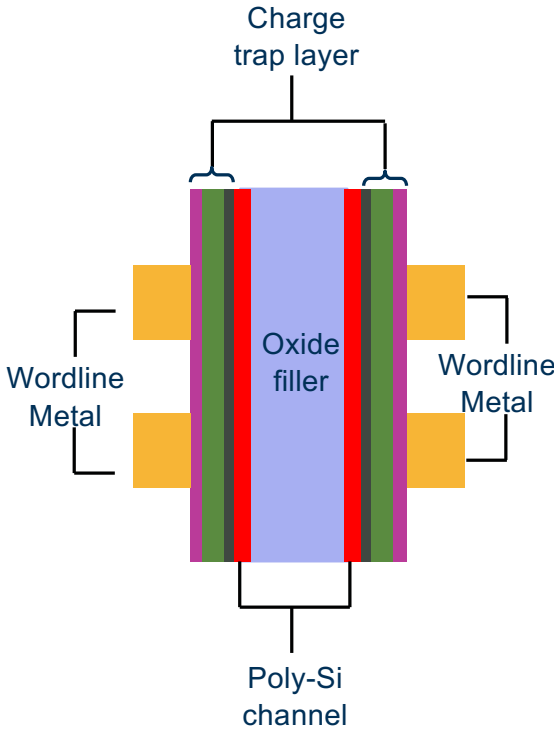
Exabyte-scale NAND Storage

		INSTALLED NAND
01	**Meta Hyperion** 5.0-GW campus	**14.5–20.9 EB**
02	**Project Camellia** 3.2-GW campus	**9.2–13.4 EB**
03	**AWS Northern Indiana** 2.4-GW buildout	**6.9–10.0 EB**
04	**Crusoe Abilene** 2.1-GW complex	**6.1–8.8 EB**
05	**xAI Greater Memphis** ≈2.0-GW cluster	**5.8–8.3 EB**

PUE 1.15 • 6.9–10 TB NAND/GPU • HBM and DRAM excluded

3-D NAND storage technology





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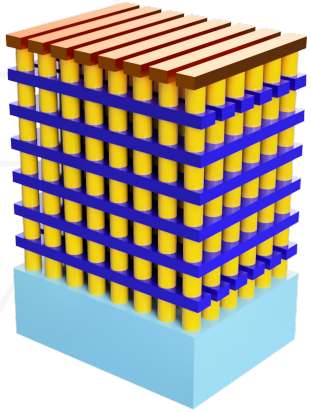
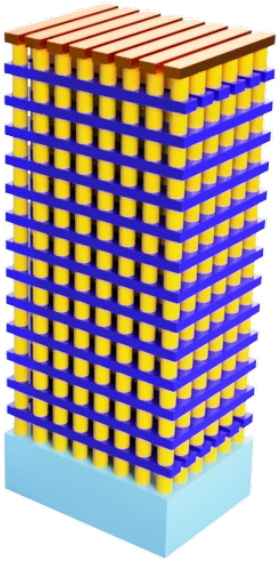
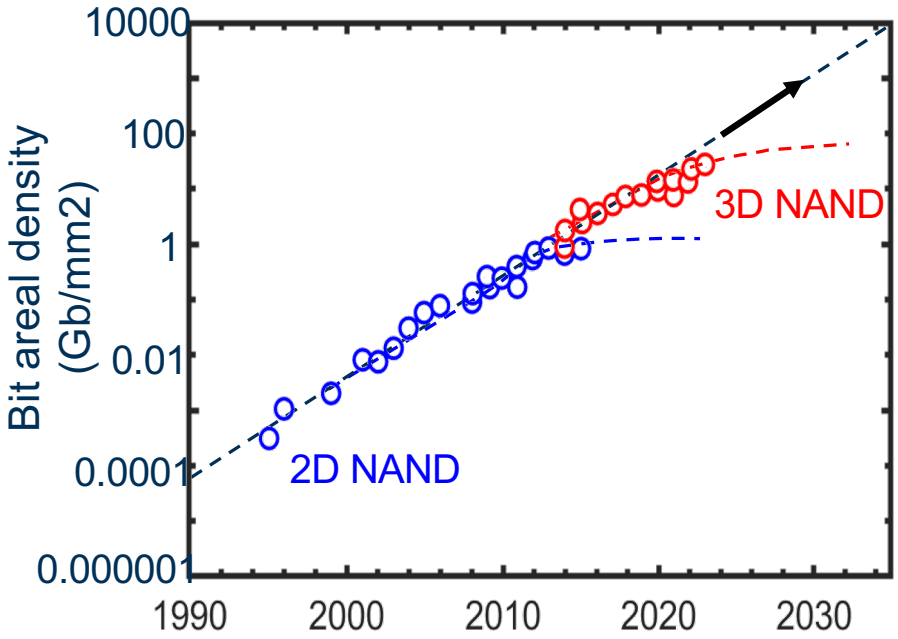
3-D NAND storage technology



2014
First 3D NAND, Samsung
24 Layers, MLC



2022-2026
Production
Samsung 236L TLC
SK hynix 238L TLC → 321L (ramping 1H25)
Micron 276L TLC
Prototype / R&D demos:
SK hynix 321L sample (FMS 2023)
SK hynix 300+L demo (ISSCC 2023)
Kioxia / WD >300L demo (VLSI 2023)
Kioxia / Sandisk 1000L using wafer-to-wafer Cu direct bonding (2026)



A. Goda, IEDM 2024

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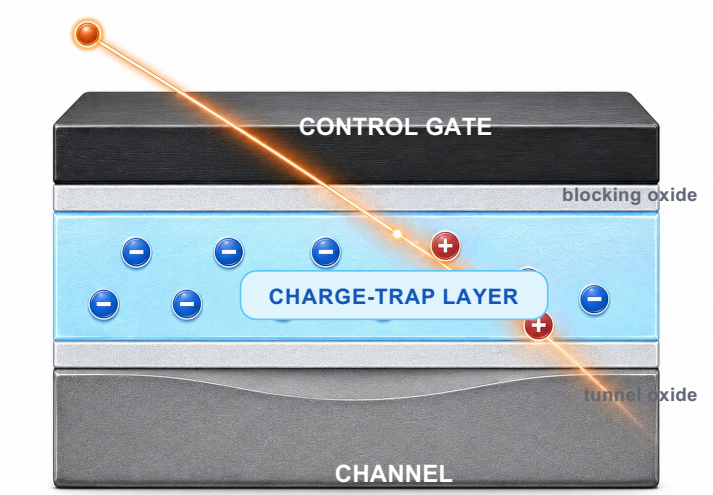
Radiation attacks the charge that stores the bit.

NAND stores information as electric charge—and space radiation also creates, removes and redistributes electric charge.

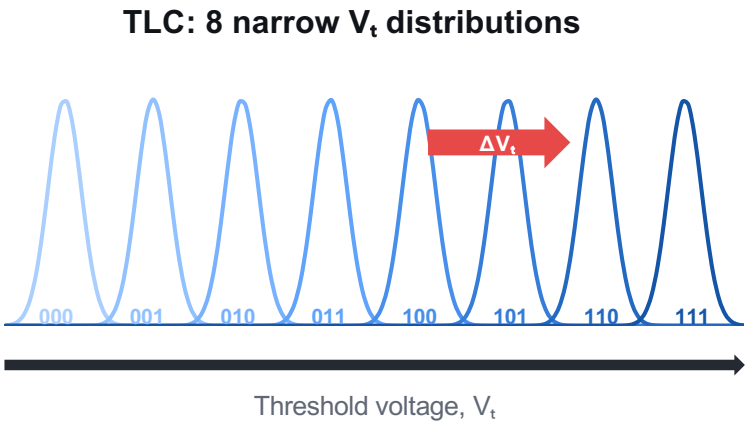
CHARGE-TRAP NAND CELL



blue = stored electrons

red = radiation-induced trapped charge

THE READOUT CONSEQUENCE



Radiation-induced shift can cross a read boundary.

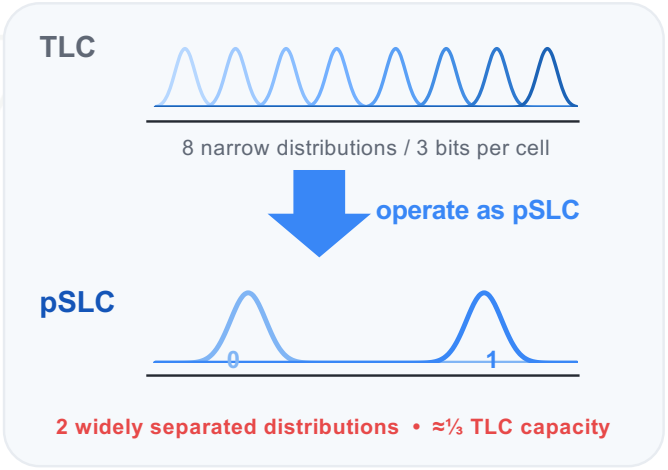
The vulnerability is intrinsic to charge-based storage.

Sources: NASA NEPP NAND radiation studies, 2019 and 2023

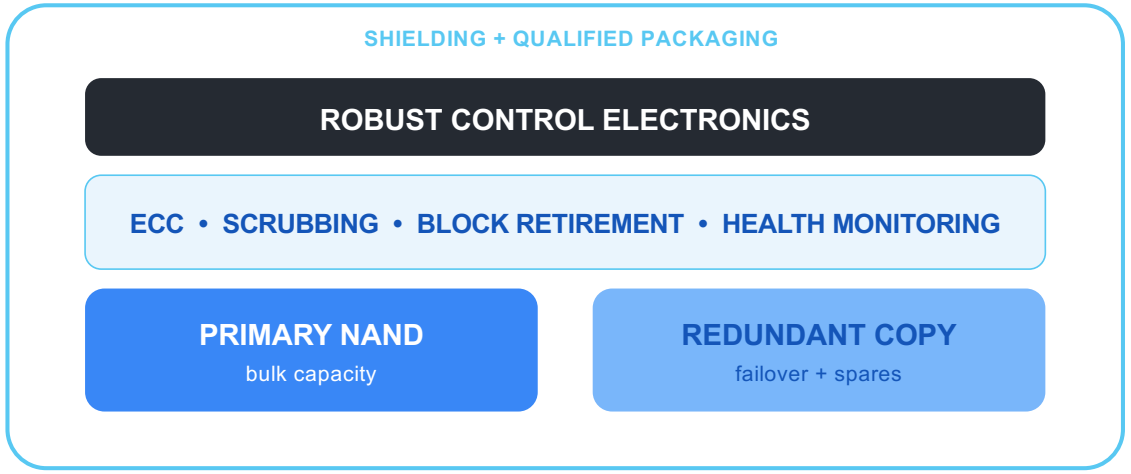
Today's solution surrounds dense NAND with protection.

High-density NAND supplies the bulk bytes; reliability is added through operating mode, coding, redundancy and hardened electronics.

1 BUY MORE VOLTAGE MARGIN



2 WRAP THE ARRAY IN SYSTEM PROTECTION



Reliability comes largely from the system wrapped around the NAND array.

Sources: NASA NEPP (2019); KIOXIA Spaceborne Computer-2; 3D PLUS

CURRENT SPACE NAND | TRUE SLC

Space-qualified SLC NAND exists—but only at gigabyte scale.

Vendor: 3D PLUS (France) • space-electronics packaging, integration and qualification

Source: 3d-plus.com

1–16 GB

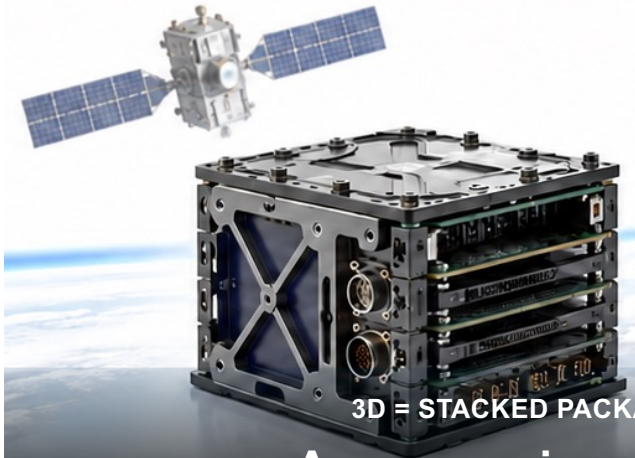
8–128 Gb PER PACKAGE
TRUE SLC • 1 BIT PER CELL
S-LEVEL SPACE SCREENING

>60 krad

TOTAL IONIZING DOSE, Si
SEL LET_{th} >62.5 MeV·cm²/mg
−55 TO +125 °C

100k

P/E CYCLES
10-YEAR RETENTION



3D = STACKED PACKAGE • NAND DIE SUPPLIER + CELL ARCHITECTURE NOT PUBLICLY SPECIFIED

Assurance is real—but one package tops out at 16 GB, not terabytes.

CURRENT SPACE NAND | ISS DEMONSTRATION

The ISS's >130 TB came from commercial KIOXIA TLC SSDs.

HPE Spaceborne Computer-2 demonstrates orbital capacity—not radiation-qualified NAND.

Sources: hpe.com • kioxia.com

134.912 TB

4 × 30.72 TB PM6 SAS
8 × 1.024 TB XG6 NVMe
4 × 0.960 TB RM6 SAS

91%

OF RAW CAPACITY FROM PM6
96-LAYER 3D TLC NAND
COMMERCIAL ENTERPRISE SSDs

COTS

SSDs NOT CUSTOMIZED
FOR SPACE

HPE SPACEBORNE COMPUTER-2 • ISS • LAUNCHED 30 JAN 2024

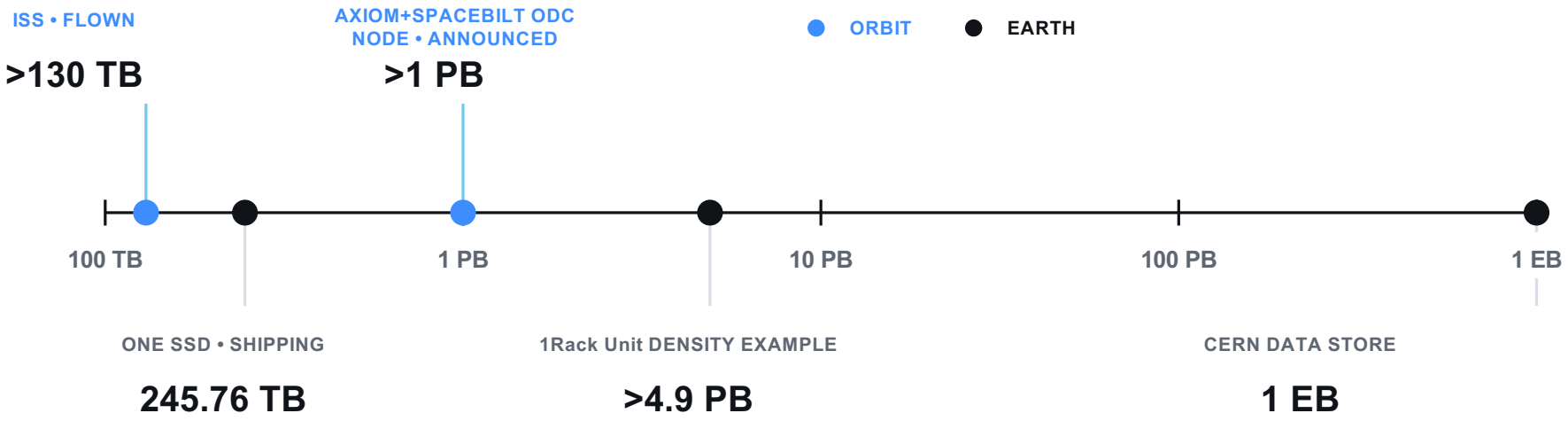
Daily health monitoring made terrestrial SSDs practical inside the ISS.

CAPACITY: ORBIT VERSUS EARTH

Orbit is approaching petabytes. Earth already operates at exabytes.

Vendor-stated capacity in decimal TB • logarithmic scale

1 GB = 1 gigabyte (10^9 bytes)
1 TB = 1,000 GB (10^{12} bytes)
1 PB = 1,000,000 GB (10^{15} bytes)
1 EB = 1,000,000,000 GB (10^{18} bytes)



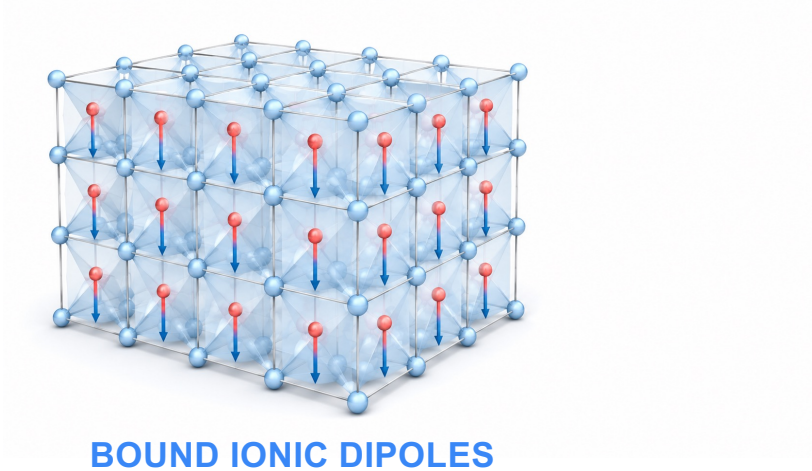
The entire 2024 ISS storage system ≈ 55% of one current terrestrial enterprise SSD.

Nominal/raw capacity comparison; usable capacity is lower after formatting, protection and sparing.

Can ferroelectrics provide better NAND storage in space?

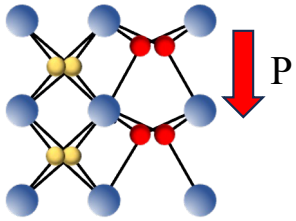
The memory state is switchable, bound polarization—not trapped electronic charge.

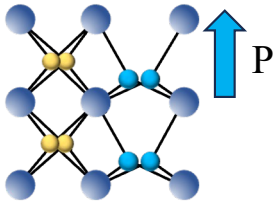
HfO_2-BASED FERROELECTRIC

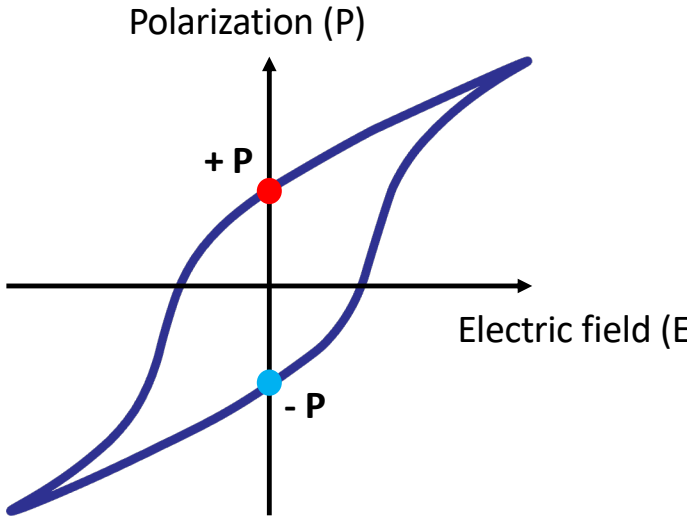


BOUND IONIC DIPOLES

Opposite polarization directions encode the two memory states.





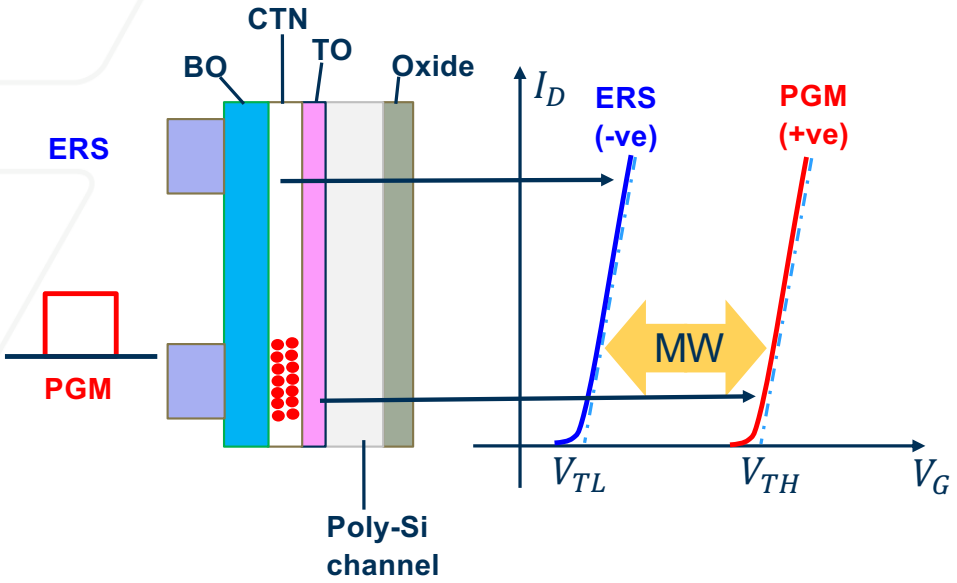


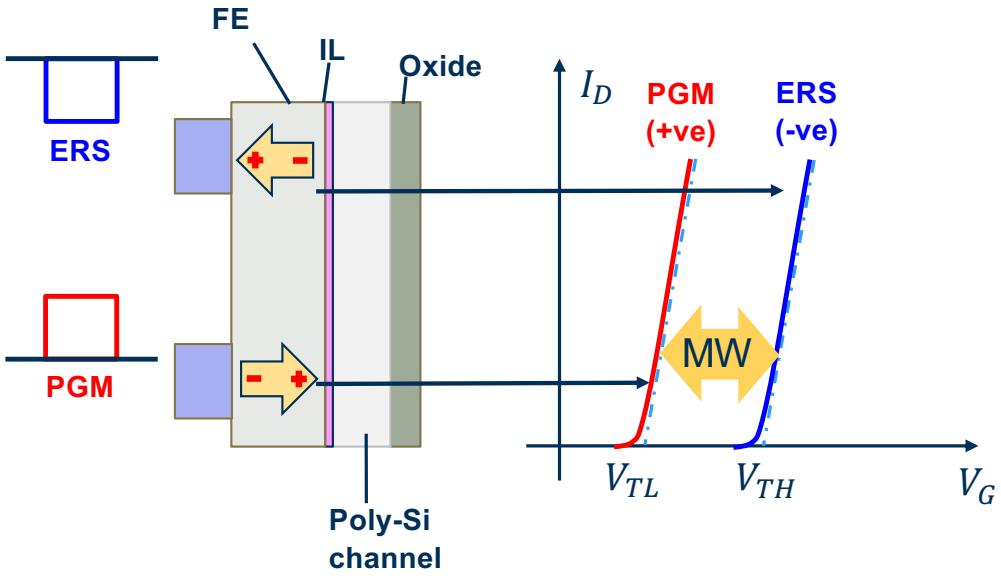
Bound polarization is resilient to radiation-generated charge.

Cell-level demonstration: programmed and erased states remained stable through 1 Mrad(air).

Source: Fang et al., Nano Letters (2026)

Charge trap flash vs. ferroelectric flash





$$MW = V_{TH} - V_{TL}$$

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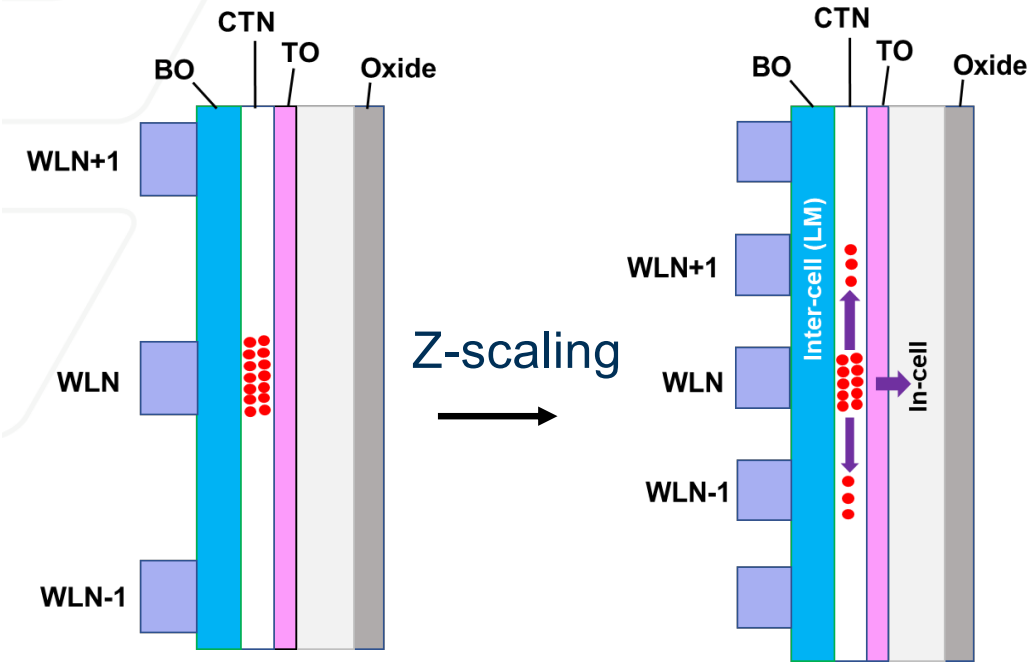
Charge trap flash vs. ferroelectric flash



1 Lateral charge migration

Continuous SiN trap layer lets stored charge migrate between cells via diffusion and trap-to-trap transport.

2 High write voltage

Fowler–Nordheim programming demands ~20 V every cycle — large on-die charge pumps and accelerated tunnel-oxide wear-out. Increased power,

3 Coupling and disturb

Electrostatic fringing fields perturb adjacent cells; pass-voltage stress accumulates with each read.

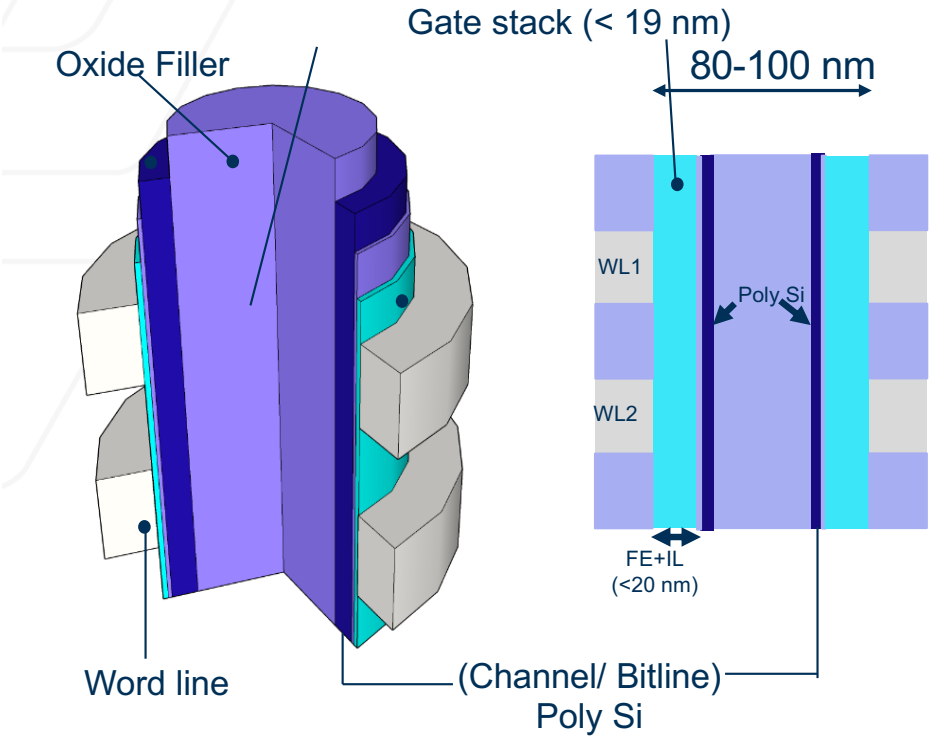
4 Variability and read margin

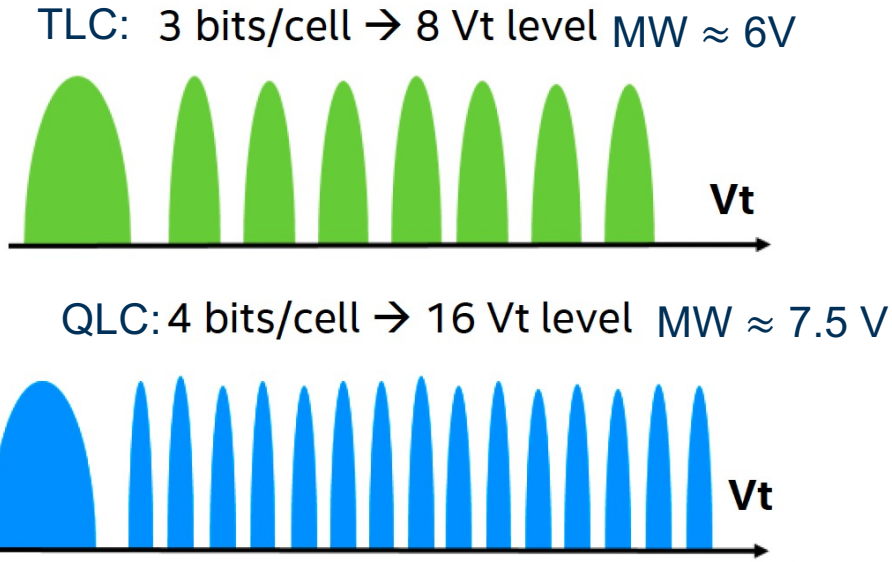
RTN, poly-Si grain variability, and channel taper compress threshold-voltage state distributions. Poly-Si channel resistance grows with cell count; grain boundaries limit mobility and uniformity.

Read sensing margin shrinks

19

Target metrics for ferroelectric NAND flash





To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm

Design constraints

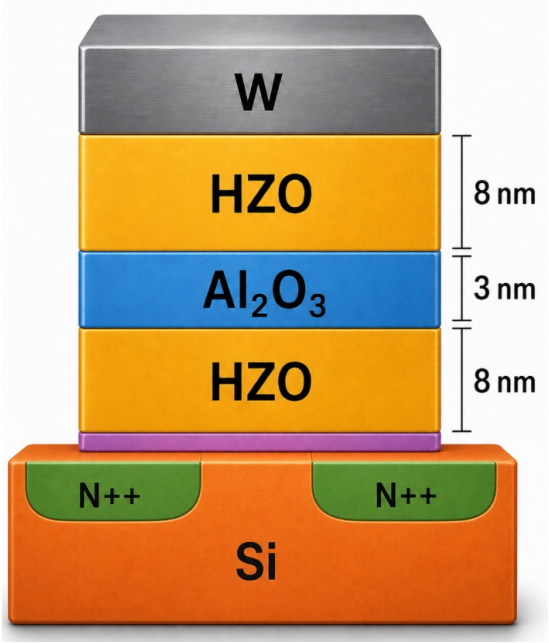
Gate stack thickness, $t \leq 19$ nm

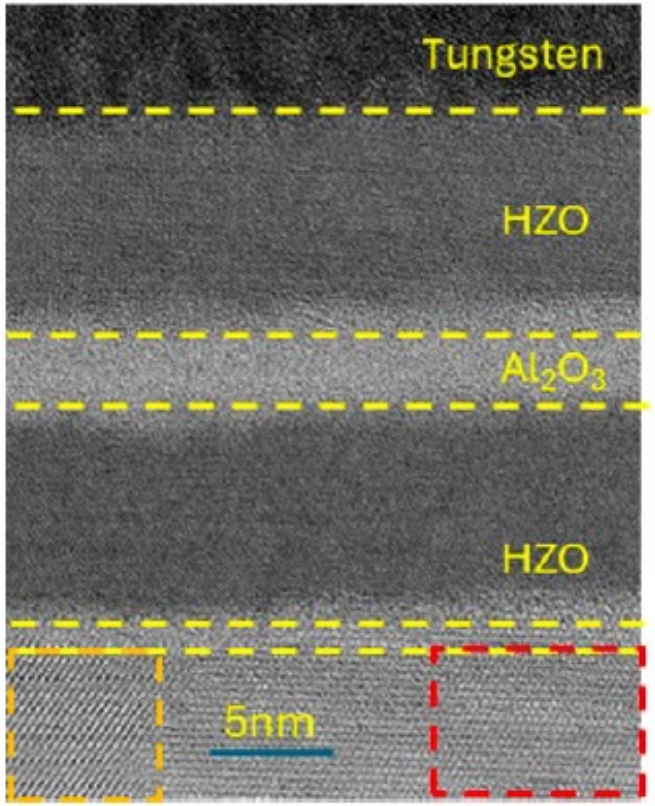
Write voltage ≤ 15 V

Memory window, MW ≥ 6.5 V

Ferroelectric field-effect transistor for NAND applications

- Poly-Si deposition at 600°C
- Source/Drain ion implantation
- Dopant activation at 900°C
- MESA pattern
- Gate stack and W gate depositior
- RTA at 500°C for 30 seconds
- Gate electrode pattern
- SiO_2 ILD deposition and Via etch
- Al/Si electrode deposition
- FGA at 400°C for 30 minutes





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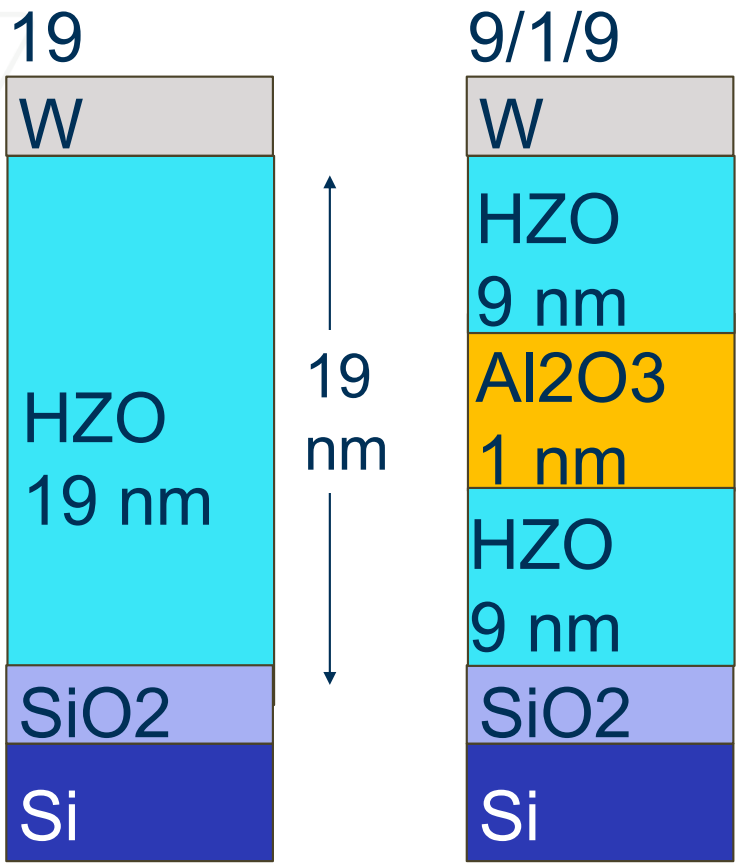
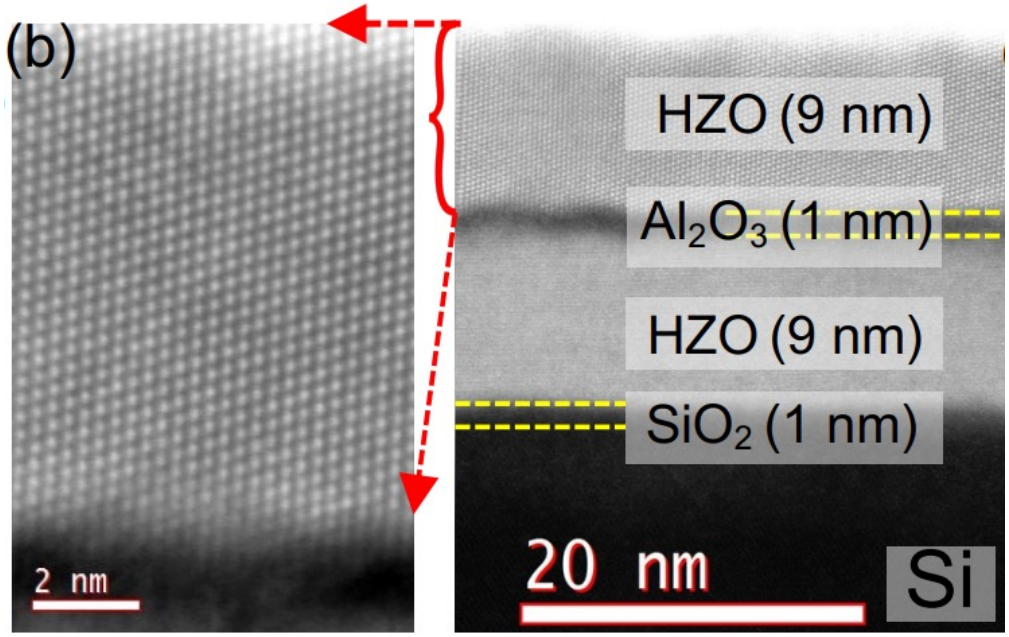
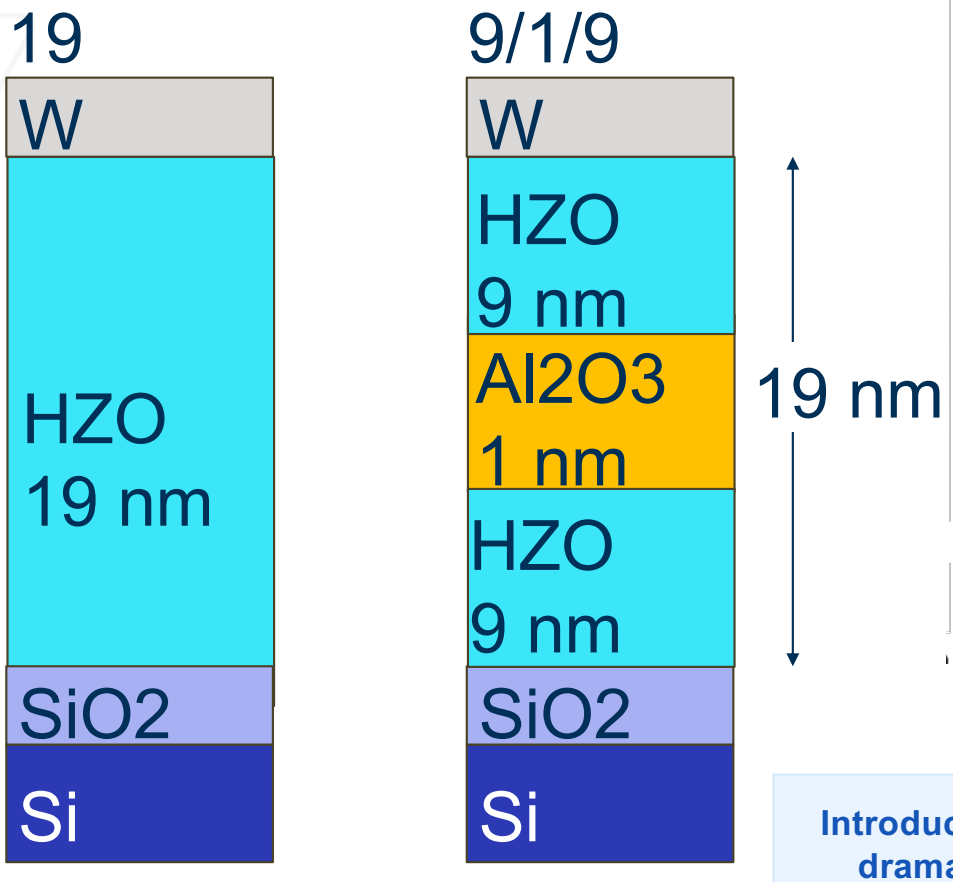
Increasing the MW by dielectric insertion

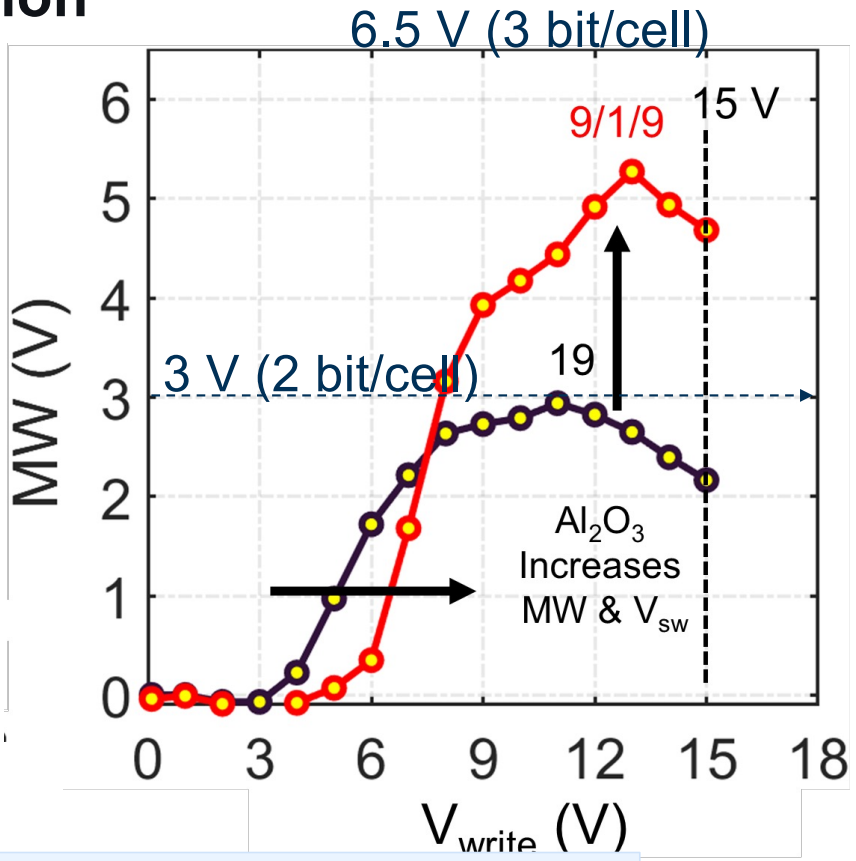




Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion





Introducing 1 nm Al2O3 intermediate layer dramatically memory window to 5.3 V.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

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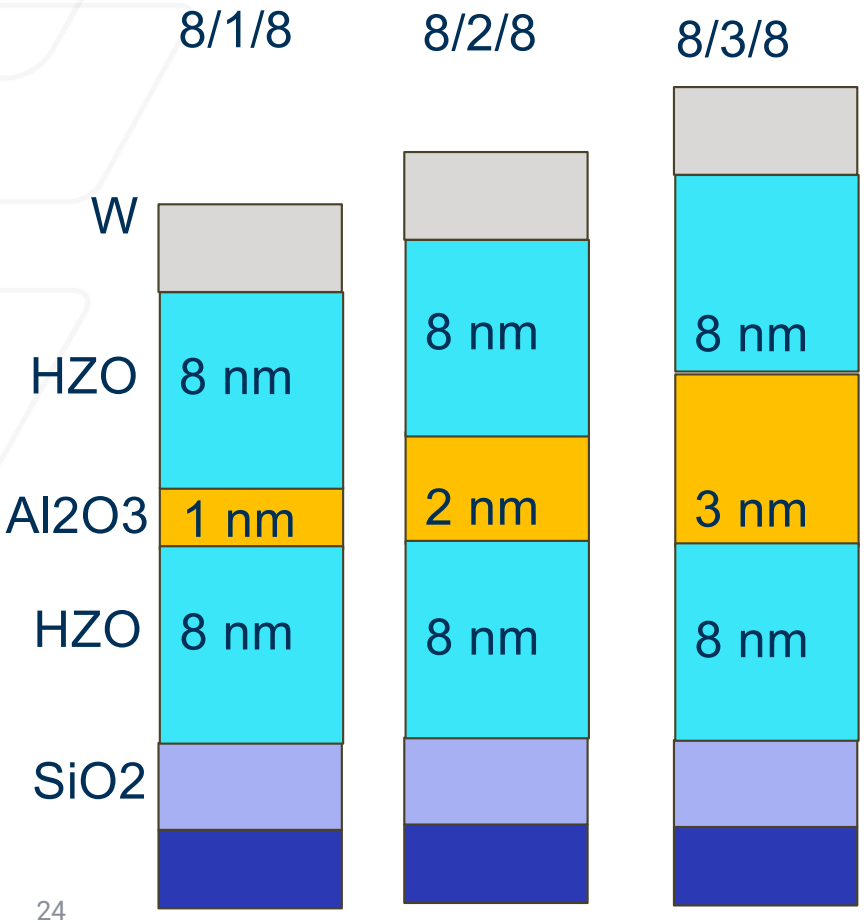
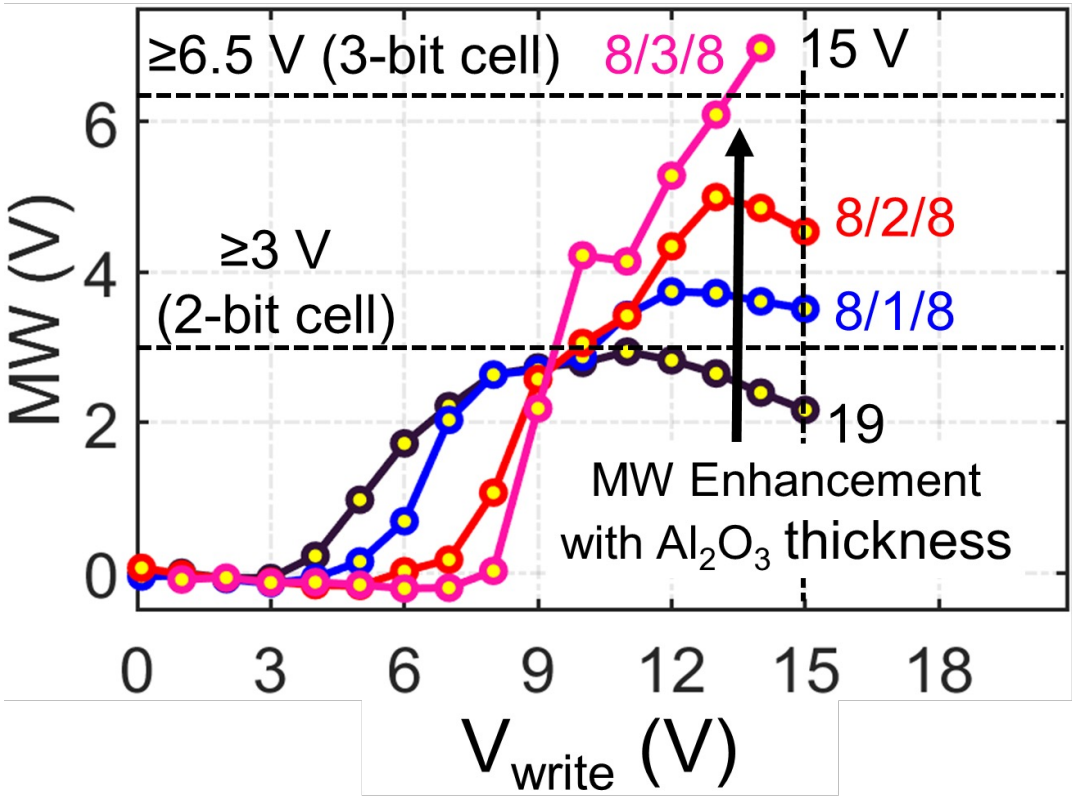
Increasing the MW by dielectric insertion

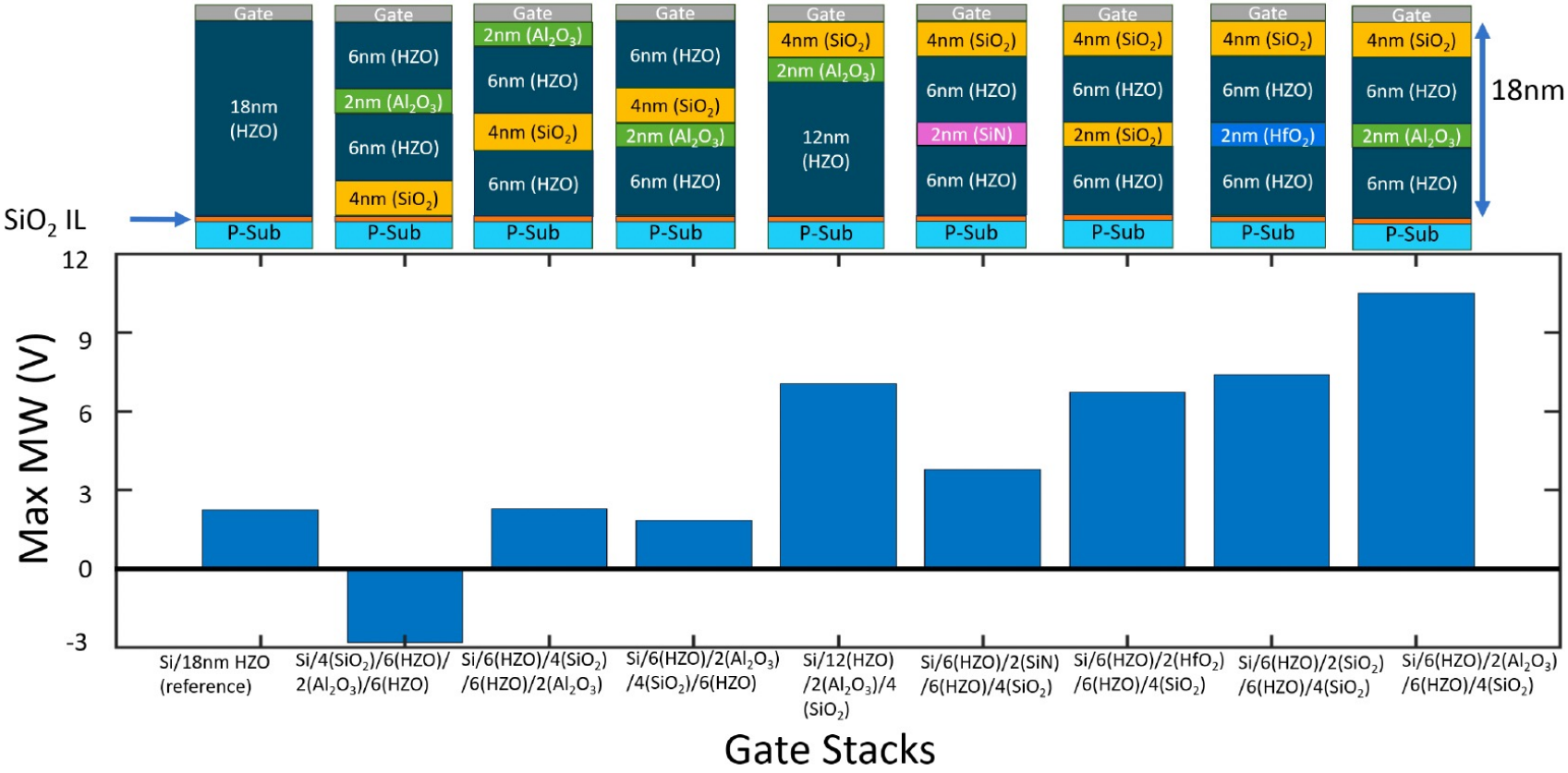




FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Position and Choice of the Dielectric Material



Fernandes, Khan et al. *Optimizing Memory Window for Ferroelectric Nand Applications: An Experimental Study on Dielectric Material Selection and Layer Positioning*. IEEE Transactions on Electron Devices 72, 234 - 239 (2024). https://doi.org/10.1109/TED.2024.3504475

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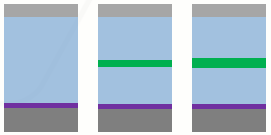
Ferroelectric NAND from the academia

Results from Georgia Tech

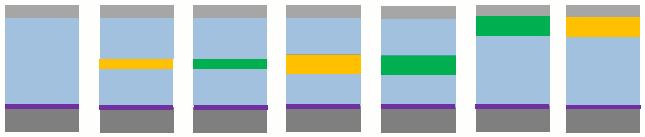
Batch 1: Tunnel Dielectric Layer

Das et al., IEDM 2023:



Batch 2: Choice and position of dielectric insert

Fernandes et al., EDL 2024:

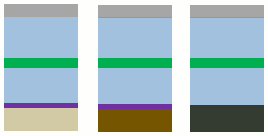


Batch 3: Hybrid structures

Fernandes et al., TED 2024:

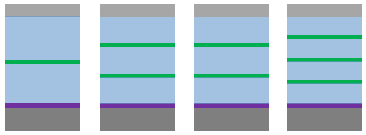
Batch 4: Channel materials

Fernandes et al., IMW 2025:



0.5 nm TDL inserts

Lee et al., TED 2024:



AOS channels

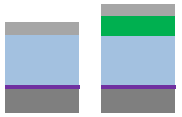
Yoo et al., VLSI 2024:

Joh et al., IEDM 2024:

Gate blocking layer

Lim et al., IEDM 2023:

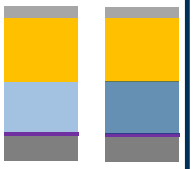
Hu et al., EDL 2024:



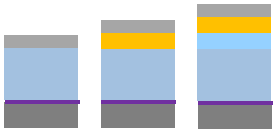
Yang et al., ICSIST 2024:

Hu et al., EDL 2024:

Chu et al., EDL 2024:

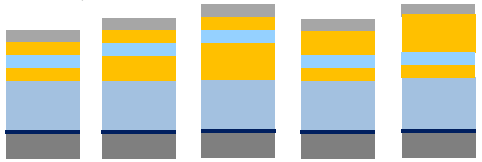


Kuk et al., IEDM 2024:

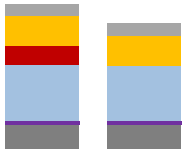


Qin et al., IEDM 2024:

Han et al., IRPS 2025:



G. Kim et al., IEDM 2024:



Ferroelectrics:

- 26 HZO
- HAO

Dielectrics:

- SiO2
- Si3N4
- TiO2
- Al2O3
- HfO2

Channel IL:

- SiO2 IL (1 nm)
- Al2O3/AlON IL (1 nm)

Semiconductor:

- Si
- SOI
- AOS
- Poly-Si

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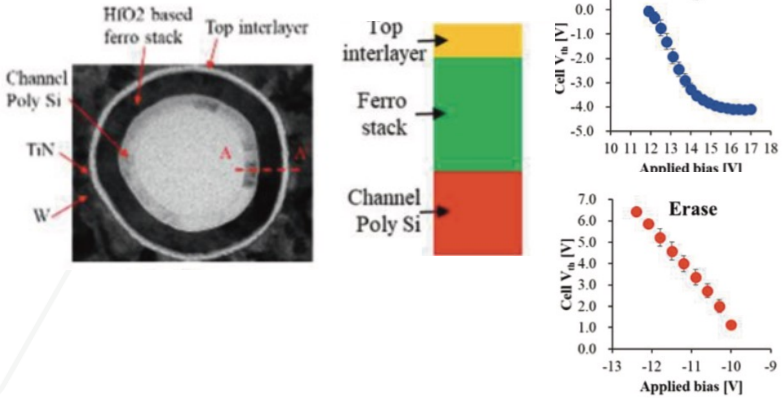
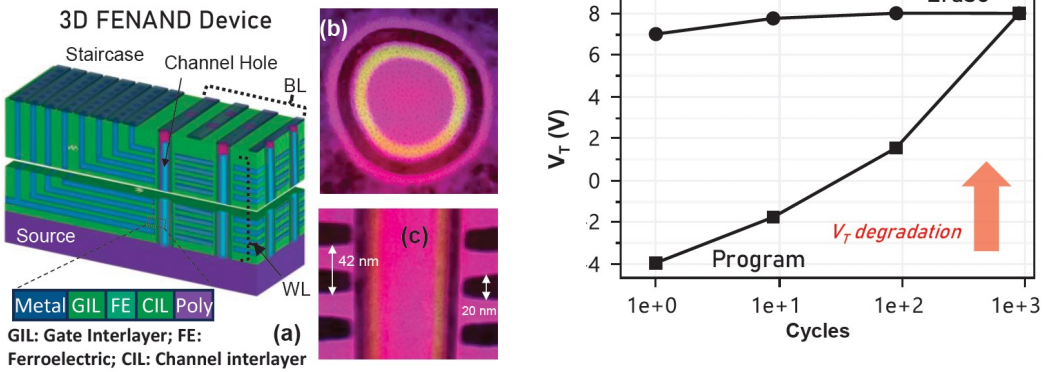
Ferroelectric 3-D NAND demonstrations

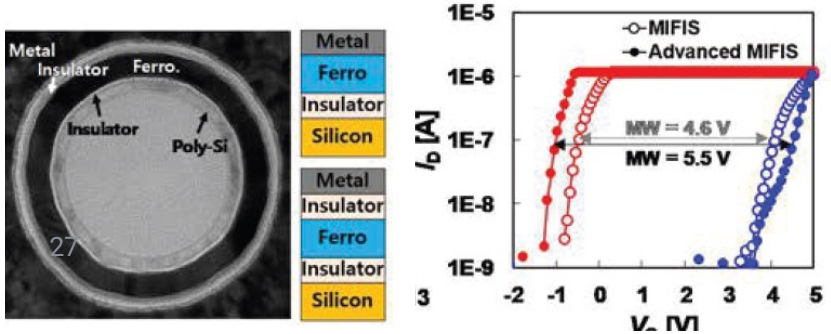
SK Hynix
Yoon et al. VLSI 2023



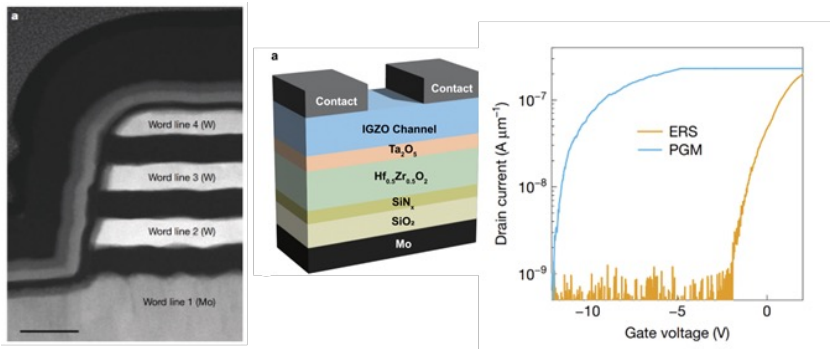
Micron
Sharma et al. VLSI 2025



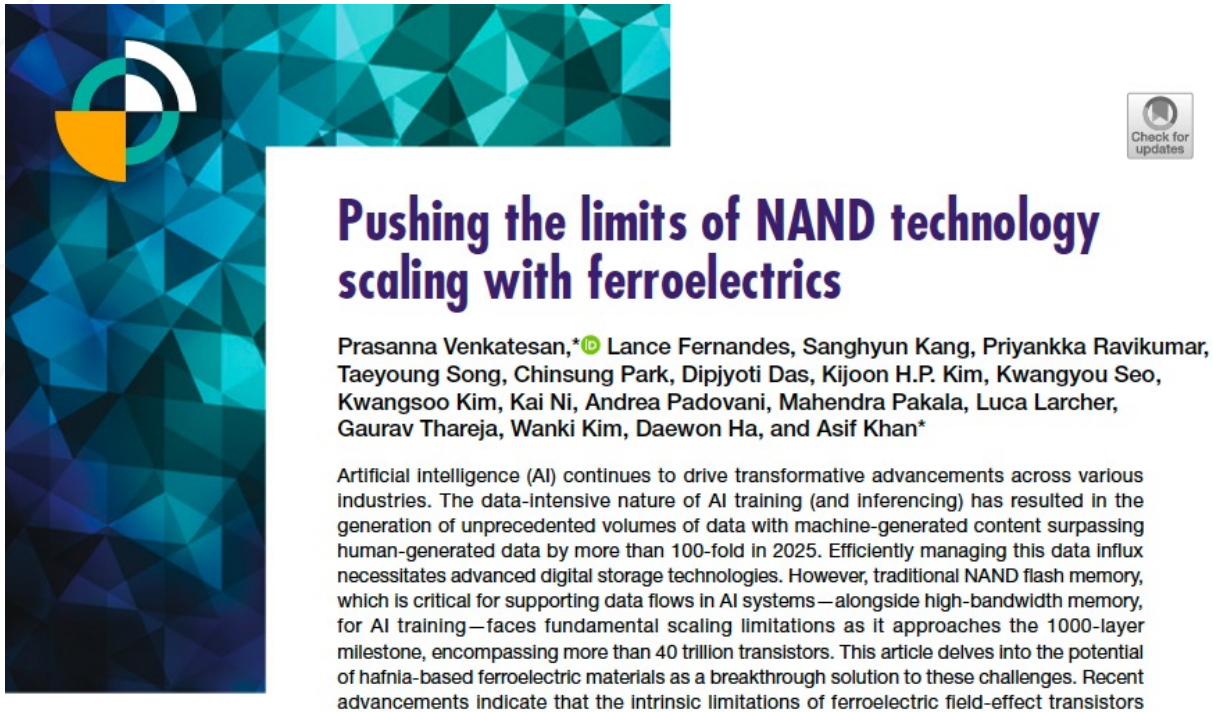
Samsung
Lim et al. IEDM 2023



Samsung
Sharma et al. Science 2025



Evaluating ferroelectric NAND Flash



Check for updates

Pushing the limits of NAND technology scaling with ferroelectrics

Prasanna Venkatesan,* Lance Fernandes, Sanghyun Kang, Priyankka Ravikumar, Taeyoung Song, Chinsung Park, Dipjyoti Das, Kijoon H.P. Kim, Kwangyou Seo, Kwangsoo Kim, Kai Ni, Andrea Padovani, Mahendra Pakala, Luca Larcher, Gaurav Thareja, Wanki Kim, Daewon Ha, and Asif Khan*

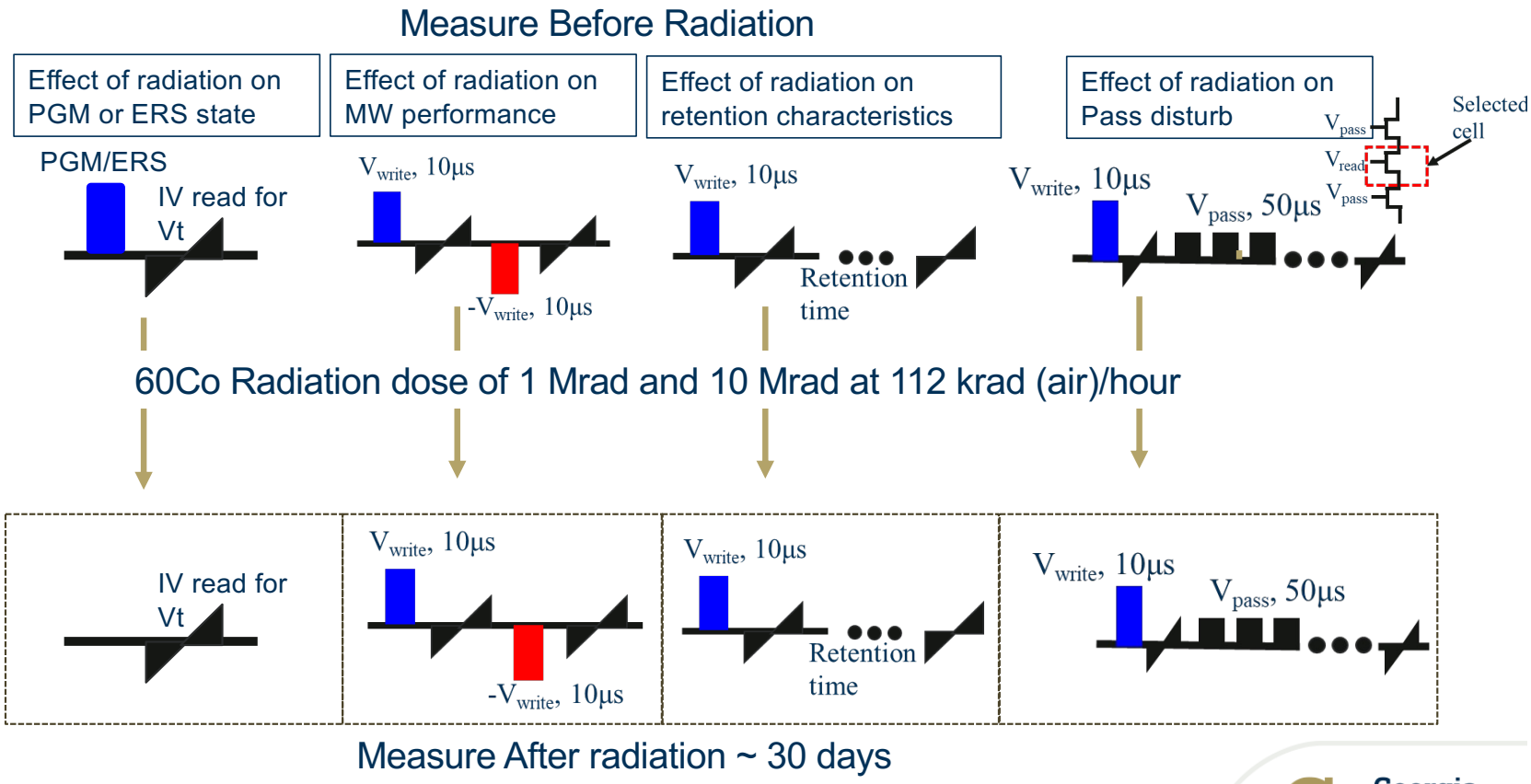
Artificial intelligence (AI) continues to drive transformative advancements across various industries. The data-intensive nature of AI training (and inferencing) has resulted in the generation of unprecedented volumes of data with machine-generated content surpassing human-generated data by more than 100-fold in 2025. Efficiently managing this data influx necessitates advanced digital storage technologies. However, traditional NAND flash memory, which is critical for supporting data flows in AI systems—alongside high-bandwidth memory, for AI training—faces fundamental scaling limitations as it approaches the 1000-layer milestone, encompassing more than 40 trillion transistors. This article delves into the potential of hafnia-based ferroelectric materials as a breakthrough solution to these challenges. Recent advancements indicate that the intrinsic limitations of ferroelectric field-effect transistors (FEFETs) can be mitigated through material and device-level engineering. These advancements enable FEFETs to meet the stringent density, reliability, and scalability requirements of future three-dimensional NAND technology. The role of ferroelectrics in addressing NAND scaling challenges and expanding storage capabilities presents a promising avenue for meeting the storage demands of the AI-driven era.

Venkatesan, Khan, et al. "Pushing the limits of NAND technology scaling with ferroelectrics: P. Venkatesan et al." *MRS Bulletin* 50.9 (2025): 1094-1107.

Georgia Tech

Radiation Experiment

Laminated Fe-FET



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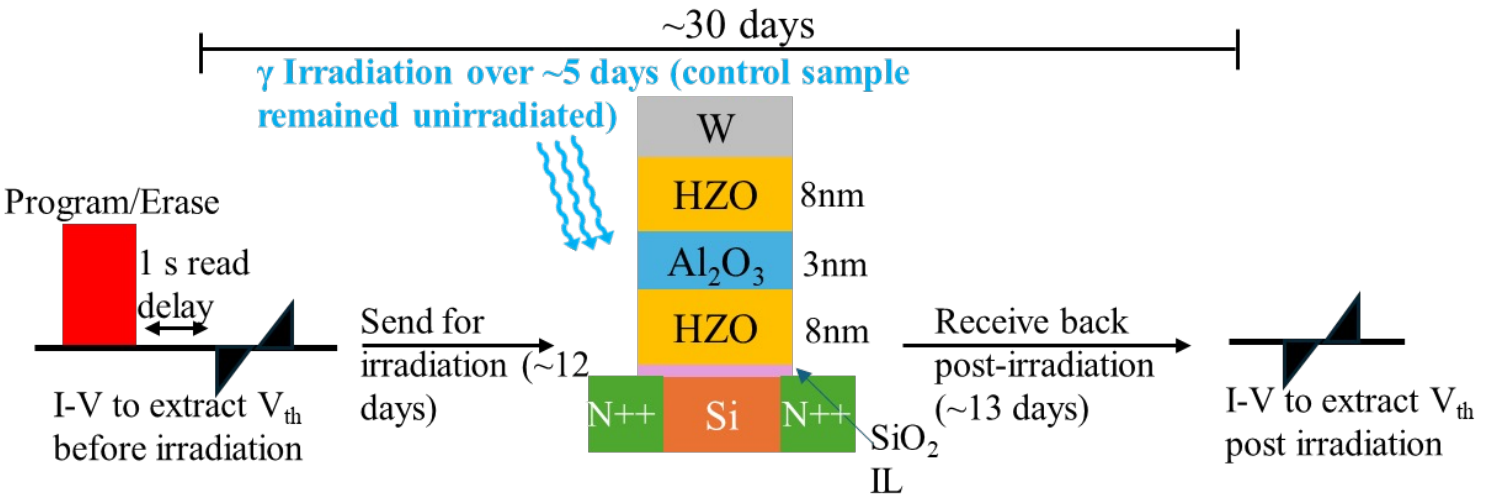
Impact of TID on stored state in Fe-NAND

Measurement scheme to understand the impact of TID on stored state



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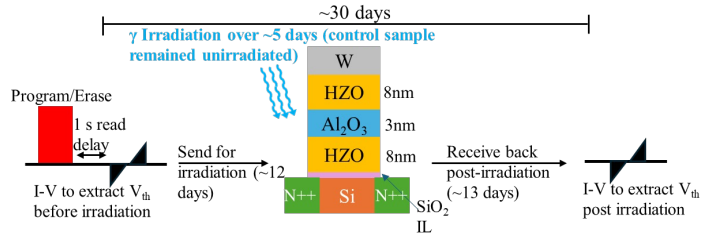
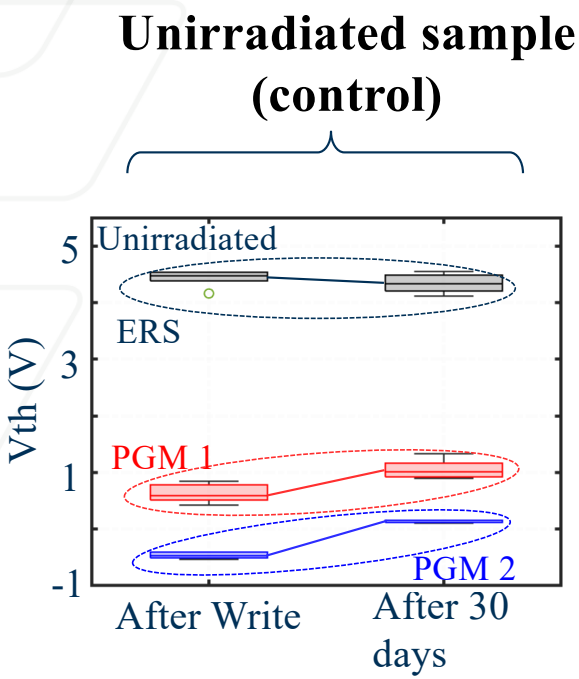
Fernandes, Lance, et al. "Enabling Radiation Hardness in Solid-State NAND Storage Utilizing a Laminated Ferroelectric Stack." *Nano Letters* 26.10 (2026): 3390-3397.

Impact of TID on stored state in Fe-NAND





- Erased State is minimally affected
- Programmed state is affected due to depolarization field

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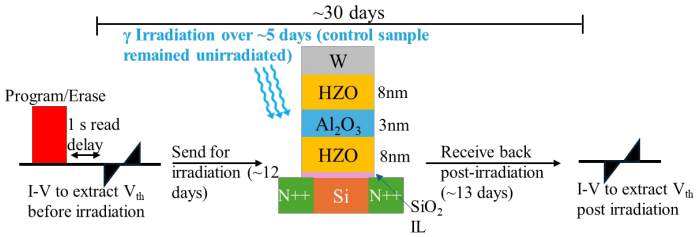
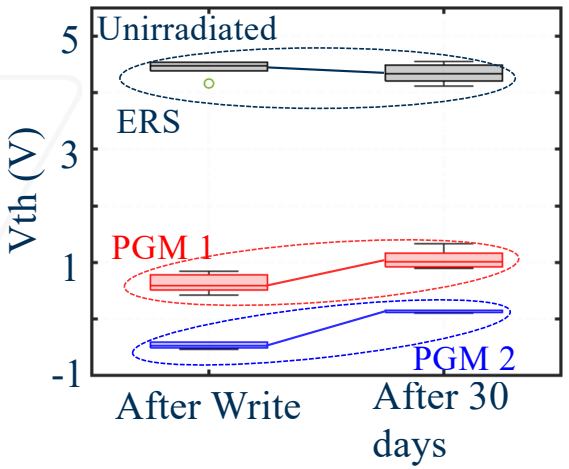
Fernandes, Lance, et al. "Enabling Radiation Hardness in Solid-State NAND Storage Utilizing a Laminated Ferroelectric Stack." *Nano Letters* 26.10 (2026): 3390-3397.

RADIATION RESPONSE | 1 MRAD

Impact of TID on stored state in Fe-NAND

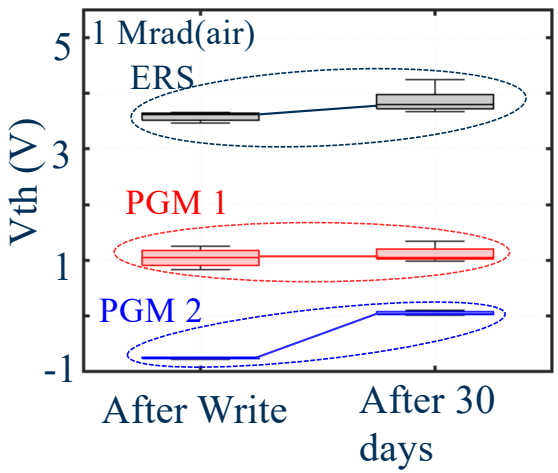


Unirradiated sample (control)



- Erased State is minimally affected
- Programmed state is affected due to depolarization field

1 Mrad



- Erased State is minimally affected
- Programmed state is affected due to depolarization field (no TID loss)

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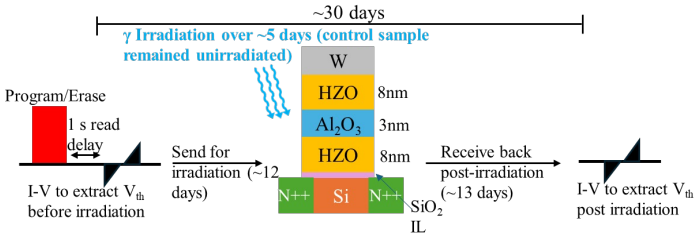
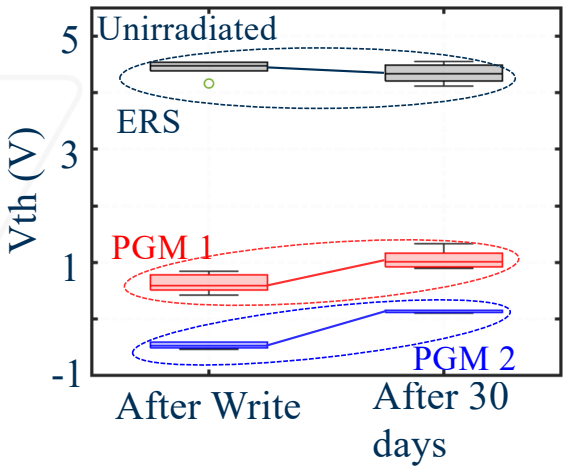
Fernandes, Lance, et al. "Enabling Radiation Hardness in Solid-State NAND Storage Utilizing a Laminated Ferroelectric Stack." *Nano Letters* 26.10 (2026): 3390-3397.

Impact of TID on stored state in Fe-NAND

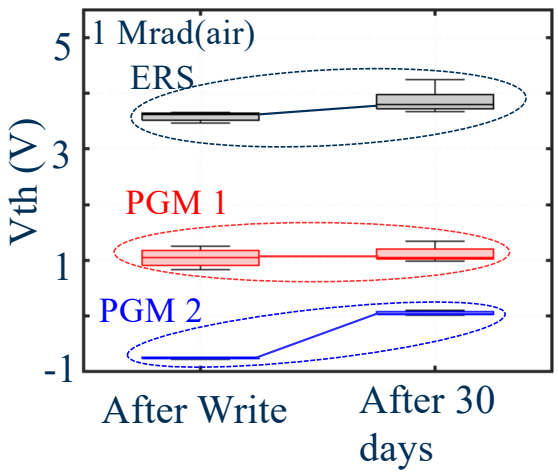


Unirradiated sample (control)



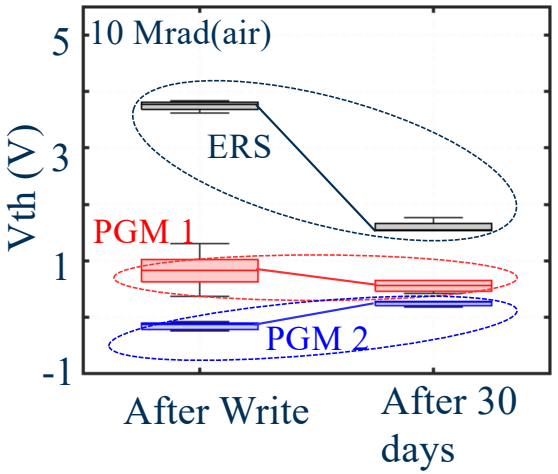
- Erased State is minimally affected
- Programmed state is affected due to depolarization field

1 Mrad- No TID degradation



- Erased State is minimally affected
- Programmed state is affected due to depolarization field (no TID loss)

10 Mrad



- Erased State is degraded due to high TID
- Programmed state 2 is affected due to depolarization field (no TID loss)

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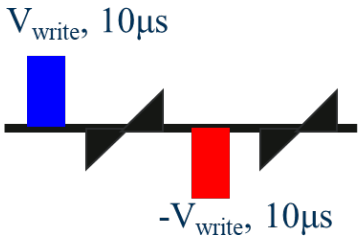
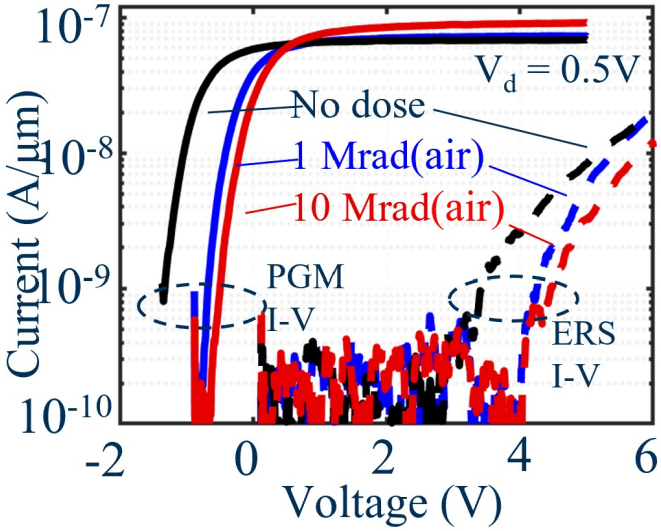
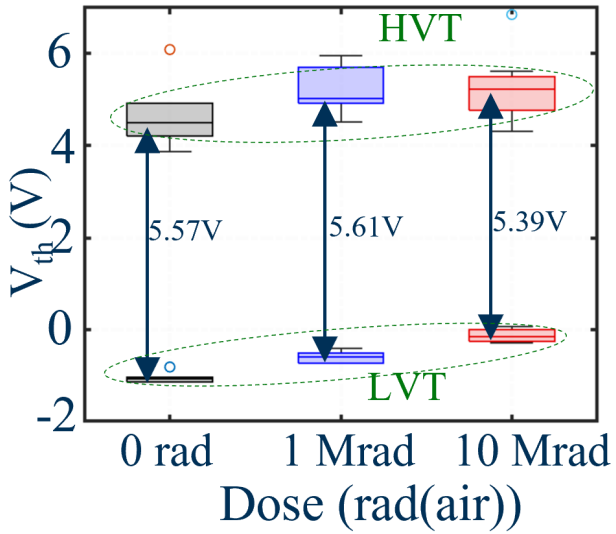
Fernandes, Lance, et al. "Enabling Radiation Hardness in Solid-State NAND Storage Utilizing a Laminated Ferroelectric Stack." *Nano Letters* 26.10 (2026): 3390-3397.

Impact of TID on MW performance







Memory Window Performance is unchanged even after irradiation where comparable MW is achieved post irradaition

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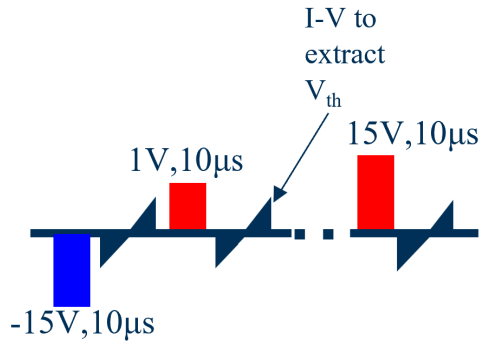
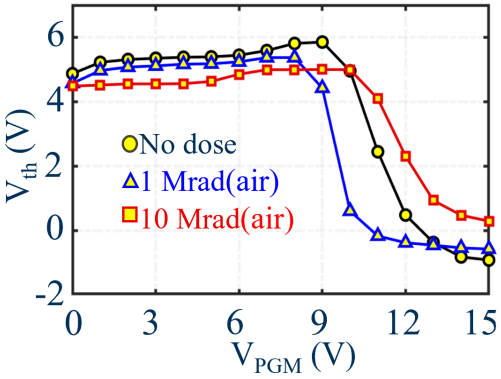
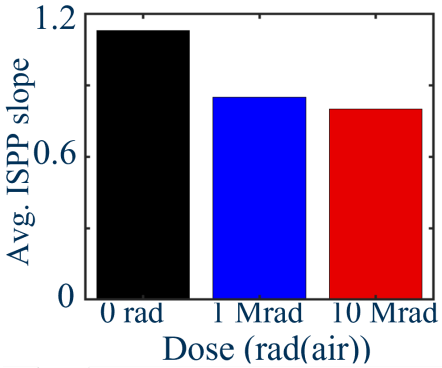
Impact of TID on ISPP/E performance

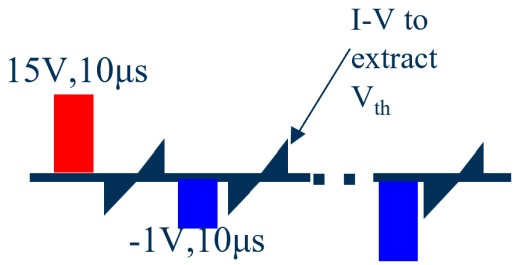
High ISPP/ISPE slope is essential for tight multi-Vth distribution



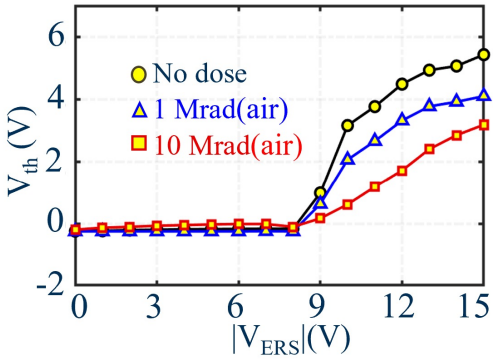
ISPP Characterization

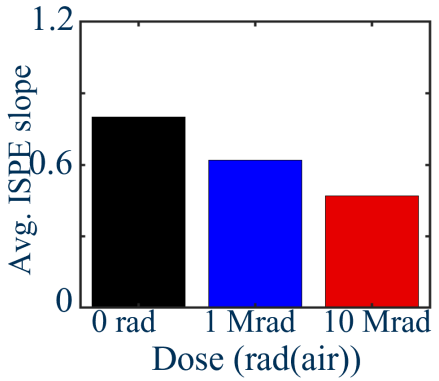






ISPE Characterization





ISPP and ISPE slope reduced after irradiation

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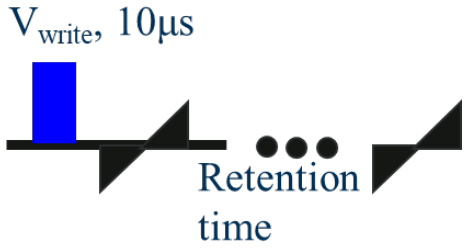
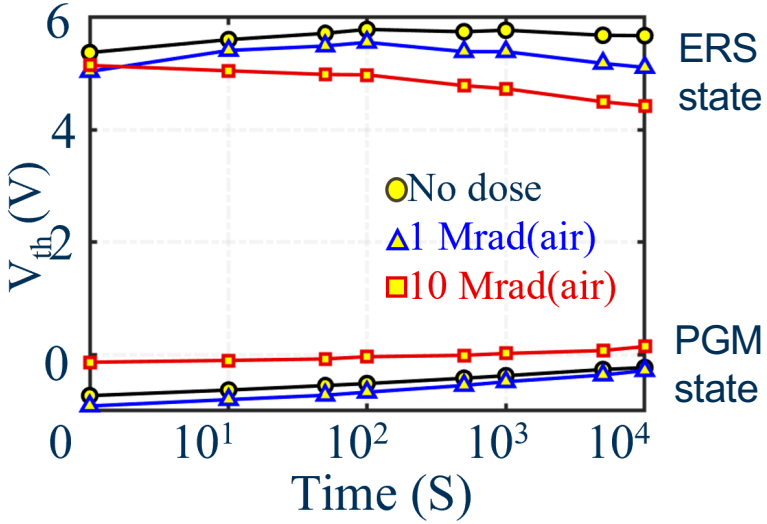
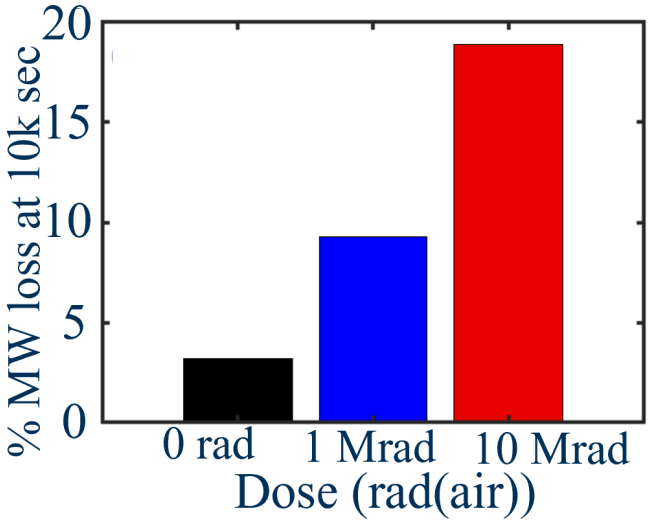
Impact of TID on Data Retention







High trap concentration due to TID □ Depolarization field increases □ Retention loss increases

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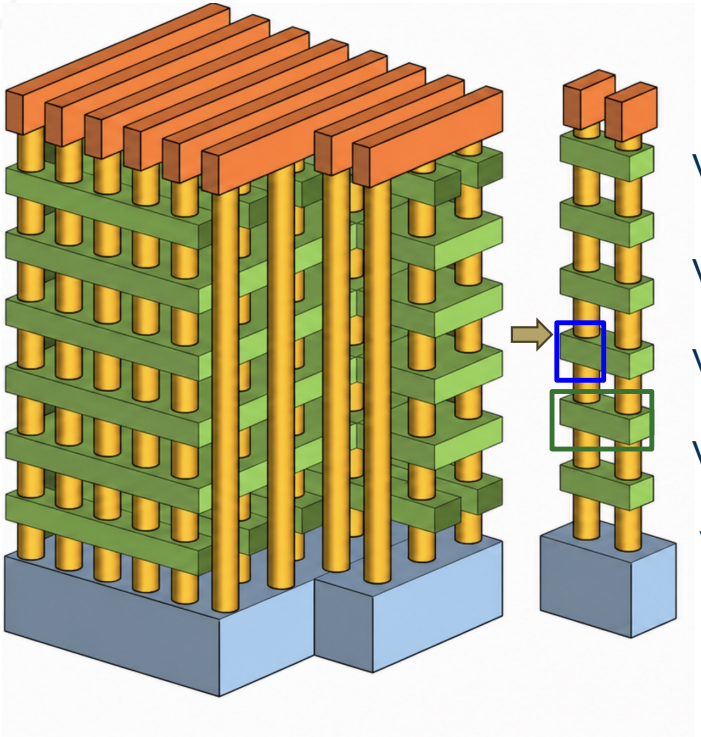
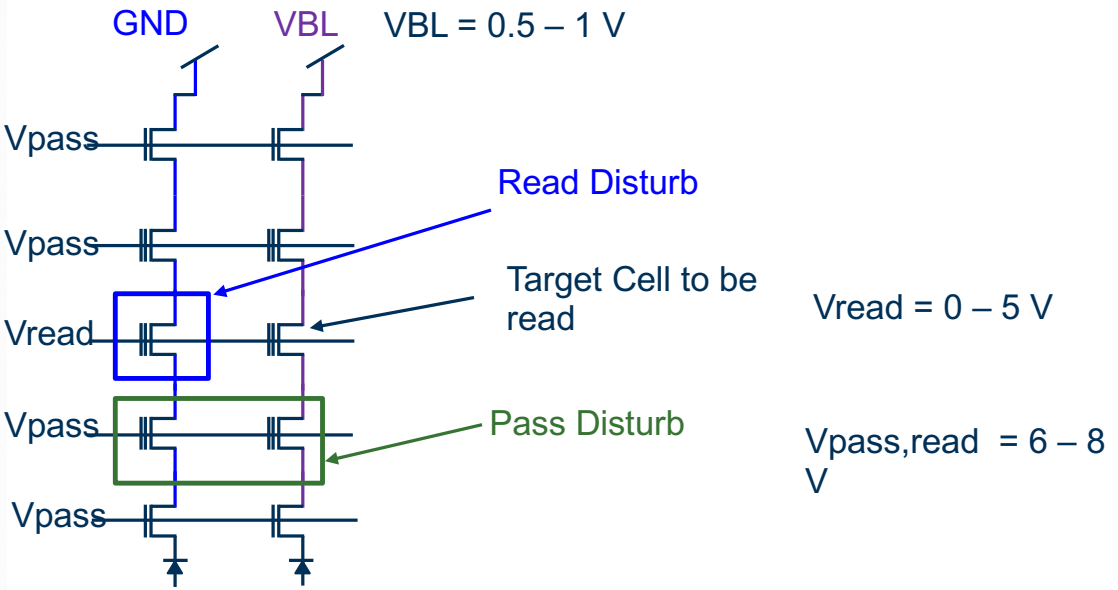
Impact of TID on Disturb





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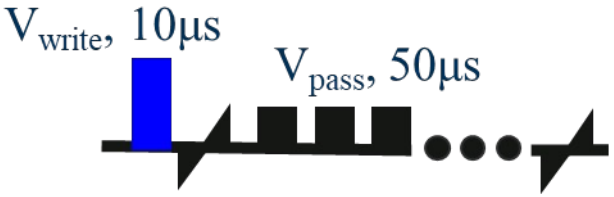
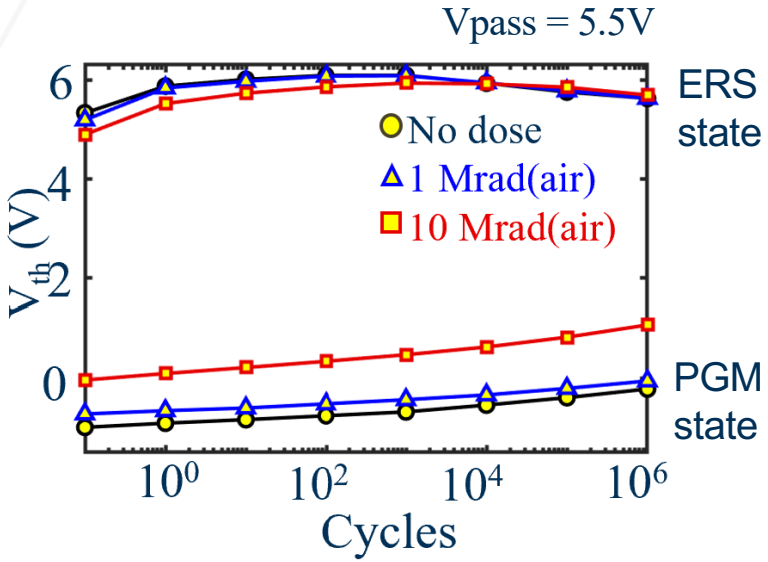
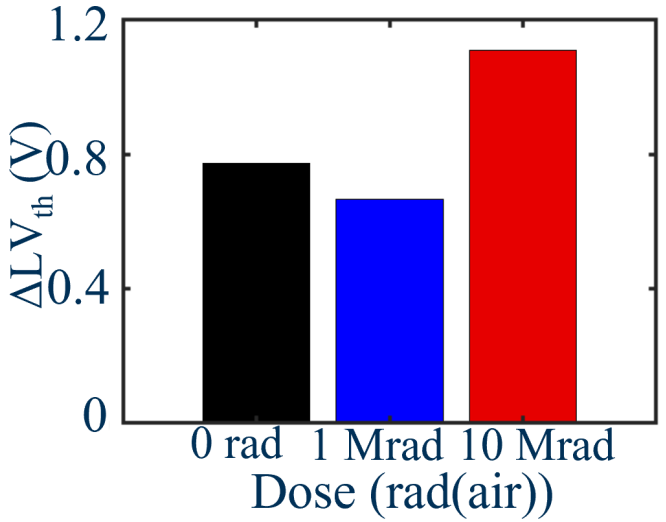
Impact of TID on Disturb







Higher TID increase trap concentration near channel-IL □ Higher electron trapping near the IL □ Larger Vth shift in PGM state

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SPACE STORAGE | CELL-LEVEL EVIDENCE

Space applications and ferroelectric NAND flash

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Letter

Enabling Radiation Hardness in Solid-State NAND Storage Utilizing a Laminated Ferroelectric Stack

Lance Fernandes,* Stuart Wodzro, Prasanna Venkatesan, Priyankka Ravikumar, Ming-Yen Lee, Minji Shon, Dyutimoy Chakraborty, Taeyoung Song, Sanghyun Kang, Salma Soliman, Mengkun Tian, Jason Yeager, Jackson Adler, Jiayi Chen, Zekai Wang, Douglas Wolfe, Shimeng Yu, Andrea Padovani, Suman Datta, Biswajit Ray, and Asif Khan*

Cite This: https://doi.org/10.1021/acs.nanolett.5c05947

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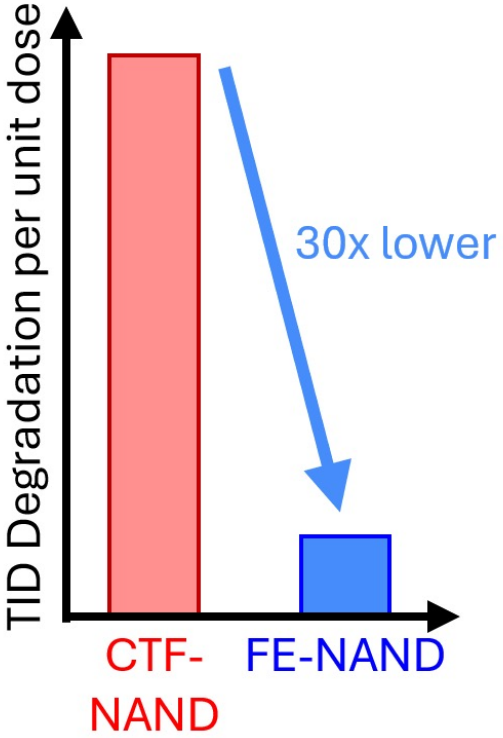
Lance Fernandes



Fernandes, Lance, et al. "Enabling Radiation Hardness in Solid-State NAND Storage Utilizing a Laminated Ferroelectric Stack." *Nano Letters* 26.10 (2026): 3390-3397.

Toward flight-qualified FeNAND: what's next

A high cell-level TID number is only the starting point; qualification must span mechanisms, combined stress, arrays and predictive models.

1

BEYOND TID

- Heavy ions: SEE cross-section vs. LET; SEGR at ±15 V
- Single-event polarization upset—the Fe-specific test
- Proton/neutron damage: V_o and o-phase stability

2

COMBINED STRESS

- TID on fatigued and imprinted cells—not pristine
- −55 to +125 °C; 85 °C retention → 10 years
- Biased in-situ irradiation; low-dose-rate and rebound

3

DEVICES → ARRAYS

- RBER tails vs. dose → define the ECC budget
- Vertical macaroni channel + full-string disturb
- Rad-hard charge pump: ~100 krad vs. ~1 Mrad cell

4

PREDICTIVE MODELS

- Independent trap metrology: CP, DLTS, EPR and XPS
- Replace fitted efficiency with measured physics
- FeNAND vs. CTF—same chamber and dosimetry

Sources: NASA NEPP NAND studies (2019, 2023); laminated FeNAND radiation study

AI in space needs a new storage foundation

FeNAND could combine data-center density with radiation resilience built into the memory cell.

- AI is moving into space, where onboard sensing, inference and autonomous decision-making will require large, persistent and trustworthy storage.
- Conventional NAND flash is not intrinsically radiation tolerant; qualified true-SLC can exceed 60 krad(Si), but only at gigabyte-scale capacity.
- Ferroelectric NAND stores information in polarization and has demonstrated a nearly stable memory window through approximately 1 Mrad at the cell level.
- Work is now focused on heavy-ion effects, combined radiation and cycling, temperature-dependent retention, array-level reliability and radiation-hard peripheral circuits.

Sources: 3D PLUS; HPE/KIOXIA; Fernandes et al., Nano Letters (2026)

Our team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Dr. Sarah Lombardo (TEL)


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(U Colorado Boulder)

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