Pushing the limits of vertical NAND scaling with *Ferroelectrics*

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IWCM^2 (14th International Workshop on Characterization and Modeling of Memory Devices)
October 3, 2025 | University of Milano-Bicocca, Italy

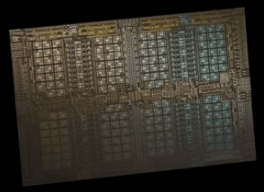
Georgia Tech

Memory technologies – The state of the art

1

Memory

Hyperscale AI, and High-performance Computing



HBM3E: 12-high, 24 GB

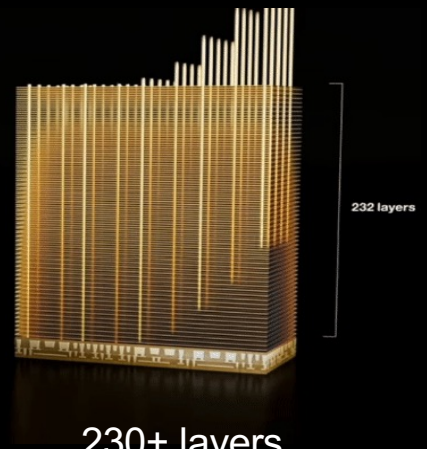
Total 192 GB, 1.18 TB/s

Source: NVIDIA

2

Storage

Client, Mobile, and Enterprise



230+ layers

2.4 GB/s

Source: Micron

3

Embedded

Automotive

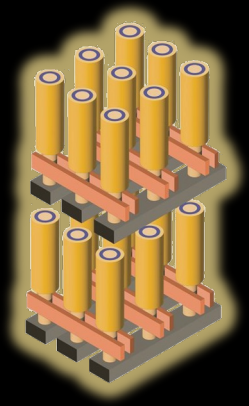
14nm eMRAM

16 MB

Source: Forbes

4

Emerging Memory



Ferroelectric NV-DRAM

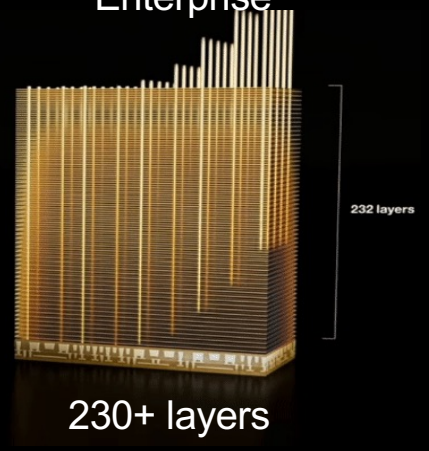
32 Gb, 3D-stacked, multi-layer

Source: IEDM 2023

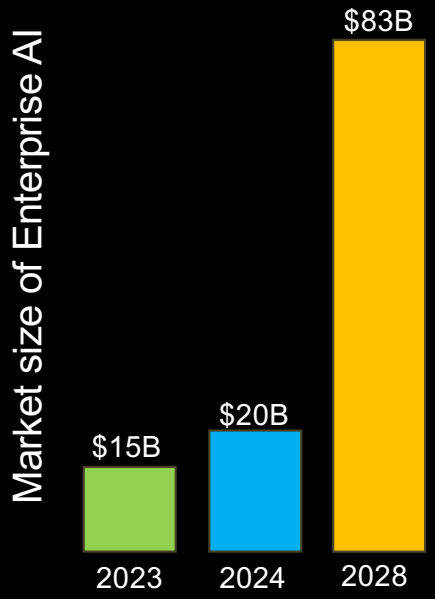
The NAND Storage Technology

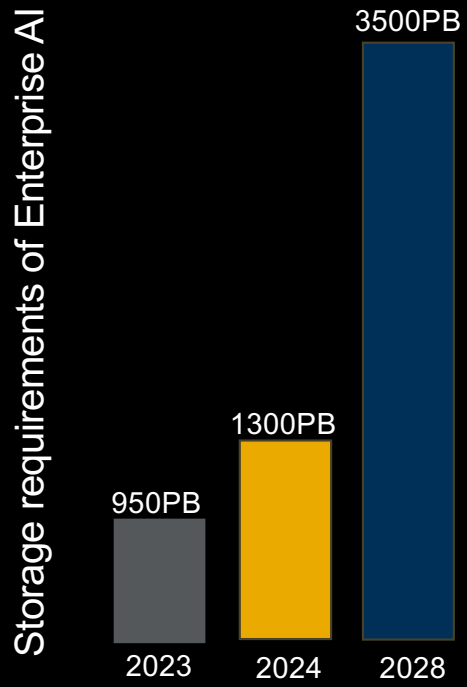
Storage

Client, Mobile, and Enterprise



Source: Micron

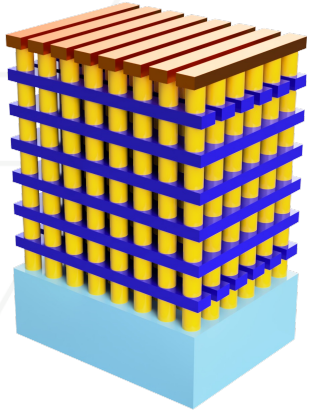




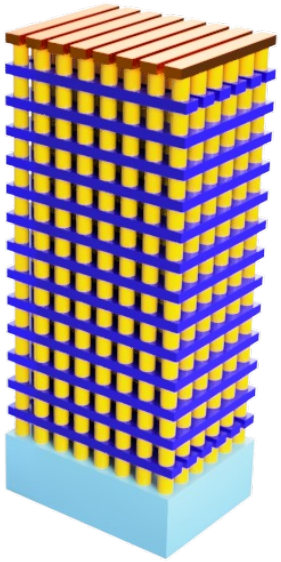
Source: The Business Research Company

Processing and storing data in AI effectively and cost efficiently can require HBM for the actual AI training, but also various types of NAND-based solid-state storage to support the data flows needed to and from the HBM.

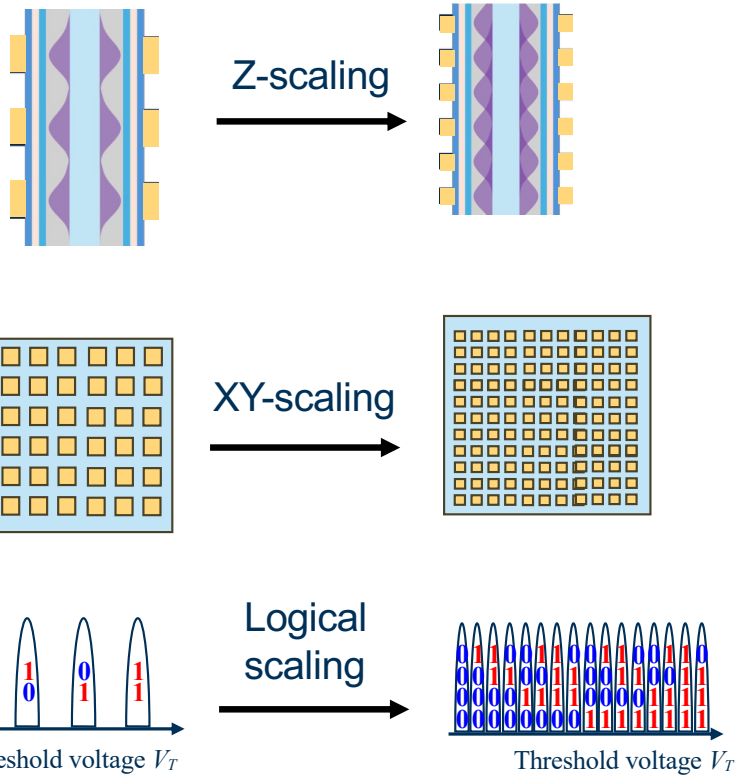
Vertical NAND Scaling



2014
First 3D NAND, Samsung
24 Layers, MLC



2022-2025
Production
Samsung 236L TLC
SK hynix 238L TLC → 321L (ramping 1H25)
Micron 276L TLC
Prototype / R&D demos:
SK hynix 321L sample (FMS 2023)
SK hynix 300+L demo (ISSCC 2023)
Kioxia / WD >300L demo (VLSI 2023)



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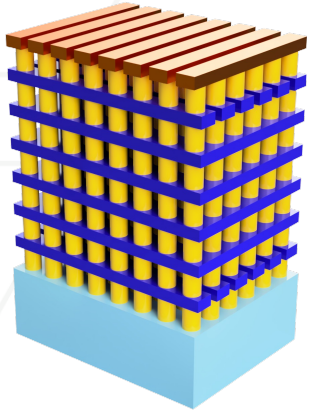
Vertical NAND Scaling



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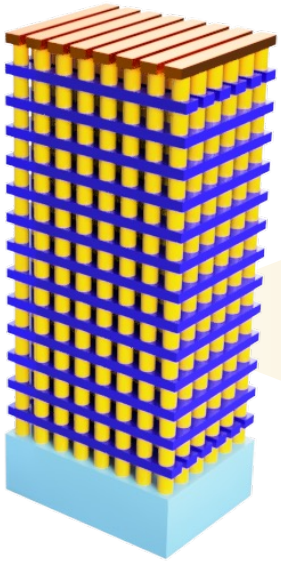

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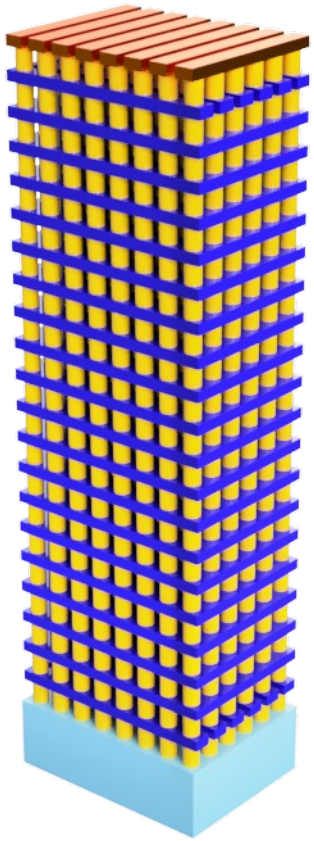

2030
Roadmap: >1000L (IEDM)

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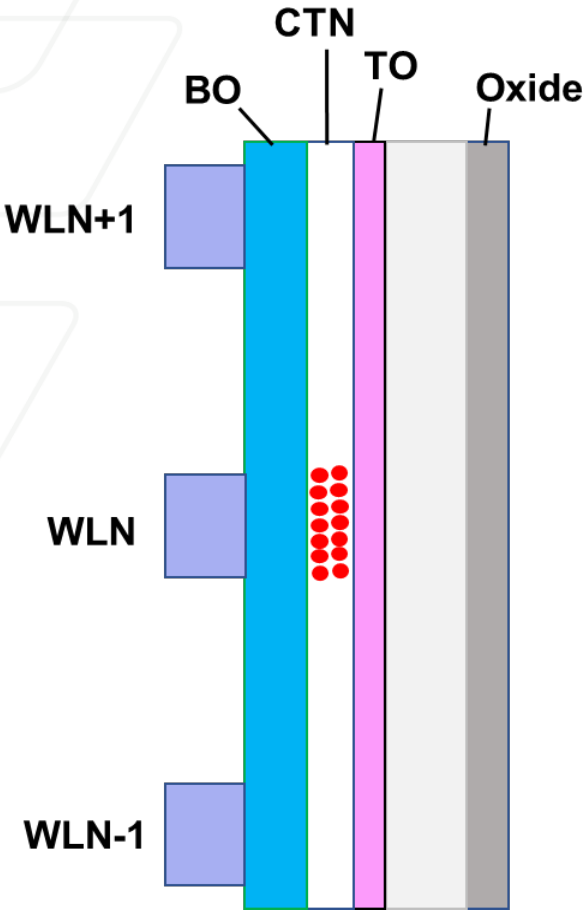
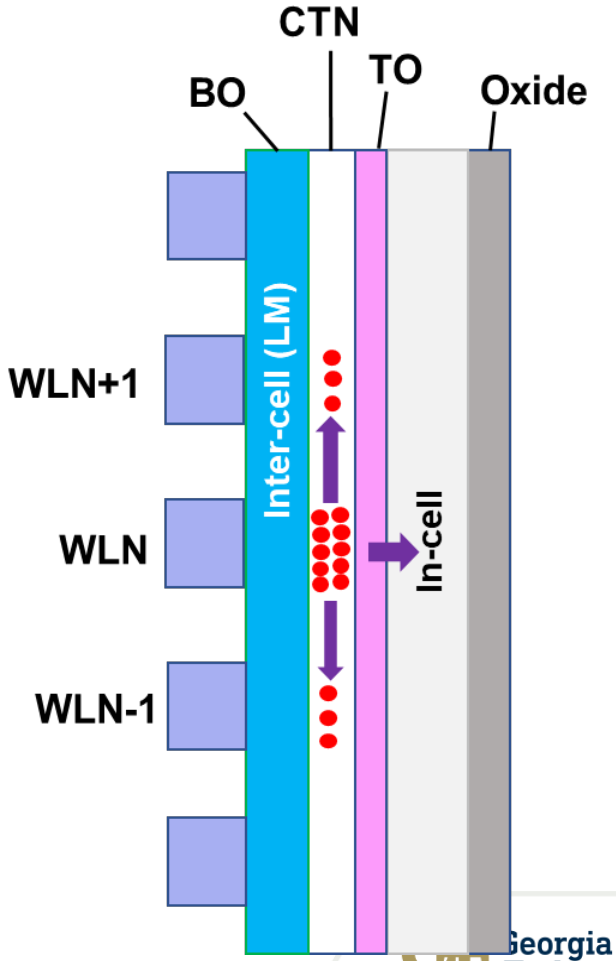
Challenges of vertical NAND flash scaling

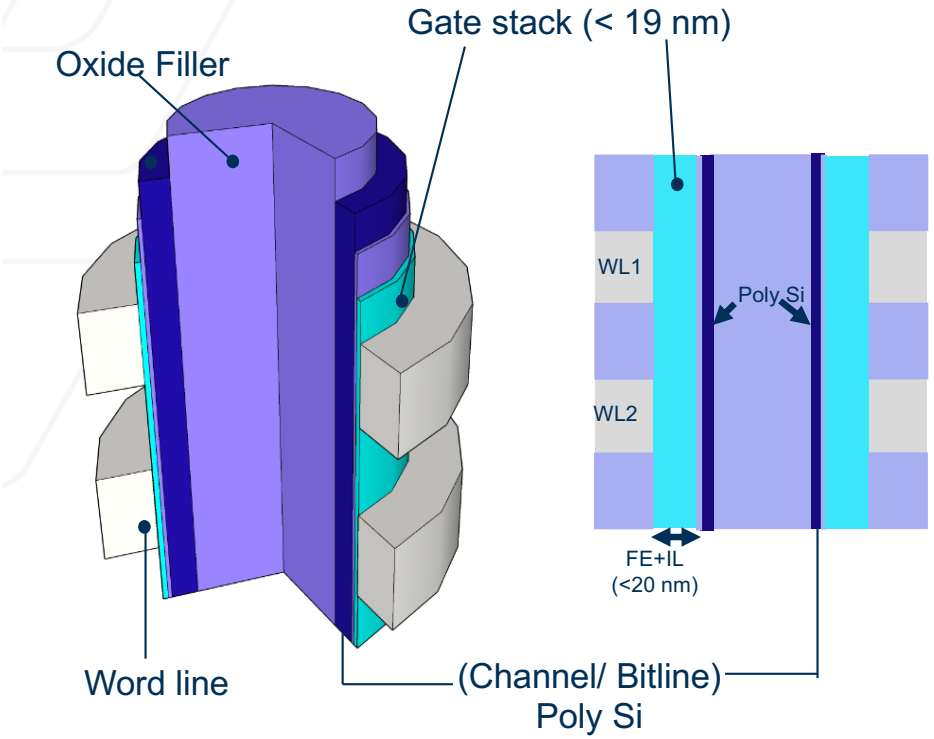


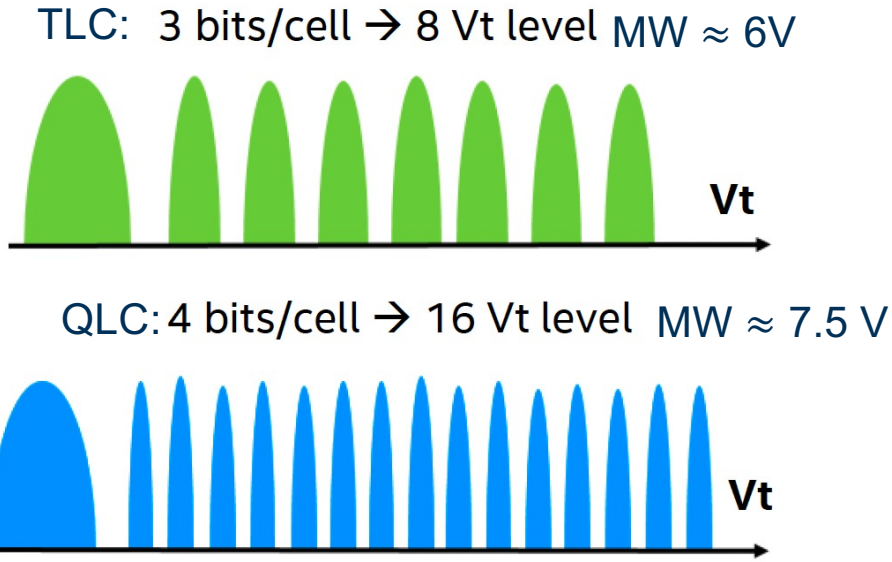
Z-scaling

1. Lateral charge migration
2. Inter-WL reliability
3. High write voltage
4. Endurance
5. Device-device variation



The future of NAND flash technology





To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm

Design constraints

Gate stack thickness, $t \leq 19$ nm

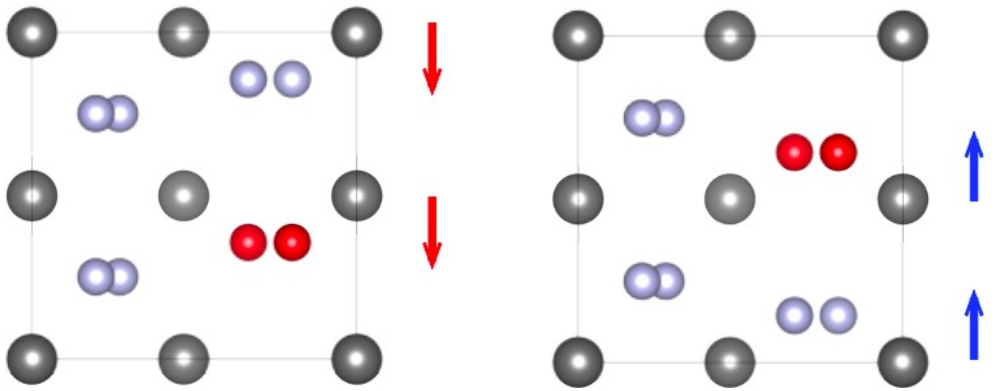
Write voltage ≤ 15 V

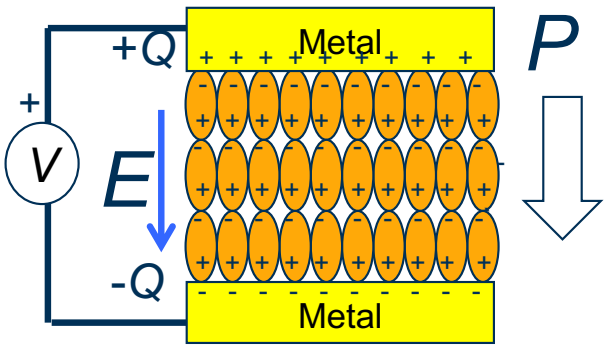
Memory window, MW ≥ 6.5 V

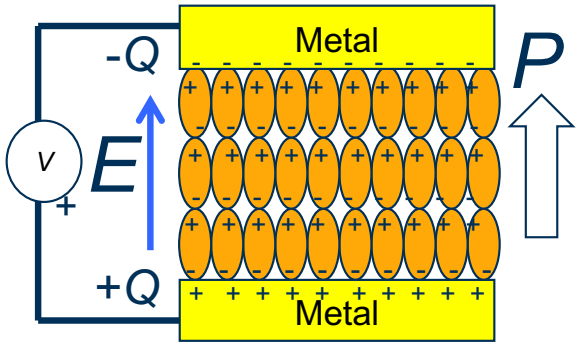
Ferroelectricity

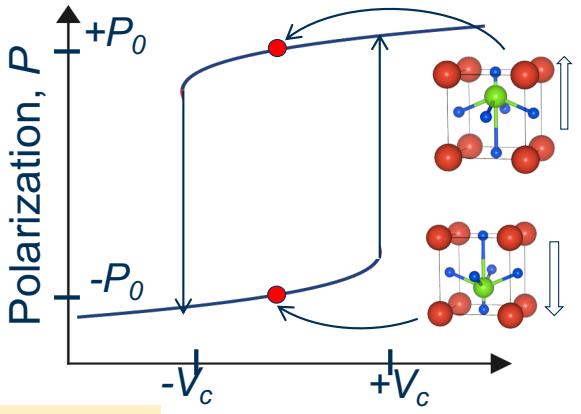
CMOS compatible HfO_2-based fluorite-structure ferroelectric

Orthorhombic *Pca2₁* structure









A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

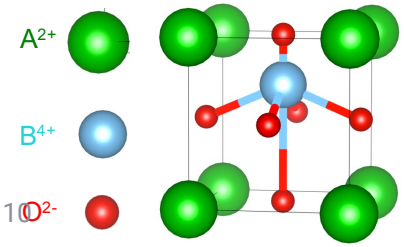
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for for code storage in microcontrollers.

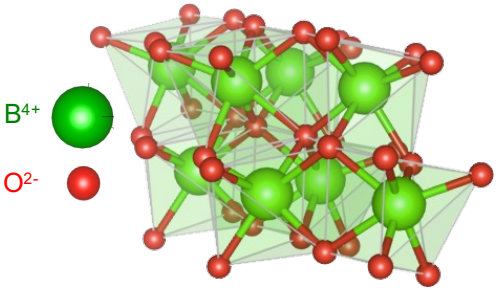
2. Controlled annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al. Appl. Phys. Lett*. 99, 112904 (2011)
- Boscke *et al. 2011 IEEE Int. Electron Devices Meeting.* p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al. Nano Lett.* 12, 4318 (2012)

Perovskite-structure ferroelectric oxide (ABO_3)



Fluorite-structure ferroelectric oxide (BO_2)



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2011→2023

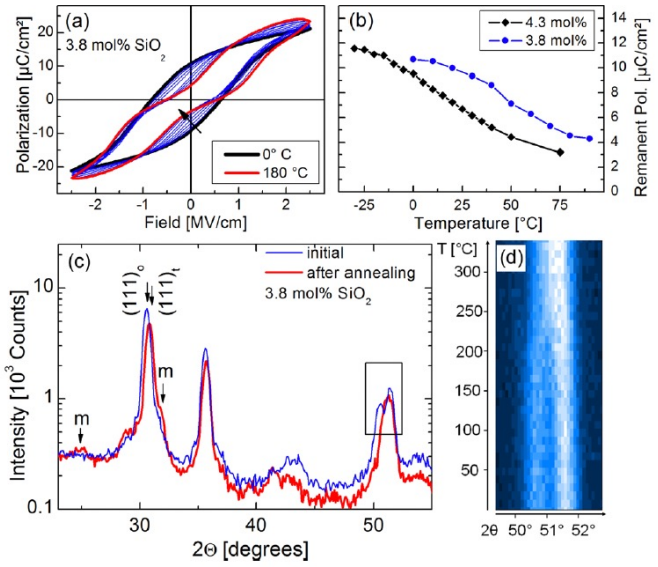
Discovery of Ferroelectricity in HfO2

APPLIED PHYSICS LETTERS **99**, 112904 (2011)

Phase transitions in ferroelectric silicon doped hafnium oxide

T. S. Böscke,[1,2,a),b)] St. Teichert,[3,b)] D. Bräuhaus,[4] J. Müller,[5] U. Schröder,[2,b)] U. Böttger,[4] and T. Mikolajick[2,6]
[1]*Löberwallgraben 2, 99096 Erfurt, Germany*
[2]*Namlab gGmbH, 01187 Dresden, Germany*
[3]*UAS Jena, Department of SciTec, 07745 Jena, Germany*
[4]*RWTH Aachen, Institut für Werkstoffe der Elektrotechnik, 52062 Aachen, Germany*
[5]*Fraunhofer Center Nanoelectronic Technologies (CNT), 01099 Dresden, Germany*
[6]*Department of Nanoelectronic Materials, University of Technology Dresden, 01062 Dresden, Germany*

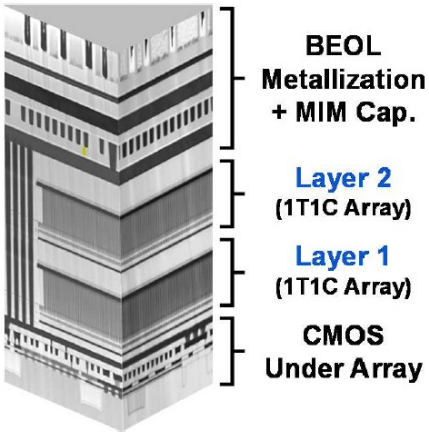
(Received 18 July 2011; accepted 19 August 2011; published online 15 September 2011)

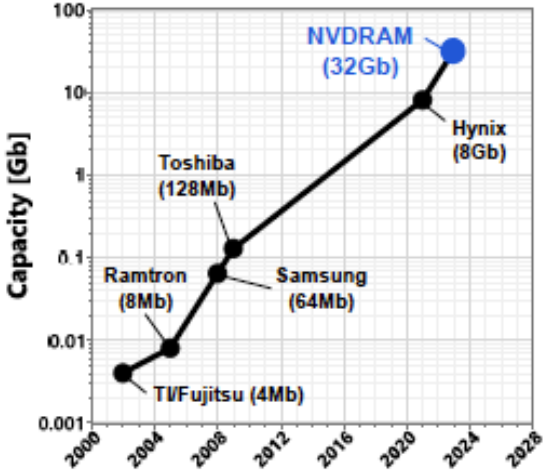


Demonstration of high-density Ferroelectric RAM

NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads

N. Ramaswamy, A. Calderoni, J. Zahurak, G. Servalli, A. Chavan, S. Chhajed, M. Balakrishnan, M. Fischer, M. Hollander, D. P. Ettisserry, A. Liao, K. Karda, M. Jerry, M. Mariani, A. Visconti, B. R. Cook, B. D. Cook, D. Mills, A. Torsi, C. Mouli, E. Byers, M. Helm, S. Pawlowski, S. Shiratake, and N. Chandrasekaran
Micron Technology Inc., Boise, USA, email: dramaswamy@micron.com





Ramaswamy et al. IEDM 2023

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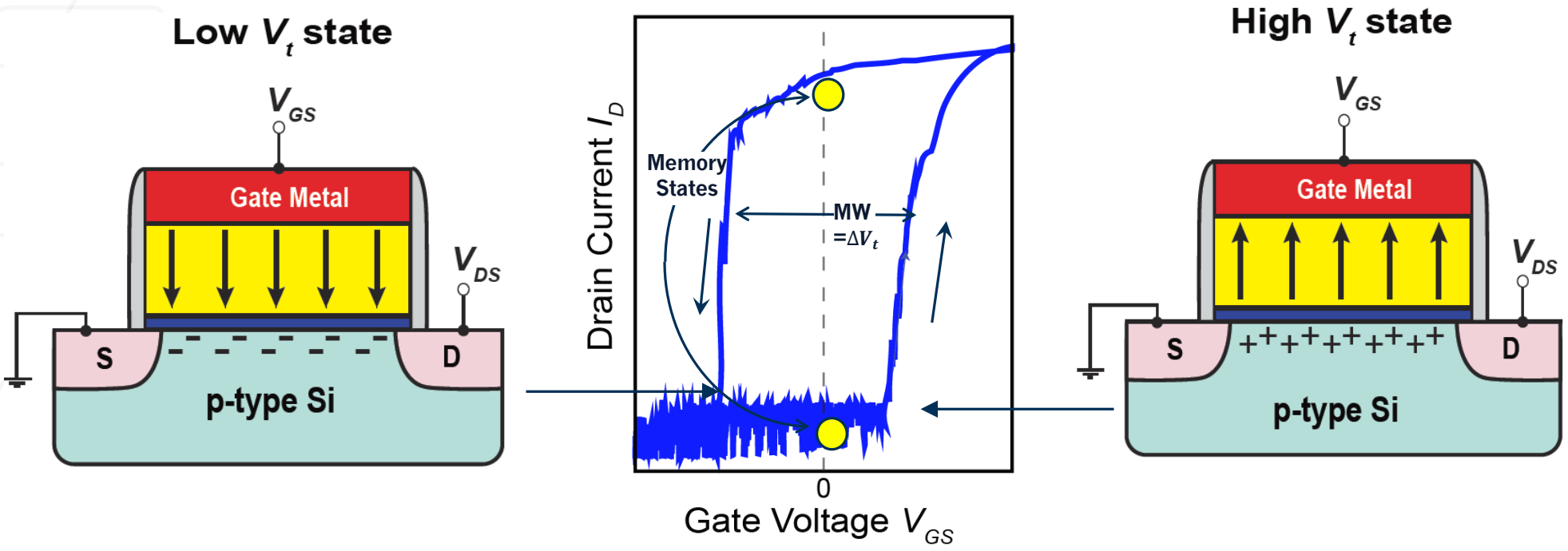
Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the "remnant" polarization.

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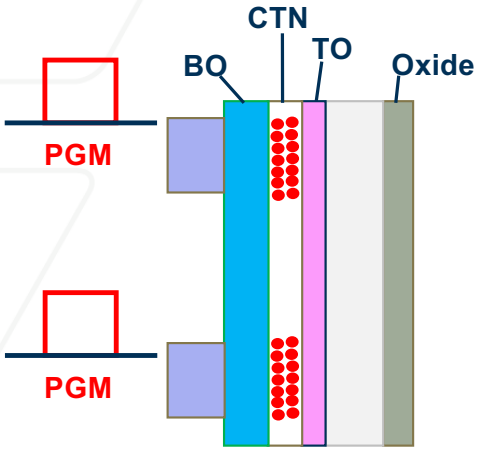
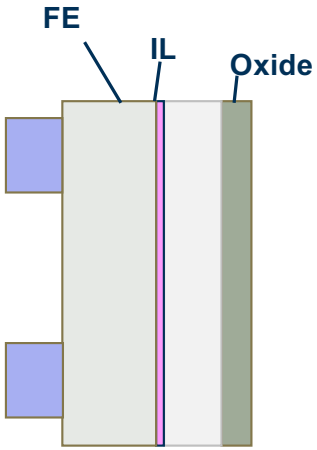
Charge trap flash vs. ferroelectric flash





CTF that stores data in the form of charge.

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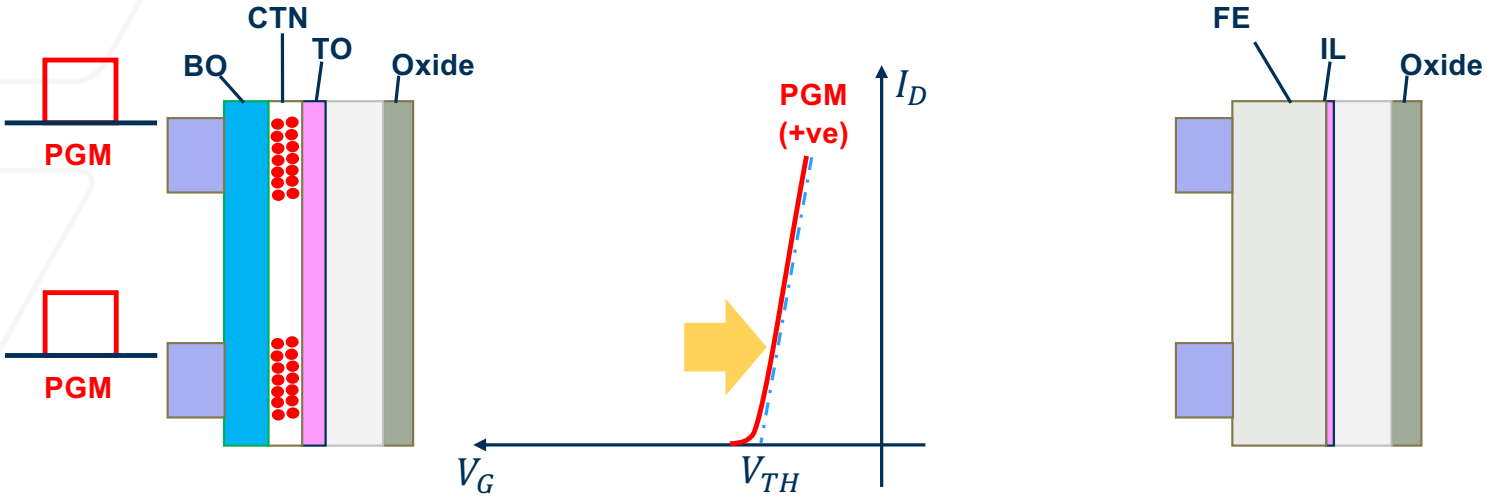
Charge trap flash vs. ferroelectric flash



A Positive PGM pulse sets the Vt to high Vt state in CTF NAND.

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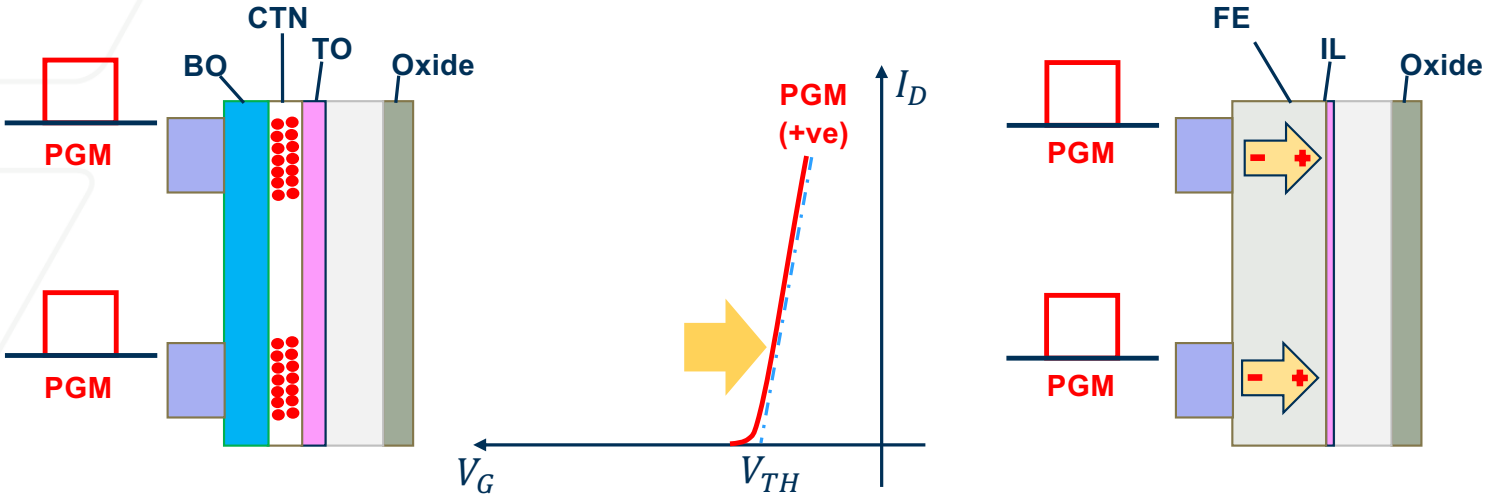
Charge trap flash vs. ferroelectric flash



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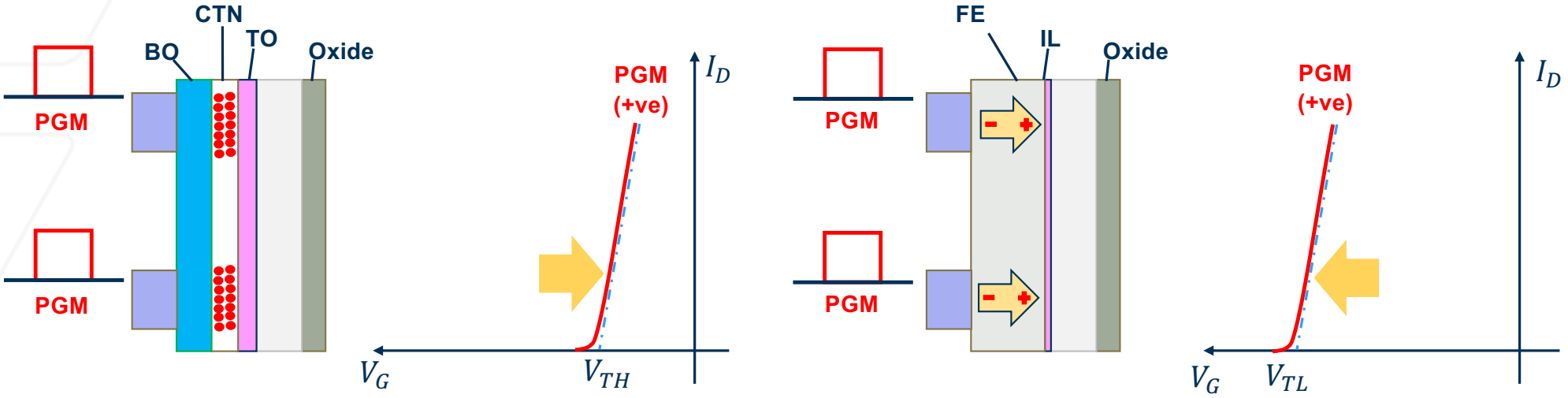

A Positive PGM pulse sets the Vt to high Vt state in CTF NAND.

On the contrary, a Positive PGM pulse sets the Vt to low Vt state in a FEFET.

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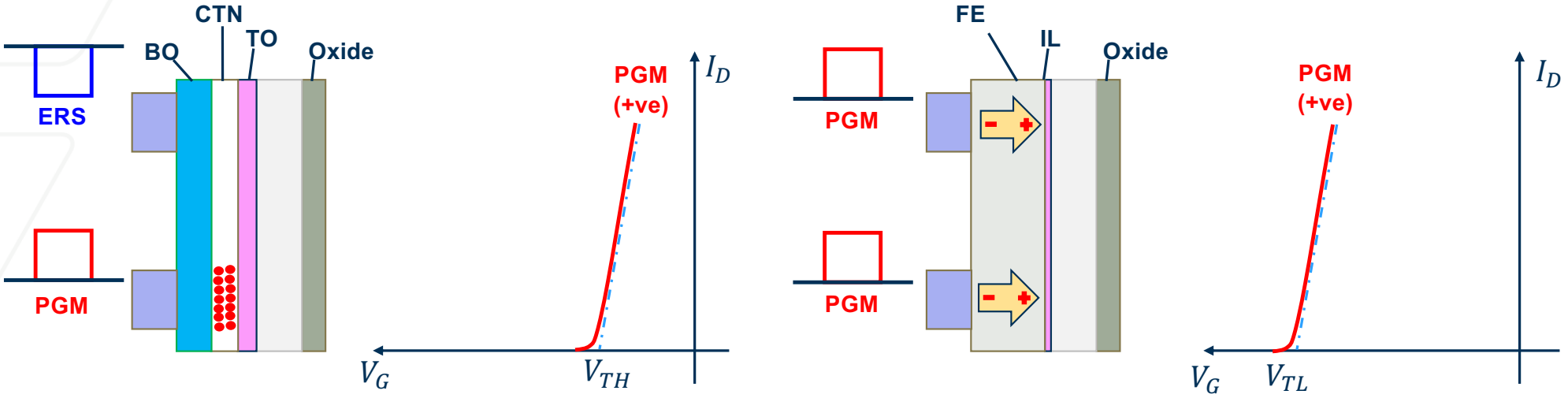
Charge trap flash vs. ferroelectric flash



A Negative ERS pulse sets the Vt to low Vt state in CTF NAND.

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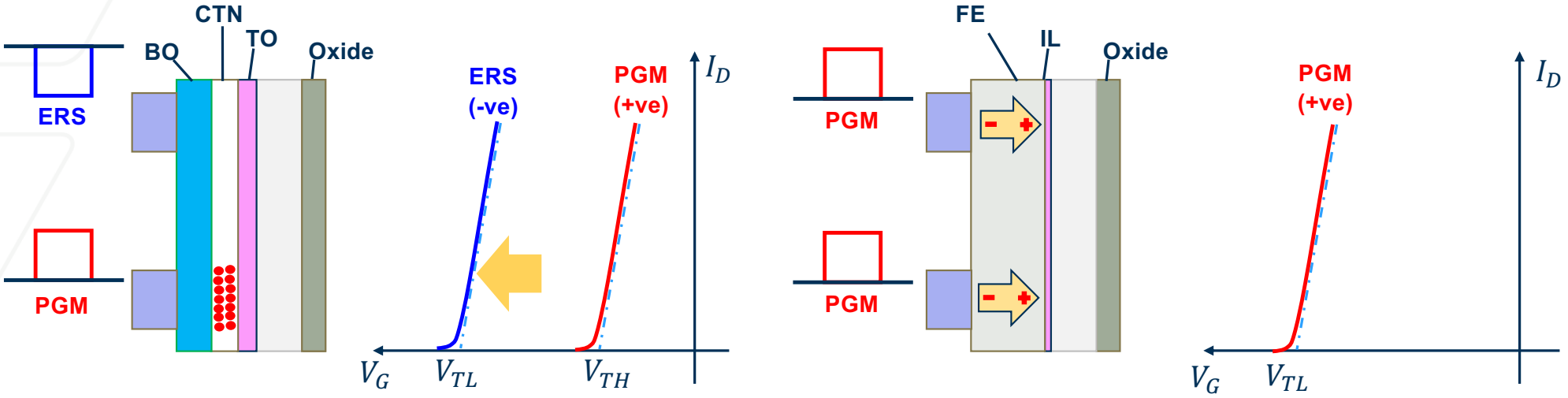
Charge trap flash vs. ferroelectric flash



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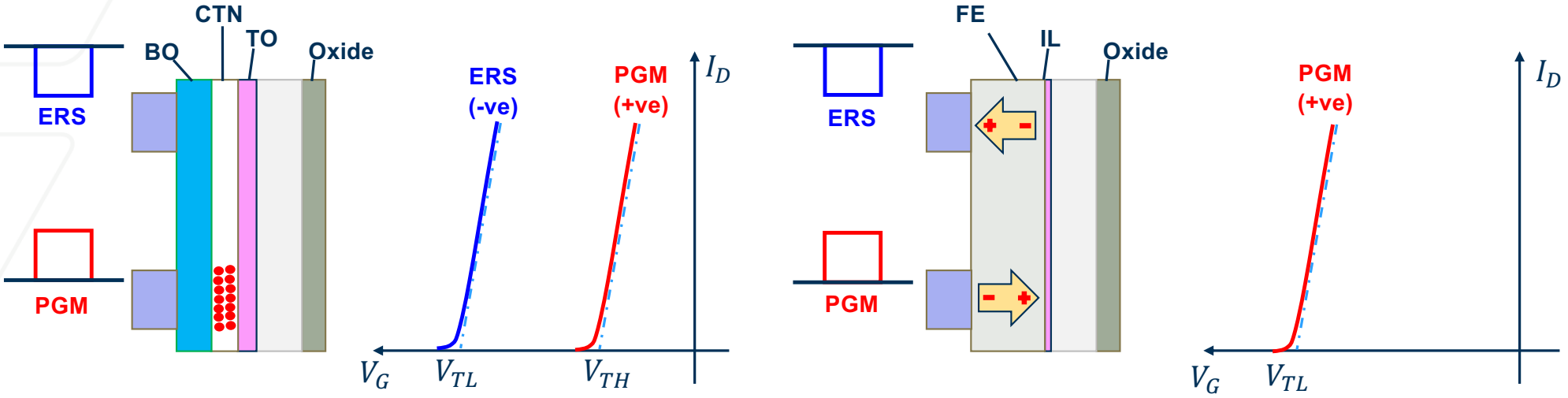
Charge trap flash vs. ferroelectric flash



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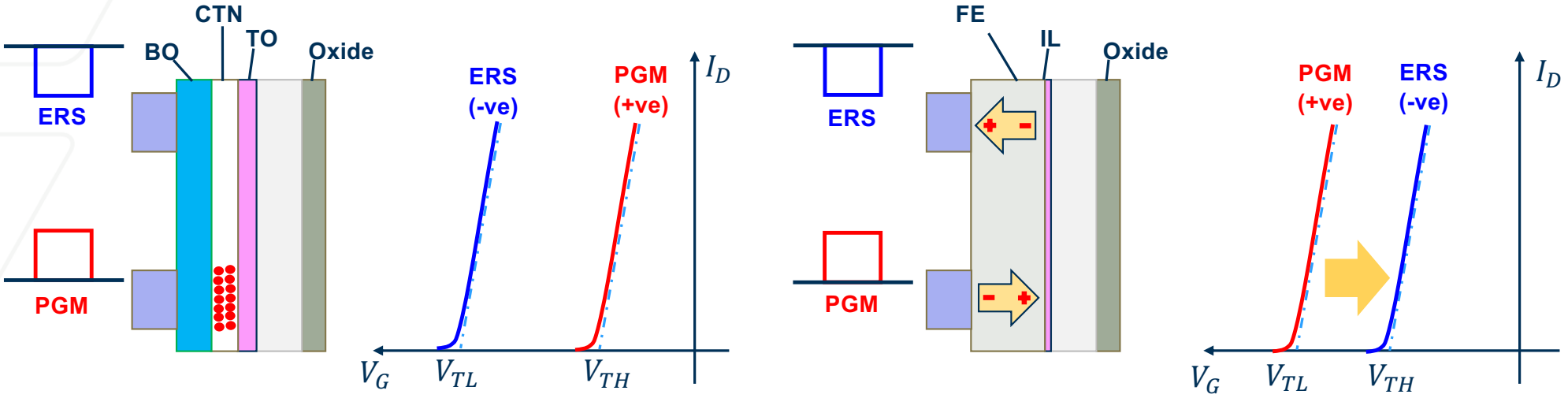
Charge trap flash vs. ferroelectric flash



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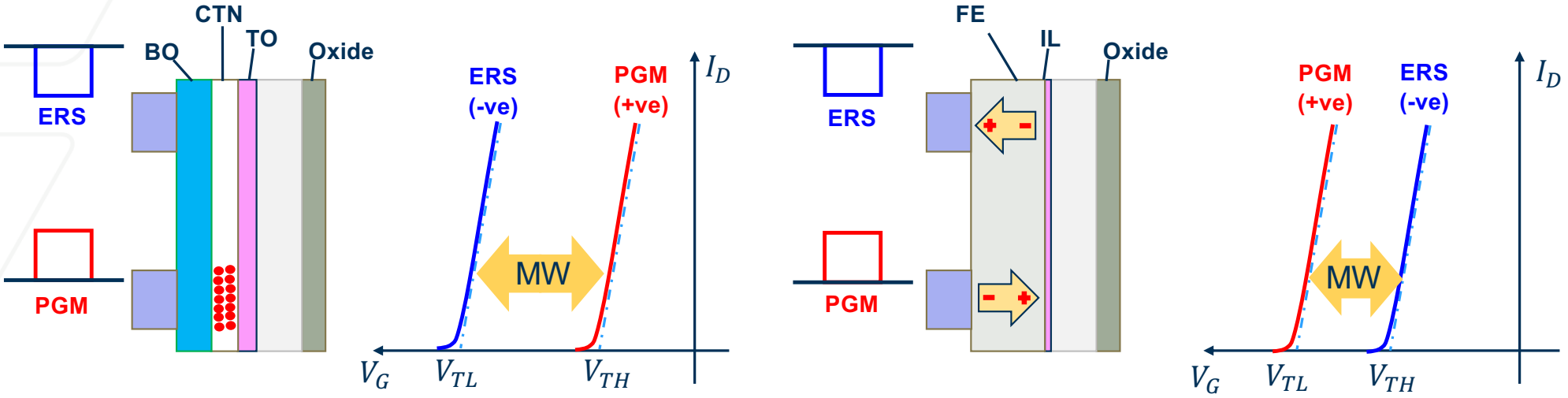

$$MW = V_{TH} - V_{TL}$$

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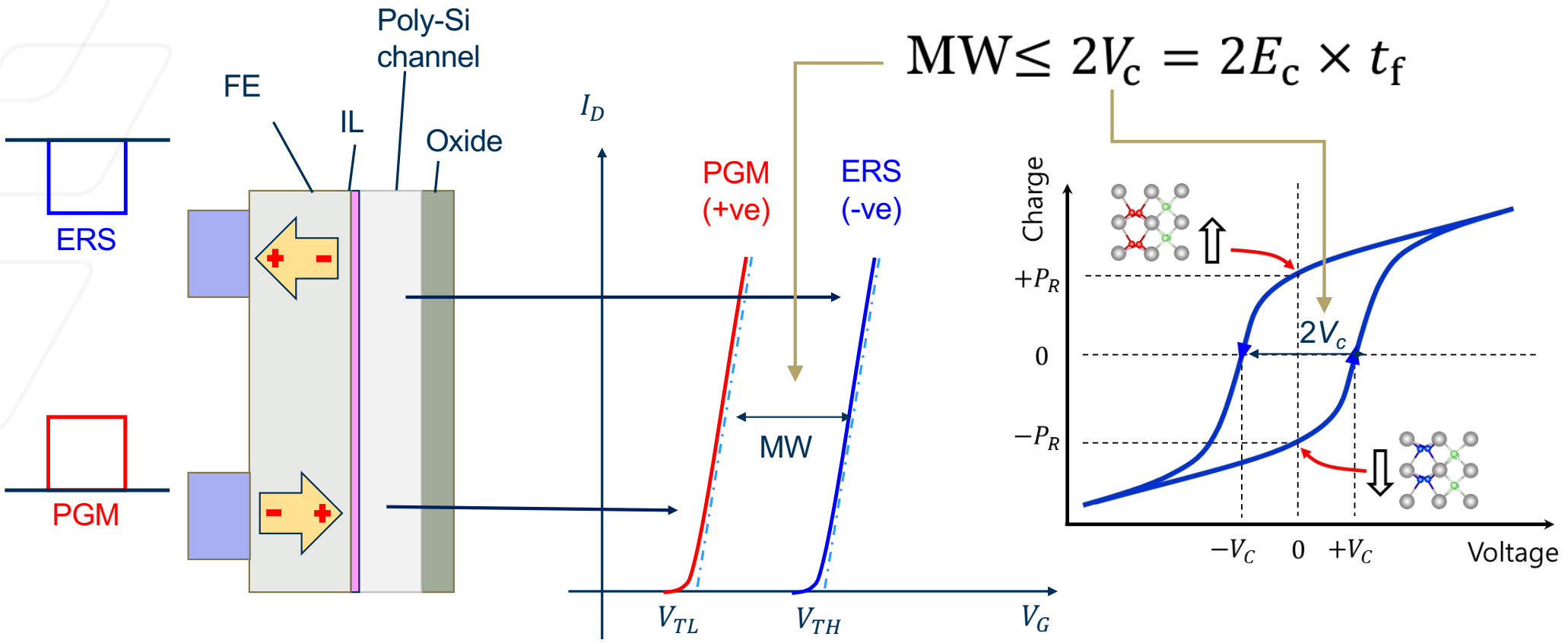
Ferroelectric flash



The maximum memory window of a FeFET is theoretically limited by the memory window of the ferroelectric layer.

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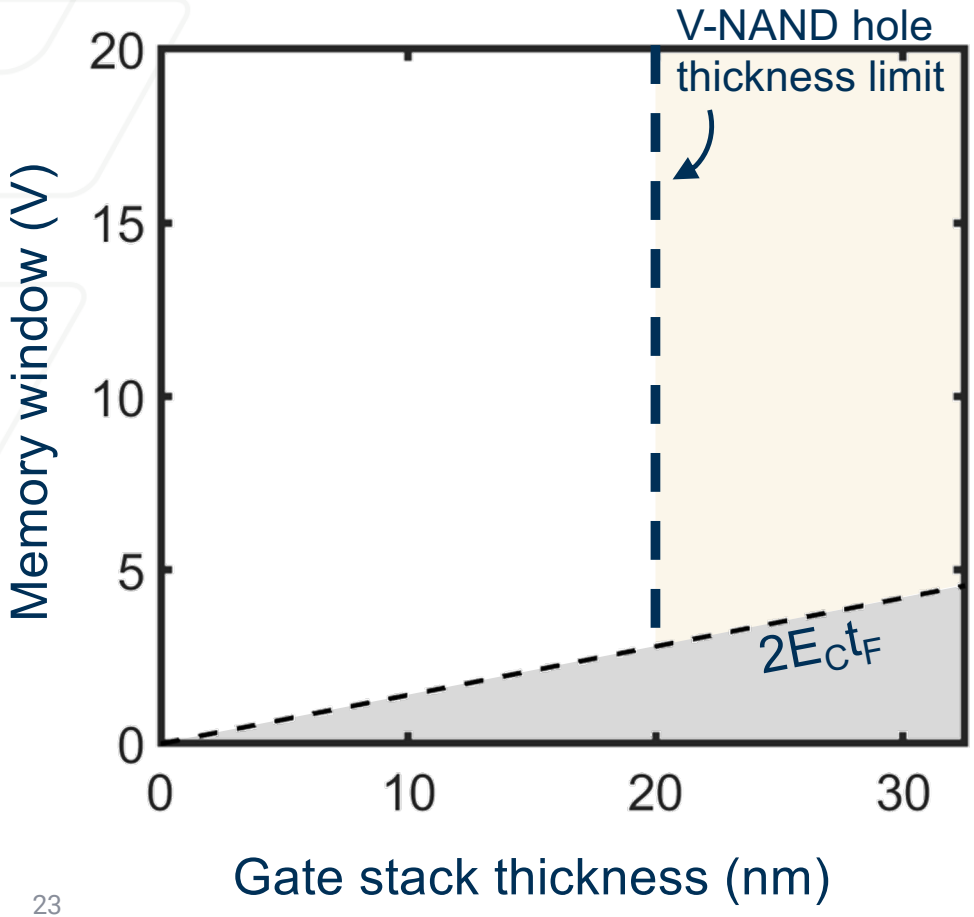
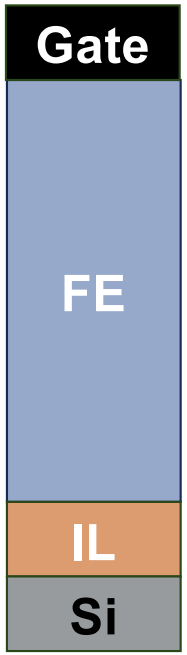
Memory window of FEFETs is limited by V_C

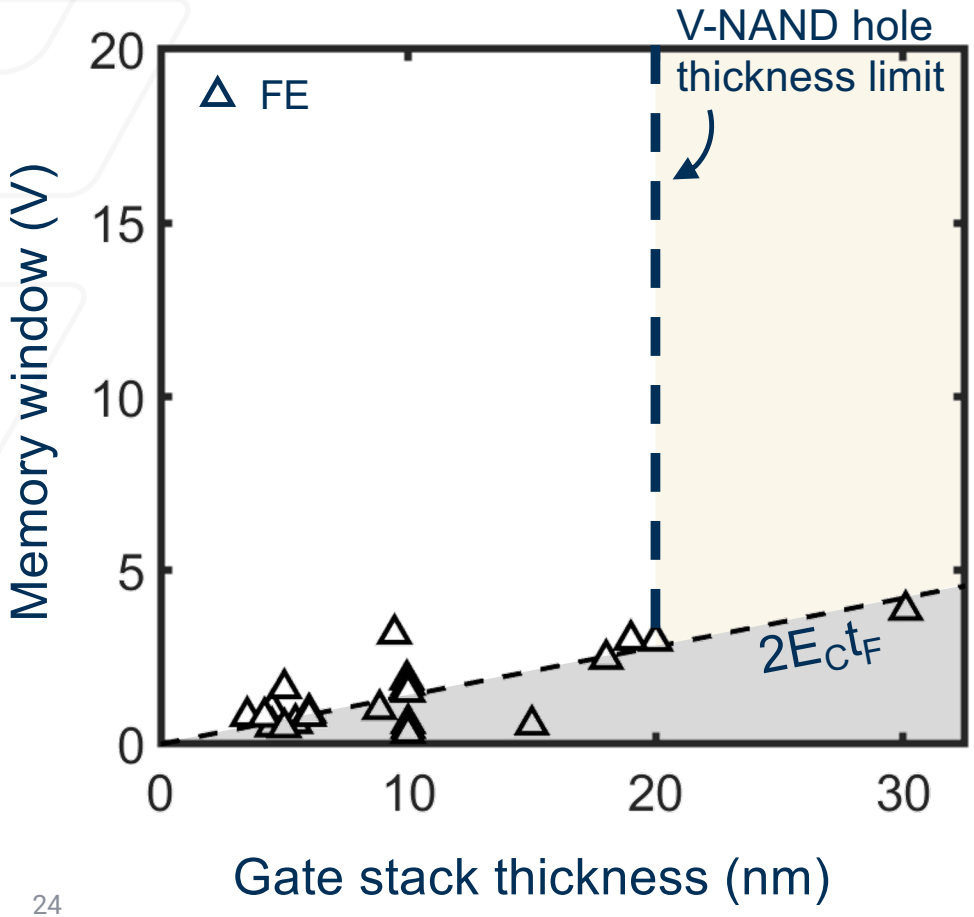


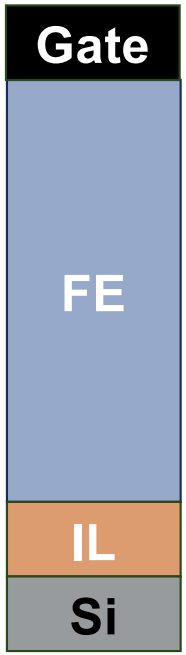


$$\mathrm{MW} \leq 2V_c = 2E_c \times t_f$$

The maximum memory window of an FeFET is theoretically limited by the memory window of the ferroelectric layer.

Memory window of FEFETs is limited by V_C





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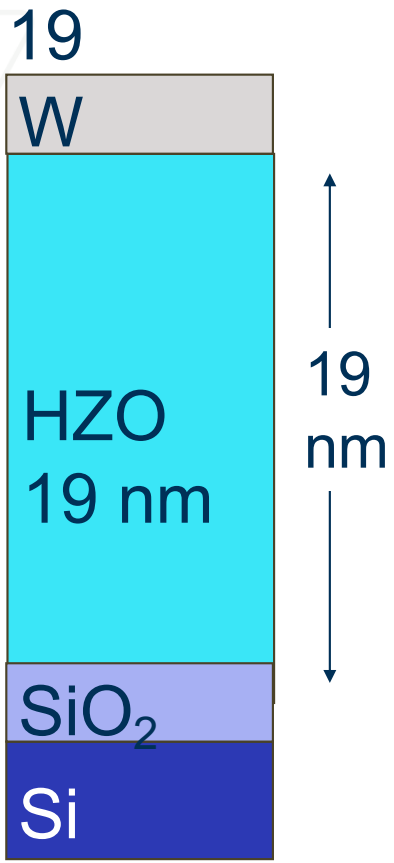
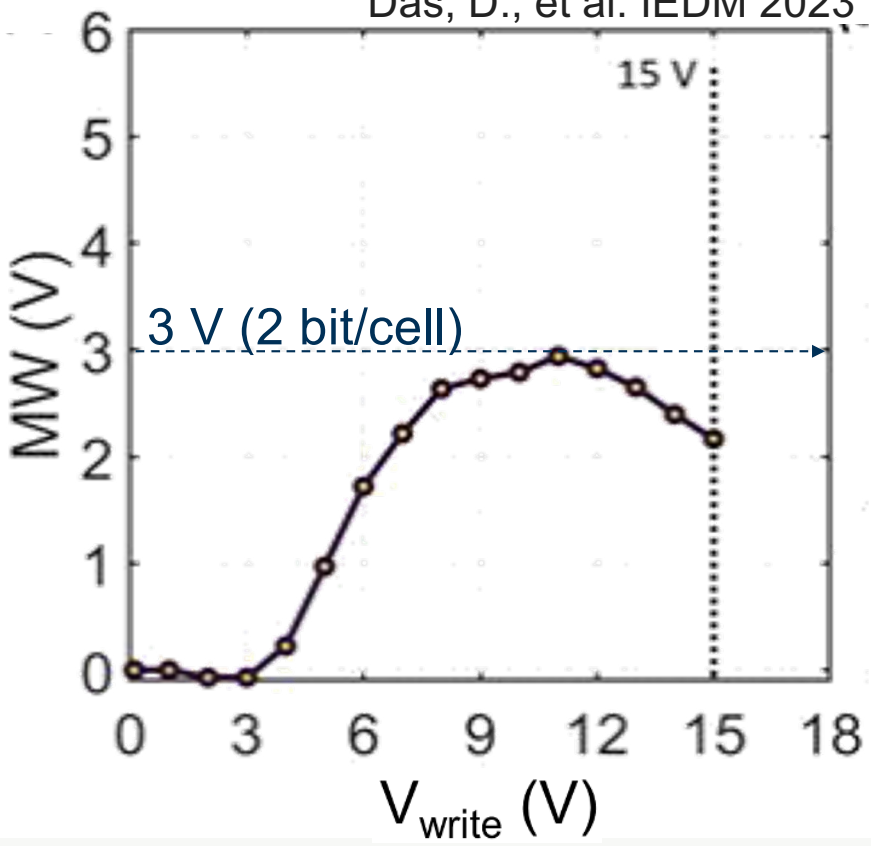
Increasing the MW by dielectric insertion



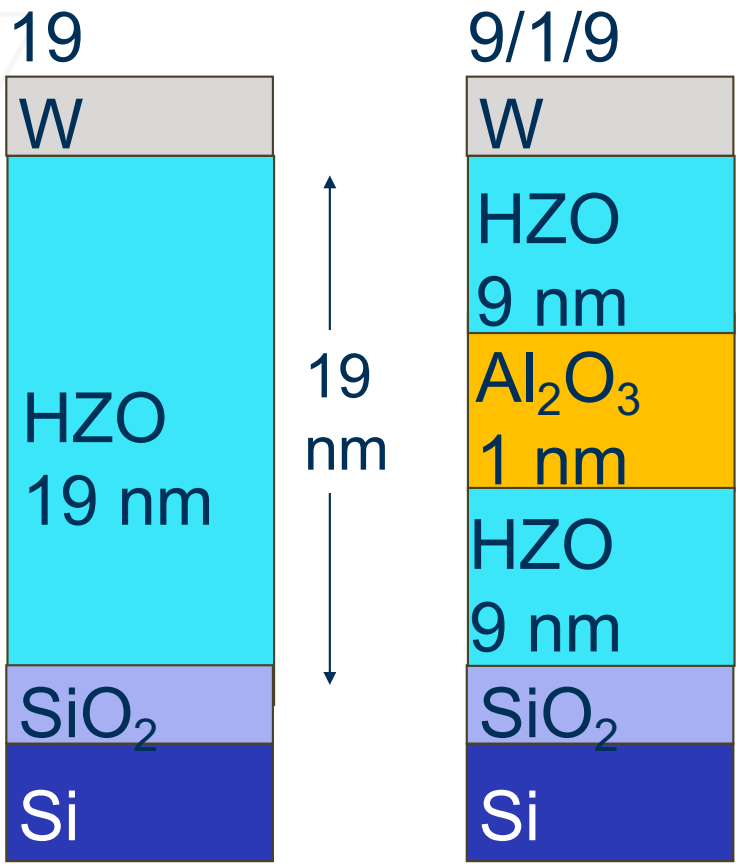
Das, D., et al. IEDM 2023

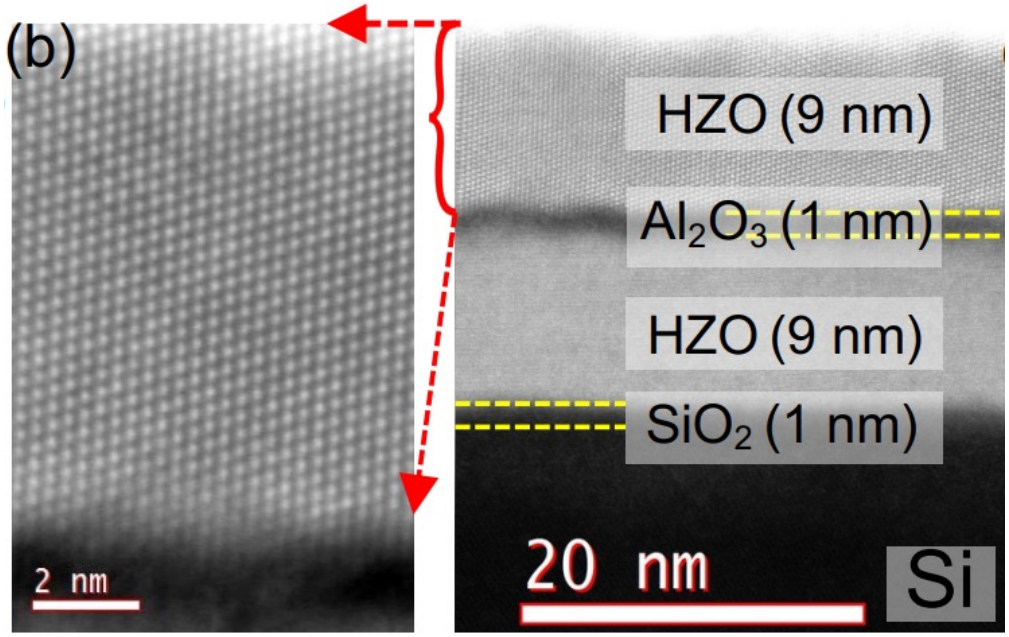


10 nm HZO layer leads to maximum memory window of 2.9 V.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion





Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

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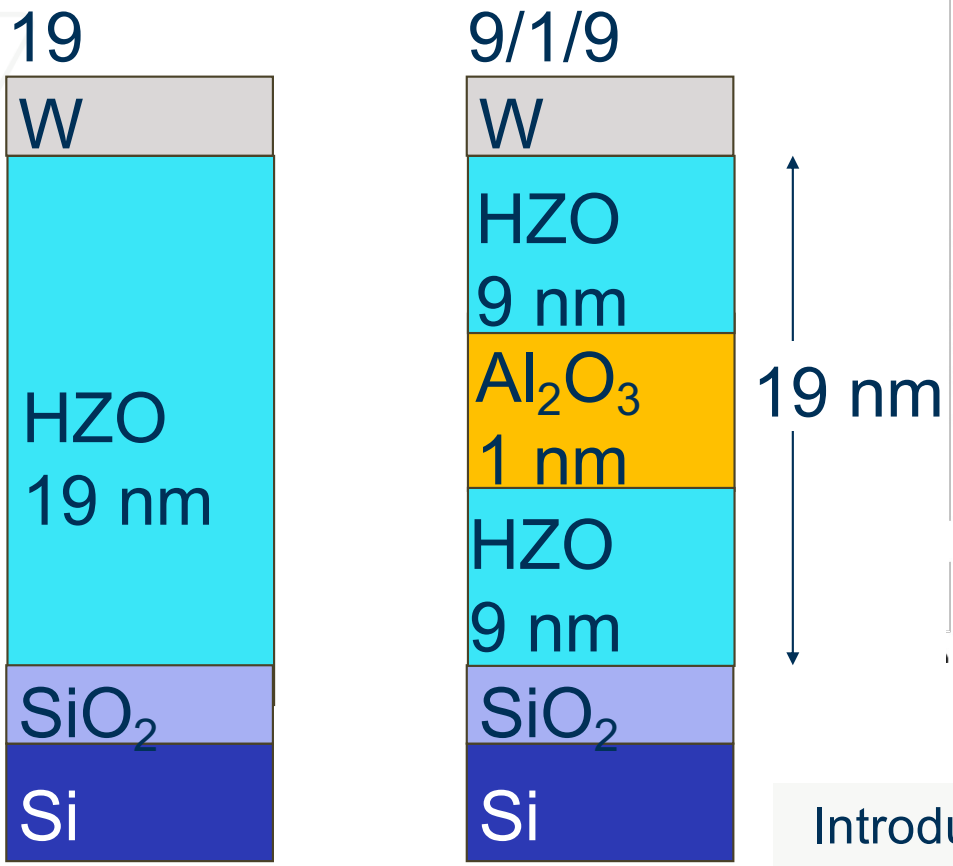
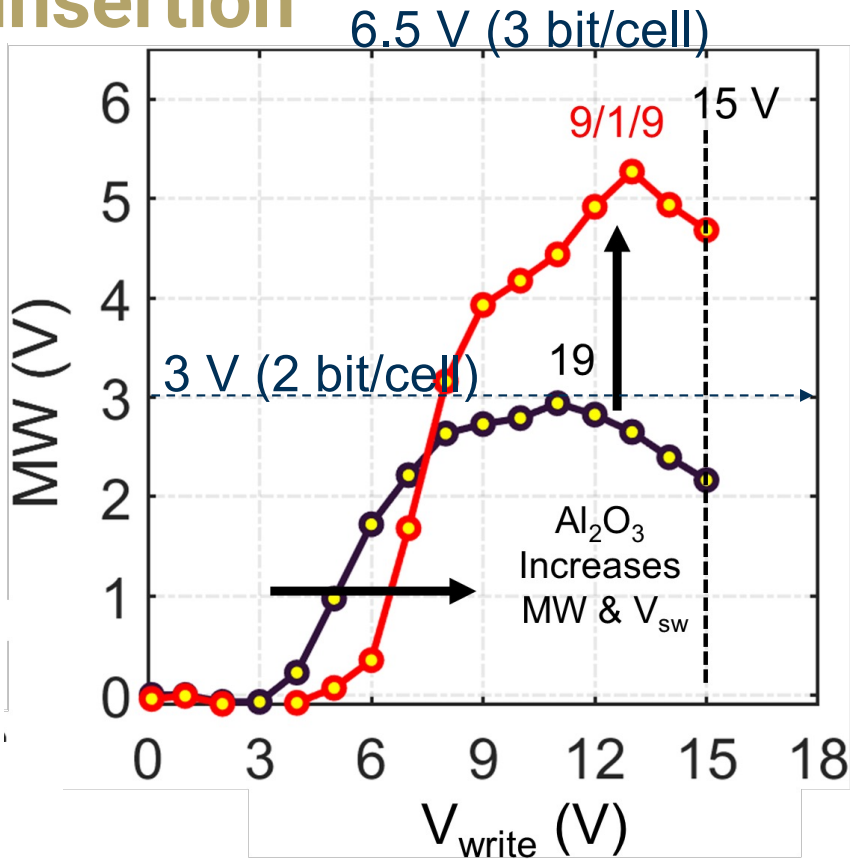
Increasing the MW by dielectric insertion

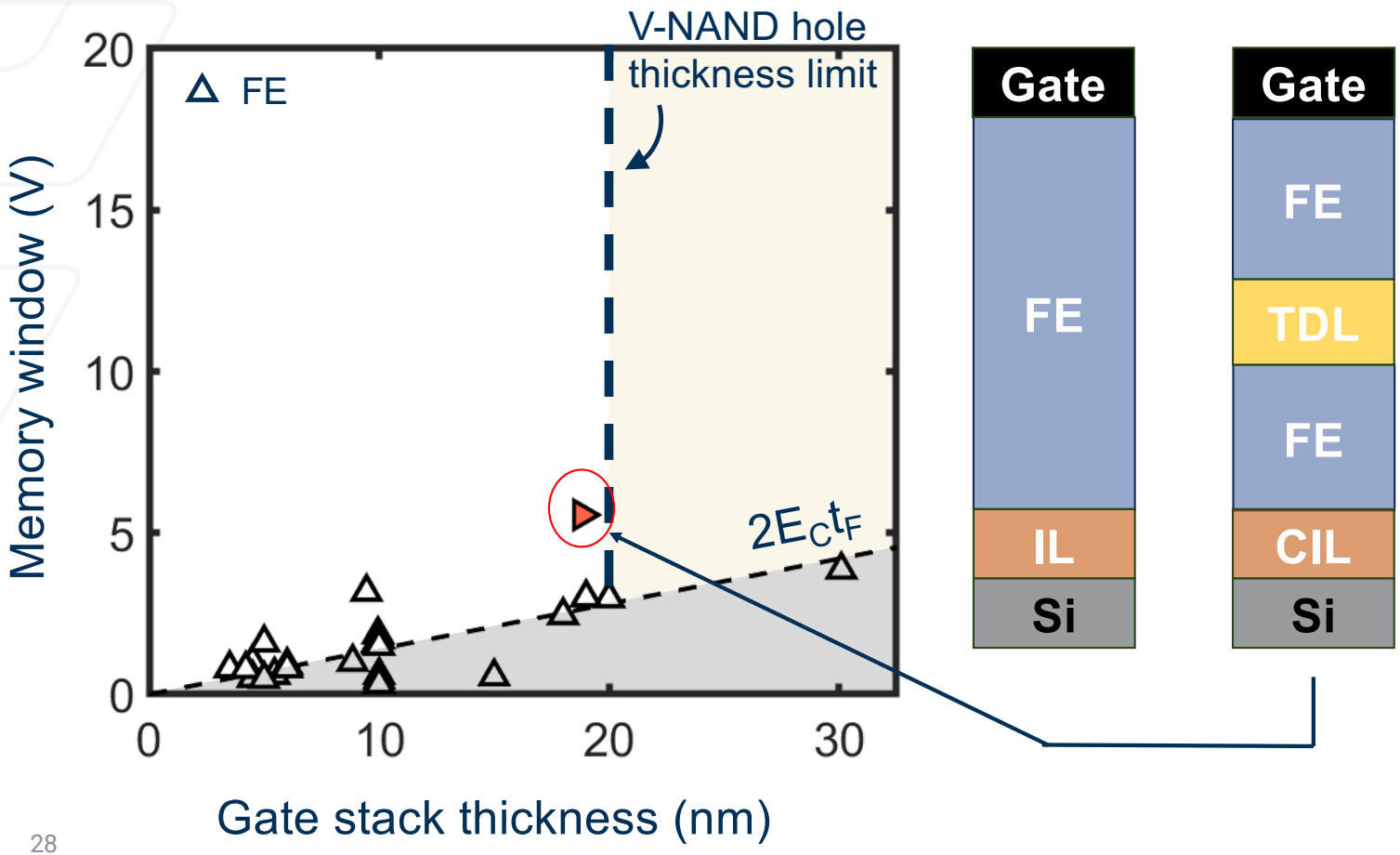




Introducing 1 nm Al_2O_3 intermediate layer dramatically memory window to 5.3 V.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Memory window of FEFETs is limited by V_C



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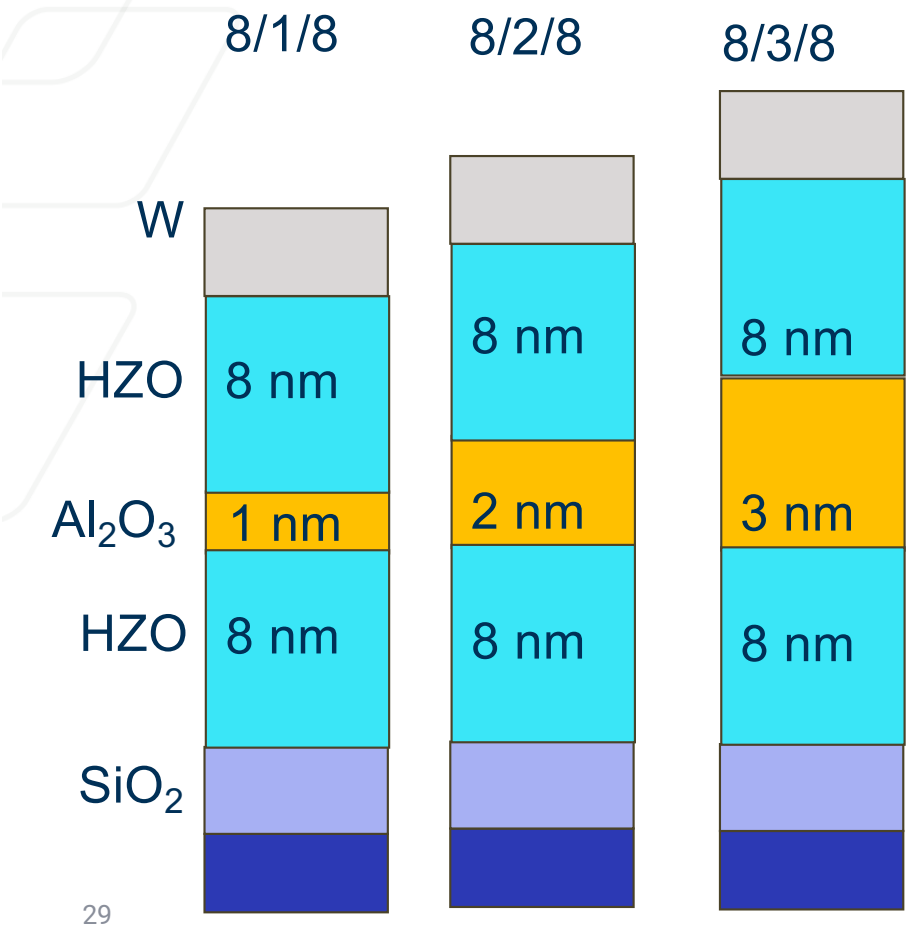
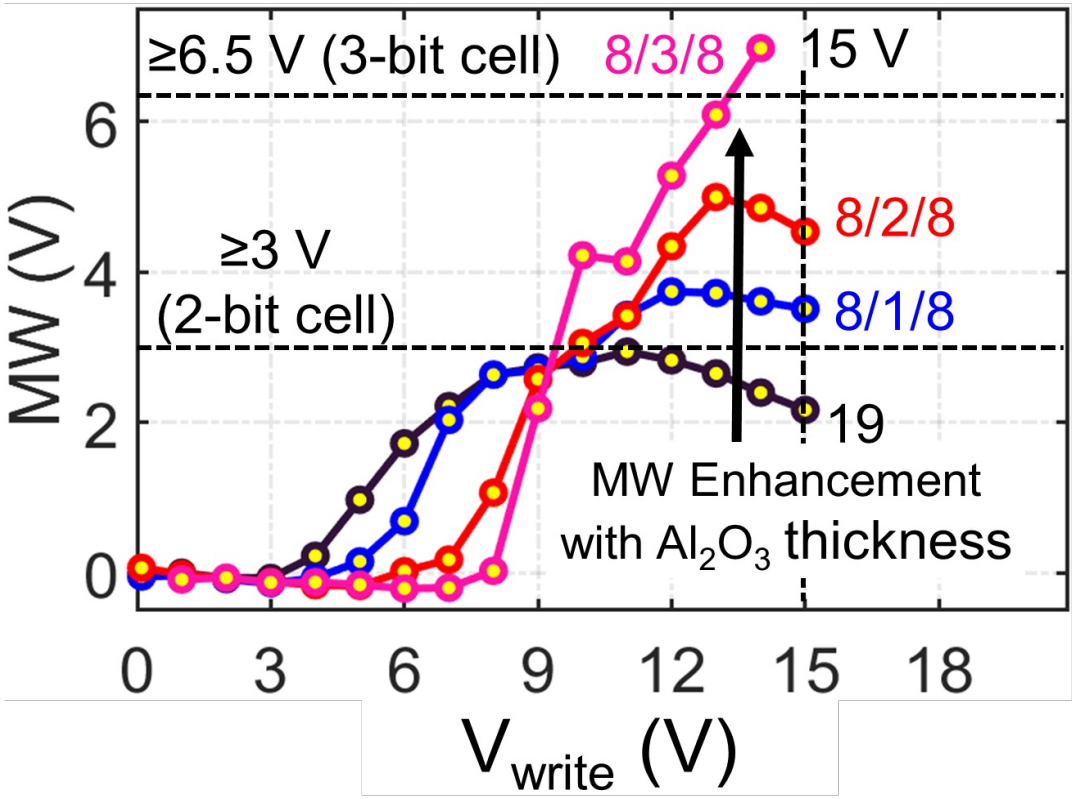
Increasing the MW by dielectric insertion

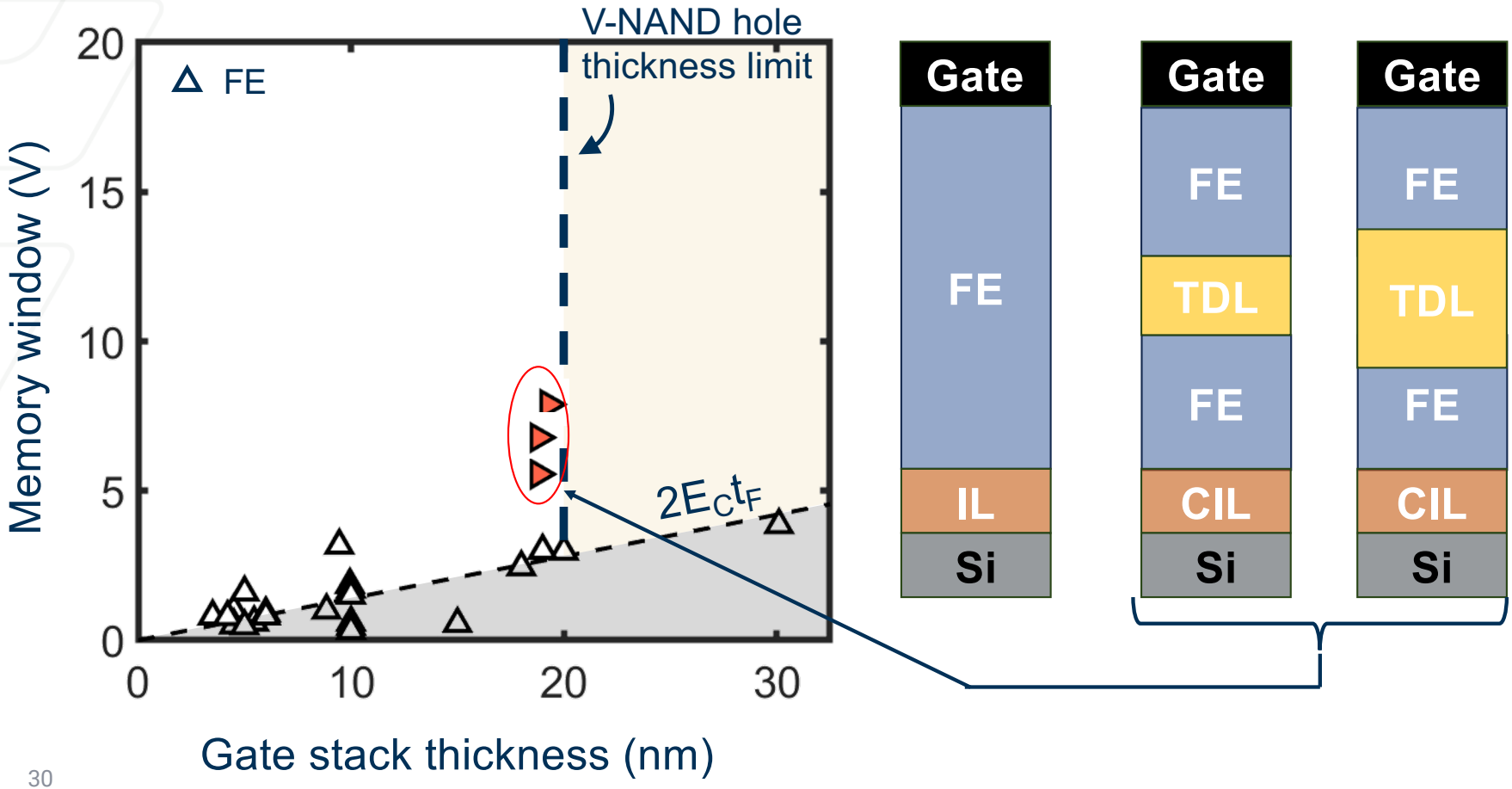




FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

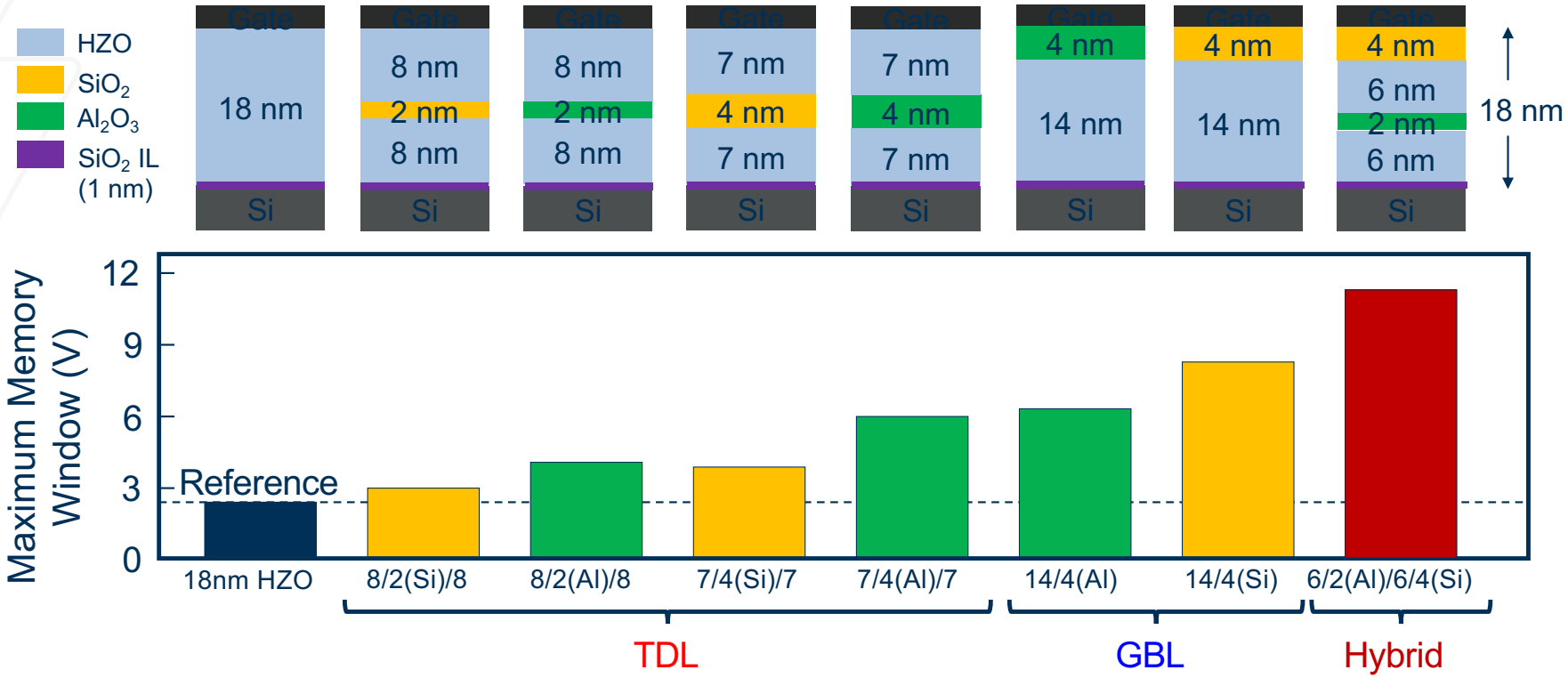
Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion



Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Position and choice of the dielectric



- GBL stacks have higher MW than TDL stacks for similar thickness and material.
- SiO_2 in GBL and Al_2O_3 in TDL gives higher MW for similar dielectric thickness

Fernandes, Khan *et al*. *Material choices for tunnel dielectric layer and gate blocking layer for ferroelectric NAND applications*. IEEE Electron Device Letter 45, 1776 - 1779 (2024). https://doi.org/10.1109/LED.2024.3437239

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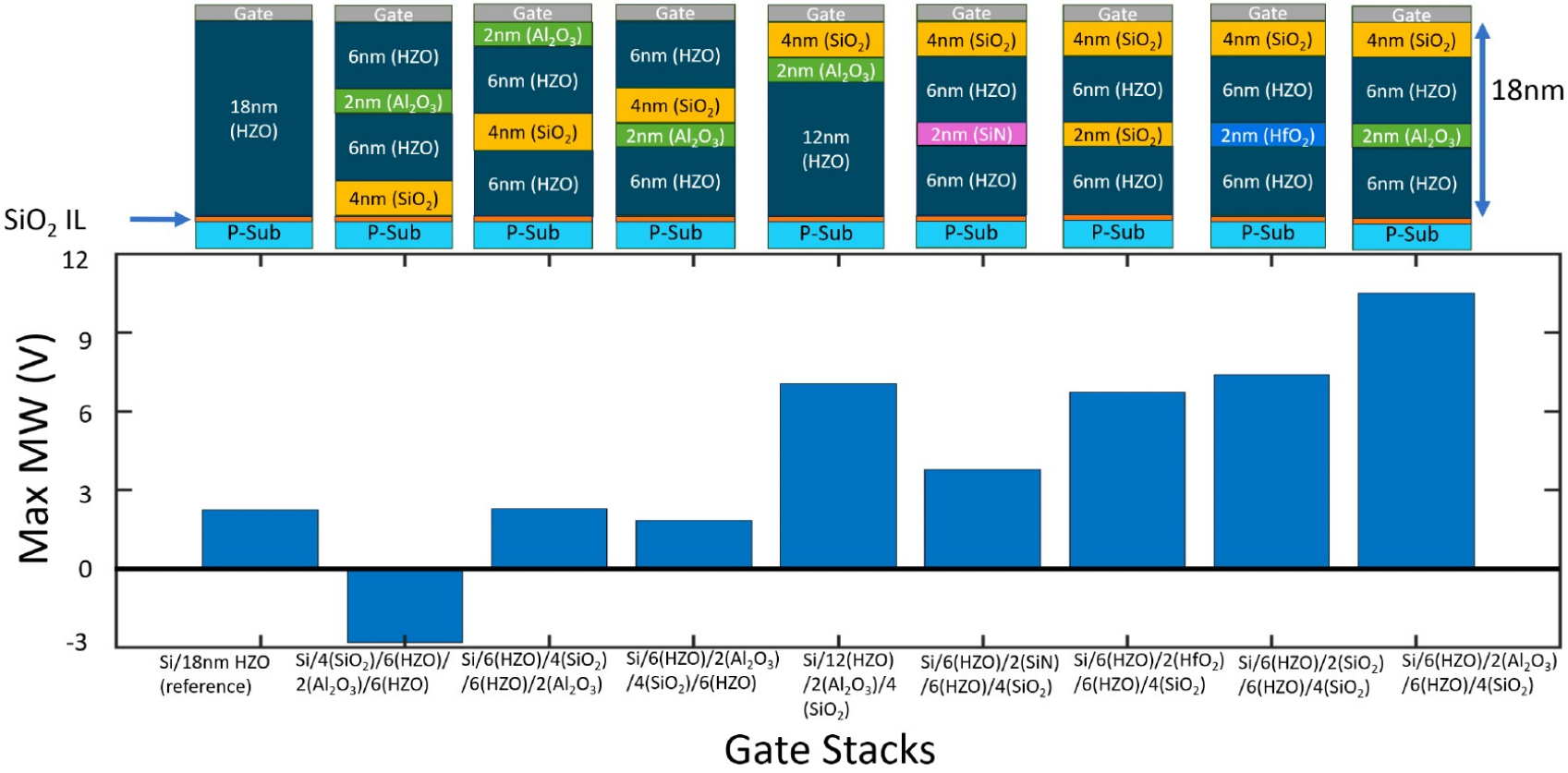
Position and choice of the dielectric



Fernandes, Khan et al. *Optimizing Memory Window for Ferroelectric Nand Applications: An Experimental Study on Dielectric Material Selection and Layer Positioning*. IEEE Transactions on Electron Devices 72, 234 - 239 (2024). https://doi.org/10.1109/TED.2024.3504475

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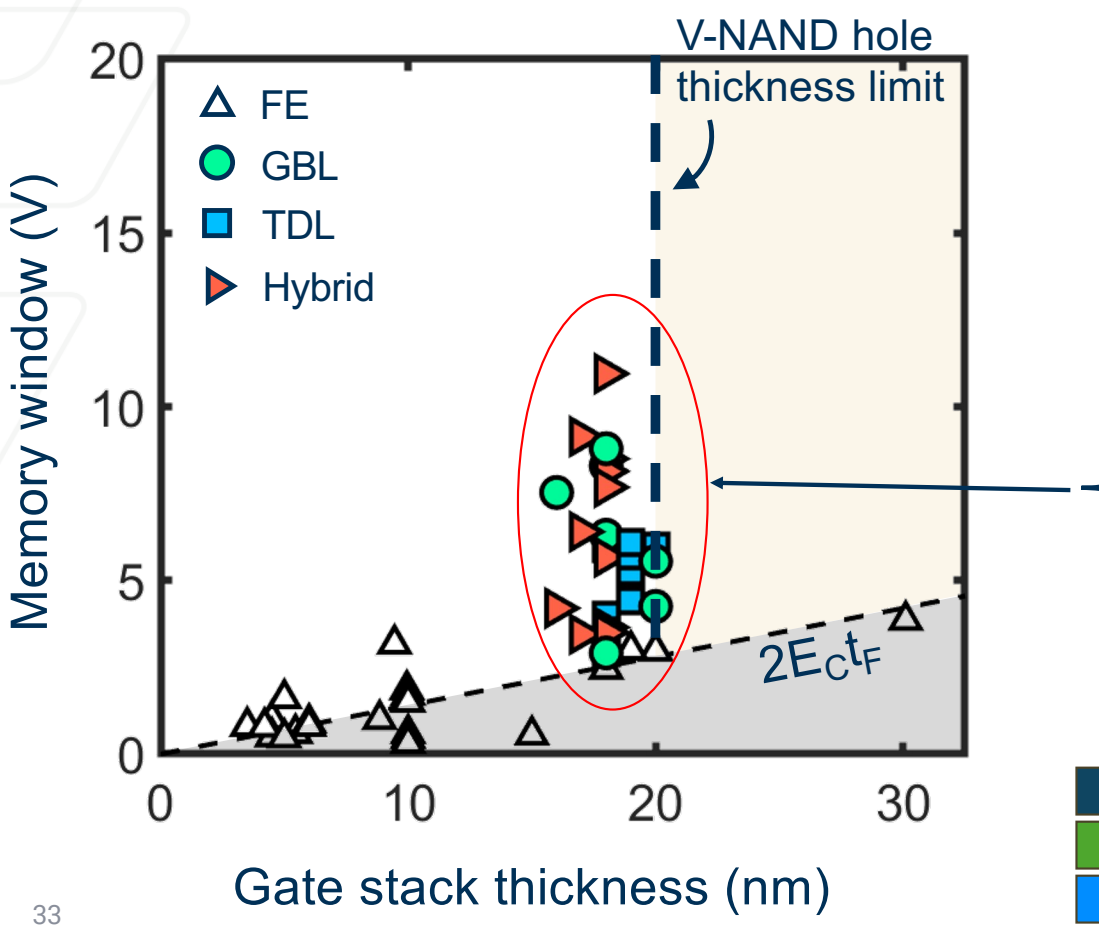
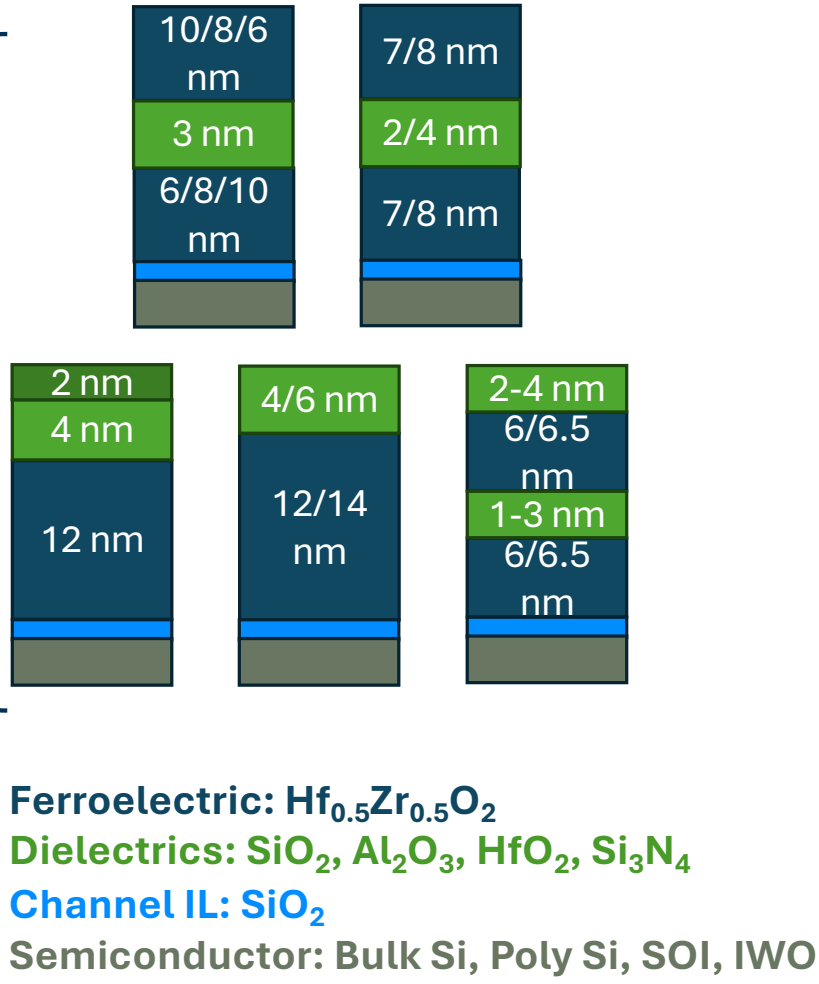
Increasing the MW by dielectric insertion

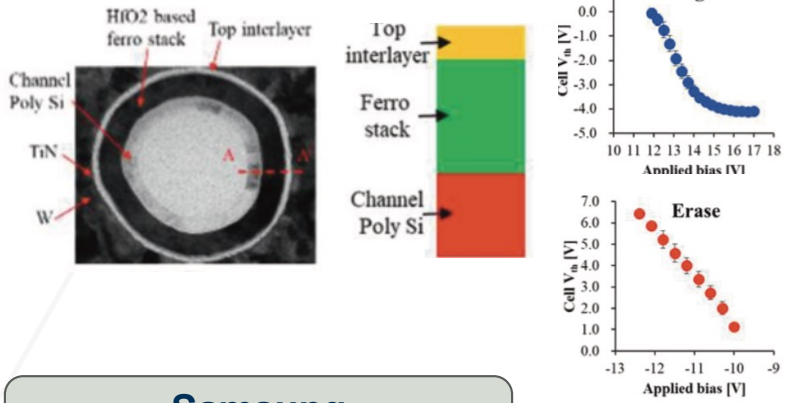




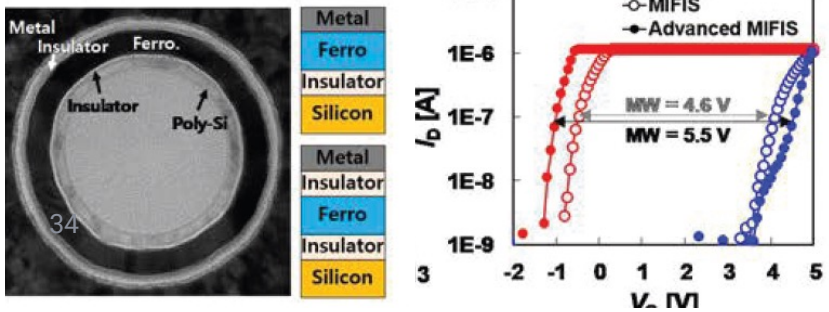
Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$
Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4
Channel IL: SiO_2
Semiconductor: Bulk Si, Poly Si, SOI, IWO

Increasing the MW by dielectric insertion

SK Hynix
Yoon et al. VLSI 2023



Samsung
Lim et al. IEDM 2023



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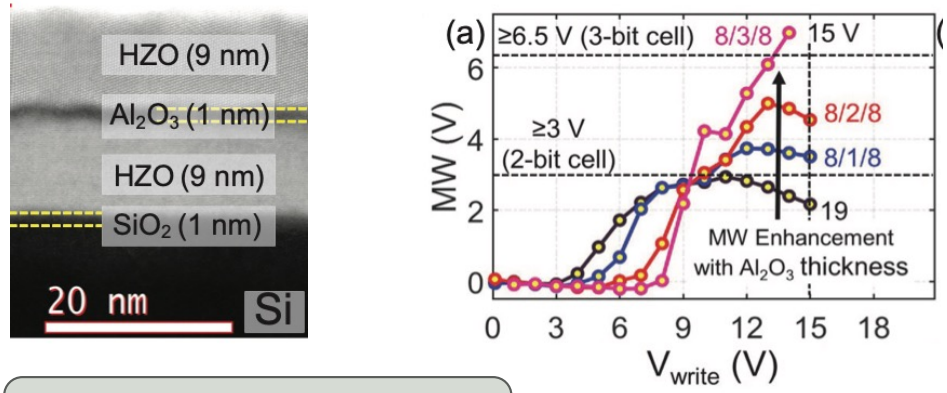
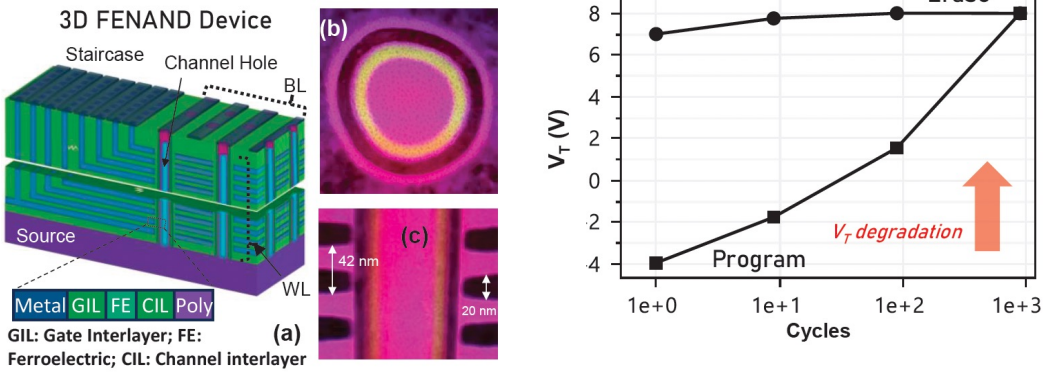
Das et al. IEDM 2023



Micron
Sharma et al. VLSI 2025



Increasing the MW by dielectric insertion

Ferroelectrics:

35 HZO

HAO

Dielectrics:

SiO_2 Si_3N_4 TiO_2

Al_2O_3 HfO_2

Channel IL:

SiO_2 IL (1 nm)

Al_2O_3/AlON IL (1 nm)

Semiconductor:

Si SOI

AOS Poly-Si

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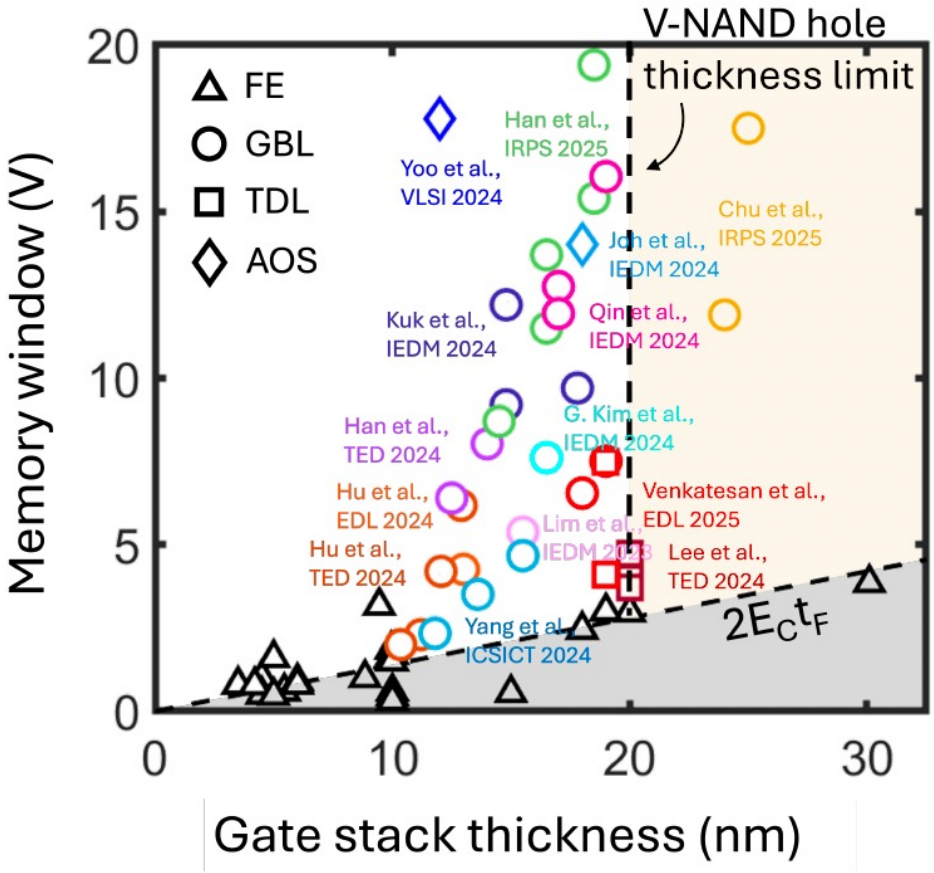
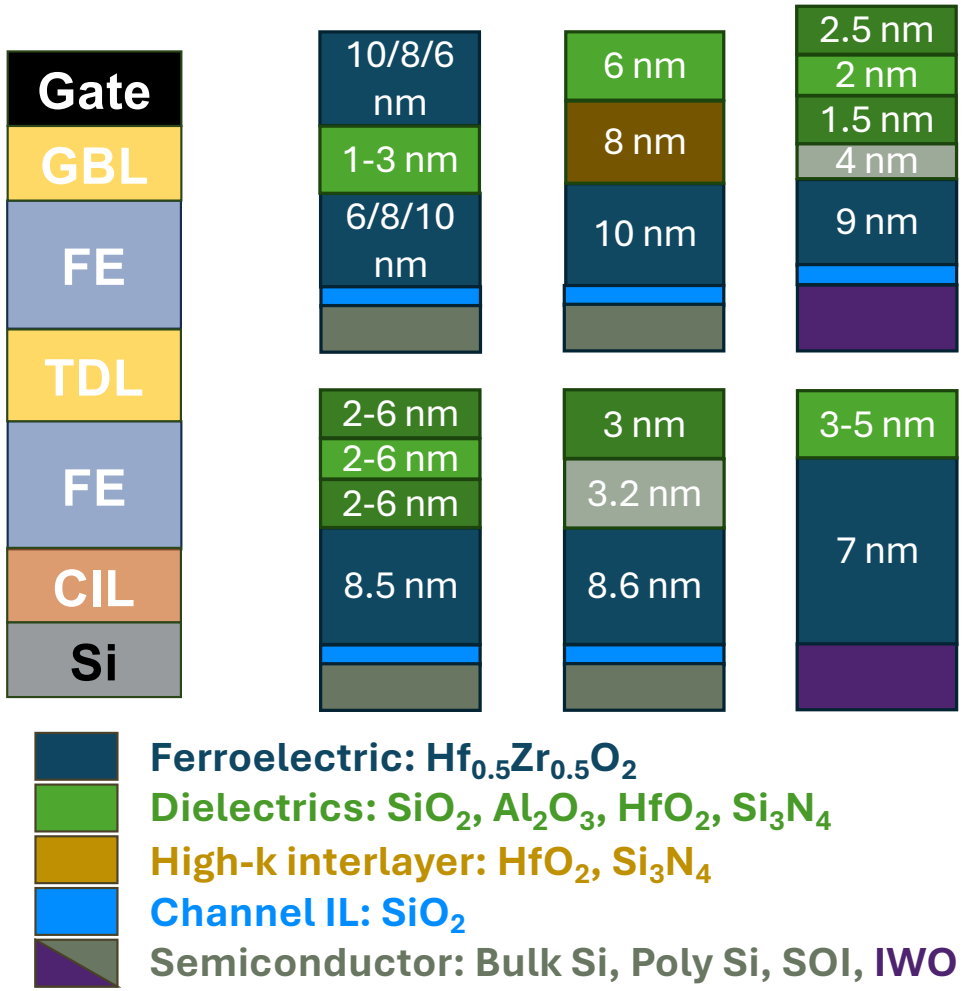
Increasing the MW by dielectric insertion





Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$

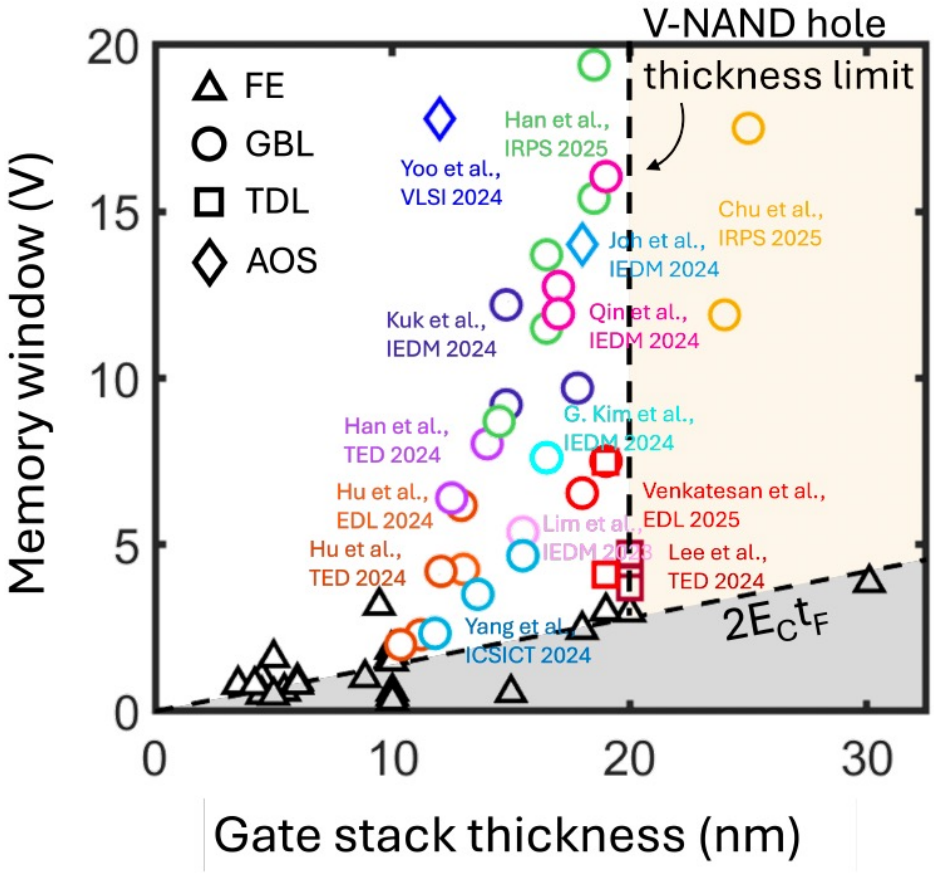
Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4

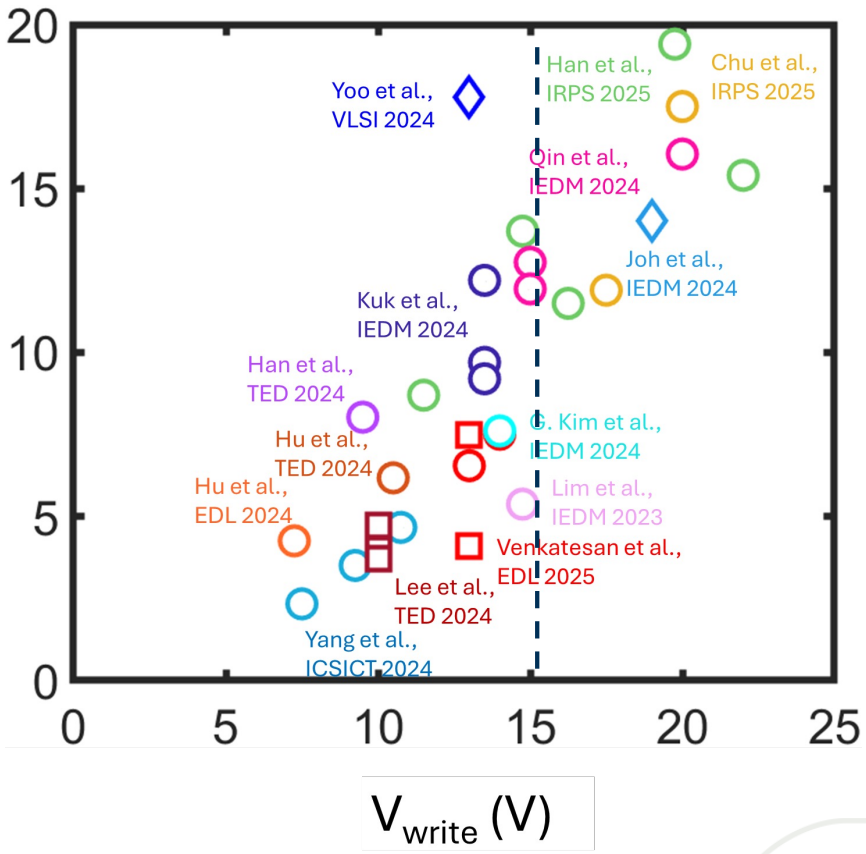
High-k interlayer: HfO_2, Si_3N_4

Channel IL: SiO_2

Semiconductor: Bulk Si, Poly Si, SOI, IWO

Increasing the MW by dielectric insertion





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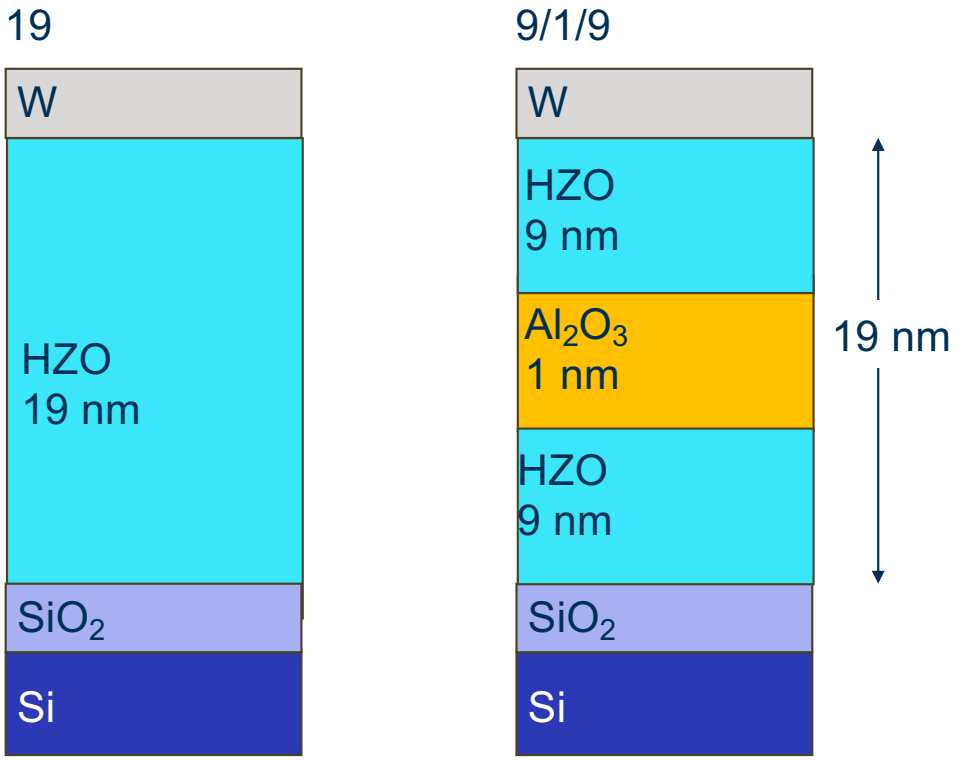
Where is the MW enhancement coming from?



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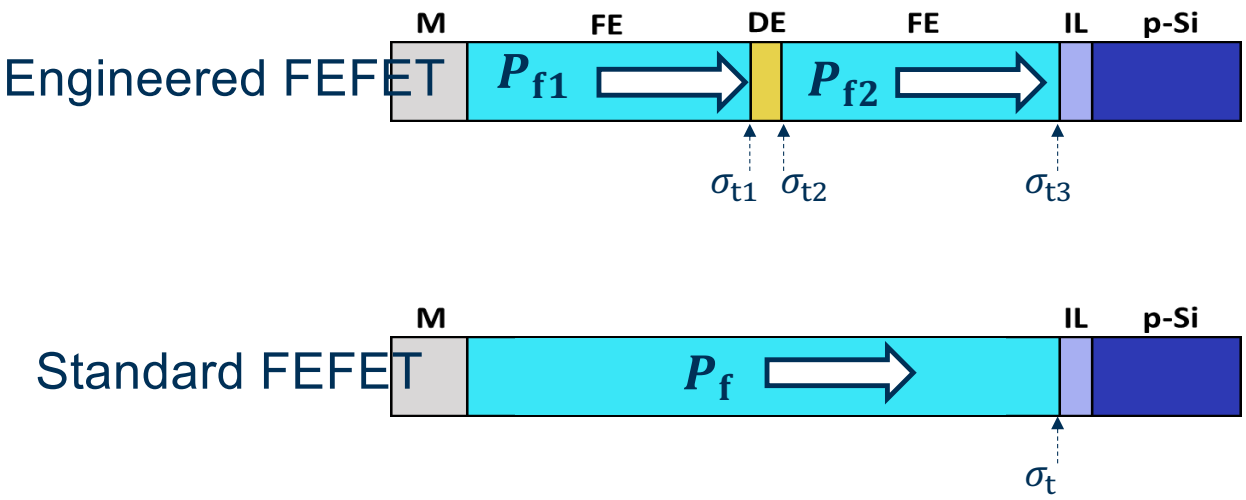
Where is the MW enhancement coming from?



Trapped charges are the key differentiator.

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Modeling framework

1. Ferroelectric switching kinetics

Preisach model was adopted to describe the steady-state characteristics of the ferroelectric polarization.

The saturated polarization hysteresis loop is defined as

$$P^{+}_{\mathrm{sat,i}}(E_\mathrm{i}) = P_{\mathrm{s,i}} \tanh[(E_\mathrm{i} - E_{\mathrm{c,i}})/2\delta_\mathrm{i}] \quad \text{If } dE_\mathrm{i}/dt > 0$$

$$P^{-}_{\mathrm{sat,i}}(E_\mathrm{i}) = -P^{+}_{\mathrm{sat,i}}(-E_\mathrm{i}) \quad \text{If } dE_\mathrm{i}/dt < 0$$

where

$$\delta_\mathrm{i} = E_{\mathrm{c,i}} \left[\ln\left(\frac{1 + P_{\mathrm{r,i}}/P_{\mathrm{s,i}}}{1 - P_{\mathrm{r,i}}/P_{\mathrm{s,i}}} \right) \right]^{-1} \quad \text{For } i = 1,2$$

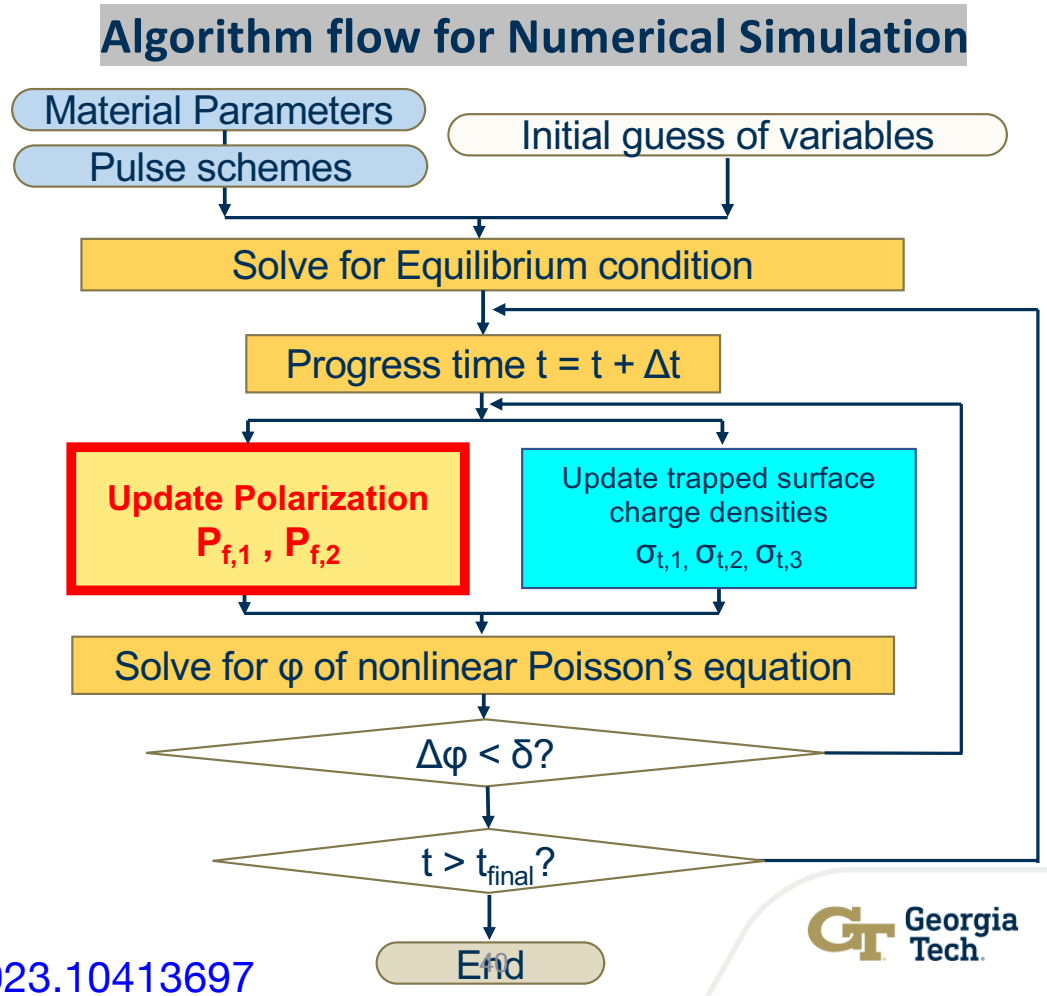
The derivative of the polarization is given by

$$\frac{dP_{\mathrm{f,i}}}{dE_\mathrm{i}} = \Gamma_\mathrm{i} \frac{dP_{\mathrm{sat,i}}}{dE_\mathrm{i}} \quad \text{For } i = 1,2$$

where

$$\Gamma_\mathrm{i} = 1 - \tanh\left[\left(\frac{P_{\mathrm{f,i}} - P_{\mathrm{sat,i}}}{\xi_\mathrm{i} P_{\mathrm{s,i}} - P_{\mathrm{f,i}}} \right)^{1/2} \right]$$

$\xi_\mathrm{i} = +1$ when $dE_\mathrm{i}/dt > 0$ and $\xi = -1$ when $dE_\mathrm{i}/dt < 0$



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Modeling framework

2. Rate equations for trapping and de-trapping

Assuming single level traps, define

$N_{t,1}$ / $P_{t,1}$: Acceptor/Donor-like trap density at HZO/Al_2O_3

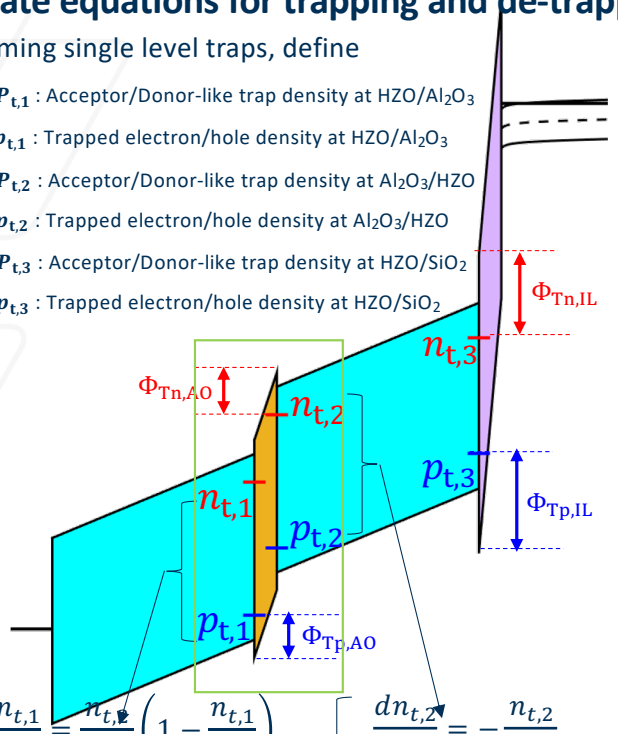
$n_{t,1}$ / $p_{t,1}$: Trapped electron/hole density at HZO/Al_2O_3

$N_{t,2}$ / $P_{t,2}$: Acceptor/Donor-like trap density at Al_2O_3/HZO

$n_{t,2}$ / $p_{t,2}$: Trapped electron/hole density at Al_2O_3/HZO

$N_{t,3}$ / $P_{t,3}$: Acceptor/Donor-like trap density at HZO/SiO_2

$n_{t,3}$ / $p_{t,3}$: Trapped electron/hole density at HZO/SiO_2



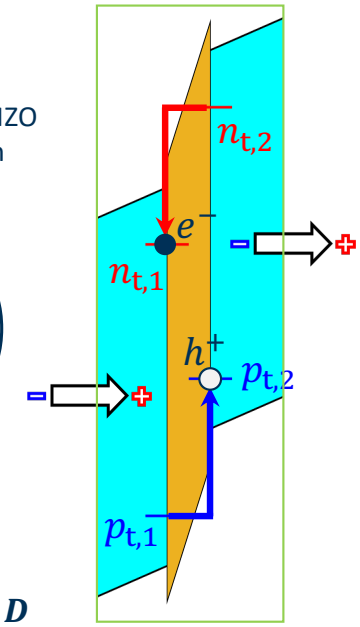
$$\frac{dn_{t,1}}{dt} = \frac{n_{t,2}}{\tau_{cn1}}\left(1 - \frac{n_{t,1}}{N_{t,1}}\right) \qquad \frac{dn_{t,2}}{dt} = -\frac{n_{t,2}}{\tau_{en2}}$$

$$\frac{dp_{t,1}}{dt} = -\frac{p_{t,1}}{\tau_{ep1}} \qquad \frac{dp_{t,2}}{dt} = \frac{p_{t,1}}{\tau_{cp2}}\left(1 - \frac{p_{t,2}}{P_{t,2}}\right)$$

The net trapped charges $\sigma_{t,i}$ are $\sigma_{t,i} = q(p_{t,i} - n_{t,i})$ For $i = 1,2,3$

The emission mechanism of the trapped charges at Al_2O_3/HZO (HZO/Al_2O_3) interfaces are assumed to be Fowler-Nordheim (FN) tunneling → **Al_2O_3 as "Tunnel Dielectric Layer"**

$$\tau_{en(p),i=2(1)} = \tau_{cn(p),i=1(2)} = \tau_0 \exp\left(-\frac{4\sqrt{2m_{AO}\Phi^3_{Tn(p),AO}}}{3q\hbar E_{AO}}\right)$$



3. Nonlinear Poisson-Boltzmann equation

For gate oxides, $\frac{\partial D}{\partial x} = 0$

With boundary conditions of the displacement field $\boldsymbol{D}$ continuity at the interfaces i with given $\boldsymbol{P_{f,i}}$ and $\boldsymbol{\sigma_{t,i}}$

For semiconductors,

$$\frac{\partial^2 \varphi}{\partial x^2} = -\frac{q}{\epsilon_s}\left[p_{po}(\exp(-\beta\varphi) - 1) - n_{po}(\exp(\beta\varphi) - 1)\right]$$

Thus, Flat band voltage is given by

$$V_{FB} = \phi_{MS} - \frac{\sigma_{it}(\psi_s)}{C_{tot}} - \frac{P_{f,1} + \sigma_{t,1} + \sigma_{t,2} + \sigma_{t,3}}{C_{f,1}} - \frac{\sigma_{t,2} + \sigma_{t,3}}{C_d} - \frac{P_{f,2} + \sigma_{t,3}}{C_{f,2}}$$

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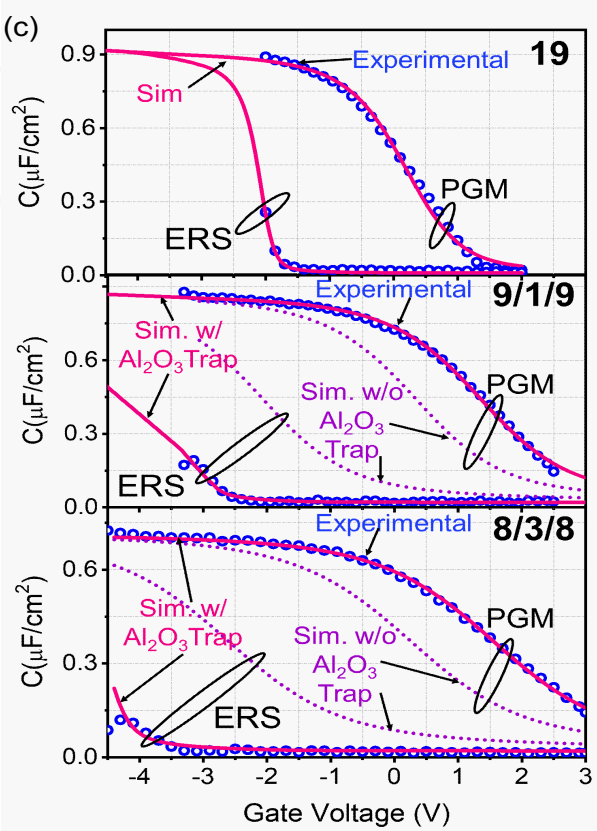
Experimental Calibration



Charge trapping in Al_2O_3 required to match the MW for 8/3/8 and 9/1/9.

Symbols	Description	19	9/1/9	8/3/8
ϵ_i	Dielectric constant of SiO_2	3.9	3.9	3.9
ϵ_d	Dielectric constant of Al_2O_3	-	8.9	8.9
ϵ_f	Dielectric constant of HZO	28	27	26
P_s	Saturated polarization	20 μC/cm²	15 μC/cm²	15 μC/cm²
P_r	Remanent polarization	17 μC/cm²	13 μC/cm²	13 μC/cm²
E_c	Coercive field	1.2 MV/cm	1.2 MV/cm	1.2 MV/cm
m_{AO}	Tunneling mass of Al_2O_3	-	$0.5\ m_0$	$0.5\ m_0$
m_{IL}	Tunneling mass of SiO_2	$0.5\ m_0$	$0.5\ m_0$	$0.5\ m_0$
$\Phi_{Bn,IL}$	SiO_2 electron de-trapping barriers	2.35 eV	2.35 eV	2.35 eV
$\Phi_{Bp,IL}$	SiO_2 hole de-trapping barriers	2.85 eV	2.85 eV	2.85 eV
$\Phi_{Tn,AO}$	Al_2O_3 electron tunneling barriers	-	1.20 eV	1.20 eV
$\Phi_{Tp,AO}$	Al_2O_3 hole tunneling barriers	-	1.40 eV	1.40 eV
N_{t1}, P_{t1}	Electron, hole Trap density at interface 1	-	$6.2\times10^{13}cm^{-2}$	$6.2\times10^{13}cm^{-2}$
N_{t2}, P_{t2}	Electron, hole Trap density at interface 2	-	$6.2\times10^{13}cm^{-2}$	$6.2\times10^{13}cm^{-2}$
N_{t3}, P_{t3}	Electron, hole Trap density at interface 3	$1.2\times10^{14}cm^{-2}$	$1.2\times10^{14}cm^{-2}$	$1.2\times10^{14}cm^{-2}$
D_{it}	Density of states at Si/SiO_2	$1.2\times10^{14}cm^{-2}eV^{-1}$	$1.4\times10^{14}cm^{-2}eV^{-1}$	$1.4\times10^{14}cm^{-2}eV^{-1}$
	Intrinsic time constant for tunneling	1 ns	1 ns	1 ns

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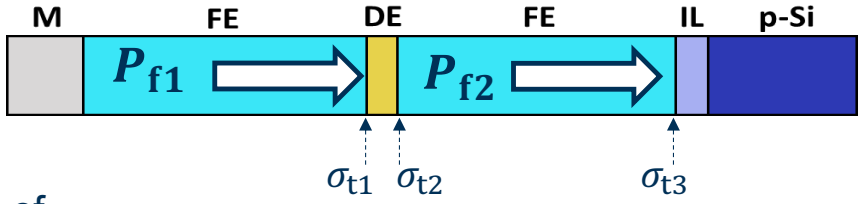
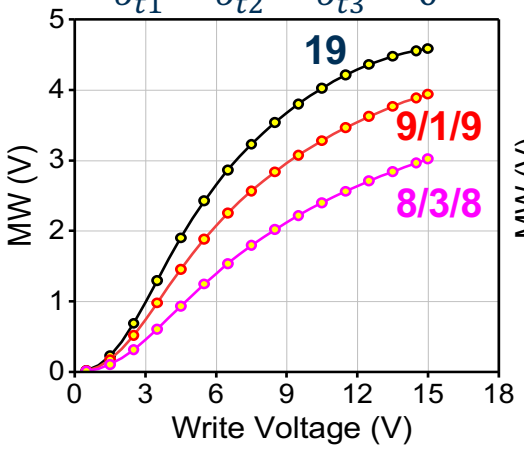
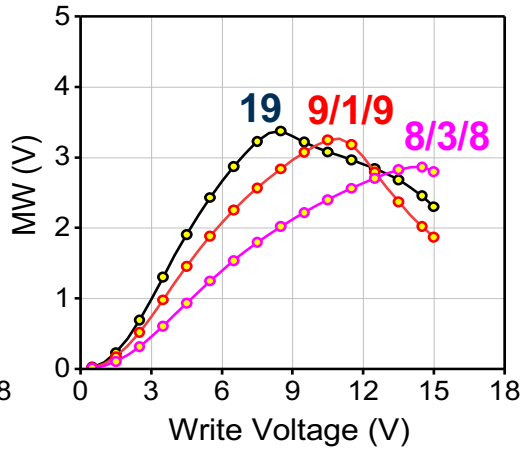
Decoupling the impacts of different trapping mechanisms



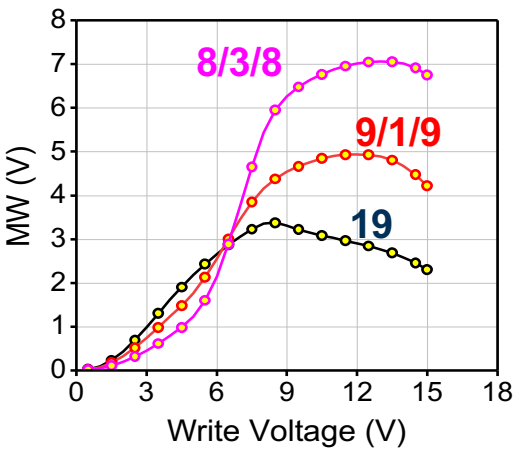
Absence of screening trap charges
$\sigma_{t1} = \sigma_{t2} = \sigma_{t3} = 0$



HZO/SiO_2 Traps only
$\sigma_{t1} = \sigma_{t2} = 0;\ \sigma_{t3} \neq 0$



Al_2O_3/HZO + HZO/SiO_2 Traps
$\sigma_{t1} \neq 0;\ \sigma_{t2} \neq 0;\ \sigma_{t3} \neq 0$



Trap effects are responsible for the observed MW trend
(MW: 8/3/8 >9/1/9>19)

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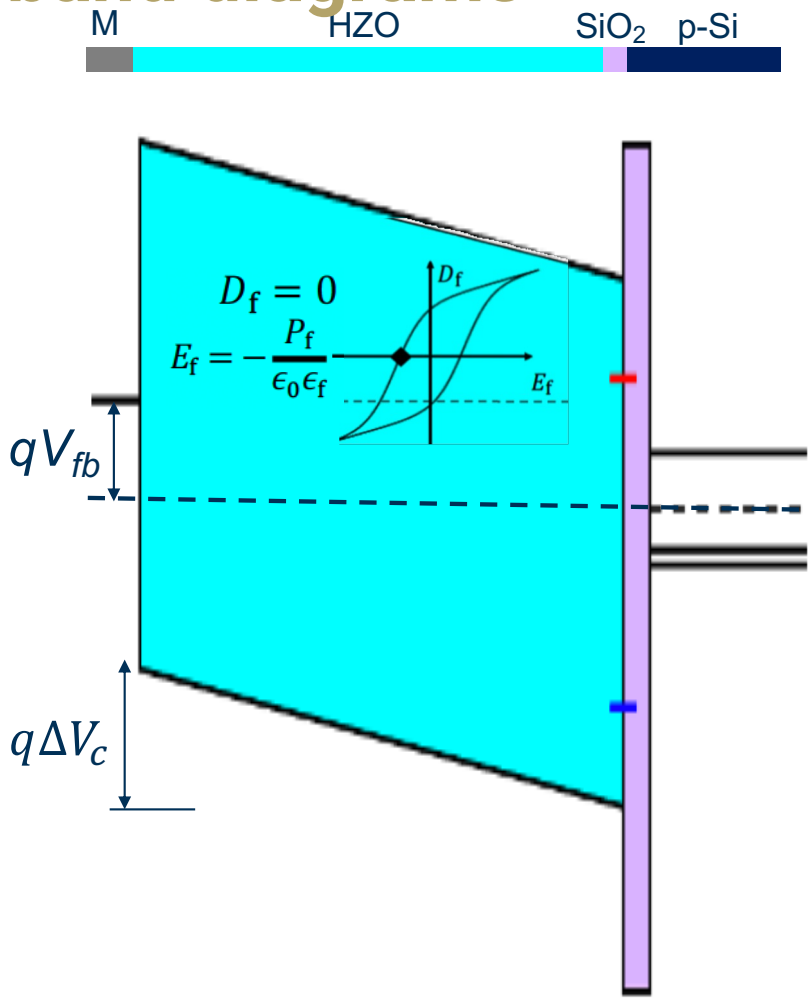
MW enhancement mechanism with band diagrams



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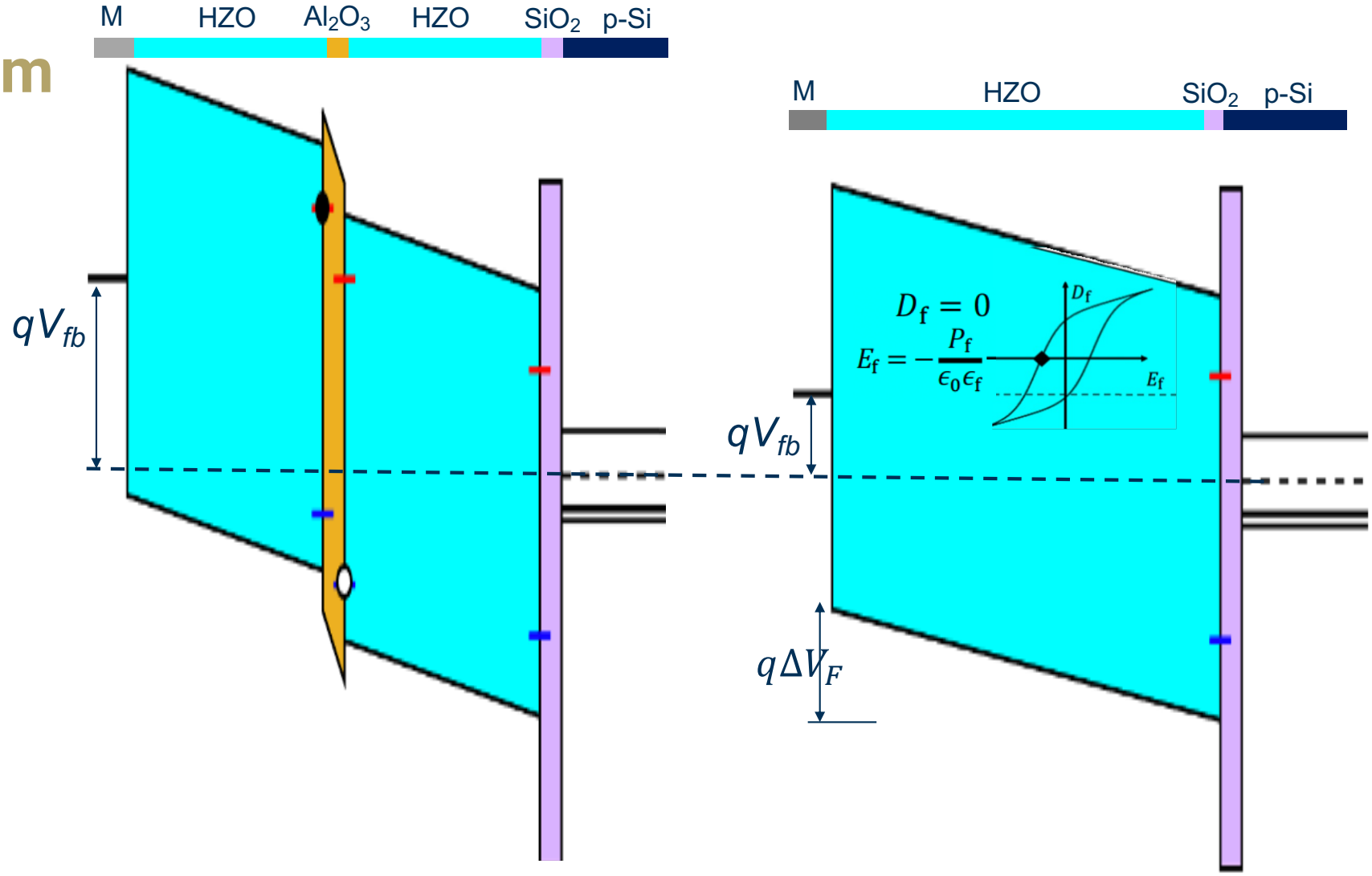
MW mechanism



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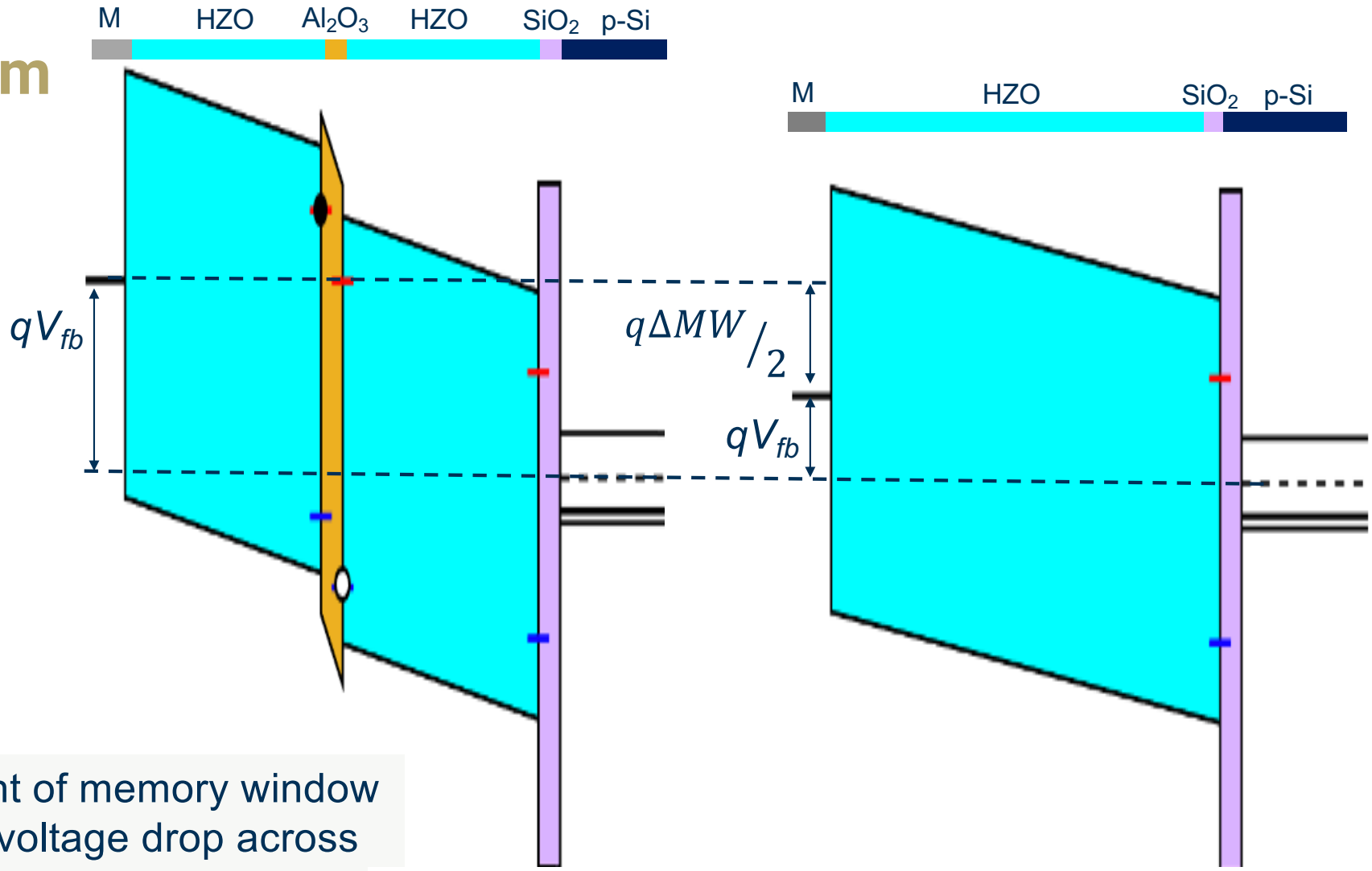
MW mechanism



Enhancement of memory window ΔMW ≈2 x voltage drop across Al_2O_3 at flatband

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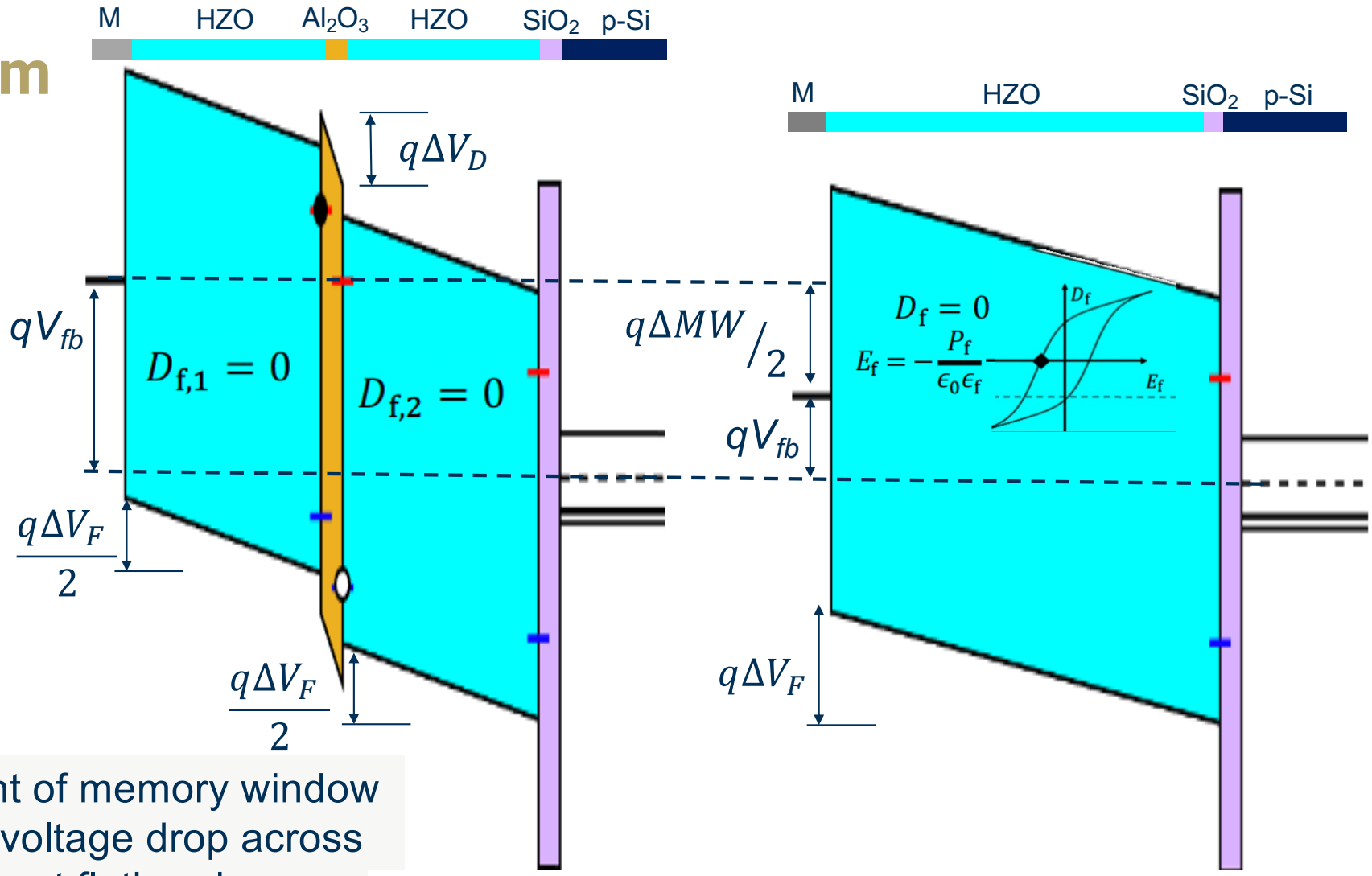
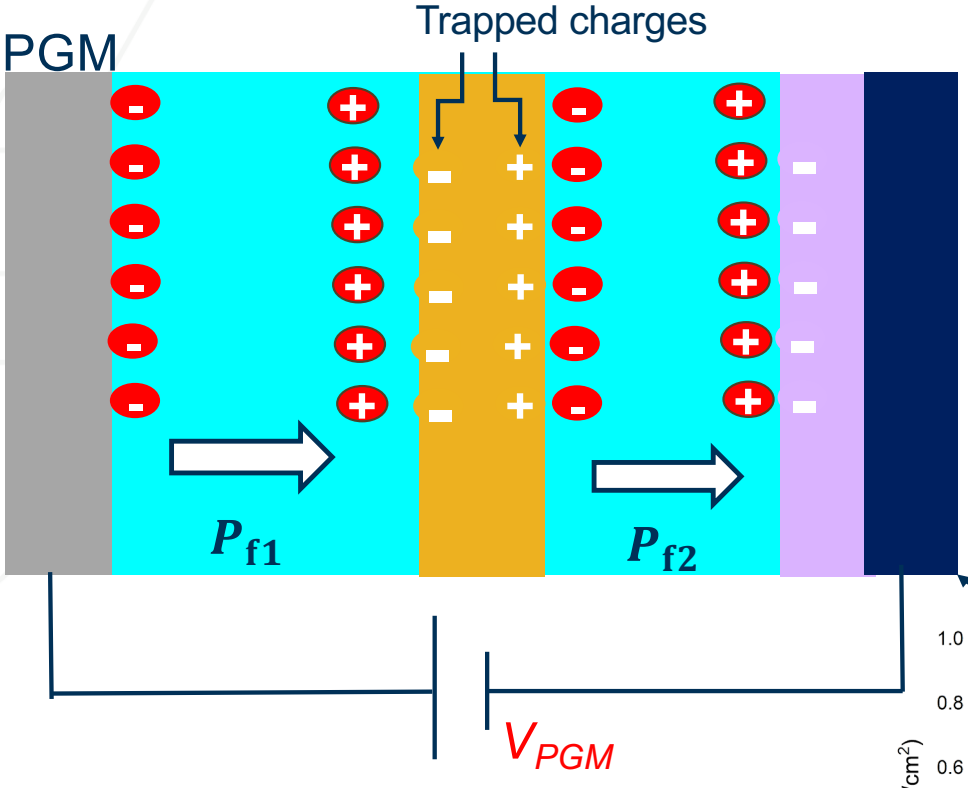
MW mechanism

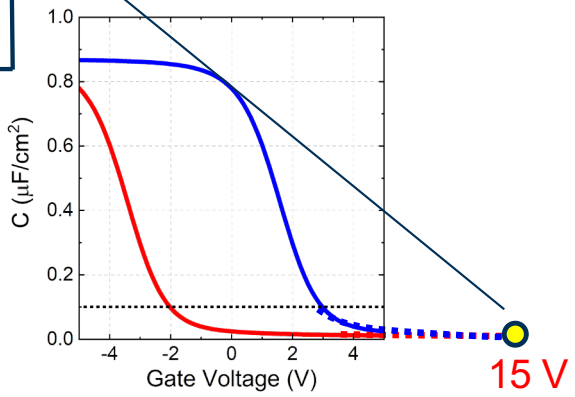


Enhancement of memory window $\Delta MW \approx 2$ x voltage drop across Al_2O_3 at flatband

Das, D., et al. IEDM 2023: [10.1109/IEDM45741.2023.10413697](https://doi.org/10.1109/IEDM45741.2023.10413697)

Where does the built-in electric field come from?





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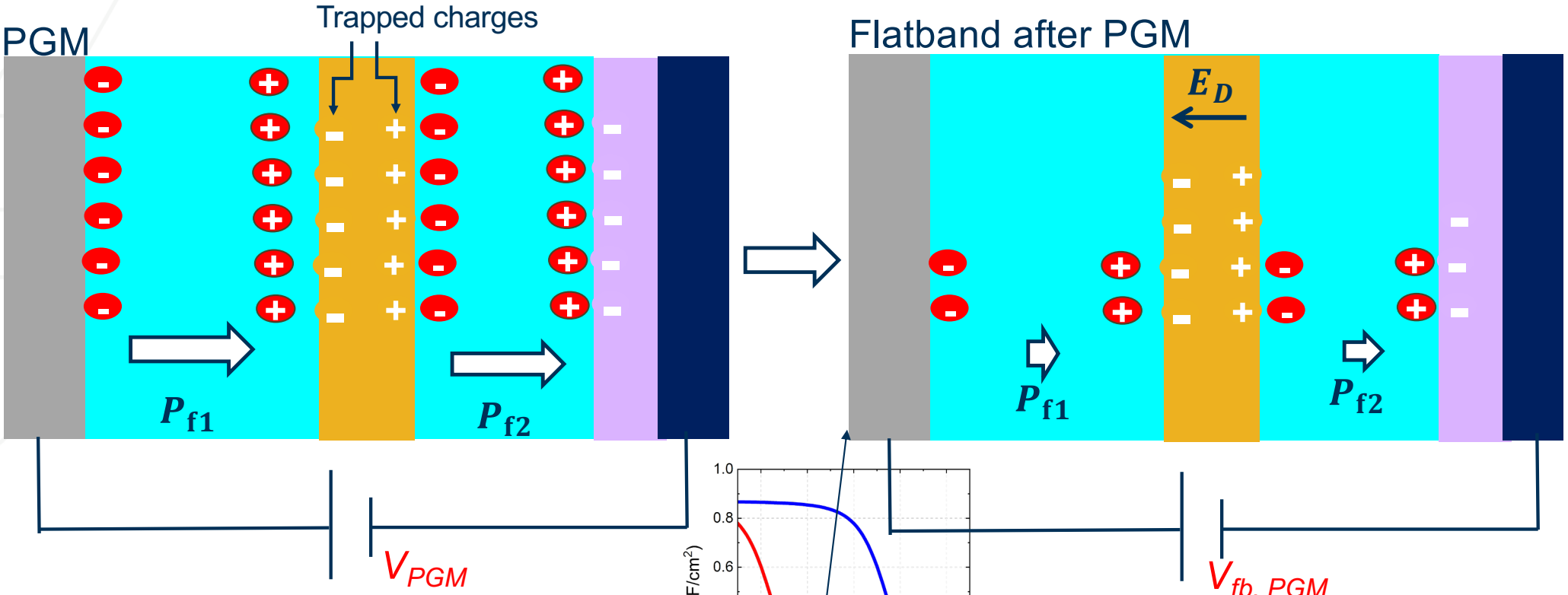
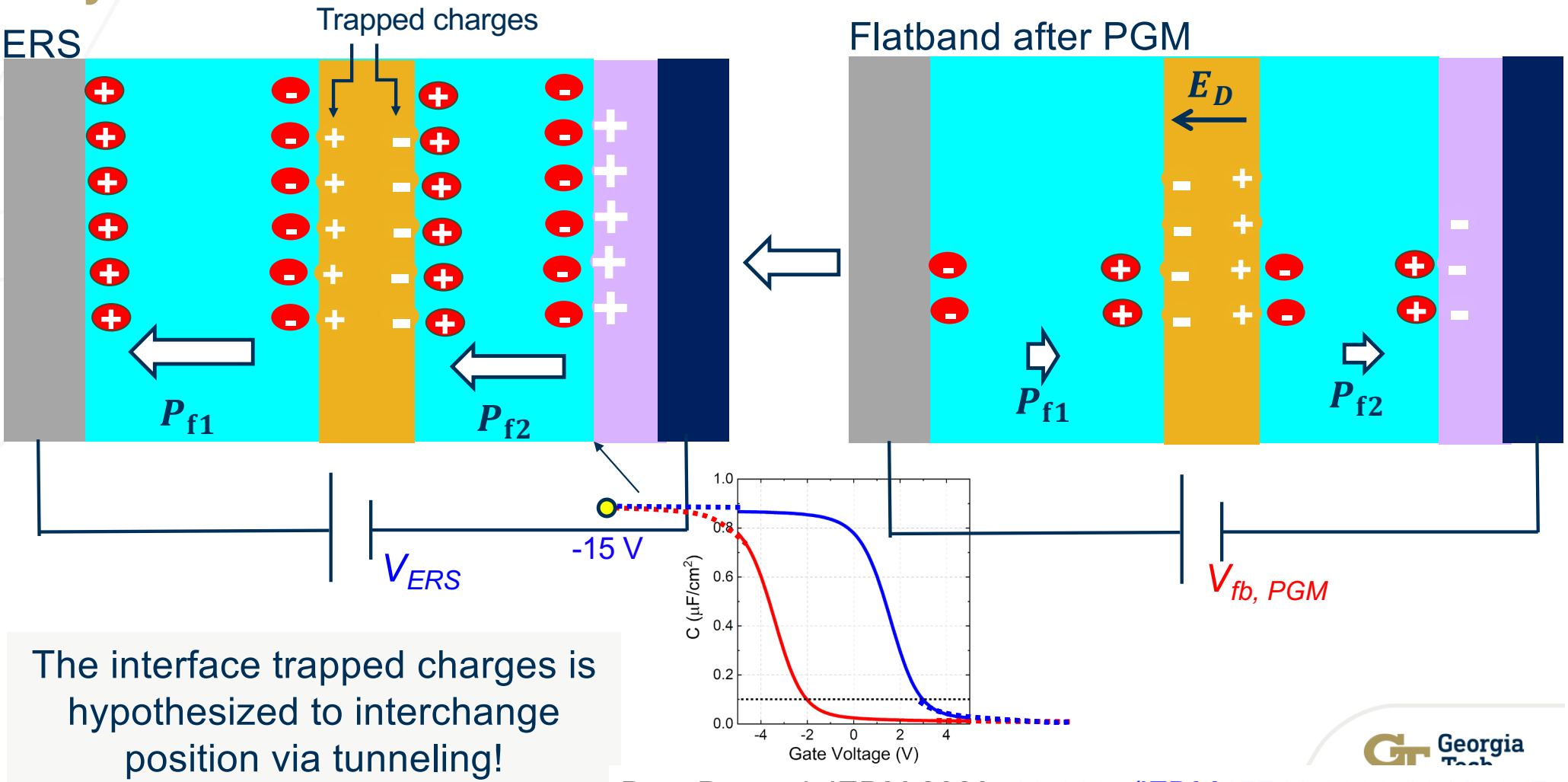
Where does the built-in electric field come from?



Built-in electric field due to defect dipole in the dielectric induced by the ferroelectric polarization leads to the MW enhancement.

Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

Why do we call it a tunnel dielectric?



The interface trapped charges is hypothesized to interchange position via tunneling!

Das, D., et al. IEDM 2023: [10.1109/IEDM45741.2023.10413697](https://doi.org/10.1109/IEDM45741.2023.10413697)

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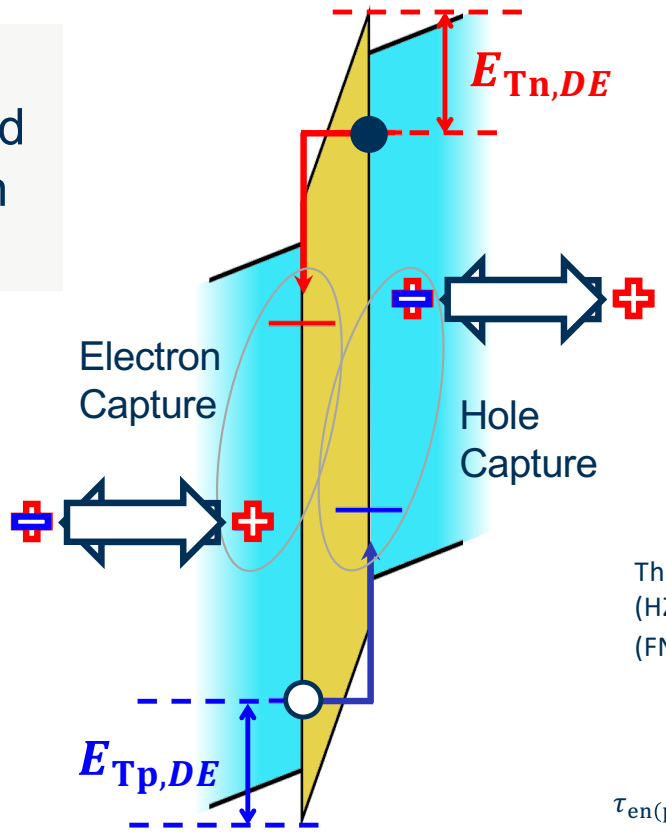

The emission mechanism of the trapped charges at Al_2O_3/HZO (HZO/Al_2O_3) interfaces are assumed to be Fowler-Nordheim (FN) tunneling → **Al_2O_3 as "Tunnel Dielectric Layer"**

$$\tau_{\mathrm{en(p)},i=2(1)} = \tau_{\mathrm{cn(p)},i=1(2)} = \tau_0 \exp\left(-\frac{4\sqrt{2m_{AO}\Phi^3_{\mathrm{Tn(p)},AO}}}{3q\hbar E_{AO}}\right)$$

Georgia Tech

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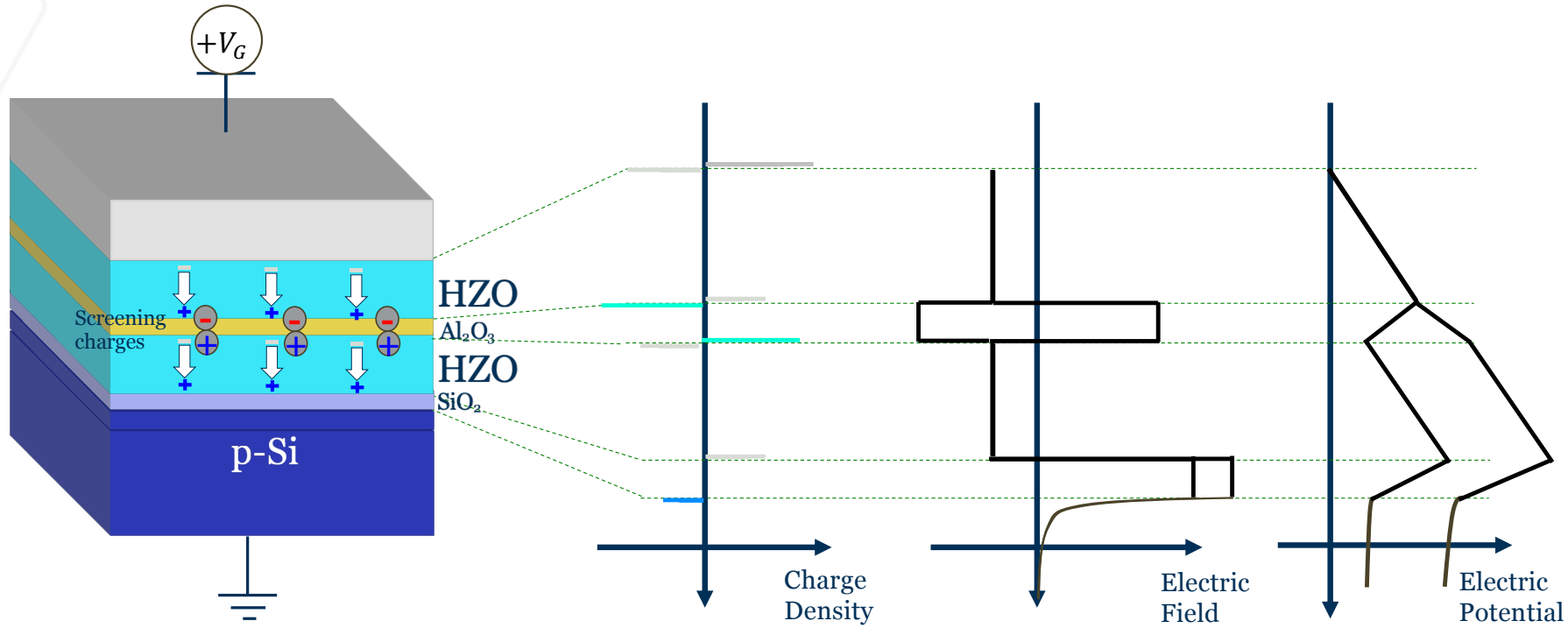
MW enhancement mechanism by screening charges



FE gate stack with TDL ($t_{HZO}/t_{ALO}/t_{HZO}$ =9/1/9 nm)

- The screening charges at interfaces between the inserted ALO layer and FE can help to *increase* the MW by inducing the additional dipoles across the TDL in the same direction as FE polarization.

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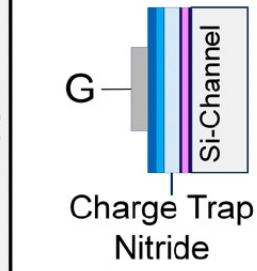
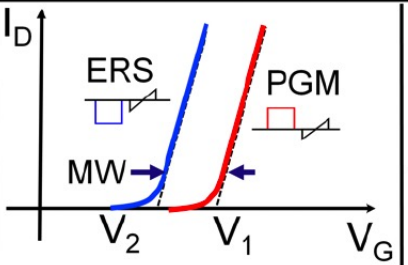
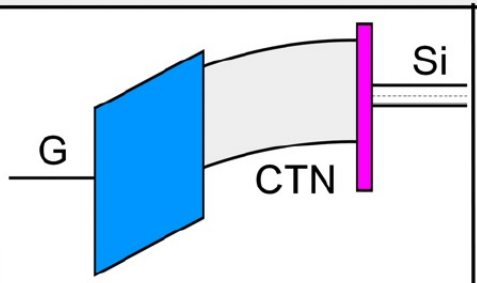
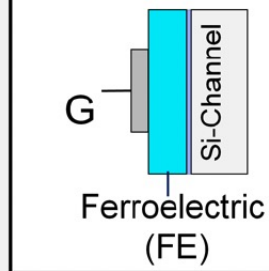
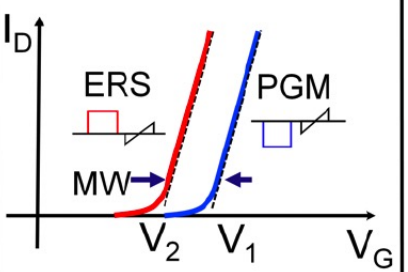
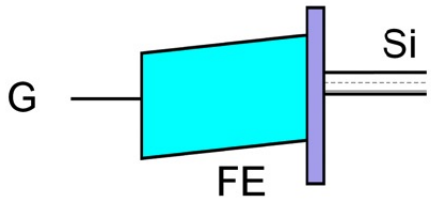
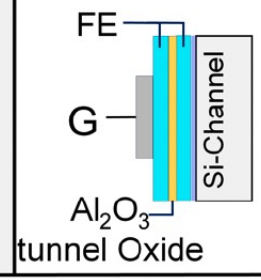
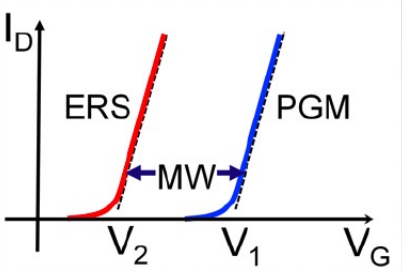
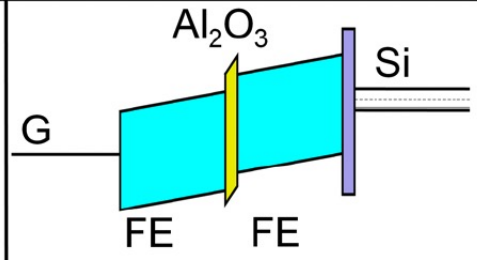
Charge trap flash vs ferroelectric flash

	Structure	Characteristics	Band diagram at FB condition	Attributes
Charge Trap Flash				✓ Large MW × Large Write Voltage Mechanism: Trapping
Conventional FEFET				× Low MW ✓ Low Write Voltage Mechanism: Polarization Switching
Proposed FEFET				✓ Large MW ✓ Moderate Write Voltage Mechanism: Polarization Switching + Trapping + Tunneling

Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

What about reliability of ferroelectric NAND?

Performance

Memory window

Device Reliability

Retention

Disturb

Write Endurance

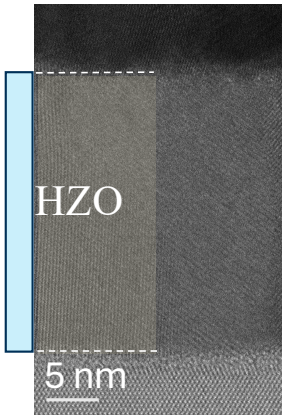
Array-level Reliability

Lateral charge migration

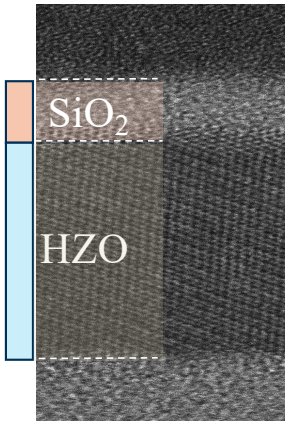
Device-device variation

Ferroelectric NAND gate stacks

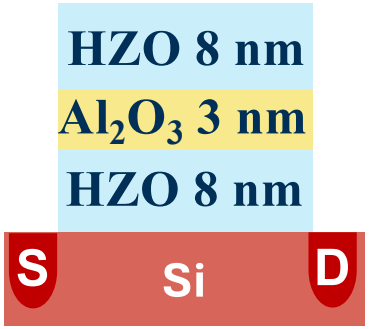
FE (reference)

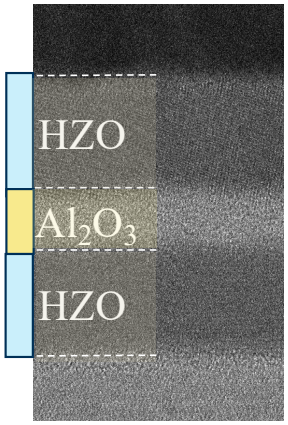


Gate blocking layer (GBL) 14/4(Si)



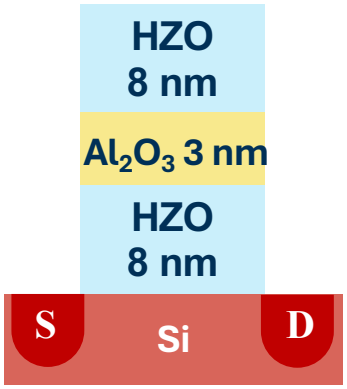
Tunnel dielectric layer (TDL) 8/3(Al)/8

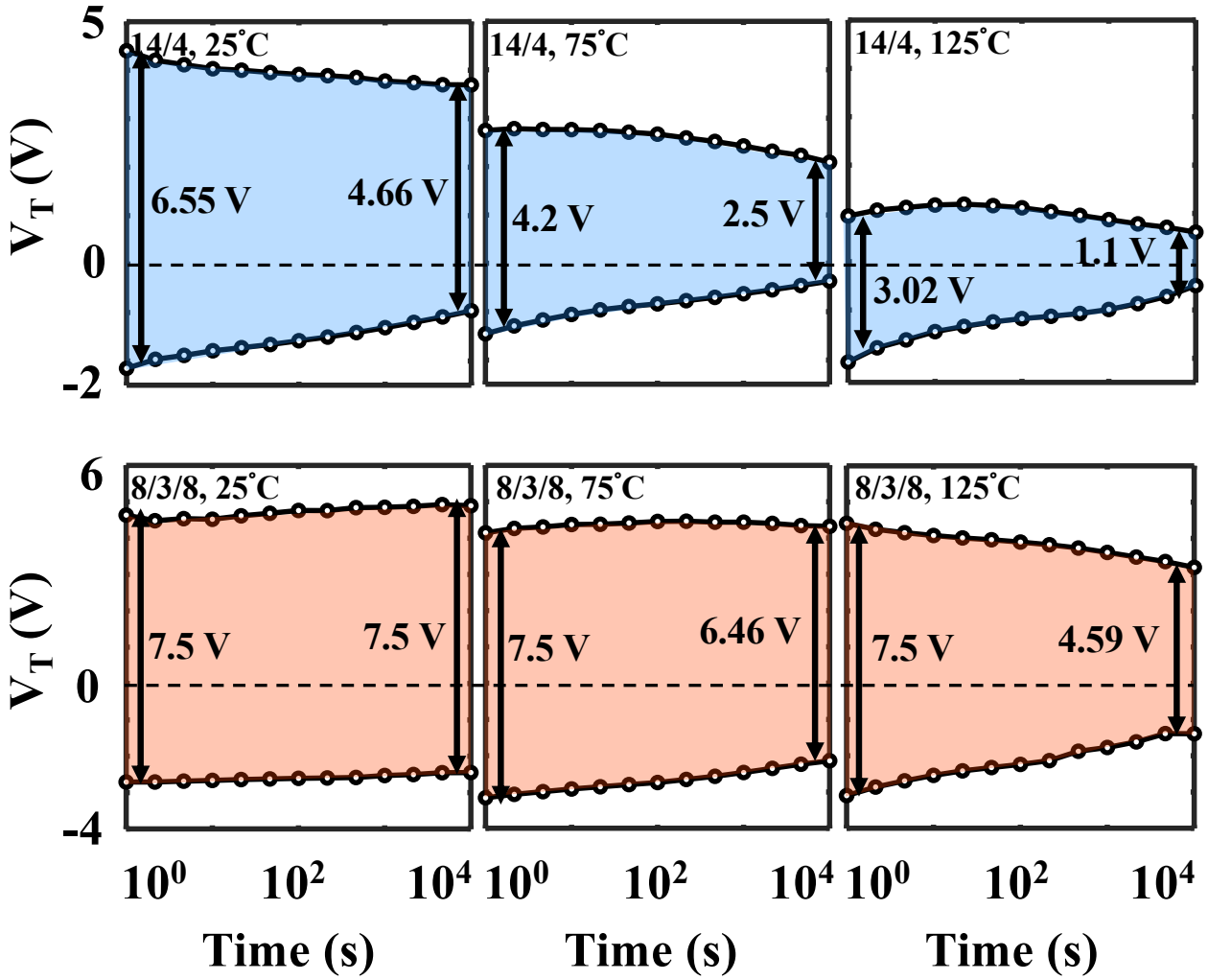




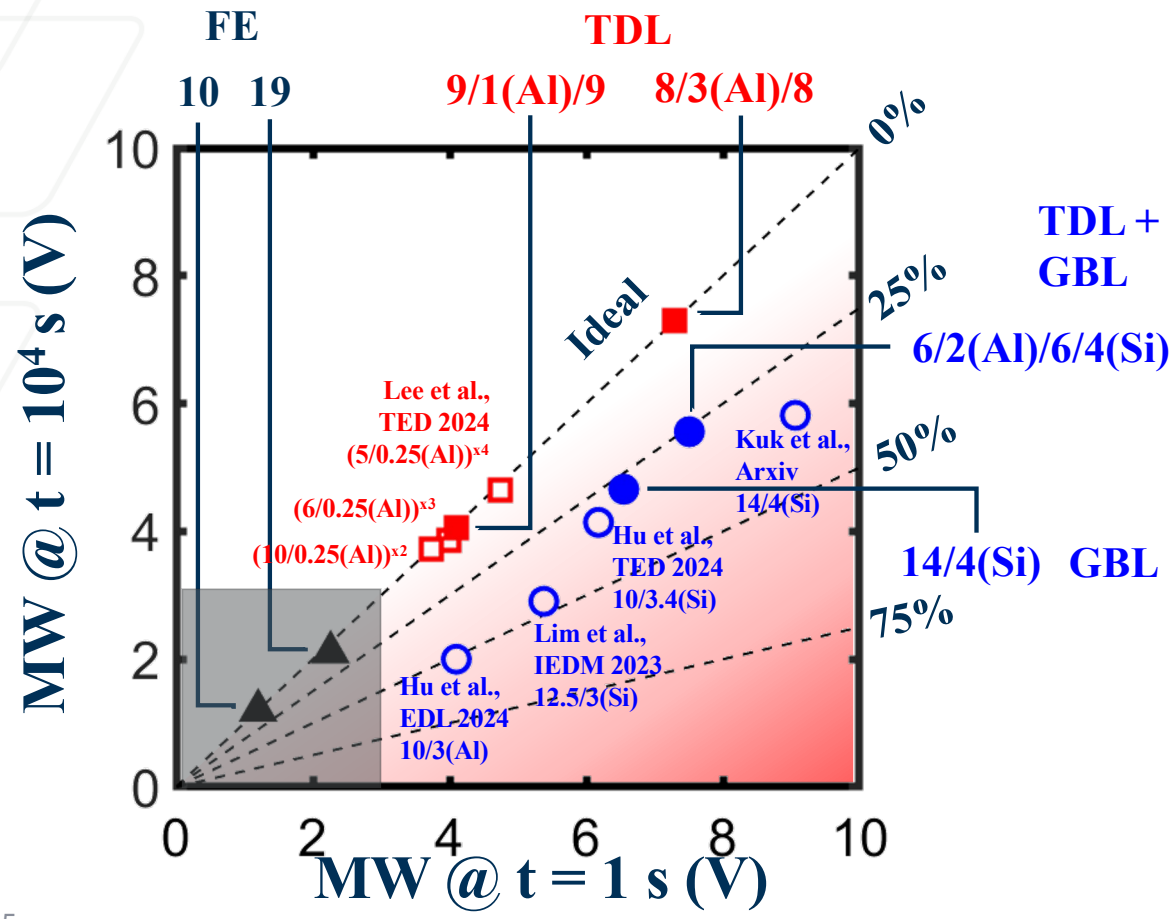
Venkatesan, Khan, et al. IRPS 2025 (Best Student Paper): https://doi.org/10.1109/IRPS48204.2025.10982749
Venkatesan, Khan, et al. EDL 2025 (Editor's Pick): 10.1109/LED.2024.3523235

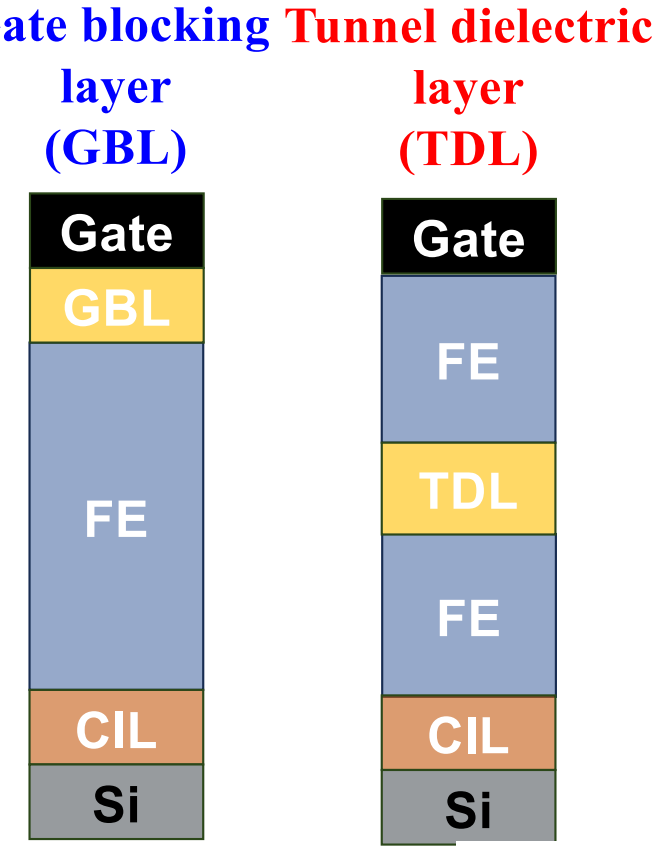
Retention characterization





MW loss in FE-NAND





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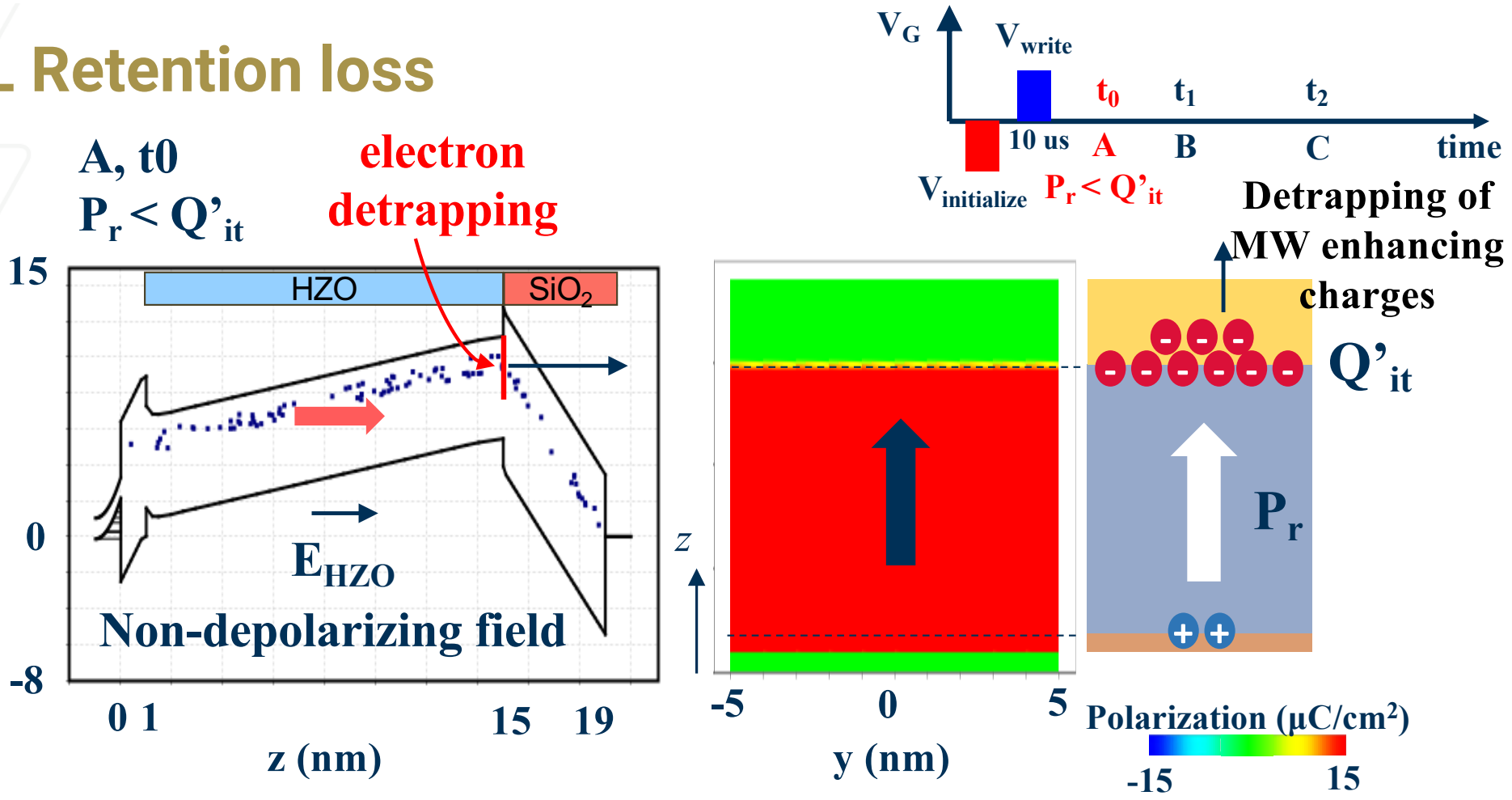
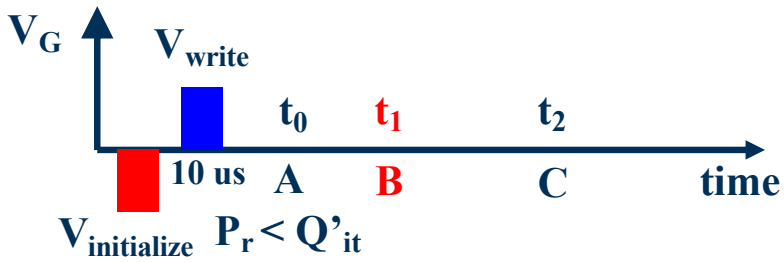
GBL Retention loss

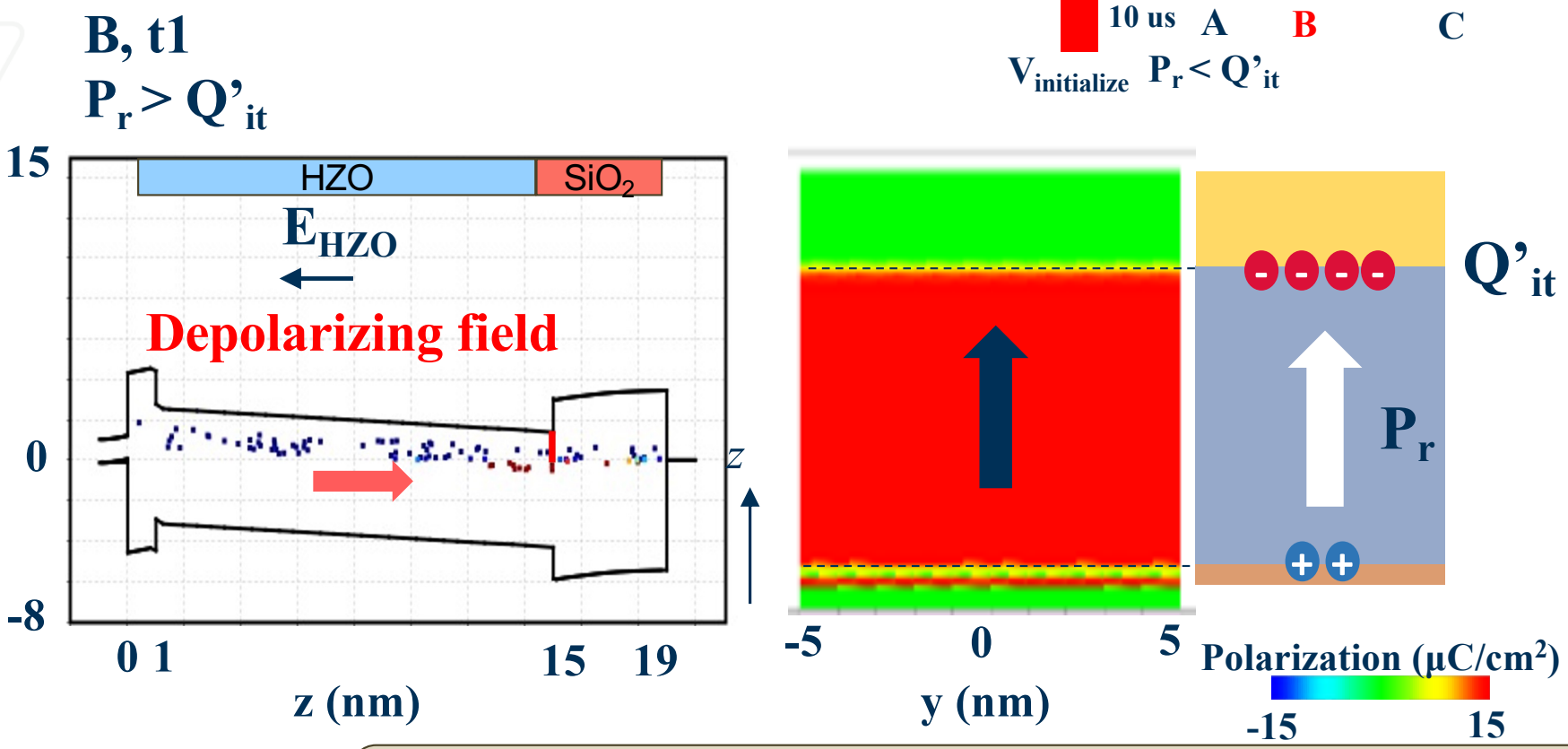


The high field across the GBL drives out the MW enhancing charges leading to loss of the MW enhancement.

Venkatesan, P., et al. IRPS 2025

GBL Retention loss





When Q'_{it} reduces below P_r, the field in the ferroelectric layer becomes depolarizing.

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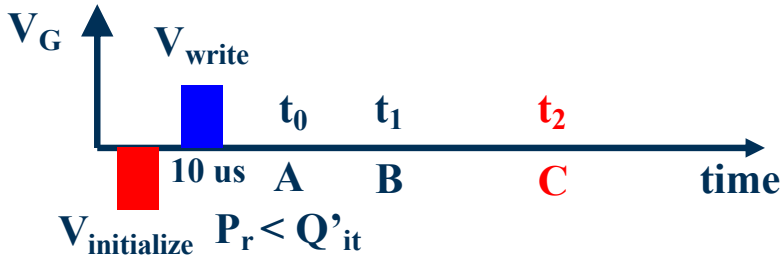
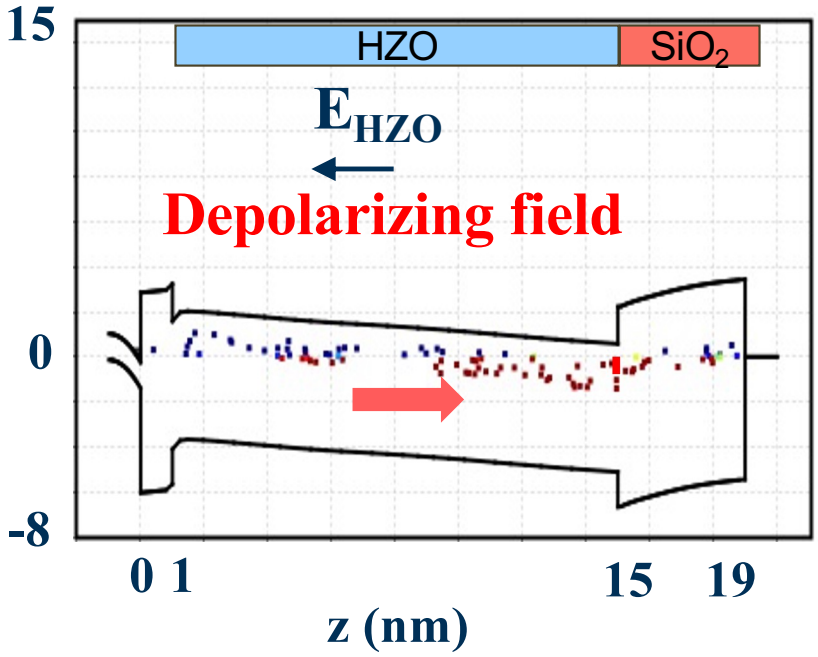
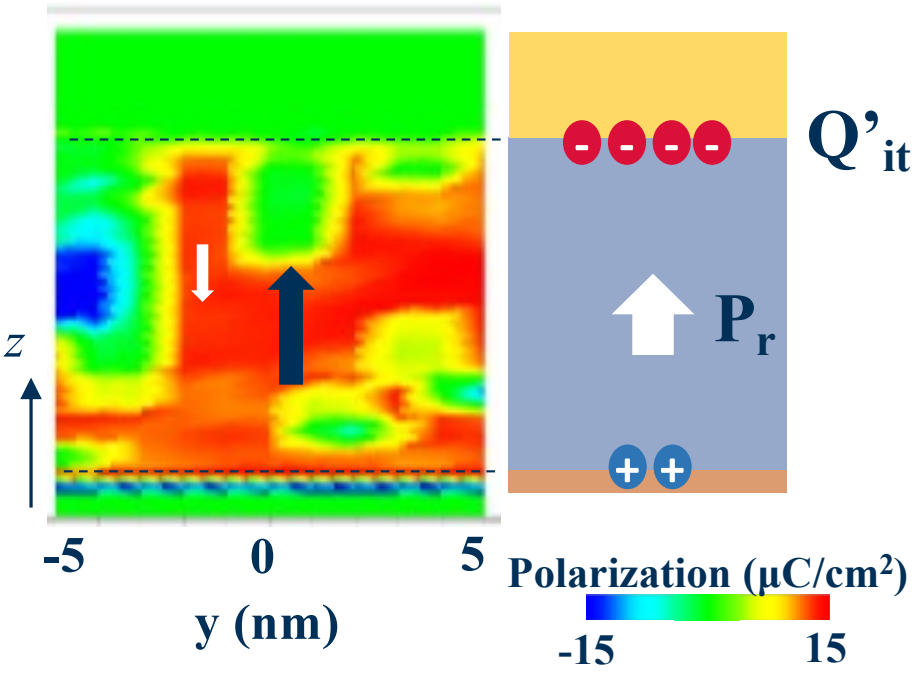
GBL Retention loss



C, t2 > t1

$P_r > Q'_{it}$





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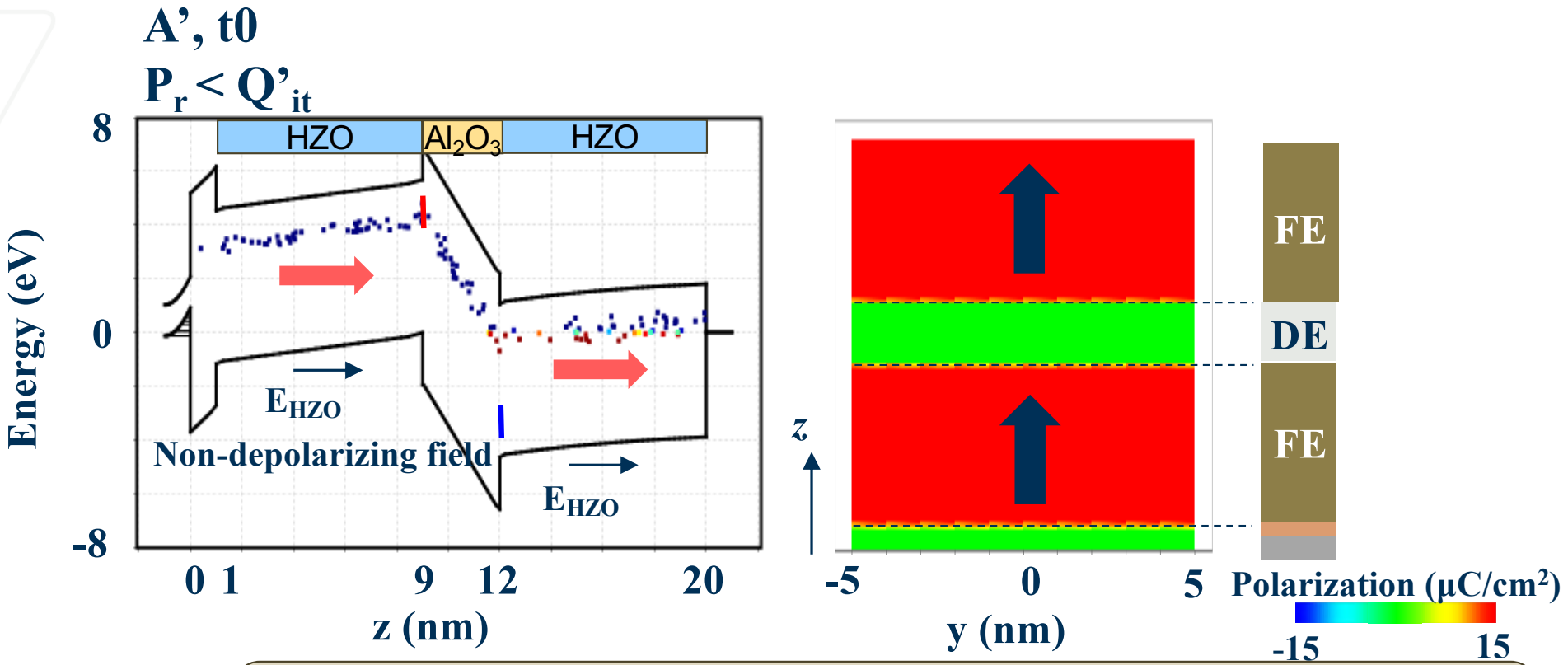
IRPS 2025

This combination of detrapping of MW enhancing charges and depolarization of ferroelectric layer leads to retention loss

TDL Retention loss



The overcompensated charge density at the FE-TDL interface, protected by the FE layers, maintains the non-depolarizing field across the FE, leading to robust retention.

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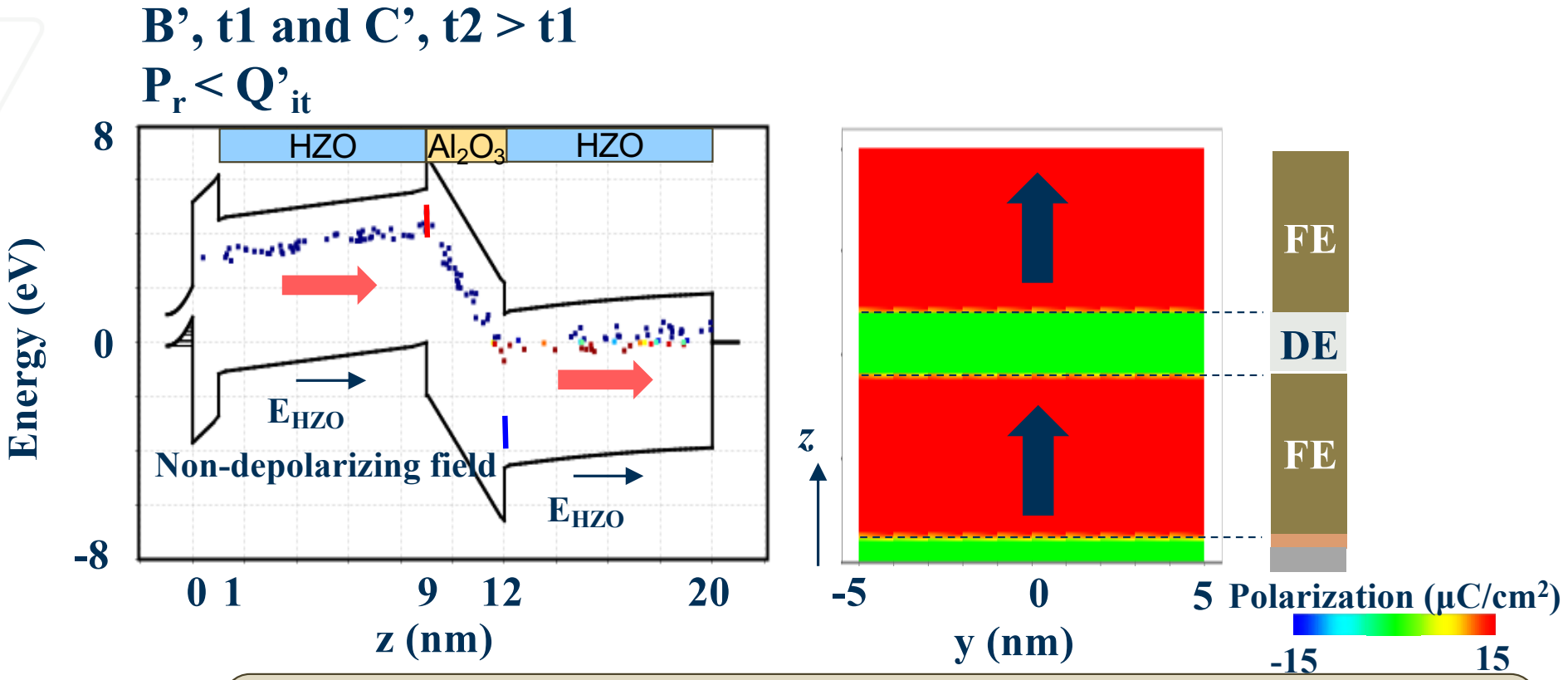
TDL Retention loss



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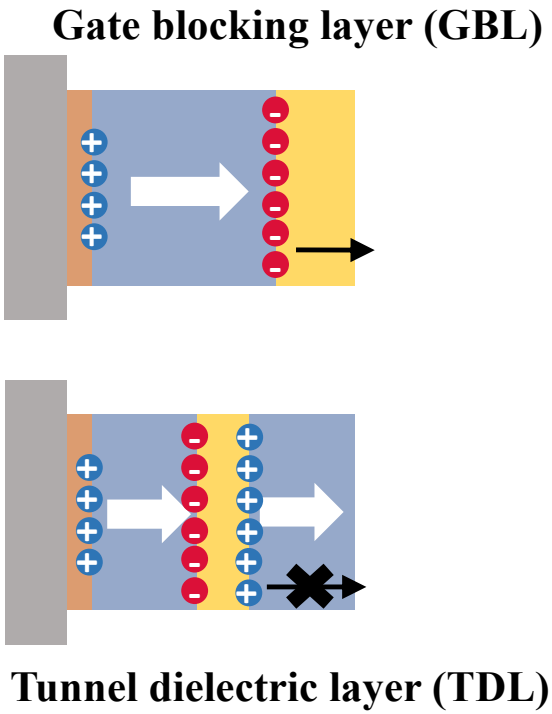
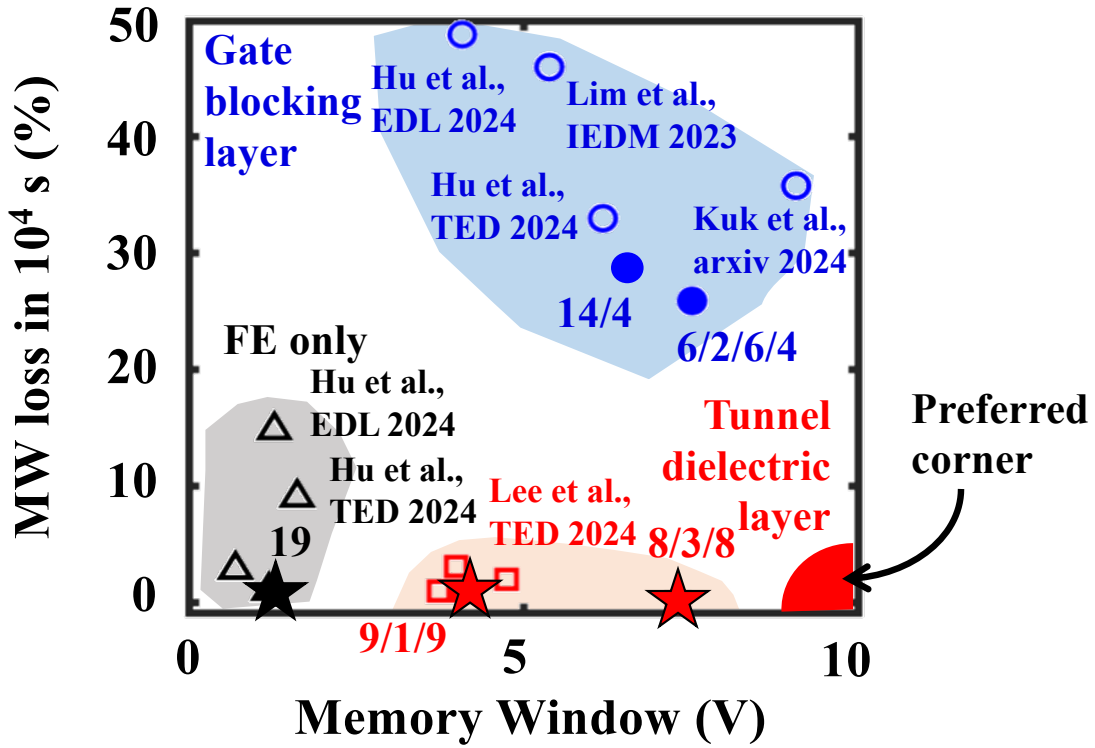
IRPS 2025

Retention benchmark





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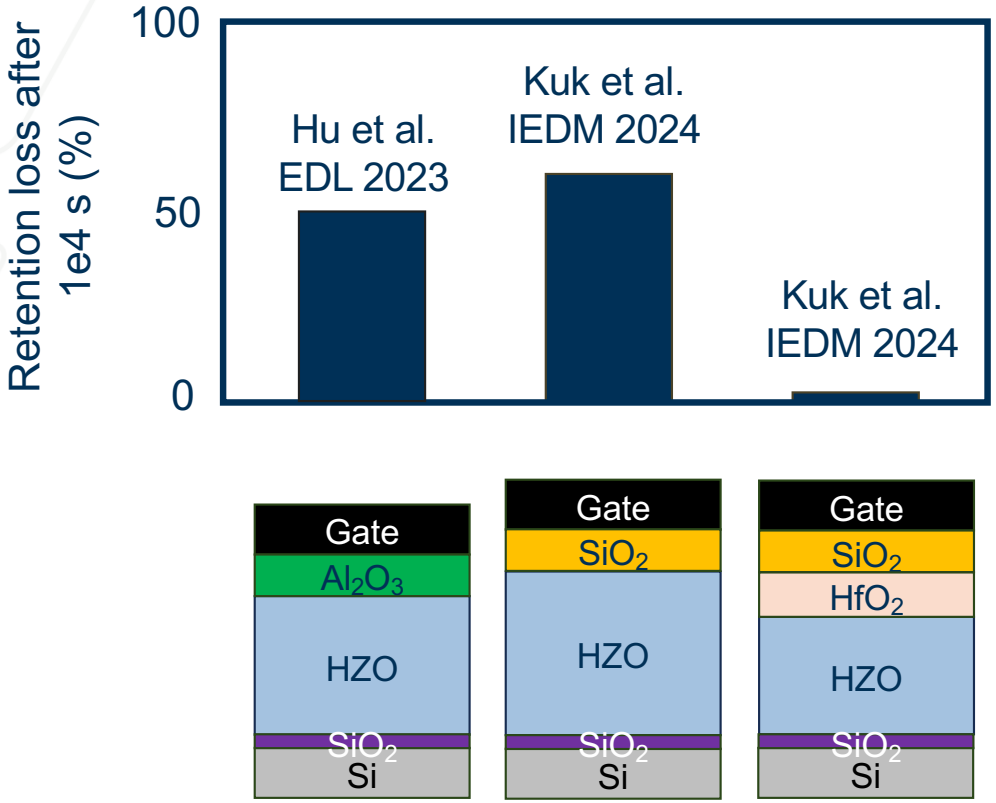
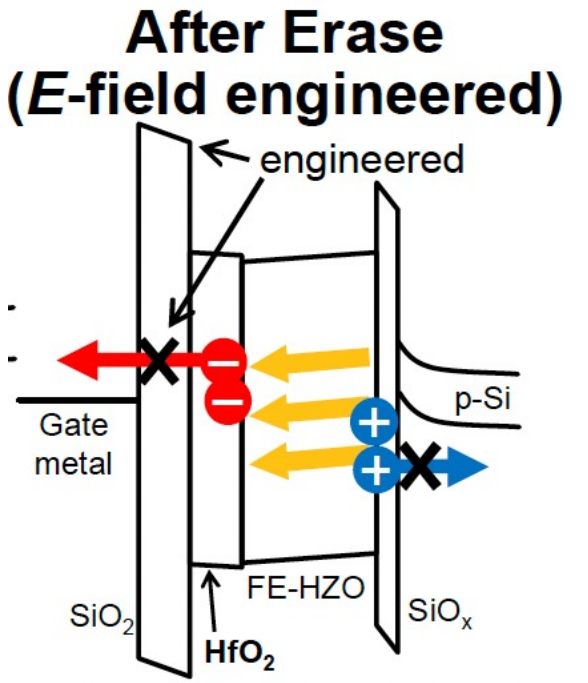
Moving the dielectric to the middle of the FE gate stack, energetically stabilizes the MW.

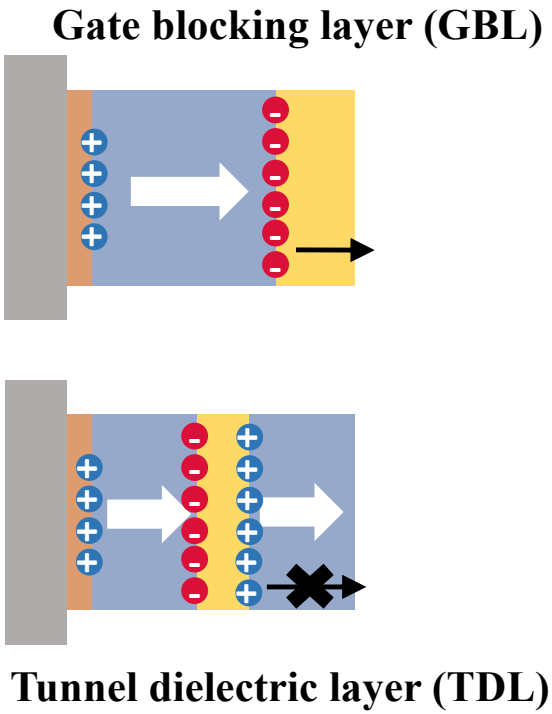
Solving retention degradation in GBL FE-NAND

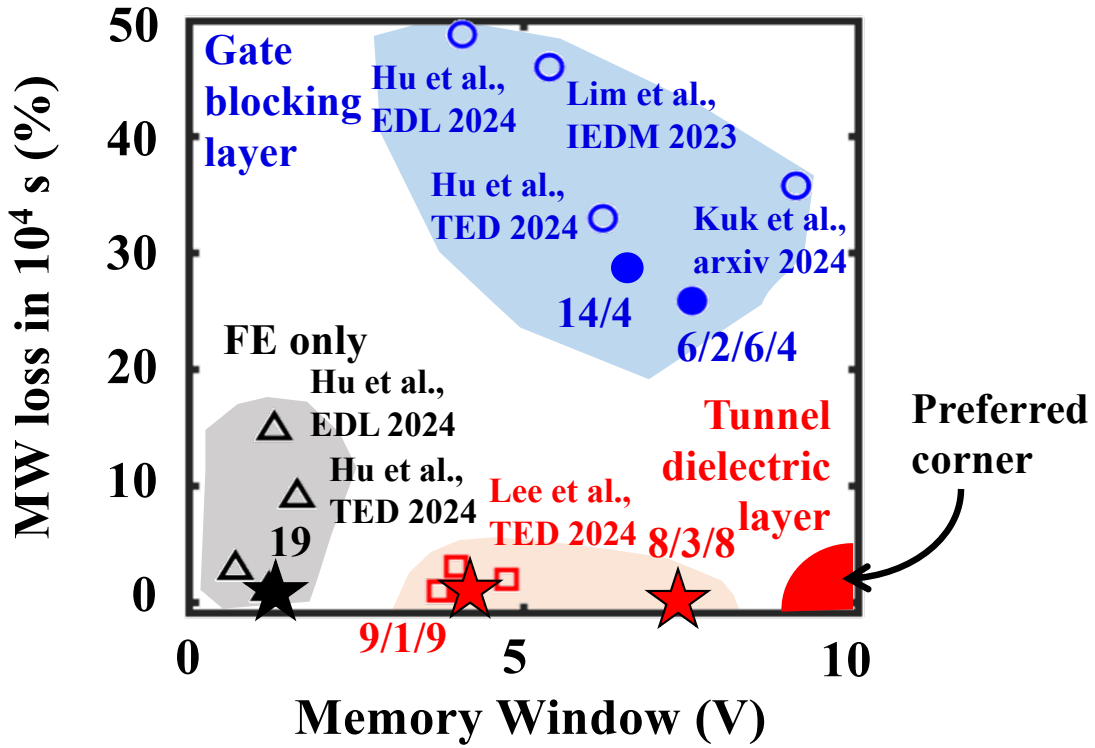




Kuk et al.
IEDM 2024

Retention benchmark





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What about reliability of ferroelectric NAND?

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Disturb

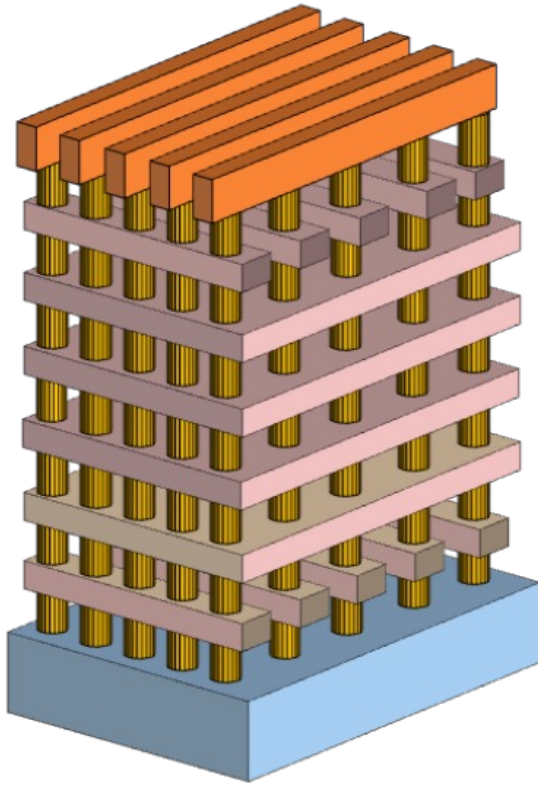
Write Endurance

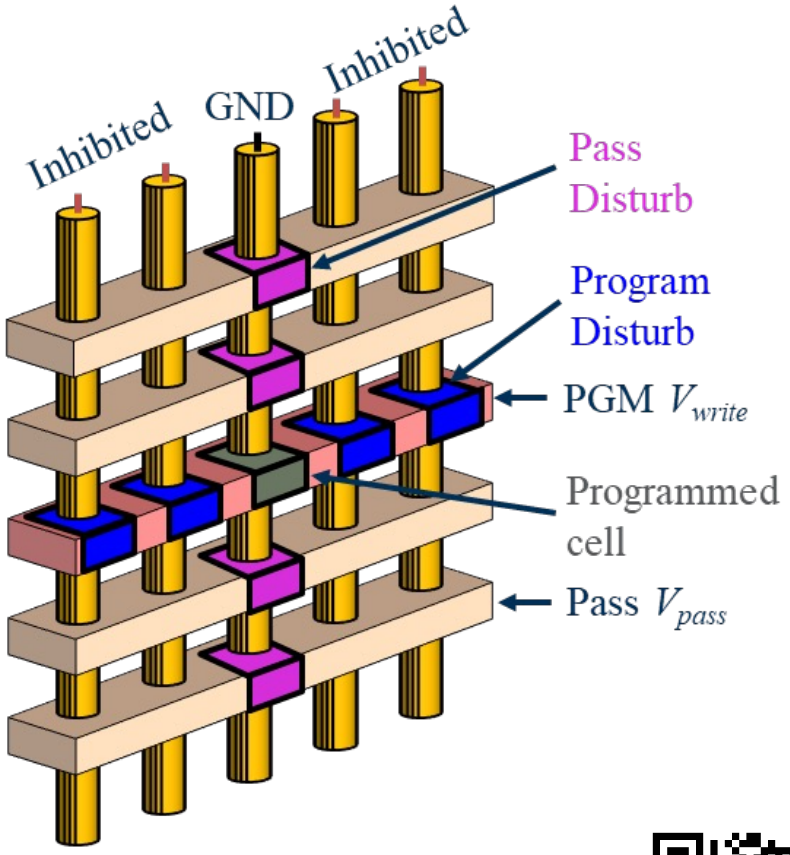
Array-level Reliability

Lateral charge migration

Device-device variation

Disturb in Ferroelectric NAND

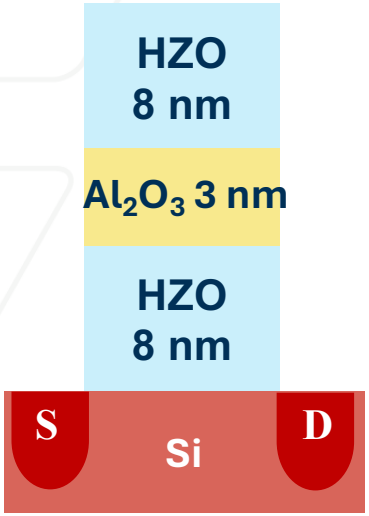


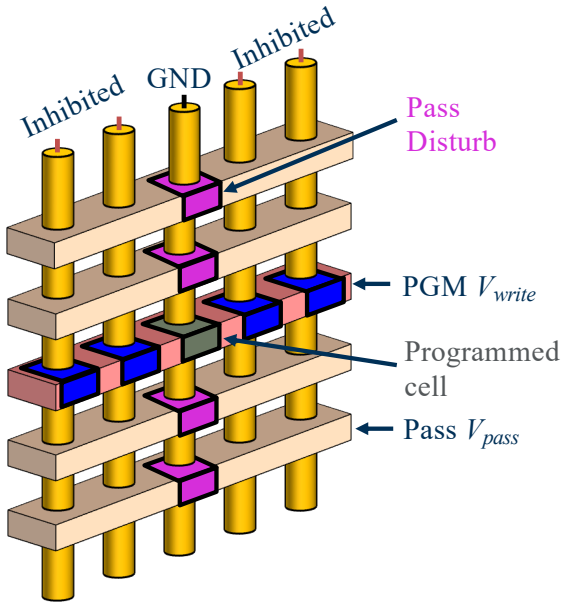


A pass voltage is applied to unaddressed cells while accessing a different cell along the bit line. This pass voltage could disturb the V_T of the cell either due to electron trapping or polarization back switching.

Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

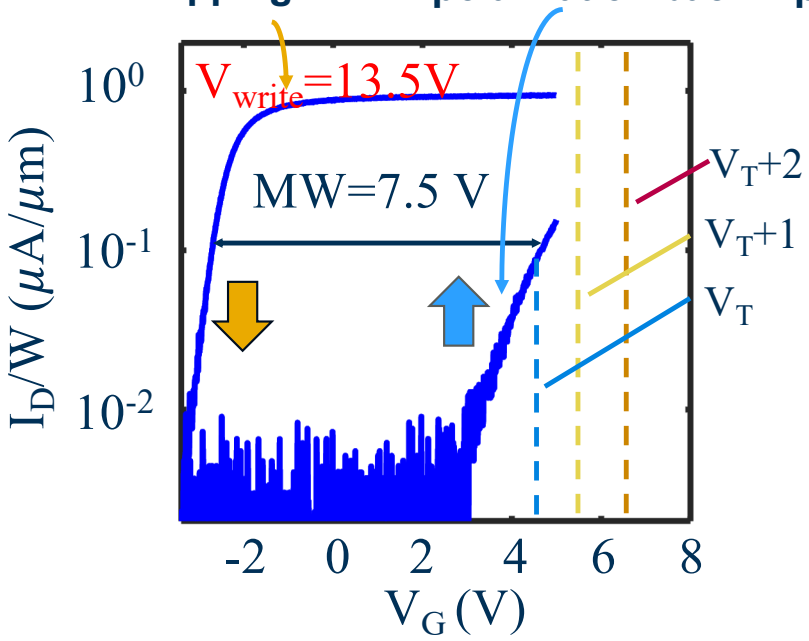
Disturb characterization





PGM state: possibility of electron trapping

ERS state: possibility of polarization back flip



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Venkatesan, P., et al. EDL 2024: 10.1109/LED.2024.3467210

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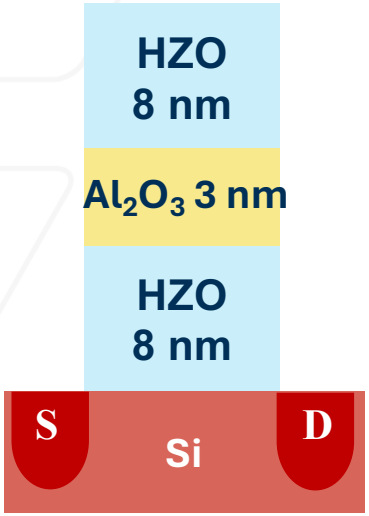

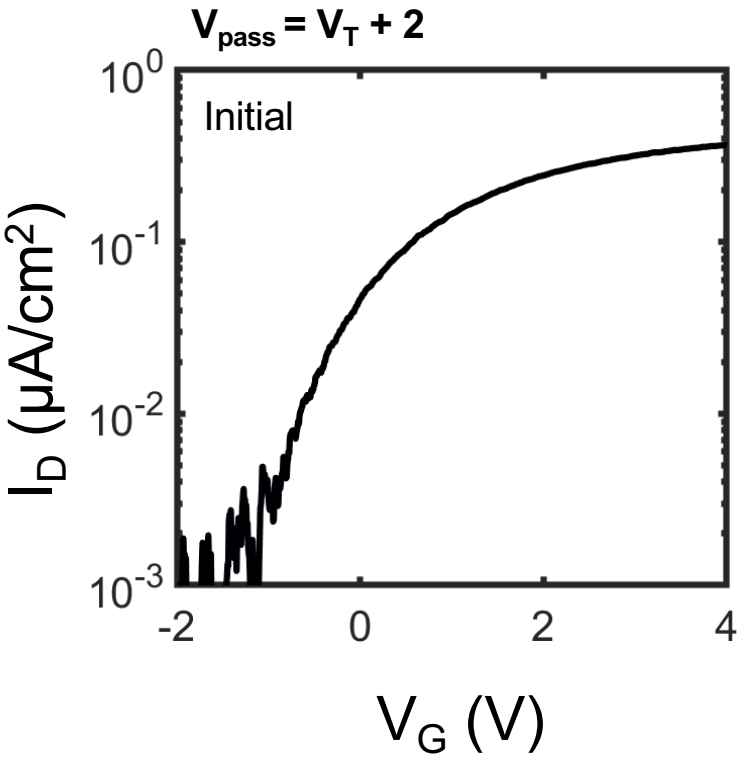

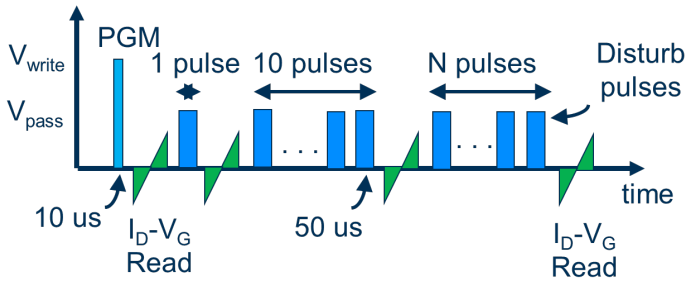

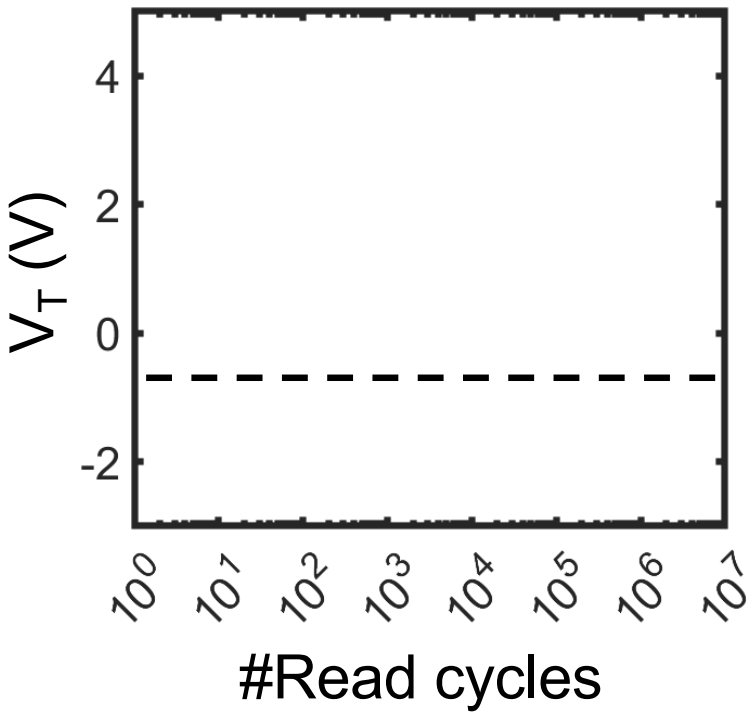

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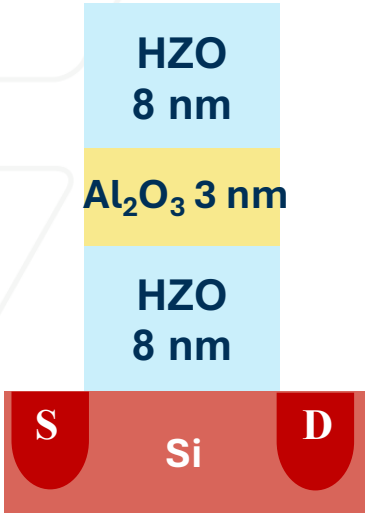
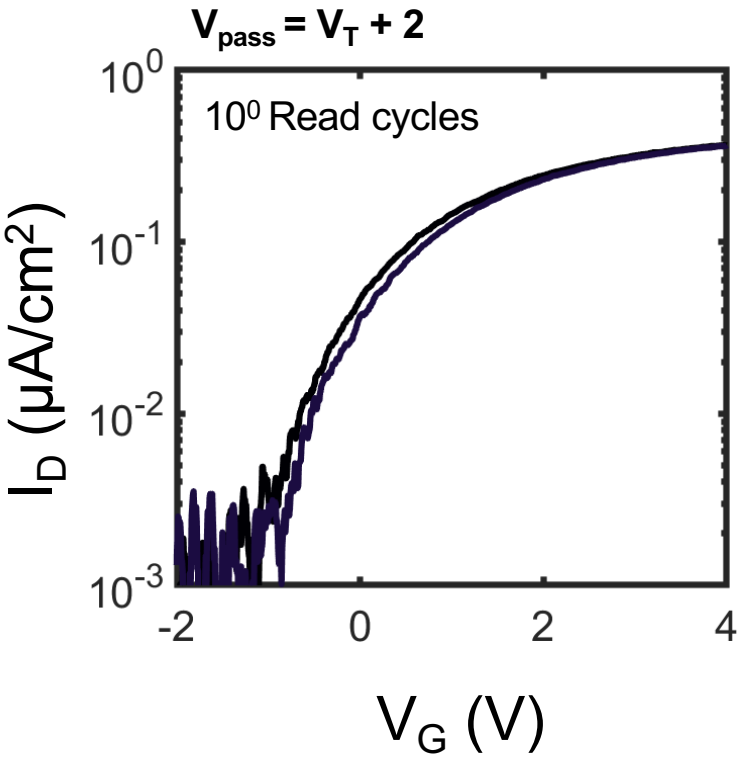
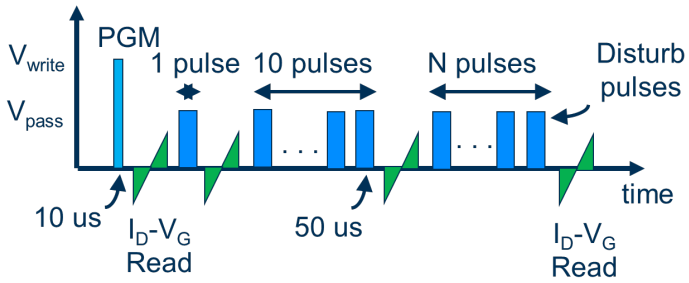
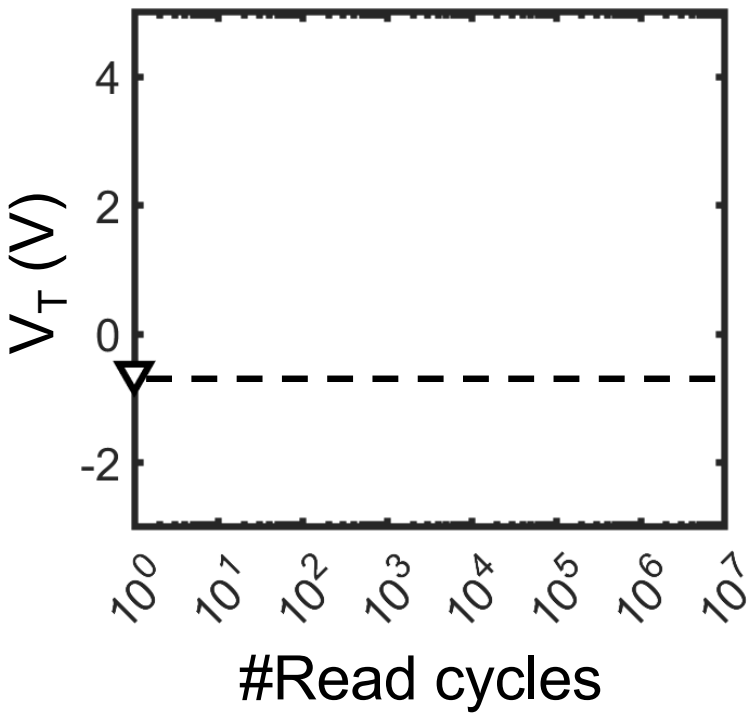
Disturb characterization









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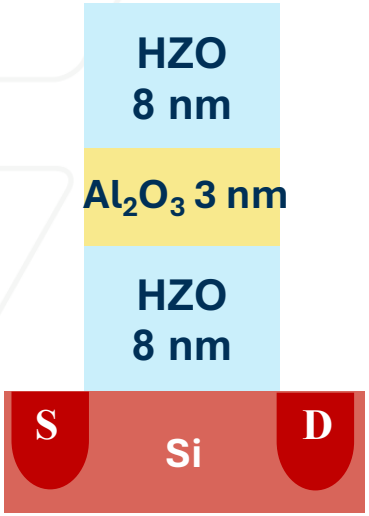
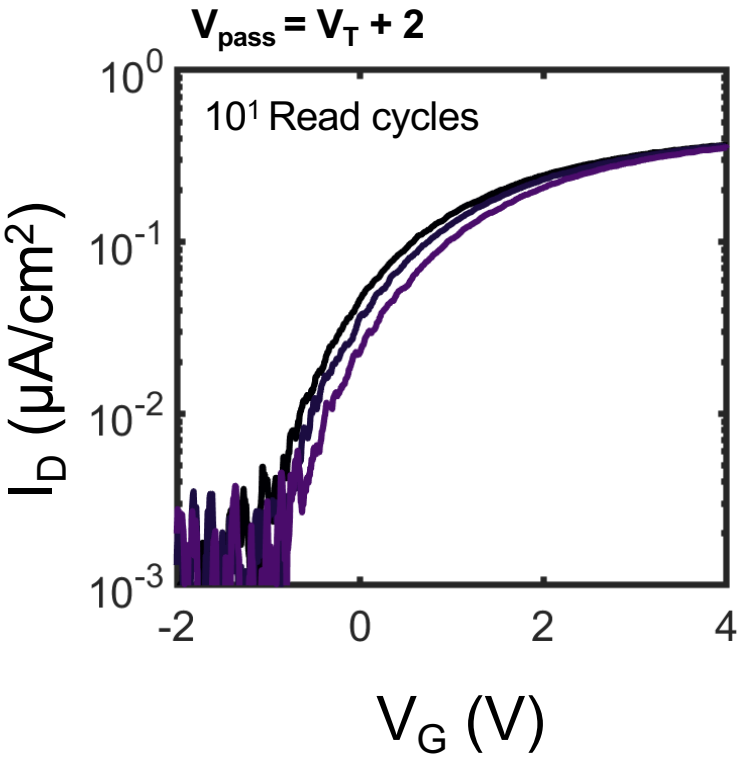
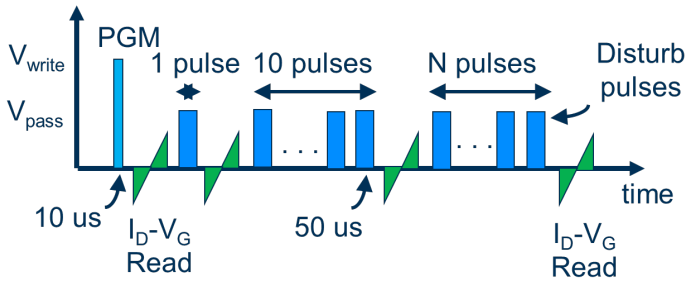
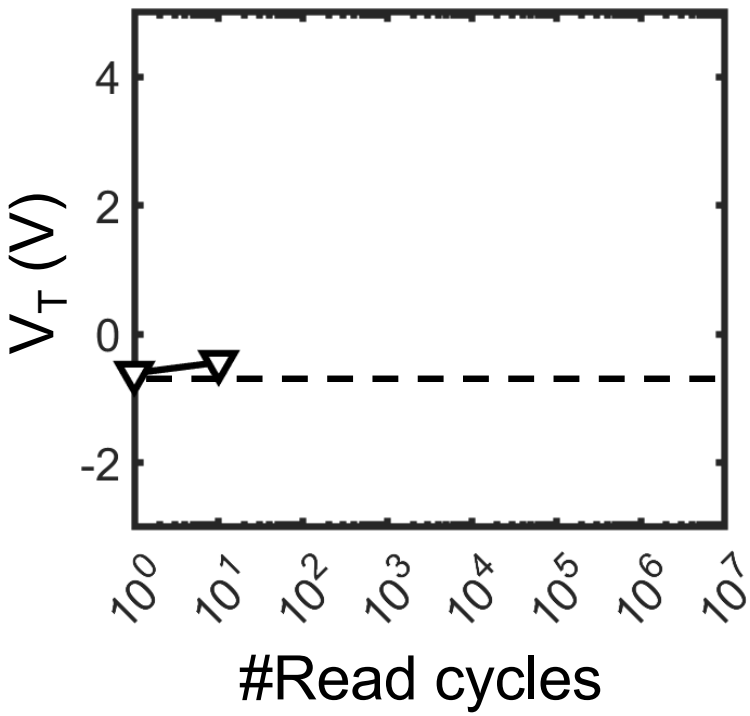


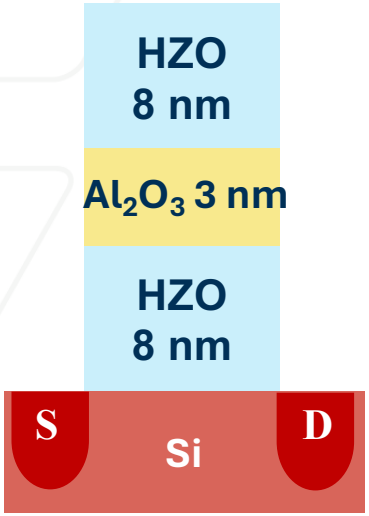


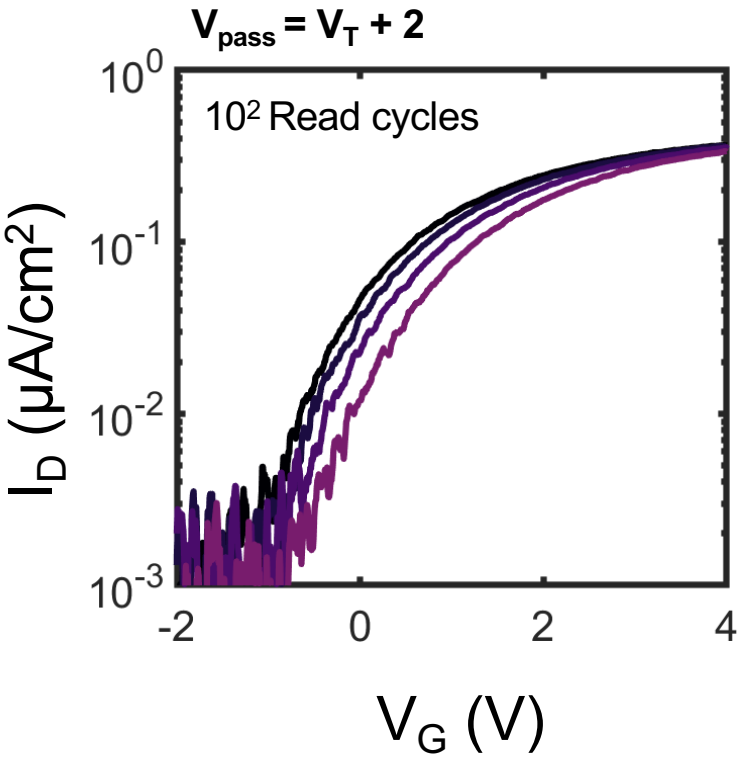


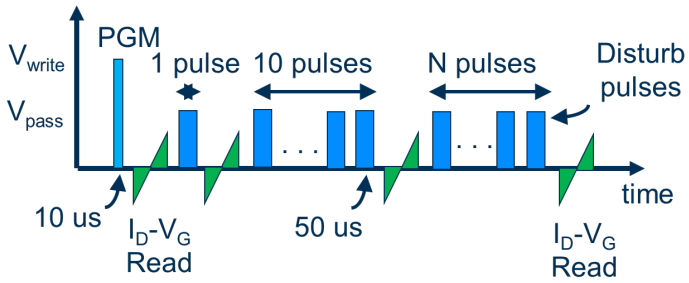


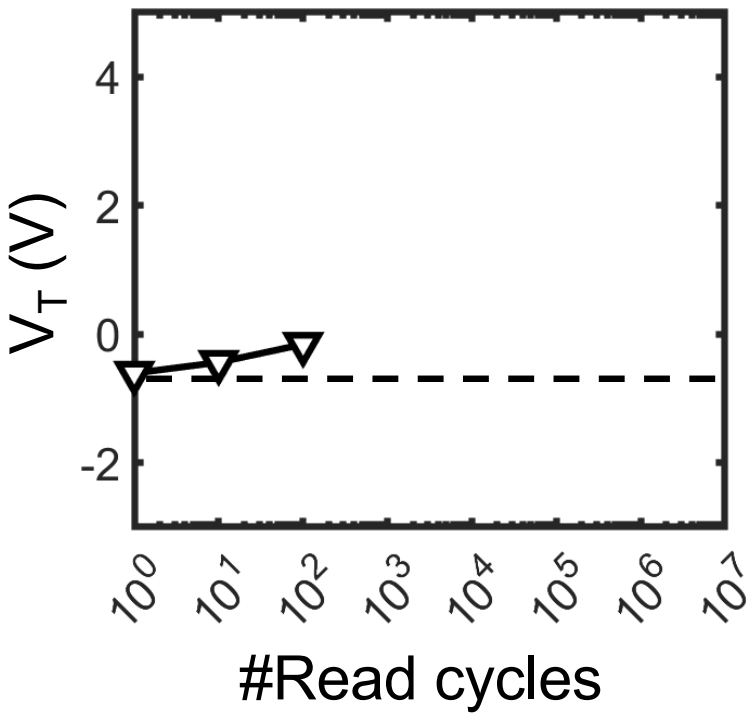
Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

Disturb characterization









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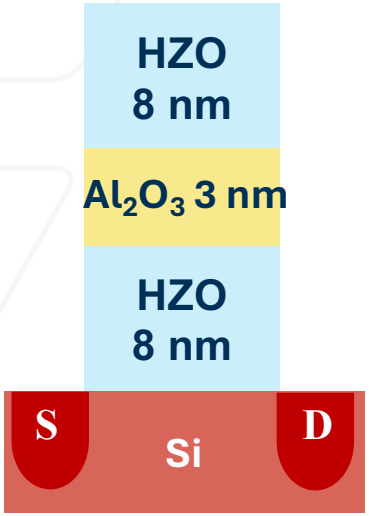
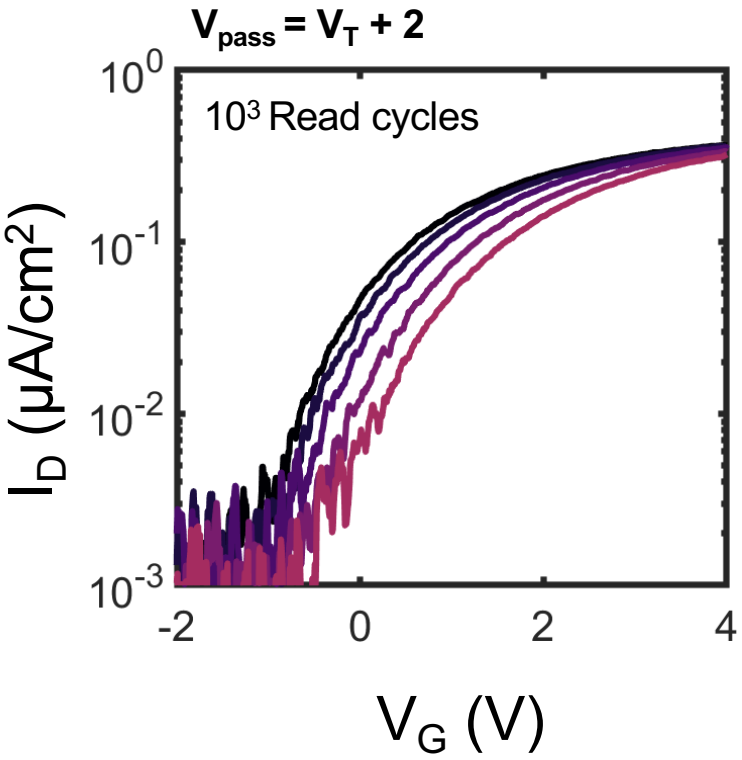
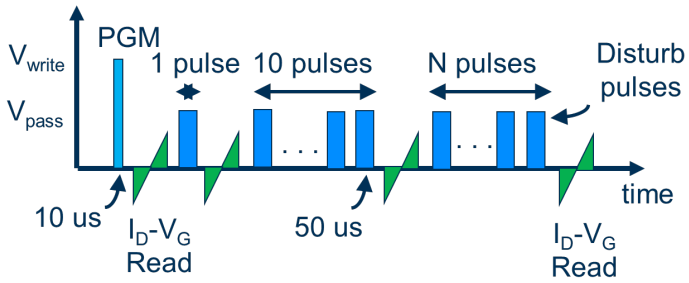
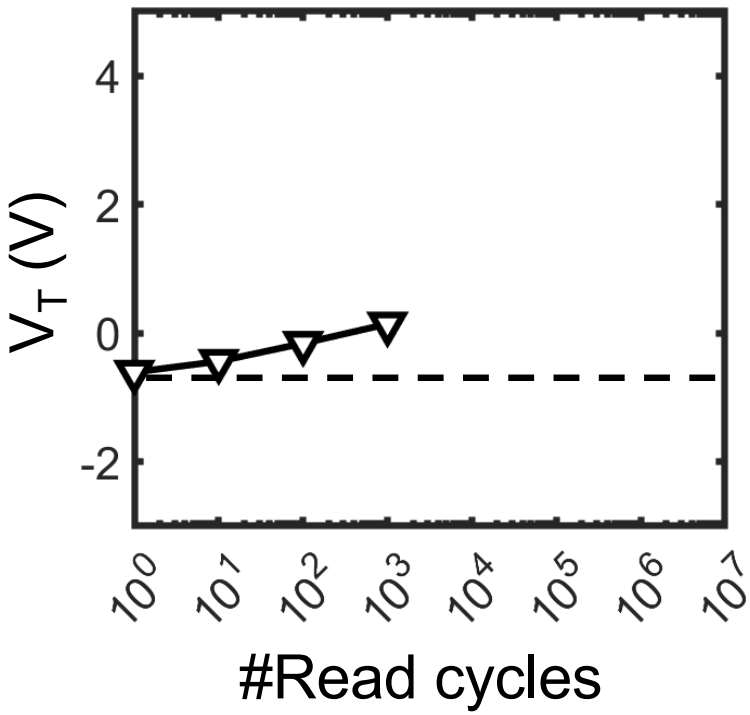
Disturb characterization









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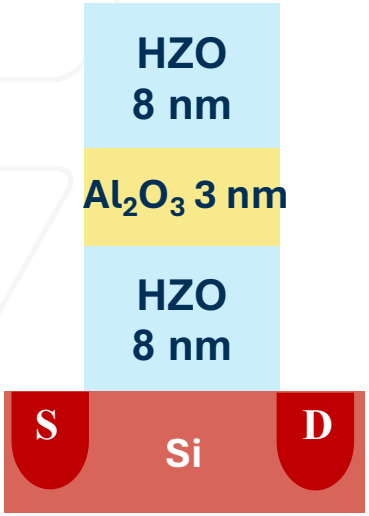
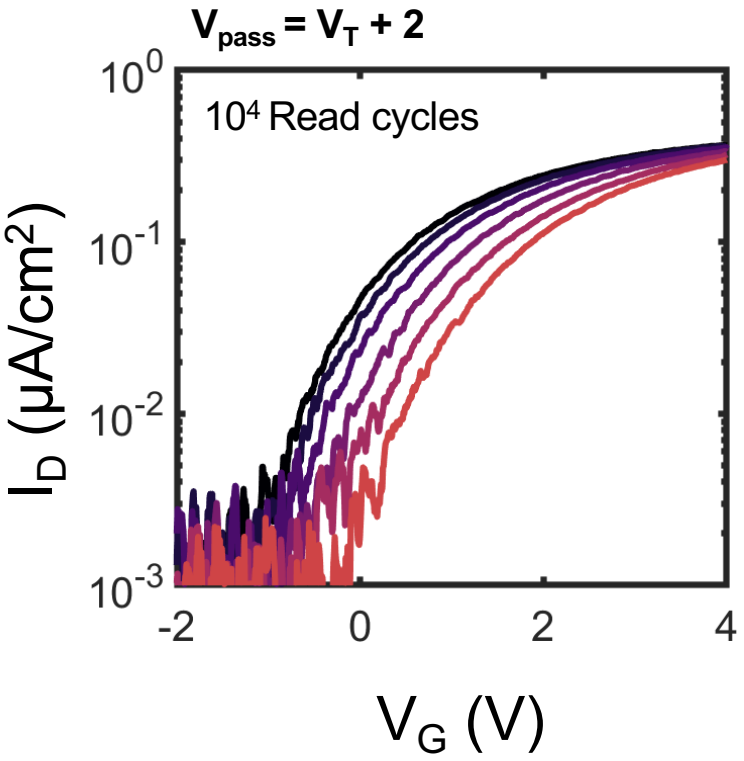
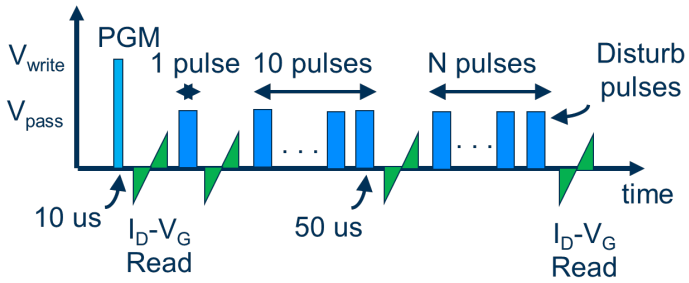
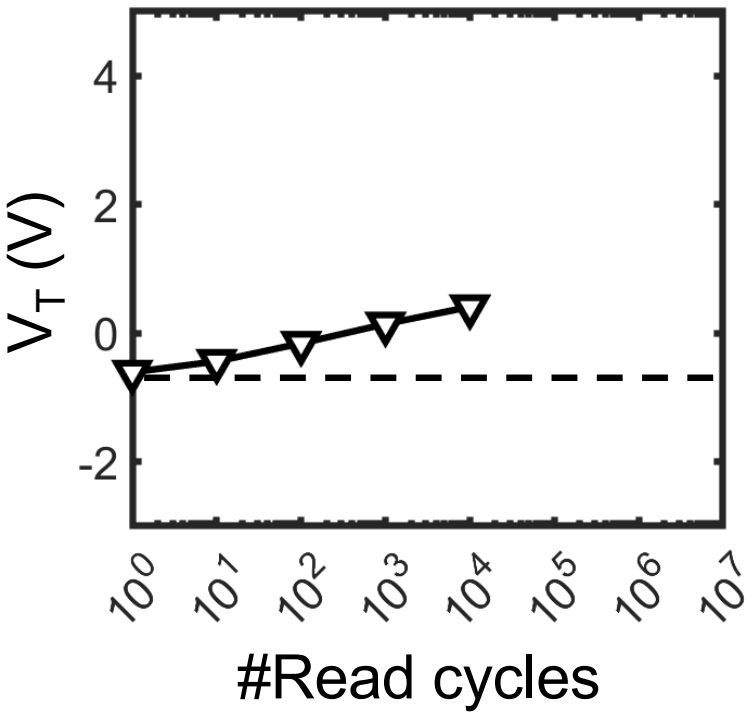
Disturb characterization



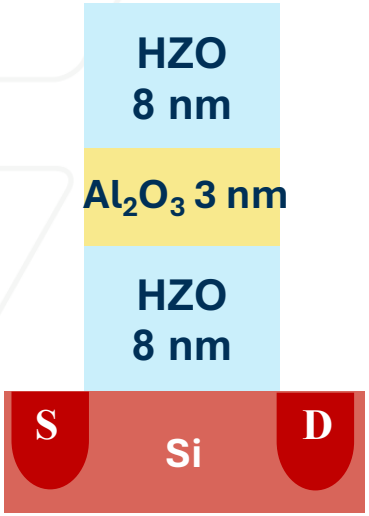


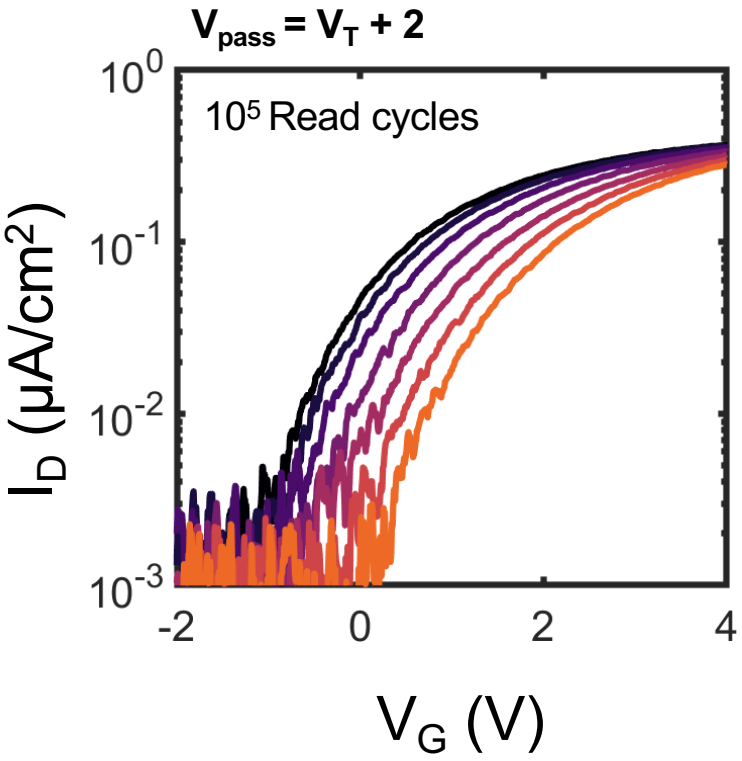


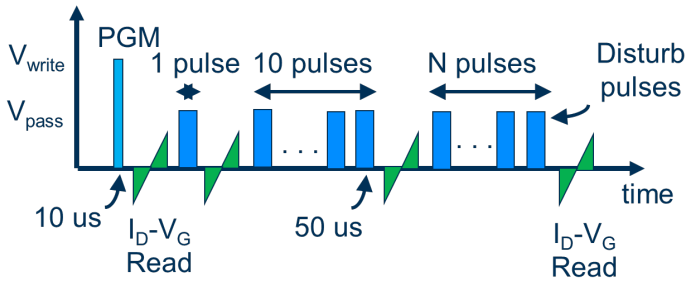


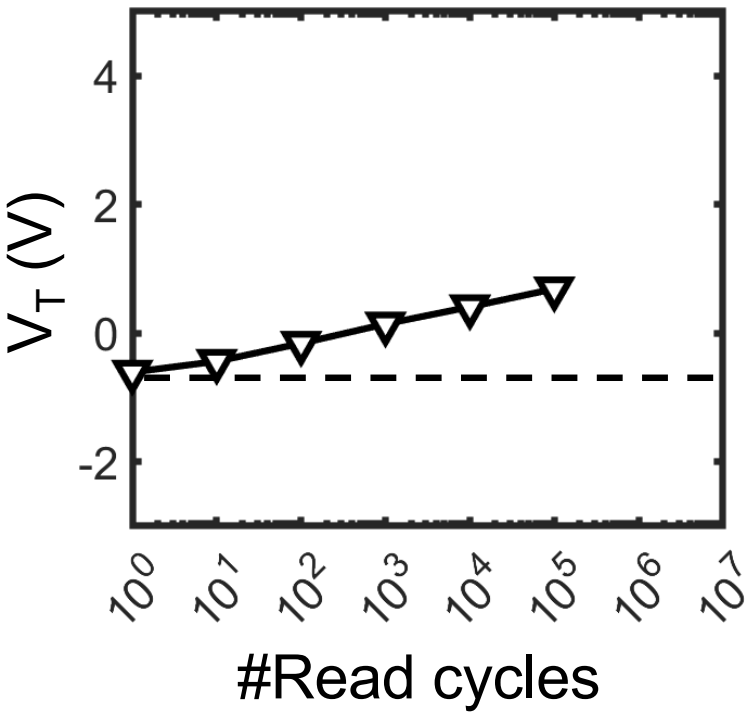
Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

Disturb characterization









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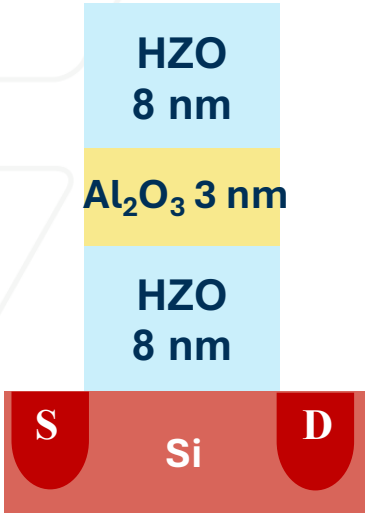

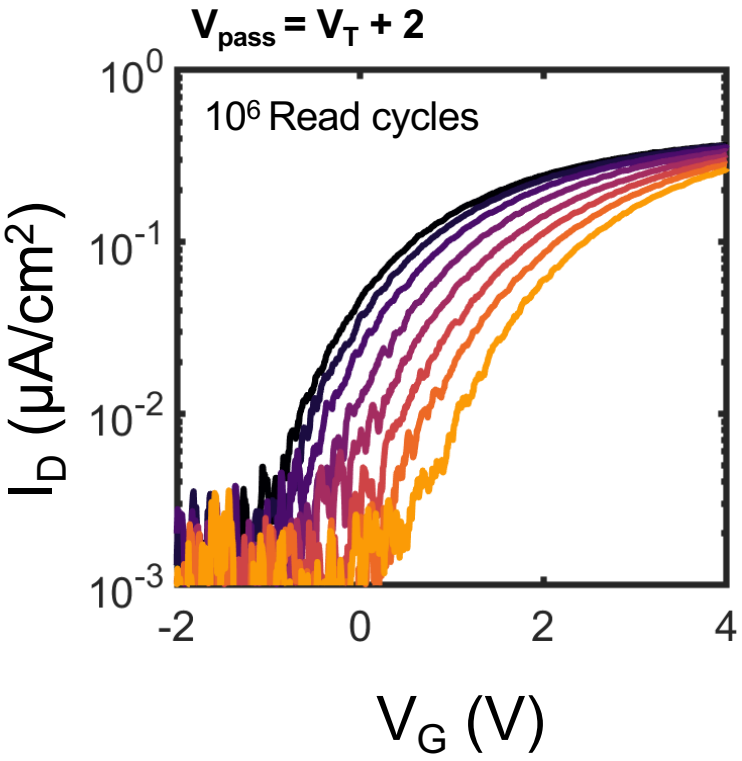

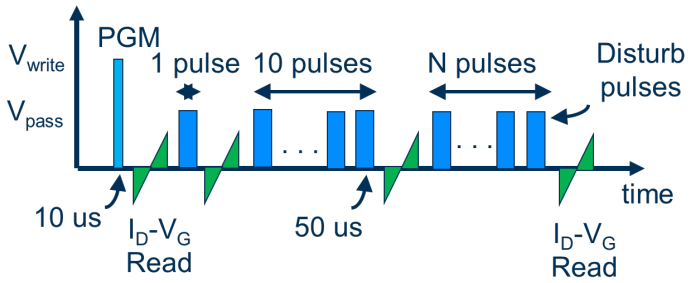

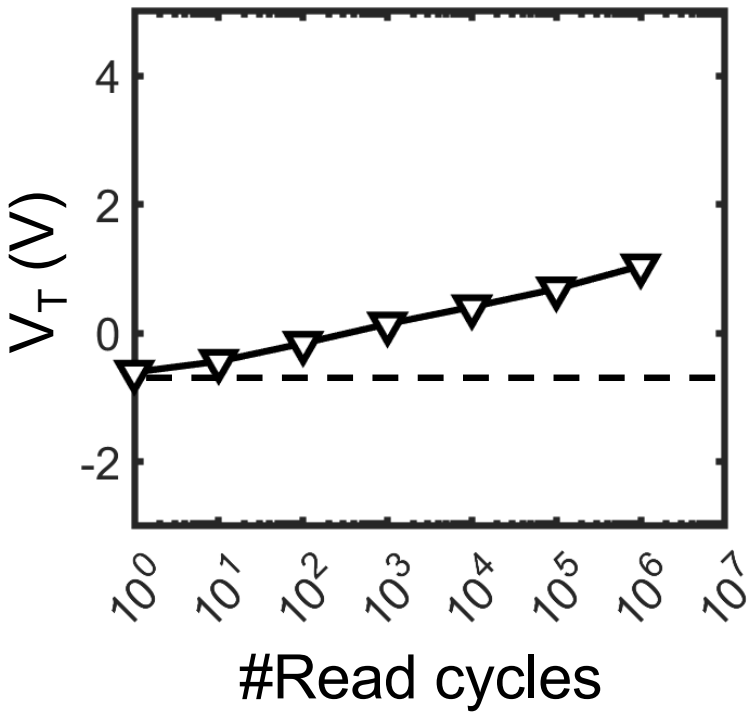

Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

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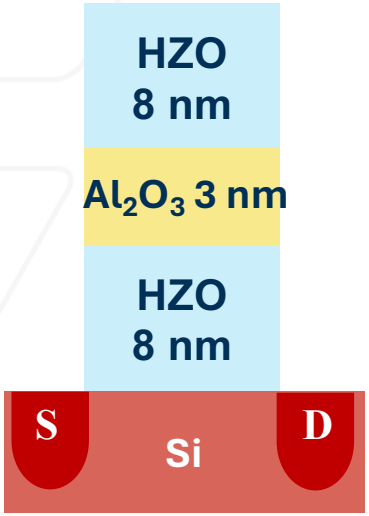
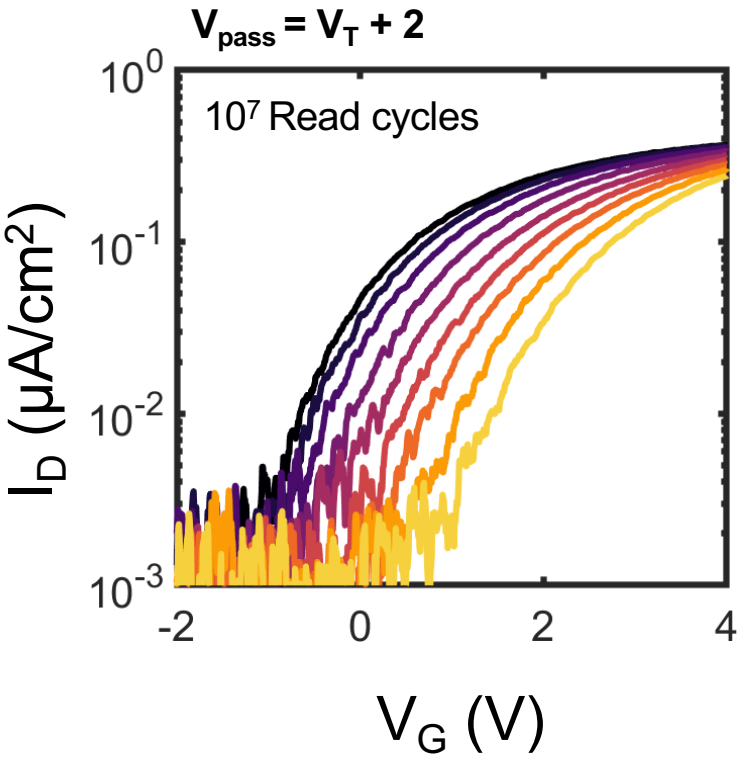
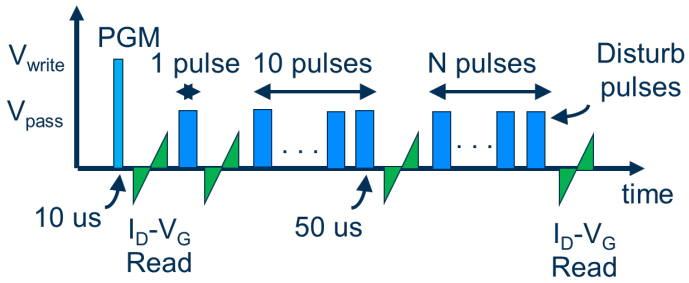
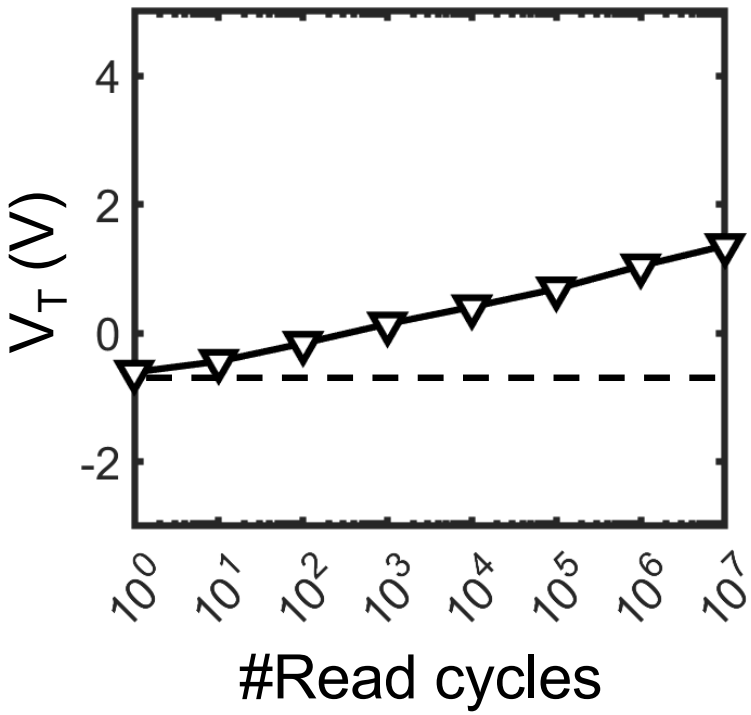


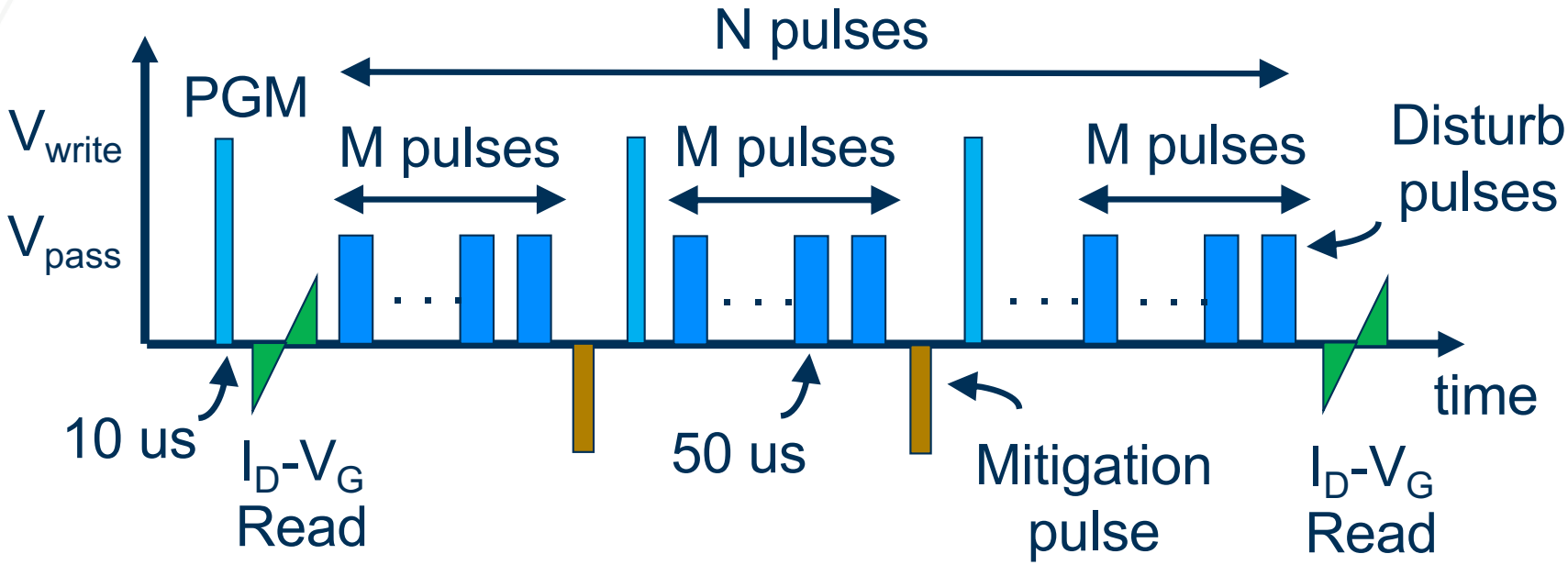






Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

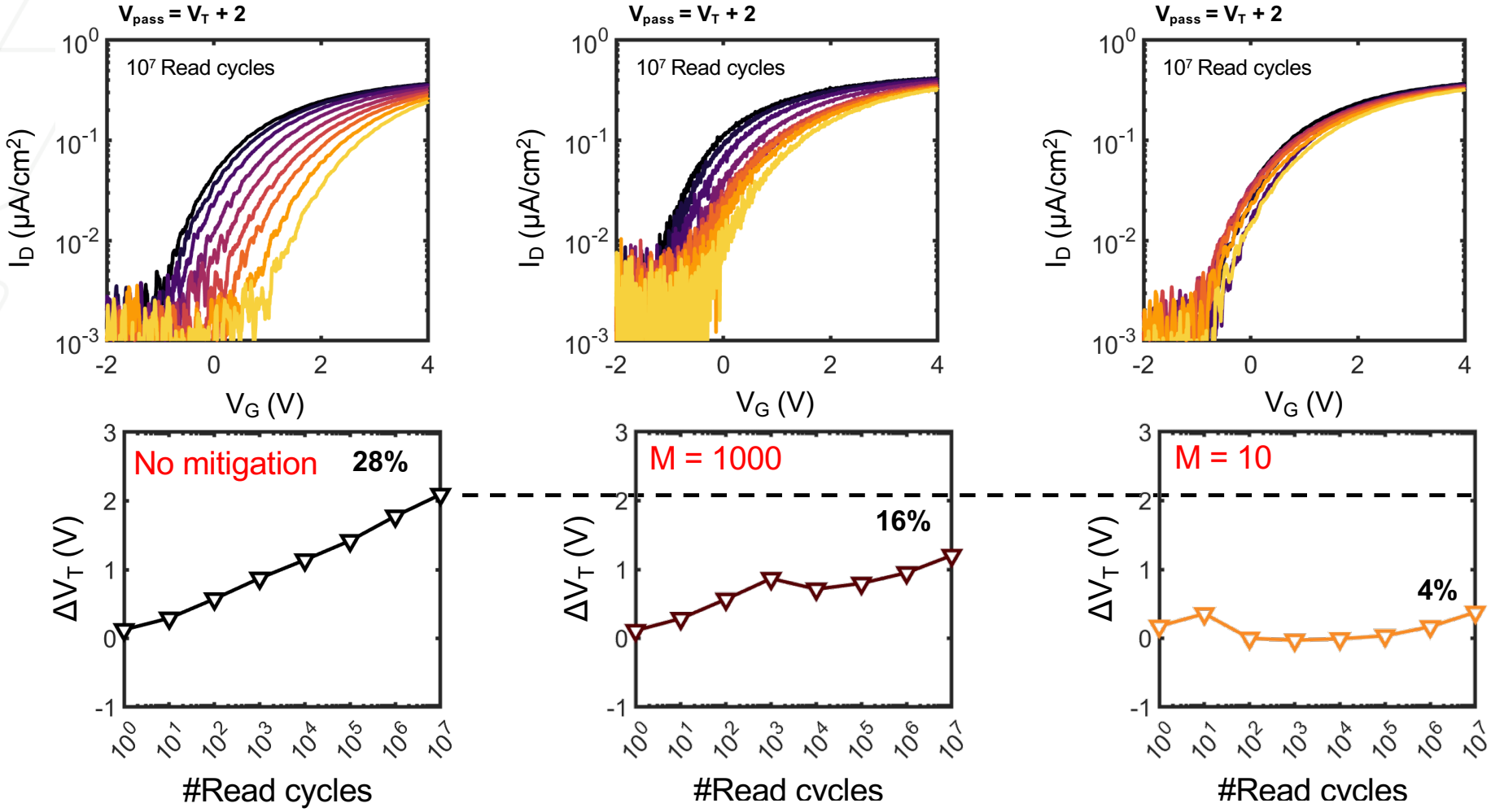
Disturb mitigation



We introduce a mitigation pulse to detrap the electrons trapped due to the disturb pulses

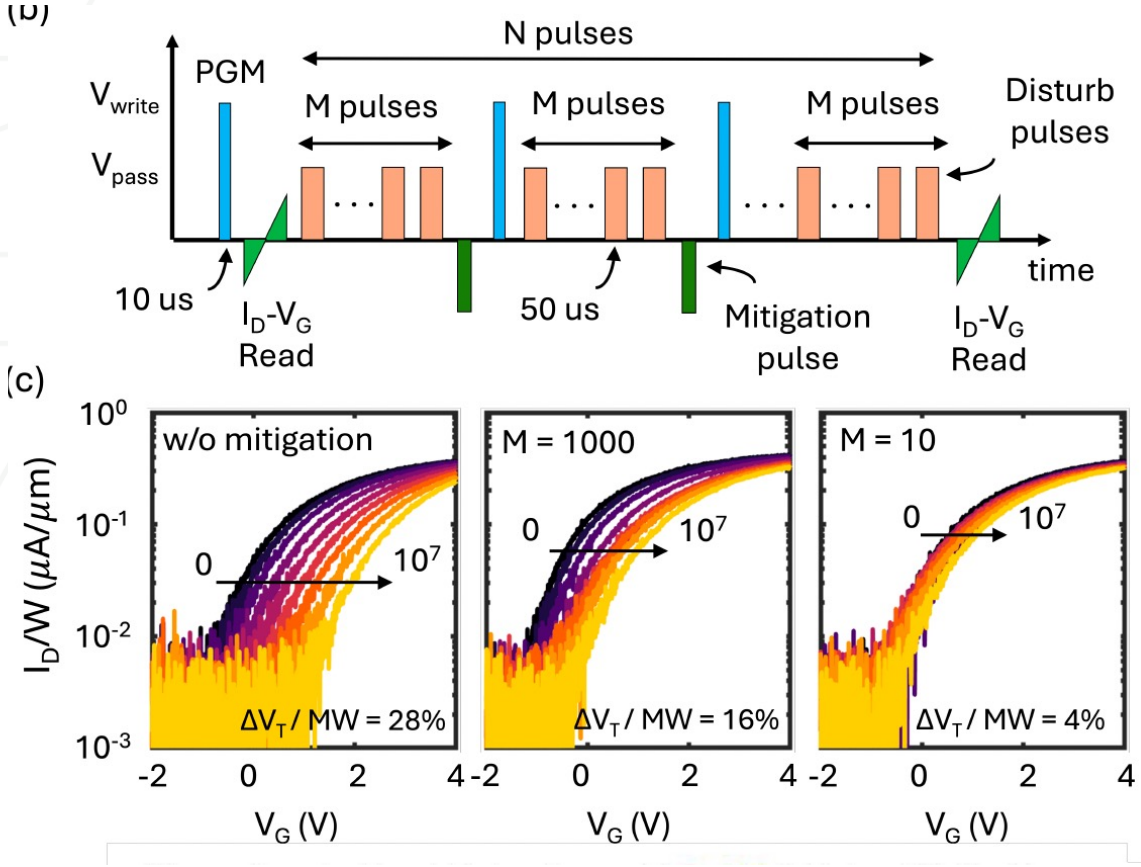
Venkatesan, P., et al. EDL 2024: 10.1109/LED.2024.3467210

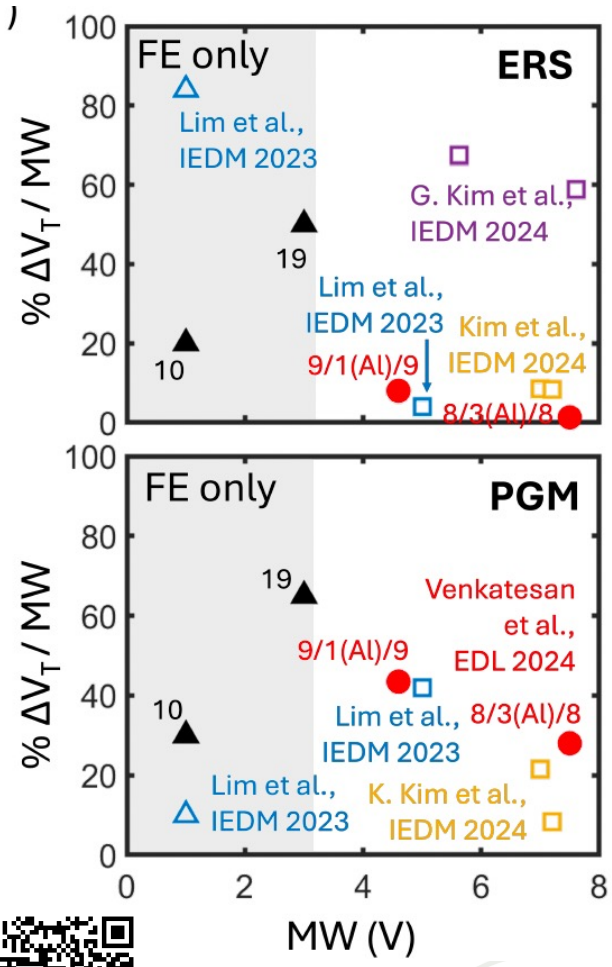
Disturb characterization



Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

Summary of Pass disturb





Mitigation scheme reduces pass disturb down to 4%!!

Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

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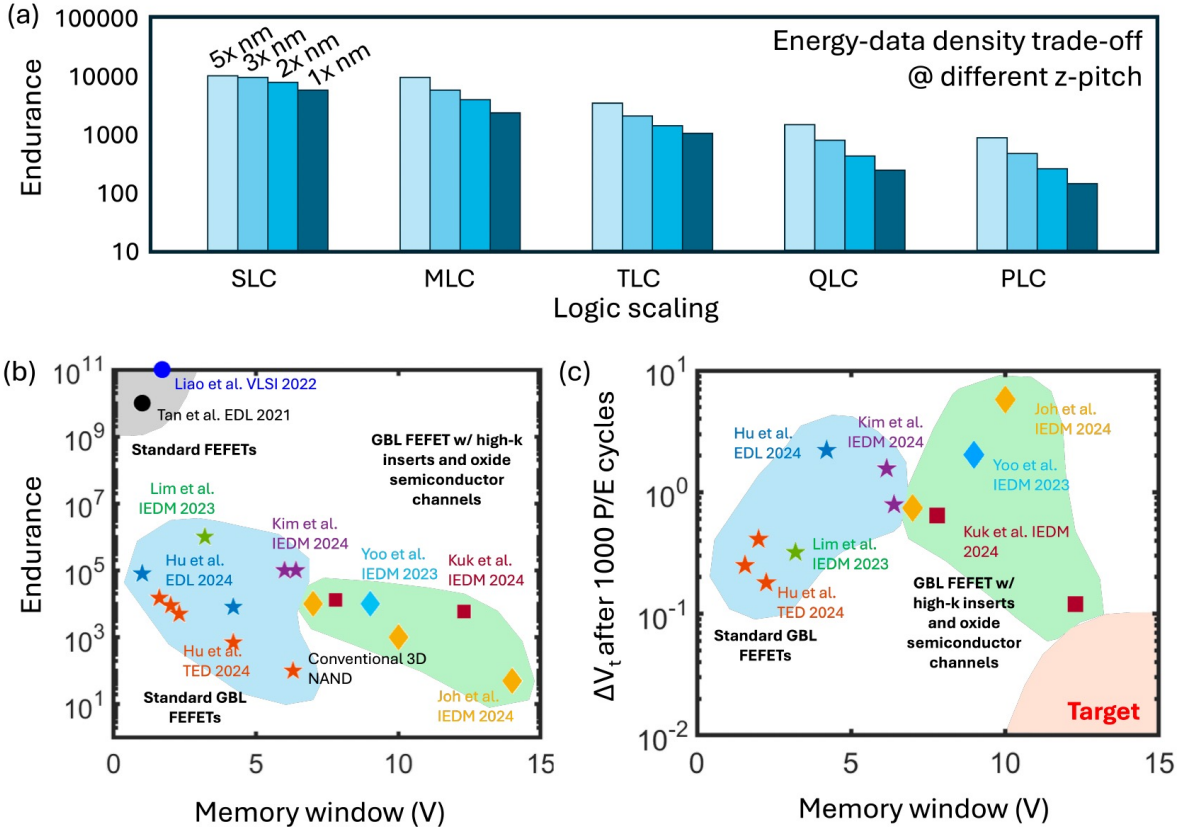
What about reliability of ferroelectric NAND?

Performance	Device Reliability	Array-level Reliability
Memory window	Retention	Lateral charge migration
	Disturb	Device-device variation
	Write Endurance	

Write Endurance



Venkatesan, P., et al. IMW 2025

Endurance decreases with increasing MW

IL degradation drives V_t shift in FEFETs

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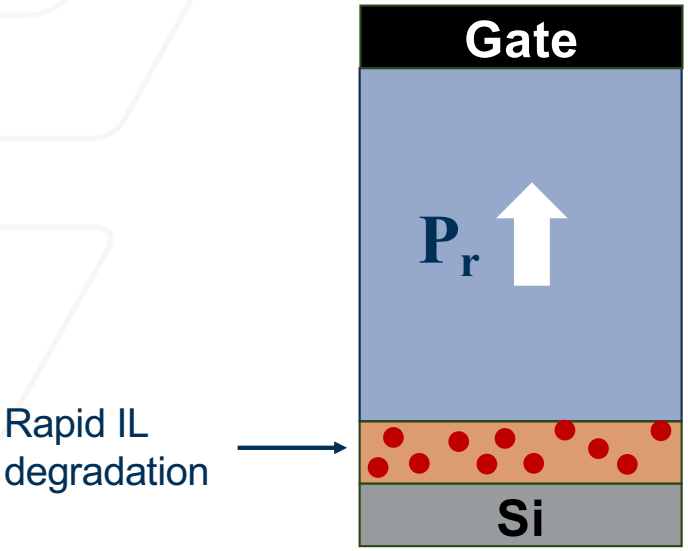
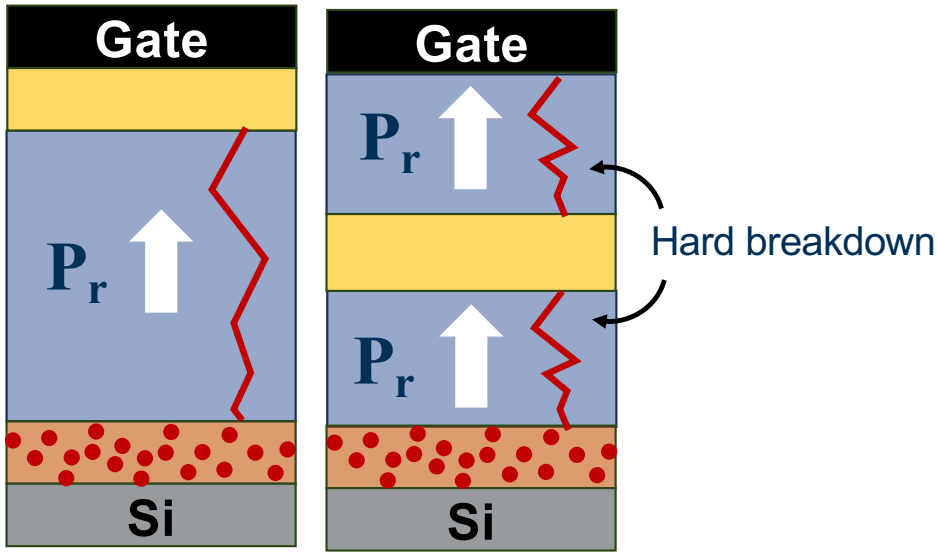
Write Endurance

Standard FEFETs



- Small MW
- V_{write} / V_{BD} lower than 1
- IL degradation dominates
- MW closure
- Minimal FE degradation

Engineered FEFETs



- Large MW
- V_{write} / V_{BD} close to 1
- Rapid IL degradation
- Increased risk of hard breakdown

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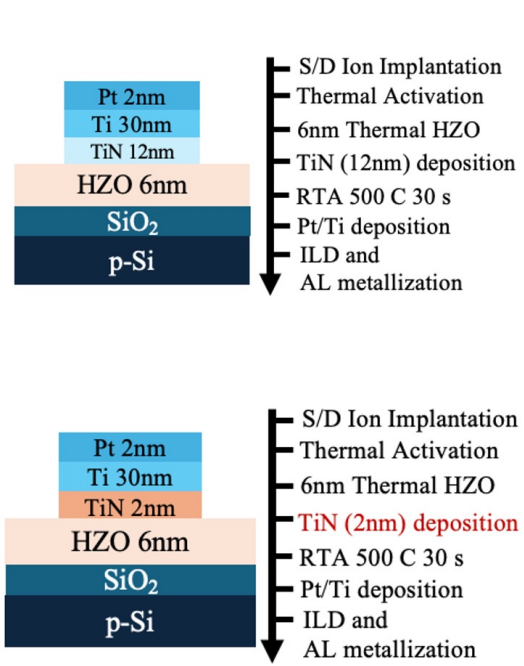
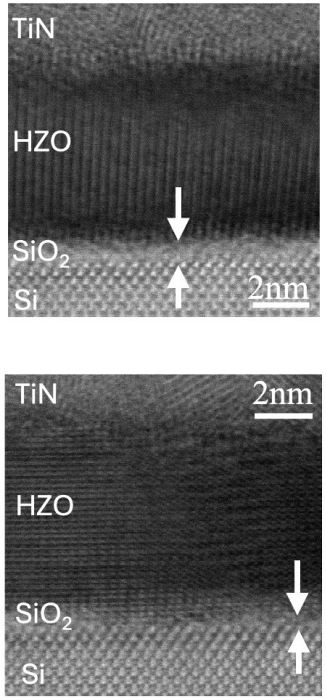
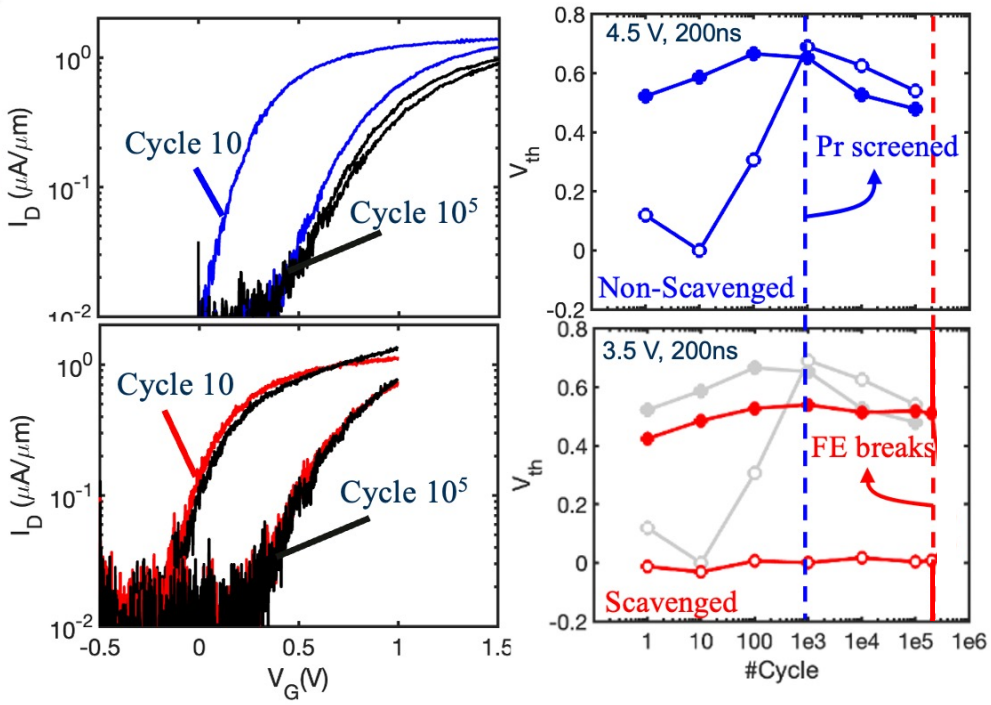
Write Endurance







71st International Electron Devices Meeting

Priyankka Ravikumar, Georgia Tech

"Experimental Demonstration of Robust High Temperature Operation with 10^4 Endurance and Stable V_{th} at 125 °C Enabled by IL Scavenging in Si Channel FeFETs"

5:15 PM | Session 23-7 Dec. 9, 2025

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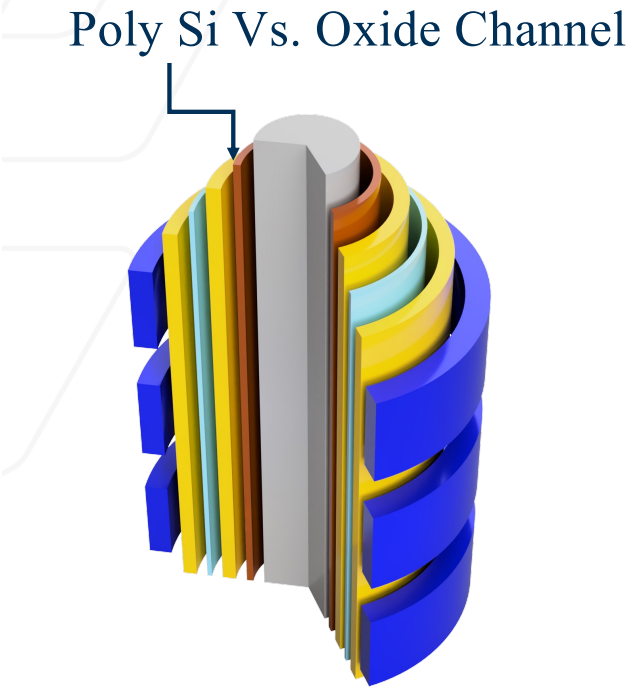
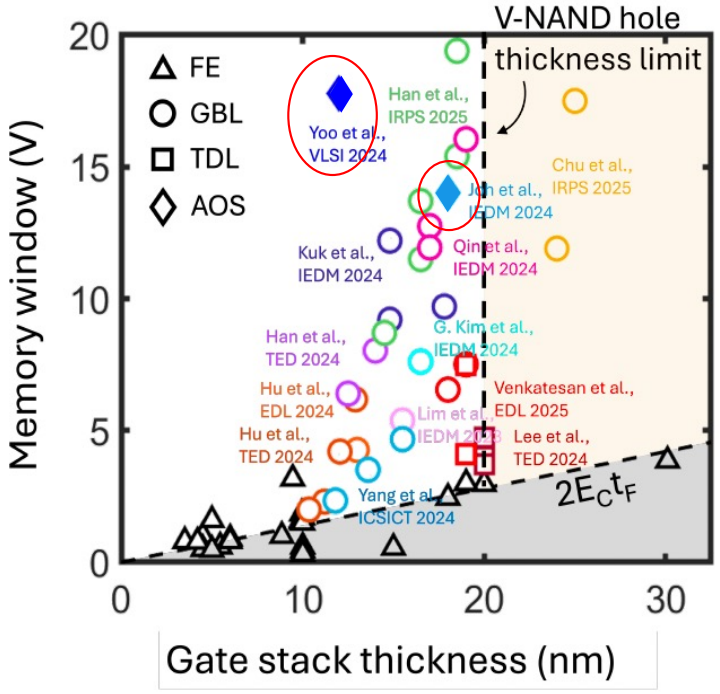
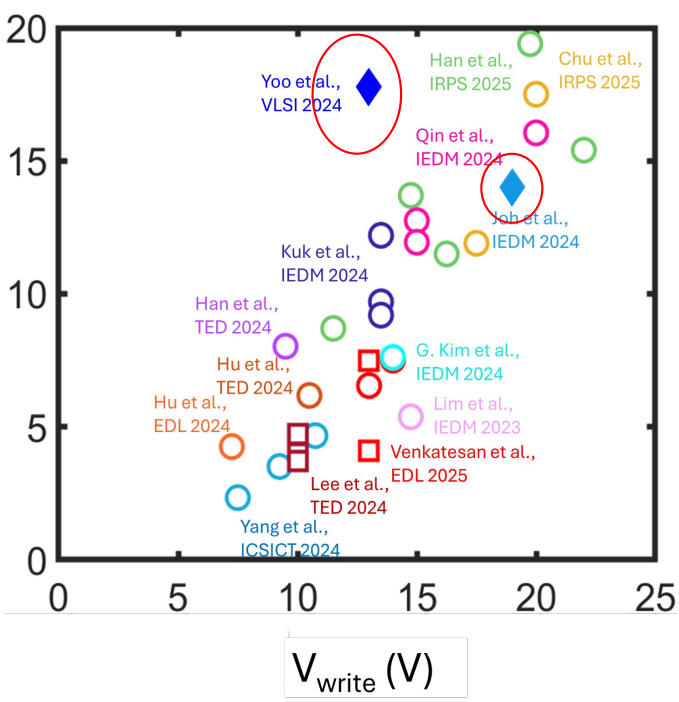
Amorphous oxide semiconductor channel



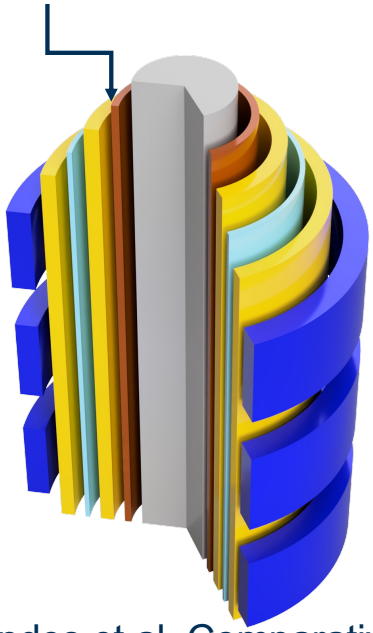




Venkatesan et al. MRS Bulletin 2025. https://doi.org/10.1557/s43577-025-00991-y

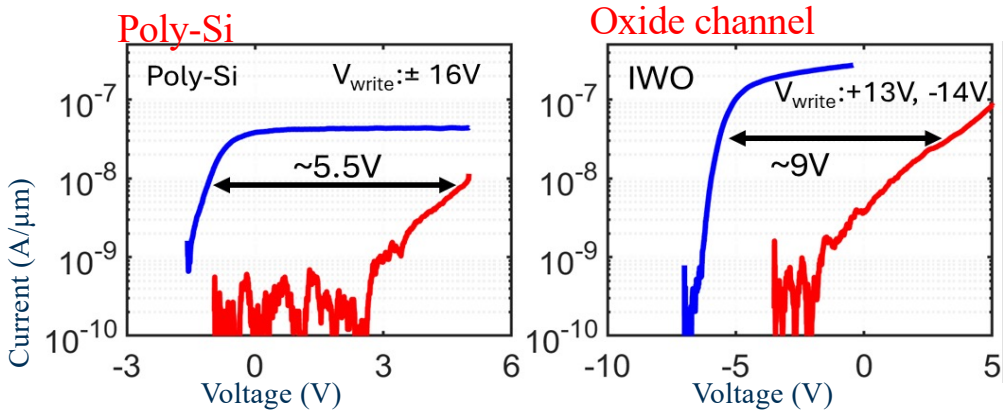
Amorphous oxide semiconductor channel

Poly Si Vs. Oxide Channel

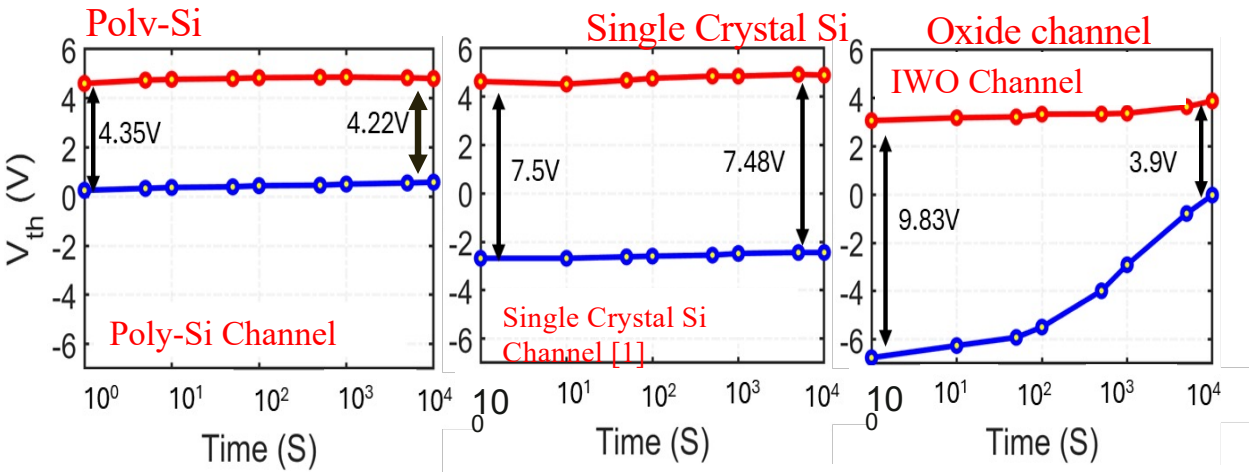


Fernandes et al. Comparative Study of Channel Materials for Ferroelectric NAND Applications. IEEE International Memory Workshop (IMW) 2025. 10.1109/IMW61990.2025.11026973

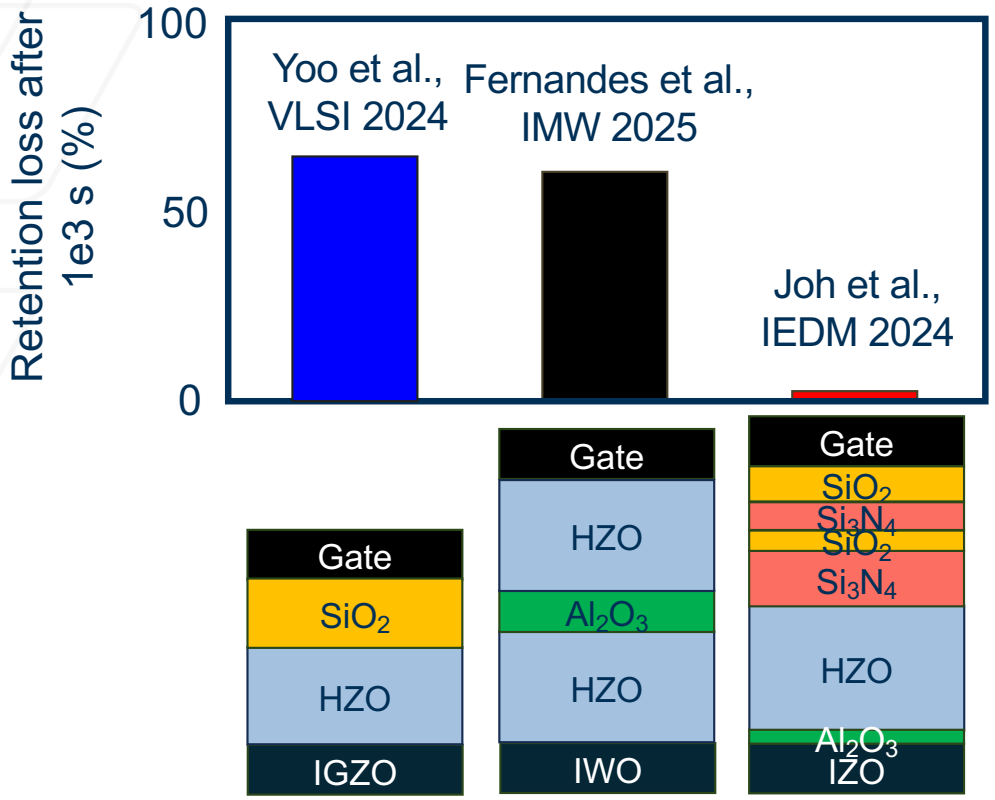
Write voltage and Memory window

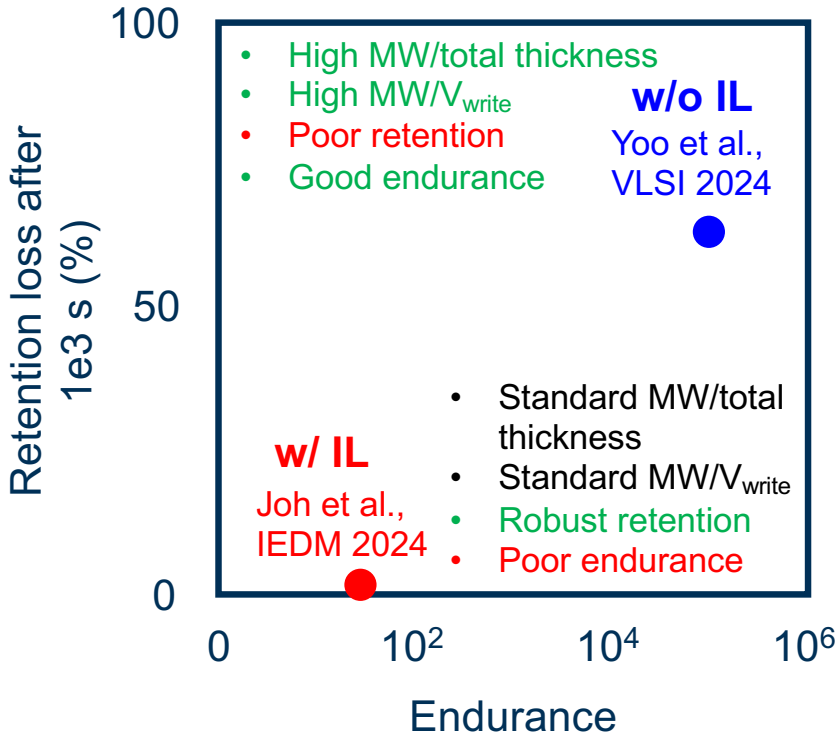


Retention characteristics



Retention – endurance trade off





Insertion of IL improves improves retention characteristics

But Introduction of IL leads to poor endurance

What about reliability of ferroelectric NAND?

Performance

Memory window

Device Reliability

Retention
✅ Demonstrated

Disturb
✅ Demonstrated

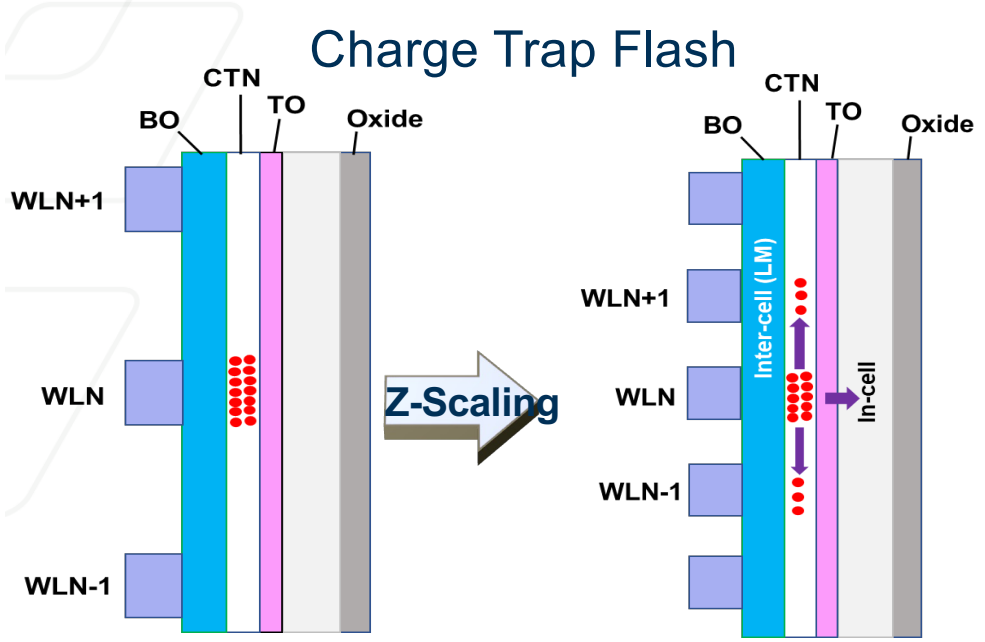
Write Endurance
⚠️ Under Evaluation

Array-level Reliability

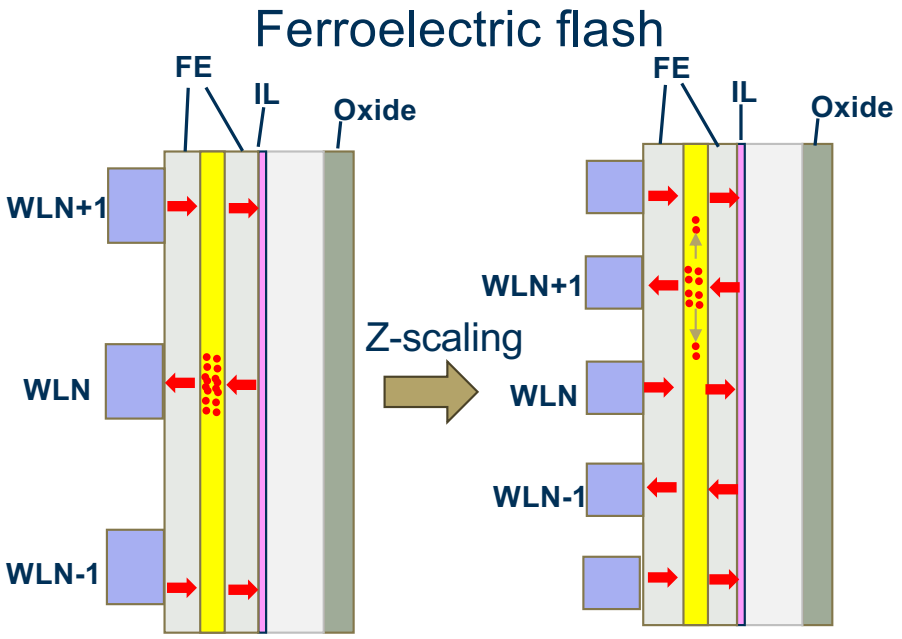
Lateral charge migration
⚠️ Under Evaluation

Device-device variation
⚠️ Under Evaluation

Lateral charge migration



Lateral charge migration prevents aggressive Z-scaling for 3D NAND.



The nature of trapped charges at the ferroelectric—interlayer interface will determine the scaling potential of ferroelectric 3D NAND technology.

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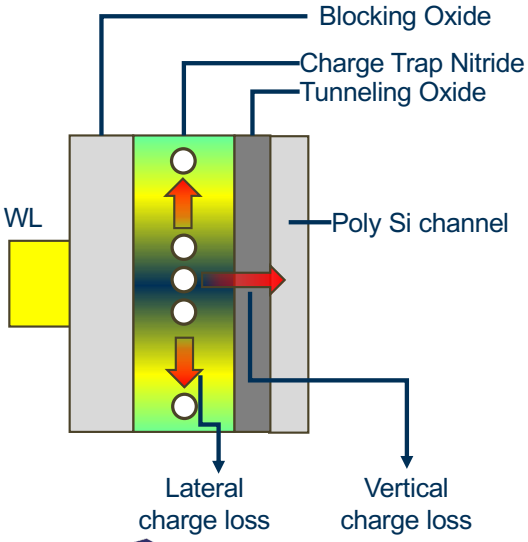
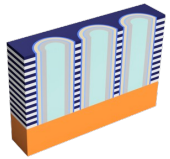
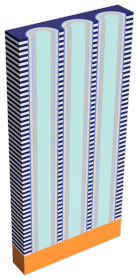
Ferroelectrics for Future NAND Storage Technology

Ferroelectric augmentation can provide enable NAND scaling in future generations

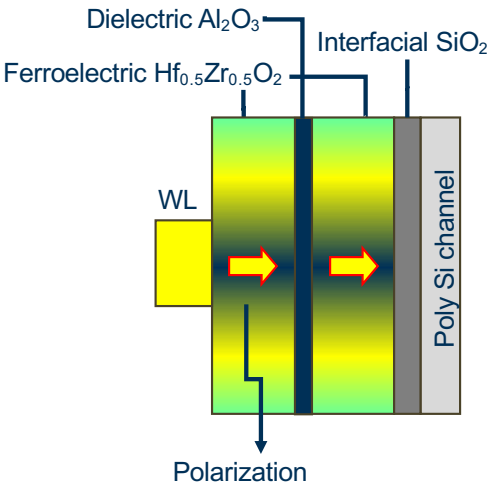


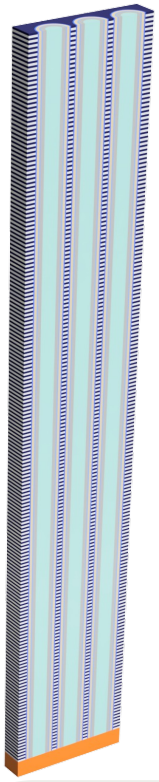


2014:
First 3D NAND
24 Layers, MLC



2025:
300+ Layers, QLC
5 Trillion+ transistors





2030 and
beyond

Georgia Tech

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