Ferroelectricity will lead the way for *21st century microelectronics*

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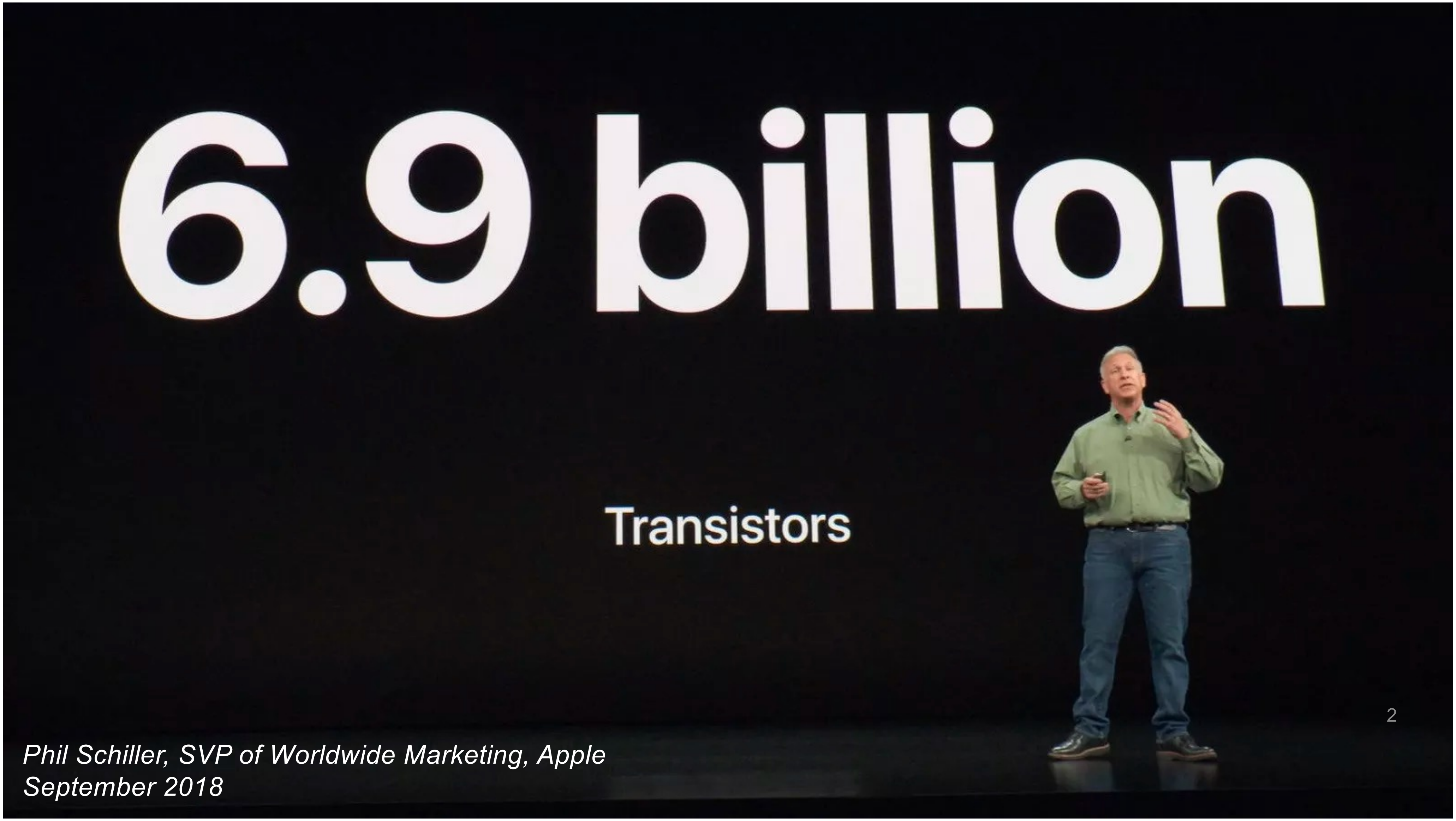
Ferroelectric Young Investigator Series, IEEE ISAF 2021



Phil Schiller, SVP of Worldwide Marketing, Apple
September 2018

Largest Chip Ever Built

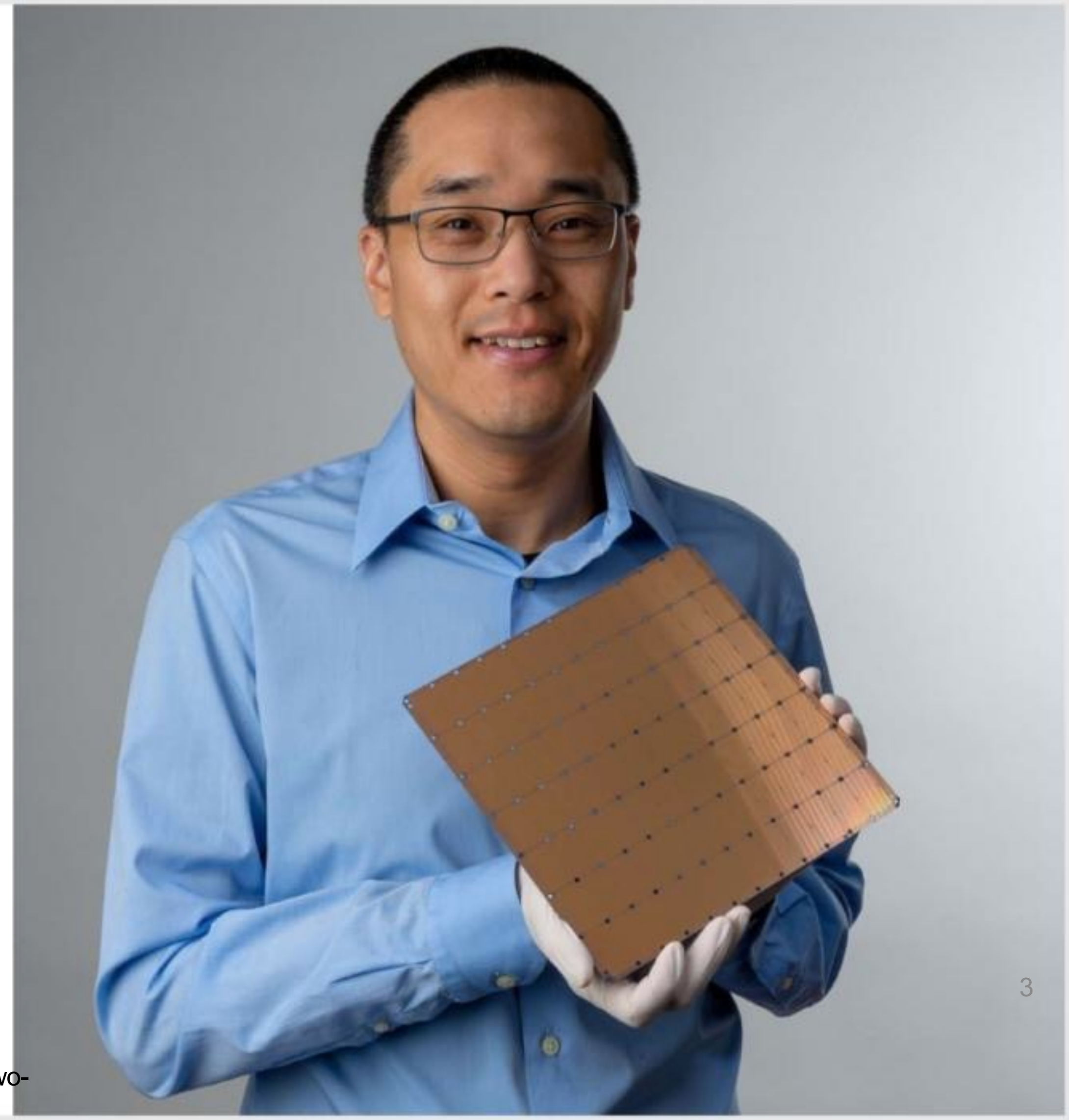
- 46,225 mm^2 silicon
- 1.2 trillion transistors
- 400,000 AI optimized cores
- 18 Gigabytes of On-chip Memory
- 9 PByte/s memory bandwidth
- 100 Pbit/s fabric bandwidth
- TSMC 16nm process

Wafer-scale integration
For massively parallel supercomputers

Year 2020

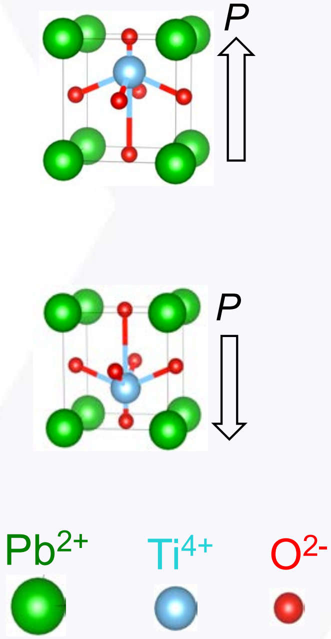
cerebras

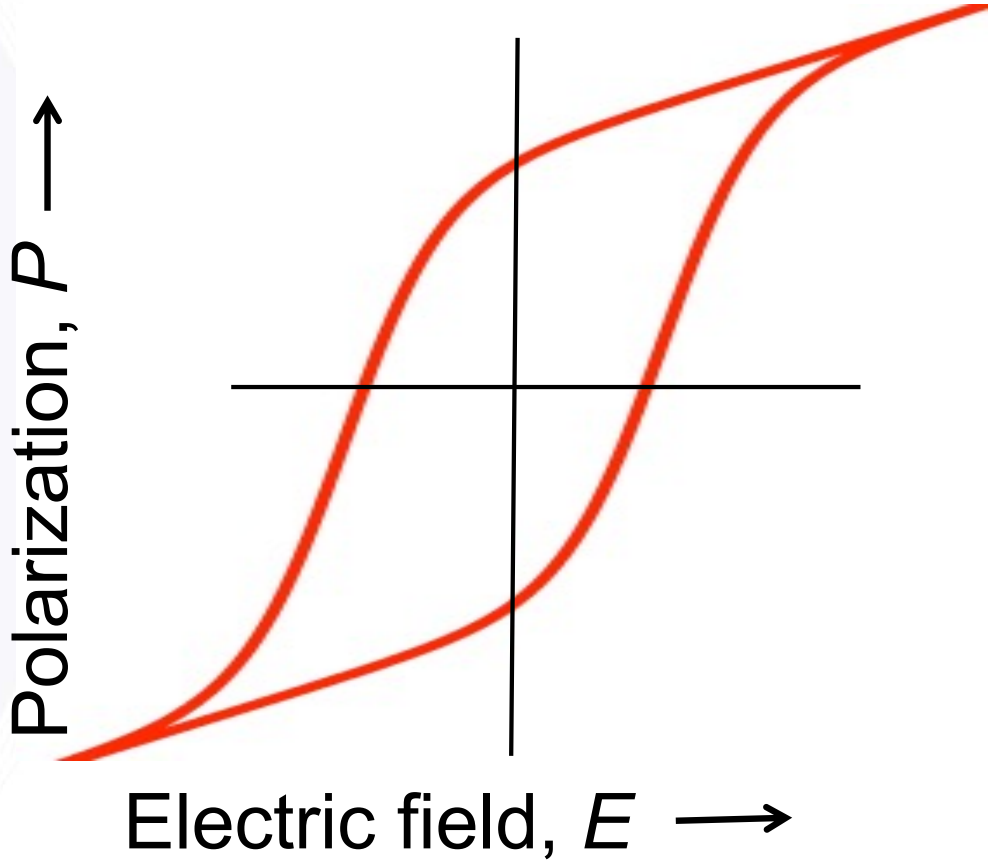
https://www.anandtech.com/show/16626/cerebras-unveils-wafer-scale-engine-two-wse2-26-trillion-transistors-100-yield

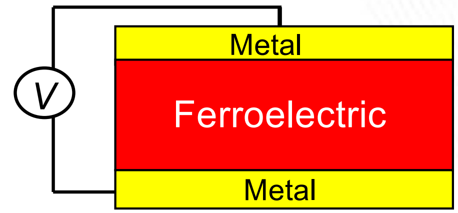


"Moore's Law is not dead, it's not slowing down, it's not even sick." -H.S.P. Wong, Taiwan Semiconductor Manufacturing Company (TSMC) and Stanford University Hot Chips 2020.

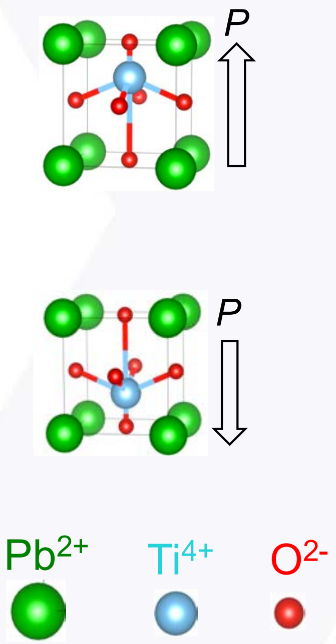
Ferroelectricity

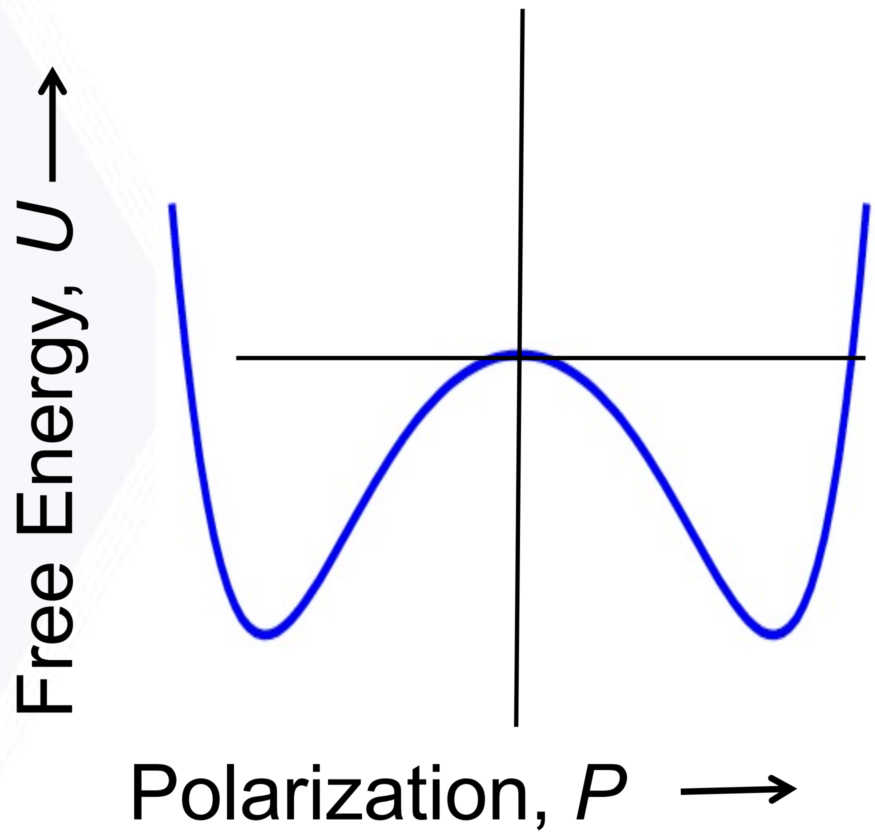


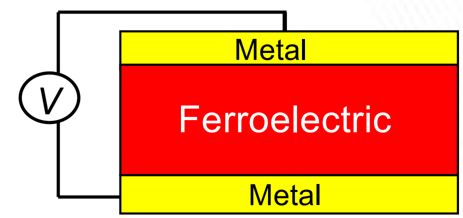




Ferroelectricity







Landau Theory of Ferroelectrics

Free energy of a ferroelectric

$$U = \alpha Q^2 + \beta Q^4 + \gamma Q^6; \alpha < 0$$

α, β, γ = Anisotropy Constants
Q = Charge

Landau & Khalatnikov. Dokl. Akad. Nauk 96, 85 469472 (1954).

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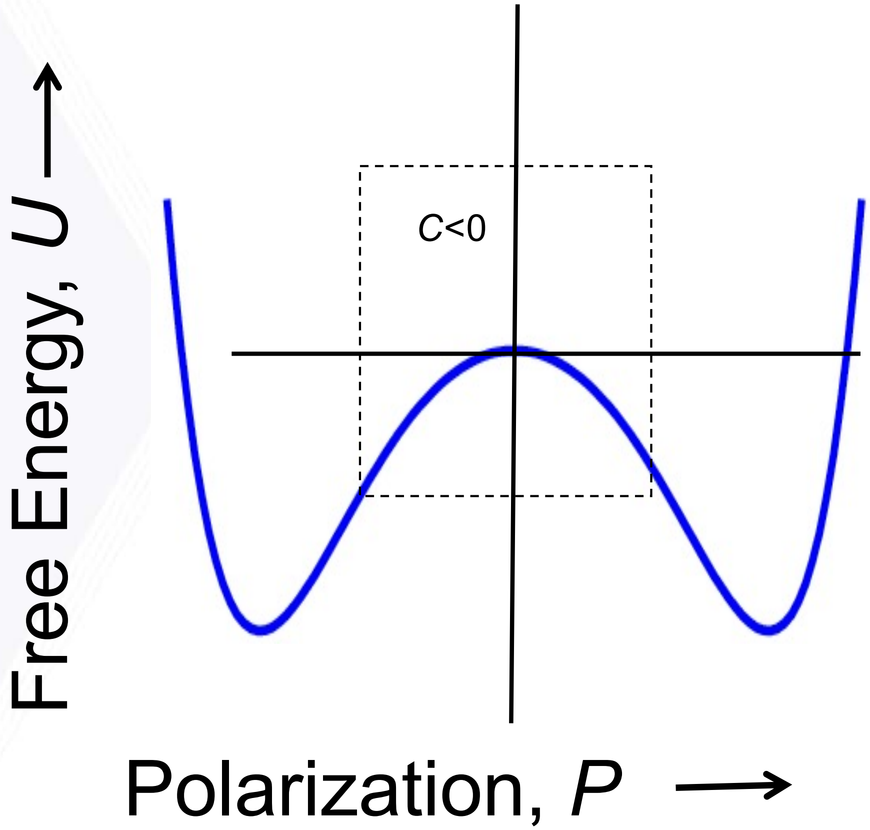
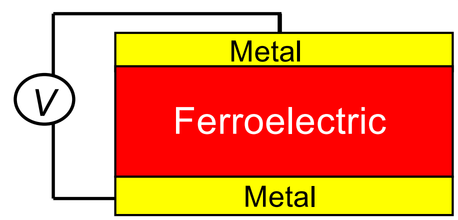
Ferroelectricity and negative capacitance



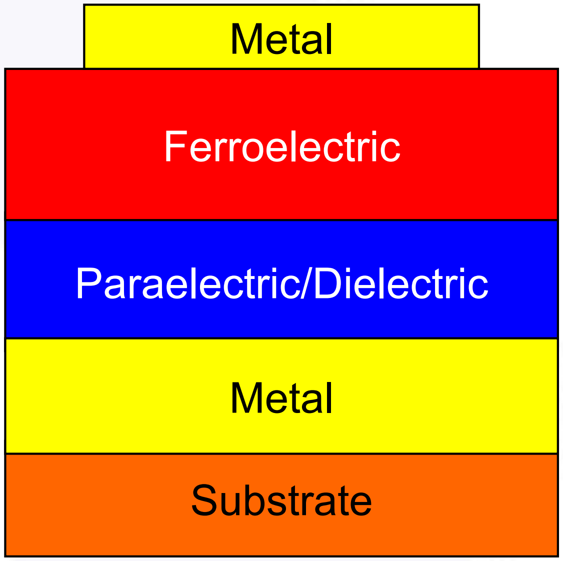


Capacitance $C = \frac{dQ}{dV}$

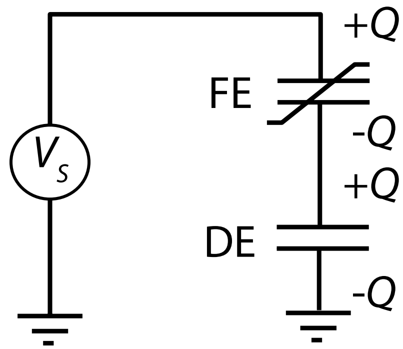
Stored Energy $U = \frac{Q^2}{2C}$

$$C = \left[\frac{d^2U}{dQ^2}\right]^{-1}$$

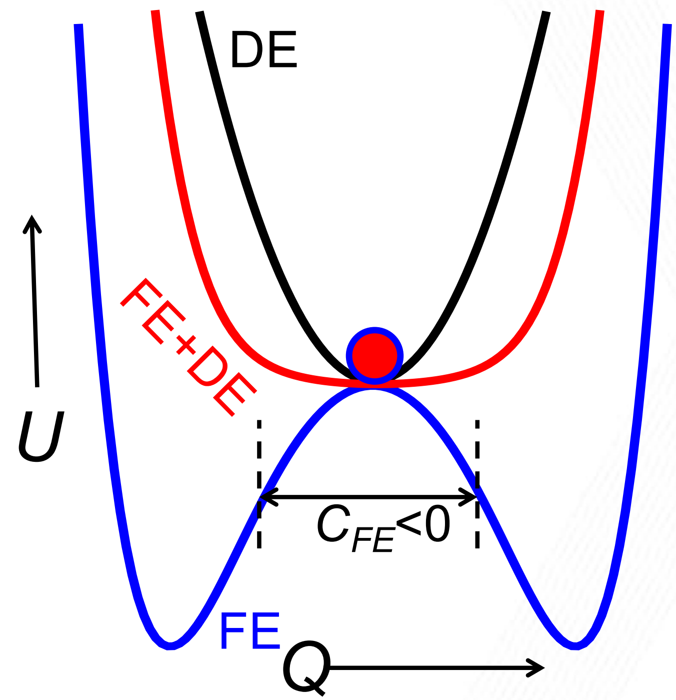
Ferroelectric Negative Capacitance



Ferroelectric-paraelectric Series Combination



Energy Landscapes

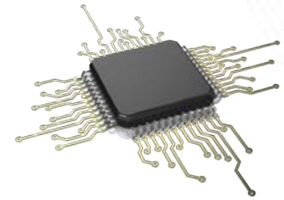


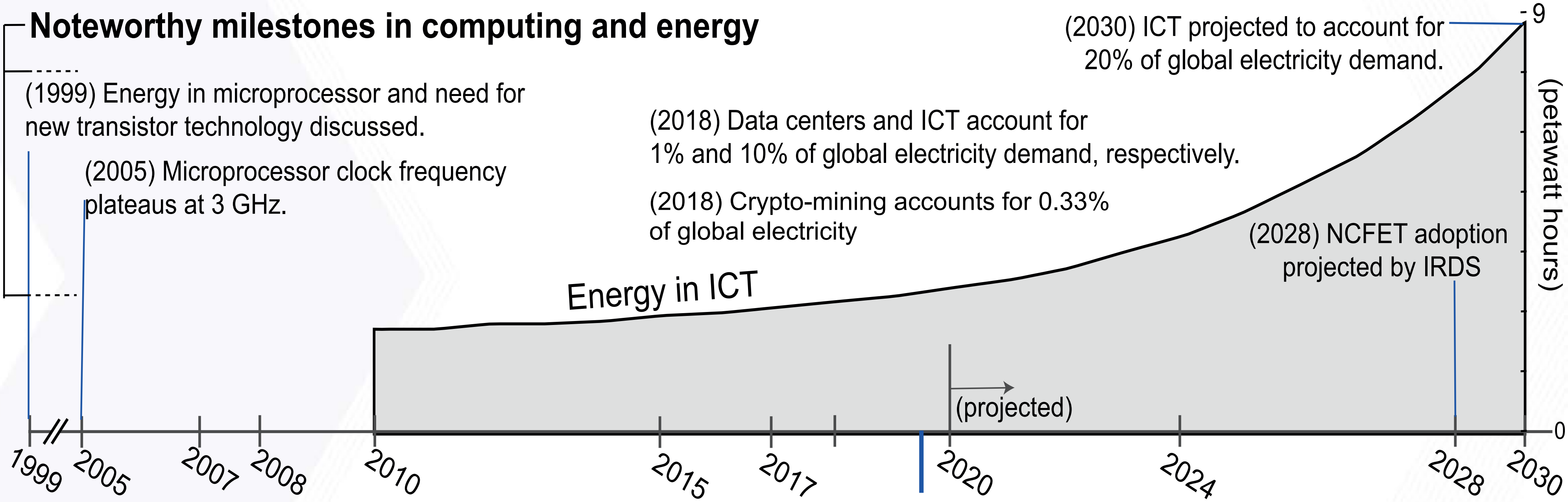
Equivalent Capacitance $$C_{FE+DE} = \left[\frac{1}{C_{FE}} + \frac{1}{C_{DE}}\right]^{-1}$$

$C_{FE+DE} > C_{DE}$ If $C_{FE} < 0$

Enhancement of capacitance in a FE-DE Series combination!

Energy in Electronics





Jones. Inside Information Factories, Nature 561, 163 (2018)

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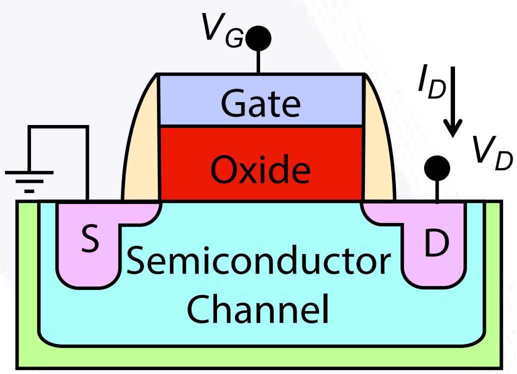
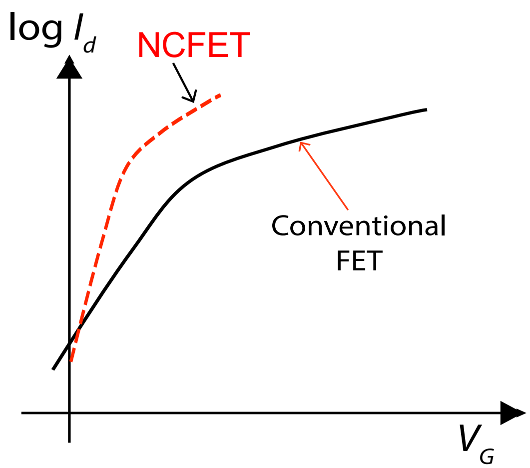
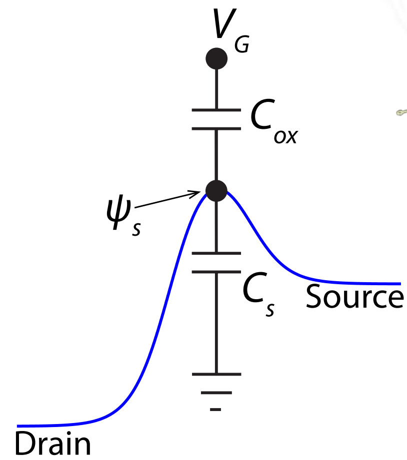
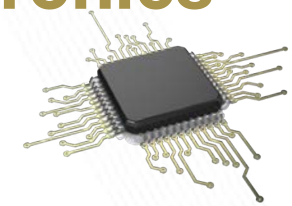
Negative capacitance and energy efficient electronics









Body Factor $m = \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_s}{C_{ox}}$ $\quad m = 1 + \frac{C_s}{C_{ox}} < 1$ if C_{ox} is negative

Boltzmann distribution dictates that

semiconductor charge, $Q \propto e^{\frac{q\psi_s}{k_B T}}$

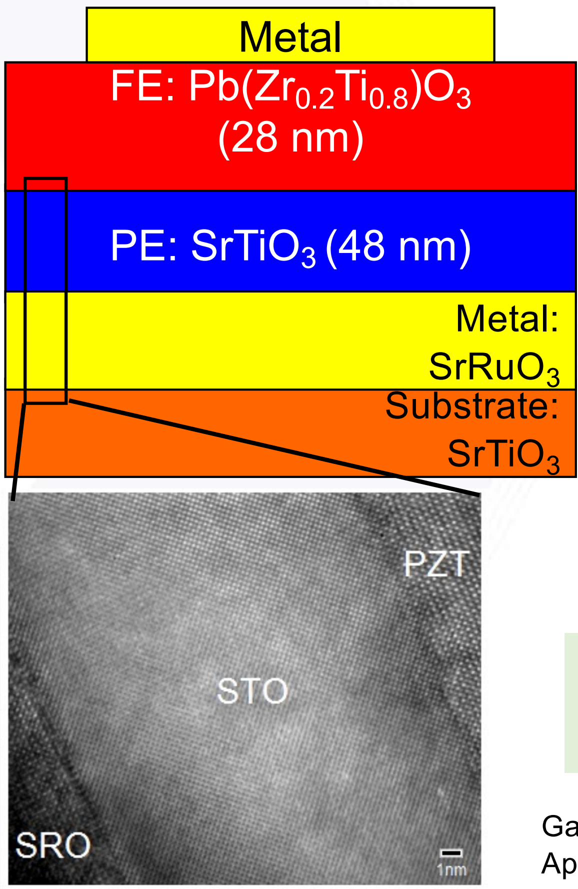
Subthreshold Swing

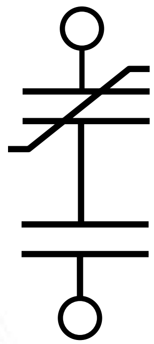
$$S = \frac{\partial V_G}{\partial(\log_{10} I_D)} = \underbrace{\frac{\partial V_G}{\partial \psi_s}}_{\equiv \mathrm{m}} \frac{\partial \psi_s}{\partial(\log_{10} I_D)} = m \times 60 \text{ mV/decade}$$

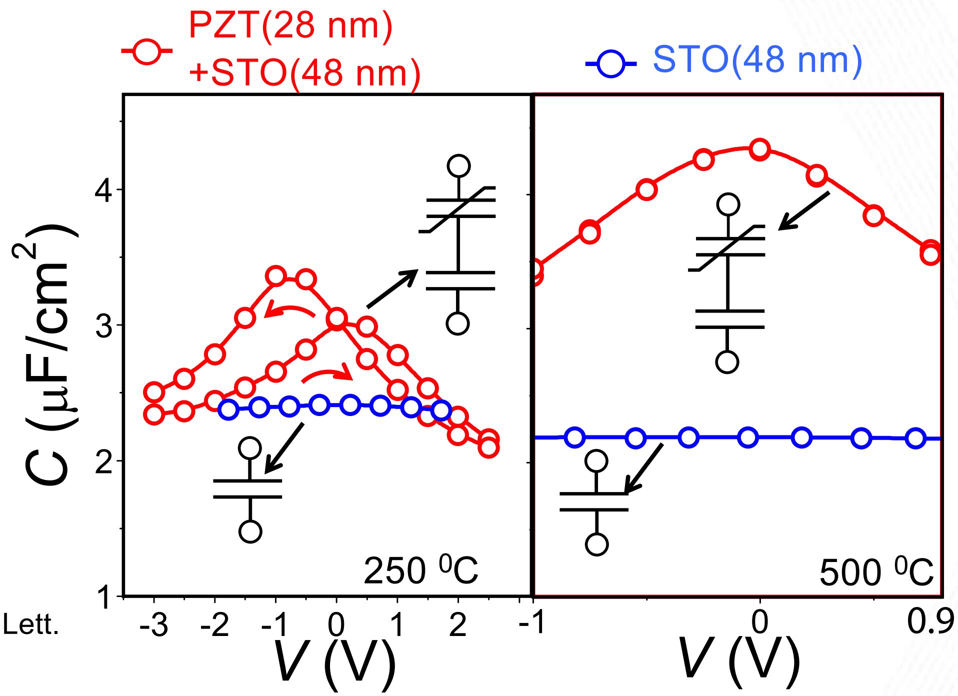
Capacitance enhancement beyond the tradition limit can allow for the reduction of the power supply voltage and hence the energy dissipation in transistors.

Salahuddin *et al*. Nano Lett. 8, 405 (2008).

Demonstration of negative capacitance







Khan *et al.* Appl. Phys. Lett. 100, 113501 (2011).

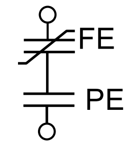
Capacitance Enhancement in a FE-PE heterostructure was experimentally observed!

Gao et al. Nano Lett. 14, 5814 (2014).
Appleby et al. Nano Lett. 14. 3864 (2014).

Zubko et al. Nature 534. 524 (2016).
Das et al. Nature Mater. 20, 194 (2021).

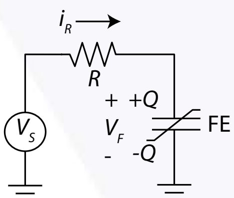
Recent progress in negative capacitance

Techniques



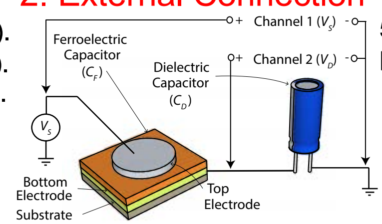
Positive Cap. + Neg. Cap.

1. Resistor + Neg. Cap.



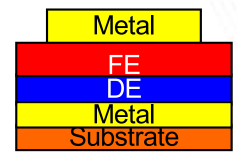
1. Khan *et al.* Nature Mater. 14, 182 (2015).
2. Hoffmann *et al.* Adv. Func. Mater. 26, 8643 (2016).
3. Hoffmann *et al*. J. Appl. Phys. 123, 184101 (2018).
4. Ku *et al.* IEEE J. Electron Dev. Soc. 5, 232 (2018).

2. External Connection

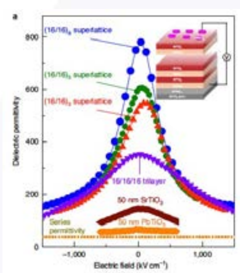


5. Khan *et al.* Appl. Phys. Lett. 111, 253501 (2018).

3. Integrated heterostructure

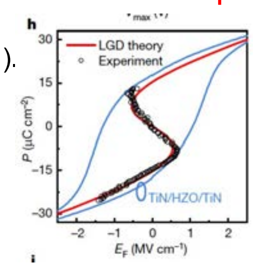


4. Multifrequency Capacitance



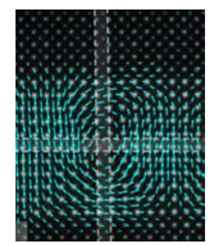
6. Khan *et al.* Appl. Phys. Lett. 100, 113501 (2011).
7. Gao *et al.* Nano Lett. 14, 5814 (2014).
8. Appleby *et al*. Nano Lett. 14. 3864 (2014).
9. Zubko *et al*. Nature 534. 524 (2016).
*. Yadav *et al.* Nature 565, 468 (2019).
*. Das *et al*. Nature Mater. 20, 194 (2021).

5. Pulsed Capacitance



10. Kim *et al.* Nano Lett. 16, 4375 (2016).
11. Hoffmann *et al.* Nature 565, 464 (2019).
12. Kim *et al.* Adv. Func. Mater. 29, 1808228 (2019).

6. Microstructural characterization



13. Yadav *et al.* Nature 565, 468 (2019).
14. Das *et al.* Nature Mater. 20, 194 (2021).

[Not a comprehensive list]

Review articles

15. Íñiguez *et al*. “Ferroelectric negative capacitance.” *Nature Rev. Mater.* 4, 243 (2019).
16. Hoffmann *et al.* "What’s next for negative capacitance electronics?." *Nature Electron.* 3, 504 (2020).
17. Hoffmann *et al.* ”Why do ferroelectrics exhibit negative capacitance ?." *Materials* 12, 3743 (2019).
18. Wong, *et al.* “Negative capacitance transistors." *Proceedings of the IEEE* 107 49 (2018).
19. Alam, *et al.* "A critical review of recent progress on negative capacitance field-effect transistors." *Appl. Phys. Lett.* 114, 090401 (2019).

Negative capacitance and controversies

Nature Nanotech. 3, 77 (2008)

NEWS & VIEWS

NANOELECTRONICS

Negative capacitance to the rescue?

Victor V. Zhirnov* and Ralph K. Cavin
are at the Semiconductor Research Corporation, Research Triangle Park, North Carolina 27709, USA.
*e-mail: Victor.Zhirnov@src.org

At this point the proposed negative capacitance mechanism has not been observed in experiments, and it remains

After

Khan *et al. Nature Mater*. 14, 182 (2015).

Published: 23 January 2015

Ferroelectrics

Negative capacitance detected

Gustau Catalan, David Jiménez & Alexei Gruverman

Nature Materials **14**, 137–139(2015) | Cite this article

After

Yadav *et al. Nature* 565, 468 (2019), and
Hoffmann *et al. Nature* 565, 464 (2019).

Research Highlight | Published: 15 February 2019

FERROELECTRICS

Negative capacitance found

Stuart Thomas

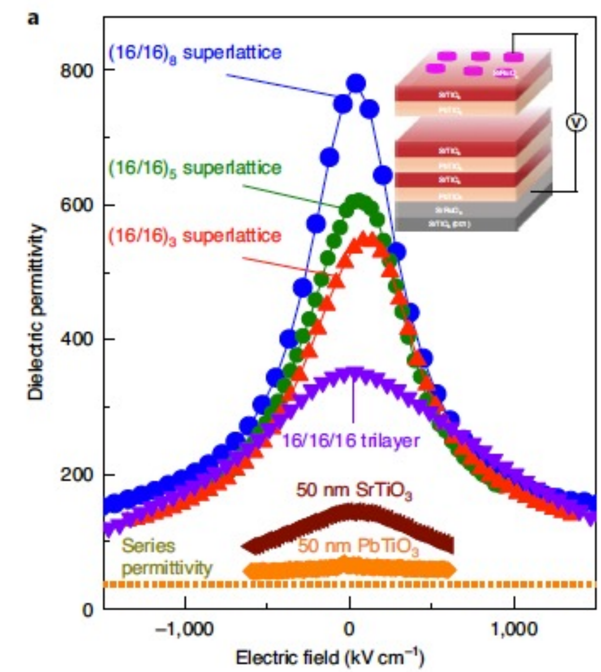
Nature Electronics **2**, 51(2019) | Cite this article

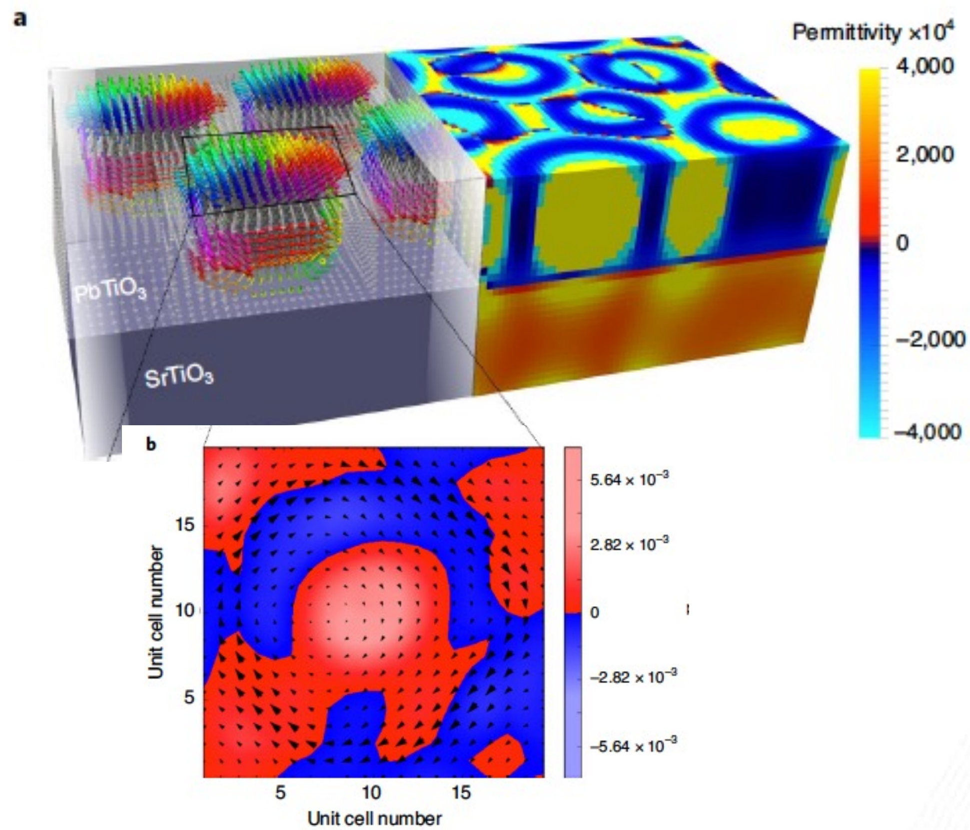
Controversies

Krowne *et al. Nano letters* 11, 988 (2011).
Saha *et al. Journal of Applied Physics* 123, 105102 (2018).
Liu *et al. IEEE Electron Device Letters* 41, 1492 (2020).
Liu *et al.* Proceedings of *2018 IEEE International Electron Devices Meeting (IEDM)*. pp. 31-2.
Kittl *et al. Applied Physics Letters* 113, 042904 (2018).

`Local' negative capacitance and `unusual' polar textures

Das *et al*. *Nature Mater*. 20, 194 (2021).





Also
Yadav et al. *Nature* 565, 468 (2019).

Negative capacitance is a spatially localized phenomenon, which macroscopically manifests as capacitance enhancement.

Negative capacitance through the years

Collective Phenomena
1976, Vol. 2, pp. 167–170

CAN CAPACITANCE BE NEGATIVE?

ROLF LANDAUER

IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598

(*Received July 25, 1975*)

Prigogine and Glansdorff in their analysis of the stability of the steady state have invoked the fact that compressibilities must be positive. The ferroelectric analog of that proposition is analyzed with the probable conclusion that negative differential dielectric constants can exist in the stable steady state.

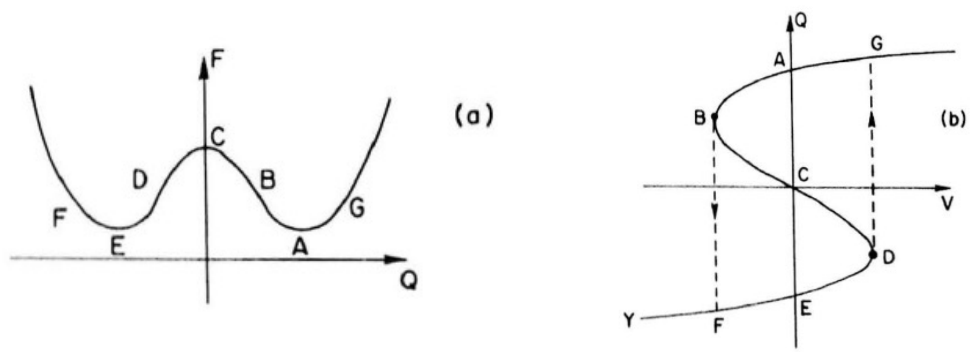
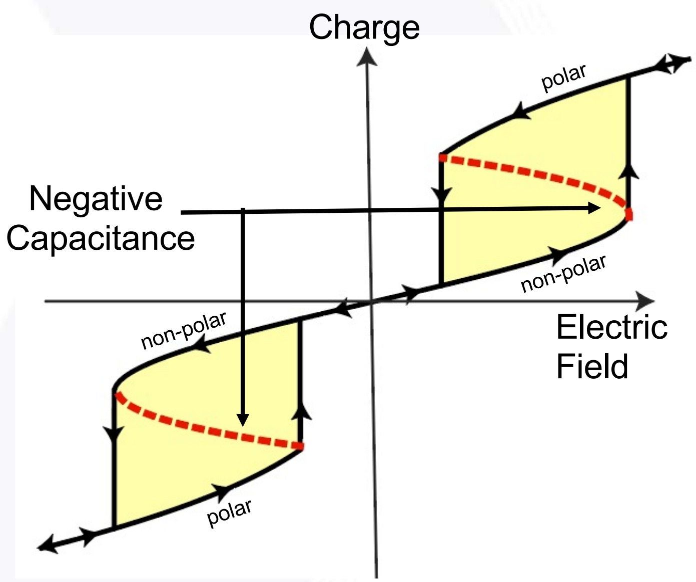


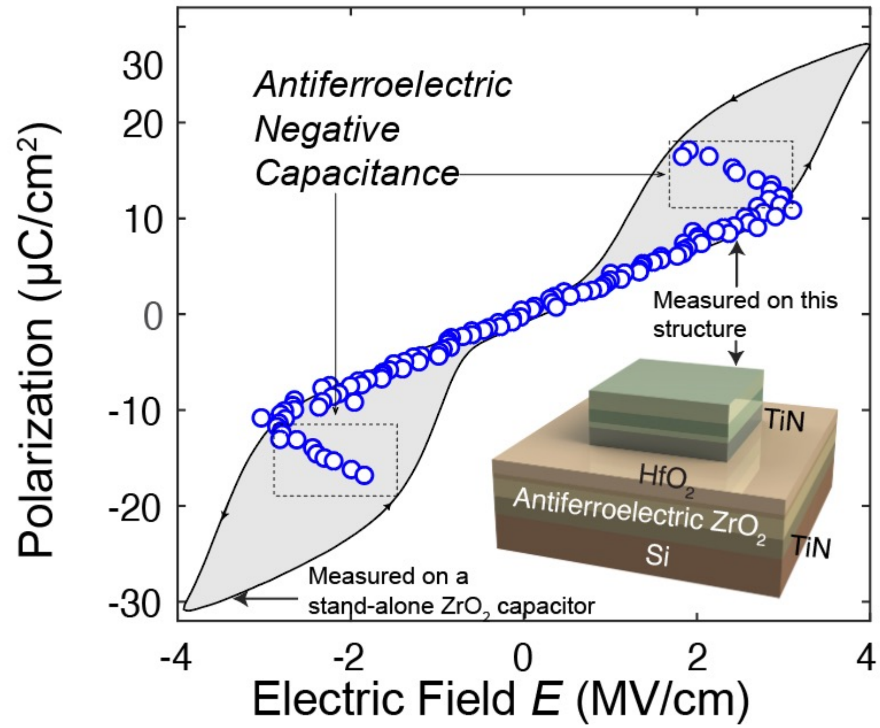
FIGURE 1 (a) Free energy vs. capacitive charge for a ferroelectric. (b) The associated charge vs. voltage characteristic.

Also
Merz. *Phys. Rev. 91*, 513 (1953).
Janovec. *Czech. fiz. zurnal*, 1959.

Negative capacitance beyond ferroelectrics

<u>Antiferroelectricity:</u> Electric field induced **1st order phase transition** from a **non-polar** ground state into a **polar** phase.





Hoffmann*, Wang*, Tasneem* *et al.* Antiferroelectric negative capacitance from a structural phase transition in zirconia. (Under review.) https://arxiv.org/abs/2104.10811

Negative capacitance beyond transistor applications

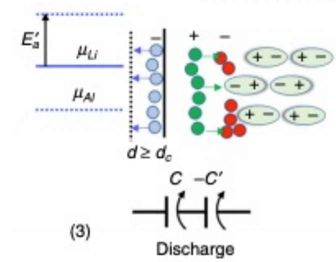
Energy storage applications

Braga *et al*. *Appl. Phys. Rev*. 7, 011406 (2020)

Performance of a ferroelectric glass electrolyte in a self-charging electrochemical cell with negative capacitance and resistance

Cite as: Appl. Phys. Rev. 7, 011406 (2020); doi: 10.1063/1.5132841
Submitted: 20 October 2019 · Accepted: 9 January 2020 ·
Published Online: 25 February 2020

M. H. Braga,[1,a)] J. E. Oliveira,[1] A. J. Murchison,[2] and J. B. Goodenough[2]

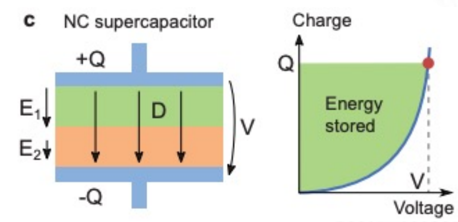


Hoffmann *et al*. *Adv. Energy Mater*. 9, 1901154 (2019)

FULL PAPER
ADVANCED ENERGY MATERIALS
www.advenergymat.de

Negative Capacitance for Electrostatic Supercapacitors

Michael Hoffmann, Franz Paul Gustav Fengler, Benjamin Max, Uwe Schroeder, Stefan Slesazeck, and Thomas Mikolajick*



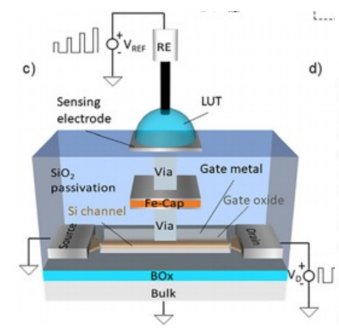
Sensing applications

Bellando *et al*. *Appl. Phys. Lett*. 116, 173503 (2020)

Subthermionic negative capacitance ion sensitive field-effect transistor

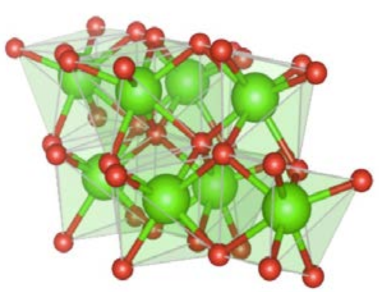
Cite as: Appl. Phys. Lett. 116, 173503 (2020); doi: 10.1063/5.0005411
Submitted: 20 February 2020 · Accepted: 15 April 2020 ·
Published Online: 28 April 2020

Francesco Bellando,[1,a)] Chetan K. Dabhi,[2] Ali Saeidi,[1] Carlotta Gastaldi,[1] Yogesh S. Chauhan,[2] and Adrian M. Ionescu[1,a)]



Ferroelectric field-effect transistor

Ferroelectric Oxide



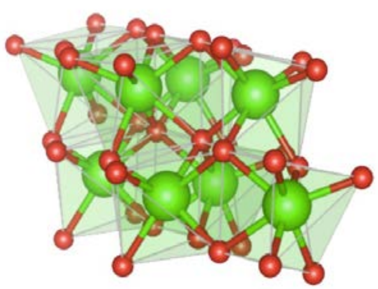
Properties of Ferroelectric oxides

- Non-volatility and hysteresis
- Plasticity, Meta-plasticity and Anti-plasticity
- Negative dielectric permittivity/negative capacitance
- Stochasticity

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

Ferroelectric field-effect transistor

Ferroelectric Oxide



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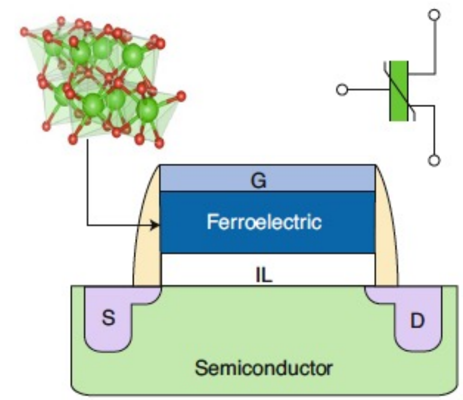
Ferroelectric field-effect transistor



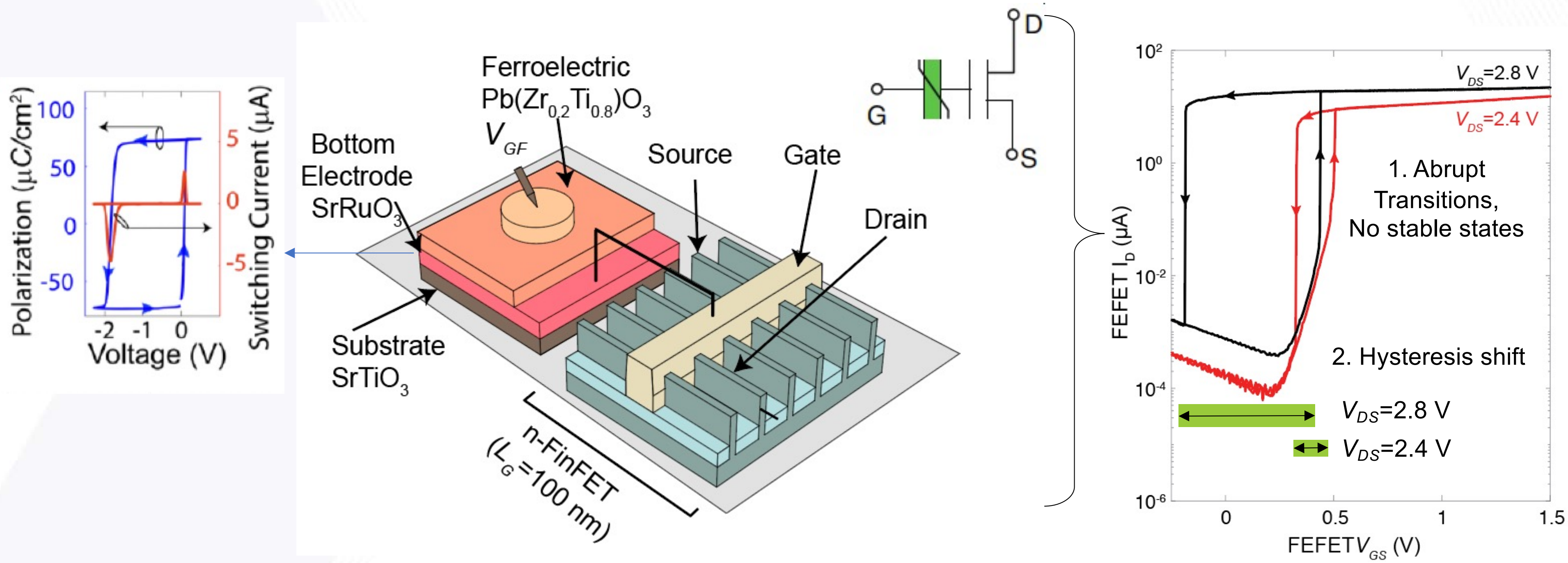
Properties enabled by a transistor structure

- Transistor physics
- Transconductance gain
- Circuit-level design

Ferroelectric FET is one of most versatile transistor technologies – ever conceived.

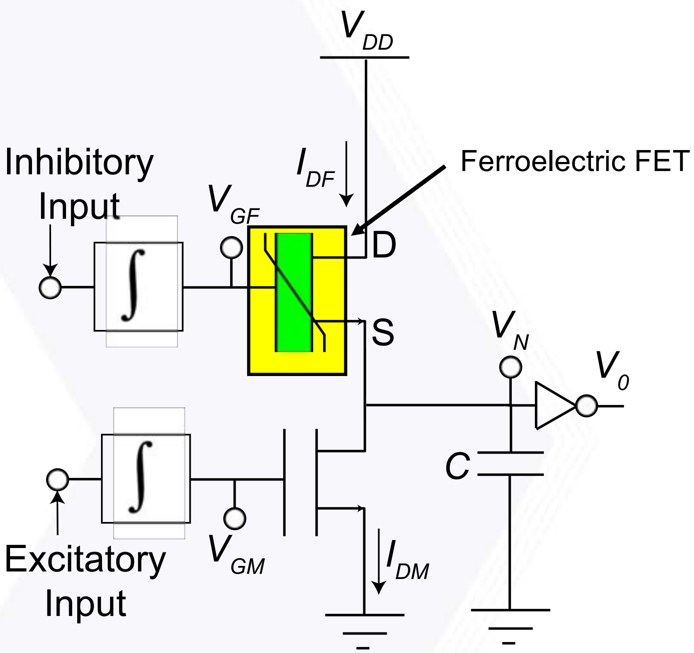
Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

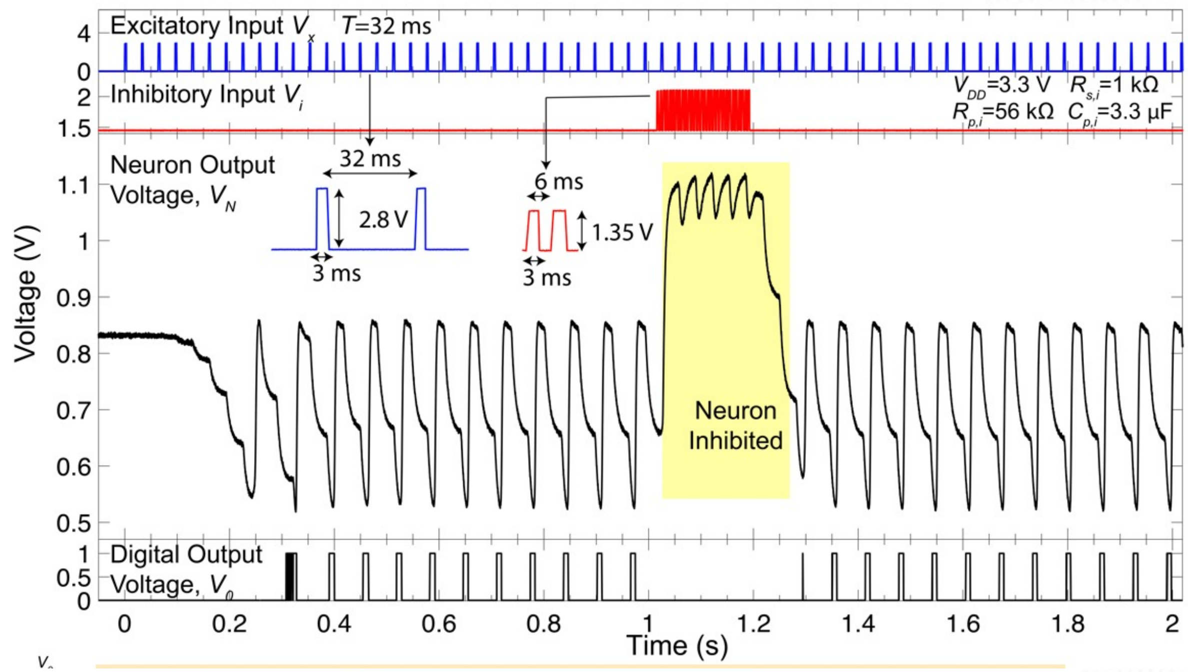
Ferroelectric Neuron with excitatory and inhibitory connection



Wang *et al.* Experimental demonstration of ferroelectric spiking neurons for unsupervised clustering. In *2018 IEEE International Electron Devices Meeting (IEDM)* (pp. 13-3). IEEE.

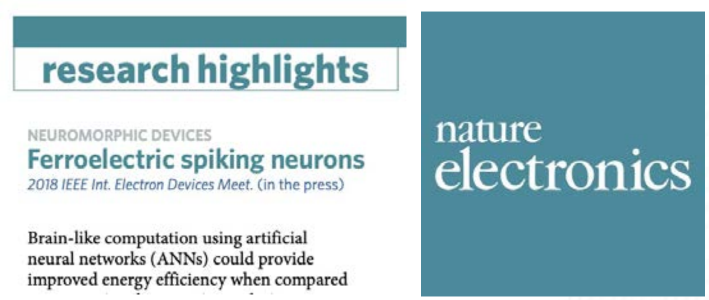
Ferroelectric Neuron with excitatory and inhibitory connection





The first demonstration of an artificial neuron with integrated inhibitory and excitatory input!

Wang *et al.* Experimental demonstration of ferroelectric spiking neurons for unsupervised clustering. In *2018 IEEE International Electron Devices Meeting (IEDM)* (pp. 13-3). IEEE.


research highlights

NEUROMORPHIC DEVICES

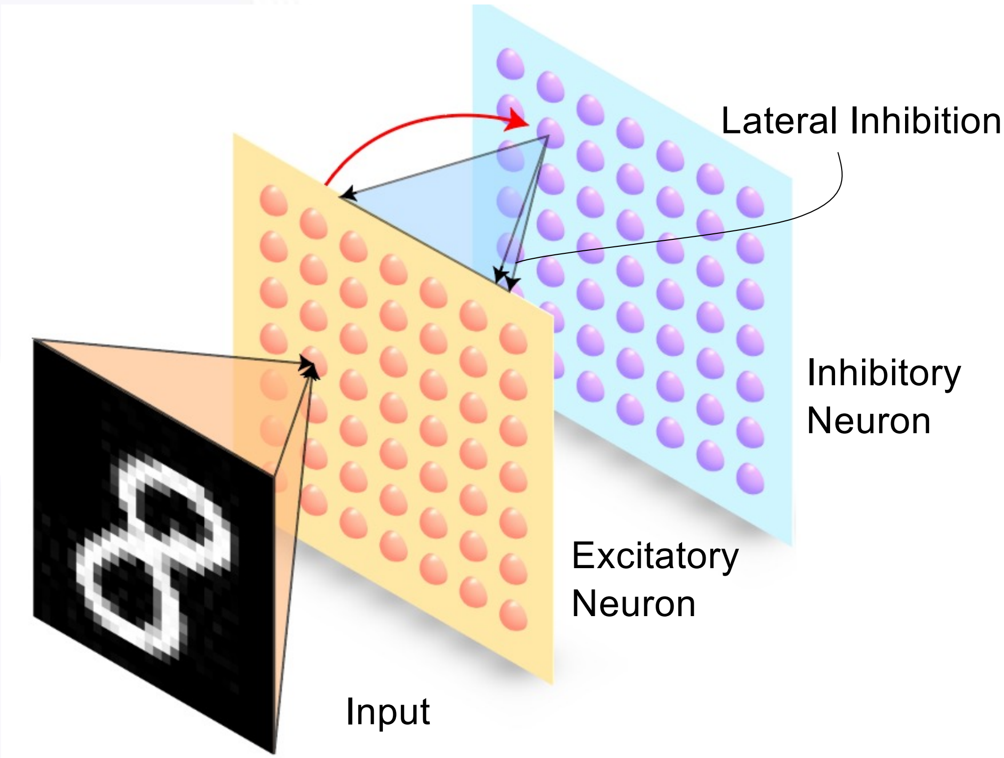
Ferroelectric spiking neurons

2018 IEEE Int. Electron Devices Meet. (in the press)

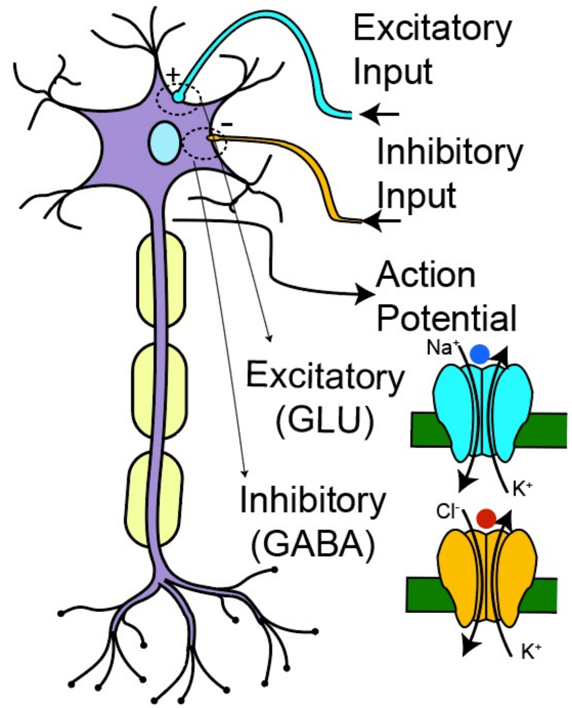
Brain-like computation using artificial neural networks (ANNs) could provide improved energy efficiency when compared

nature electronics

Spiking Neural Network: The Role of Inhibition



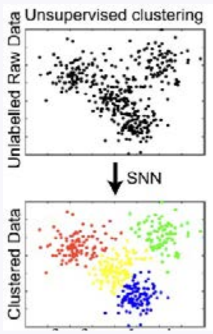
Deihl & Cook, Frontiers Comp. Neurosci. 9, 99 (2015)

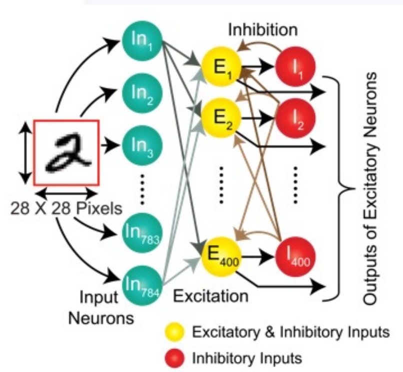


Biology: Inhibition required for regulation in activation of excitatory neurons; homeostasis.
Bio-inspired computing: High accuracy in unsupervised learning.

Ferroelectric SNNs for unsupervised clustering

Wang *et al.* Experimental demonstration of ferroelectric spiking neurons for unsupervised clustering. In *2018 IEEE International Electron Devices Meeting (IEDM)* (pp. 13-3). IEEE.



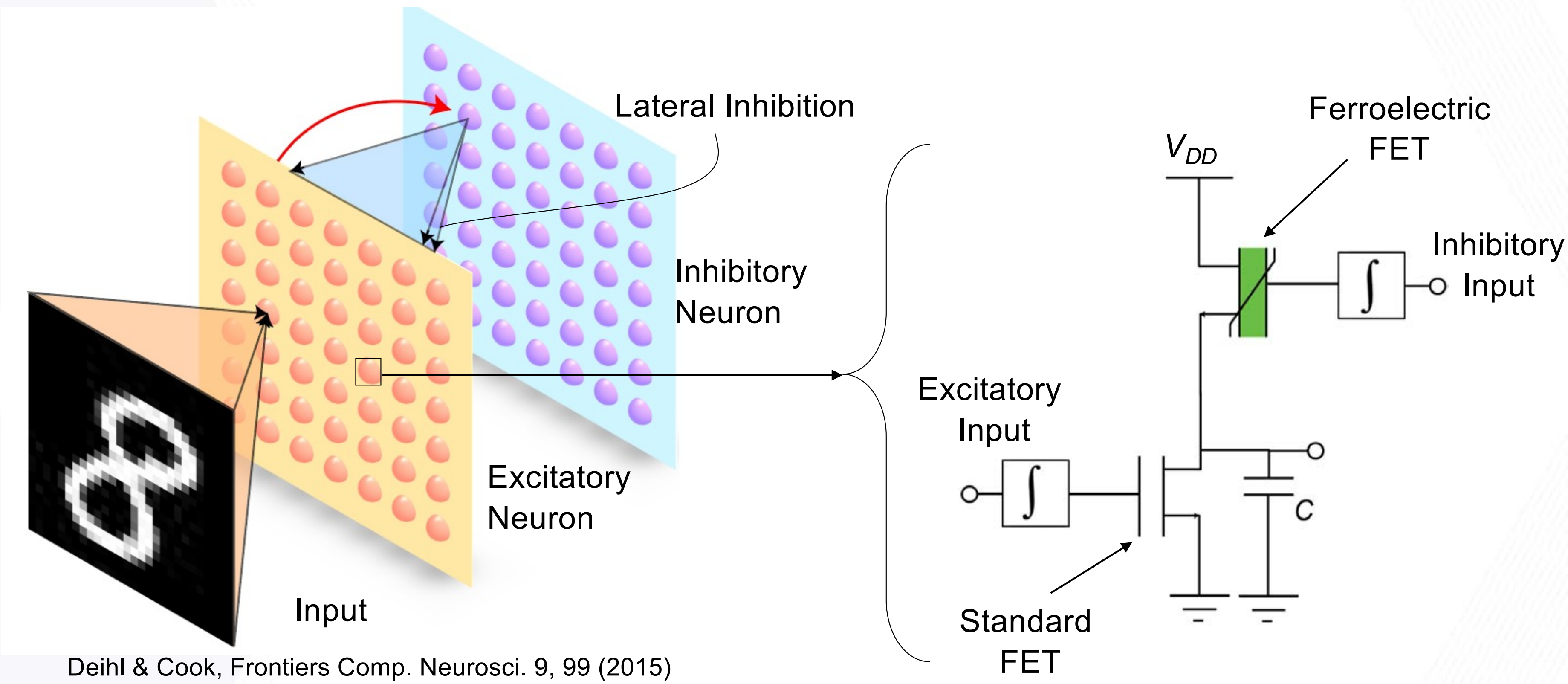


	Indiveri ISCAS 2003	Amravati ISSCC 2018	Jerry et al. VLSI 2017	Current work
Technology	CMOS Analog, Mixed Signal		Emerging Technology	
Neuron Type	LIF	Multiply-Accumulate	LIF	LIF
Network Type	Spiking	Non-spiking	Spiking	Spiking
Data Encoding Architecture	Spike Timing	Multi-level perceptron	Spiking Rate	Spike Timing
Input Type	Excitatory	Excitatory	Excitatory	Excit. & Inhib.
Device Count	15 T	64 T	1T - 1 VO_2	1T - 1 FEFET
Synapse Weight	Pos. & Neg.	Pos. & Neg.	Pos. & Neg.	Pos.
Training & Classification	Unsupervised	Reinforcement	Supervised	Unsupervised
Power	10 nW	125 nW	Not reported	3.6 nW

Publications from other groups

Han, Joon-Kyu, *et al. IEEE Electron Device Letters* 41.2 (2019): 208-211.
Dutta, S., et al. *2019 Symposium on VLSI Technology*. IEEE, 2019.
Chen, C., et al. *2019 Symposium on VLSI Technology*. IEEE, 2019.
Luo, Jin, *et al. 2019 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2019.

Ferroelectric Neuron with excitatory and inhibitory connection



Deihl & Cook, Frontiers Comp. Neurosci. 9, 99 (2015)

Biology: Inhibition required for regulation in activation of excitatory neurons; homeostasis.
Bio-inspired computing: High accuracy in unsupervised learning.

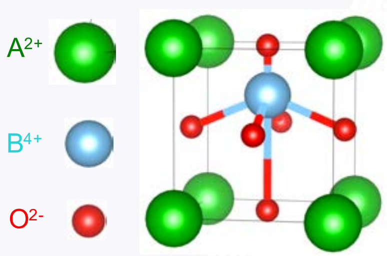
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for for code storage in microcontrollers.

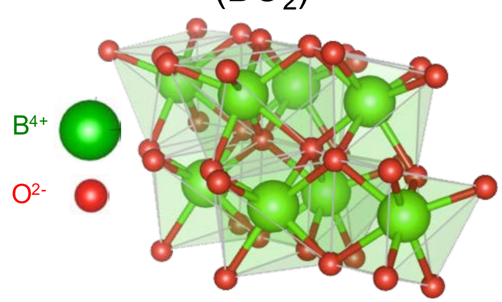
2. Controlled annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al. Appl. Phys. Lett*. 99, 112904 (2011)
- Boscke *et al. 2011 IEEE Int. Electron Devices Meeting.* p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al. Nano Lett.* 12, 4318 (2012)

Perovskite-structure ferroelectric oxide (ABO_3)



Fluorite-structure ferroelectric oxide (BO_2)



Why does ferroelectric technology stand out?

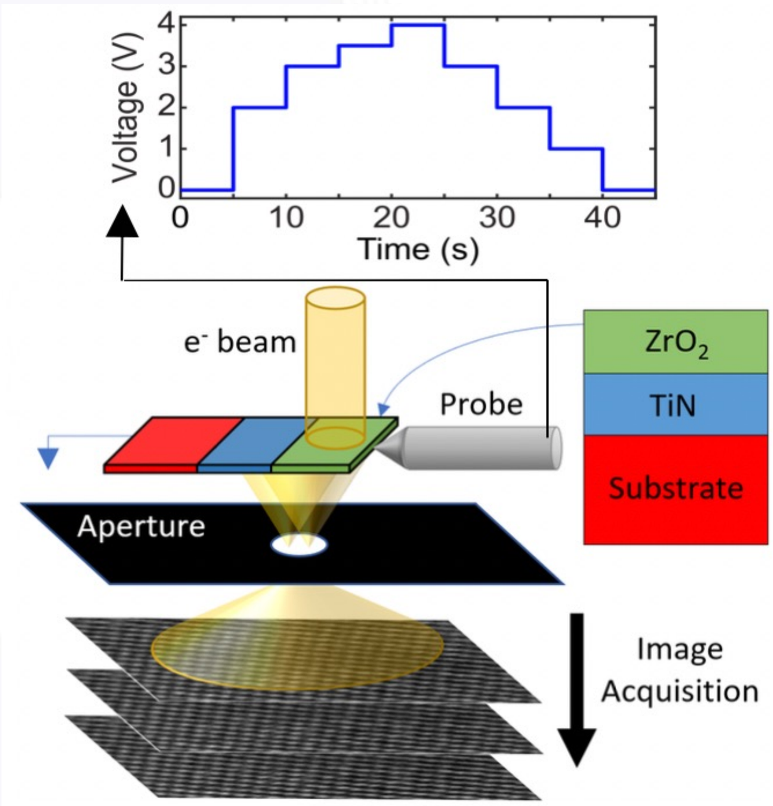
Table 1 | Key parameters and metrics

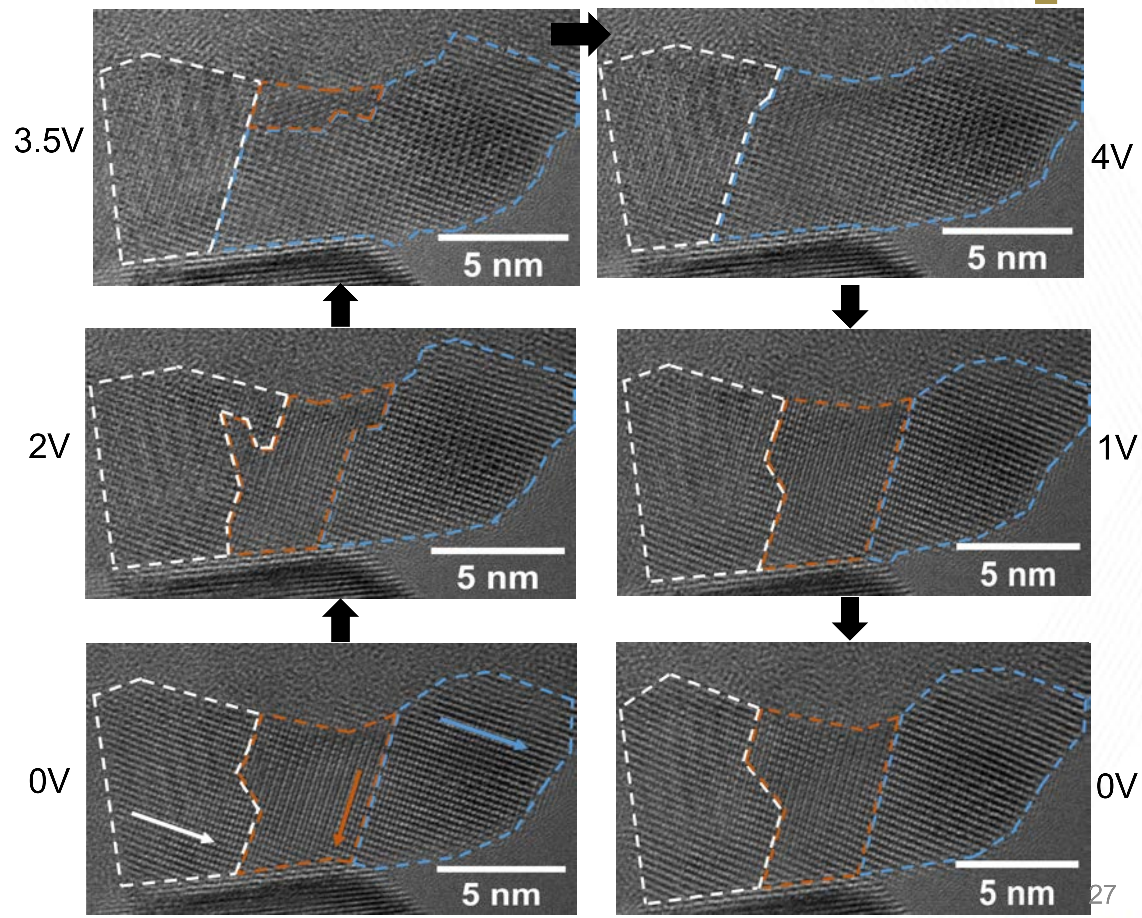
Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	**eDRAM**[70]	**eFlash (FG)**	**eFlash (SG MONOS)**[42]	**eFlash (SONOS)**[41]	**FEFET (hafnia based, MFIS structure)**	**FEFET (hafnia based, MFMIS structure)**	**FRAM (hafnia based)**	**FRAM (perovskite based)**[67]
Cell size	120–150F^2	40F^2	40–60F^2	40–50F^2	50–60F^2	10–30F^2	10–30F^2	30–40F^2	50–60F^2
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 µs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	$>10^{16}$	$>10^{16}$	$\sim10^{4}$	$\sim10^{5}$	$\sim10^{6}$	10^{5}–10^{9}	$>10^{10}$	$>10^{12}$	$>10^{14}$

Key device parameters and performance metrics comparing current embedded memory candidates and ferroelectric technologies. Data for eDRAM, SG MONOS eFlash, SONOS eFlash and perovskite based FRAM are obtained from ref. [70], ref. [42], ref. [41] and ref. [67], respectively. FG, floating gate; SG MONOS, split gate metal-oxide-nitride-oxide-Si; SONOS, Si-oxide-nitride-oxide-Si; eSRAM, embedded static random-access memory; eFlash, embedded flash; eDRAM, embedded dynamic random-access memory; FRAM, ferroelectric random access memory; T, transistor; C, capacitor; FE, ferroelectric; Av., commercially available; Dev., development; Res., research.

Khan, Keshavarzi, Datta. “The future of ferroelectric field-effect transistors.” *Nature Electronics* 3, 588 (2020).

Microstructural transformations with electric-field in ZrO_2

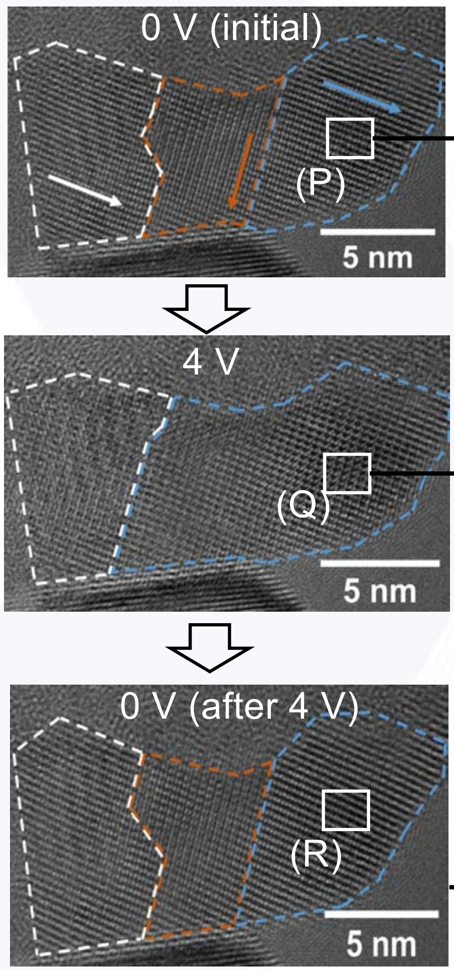


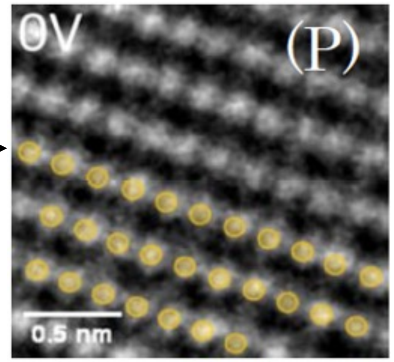


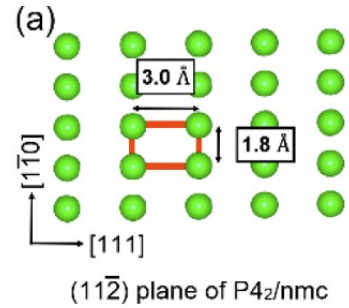
Lombardo, S., *et al.* "Atomic-scale imaging of polarization switching in an (anti-) ferroelectric memory material: Zirconia (ZrO_2)." *2020 IEEE Symposium on VLSI Technology*.

Collaboration with Oak Ridge National Lab.

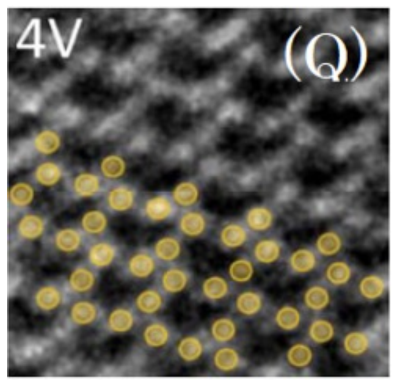
Microstructural transformations with electric-field in ZrO_2

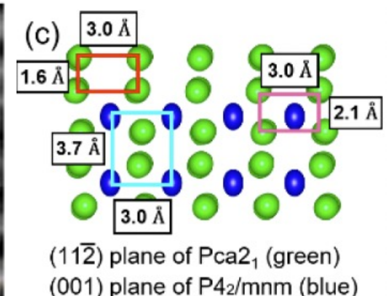




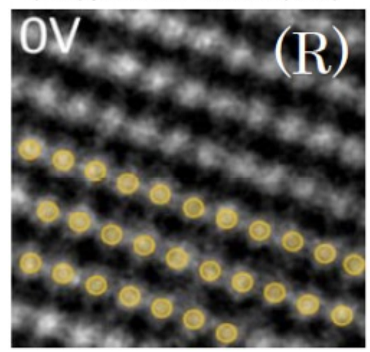


Atomic model of (11$\bar{2}$) projected plane of the *P4$_2$/nmc* phase (a) superimposed onto the HRTEM image of the right-most domain at 0V (b).





Atomic model of (11$\bar{2}$) projected plane of the *Pca2$_1$* phase and (001) projected plane of the *P4$_2$/mnm* phase (not unique) (a) superimposed onto the HRTEM of the right-most domain at 4V (b).



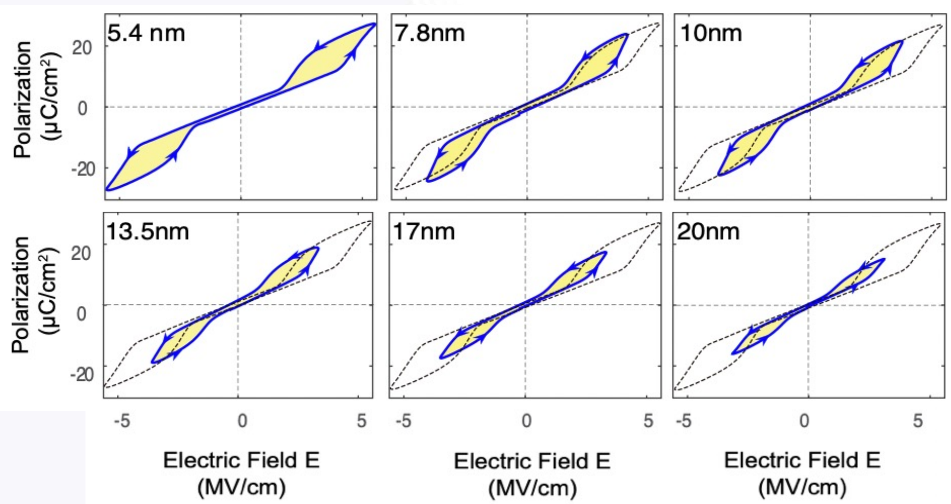
Lombardo, S., *et al.* "Atomic-scale imaging of polarization switching in an (anti-) ferroelectric memory material: Zirconia (ZrO_2)." *2020 IEEE Symposium on VLSI Technology*.

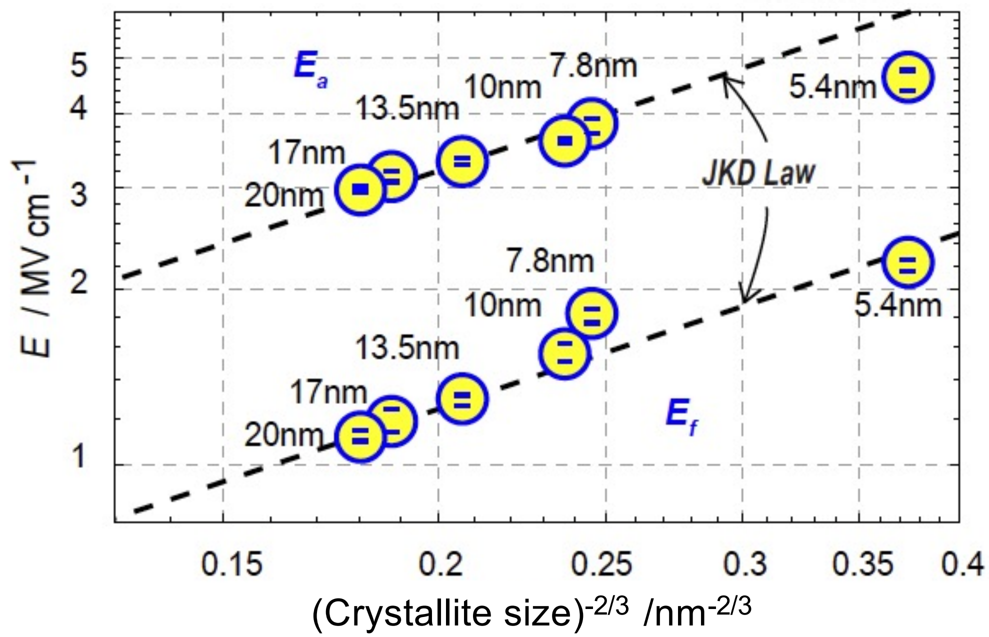
Collaboration with Oak Ridge National Lab.

Functional response and microstructure

Modified Jannovec-Kay-Dunn law for ZrO_2

Critical field ∝ (crystallite size)$^{-2/3}$





Tasneem *et al.* "A Janovec-Kay-Dunn-like behavior at thickness scaling in ultra-thin antiferroelectric ZrO_2 films." (under review.)

Georgia Tech
CREATING THE NEXT

Barriers to ferroelectric technology enablement

Barrier #1: Device-to-device variation due to nano-crystalline microstructure at scaled dimensions.

Barrier #2: Voltage scalability to ~1 V for compatibility with logic circuits for embedded applications.

Barrier #3: Reliability and endurance.

Many of these challenges were solved for perovskite-structure ferroelectrics in 1990s, leading to commercial ferroelectric random-access memories (FRAMs).

The era of **ferroelectronics**

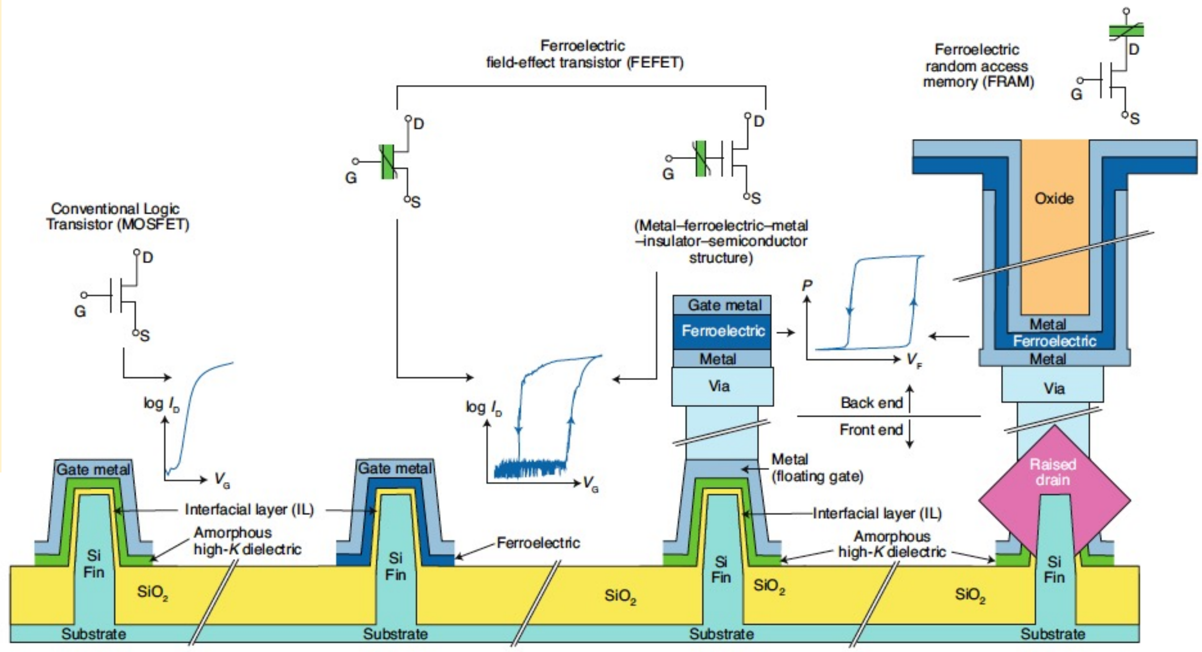
- The next wave of exponential growth of the semiconductor industry depends on how well the electronic hardware can support the explosion of data-centric computing applications.

- Ferroelectric technology will be a key component due to performance, energy and area efficiency and merged logic-memory functionalities, ushering into the era of ***ferroelectronics***.

PERSPECTIVE
https://doi.org/10.1038/s41928-020-00492-7
nature electronics

The future of ferroelectric field-effect transistor technology

Asif Islam Khan[1,2], Ali Keshavarzi[3] and Suman Datta[4]



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

Thank you

Our group at Georgia Tech

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GLOBALFOUNDRIES
TEL Technology Center America
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