



Ferroelectronics **From Applications to Microstructure**

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ALD/ALE
2021
VIRTUAL MEETING

Georgia Tech



Our Team and Sponsors

Our group at Georgia Tech



Collaborators

Lane Martin, University of California, Berkeley
Andrew Kummel, University of California, San Diego
Kyeongjae Cho, University of Texas, Dallas
NaMLab, Dresden Germany
Christopher Nelson, Oak Ridge National Lab
Ali Keshavarzi, Stanford University
GLOBALFOUNDRIES
TEL Technology Center America
Eugenus

Sponsors



6.9 billion

Transistors



*Phil Schiller, SVP of Worldwide Marketing, Apple
September 2018*

Largest Chip Ever Built

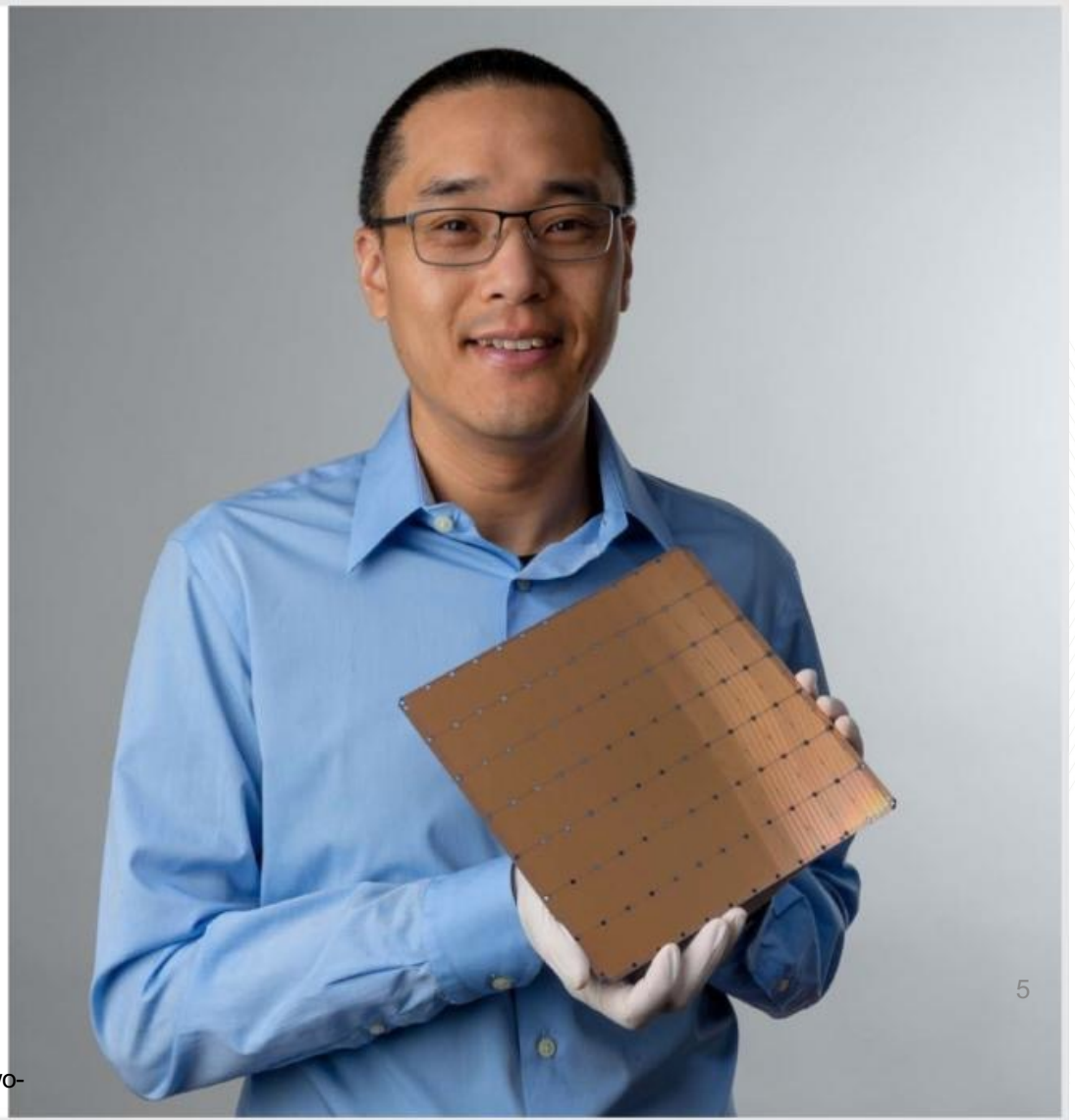
- 46,225 mm² silicon
- 1.2 trillion transistors
- 400,000 AI optimized cores
- 18 Gigabytes of On-chip Memory
- 9 PByte/s memory bandwidth
- 100 Pbit/s fabric bandwidth
- TSMC 16nm process

Wafer-scale integration
For massively parallel supercomputers

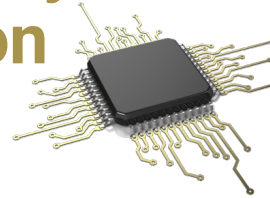
Year 2020



<https://www.anandtech.com/show/16626/cerebras-unveils-wafer-scale-engine-two-wse2-26-trillion-transistors-100-yield>



Energy in Electronics, Data Economy and the Forth Industrial Revolution



Noteworthy milestones in computing and energy

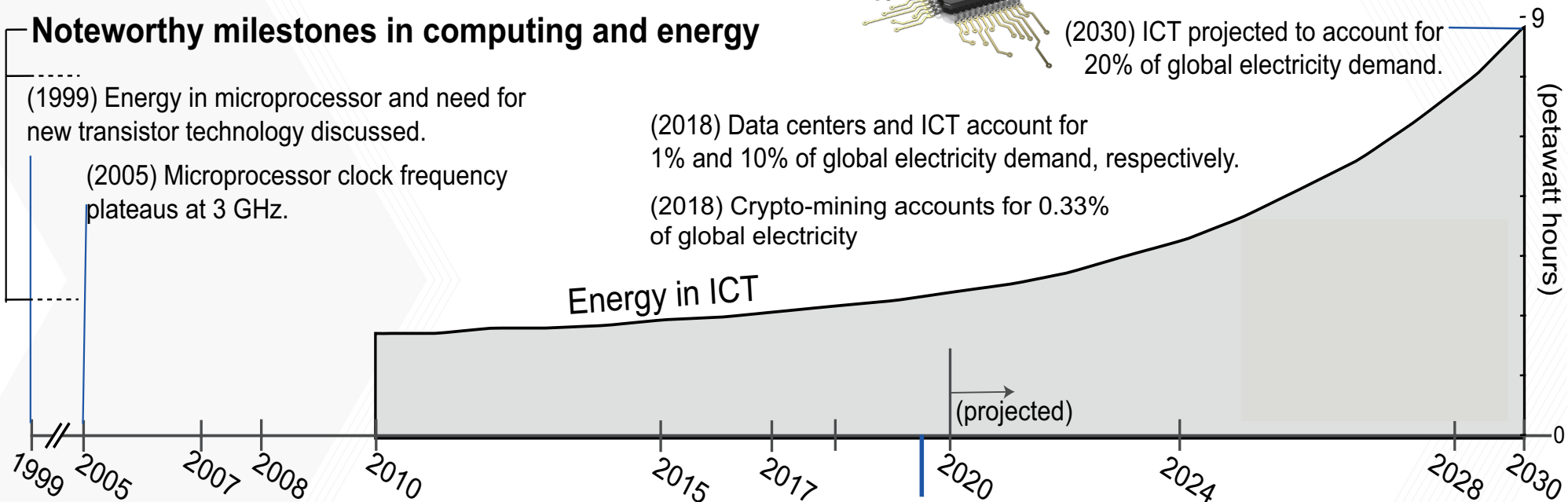
(1999) Energy in microprocessor and need for new transistor technology discussed.

(2005) Microprocessor clock frequency plateaus at 3 GHz.

(2018) Data centers and ICT account for 1% and 10% of global electricity demand, respectively.

(2018) Crypto-mining accounts for 0.33% of global electricity

(2030) ICT projected to account for 20% of global electricity demand.

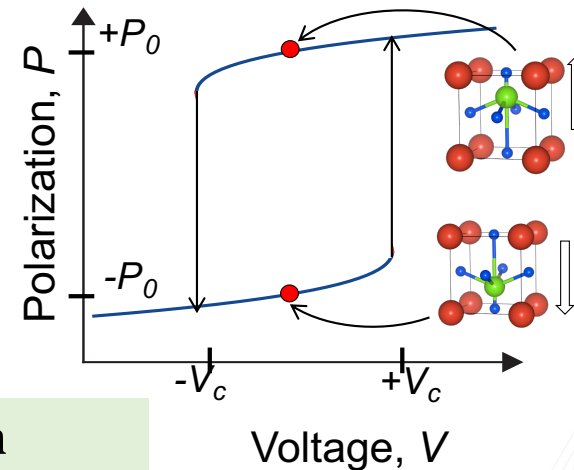
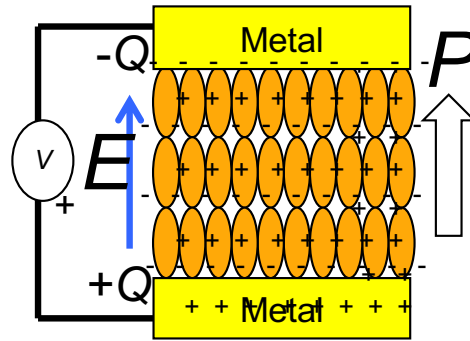
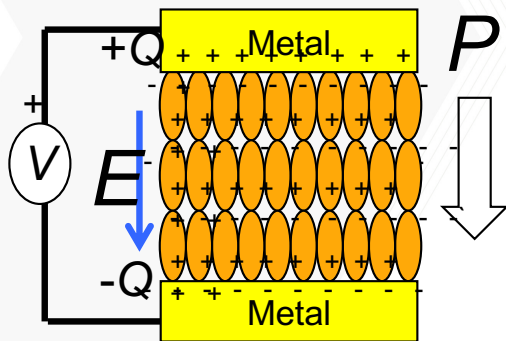
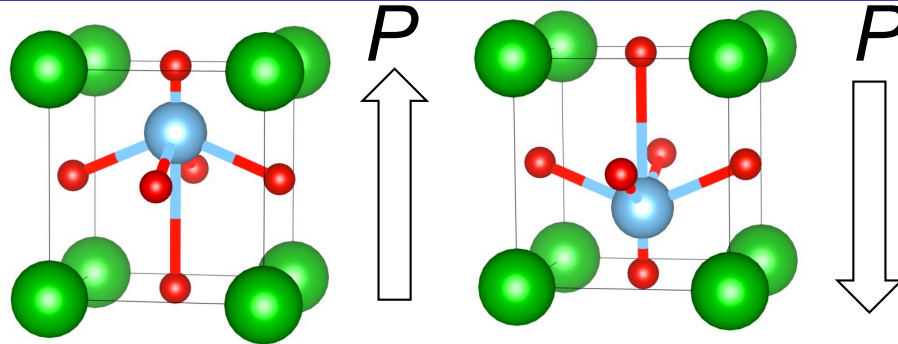


Jones. Inside Information Factories, Nature 561, 163 (2018)

Ferroelectric Oxides

Classical Ferroelectric
 PbTiO_3 , BaTiO_3 etc.

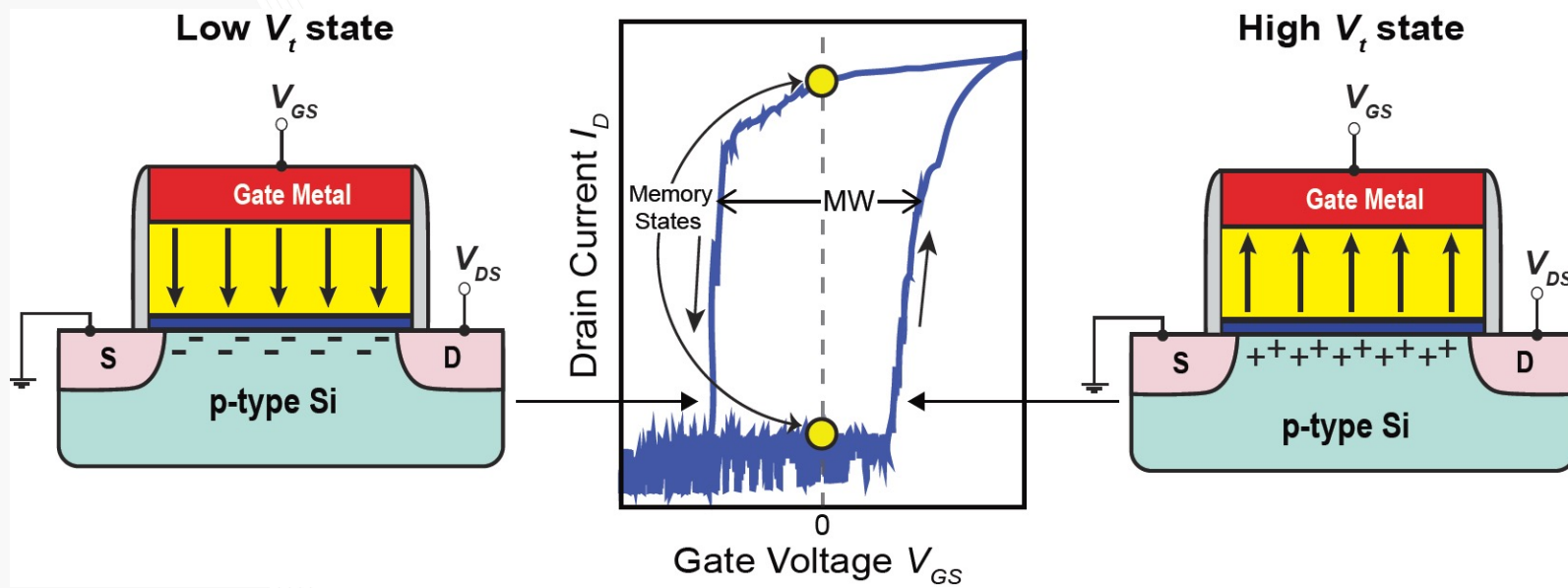
Emerging CMOS compatible
Ferroelectrics:
Doped HfO_2



A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

A ferroelectric field-effect transistor

Ferroelectric Transistors (FEFET): Gate oxide stack includes a FE oxide



A ferroelectric transistor is a **non-volatile memory** device where the data is encoded in its threshold voltage.

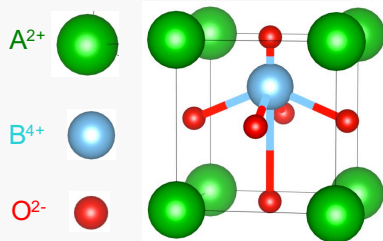
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for code storage in microcontrollers.

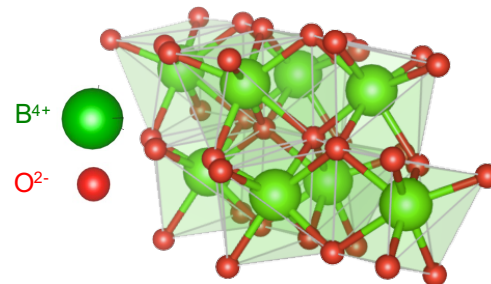
2. Controlled annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al.* *Appl. Phys. Lett.* 99, 112904 (2011)
- Boscke *et al.* *2011 IEEE Int. Electron Devices Meeting*. p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al.* *Nano Lett.* 12, 4318 (2012)

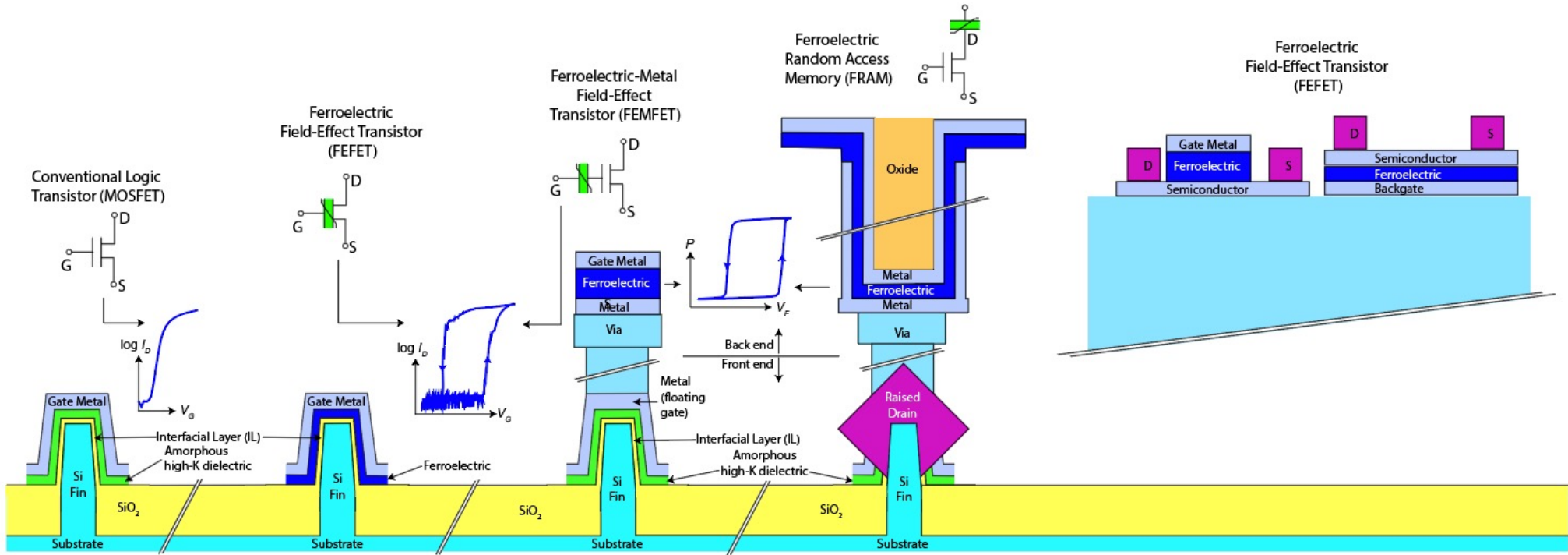
Perovskite-structure
ferroelectric oxide
(ABO_3)



Fluorite-structure
ferroelectric oxide
(BO_2)



The Suite of Ferroelectric devices



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

Why does ferroelectric technology stand out?

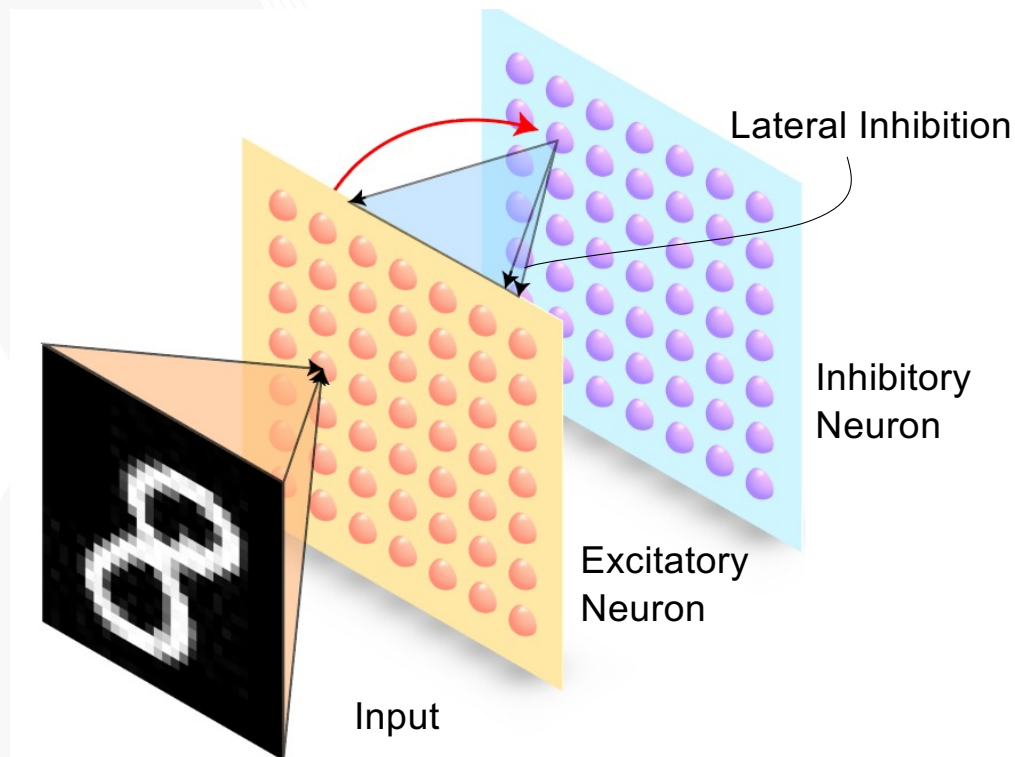
Table 1 | Key parameters and metrics

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM ⁷⁰	eFlash (FG)	eFlash (SG MONOS) ⁴²	eFlash (SONOS) ⁴¹	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based) ⁶⁷
Cell size	120–150F ²	40F ²	40–60F ²	40–50F ²	50–60F ²	10–30F ²	10–30F ²	30–40F ²	50–60F ²
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 μs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	>10 ¹⁶	>10 ¹⁶	~10 ⁴	~10 ⁵	~10 ⁶	10 ⁵ –10 ⁹	>10 ¹⁰	>10 ¹²	>10 ¹⁴

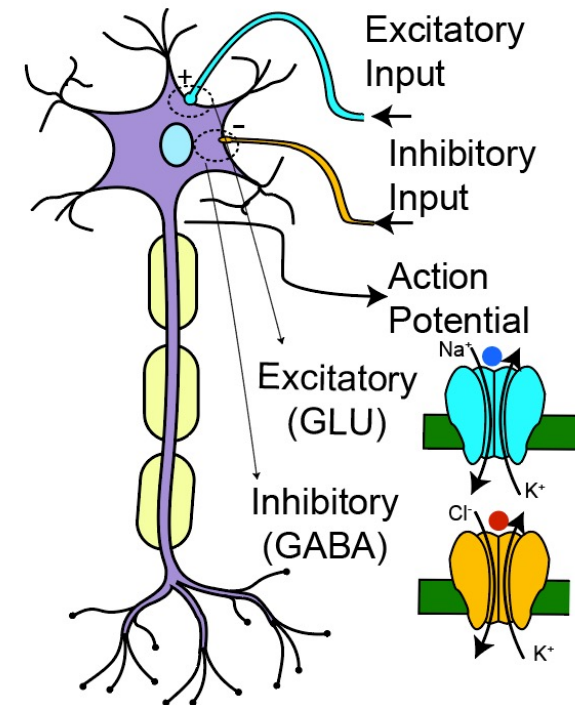
Key device parameters and performance metrics comparing current embedded memory candidates and ferroelectric technologies. Data for eDRAM, SG MONOS eFlash, SONOS eFlash and perovskite based FRAM are obtained from ref. ⁷⁰, ref. ⁴², ref. ⁴¹ and ref. ⁶⁷, respectively. FG, floating gate; SG MONOS, split gate metal-oxide-nitride-oxide-Si; SONOS, Si-oxide-nitride-oxide-Si; eSRAM, embedded static random-access memory; eFlash, embedded flash; eDRAM, embedded dynamic random-access memory; FRAM, ferroelectric random access memory; T, transistor; C, capacitor; FE, ferroelectric; Av., commercially available; Dev., development; Res., research.

Khan, Keshavarzi, Datta. “The future of ferroelectric field-effect transistors.” *Nature Electronics* 3, 588 (2020).

Spiking Neural Network: The Role of Inhibition

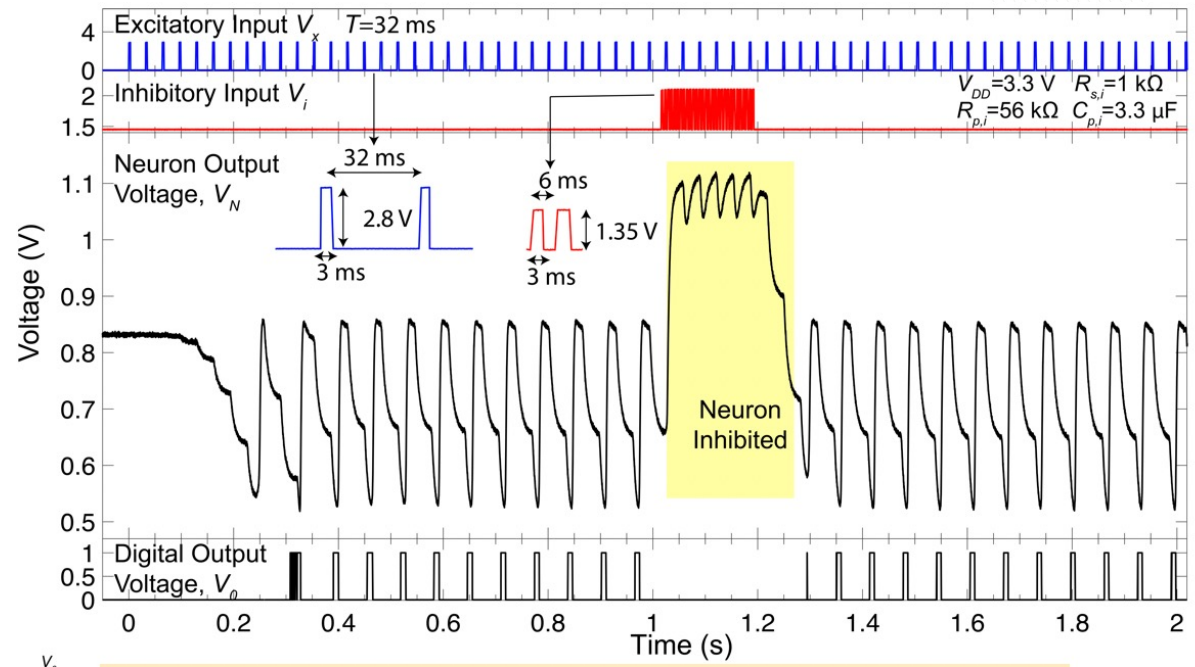
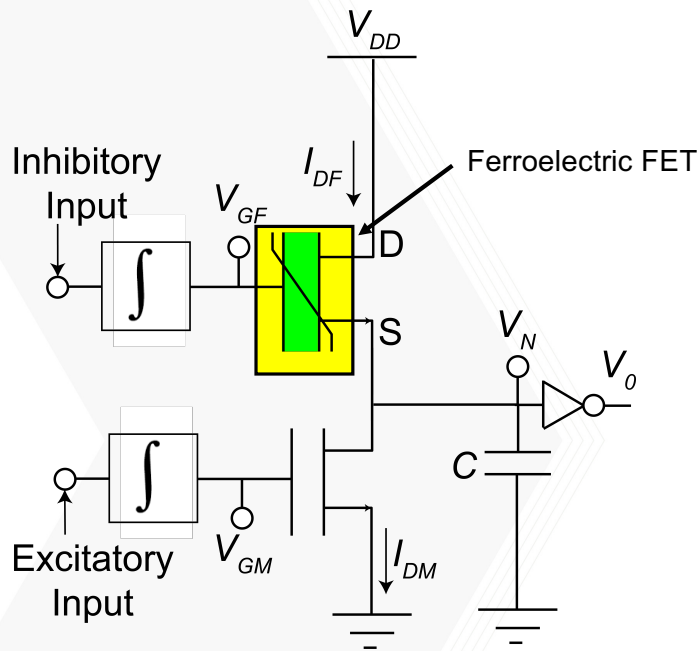


Deihl & Cook, Frontiers Comp. Neurosci. 9, 99 (2015)



Biology: Inhibition required for regulation in activation of excitatory neurons; homeostasis
Bio-inspired computing: High accuracy in unsupervised learning.

Ferroelectric Neuron with excitatory and inhibitory connection



The first demonstration of an artificial neuron with integrated **inhibitory and excitatory** input!

Wang *et al.* Experimental demonstration of ferroelectric spiking neurons for unsupervised clustering. In *2018 IEEE International Electron Devices Meeting (IEDM)* (pp. 13-3). IEEE.

research highlights

NEUROMORPHIC DEVICES
Ferroelectric spiking neurons
2018 IEEE Int. Electron Devices Meet. (in the press)

Brain-like computation using artificial neural networks (ANNs) could provide improved energy efficiency when compared

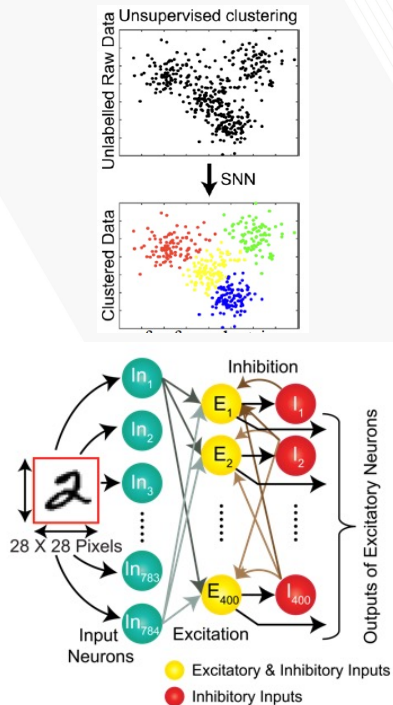
nature
electronics

13

Georgia
Tech
CREATING THE NEXT

Ferroelectric SNNs for unsupervised clustering

Wang et al. Experimental demonstration of ferroelectric spiking neurons for unsupervised clustering. In *2018 IEEE International Electron Devices Meeting (IEDM)* (pp. 13-3). IEEE.



	Indiveri ISCAS 2003	Amravati ISSCC 2018	Jerry et al. VLSI 2017	Current work
Technology	CMOS Analog, Mixed Signal		Emerging Technology	
Neuron Type	LIF	Multiply-Accumulate	LIF	LIF
Network Type	Spiking	Non-spiking	Spiking	Spiking
Data Encoding Architecture	Spike Timing	Multi-level perceptron	Spiking Rate	Spike Timing
Input Type	Excitatory	Excitatory	Excitatory	Excit. & Inhib.
Device Count	15 T	64 T	1T - 1 VO ₂	1T - 1 FEFET
Synapse Weight	Pos. & Neg.	Pos. & Neg.	Pos. & Neg.	Pos.
Training & Classification	Unsupervised	Reinforcement	Supervised	Unsupervised
Power	10 nW	125 nW	Not reported	3.6 nW

Publications from
other groups

Han, Joon-Kyu, et al. *IEEE Electron Device Letters* 41.2 (2019): 208-211.

Dutta, S., et al. *2019 Symposium on VLSI Technology*. IEEE, 2019.

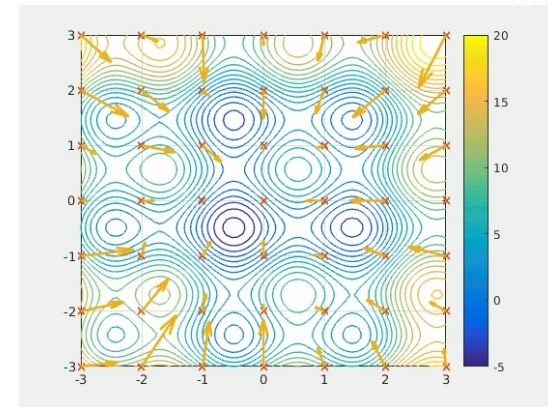
Chen, C., et al. *2019 Symposium on VLSI Technology*. IEEE, 2019.

Luo, Jin, et al. *2019 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2019.

Collective Behavior and Swarm Intelligence

- Neuro-biology and natural swarm behaviors
- Large number of simple agents giving rise to intelligent behavior
- Computationally hard problems (graph coloring, traveling salesman problem etc.)

General
Framework

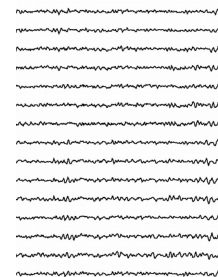


A school of fish and a shark

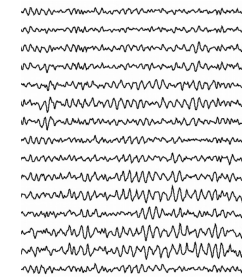


Collective Spatio-temporal oscillations
in Primary Visual Cortex

Eyes open

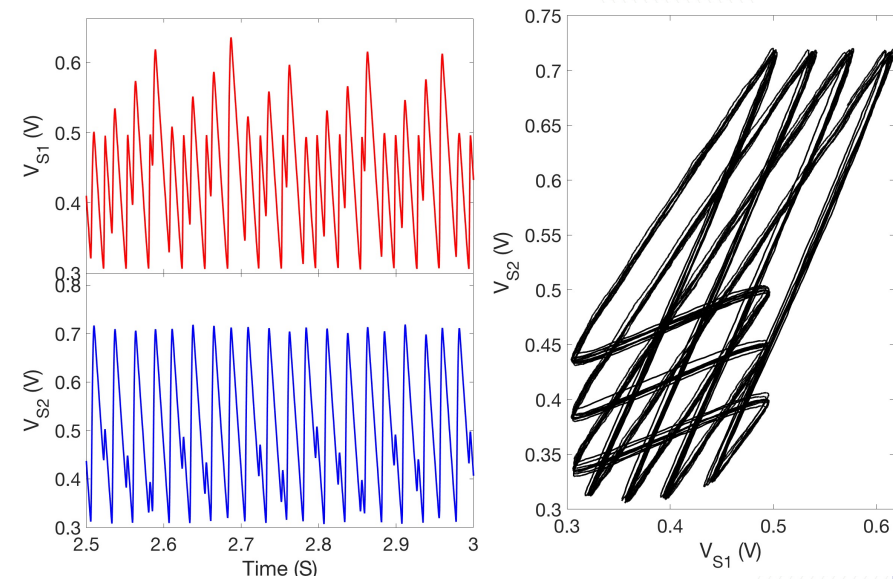
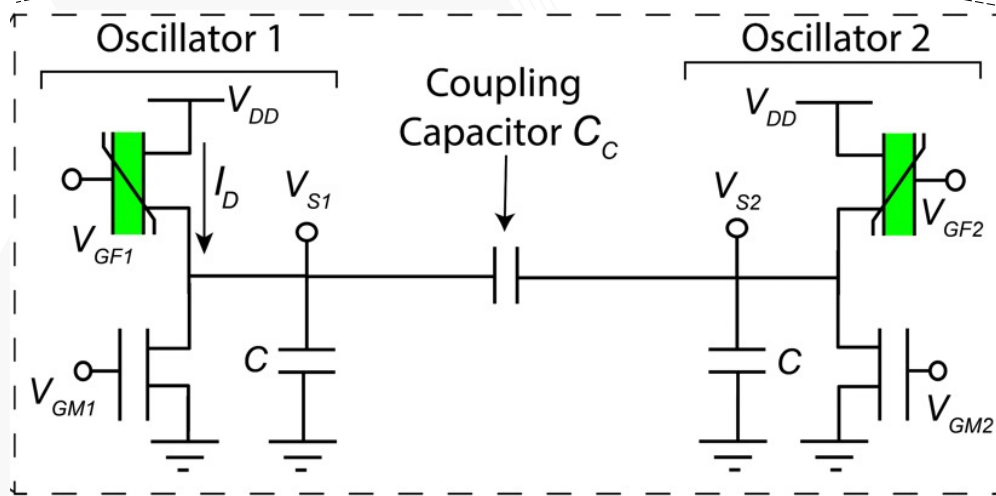
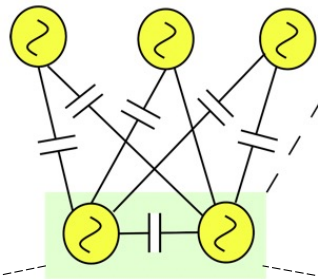


Eyes closed



Collaboration with Arijit Raychowdhury (Georgia Tech)

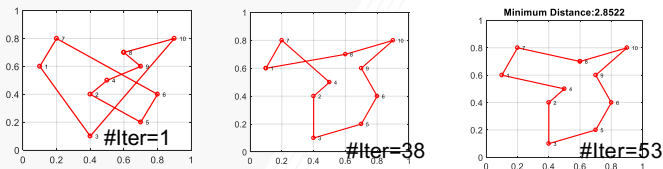
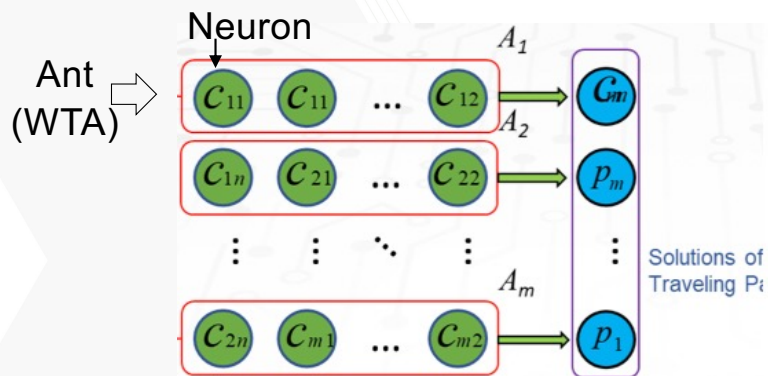
Coupled Ferroelectric Neurons (Experiments)



When the coupled strength of two oscillators is tuned, the coupled system is **synchronized**, showing a periodic pattern.

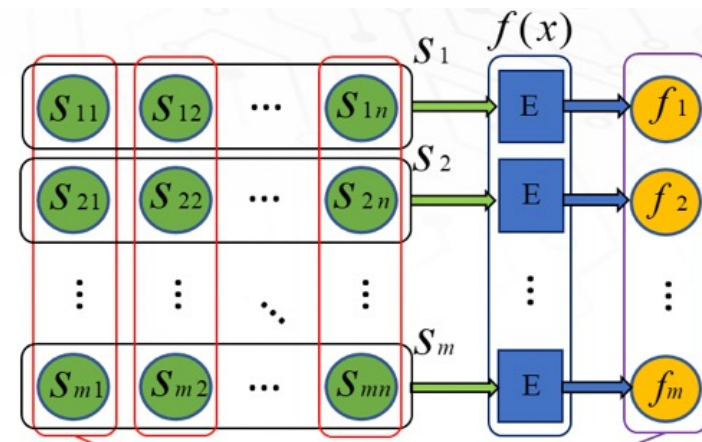
Coupled FE Neurons for Computationally Hard Problems

Ant Colony Algorithm for Traveling Salesman Problem



FE Neuron: **Regular Spiking (RS)** mode.
Inhibition Needed.
Phase based Representation.

Optimization of Continuous Objective Function



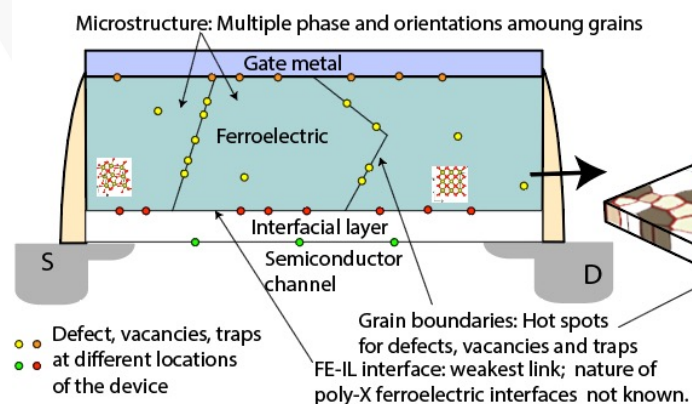
FE Neuron: **Fast Spiking (FS)** mode.
Inhibition disabled.
Rate-based Representation

Fan et al. Frontiers in Neuroscience 2019.

FEFET challenges for embedded applications

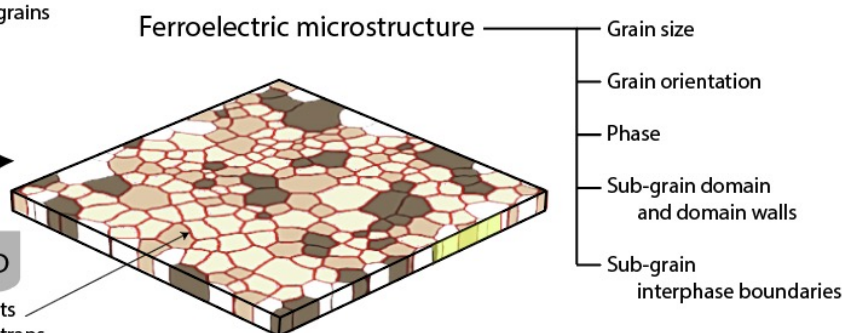
1

Write voltage and memory window



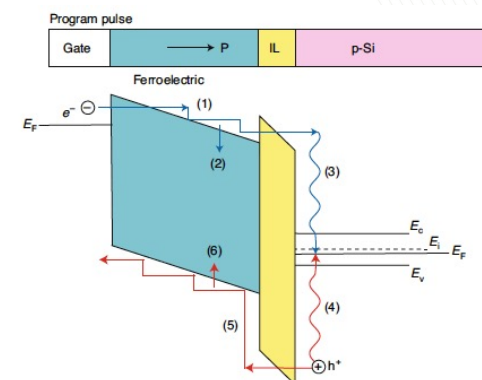
2

Device-to-device and cycle-to-cycle variation



3

Reliability and endurance



“The future of ferroelectric field-effect transistor technology”, Nature Ele. 2020.

Goals (on the ambitious side)

<1.5 V write voltage
>0.5 V memory window

$\Delta V_{t,3\sigma} = 20\text{-}50 \text{ mV}$ (7 nm node)

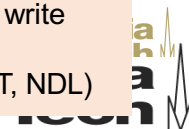
> 10^{12} cycles

State-of-the-art

BEOL: ~1.8 V write with >0.7 V memory window (Sharma et al. IEDM 2020)
FEOL: 3-9 V write for 0.5-1.2 V memory window

$\Delta V_{t,3\sigma} = 200\text{-}500 \text{ mV}$ (W,L=200 nm)
(Maekawa et al. VLSI 2019)

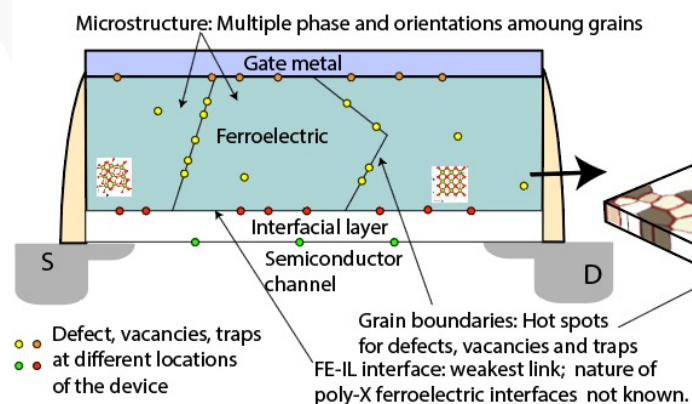
BEOL: > 10^{12} cycles w/ <1 ns write (Sharma et al. IEDM 2020)
FEOL: > 10^{10} cycles (ASCENT, NDL)



FEFET challenges for embedded applications

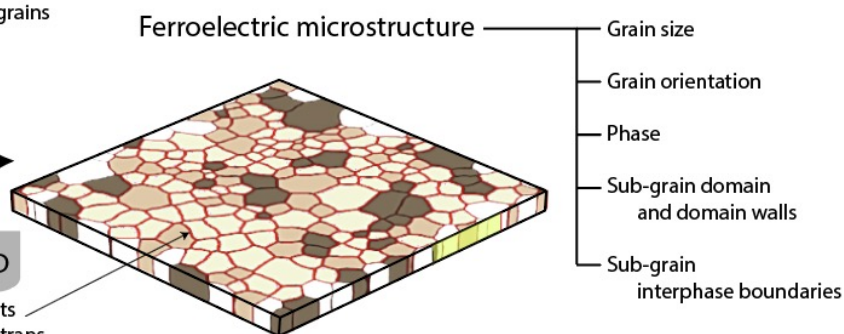
1

Write voltage and memory window



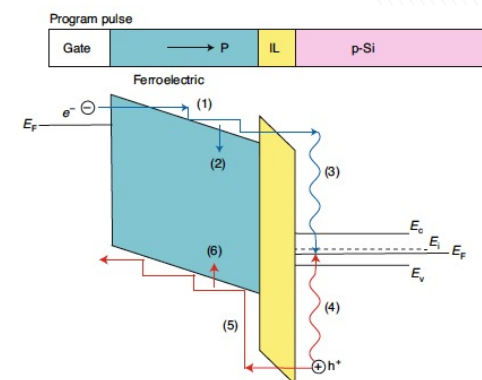
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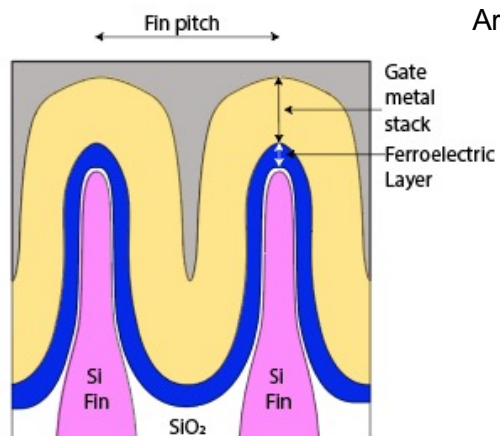
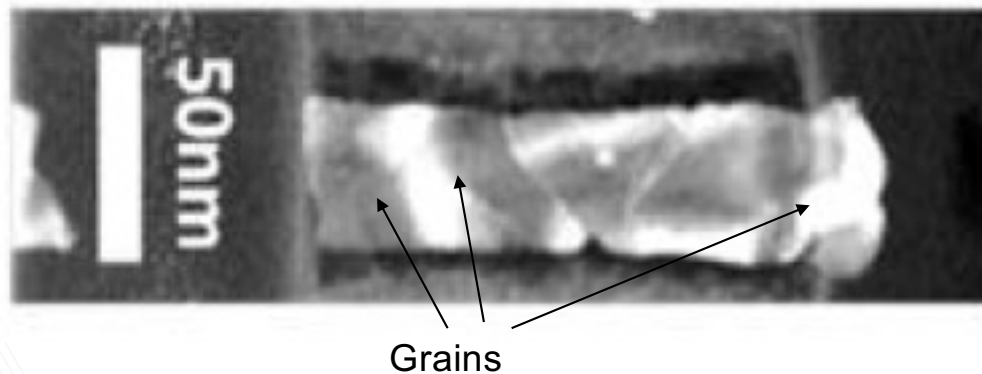
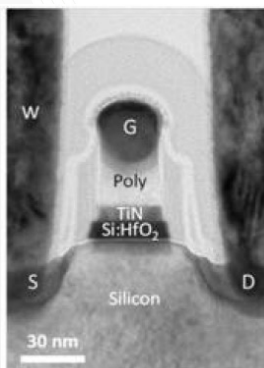
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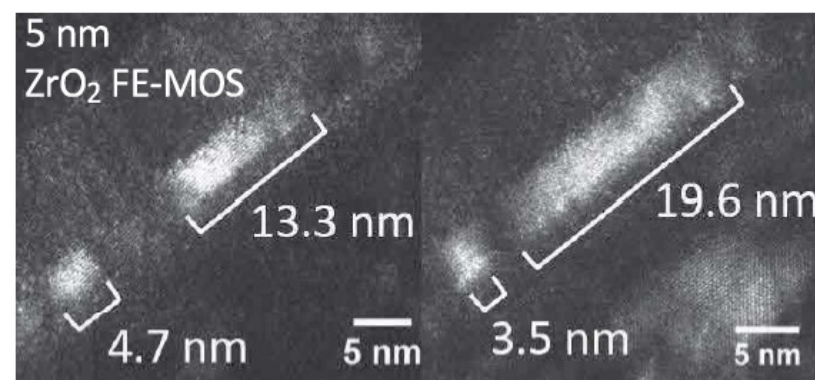
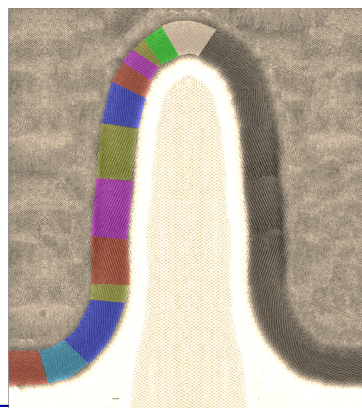


Polycrystalline microstructure in FEFET

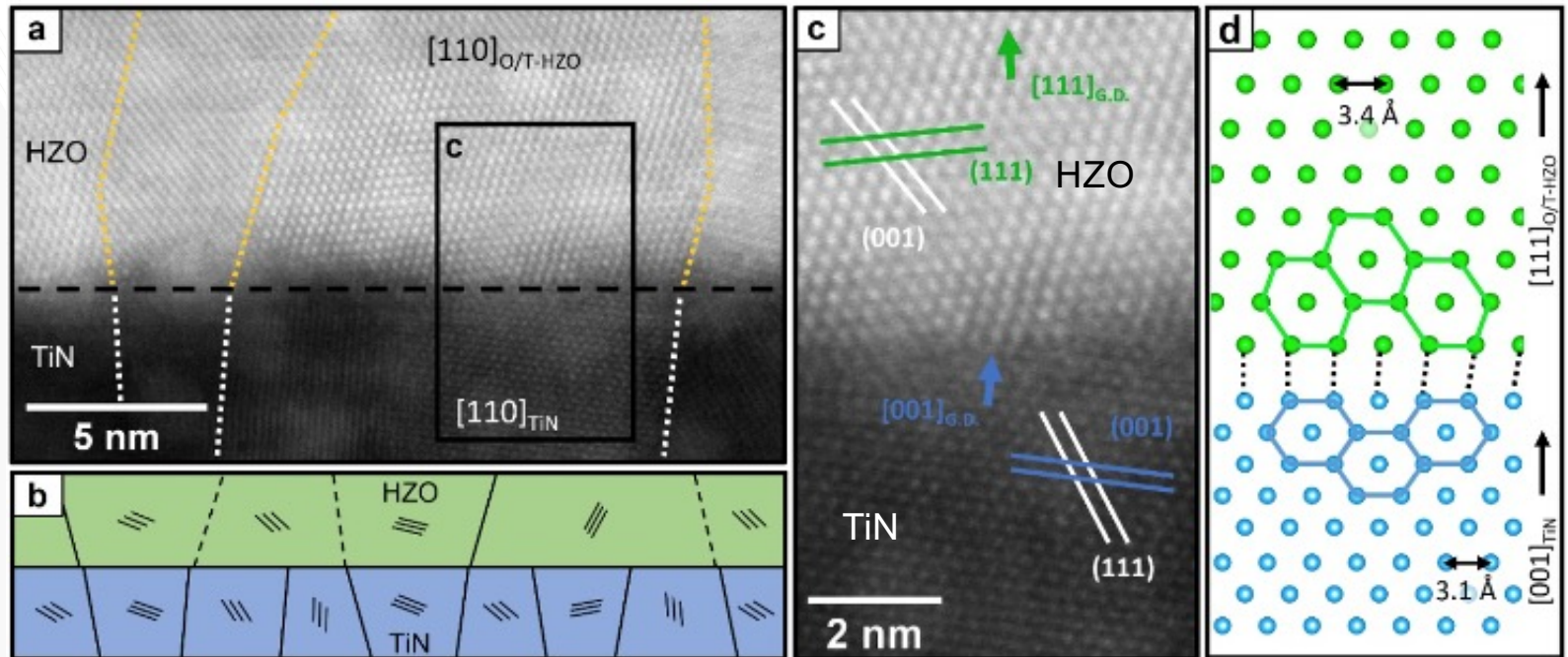
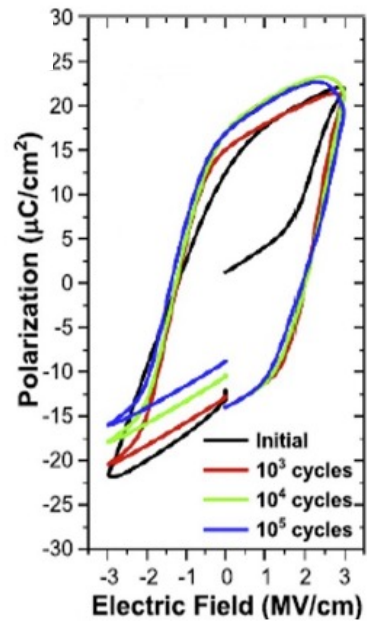
Mulaosmanovic et al. ACS Appl Mater Int. 2017



Artistic rendition (NOT an actual device)

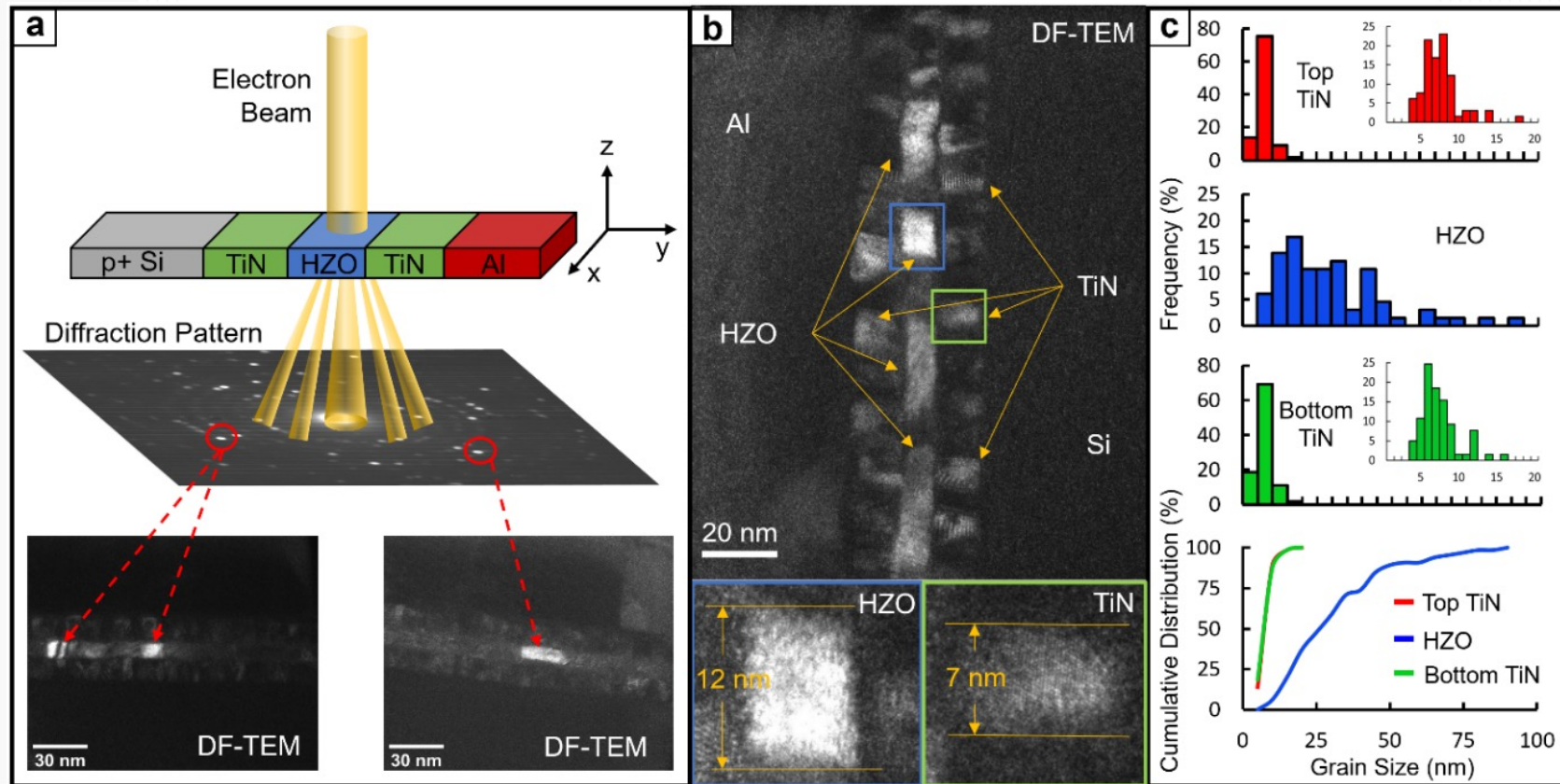


Microstructure (STEM) of FE ZrO₂ on TiN



Evidence of **near-coincident site epitaxy** from both top and bottom TiN

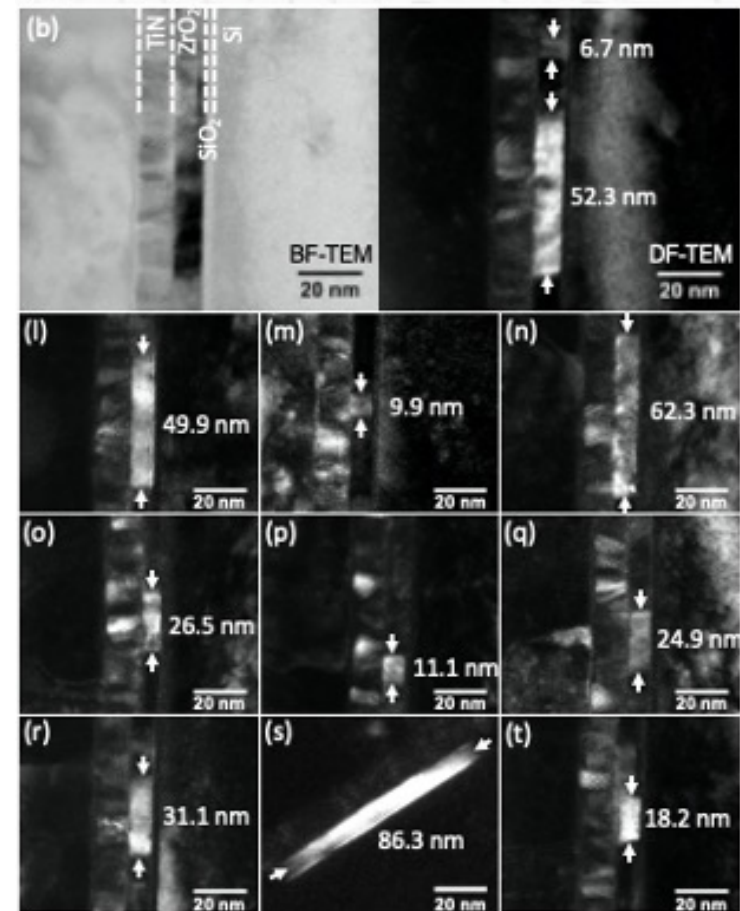
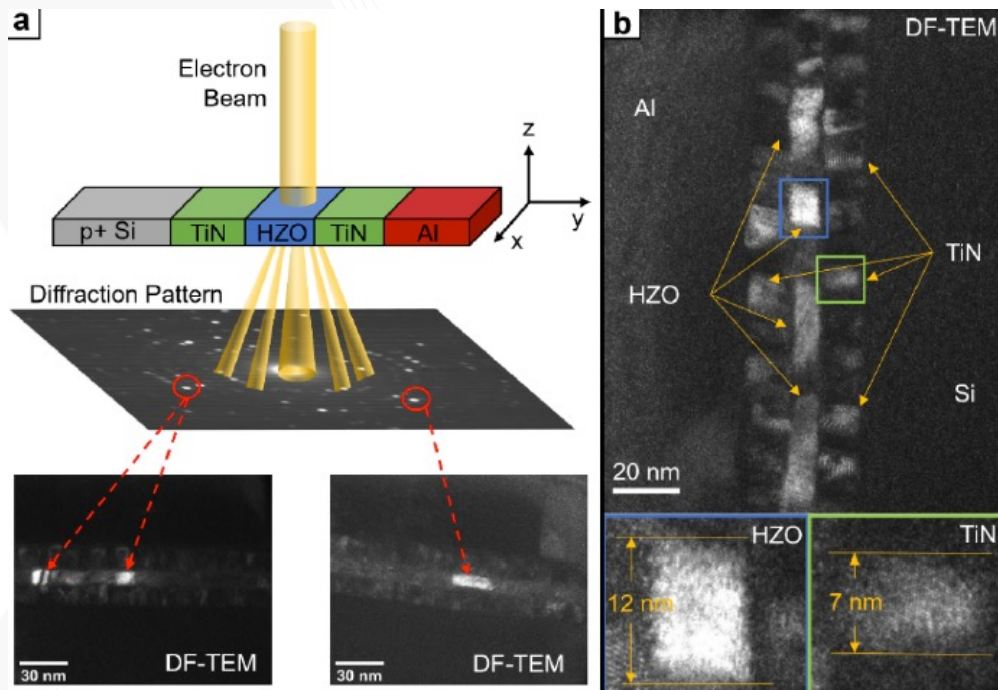
Microstructure (DF-TEM) of FE HZO



Grain size measurement from 2-D cross-section
Need statistics (~100 grains)

Lombardo et al. (submitted)

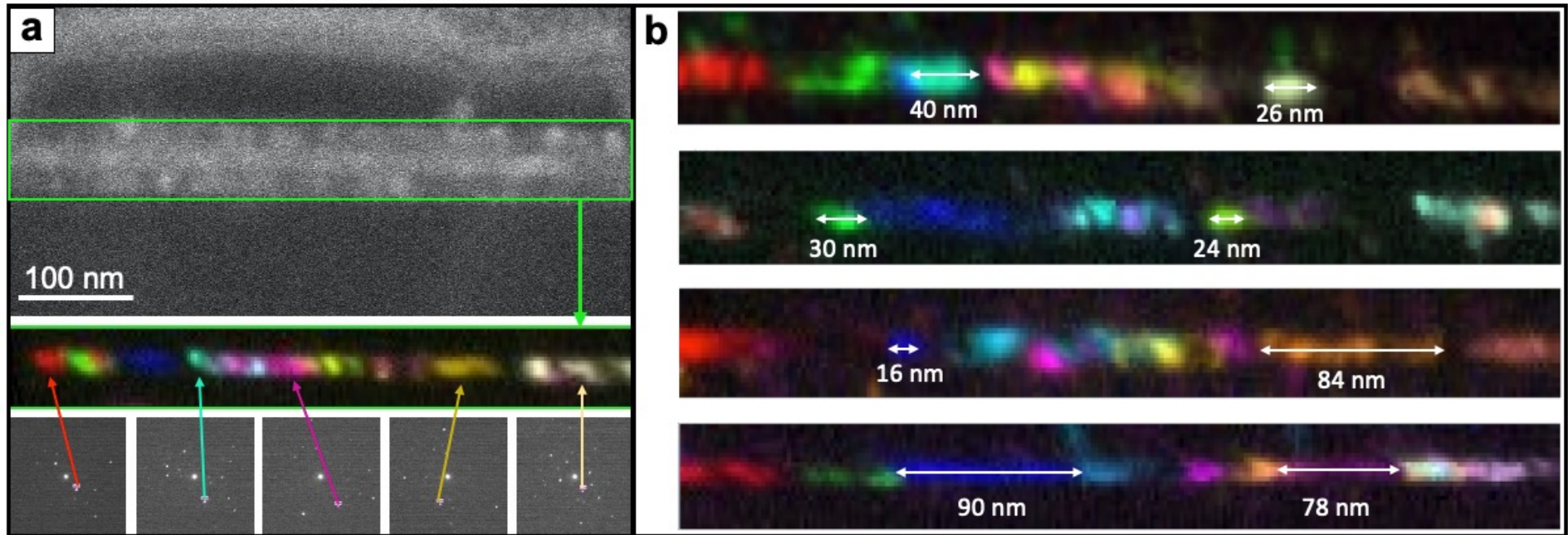
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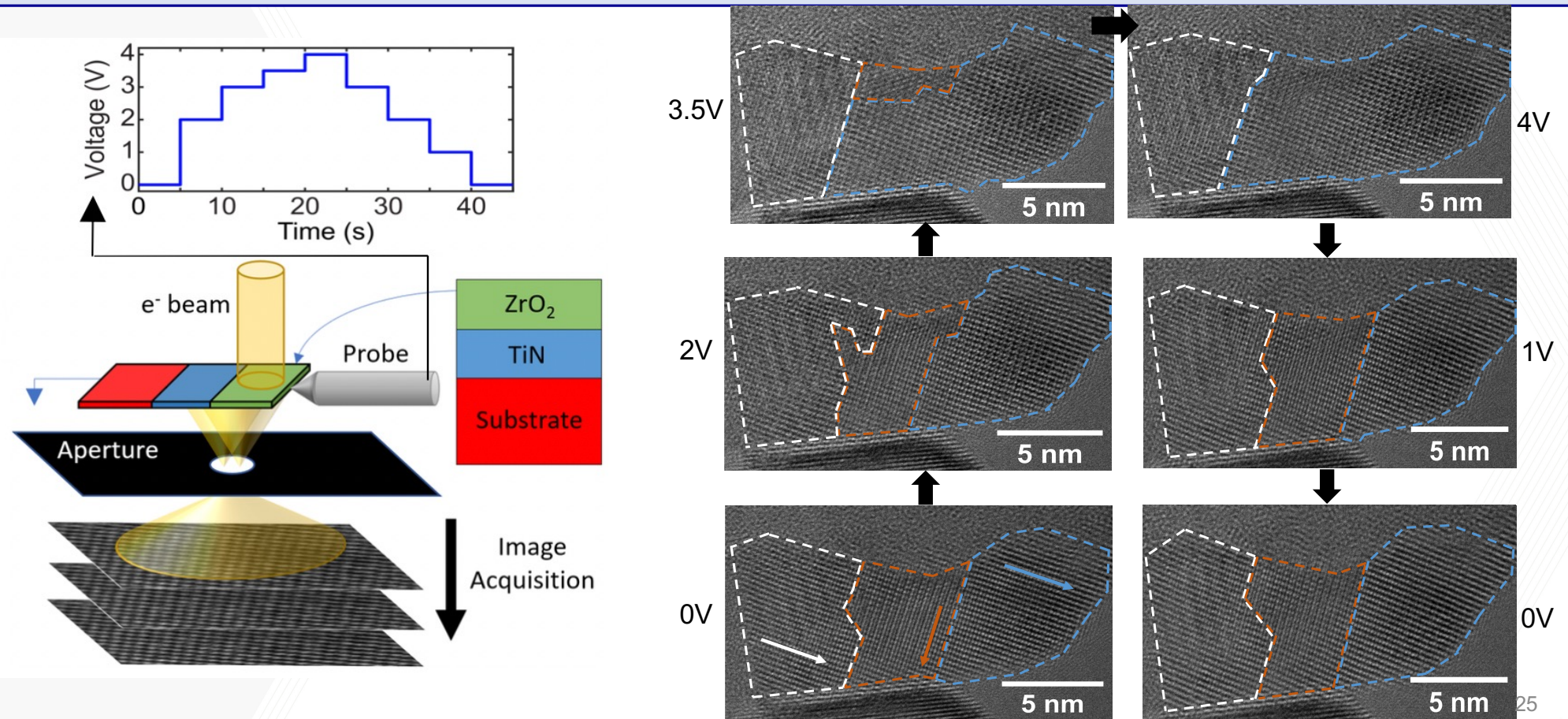
Microstructure (NBED) of FE HZO



Evidence of **near-coincident site epitaxy** from both top and bottom TiN in NBED

Lombardo et al. (submitted)

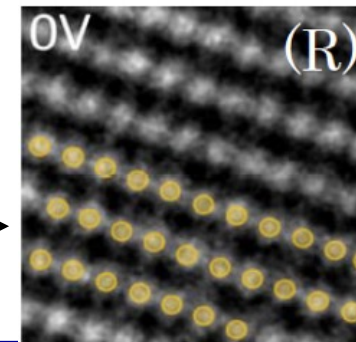
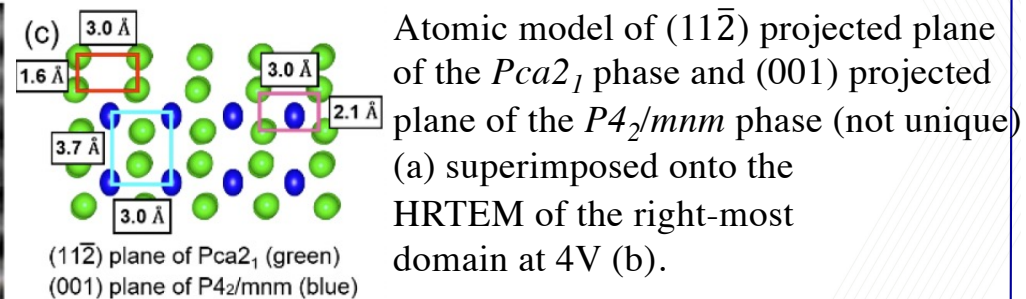
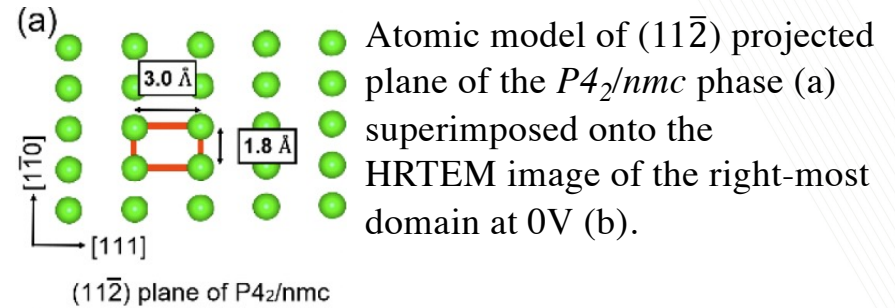
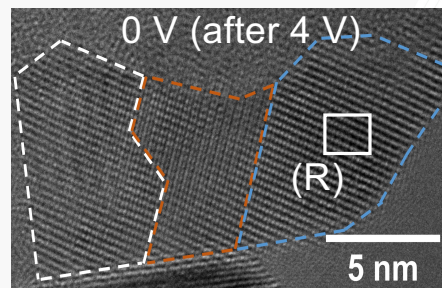
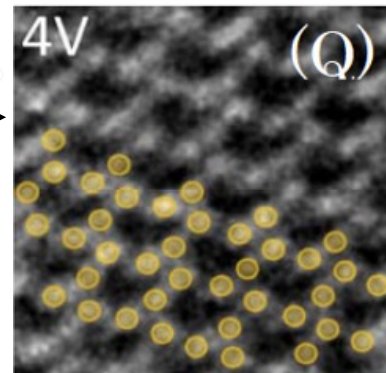
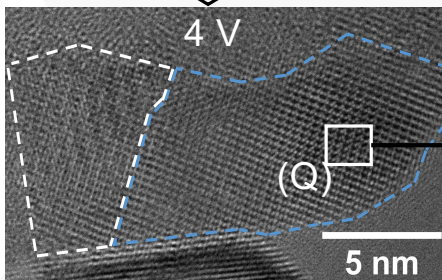
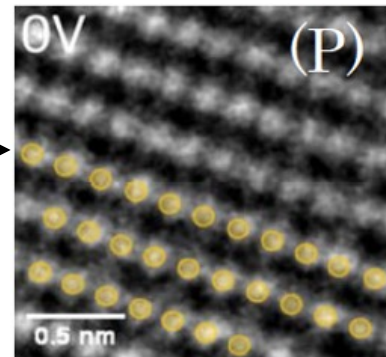
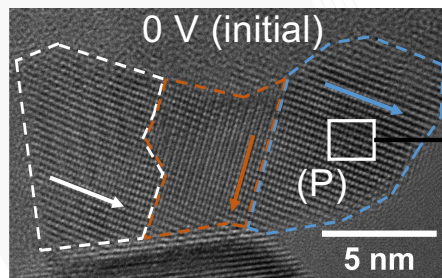
Microstructural transformations with electric-field in ZrO_2



Lombardo, S., et al. "Atomic-scale imaging of polarization switching in an (anti-) ferroelectric memory material: Zirconia (ZrO_2).
2020 IEEE Symposium on VLSI Technology.

Collaboration with Oak Ridge National Lab.

Microstructural transformations with electric-field in ZrO_2



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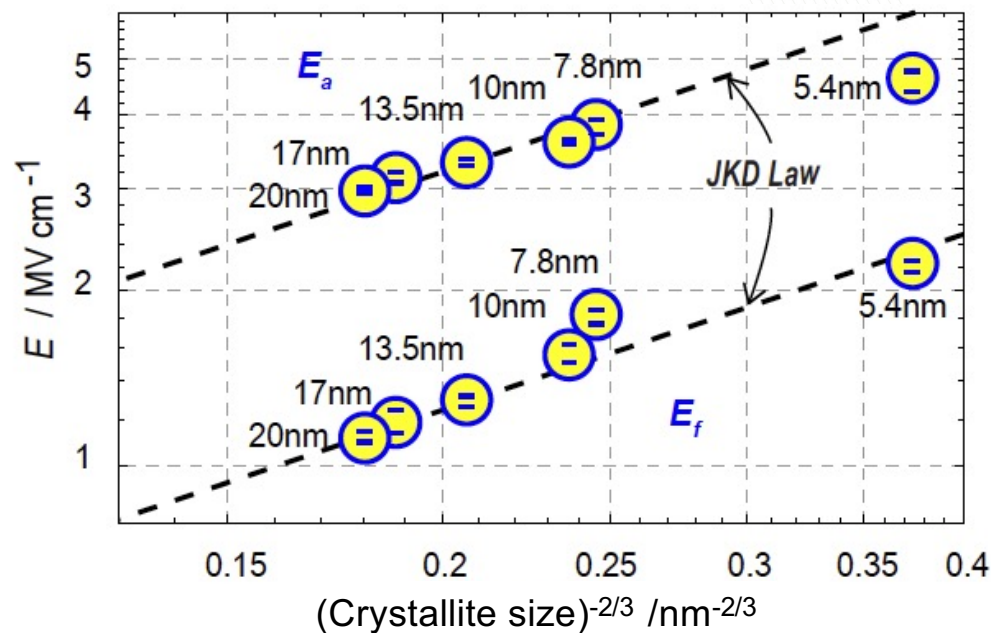
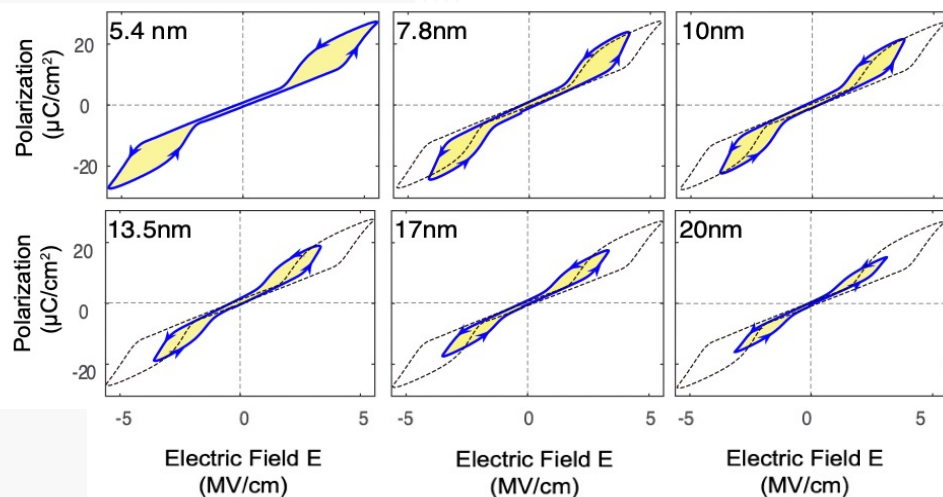
26

Collaboration with Oak Ridge National Lab.

Functional response and microstructure

Modified Jannovec-Kay-Dunn law for ZrO_2

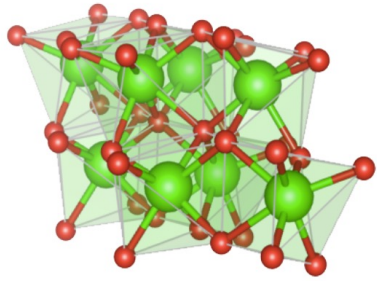
Critical field $\propto (\text{crystallite size})^{-2/3}$



Tasneem *et al.* "A Janovec-Kay-Dunn-like behavior at thickness scaling in ultra-thin antiferroelectric ZrO_2 films." (under review.)

Ferroelectric field-effect transistor

Ferroelectric Oxide



Properties of
Ferroelectric oxides

Non-volatility and
hysteresis

Plasticity,
Meta-plasticity and
Anti-plasticity

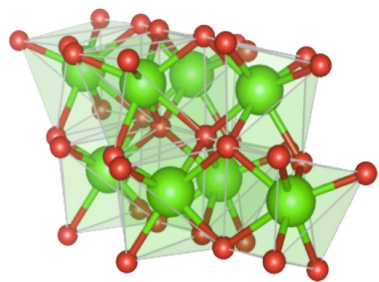
Negative dielectric
permittivity/negative
capacitance

Stochasticity

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

Ferroelectric field-effect transistor

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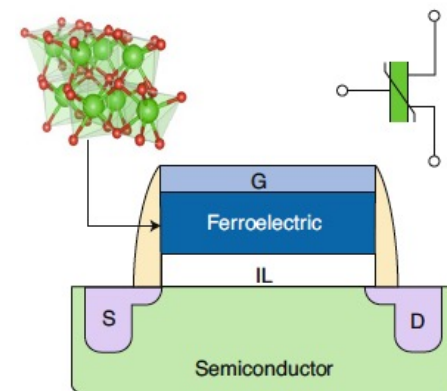
Stochasticity

Transistor
physics

Transconductance
gain

Circuit-level design

Ferroelectric field-effect
transistor



Properties enabled by
a transistor structure

The era of ferroelectronics

- The next wave of exponential growth of the semiconductor industry depends on how well the electronic hardware can support the explosion of data-centric computing applications.
- Ferroelectric technology will be a key component due to performance, energy and area efficiency and merged logic-memory functionalities, ushering into the era of **ferroelectronics**.

PERSPECTIVE

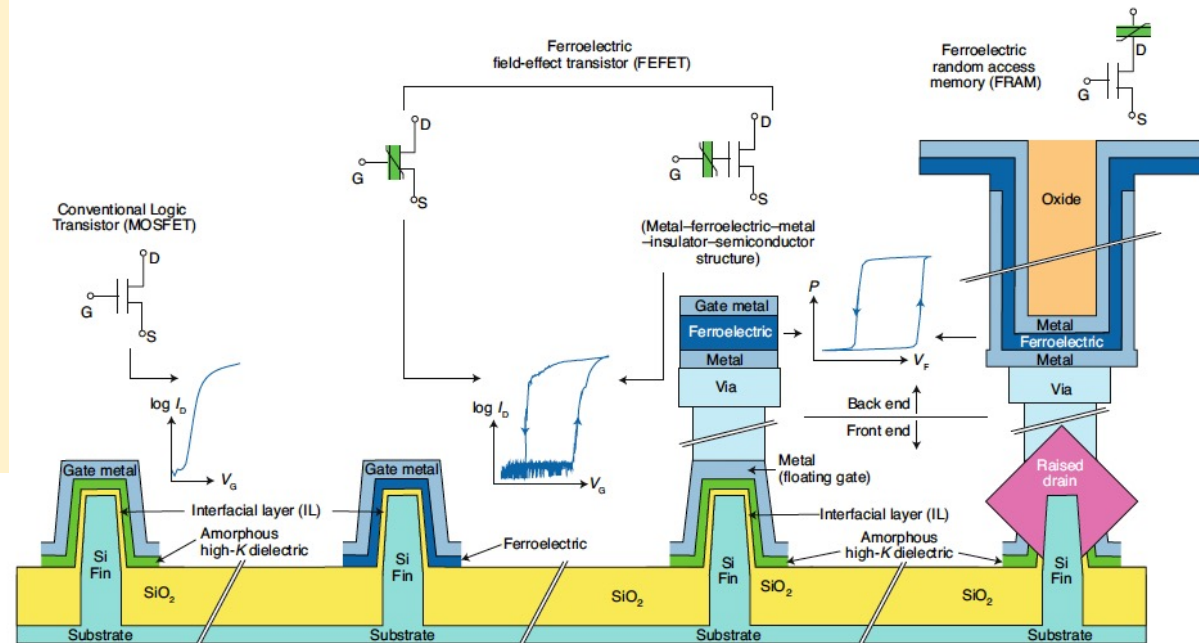
<https://doi.org/10.1038/s41928-020-00492-7>

nature
electronics

Check for updates

The future of ferroelectric field-effect transistor technology

Asif Islam Khan^{1,2}, Ali Keshavarzi³ and Suman Datta⁴



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

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Our Team and Sponsors

Our group at Georgia Tech



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