Pushing the limits of NAND scaling with *Ferroelectrics*

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EMD Performance Materials

intel

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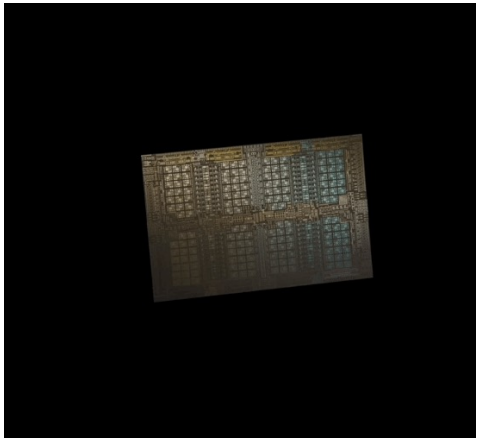
The World of Chips

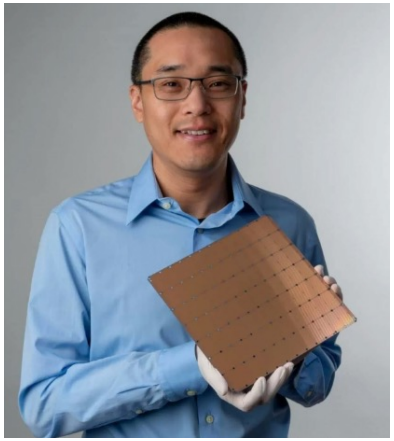
iPhone 17
A19 Chip

~20 Billion Transistors



NVIDIA Blackwell

~200 Billion Transistors



Cerebras Wafer Scale Engine
AI Superchip

~2 Trillion Transistors

Solid State Hard-drives
NAND Storage

~5 Trillion Transistors

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The NAND Storage Technology in the Age of AI

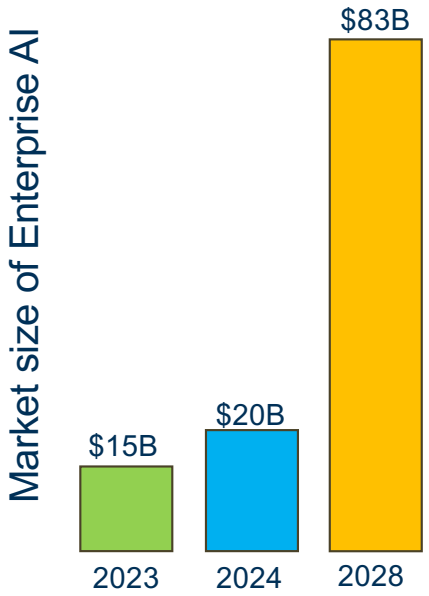
Storage

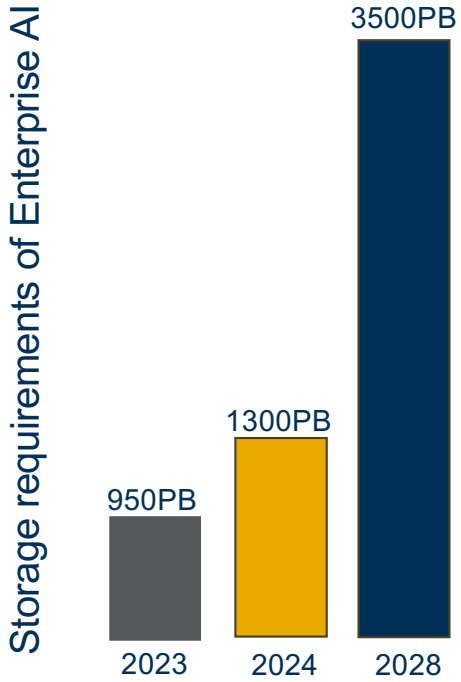
Client, Mobile, and Enterprise

230+ layers

2.4 GB/s

Source: Micron





Source: The Business Research Company

Processing and storing data in AI effectively and cost efficiently can require HBM for the actual AI training, but also various types of NAND-based solid-state storage to support the data flows needed to and from the HBM.

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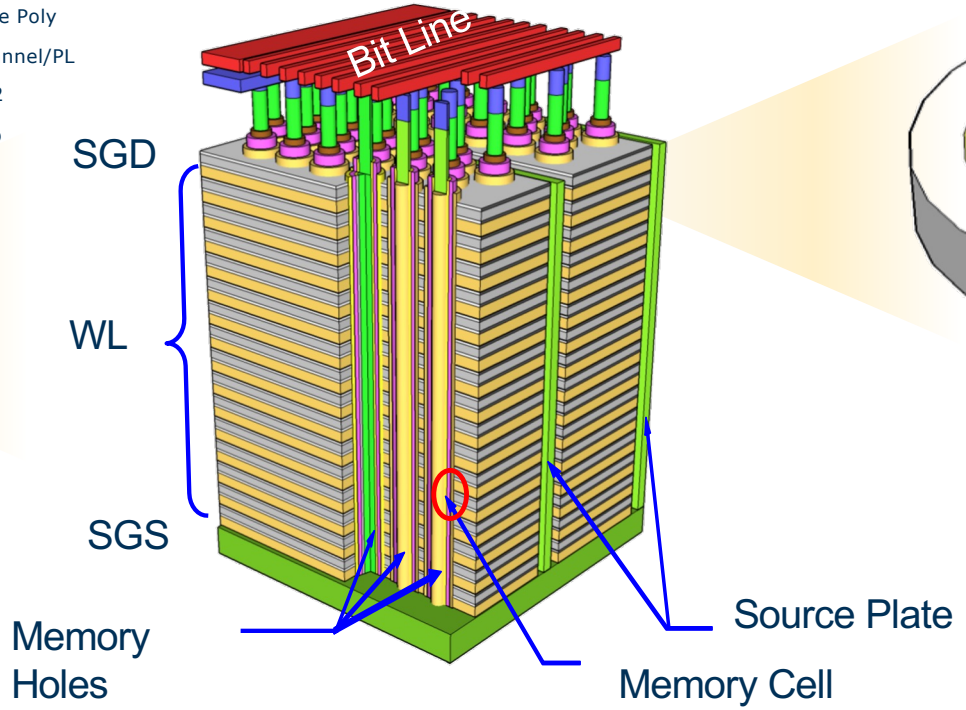
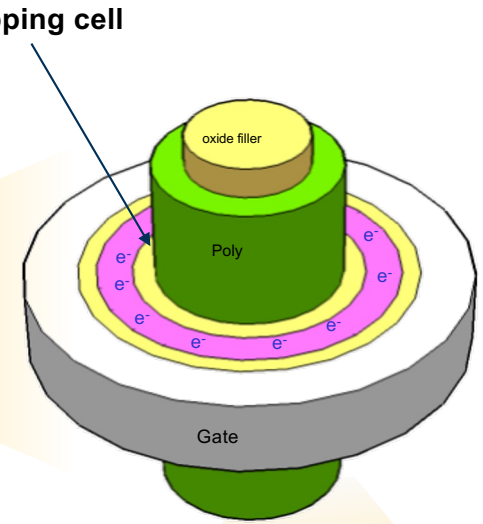
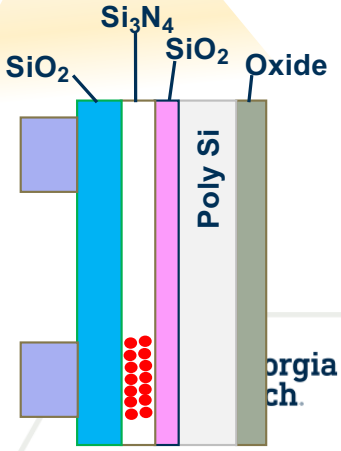
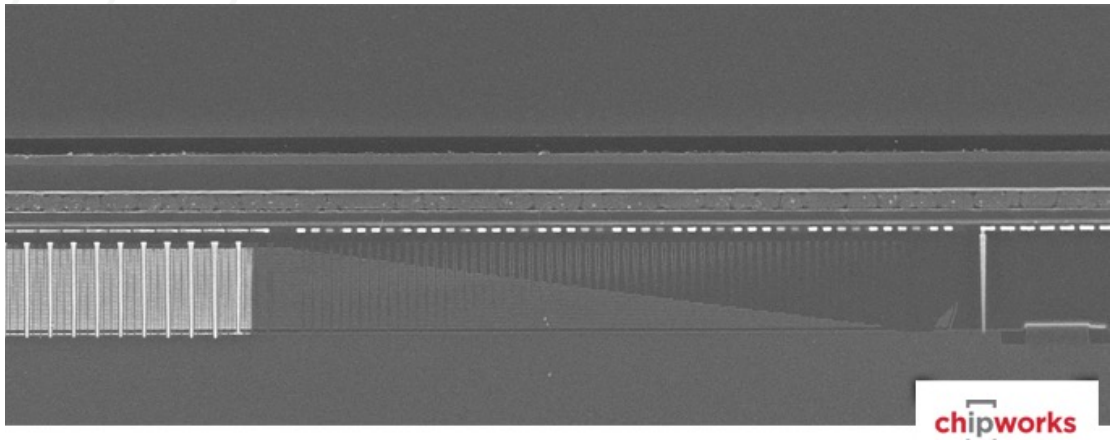
How to pack 50 Trillion Transistors – Vertical NAND



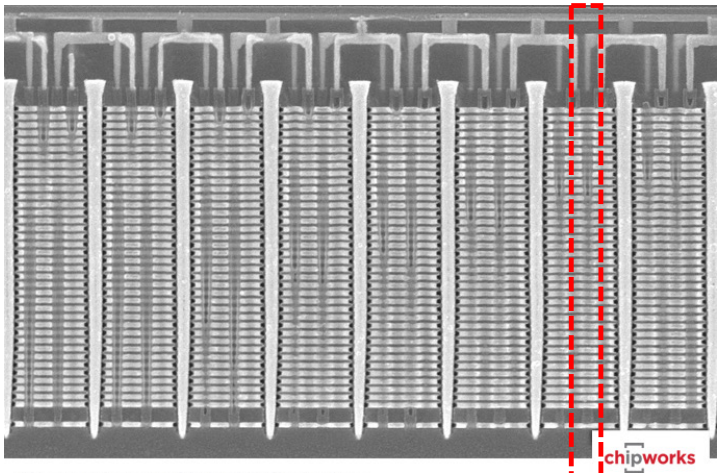


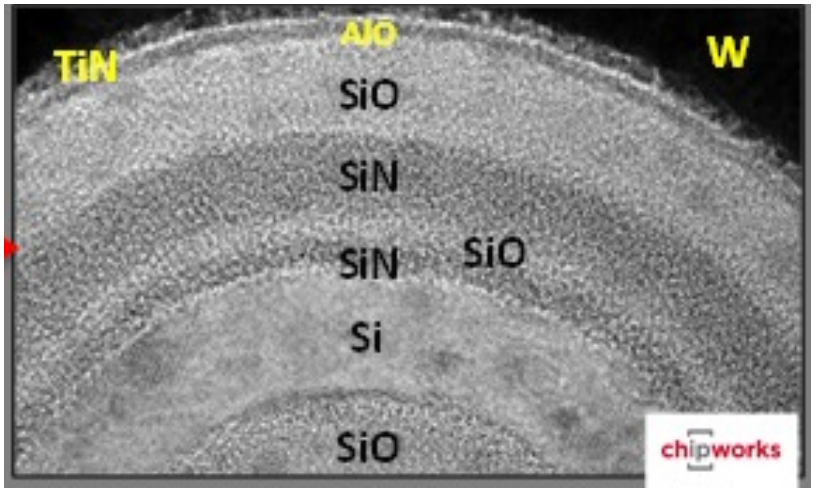


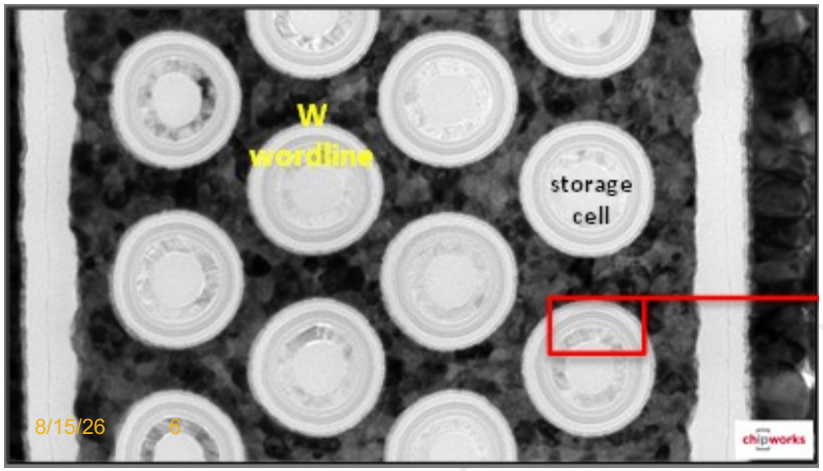
Bit Cost Scalable (BiCS) Architecture of Vertical NAND



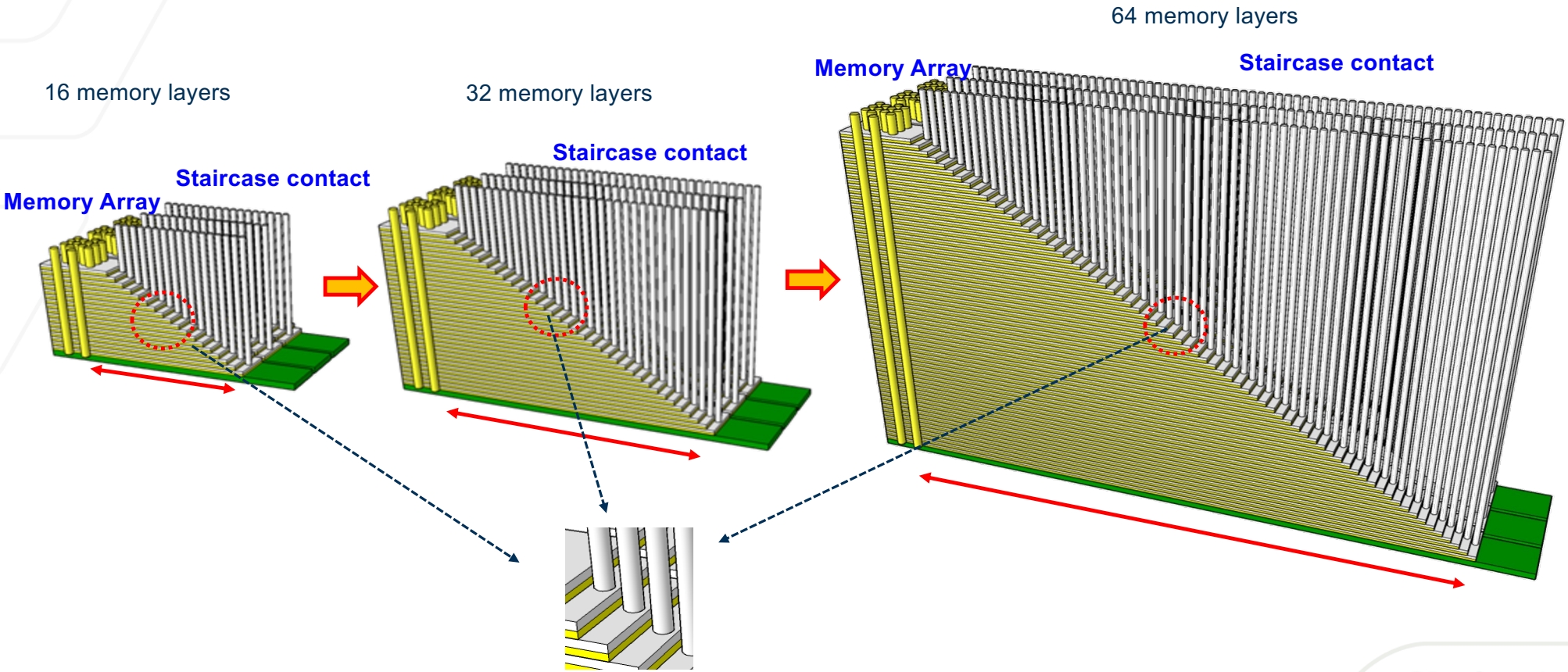
SEM cross-section of Samsung V-NAND stack







Bit Cost Scalable (BiCS) Architecture of Vertical NAND



C. Lu (Macronix), *et al.*, "3D Non-Volatile Memories for Terabit Era", *International Symposium on Nonvolatile Memory, Taiwan* 2017

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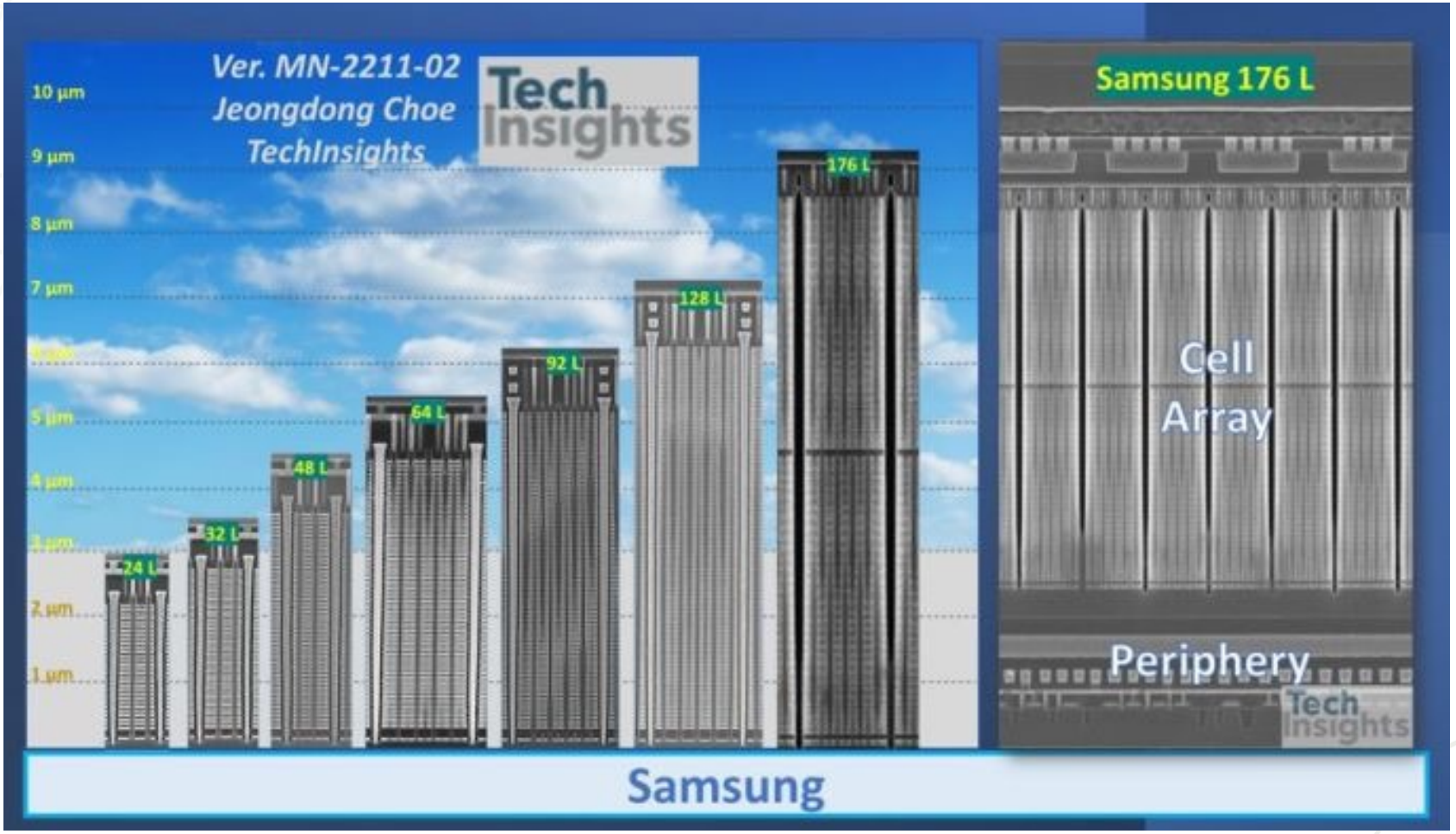
Evolution of Vertical NAND technology



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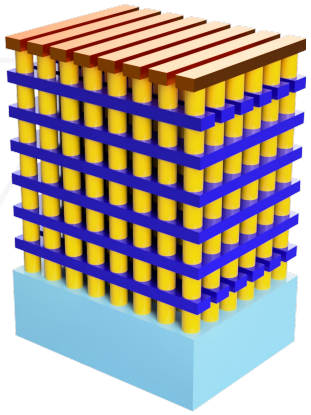
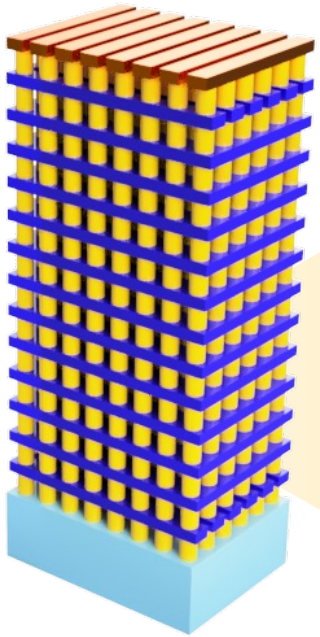
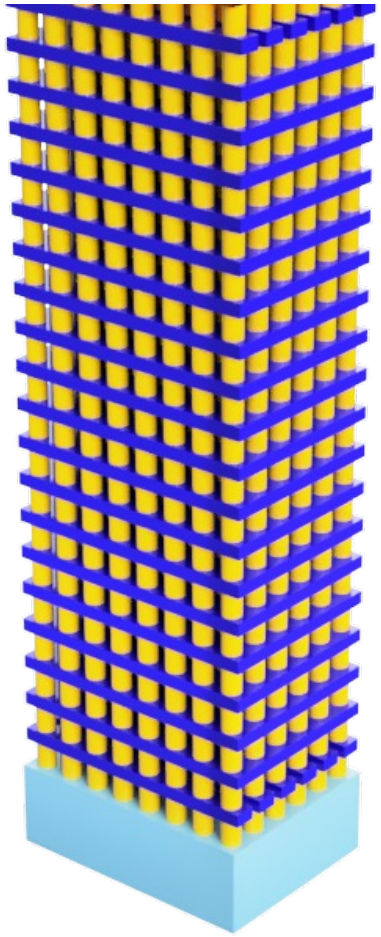
Evolution of vertical NAND Technology



2014
First 3D NAND, Samsung
24 Layers, MLC



2022-2025
Samsung 236L TLC
SK Hynix 238L TLC
Micron 232L TLC
192L QLC



2030
?

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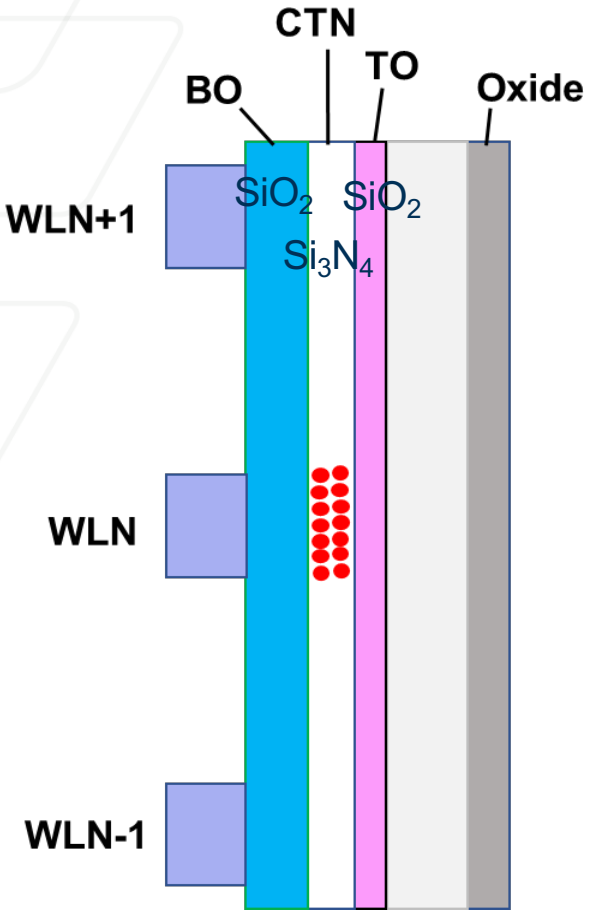
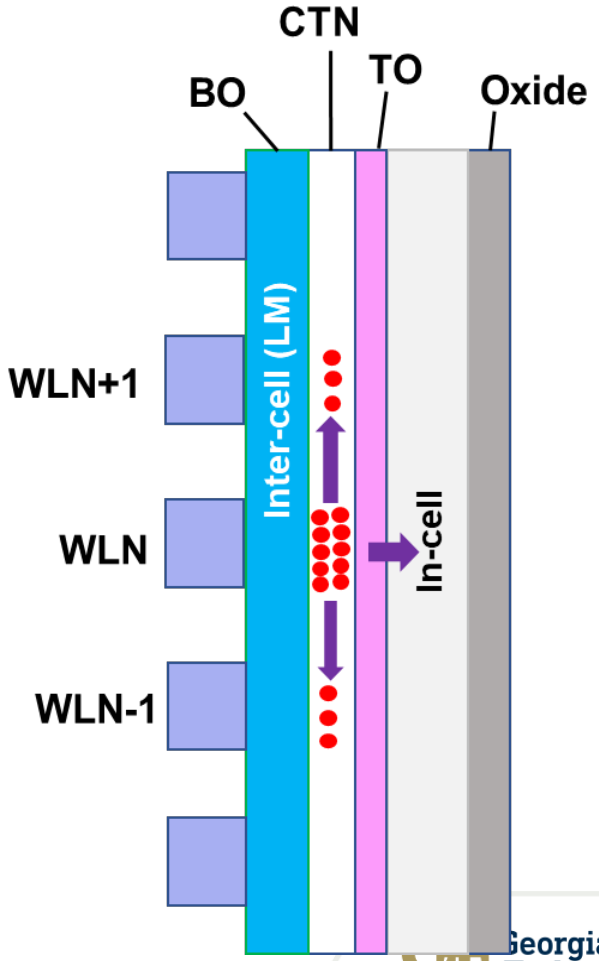
Challenges of vertical NAND flash scaling



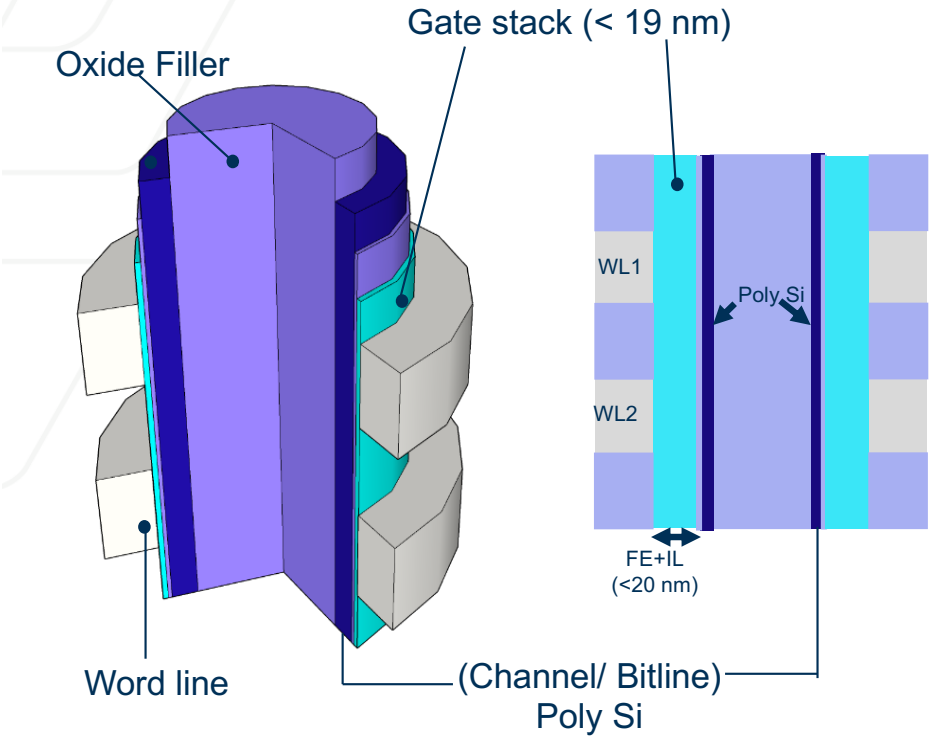
Z-scaling

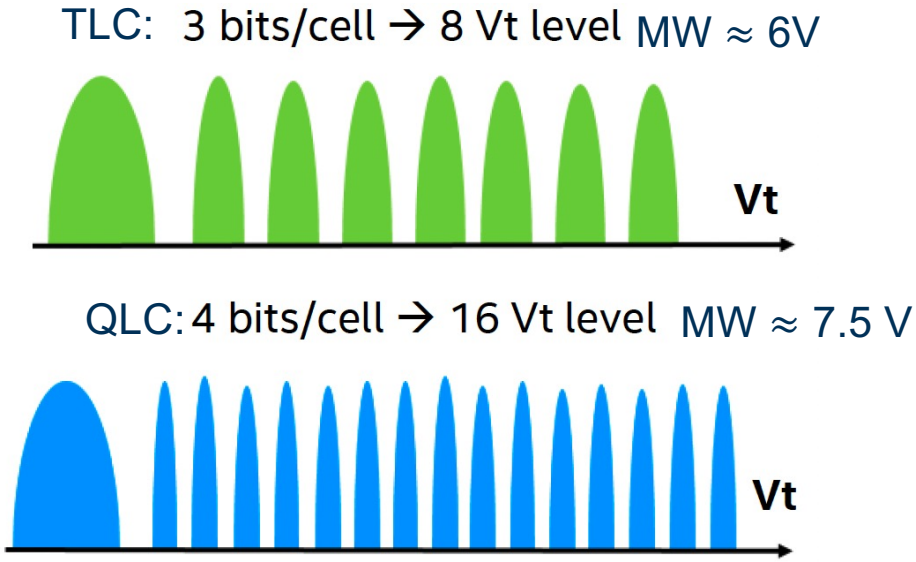
1. Lateral charge migration
2. Inter-WL reliability
3. High write voltage
4. Endurance
5. Device-device variation



13

The future of NAND flash technology





To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm

Design constraints

Gate stack thickness, $t \leq 19$ nm

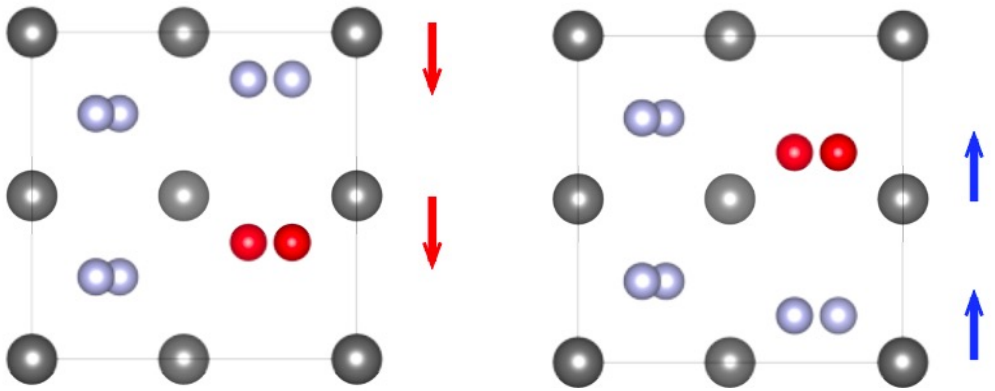
Write voltage ≤ 15 V

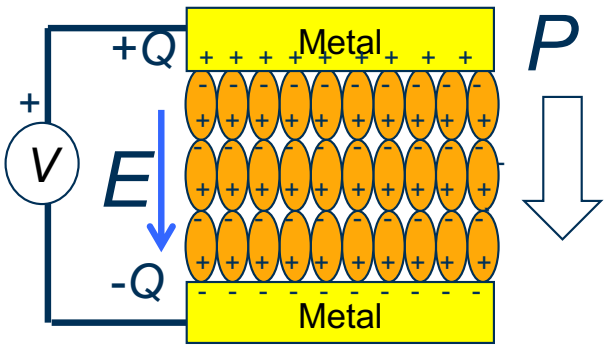
Memory window, MW ≥ 6.5 V

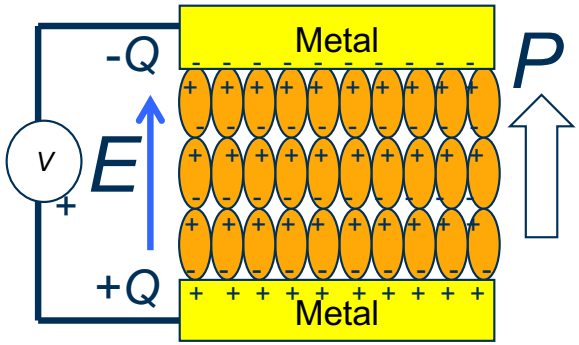
Ferroelectricity

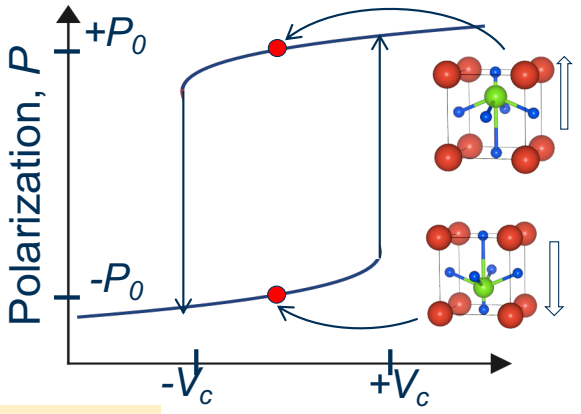
CMOS compatible HfO_2-based fluorite-structure ferroelectric

Orthorhombic *Pca2₁* structure









A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

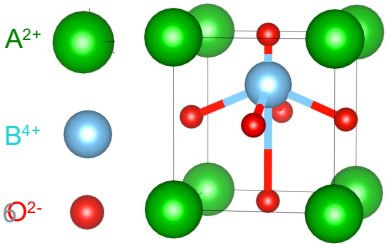
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for for code storage in microcontrollers.

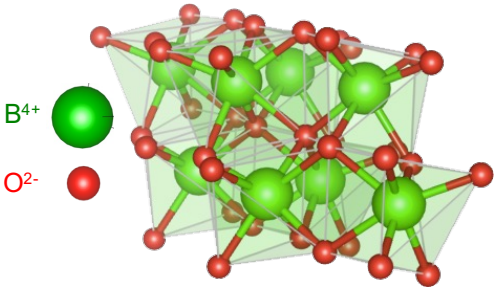
2. Controlled annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al. Appl. Phys. Lett*. 99, 112904 (2011)
- Boscke *et al. 2011 IEEE Int. Electron Devices Meeting.* p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al. Nano Lett.* 12, 4318 (2012)

Perovskite-structure ferroelectric oxide (ABO_3)



Fluorite-structure ferroelectric oxide (BO_2)



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2011→2023

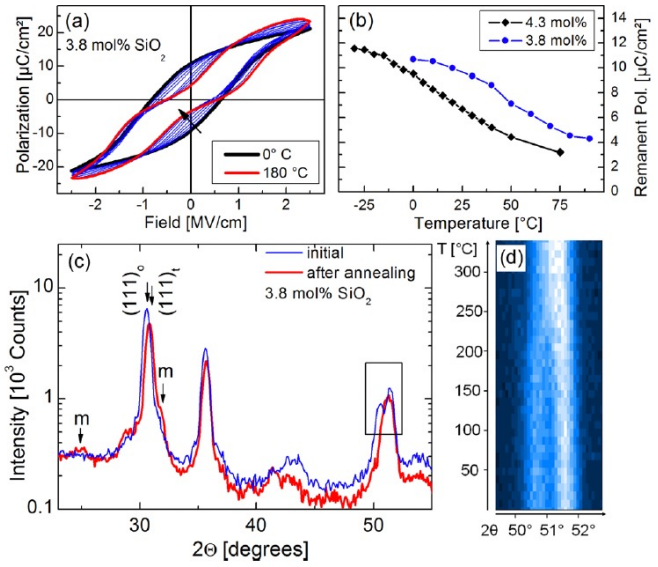
Discovery of Ferroelectricity in HfO2

APPLIED PHYSICS LETTERS **99**, 112904 (2011)

Phase transitions in ferroelectric silicon doped hafnium oxide

T. S. Böscke,[1,2,a),b)] St. Teichert,[3,b)] D. Bräuhaus,[4] J. Müller,[5] U. Schröder,[2,b)] U. Böttger,[4] and T. Mikolajick[2,6]
[1]*Löberwallgraben 2, 99096 Erfurt, Germany*
[2]*Namlab gGmbH, 01187 Dresden, Germany*
[3]*UAS Jena, Department of SciTec, 07745 Jena, Germany*
[4]*RWTH Aachen, Institut für Werkstoffe der Elektrotechnik, 52062 Aachen, Germany*
[5]*Fraunhofer Center Nanoelectronic Technologies (CNT), 01099 Dresden, Germany*
[6]*Department of Nanoelectronic Materials, University of Technology Dresden, 01062 Dresden, Germany*

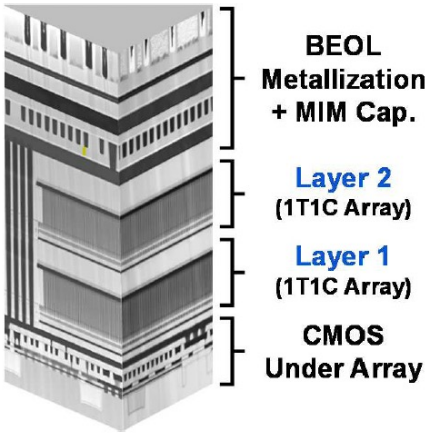
(Received 18 July 2011; accepted 19 August 2011; published online 15 September 2011)

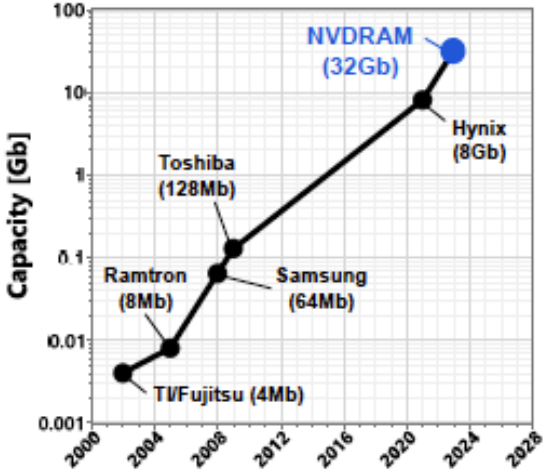


Demonstration of high-density Ferroelectric RAM

NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads

N. Ramaswamy, A. Calderoni, J. Zahurak, G. Servalli, A. Chavan, S. Chhajed, M. Balakrishnan, M. Fischer, M. Hollander, D. P. Ettisserry, A. Liao, K. Karda, M. Jerry, M. Mariani, A. Visconti, B. R. Cook, B. D. Cook, D. Mills, A. Torsi, C. Mouli, E. Byers, M. Helm, S. Pawlowski, S. Shiratake, and N. Chandrasekaran
Micron Technology Inc., Boise, USA, email: dramaswamy@micron.com





Ramaswamy et al. IEDM 2023

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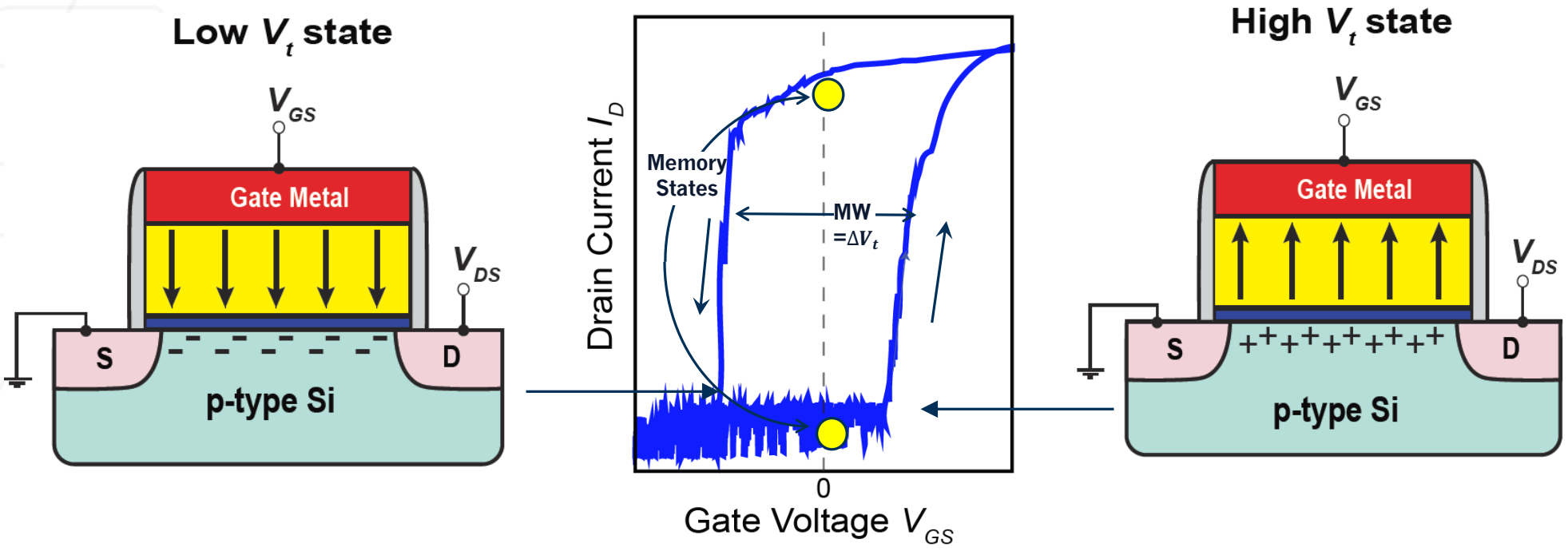
Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the "remnant" polarization.

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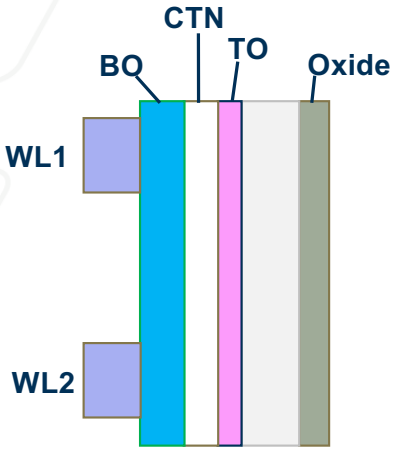
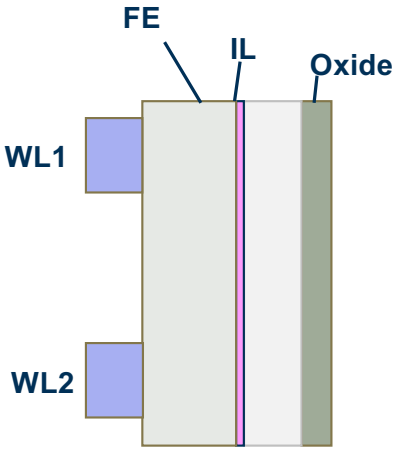
Charge trap flash vs. ferroelectric flash





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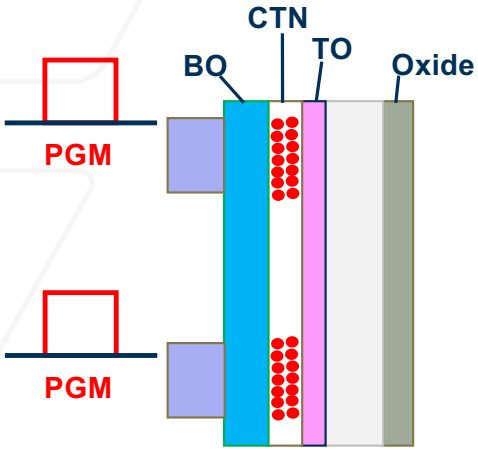
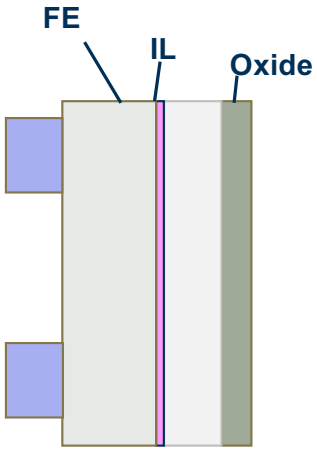
Charge trap flash vs. ferroelectric flash





CTF that stores data in the form of charge

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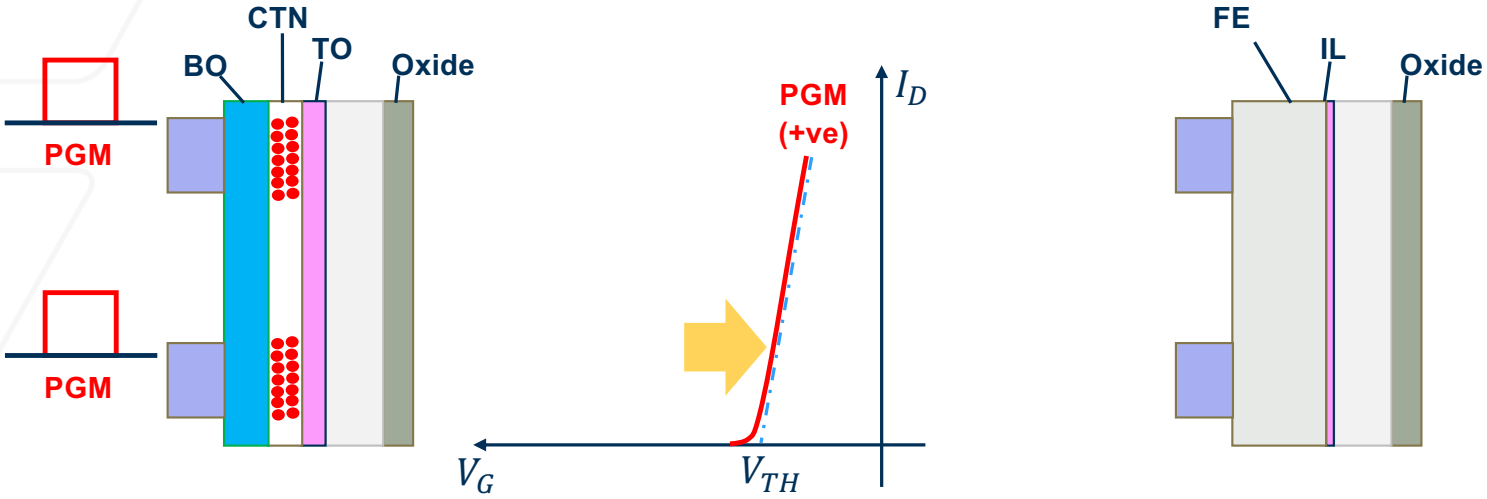
Charge trap flash vs. ferroelectric flash



Positive PGM pulse sets the Vt to high Vt state in CTF

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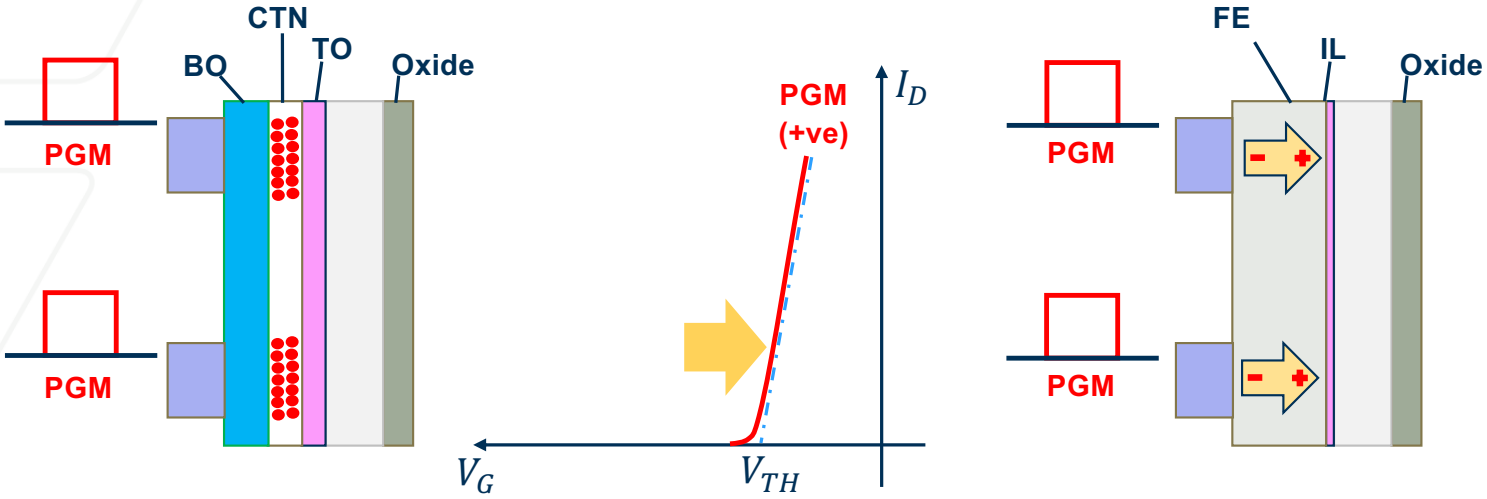
Charge trap flash vs. ferroelectric flash



Positive PGM pulse sets the Vt to high Vt state in CTF

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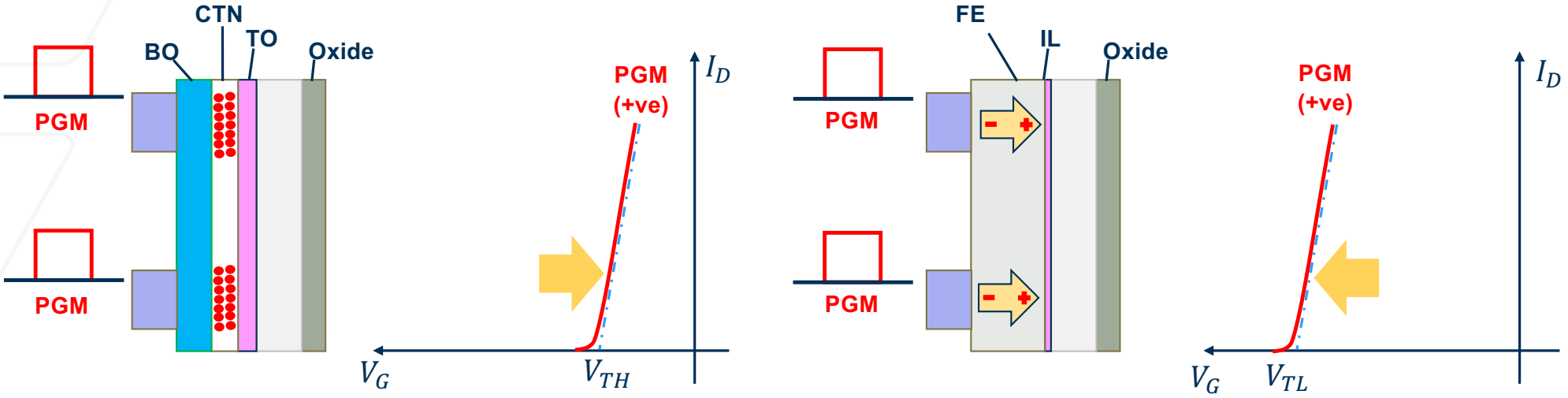
Charge trap flash vs. ferroelectric flash



On the contrary, Positive PGM pulse sets the Vt to low Vt state in FEFET

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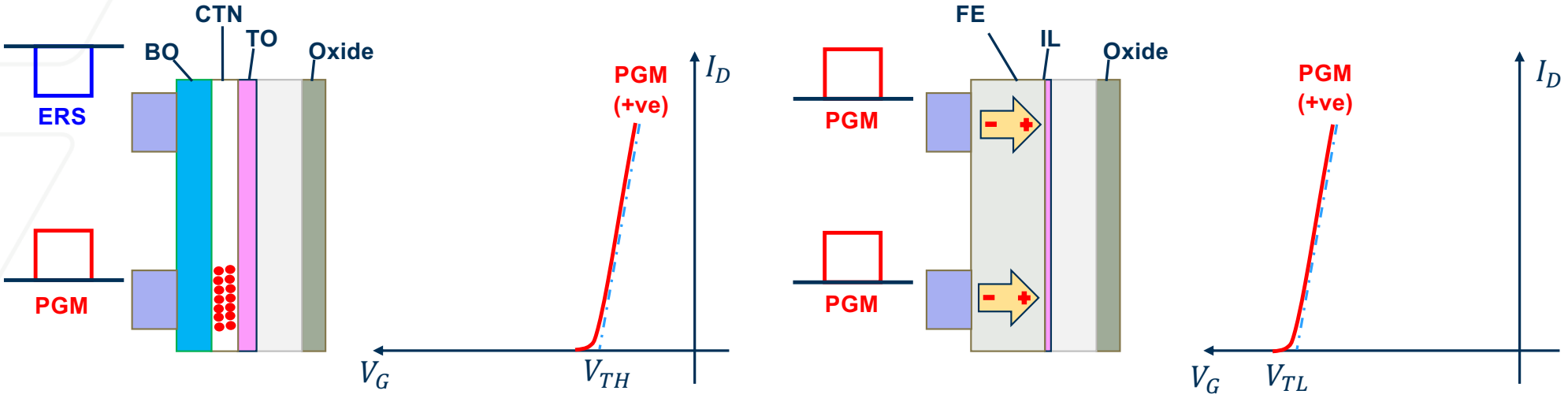
Charge trap flash vs. ferroelectric flash



Negative ERS pulse sets the Vt to low Vt state in CTF

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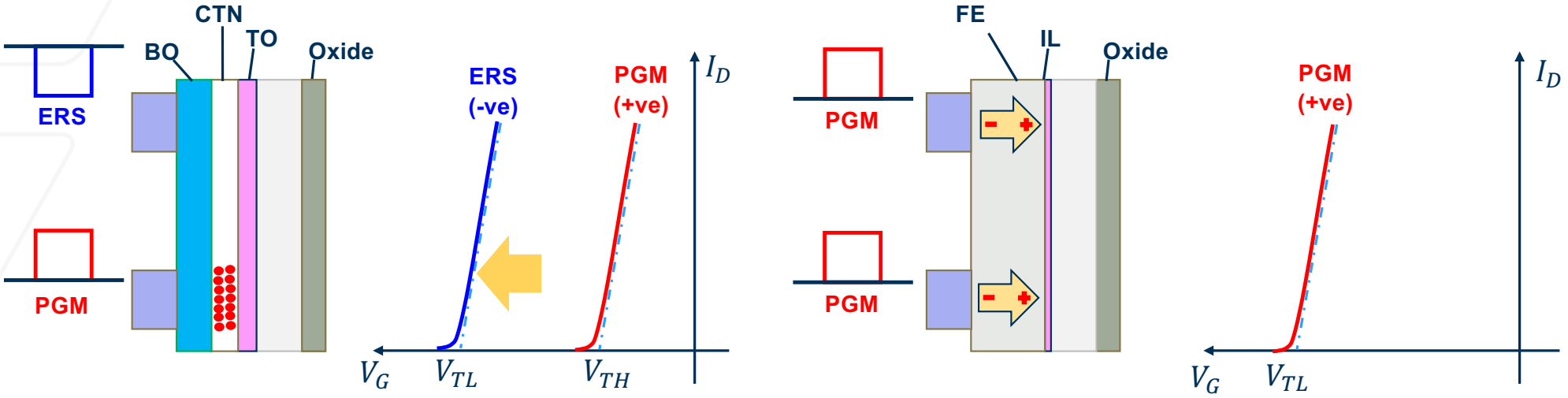
Charge trap flash vs. ferroelectric flash



Negative ERS pulse sets the Vt to low Vt state in CTF

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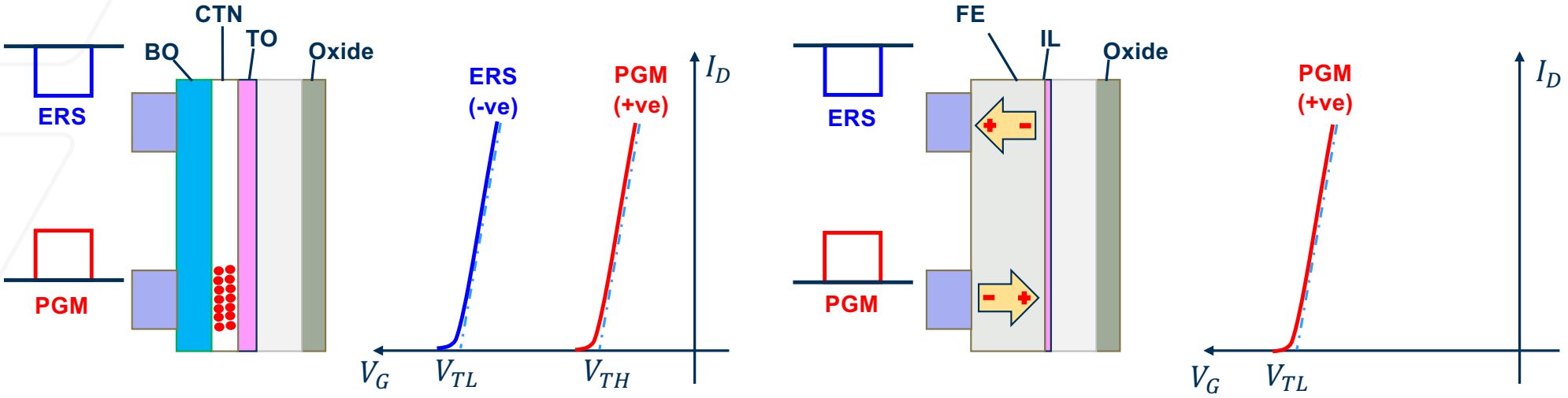
Charge trap flash vs. ferroelectric flash



Negative ERS pulse sets the Vt to high Vt state in FEFET

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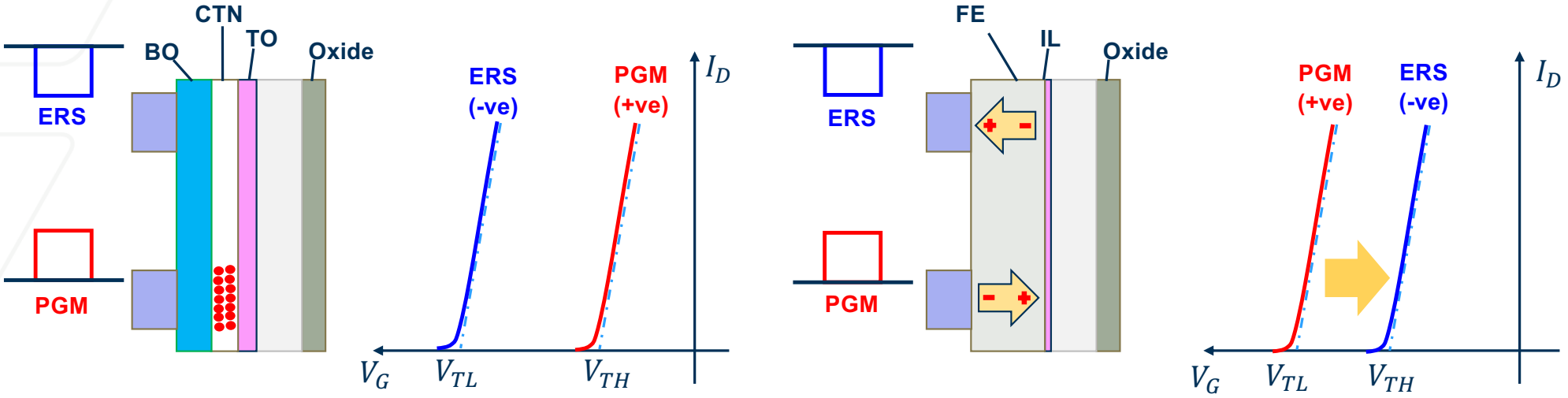
Charge trap flash vs. ferroelectric flash



Negative ERS pulse sets the Vt to high Vt state in FEFET

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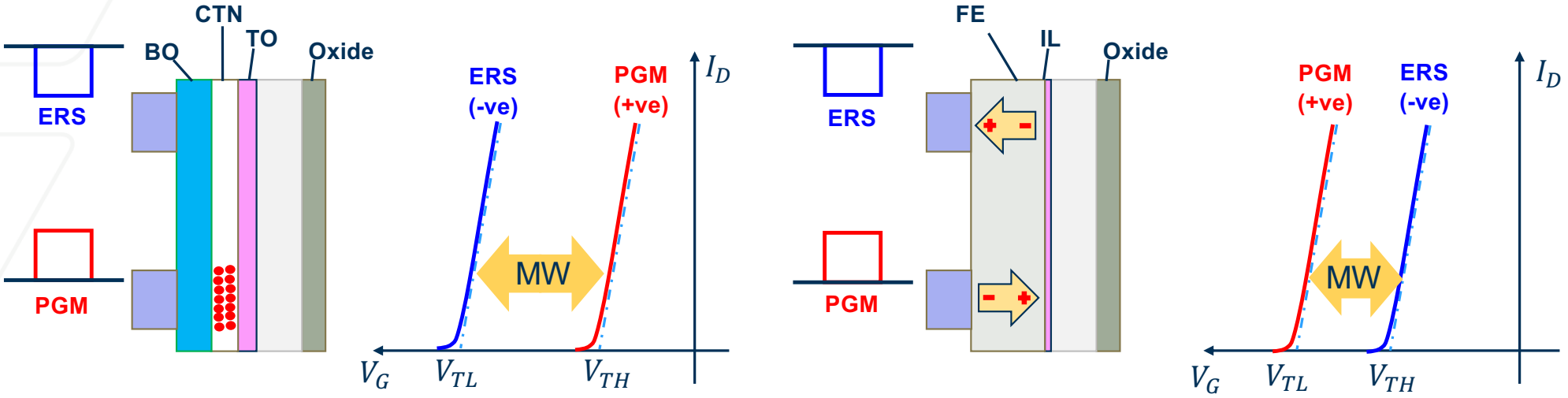
Charge trap flash vs. ferroelectric flash



$$MW = V_{TH} - V_{TL}$$

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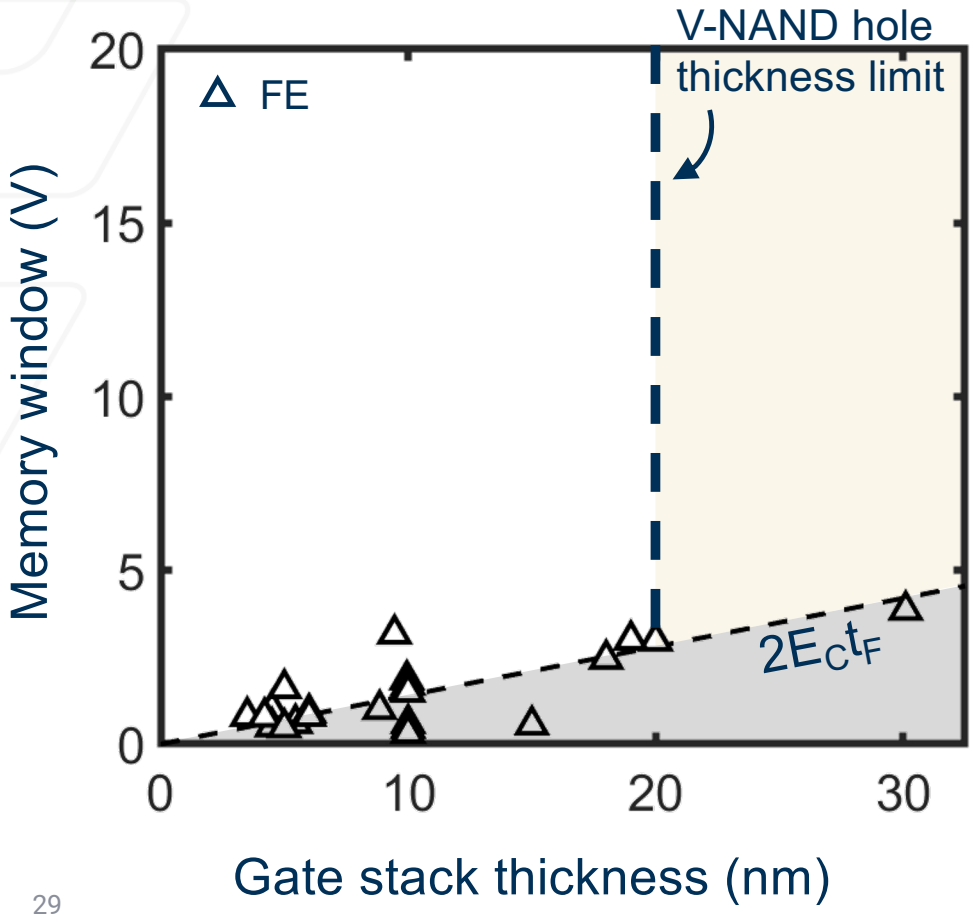
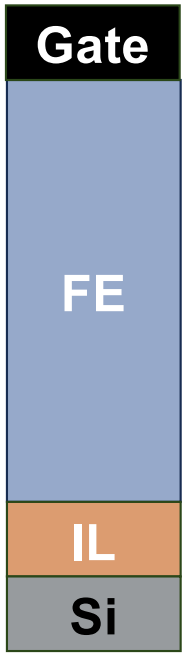
Memory window of FEFETs is limited by V_C



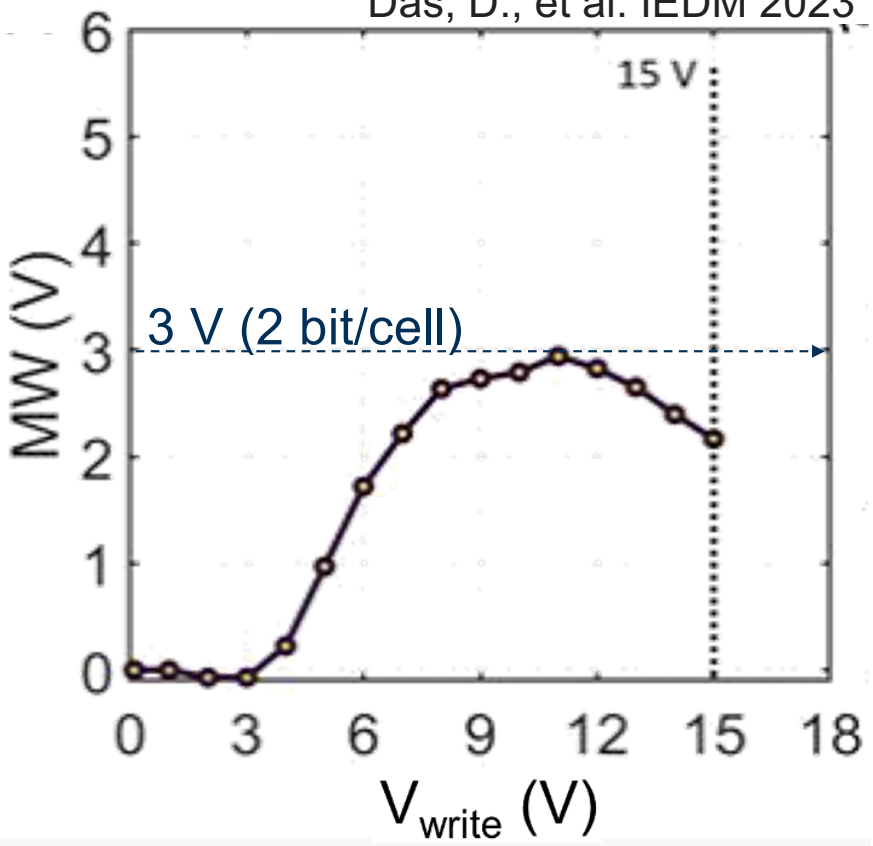


$$\mathrm{MW} \leq 2V_c = 2E_c \times t_f$$

The maximum memory window of an FeFET is theoretically limited by the memory window of the ferroelectric layer.

Increasing the MW by dielectric insertion

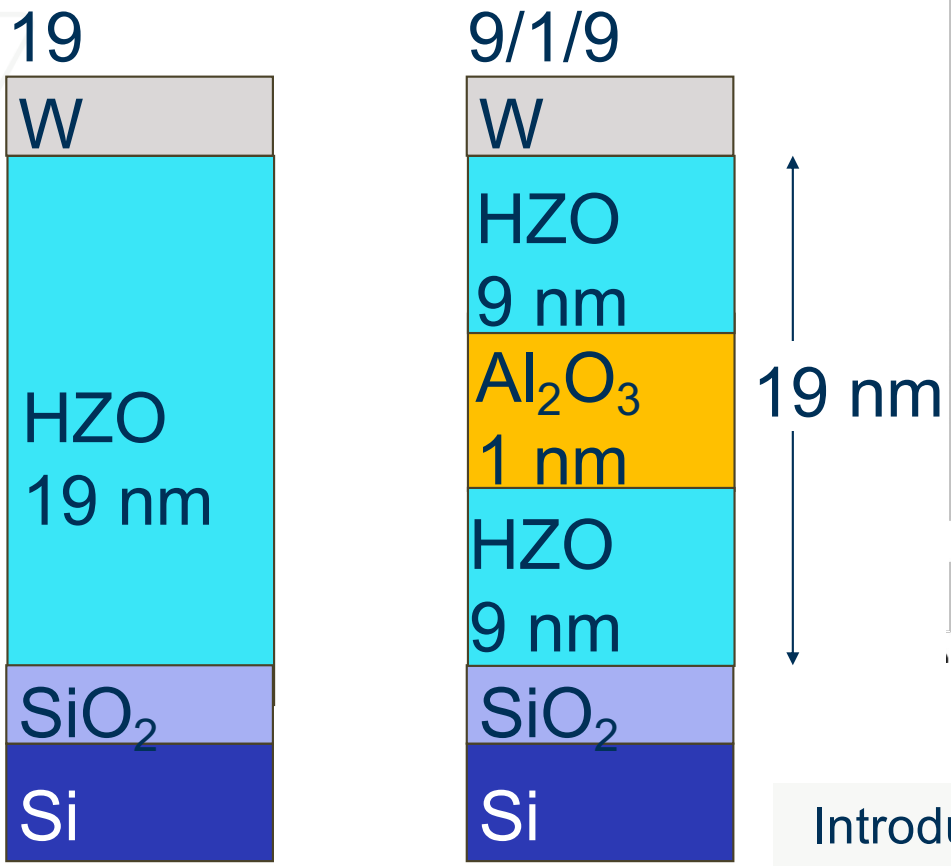
Das, D., et al. IEDM 2023

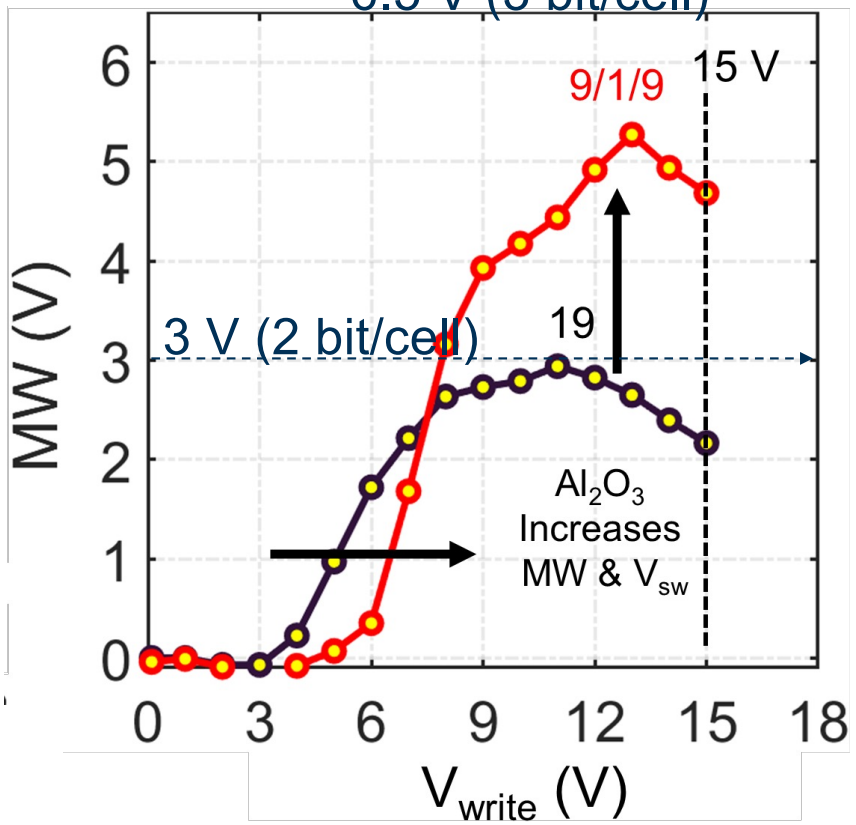


10 nm HZO layer leads to maximum memory window of 2.9 V.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion

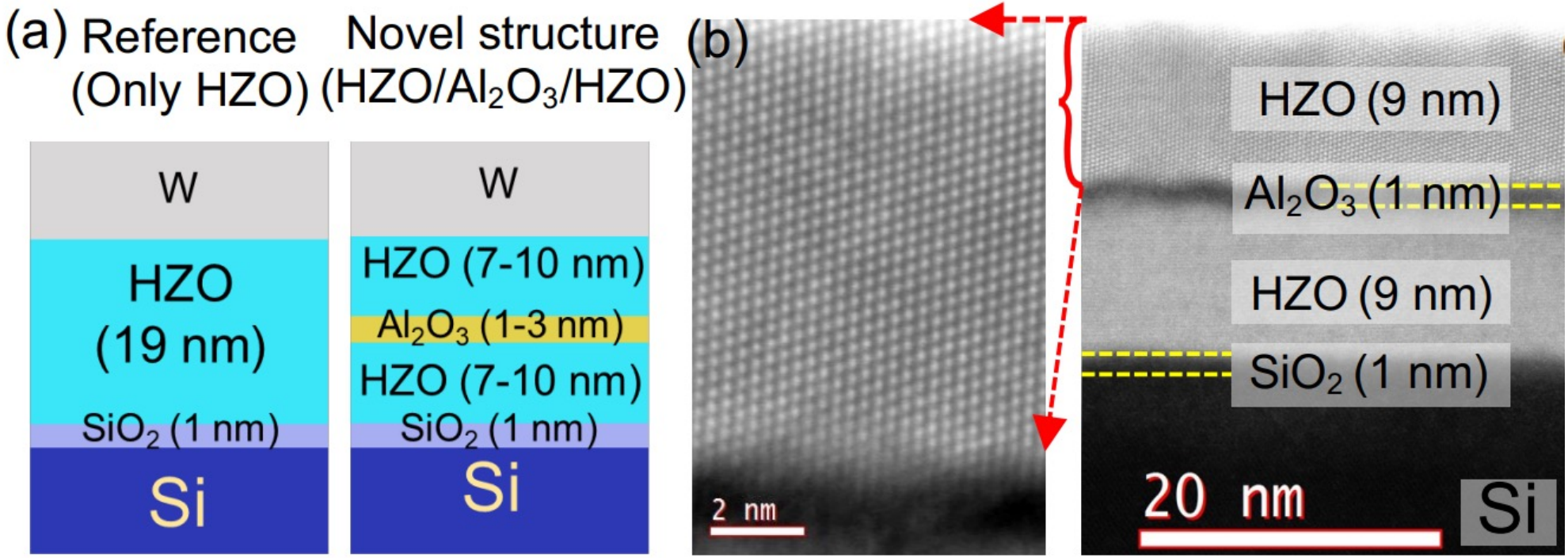




Introducing 1 nm Al_2O_3 intermediate layer dramatically memory window to 5.3 V.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion



A homogeneous 1 nm Al_2O_3 TDL is clearly visible in the HRTEM image suggesting the formation of Al_2O_3 interlayer with uniform thickness and full coverage

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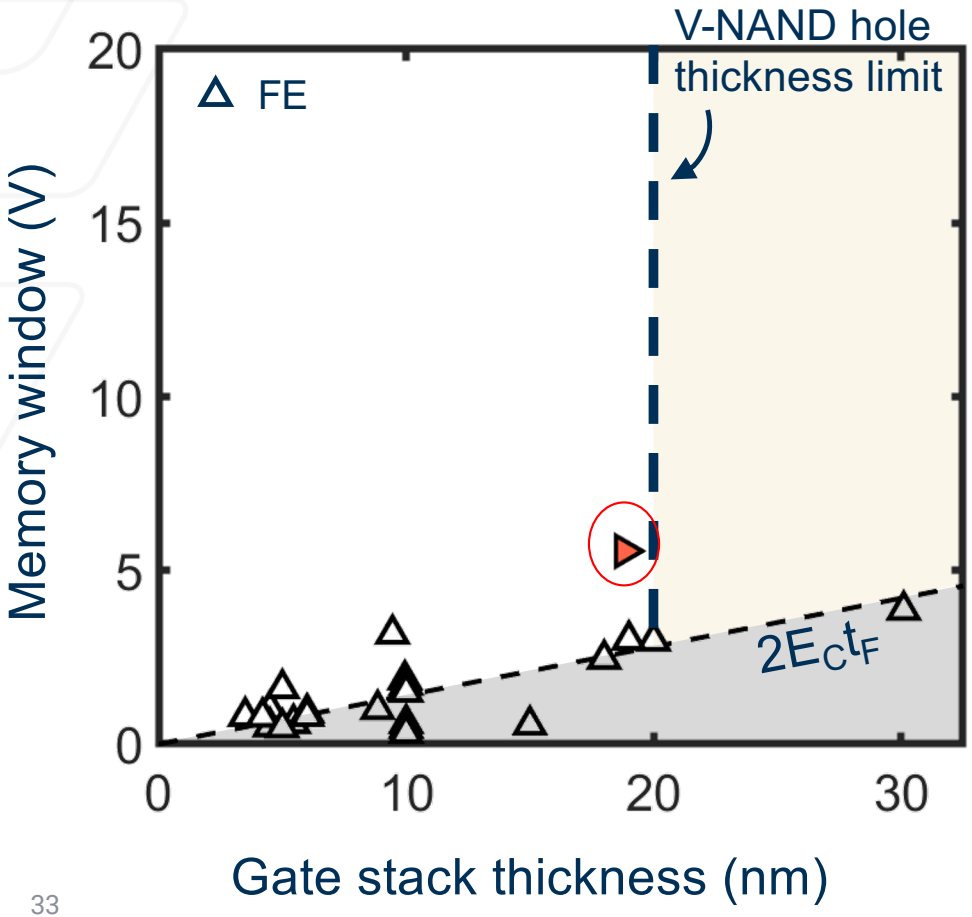
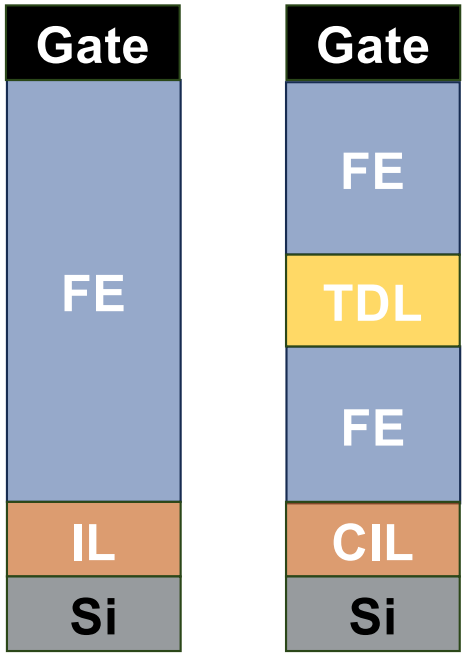
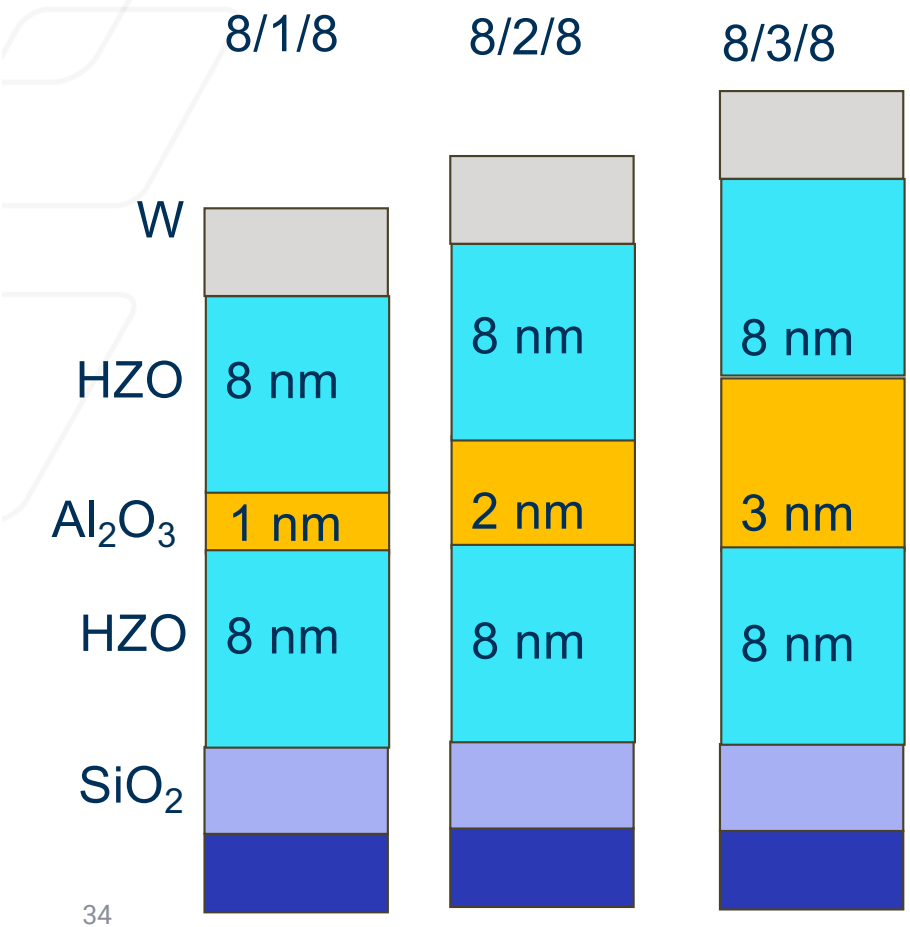
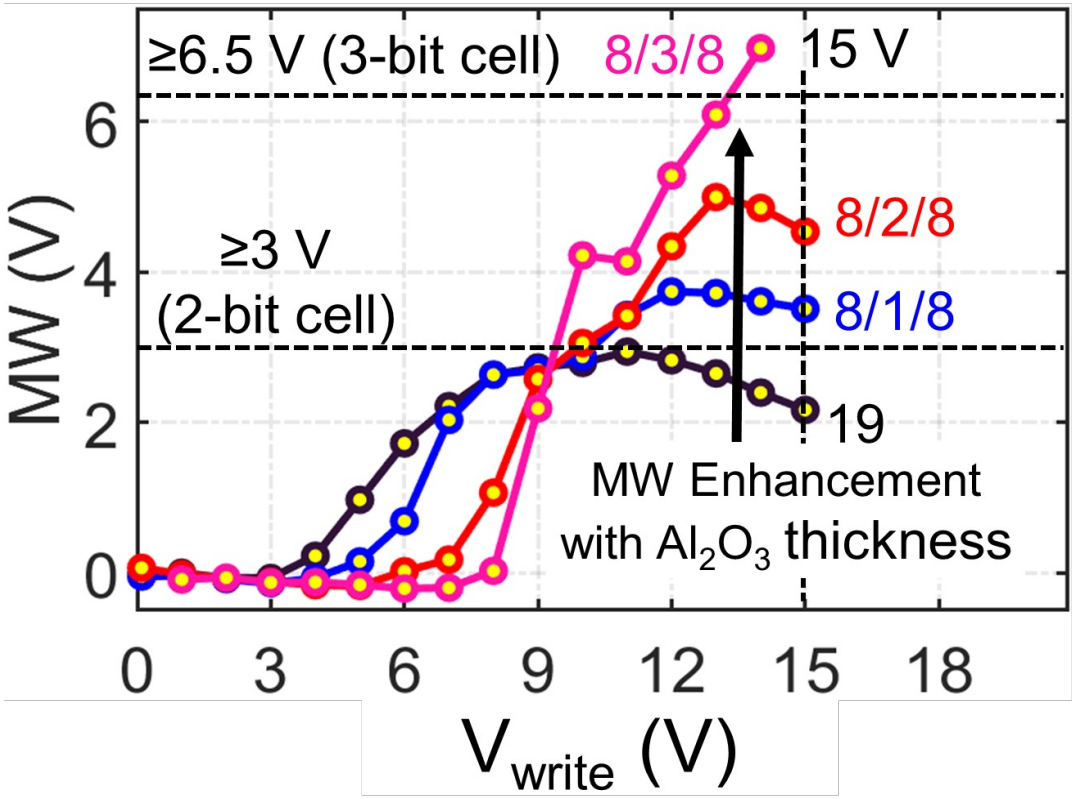
Memory window of FEFETs is limited by V_C





Increasing the MW by dielectric insertion

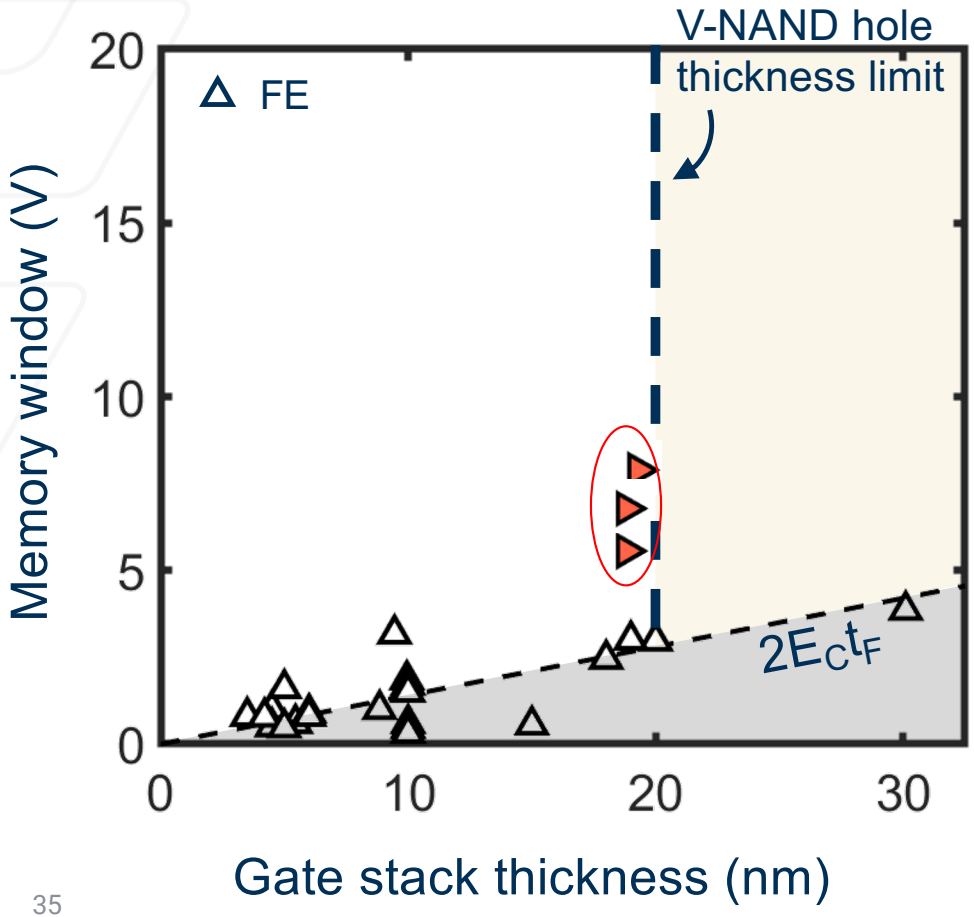


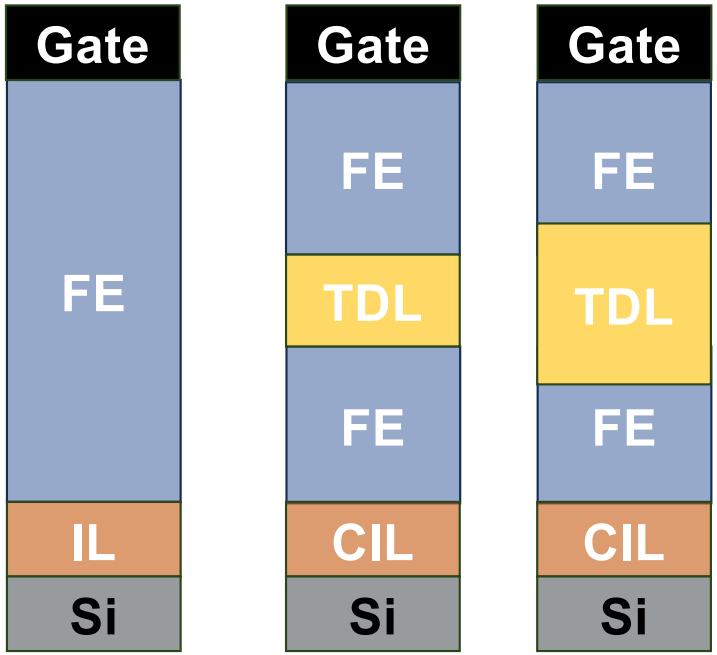


FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

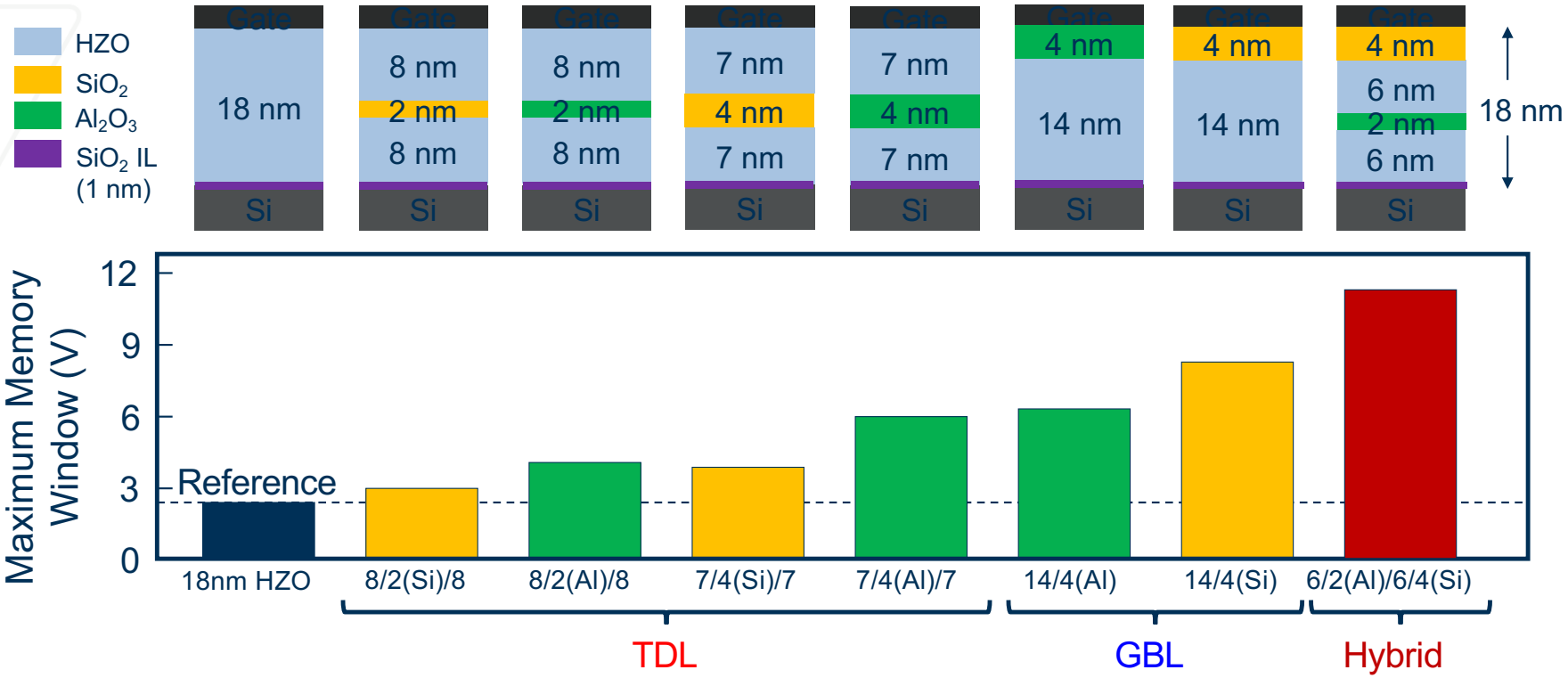
Increasing the MW by dielectric insertion





Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Position and choice of the dielectric



- GBL stacks have higher MW than TDL stacks for similar thickness and material.
- SiO_2 in GBL and Al_2O_3 in TDL gives higher MW for similar dielectric thickness

Fernandes, L., Ravindran, P. V., Song, T., Das, D., Park, C., Afroze, N., ... & Khan, A. (2024). Material choices for tunnel dielectric layer and gate blocking layer for ferroelectric NAND applications. *IEEE Electron Device Letters*.

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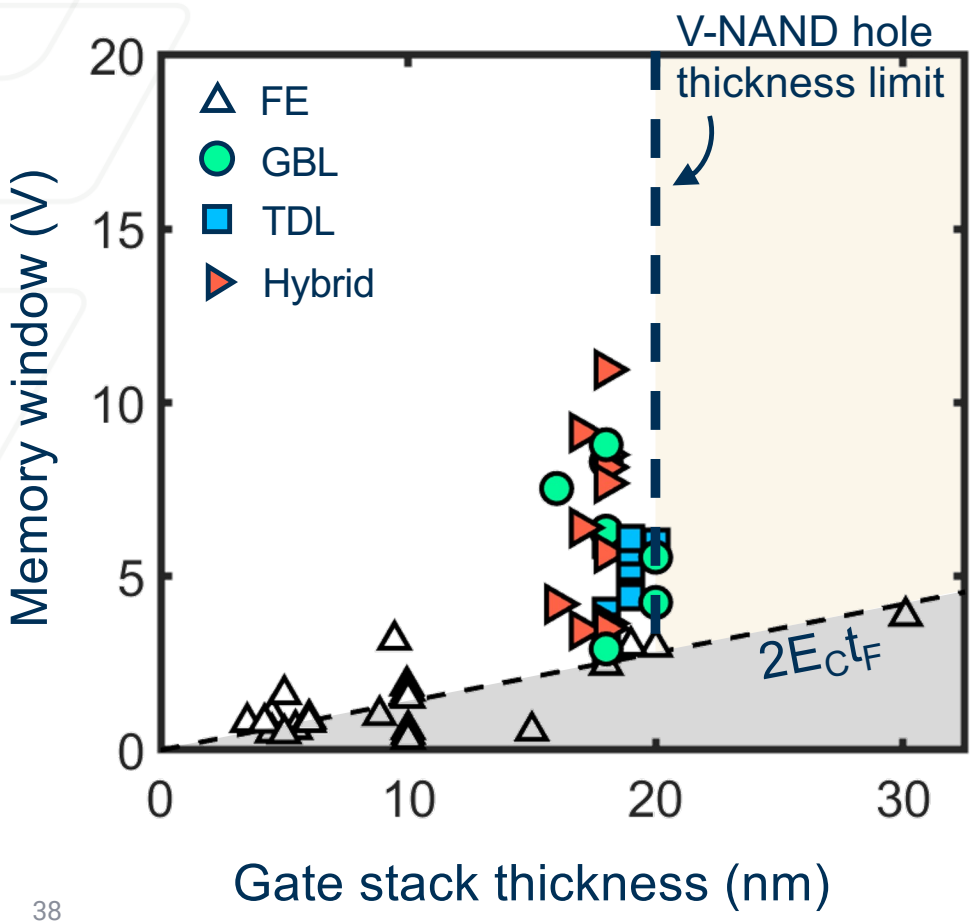
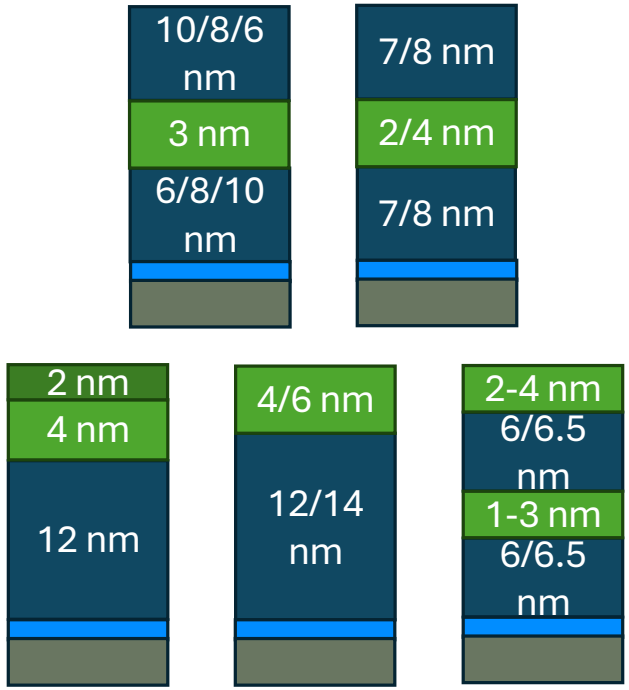
Increasing the MW by dielectric insertion

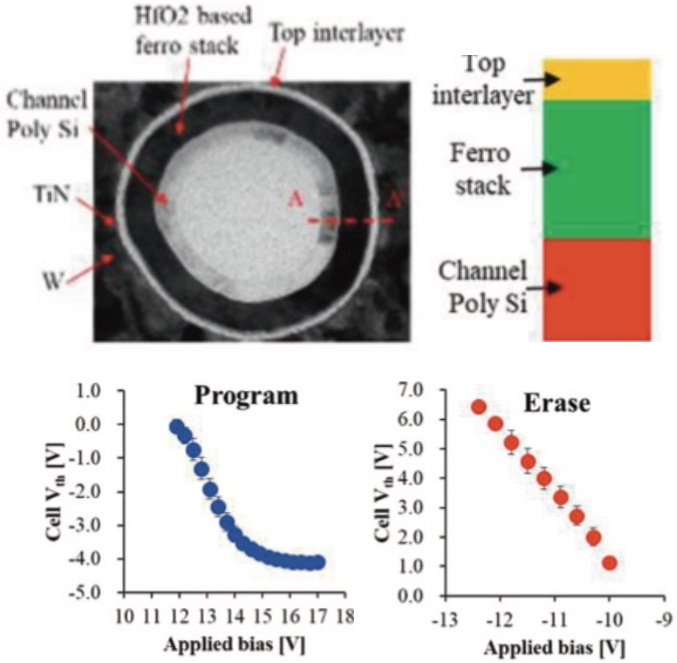




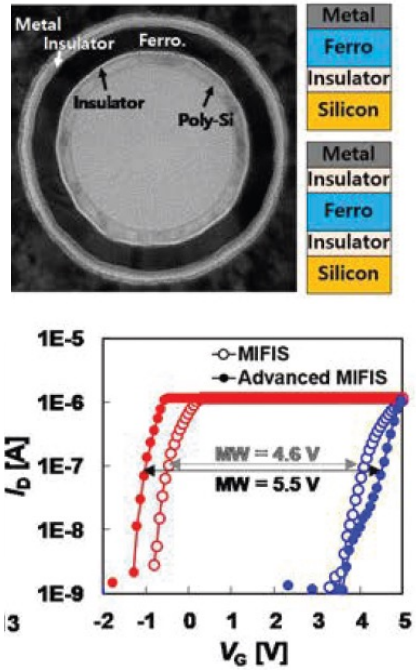
Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$
Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4
Channel IL: SiO_2
Semiconductor: Bulk Si, Poly Si, SOI, IWO

Increasing the MW by dielectric insertion

SK Hynix
Yoon et al. VLSI 2023



Samsung
Lim et al. IEDM 2023



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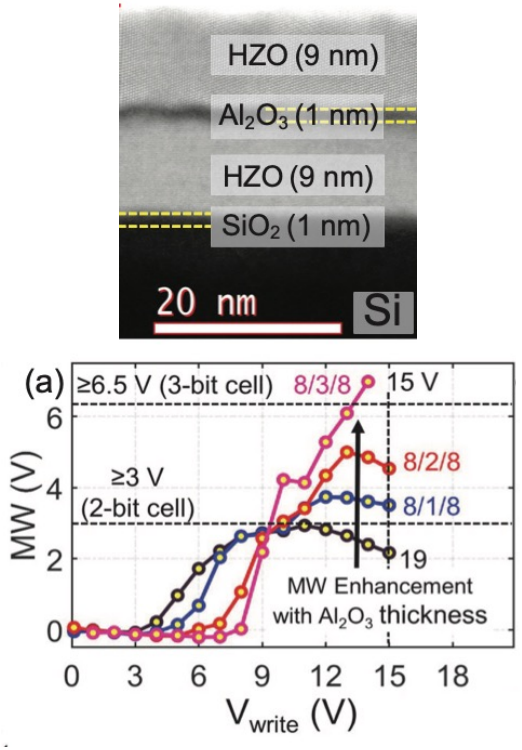
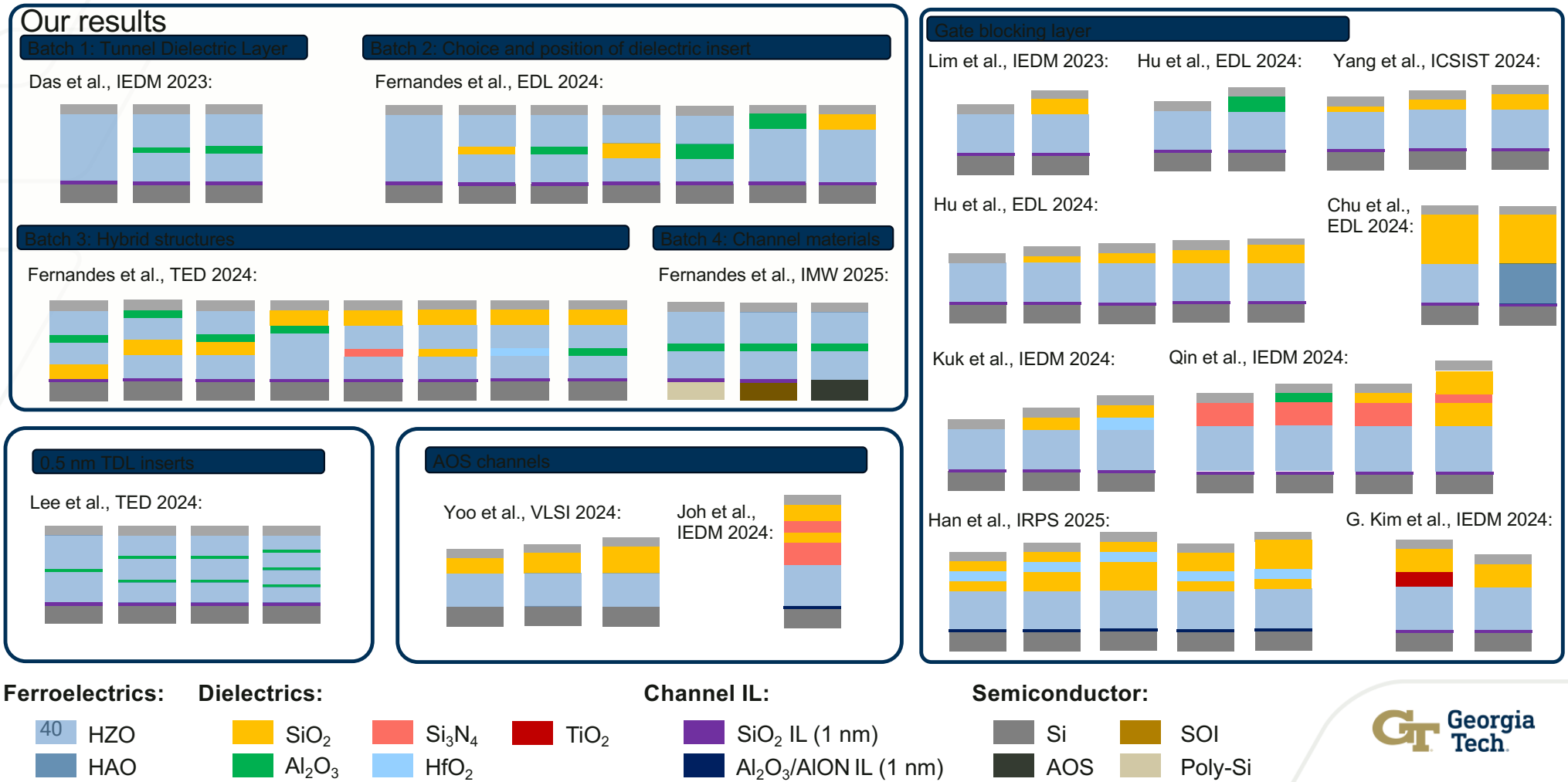
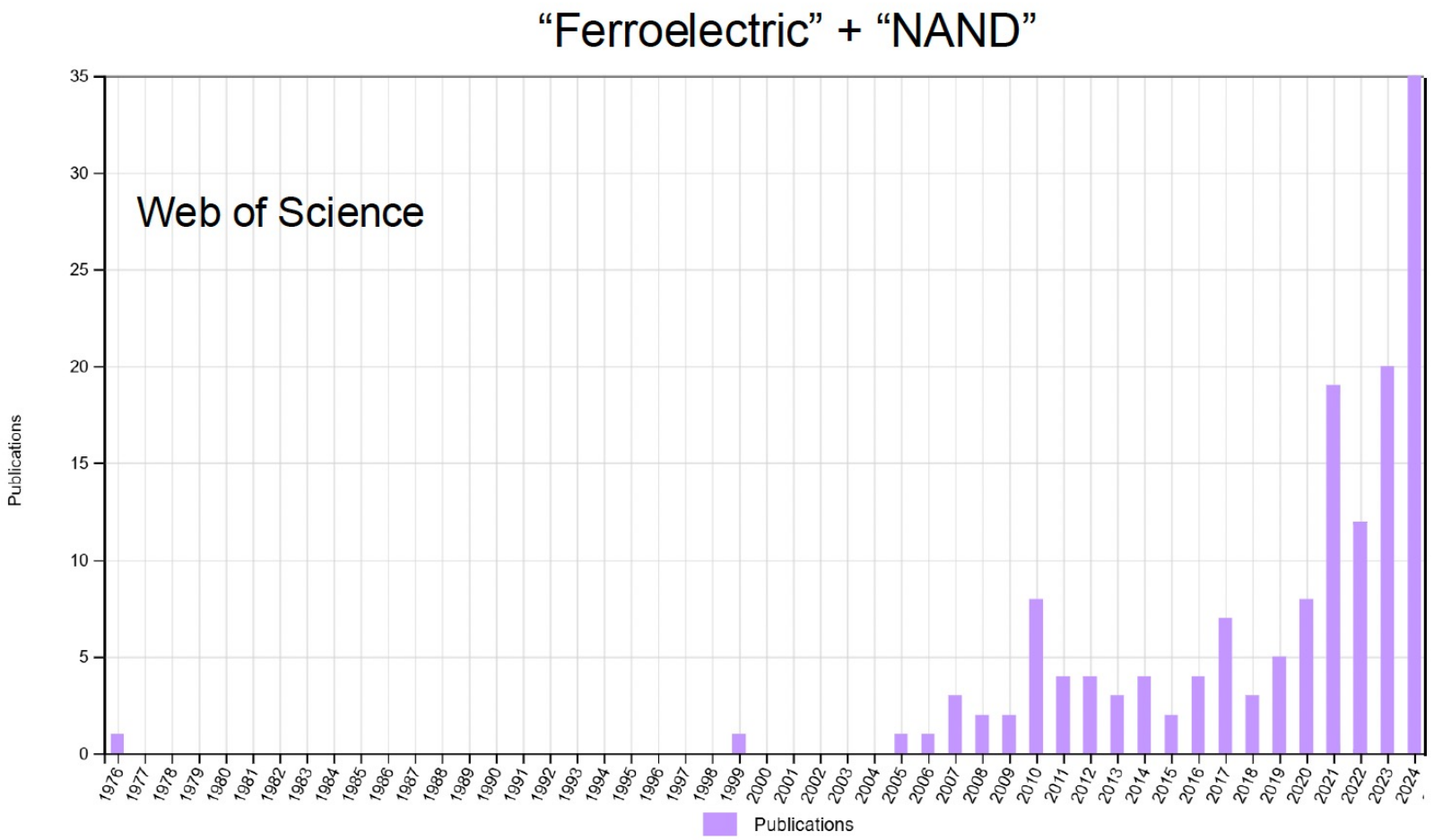
Das et al. IEDM 2023



Increasing the MW by dielectric insertion



An Active Area of Research – Ferroelectrics for V-NAND



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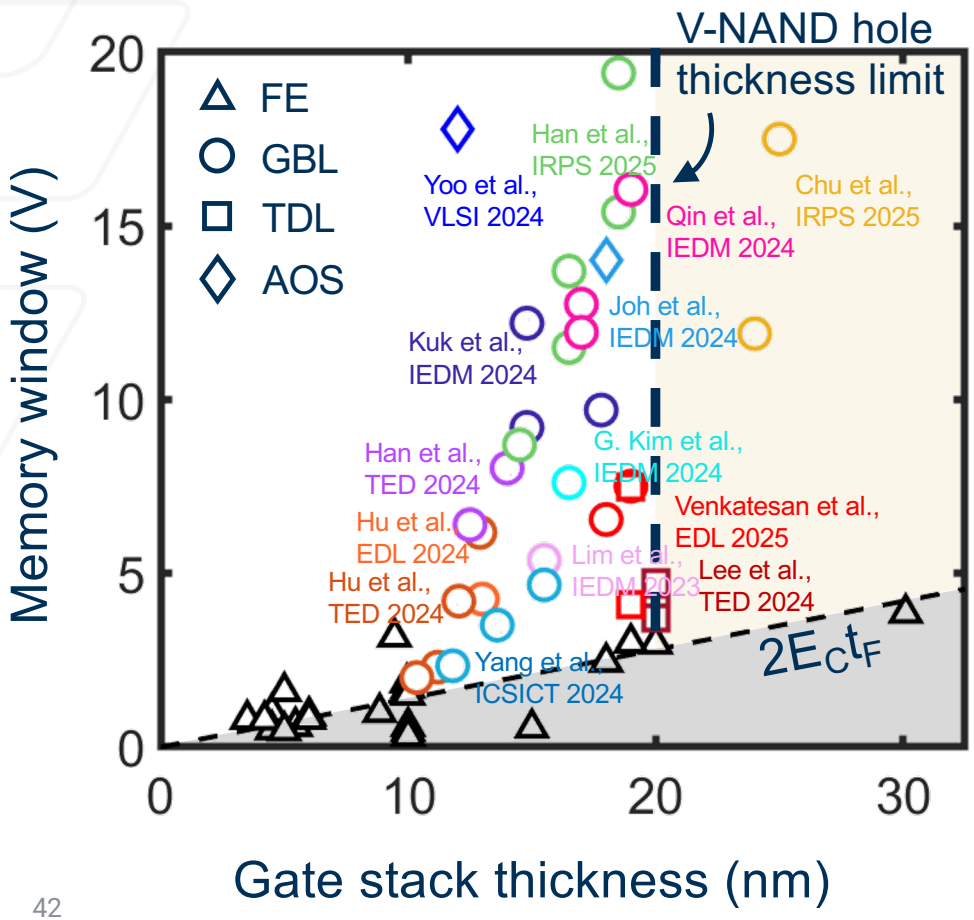
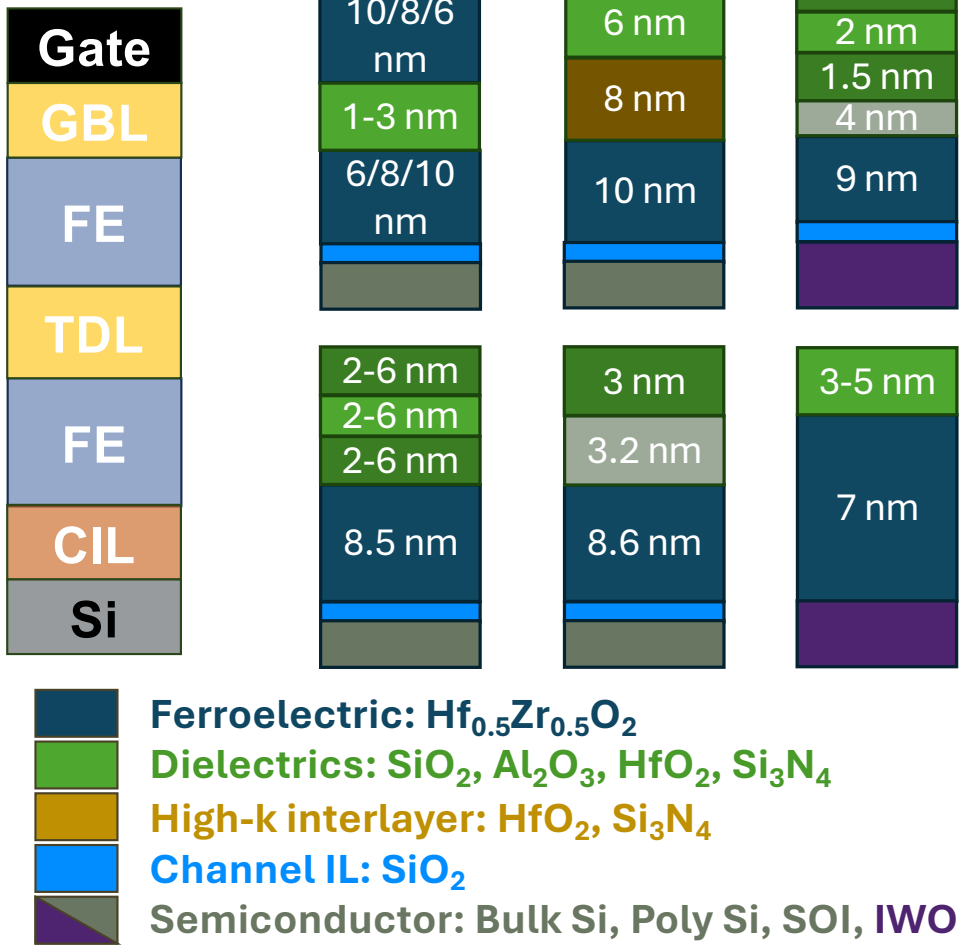
Increasing the MW by dielectric insertion





Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$

Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4

High-k interlayer: HfO_2, Si_3N_4

Channel IL: SiO_2

Semiconductor: Bulk Si, Poly Si, SOI, IWO

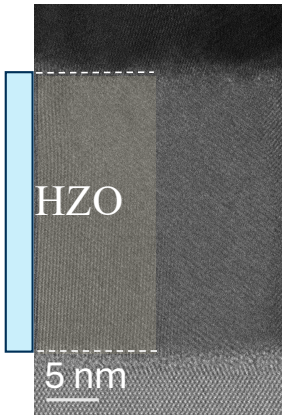
Key questions to address for ferroelectric NAND?

1. Retention
2. Disturb
3. Write endurance
4. Lateral charge migration
5. Device-device variation

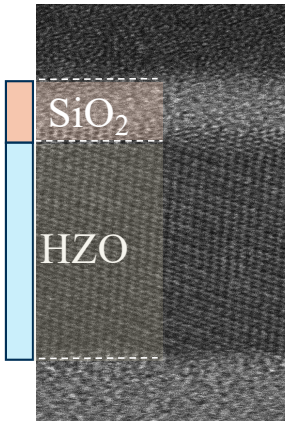
⋮

Ferroelectric NAND gate stacks

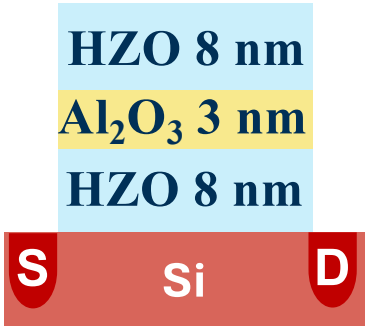
FE (reference)

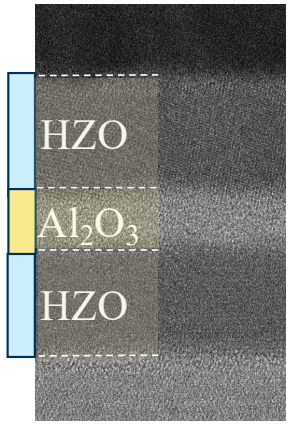


Gate blocking layer (GBL) 14/4(Si)



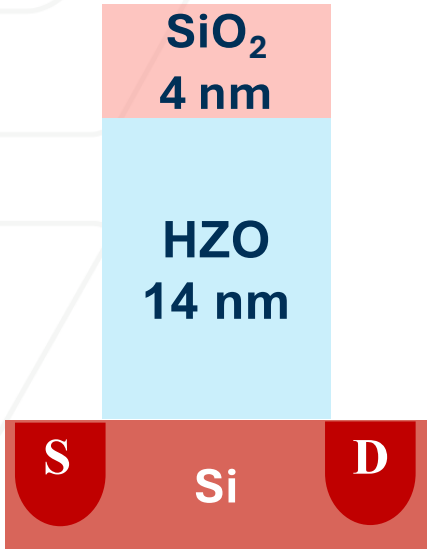
Tunnel dielectric layer (TDL) 8/3(Al)/8

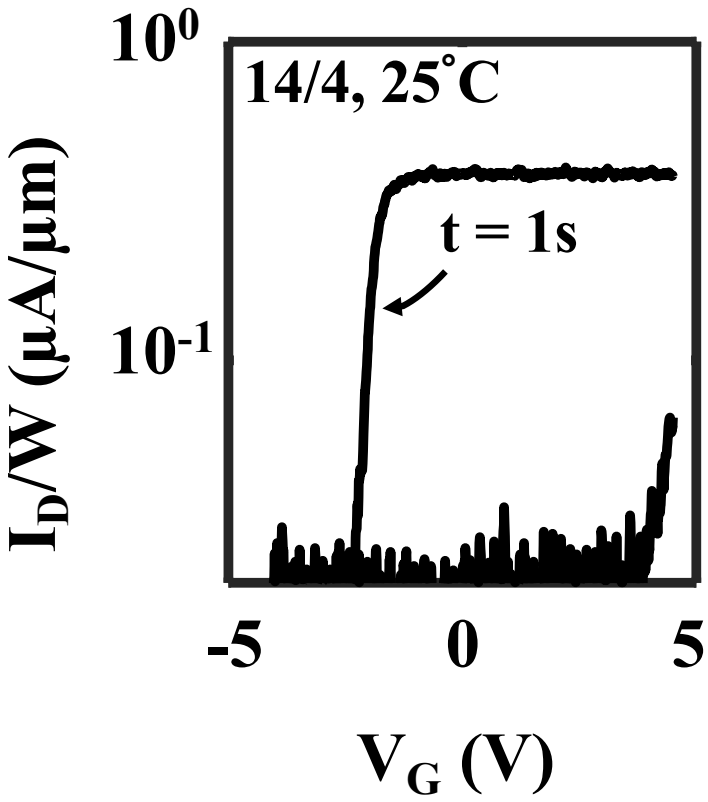


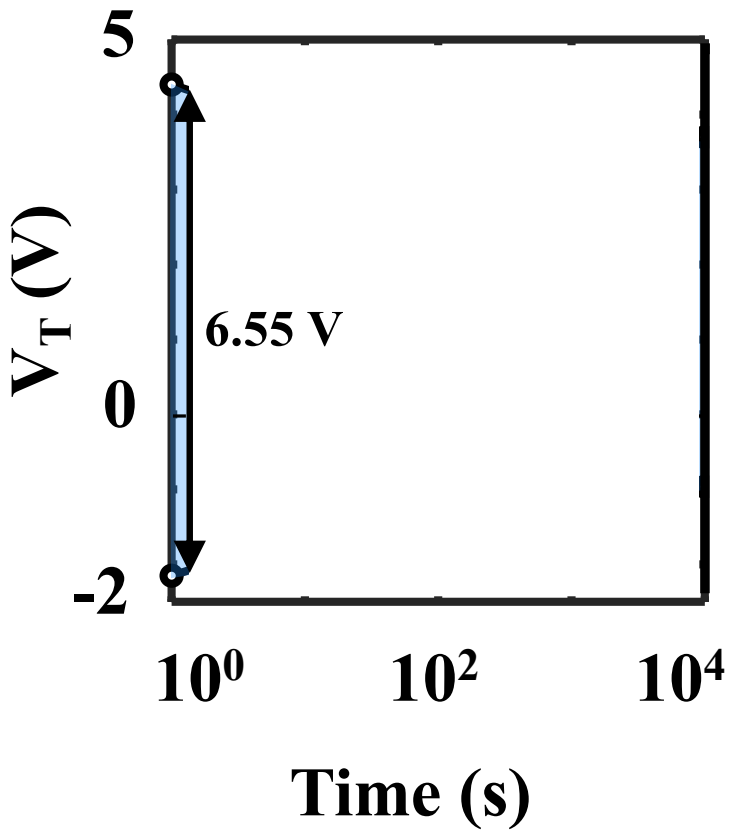


Venkatesan, Khan, et al. IRPS 2025 (Best Student Paper): https://doi.org/10.1109/IRPS48204.2025.10982749
Venkatesan, Khan, et al. EDL 2025 (Editor's Pick): 10.1109/LED.2024.3523235

Retention characterization







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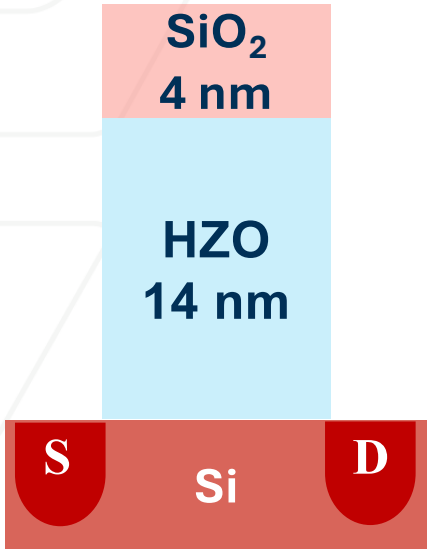

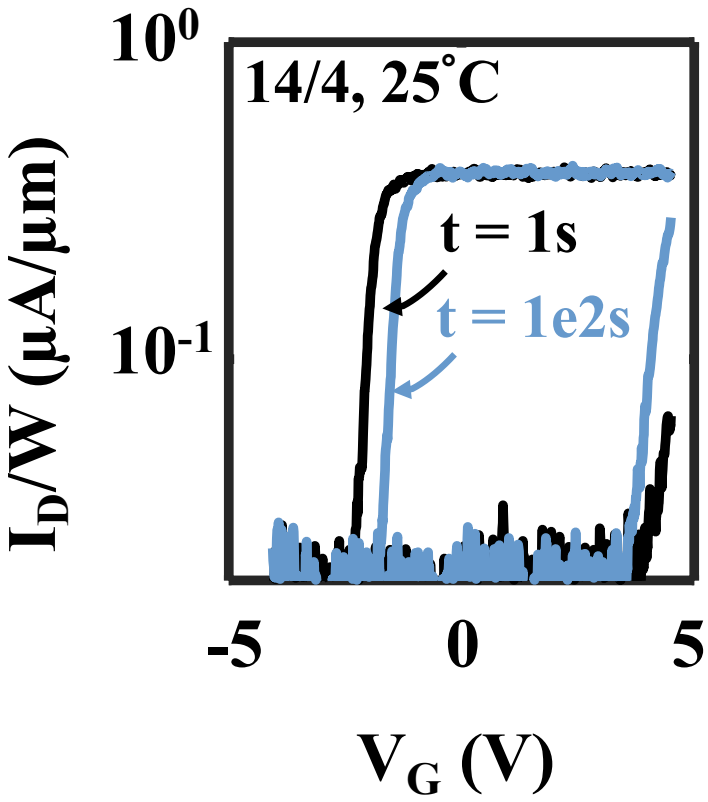

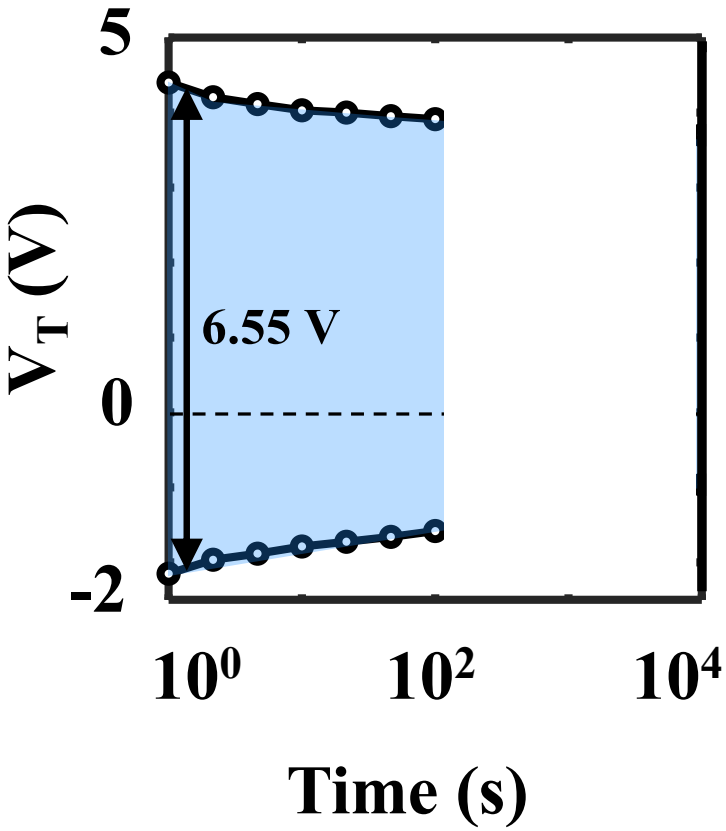

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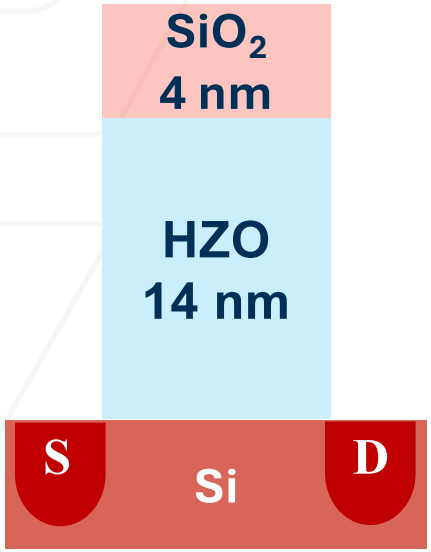

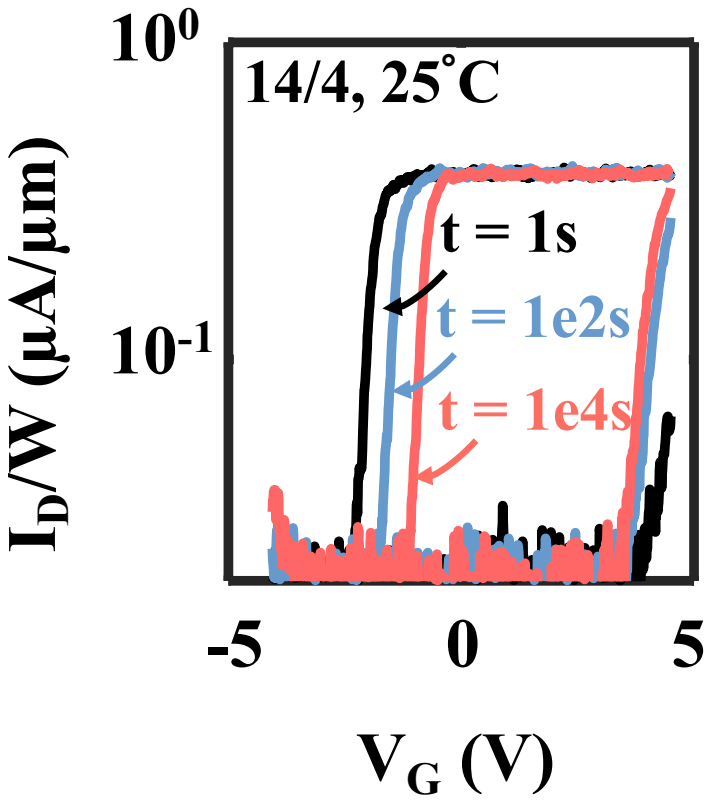

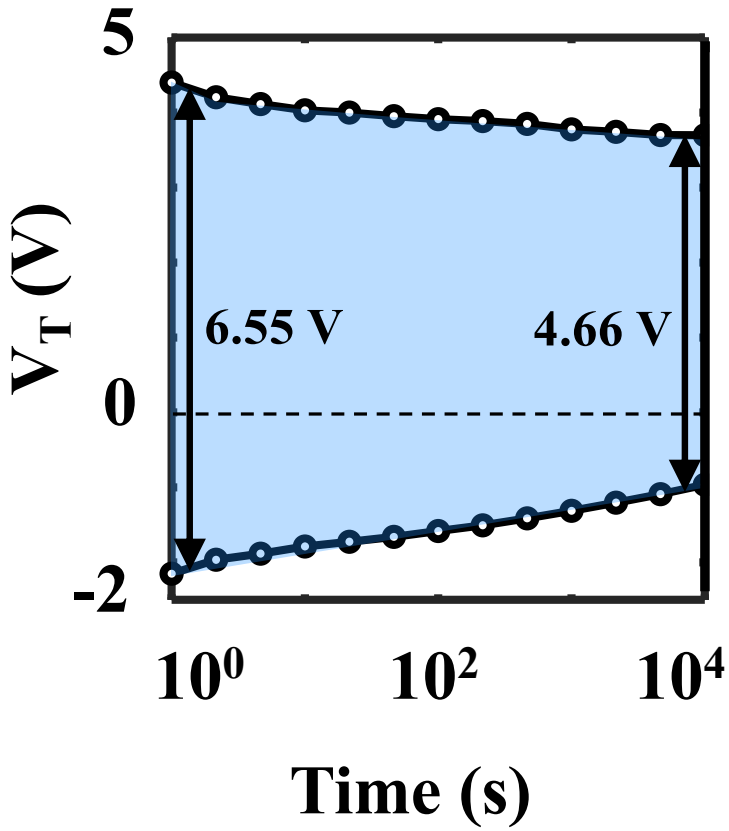

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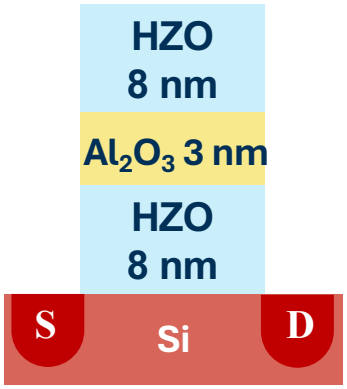
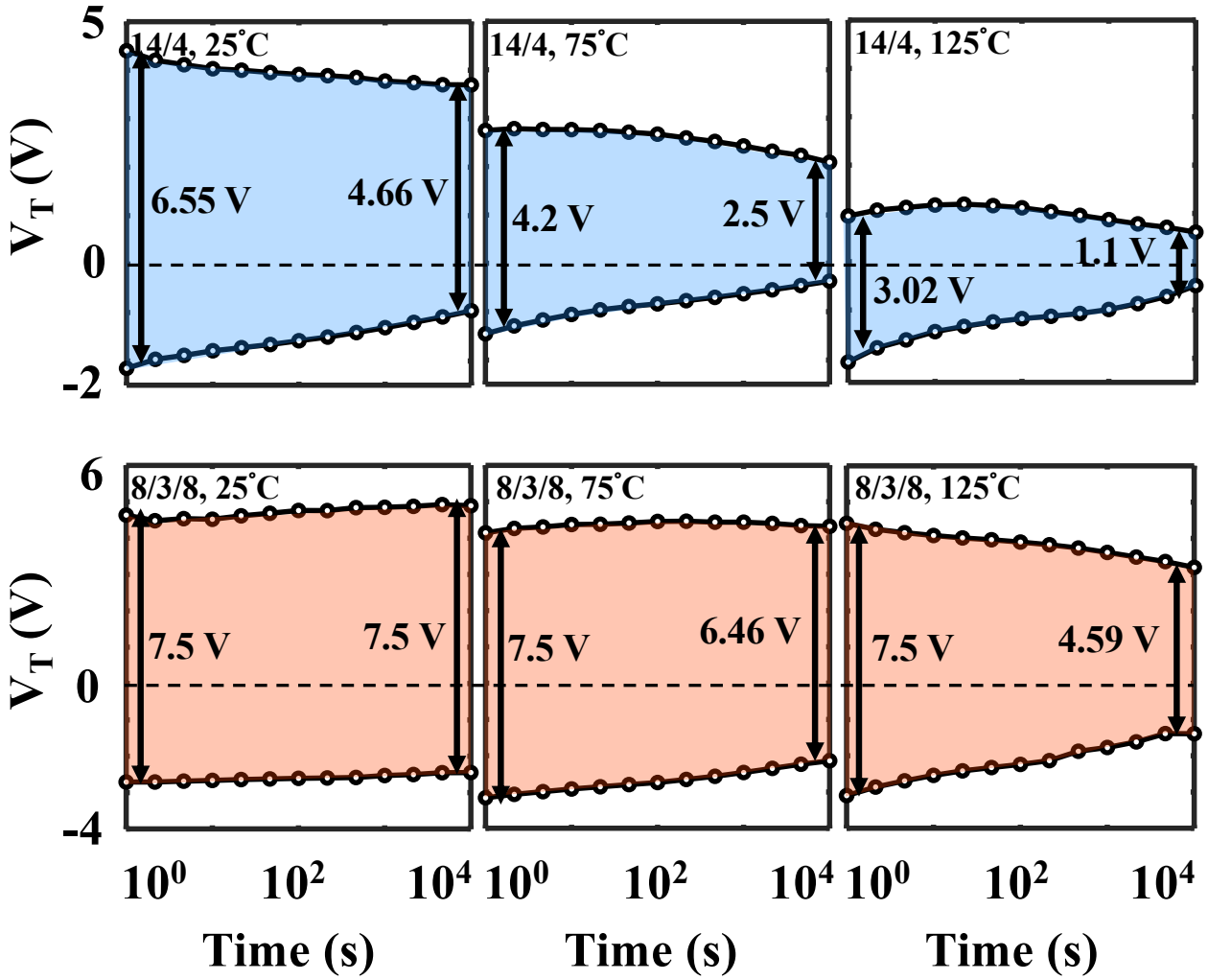
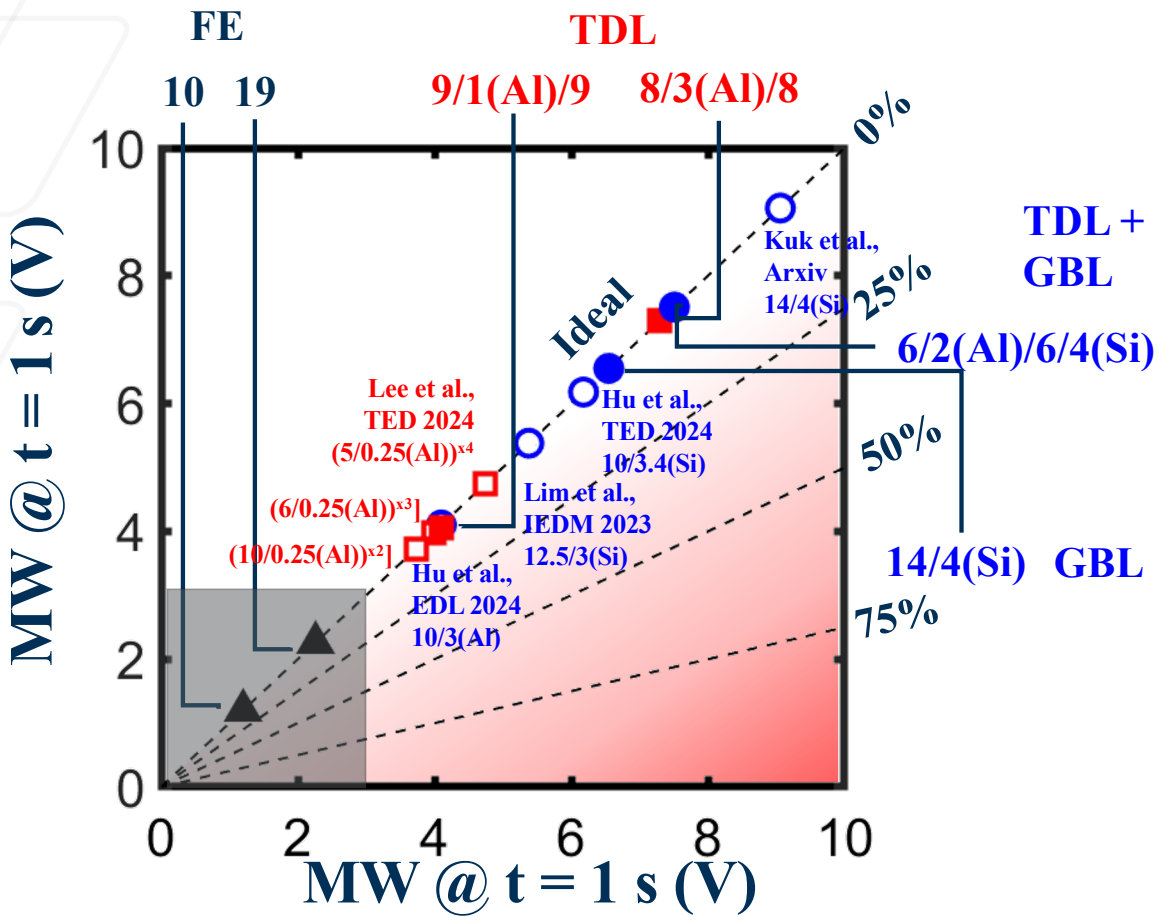
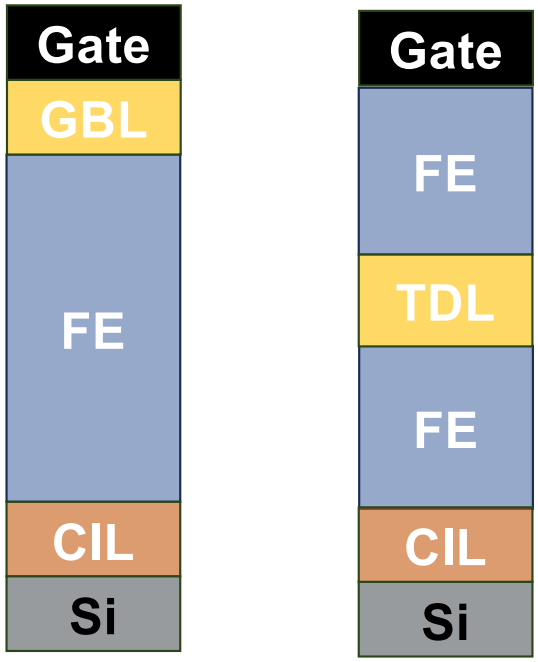




MW loss in FE-NAND





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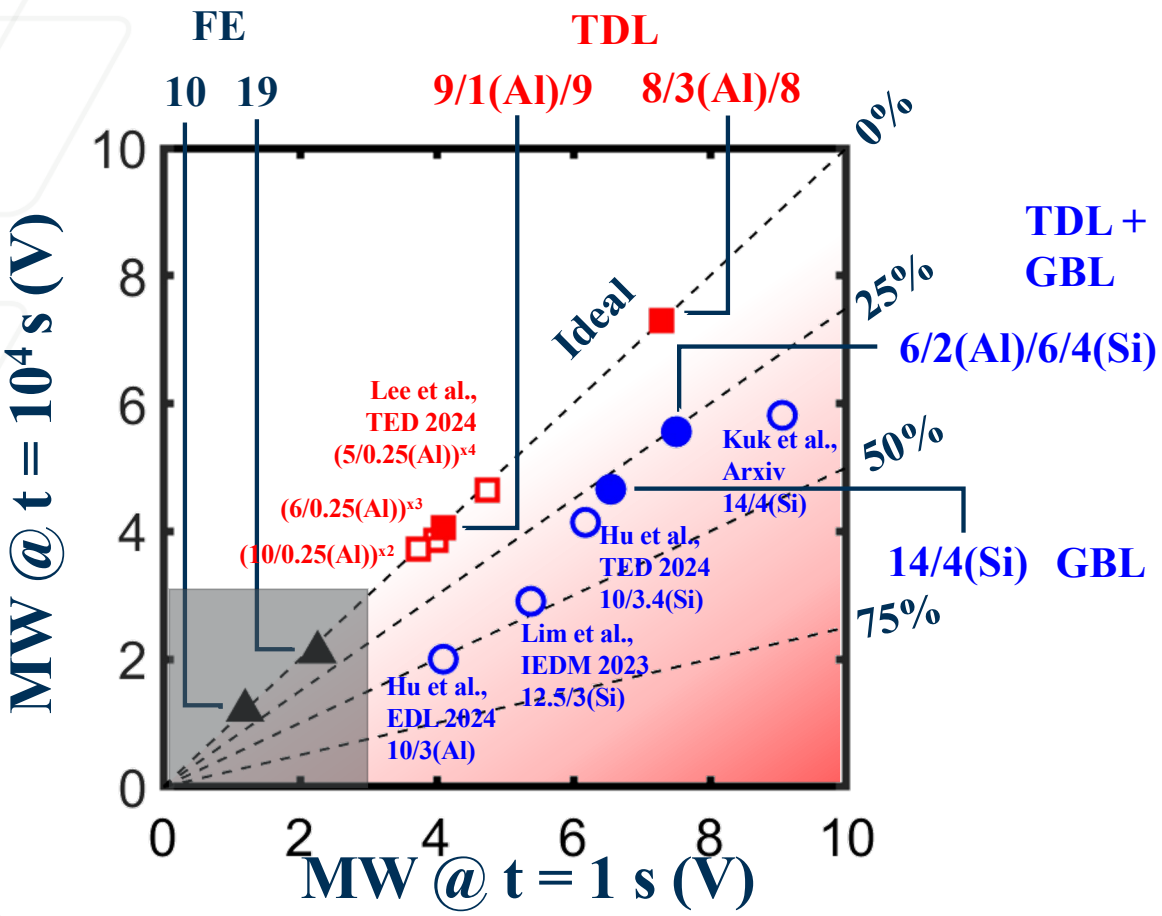

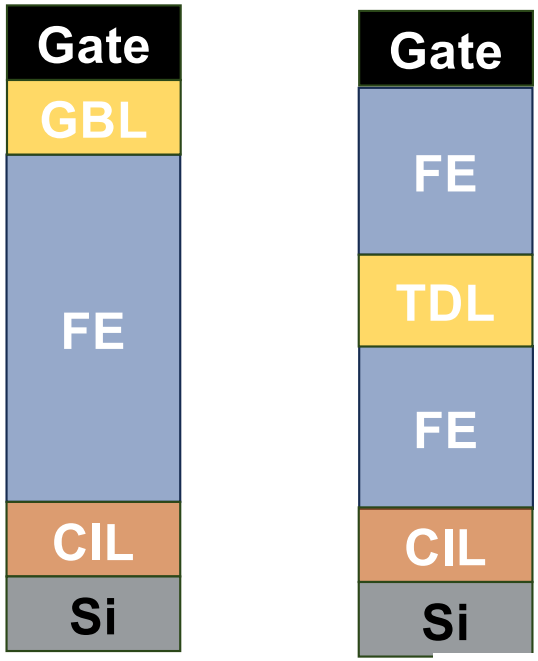

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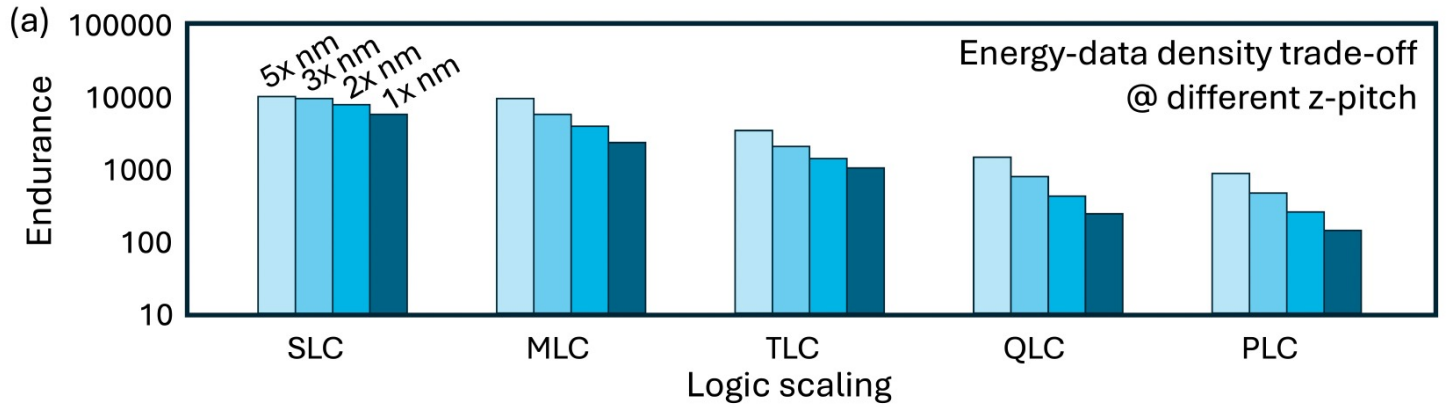
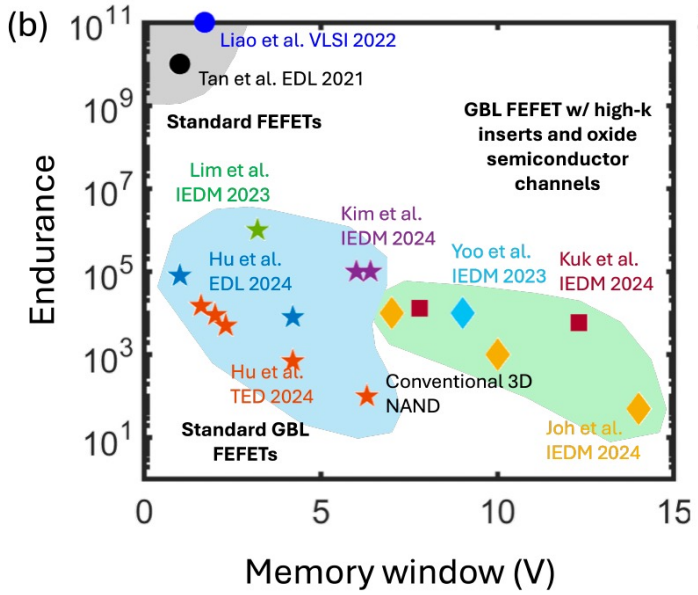
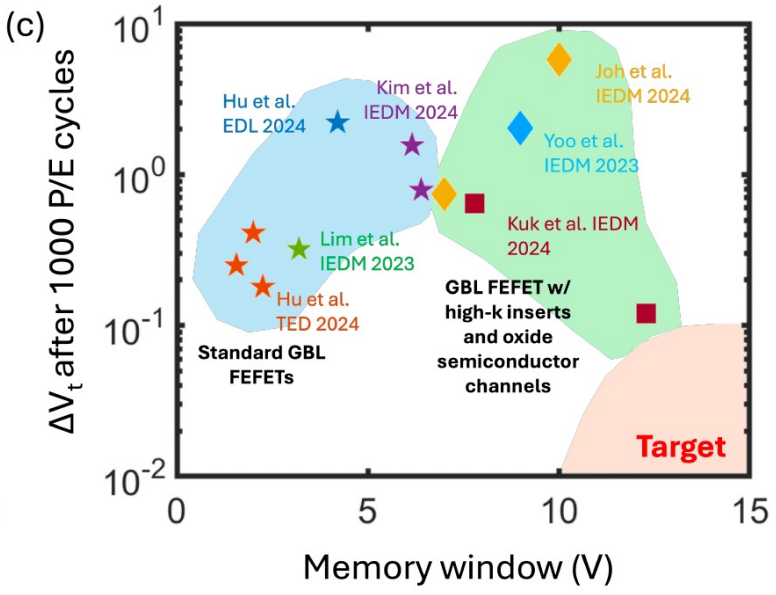
Write Endurance







Venkatesan, P., et al. IMW 2025

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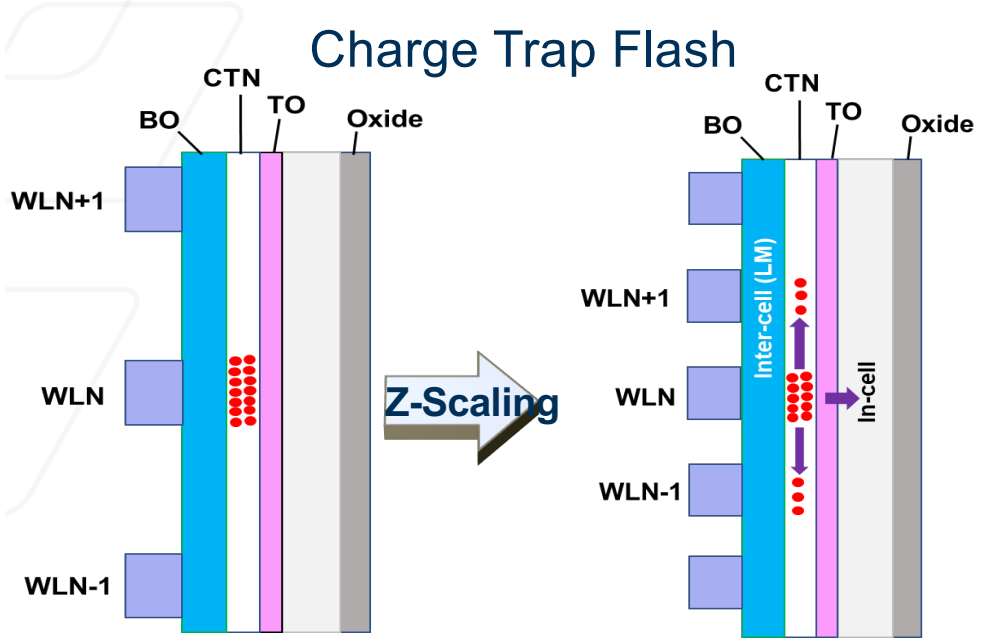
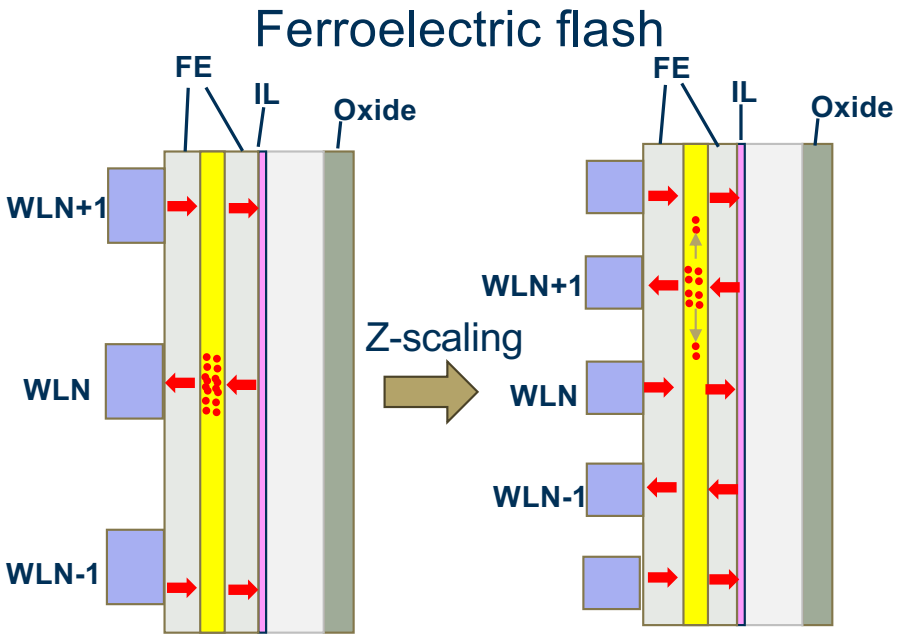
Lateral charge migration



Lateral charge migration prevents aggressive Z-scaling for 3D NAND.



The nature of trapped charges at the ferroelectric—interlayer interface will determine the scaling potential of ferroelectric 3D NAND technology.

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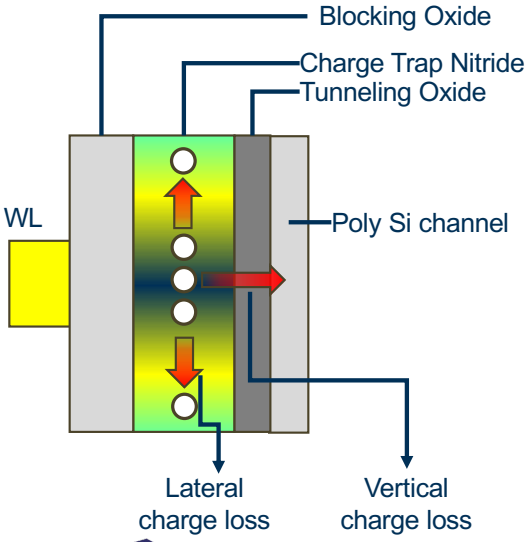
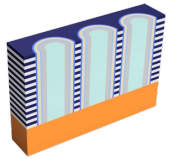
What about reliability of ferroelectric NAND?

❶ Retention	✅ Demonstrated
❷ Disturb	✅ Demonstrated
❸ Write endurance	⚠️ Under Evaluation
❹ Lateral charge migration	⚠️ Under Evaluation
❺ Device-device variation	⚠️ Under Evaluation
⋮	

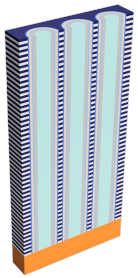
Ferroelectrics for Future NAND Storage Technology

Ferroelectric augmentation can provide enable NAND scaling in future generations

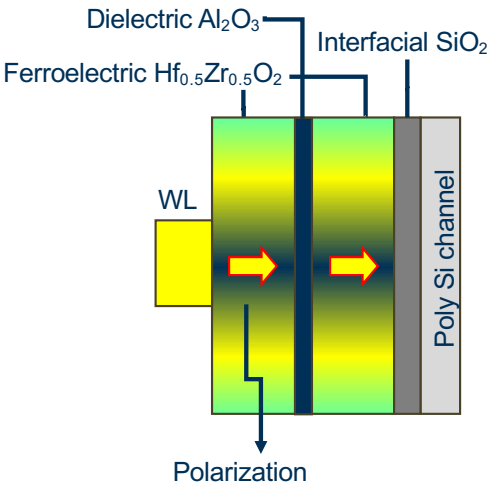


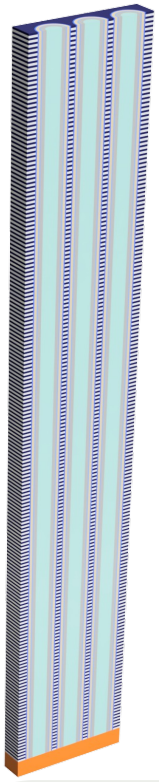


2014:
First 3D NAND
24 Layers, MLC



2025:
300+ Layers, QLC
5 Trillion+ transistors





2030 and
beyond

Georgia Tech

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Dr. Zheng Wang (Micron)


Dr. Sarah Lombardo (TEL)


Dr. Nujhat Tasneem (Intel)


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Prof. Lauren Garten, Prof. Shimeng Yu, Prof. Suman Datta, Georgia Tech

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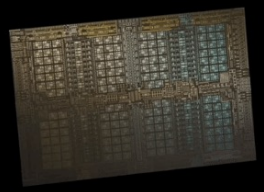
Memory technologies – The state of the art

1 **Memory**

Hyperscale AI, and High-performance Computing



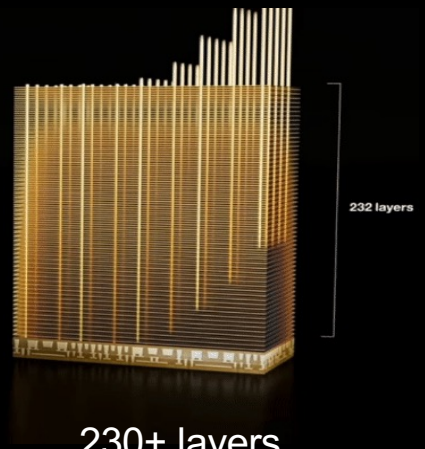
HBM3E: 12-high, 24 GB

Total 192 GB, 1.18 TB/s

Source: NVIDIA

2 **Storage**

Client, Mobile, and Enterprise



230+ layers

2.4 GB/s

Source: Micron

3 **Embedded**

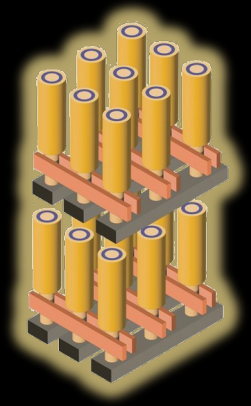
Automotive

14nm eMRAM

16 MB

Source: Forbes

4 **Emerging Memory**



Ferroelectric NV-DRAM

32 Gb, 3D-stacked, multi-layer

Source: IEDM 2023