Pushing the limits of NAND scaling with *Ferroelectrics*

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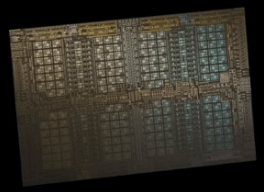
Memory technologies – The state of the art

1 Memory

Hyperscale AI, and High-performance Computing



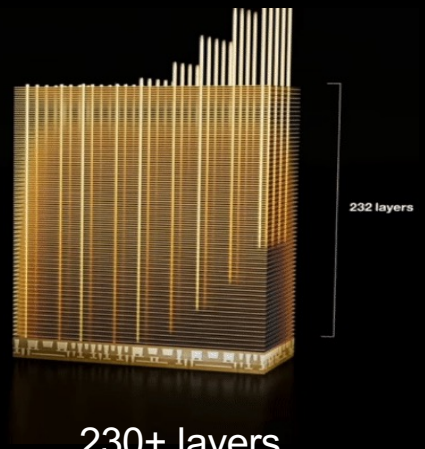
HBM3E: 12-high, 24 GB

Total 192 GB, 1.18 TB/s

Source: NVIDIA

2 Storage

Client, Mobile, and Enterprise



230+ layers

2.4 GB/s

Source: Micron

3 Embedded

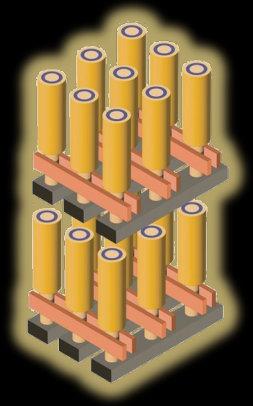
Automotive

14nm eMRAM

16 MB

Source: Forbes

4 Emerging Memory



Ferroelectric NV-DRAM

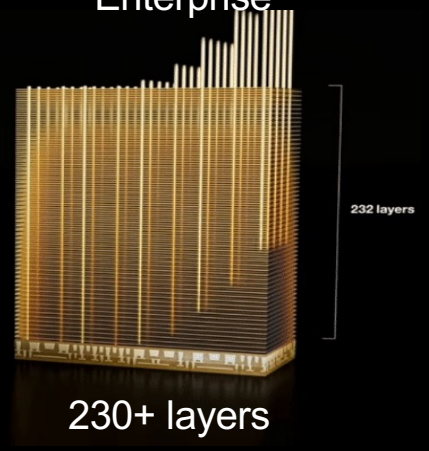
32 Gb, 3D-stacked, multi-layer

Source: IEDM 2023

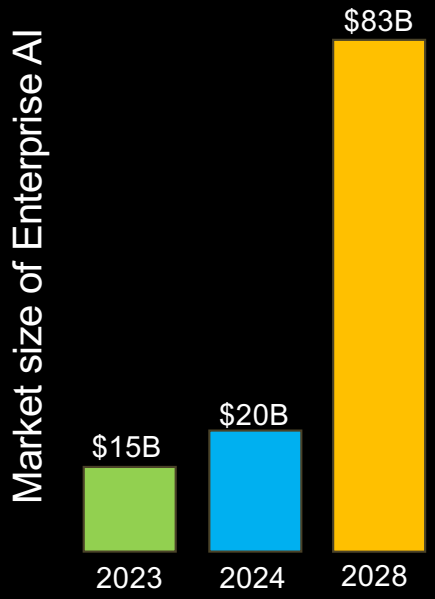
The NAND Storage Technology

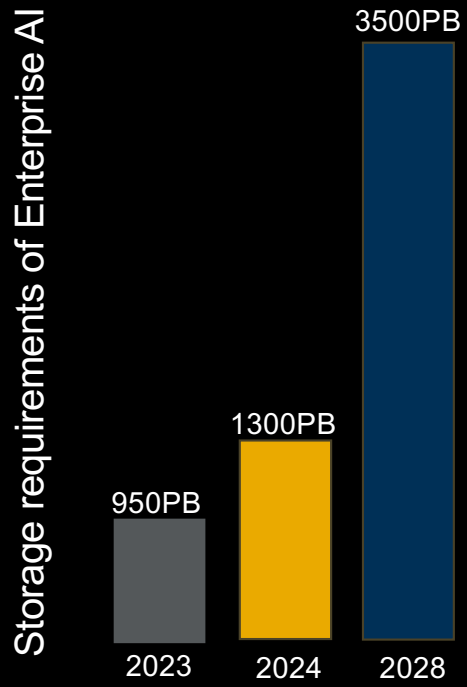
Storage

Client, Mobile, and Enterprise



Source: Micron





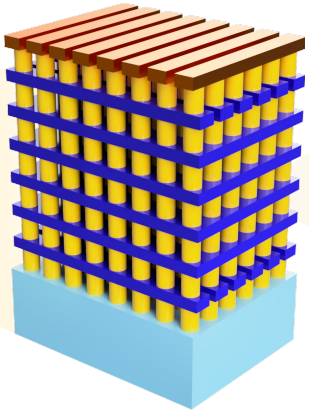
Source: The Business Research Company

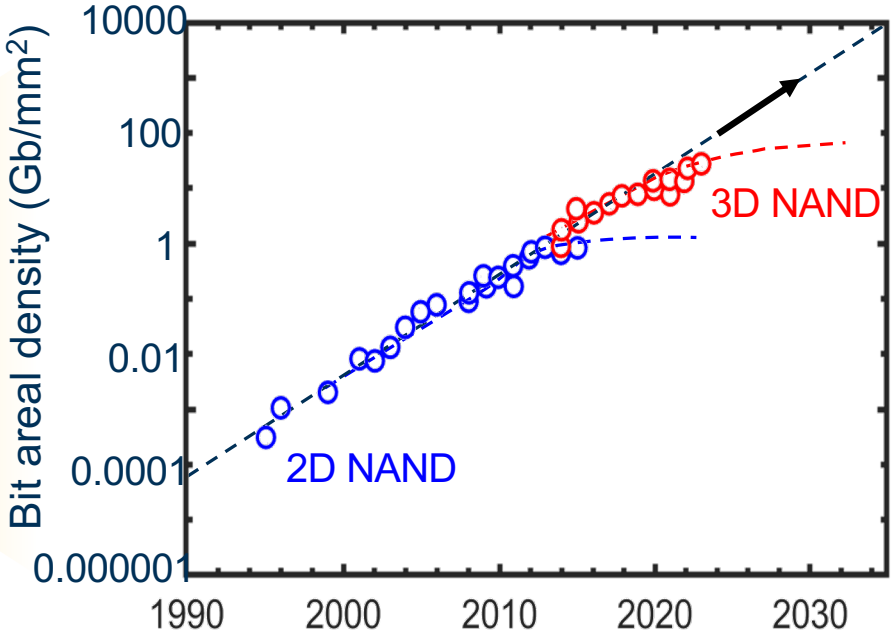
Processing and storing data in AI effectively and cost efficiently can require HBM for the actual AI training, but also various types of NAND-based solid-state storage to support the data flows needed to and from the HBM.

Vertical NAND Scaling

Solid-state drive

3D NAND flash structure





A. Goda, IEDM 2024

Relentless innovations have led to a 50x improvement in bit arial density per decade.

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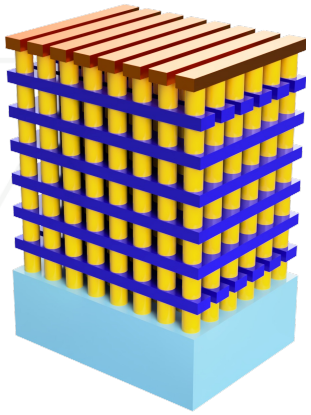
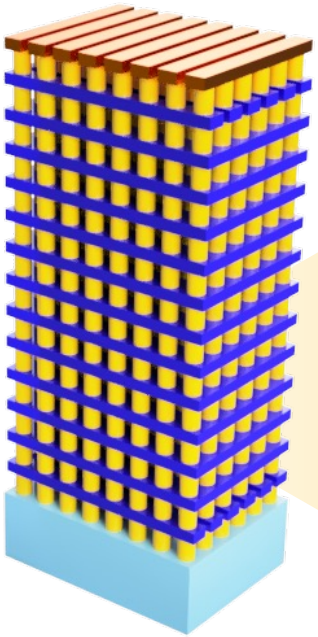
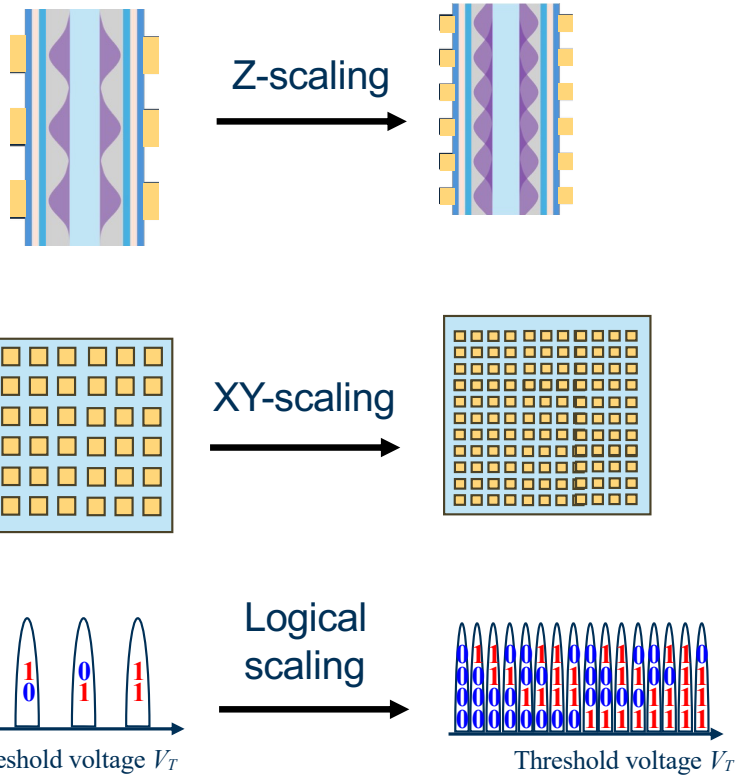
Vertical NAND Scaling



2014
First 3D NAND, Samsung
24 Layers, MLC



2022-2025
Samsung 236L TLC
SK Hynix 238L TLC
Micron 232L TLC
192L QLC



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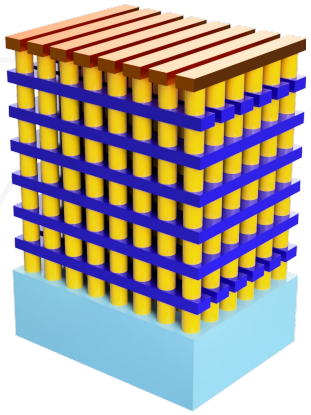
Vertical NAND Scaling



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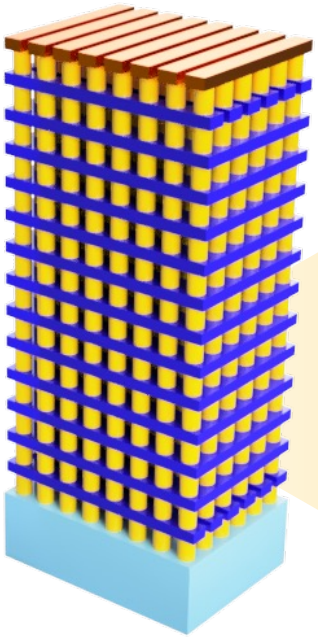

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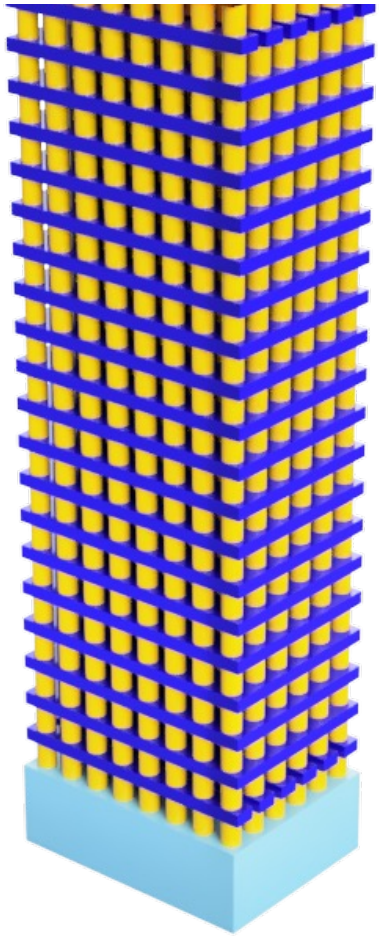

2030
?

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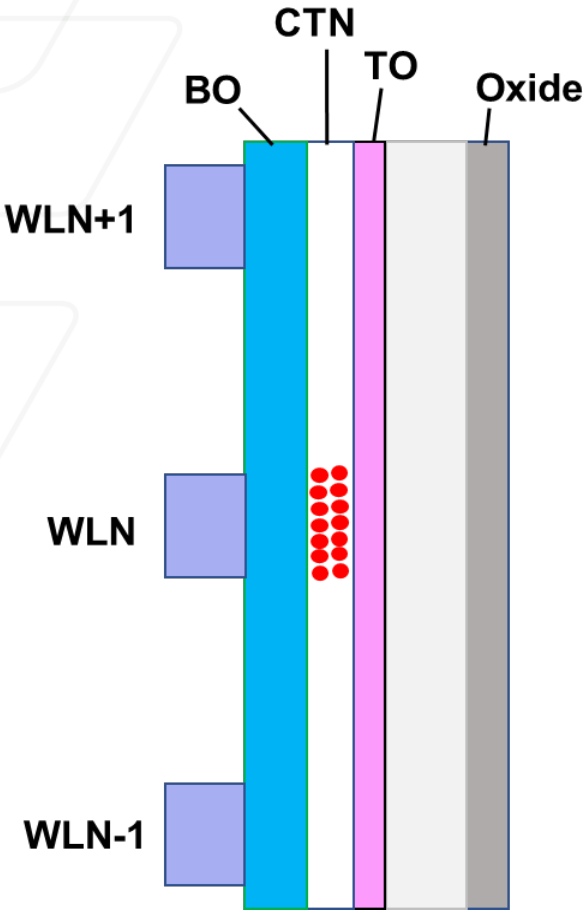
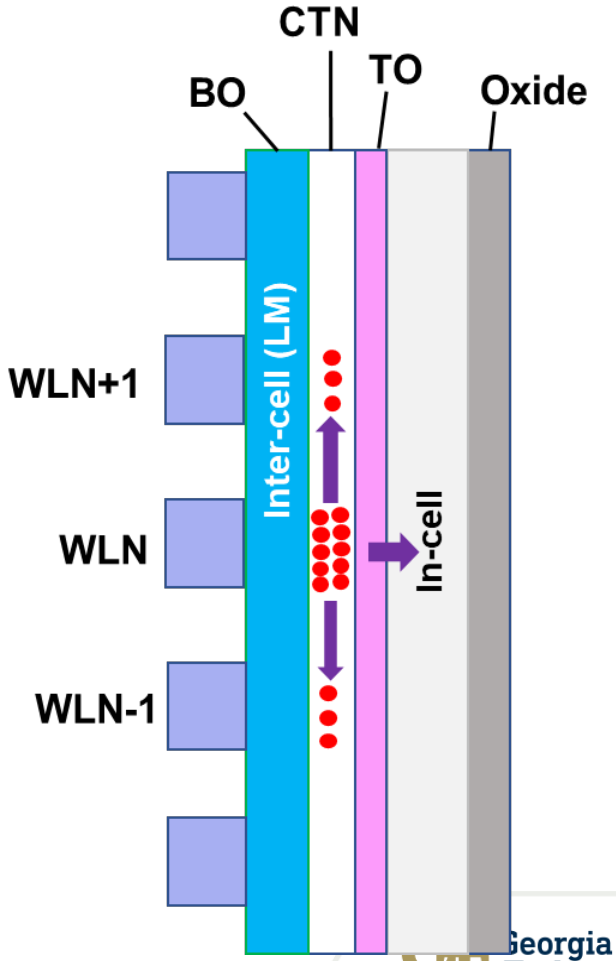
Challenges of vertical NAND flash scaling

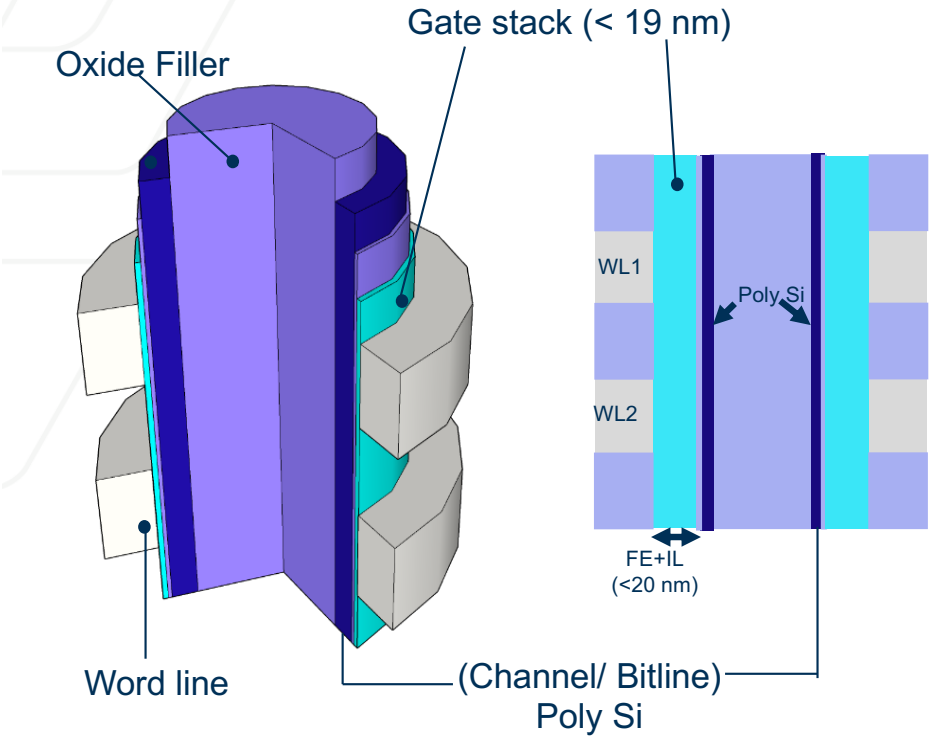


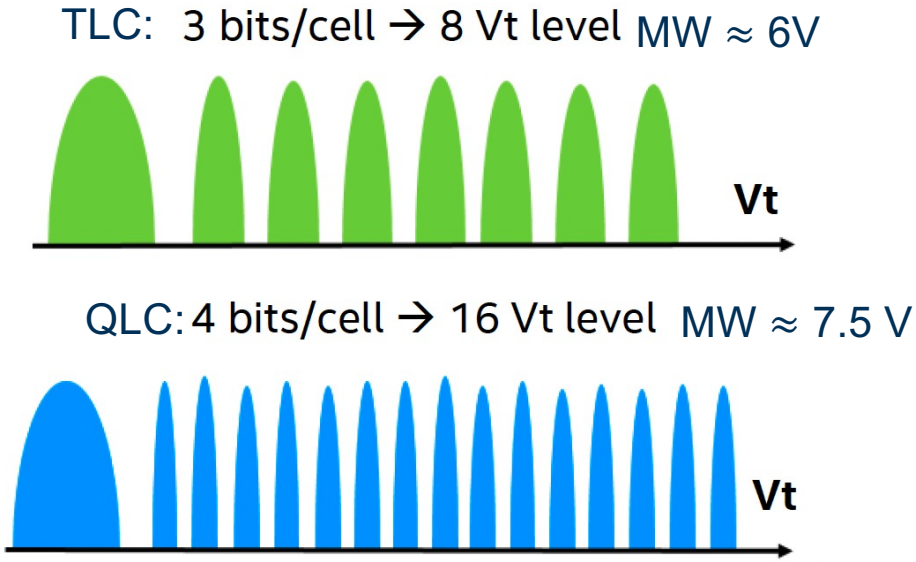
Z-scaling

1. Lateral charge migration
2. Inter-WL reliability
3. High write voltage
4. Endurance
5. Device-device variation



The future of NAND flash technology





To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm

Design constraints

Gate stack thickness, $t \leq 19$ nm

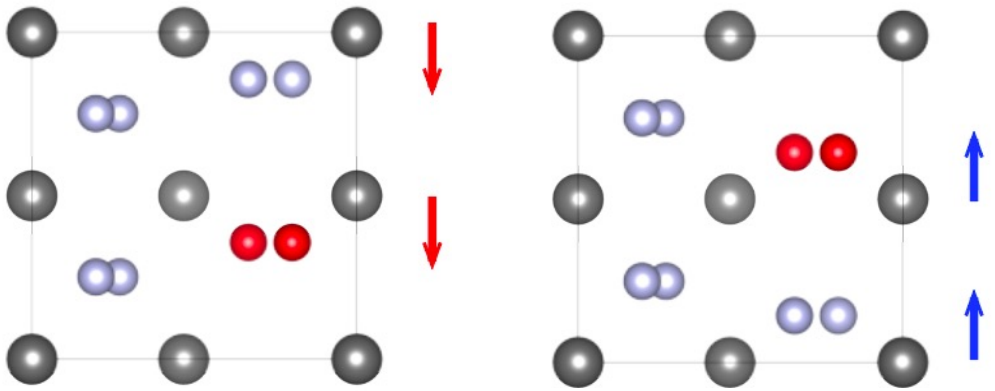
Write voltage ≤ 15 V

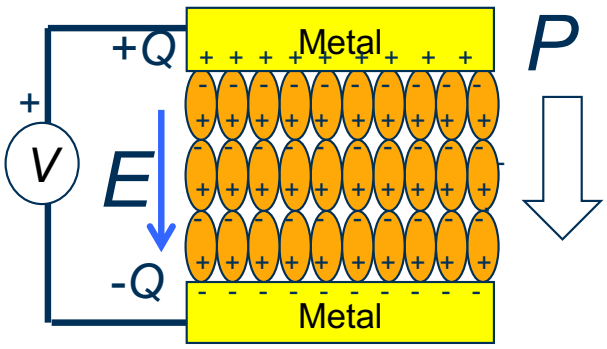
Memory window, MW ≥ 6.5 V

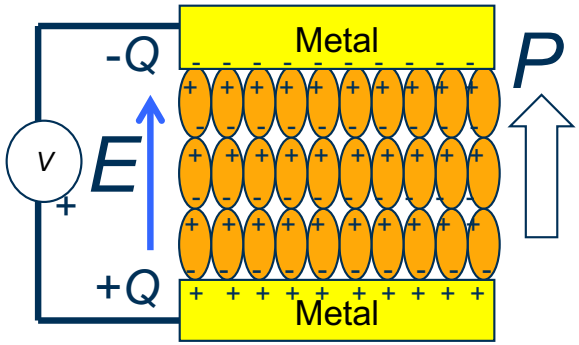
Ferroelectricity

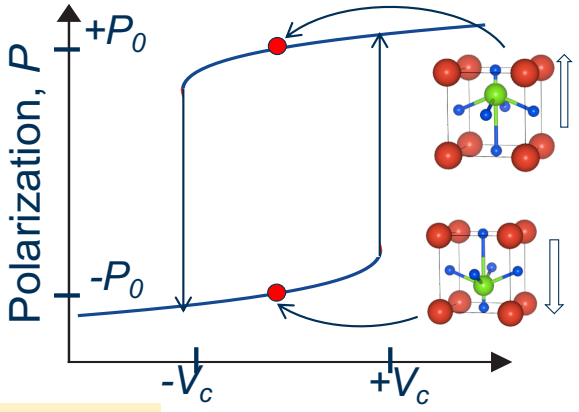
CMOS compatible HfO_2-based fluorite-structure ferroelectric

Orthorhombic *Pca2₁* structure



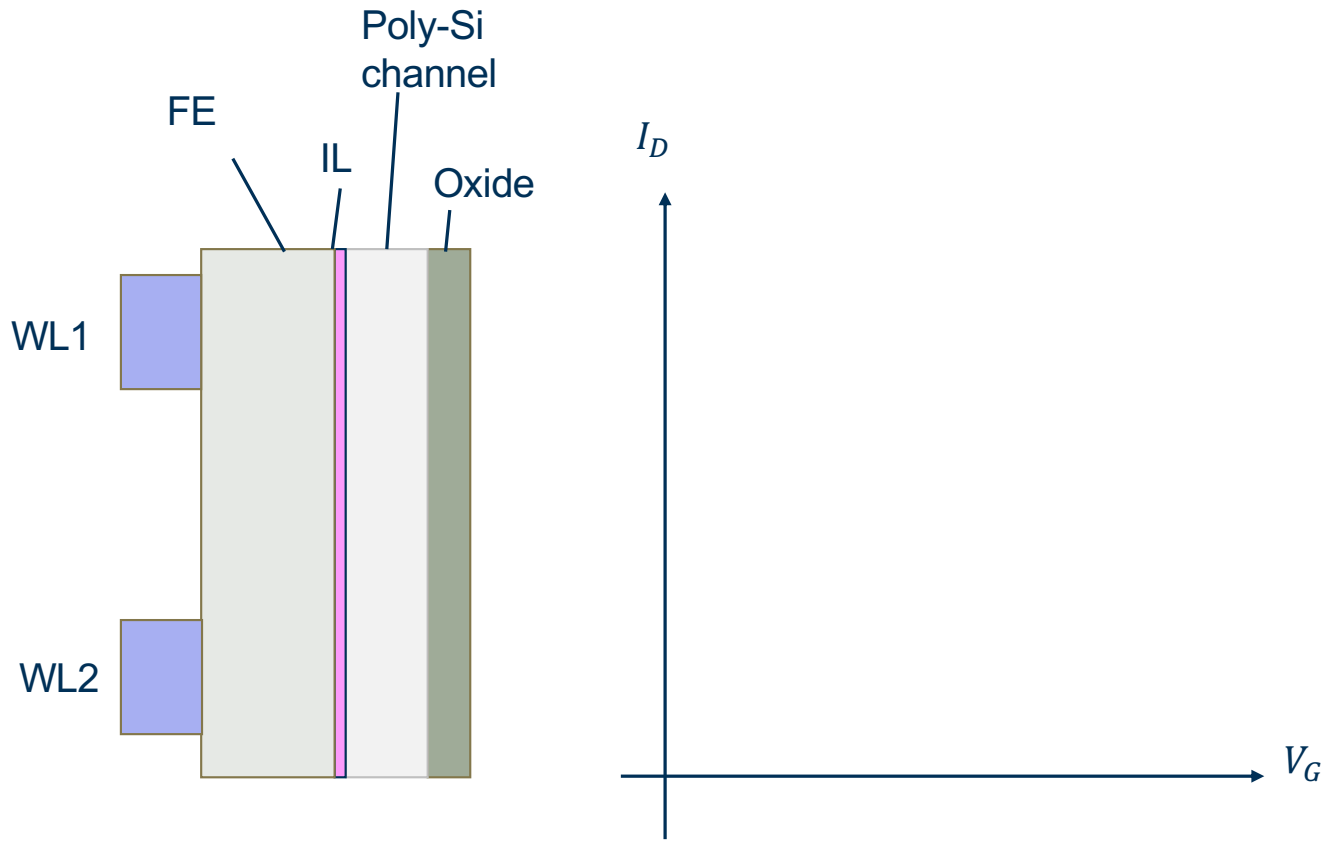






A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

Ferroelectric flash



FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the “remnant” polarization.

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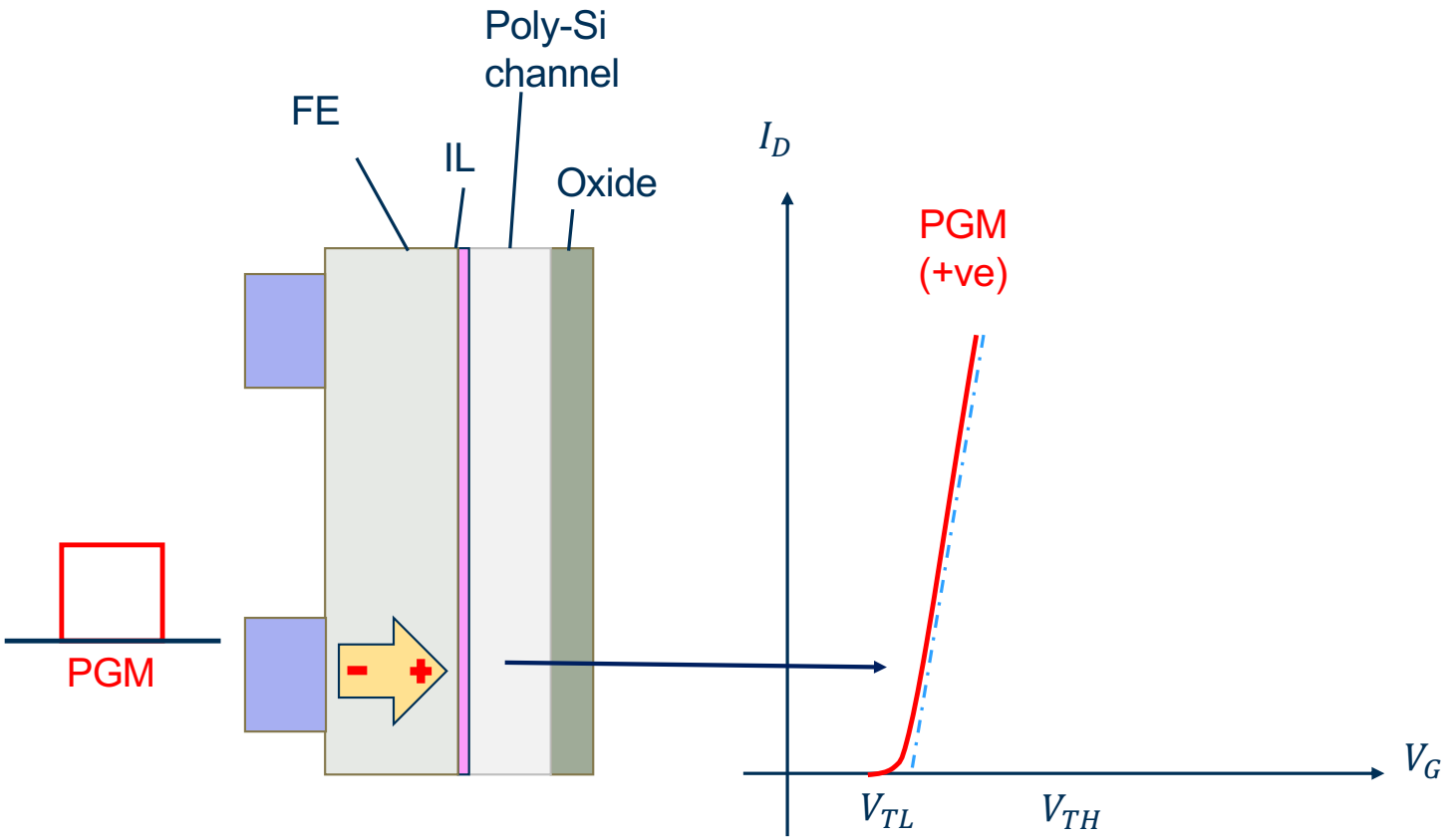
Ferroelectric flash



PGM (positive voltage) pulse sets the Vt to high Vt state in FEFET

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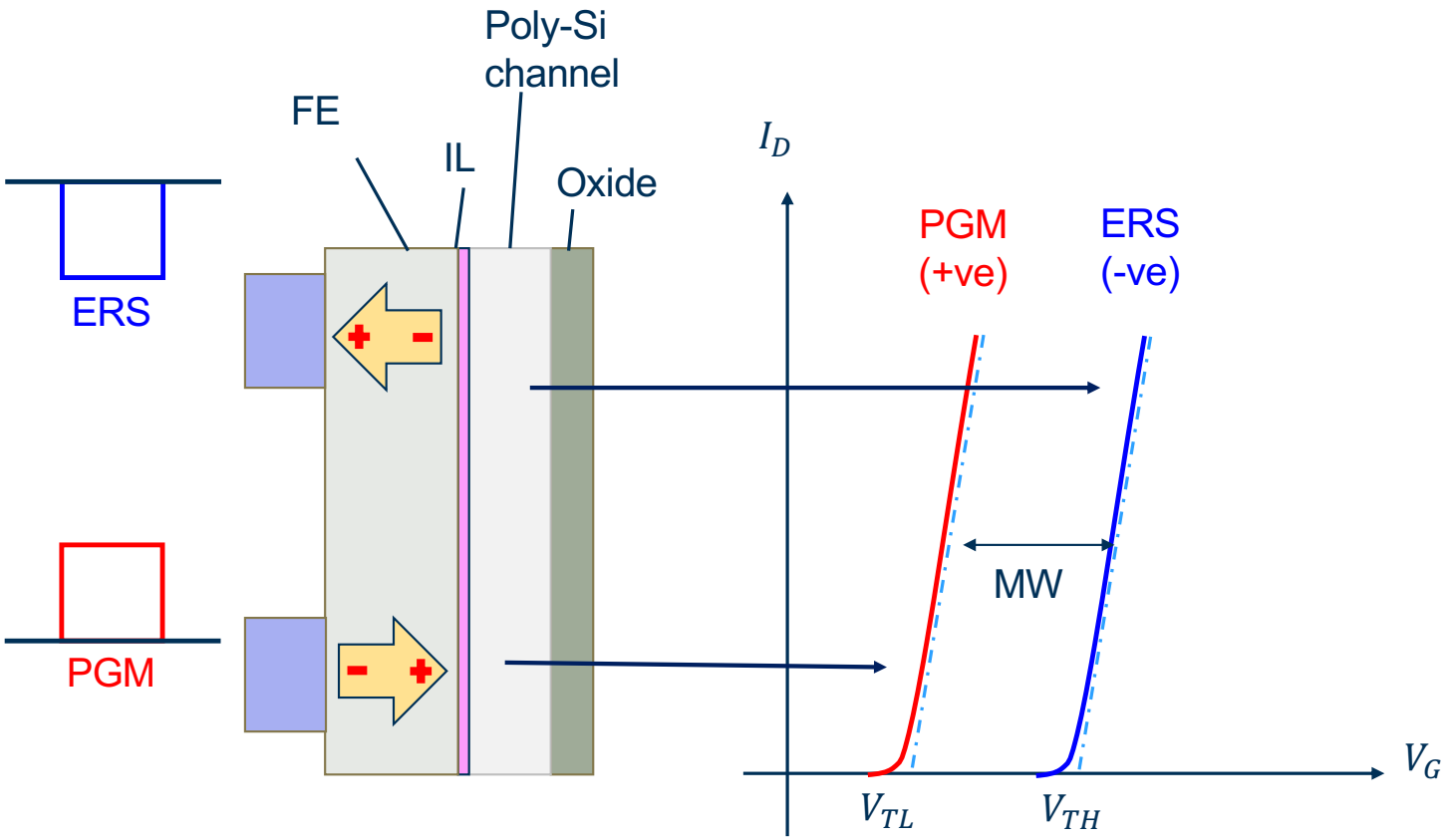
Ferroelectric flash



ERS (negative voltage) pulse sets the Vt to high Vt state in FEFET

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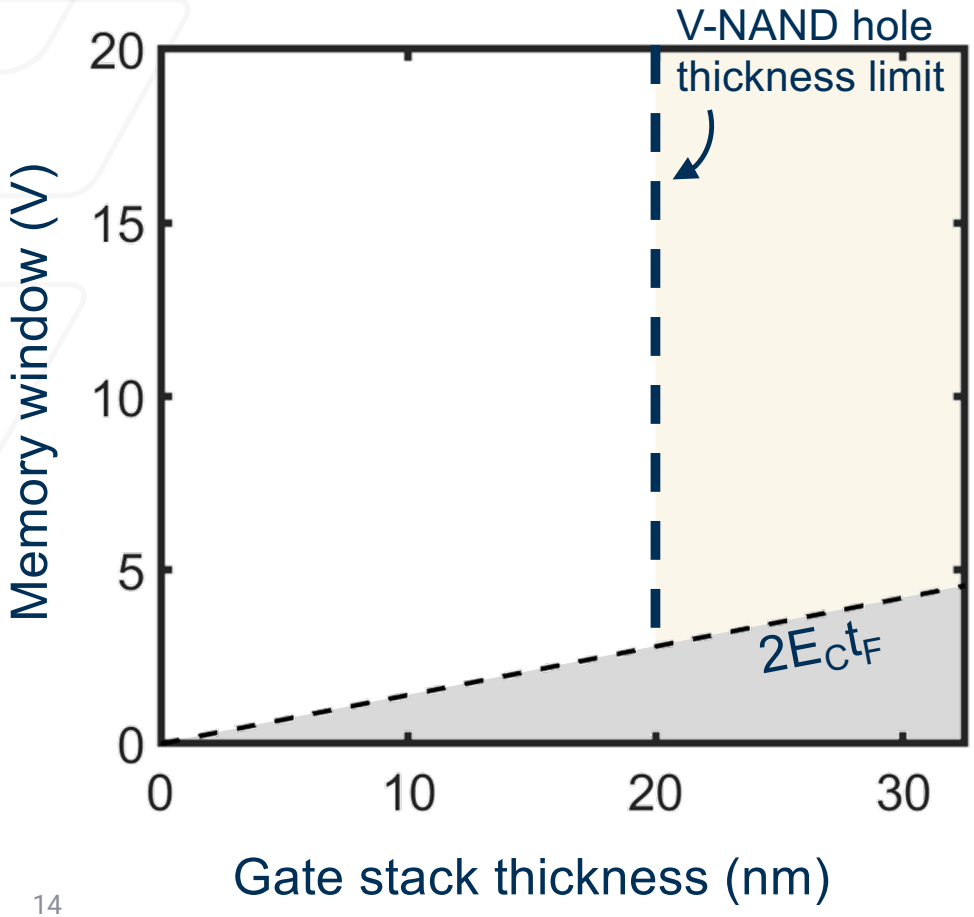
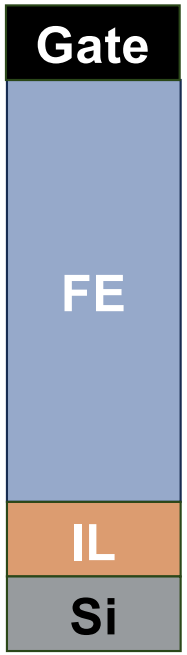
Memory window of FEFETs is limited by V_C

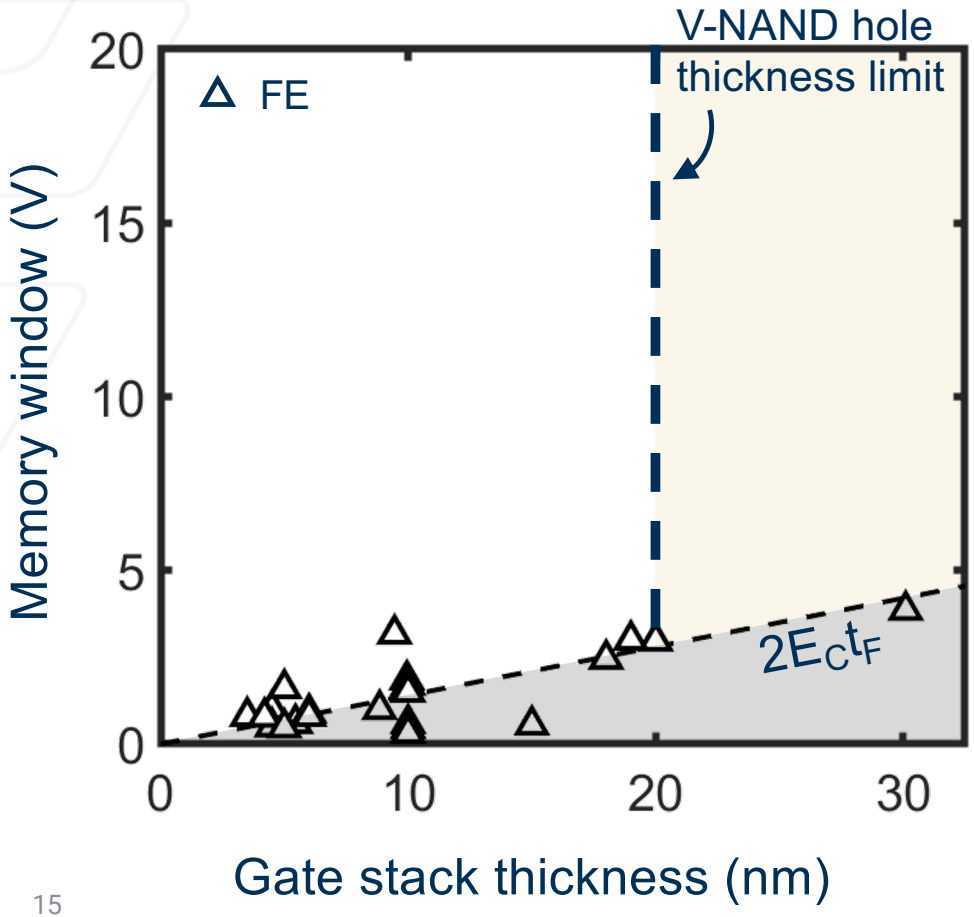


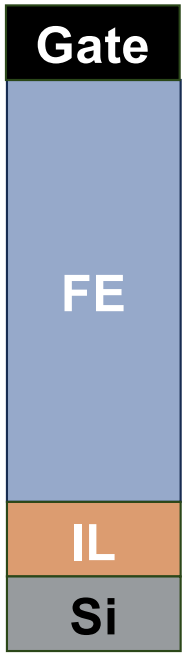


$$\mathrm{MW} \leq 2V_c = 2E_c \times t_f$$

The maximum memory window of an FeFET is theoretically limited by the memory window of the ferroelectric layer.

Memory window of FEFETs is limited by V_C



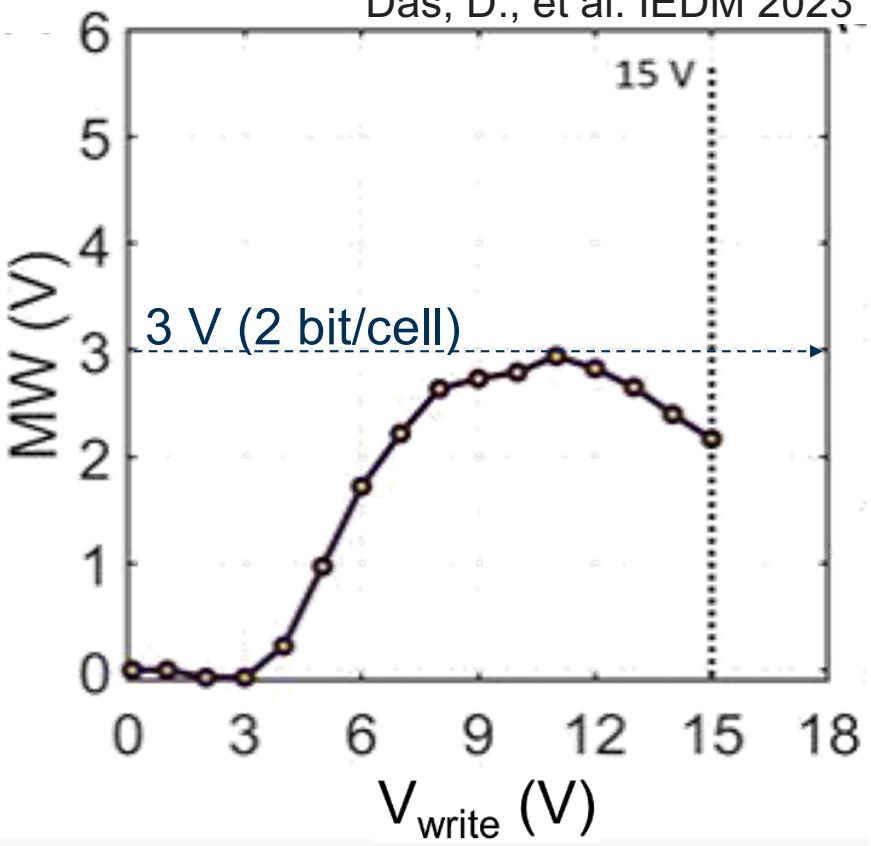


$$\mathrm{MW} \leq 2V_c = 2E_c \times t_f$$

The maximum memory window of an FeFET is theoretically limited by the memory window of the ferroelectric layer.

Increasing the MW by dielectric insertion

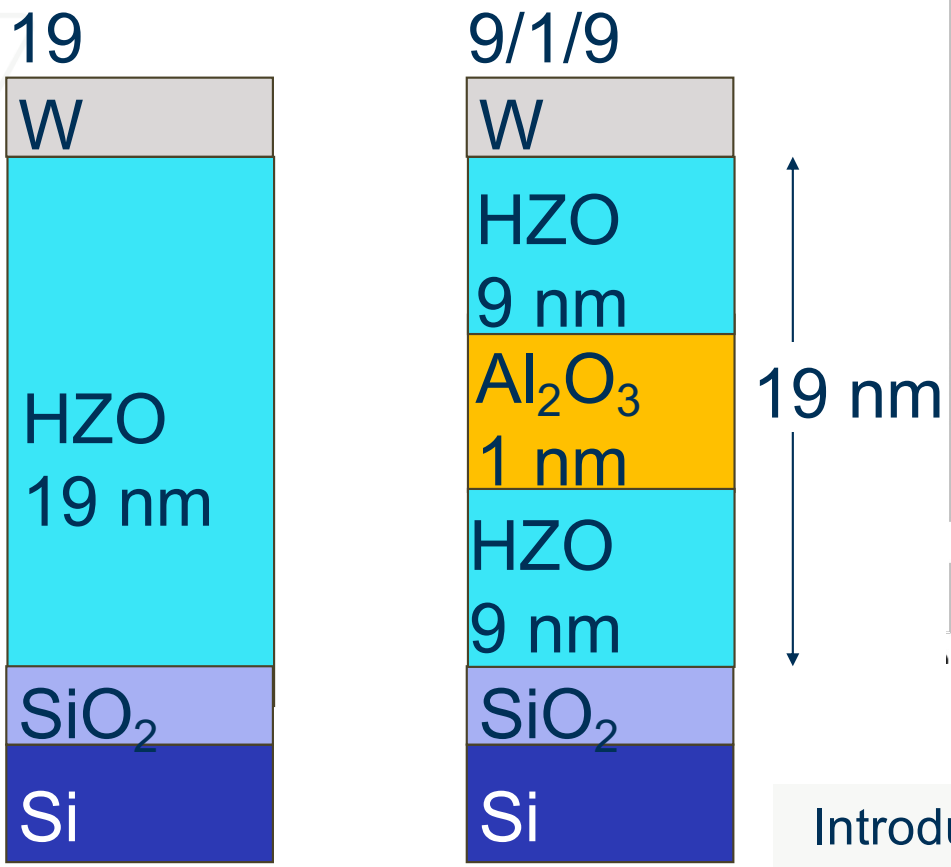
Das, D., et al. IEDM 2023

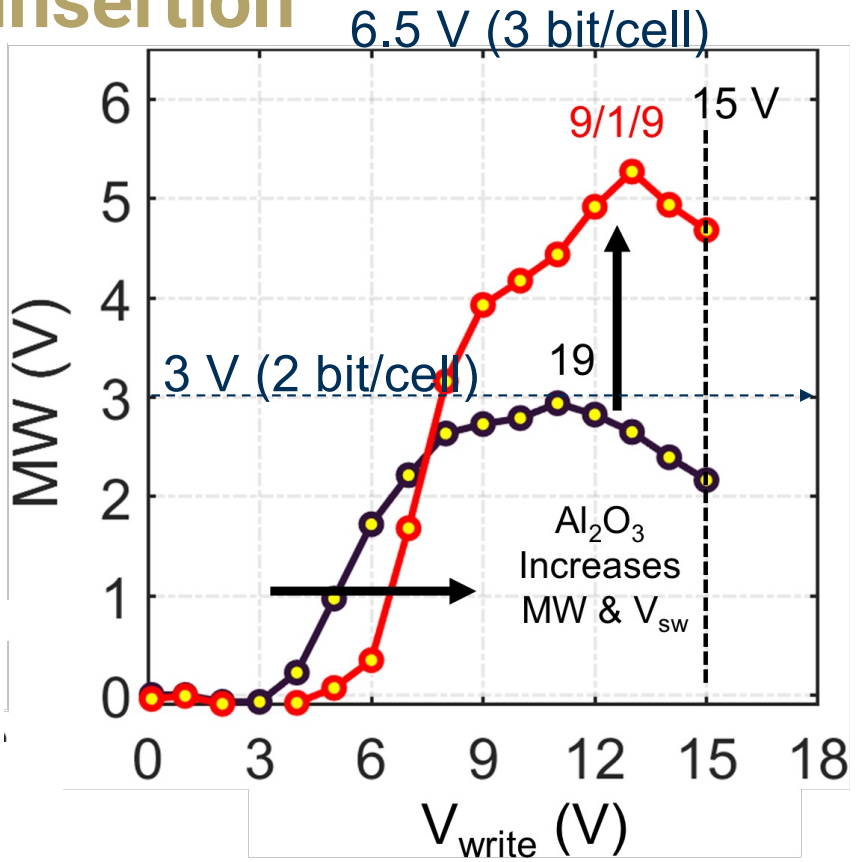


10 nm HZO layer leads to maximum memory window of 2.9 V.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion

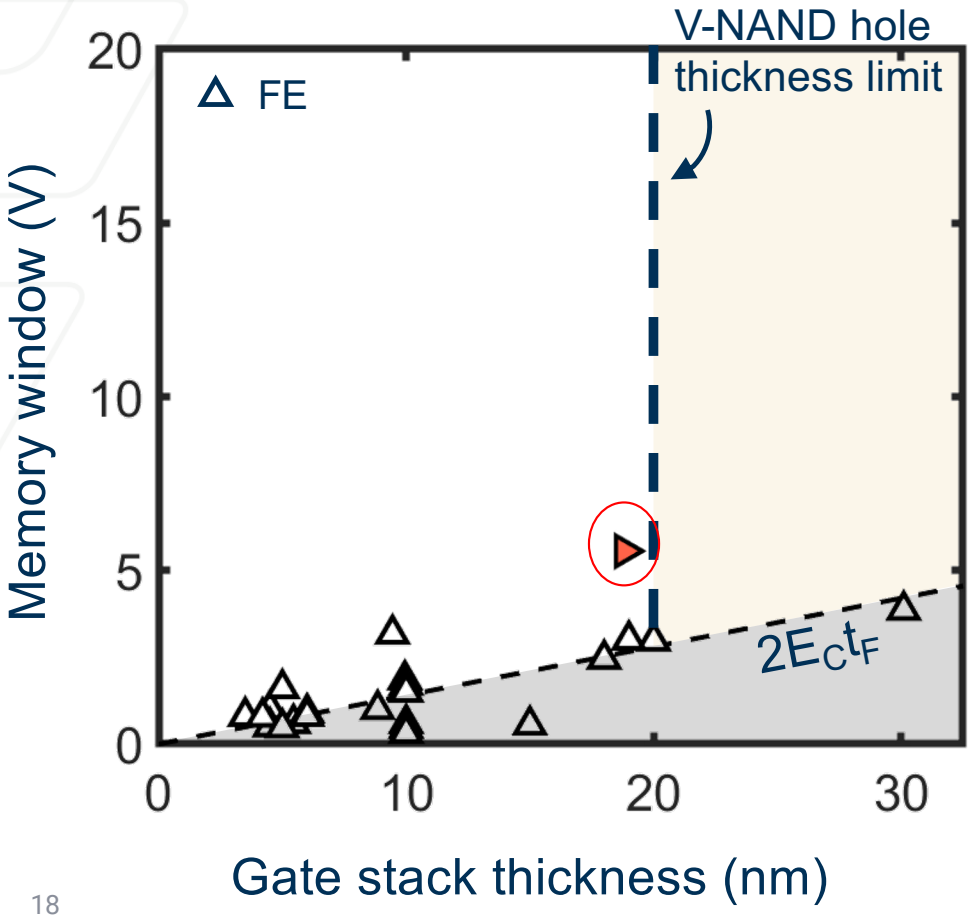


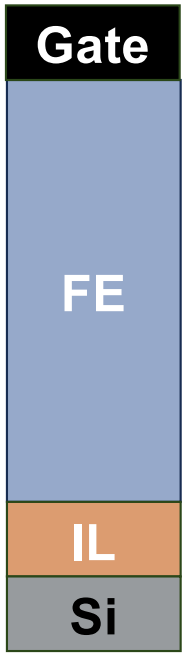


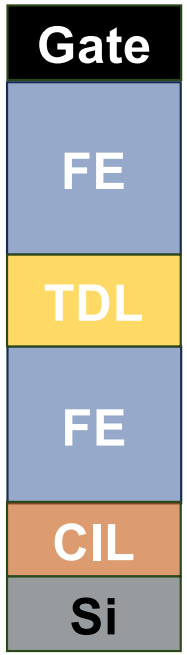
Introducing 1 nm Al_2O_3 intermediate layer dramatically memory window to 5.3 V.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Memory window of FEFETs is limited by V_C







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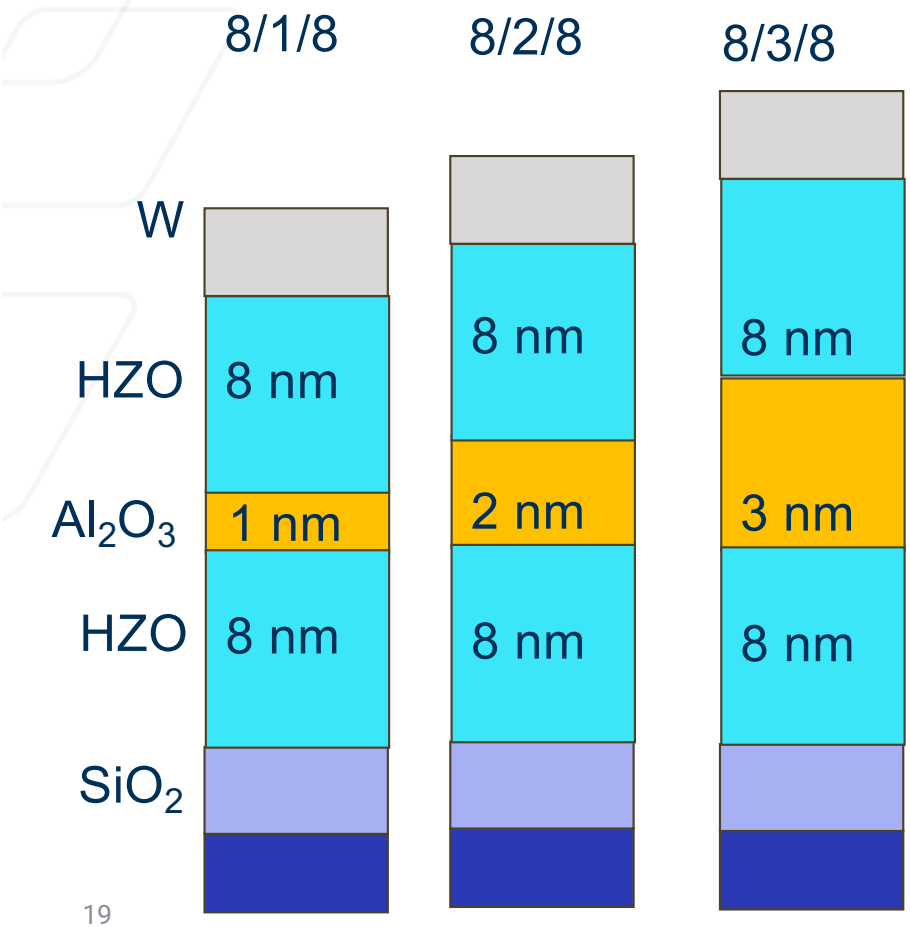
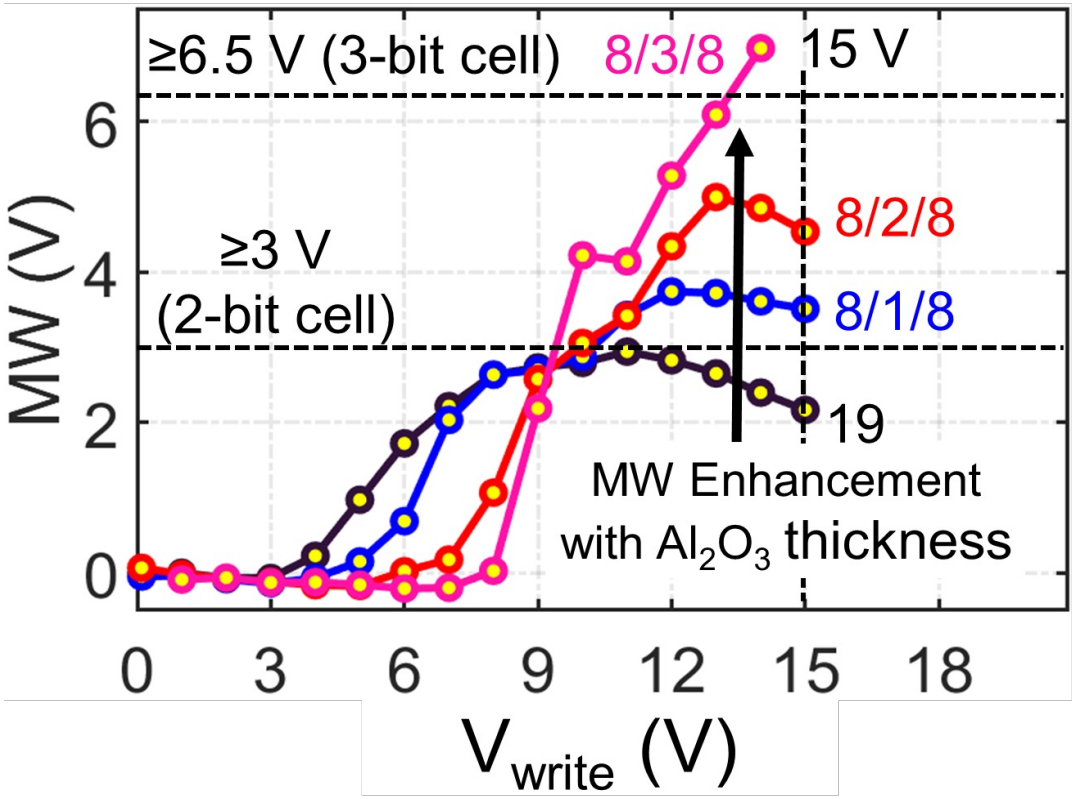
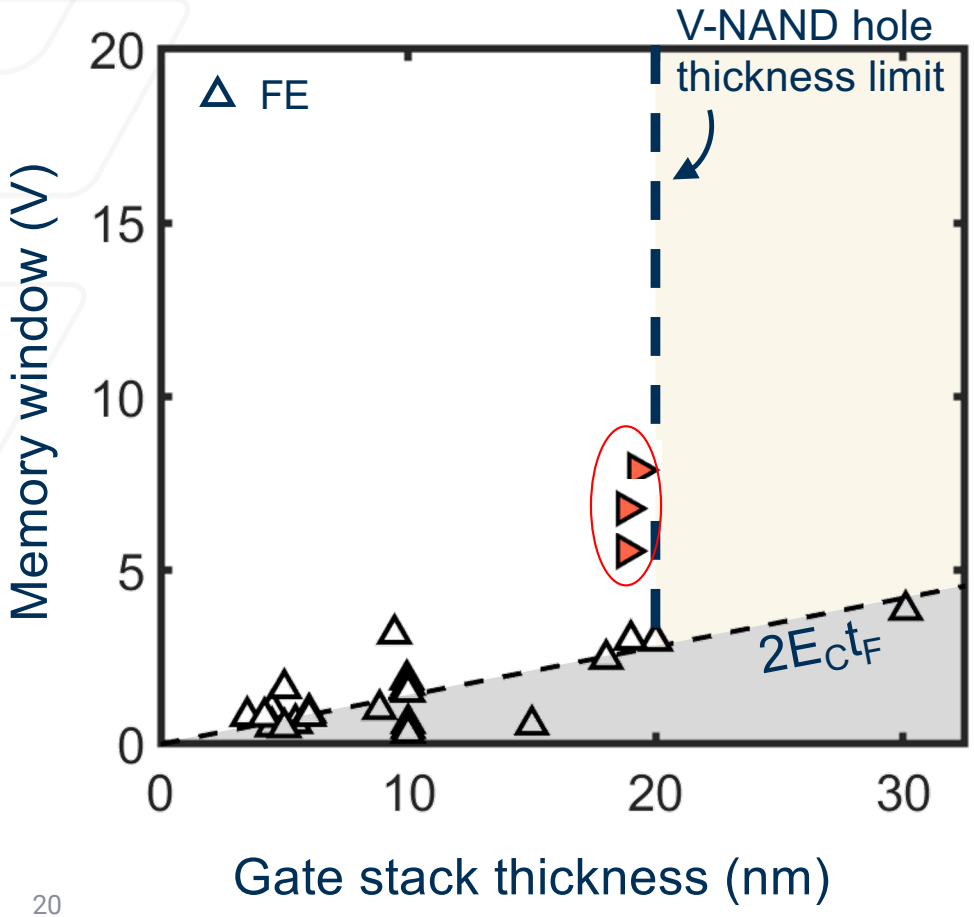


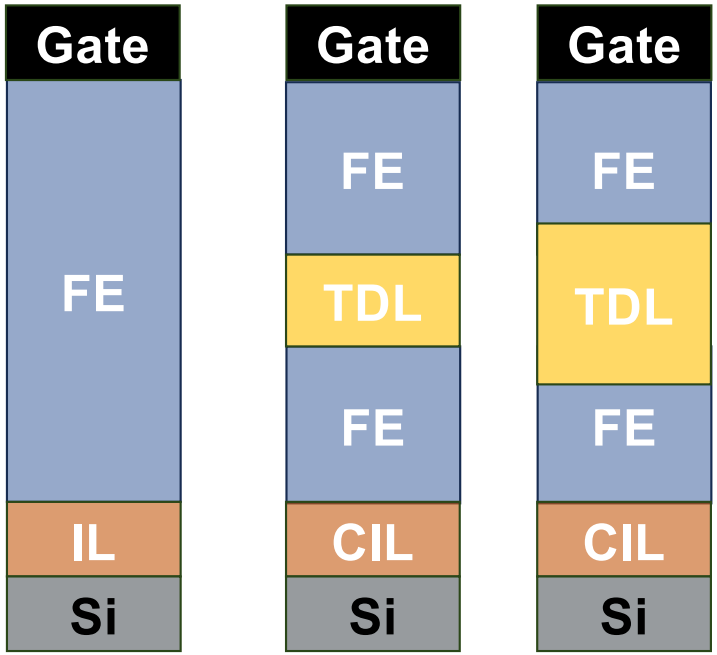


FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

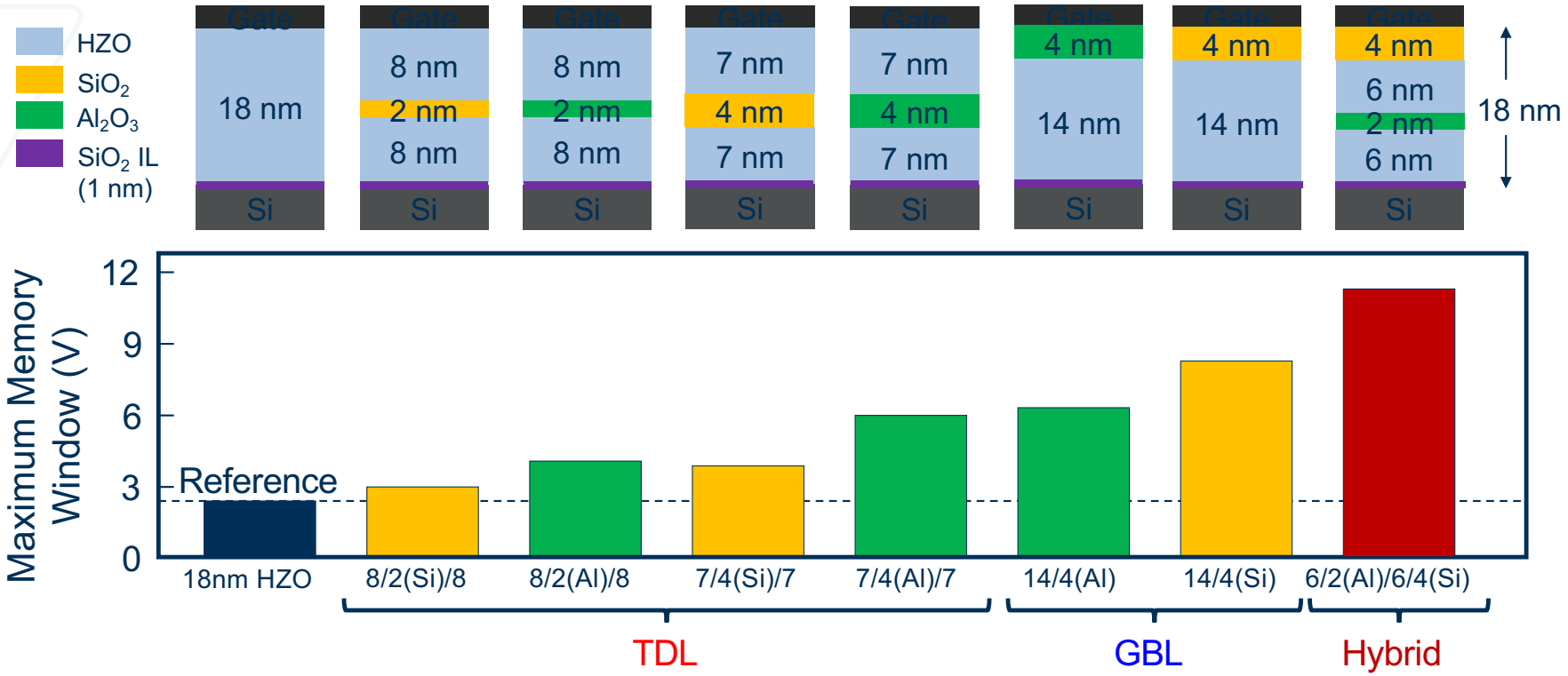
Increasing the MW by dielectric insertion





Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Position and choice of the dielectric



- GBL stacks have higher MW than TDL stacks for similar thickness and material.
- SiO_2 in GBL and Al_2O_3 in TDL gives higher MW for similar dielectric thickness

Fernandes, L., Ravindran, P. V., Song, T., Das, D., Park, C., Afroze, N., ... & Khan, A. (2024). Material choices for tunnel dielectric layer and gate blocking layer for ferroelectric NAND applications. *IEEE Electron Device Letters*.

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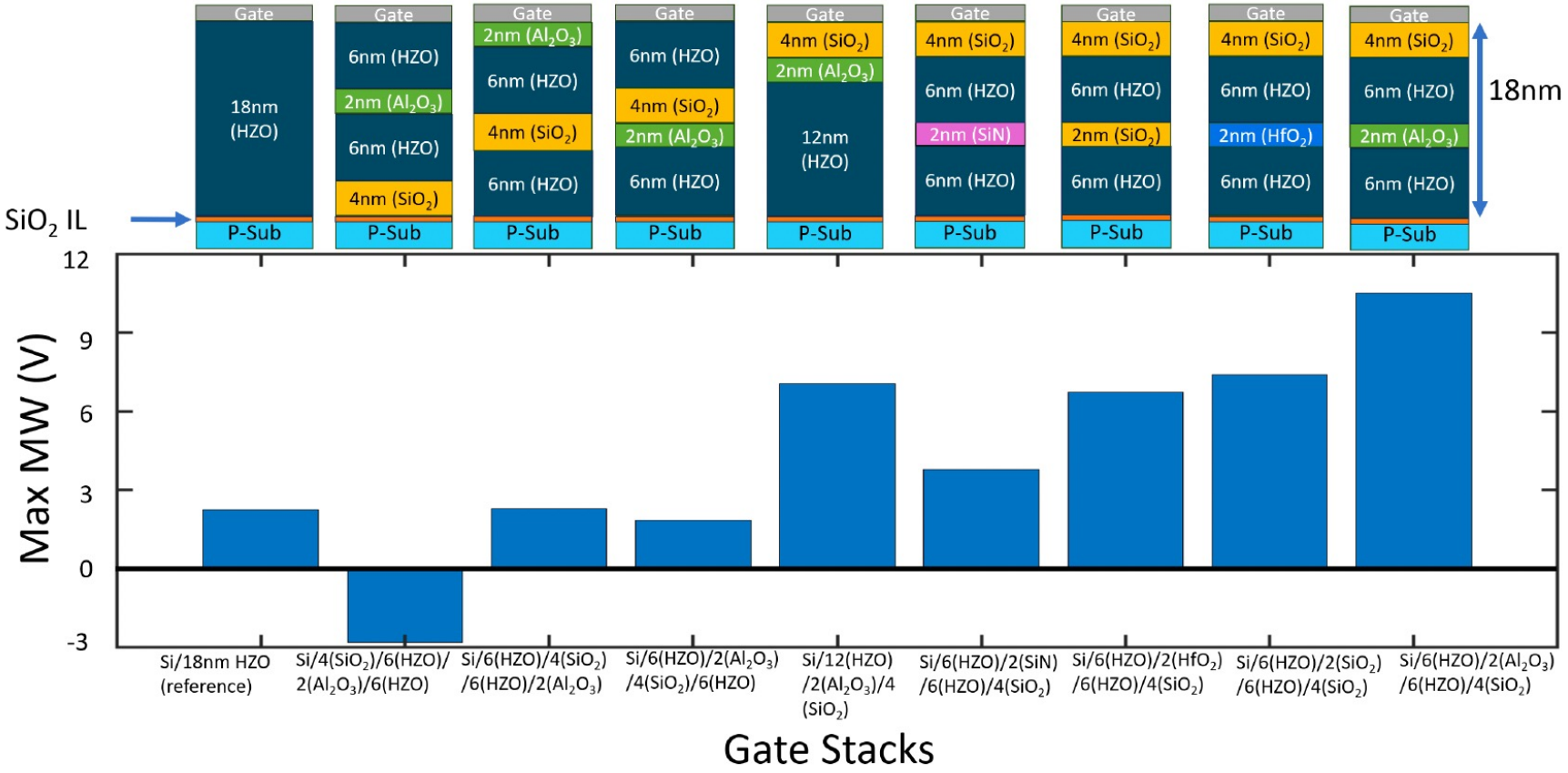

Fernandes, L., Ravindran, P. V., Chen, J., Tian, M., Das, D., Chen, H., ... & Khan, A. (2024). Optimizing Memory Window for Ferroelectric Nand Applications: An Experimental Study on Dielectric Material Selection and Layer Positioning. *IEEE Transactions on Electron Devices*.

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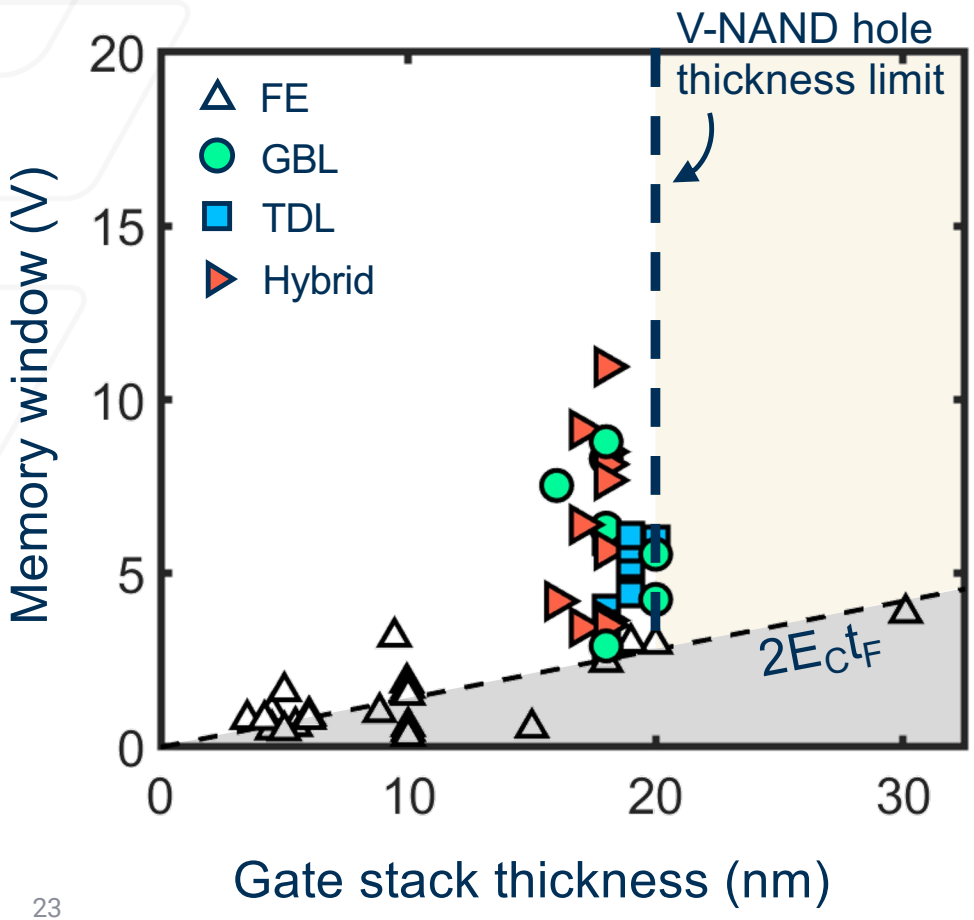
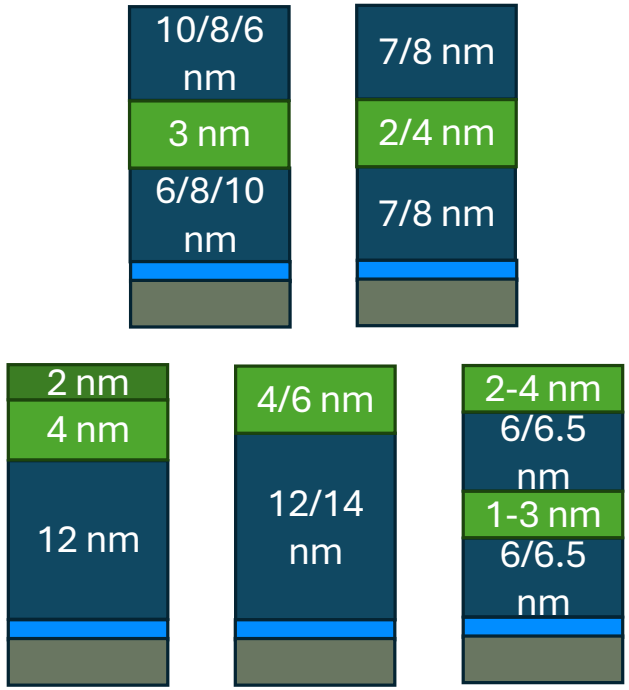
Increasing the MW by dielectric insertion

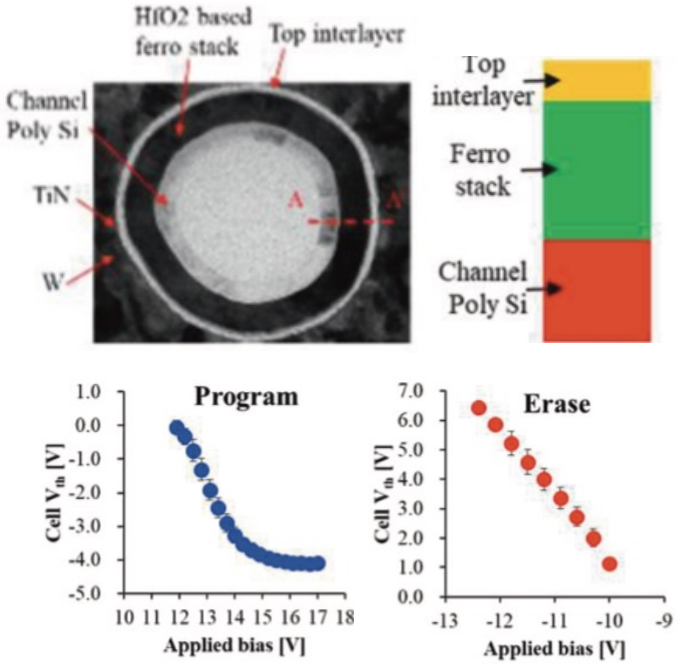




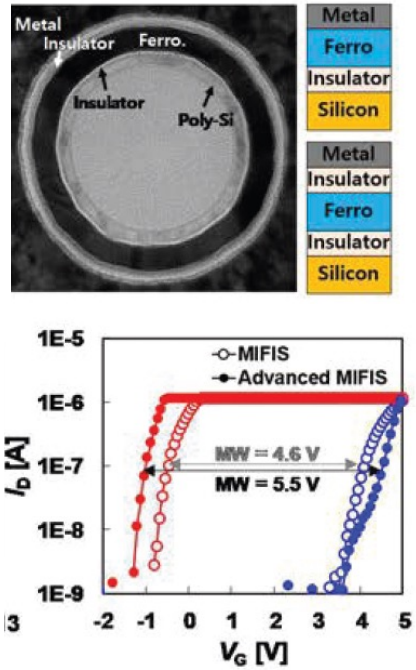
Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$
Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4
Channel IL: SiO_2
Semiconductor: Bulk Si, Poly Si, SOI, IWO

Increasing the MW by dielectric insertion

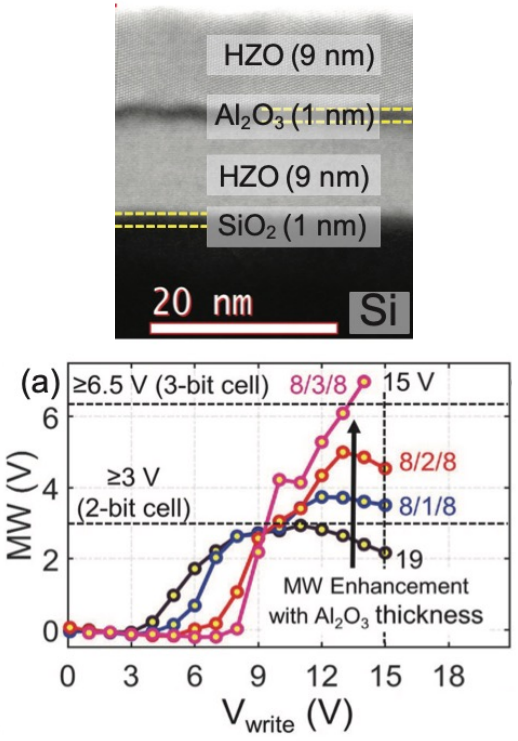
SK Hynix
Yoon et al. VLSI 2023



Samsung
Lim et al. IEDM 2023



Georgia Tech
Das et al. IEDM 2023



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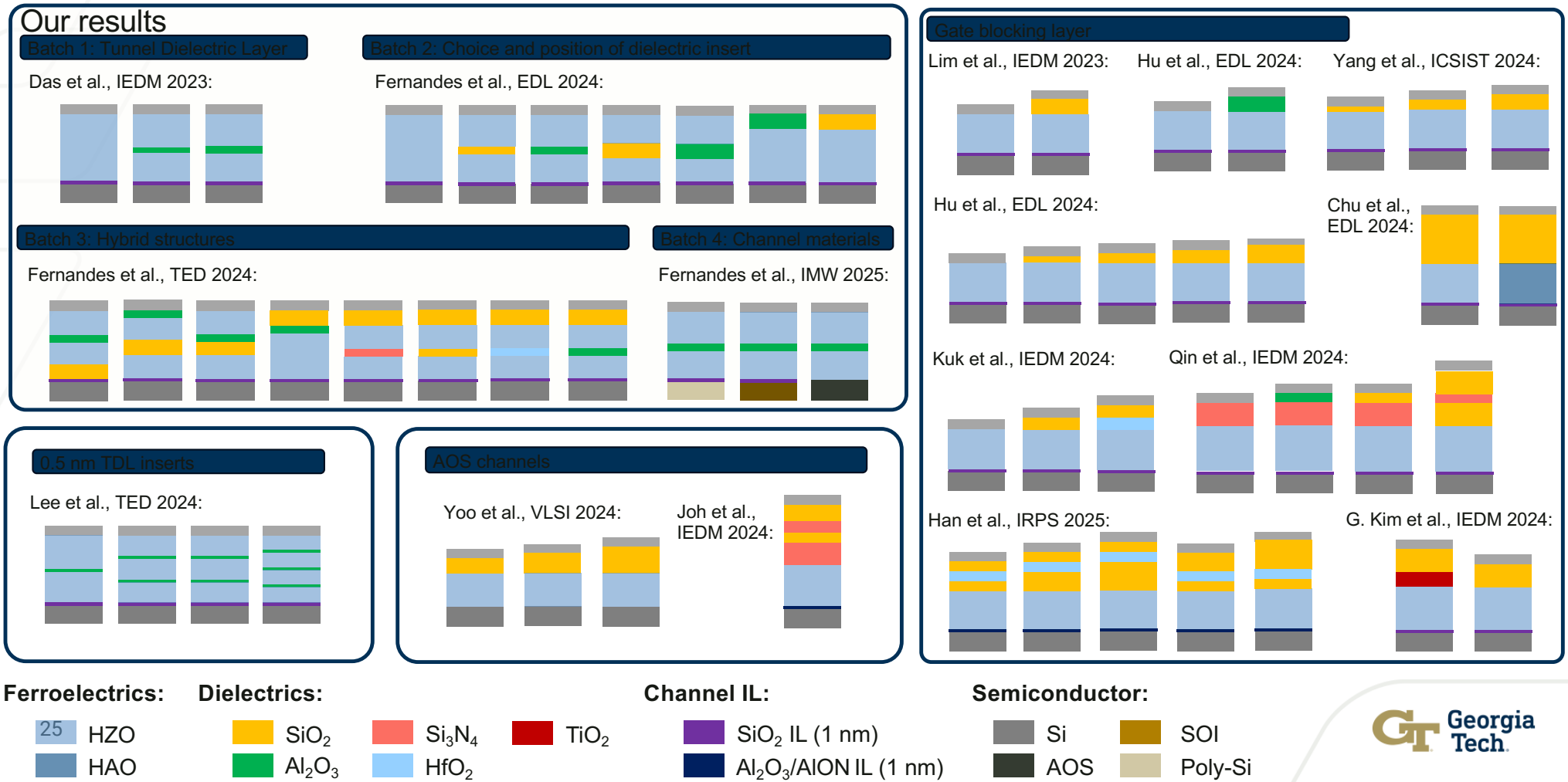

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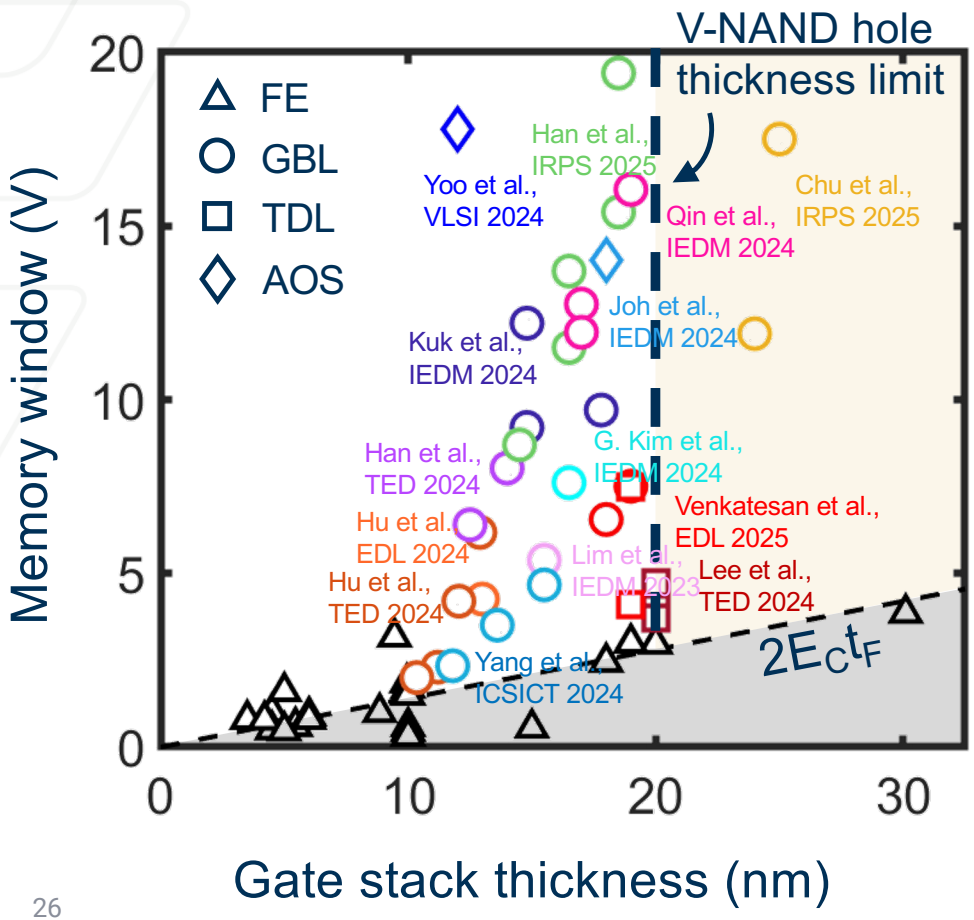
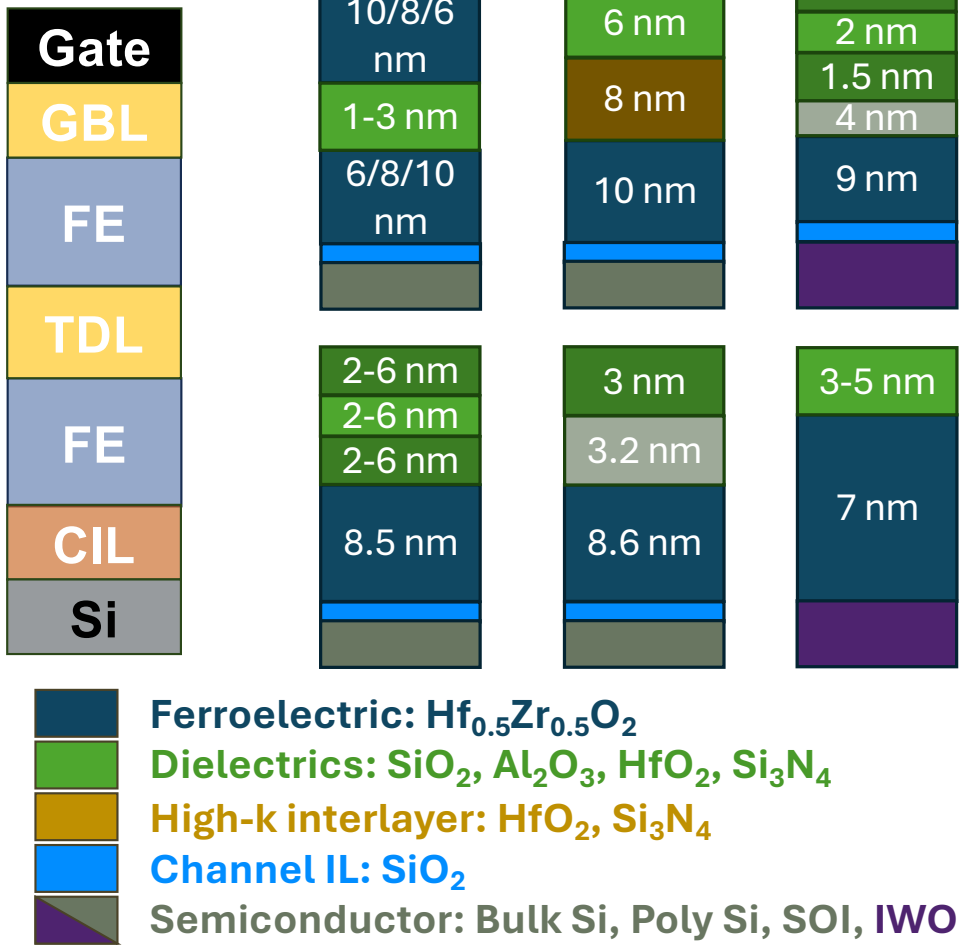




Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$

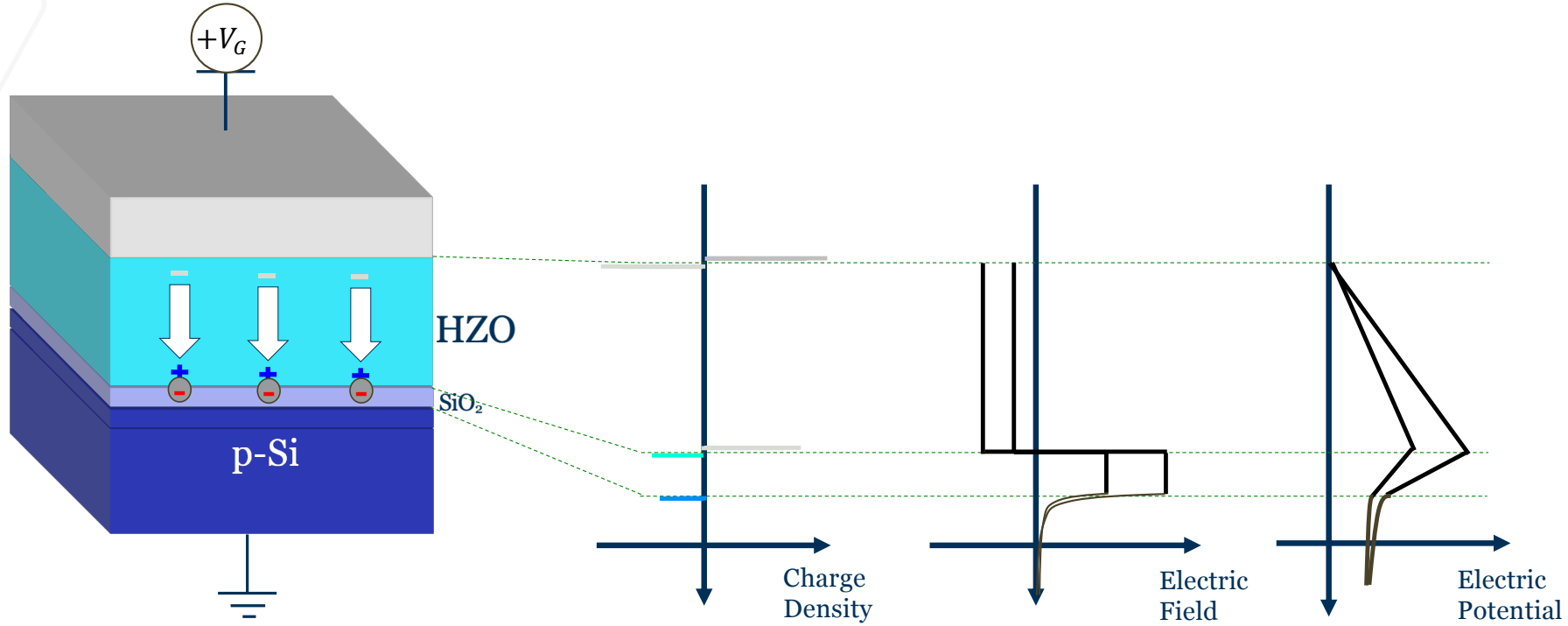
Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4

High-k interlayer: HfO_2, Si_3N_4

Channel IL: SiO_2

Semiconductor: Bulk Si, Poly Si, SOI, IWO

MW enhancement mechanism by screening charges

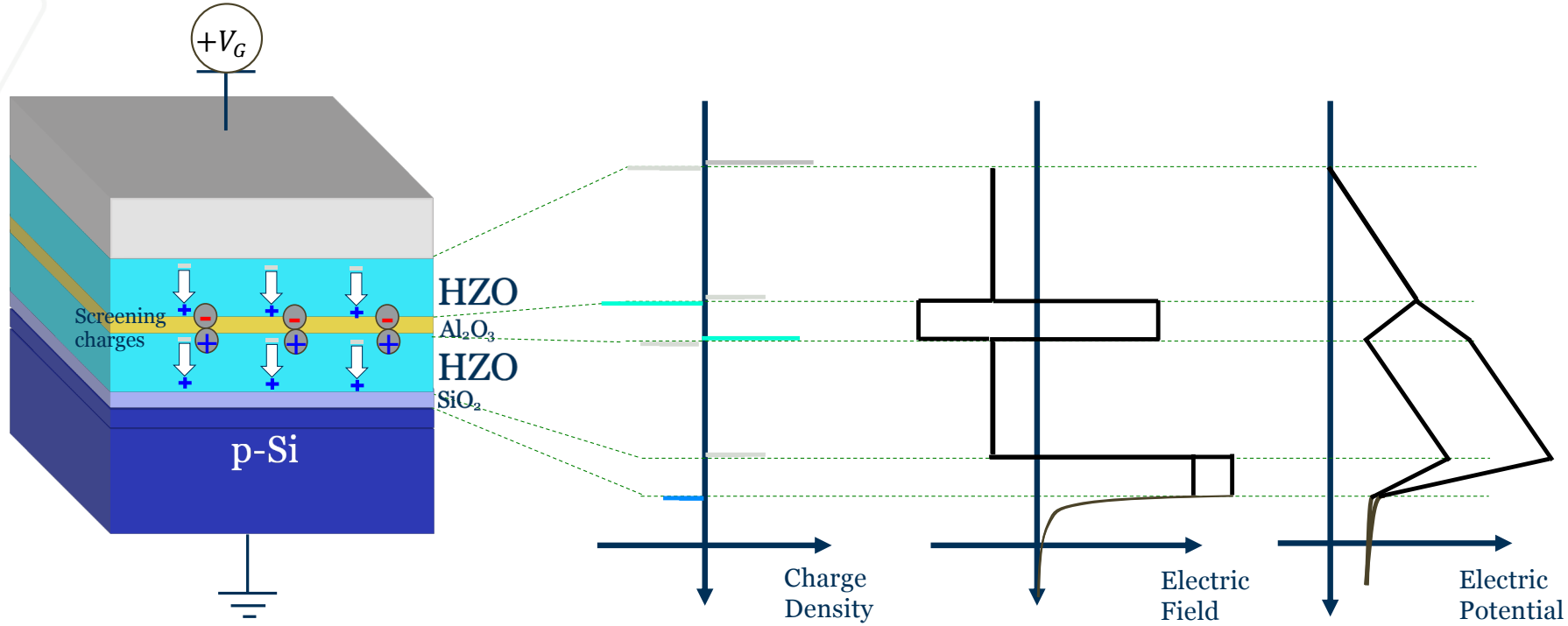


Conventional MFIS (t_{HZO} =19 nm)

- The screening of FE polarization bound charge at FE/IL interface *decreases* the MW by lowering the overall potential generated by FE bound charges

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

MW enhancement mechanism by screening charges

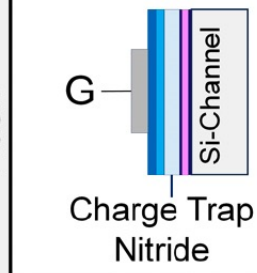
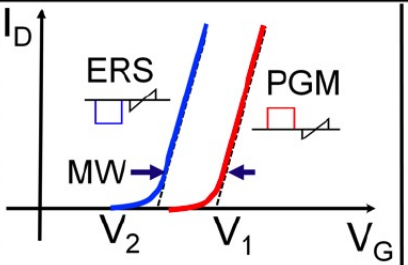
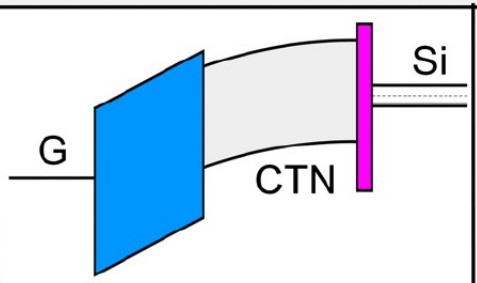
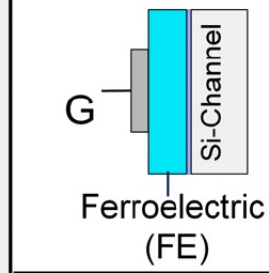
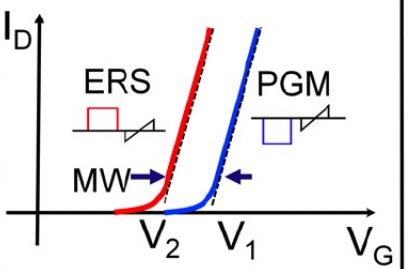
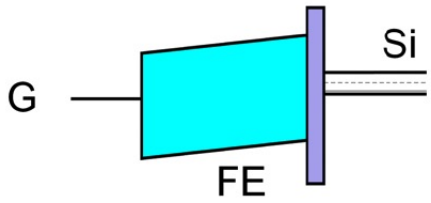
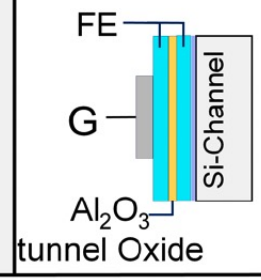
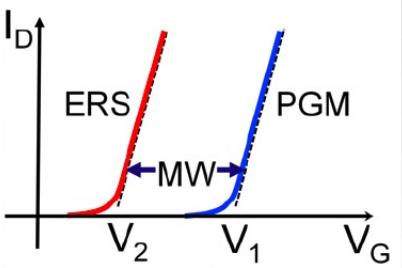
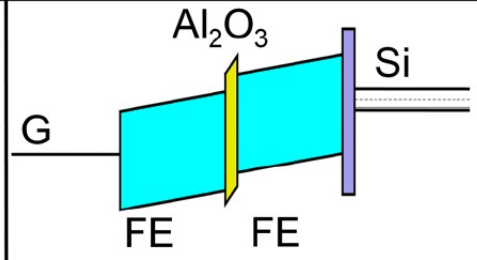


FE gate stack with TDL ($t_{HZO}/t_{ALO}/t_{HZO}$ =9/1/9 nm)

- The screening charges at interfaces between the inserted ALO layer and FE can help to *increase* the MW by inducing the additional dipoles across the TDL in the same direction as FE polarization.

Das, Khan, et al. IEDM 2023 (highlight paper): 10.1109/IEDM45741.2023.10413697

Charge trap flash vs ferroelectric flash

	Structure	Characteristics	Band diagram at FB condition	Attributes
Charge Trap Flash				✓ Large MW × Large Write Voltage Mechanism: Trapping
Conventional FEFET				× Low MW ✓ Low Write Voltage Mechanism: Polarization Switching
Proposed FEFET				✓ Large MW ✓ Moderate Write Voltage Mechanism: Polarization Switching + Trapping + Tunneling

Das, Khan, et al. IEDM 2023 (highlight paper): [10.1109/IEDM45741.2023.10413697](https://doi.org/10.1109/IEDM45741.2023.10413697)

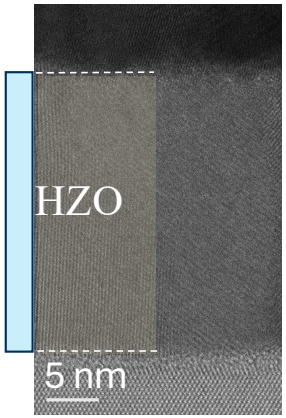
What about reliability of ferroelectric NAND?

1. Retention
2. Disturb
3. Write endurance
4. Lateral charge migration
5. Device-device variation

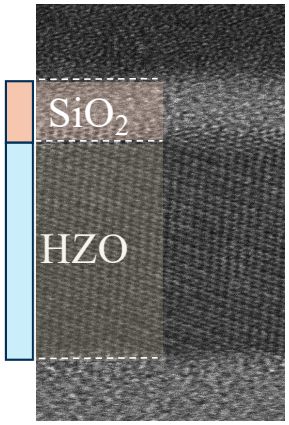
⋮

Ferroelectric NAND gate stacks

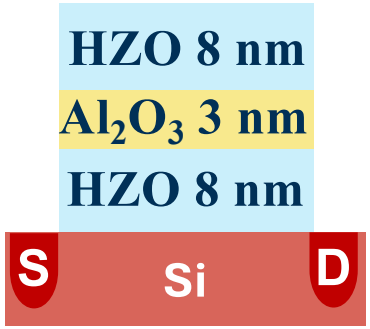
FE (reference)

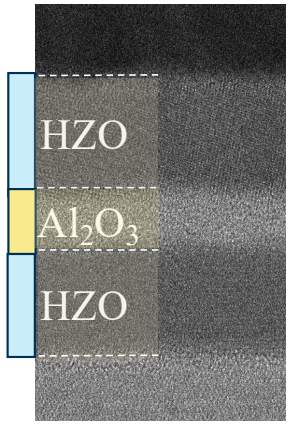


Gate blocking layer (GBL) 14/4(Si)



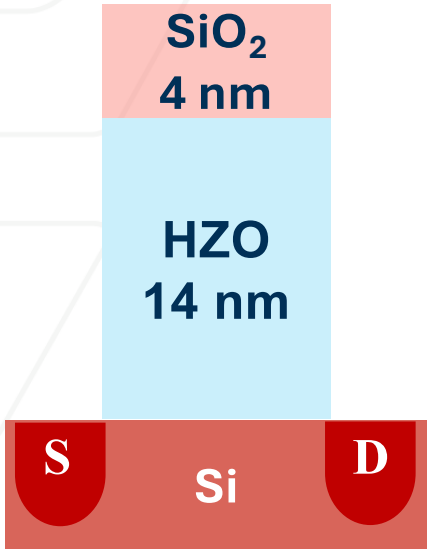
Tunnel dielectric layer (TDL) 8/3(Al)/8

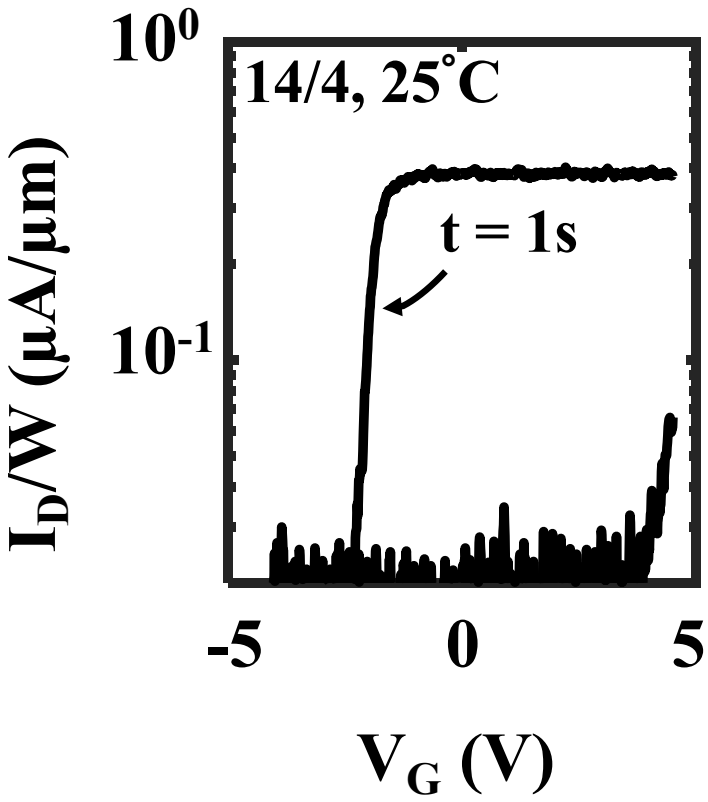


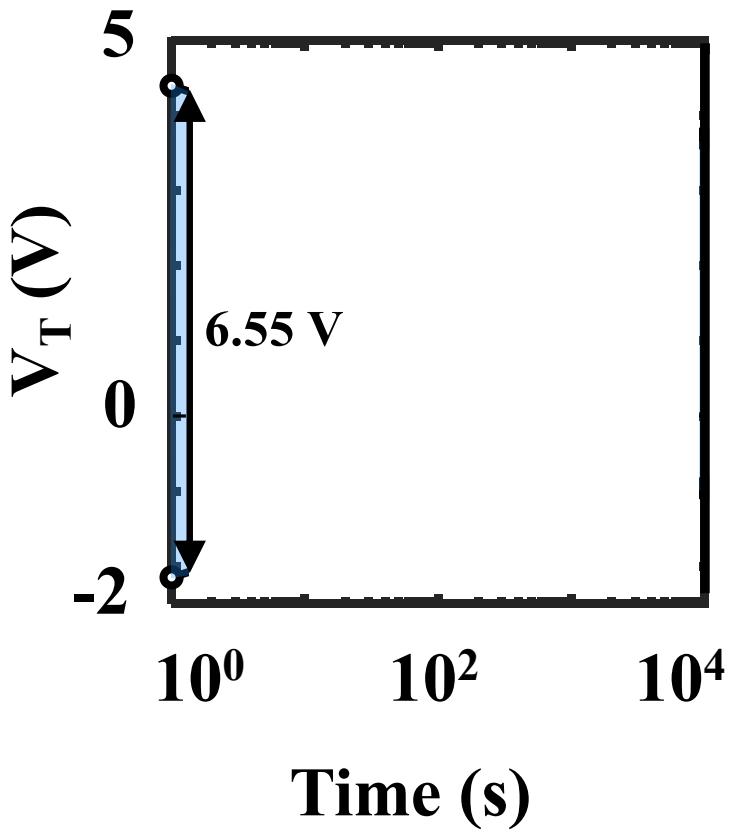


Venkatesan, Khan, et al. IRPS 2025 (Best Student Paper): https://doi.org/10.1109/IRPS48204.2025.10982749
Venkatesan, Khan, et al. EDL 2025 (Editor's Pick): 10.1109/LED.2024.3523235

Retention characterization







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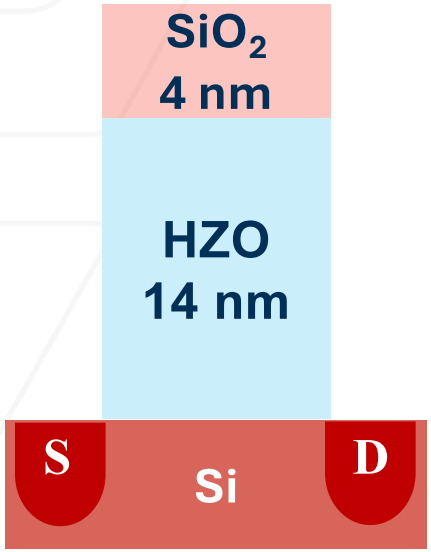

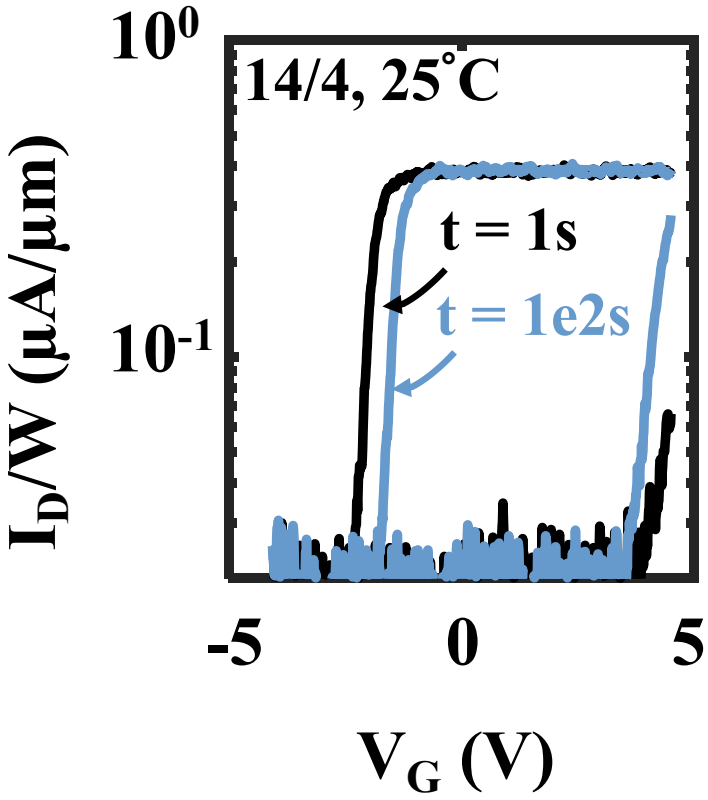

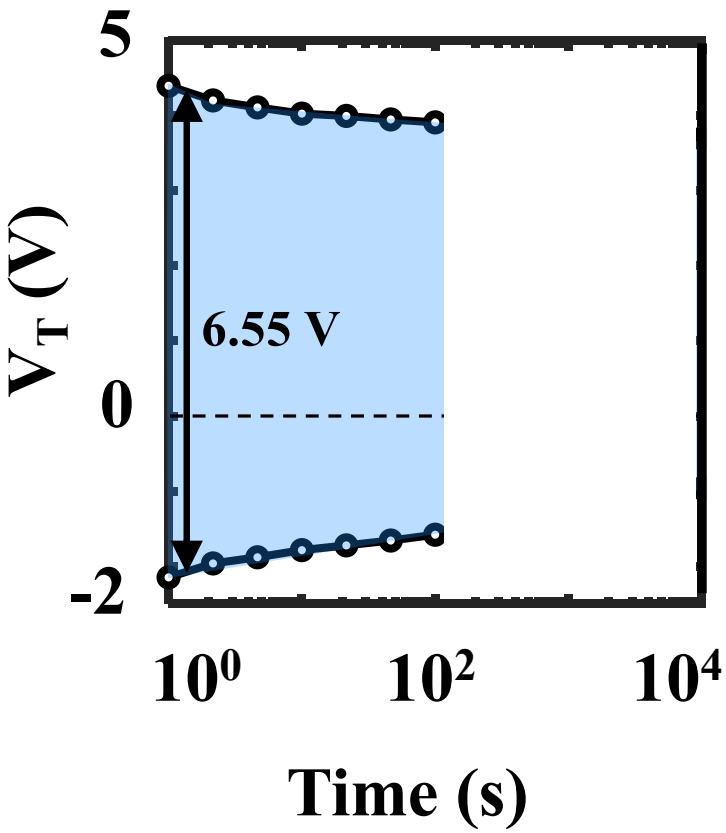

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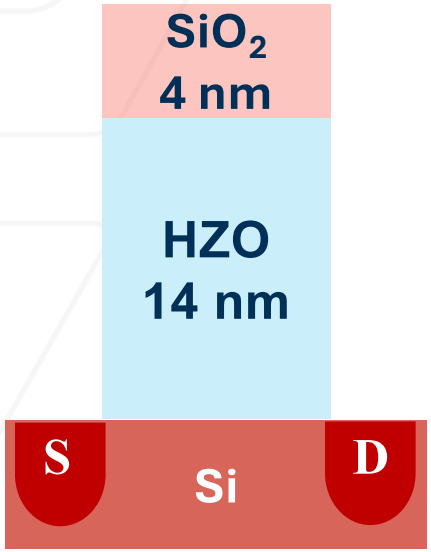
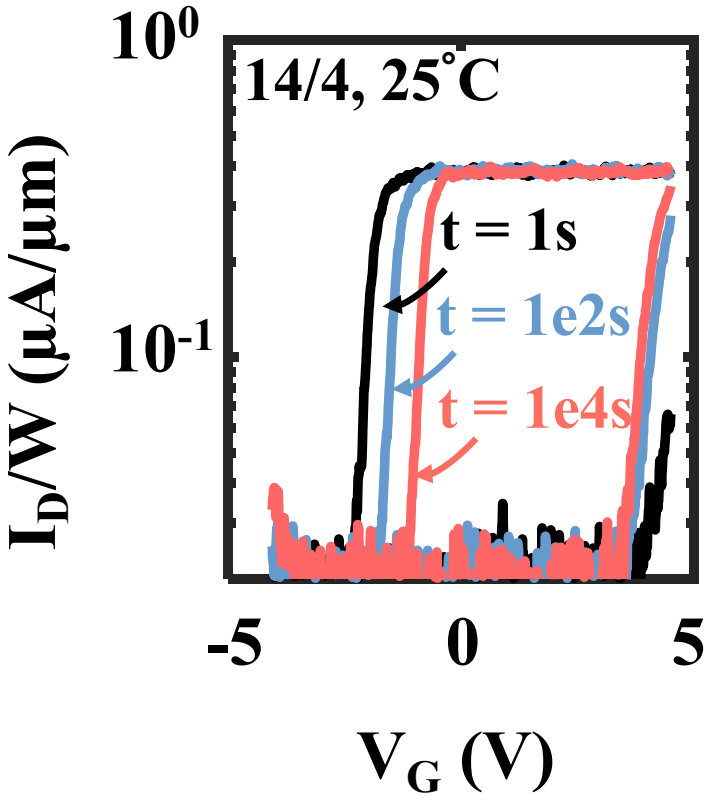
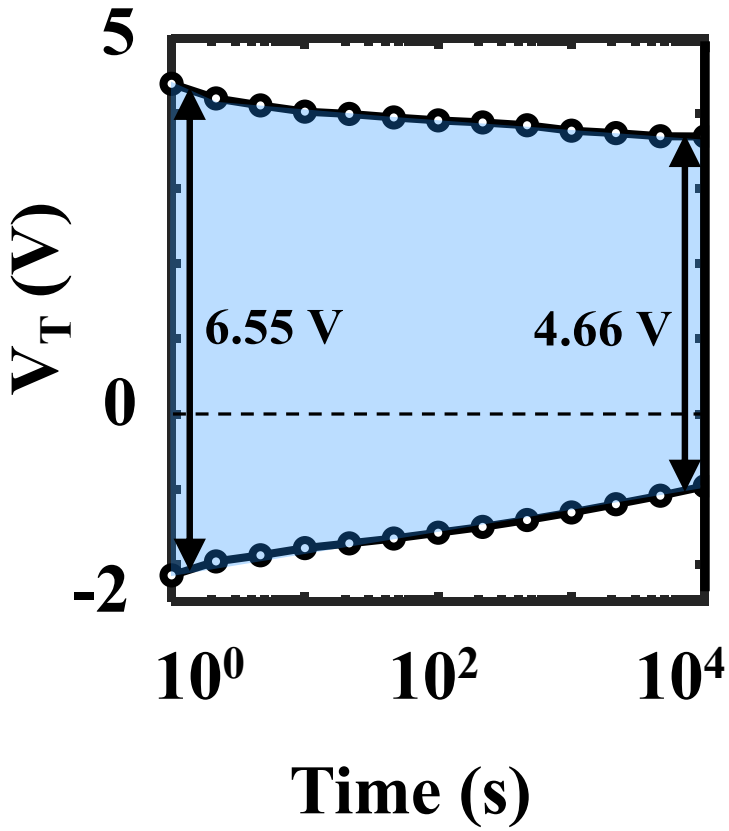
Retention characterization







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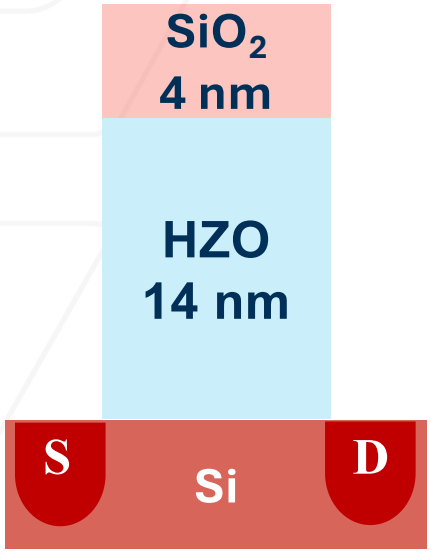
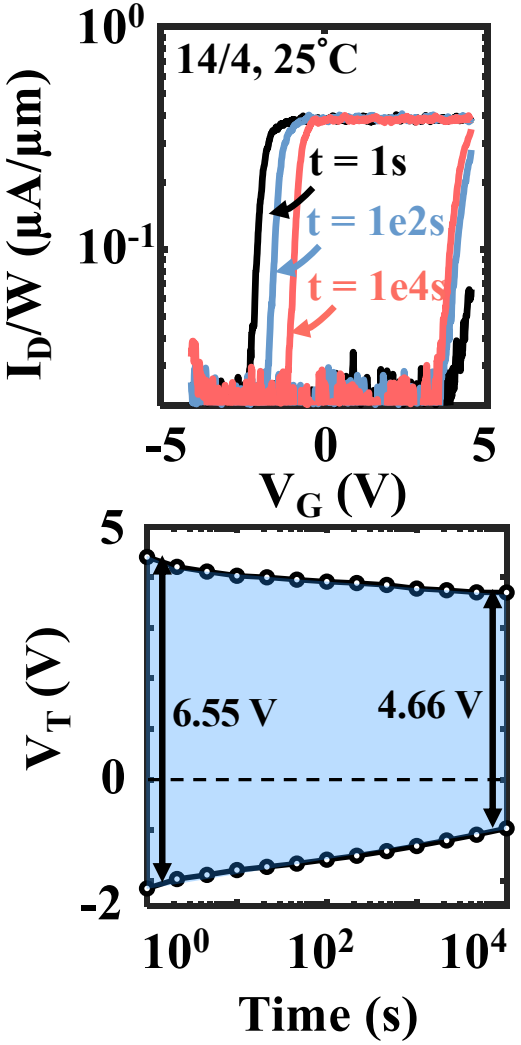
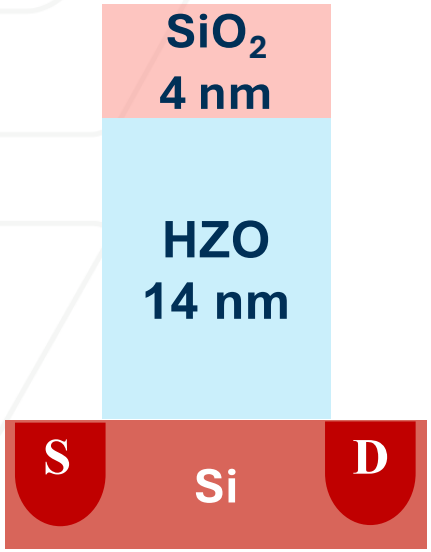
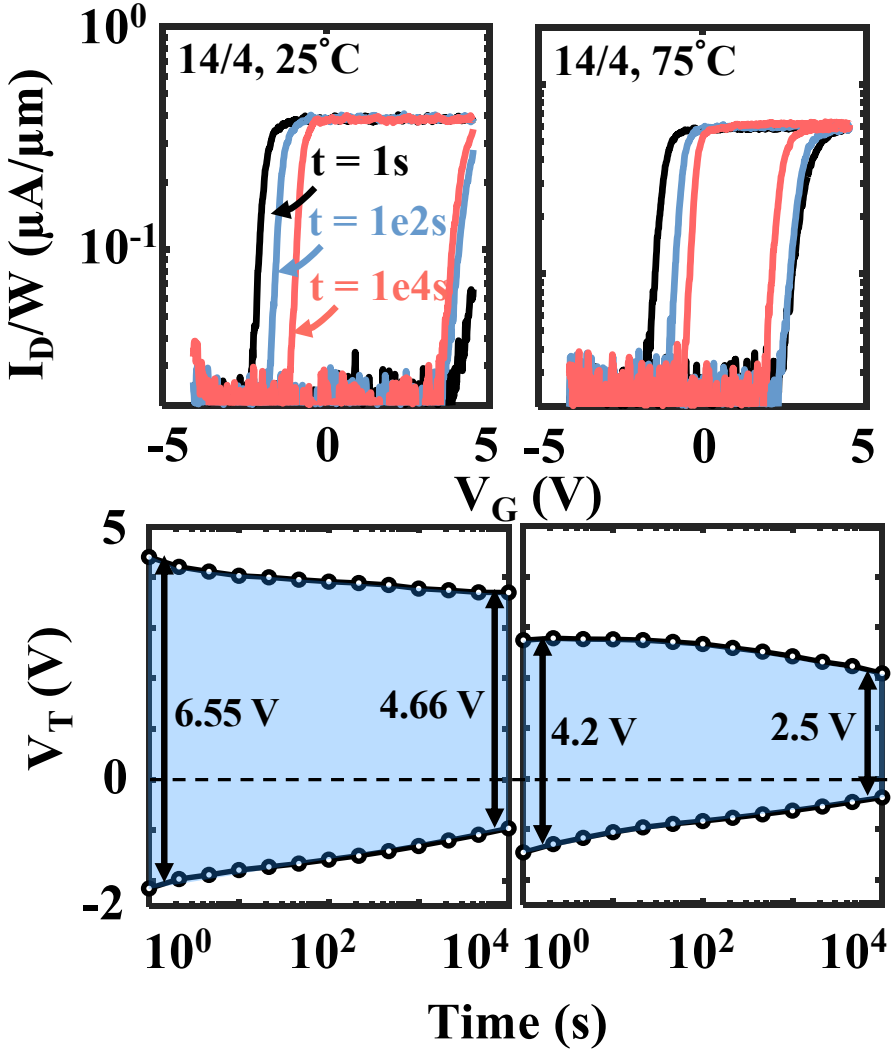




Retention characterization





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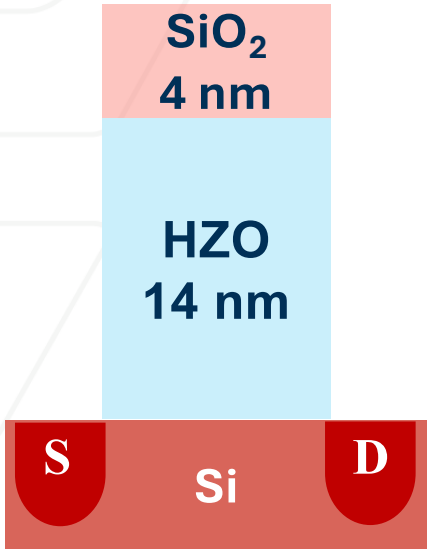
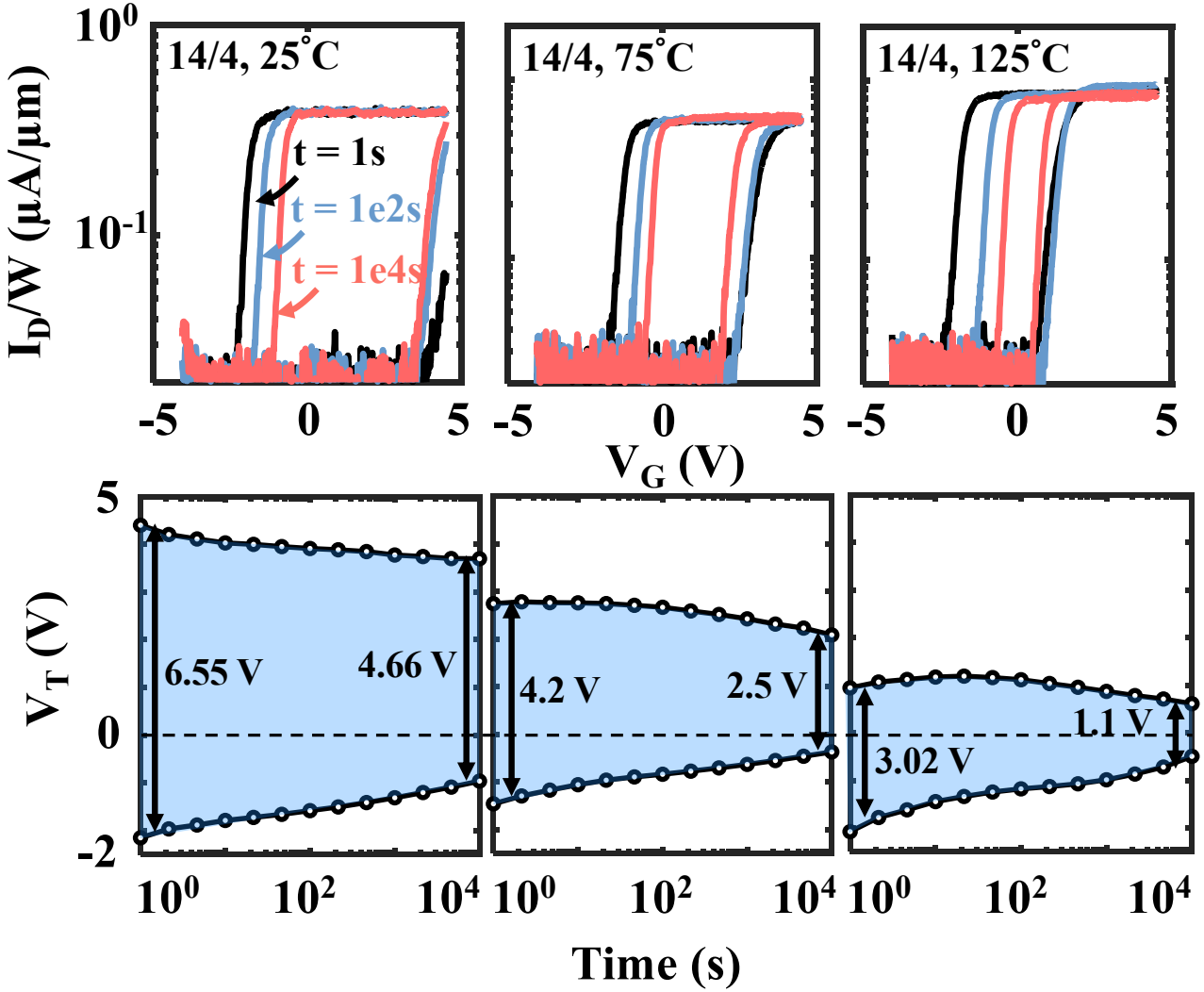
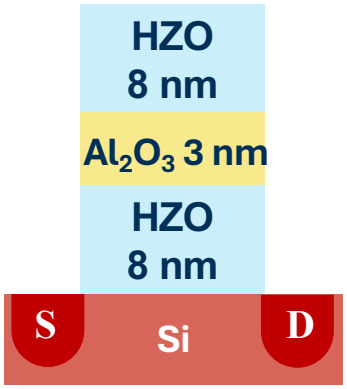
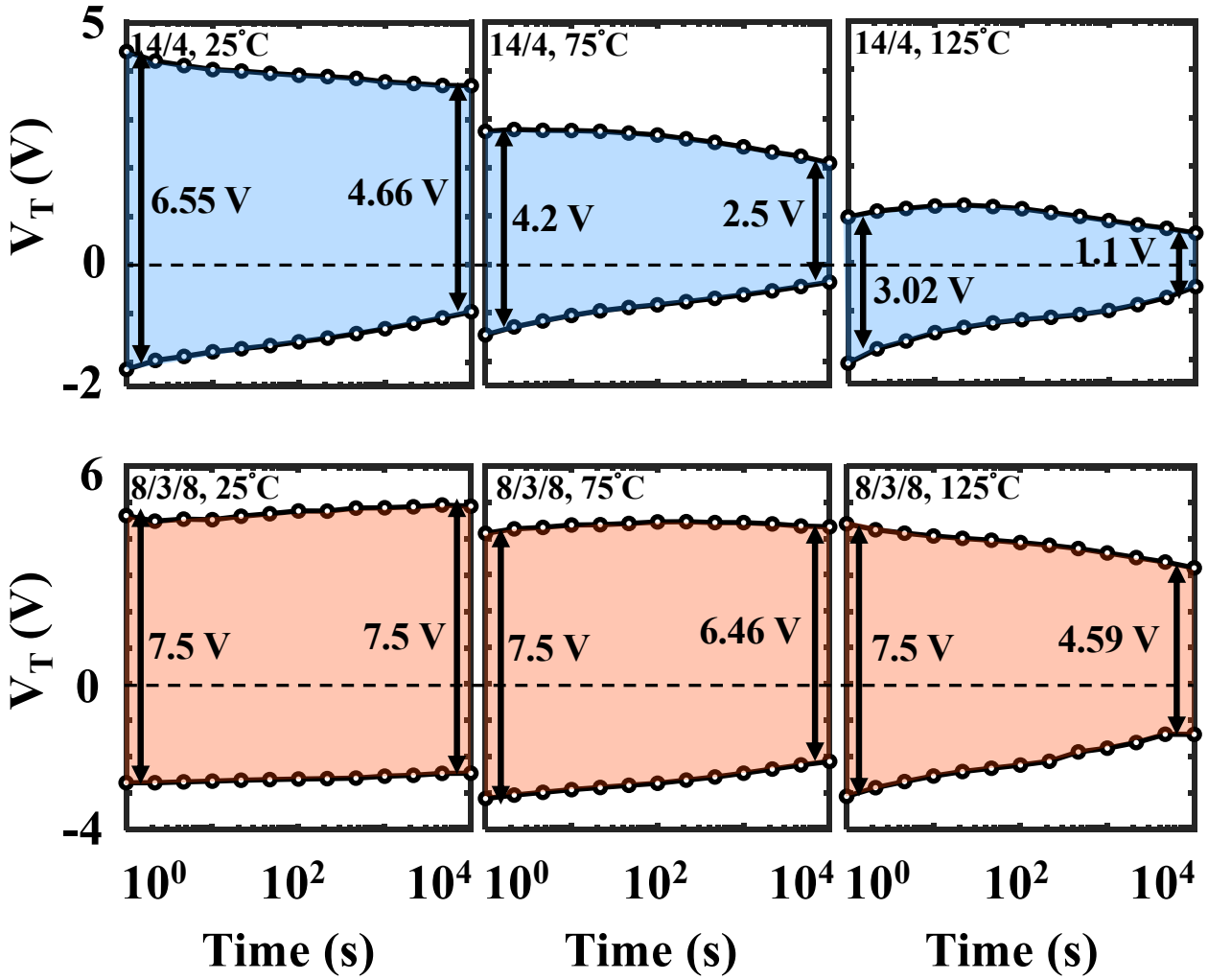


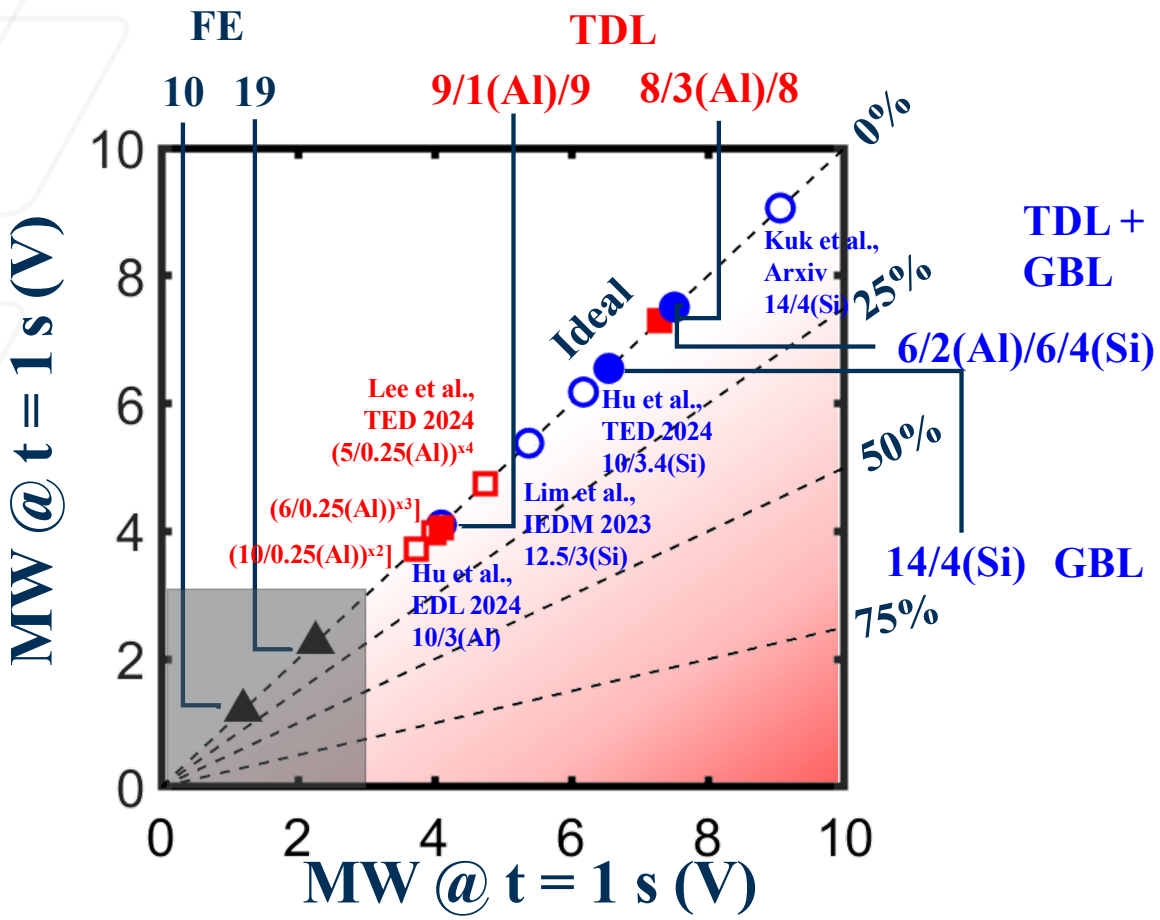


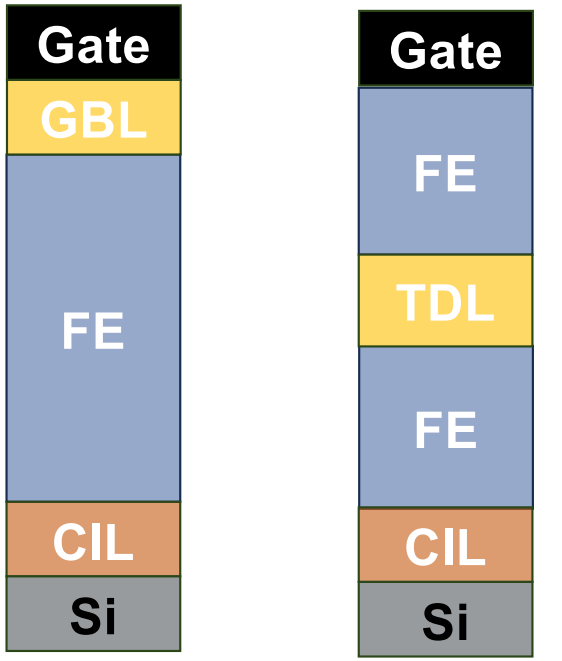
Retention characterization





MW loss in FE-NAND





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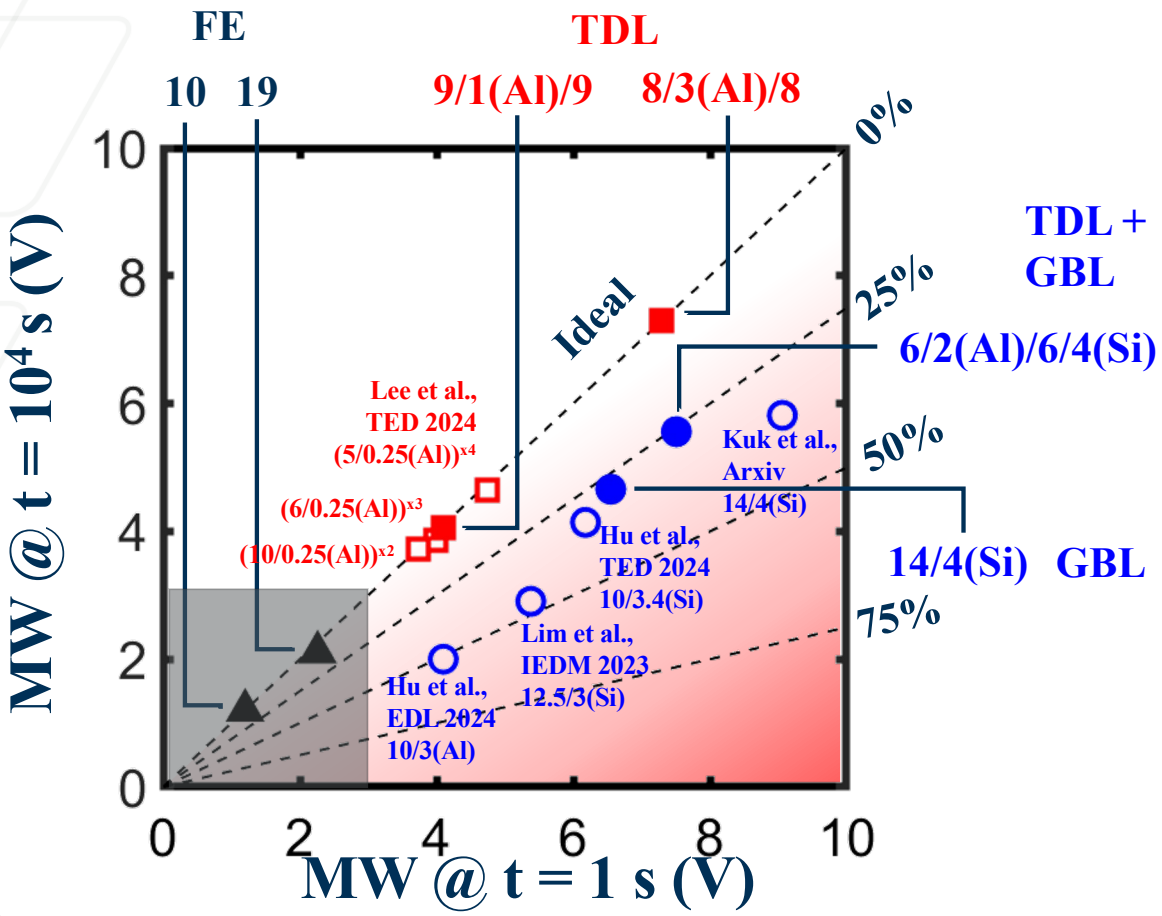
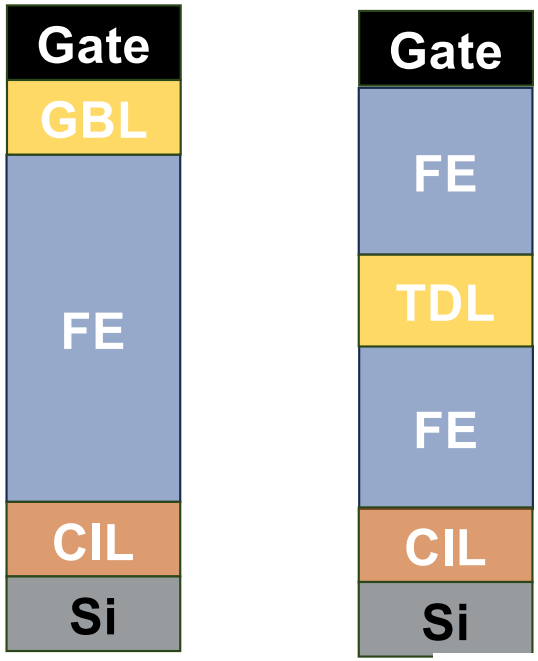
MW loss in FE-NAND





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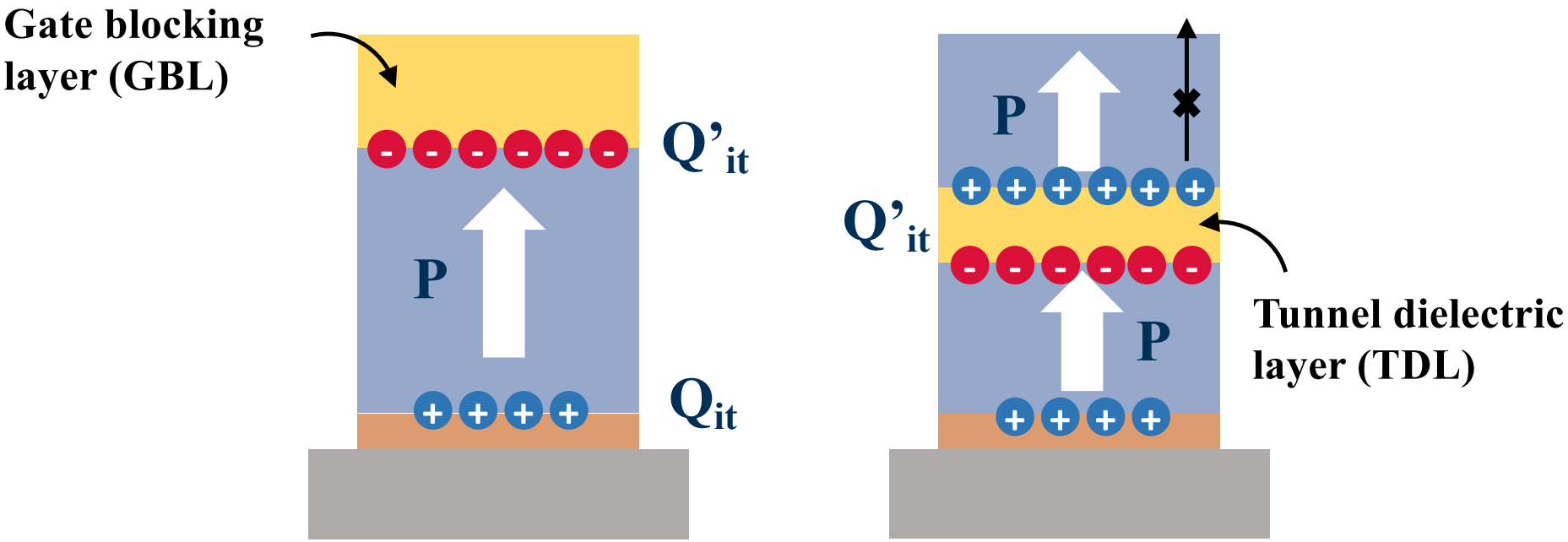
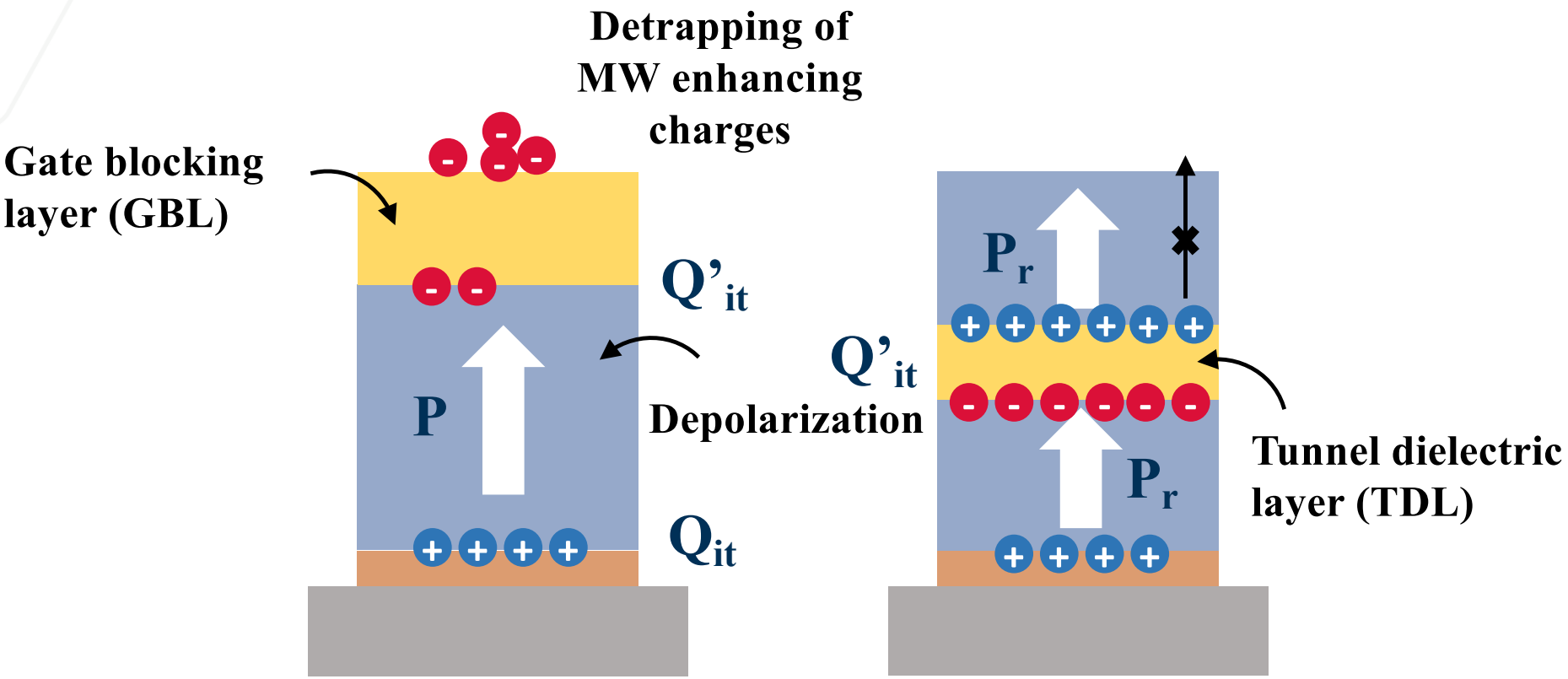
Detrapping mechanisms



Venkatesan, P., Padovani, A., ... & Khan, A. (2025). Enhanced Memory Performance in Ferroelectric NAND applications: The Role of Tunnel Dielectric position for Robust 10-year Retention. In *2025 IEEE International Reliability Physics Symposium (IRPS)* (pp. 1-6). IEEE. *(Highlighted paper)*

Retention loss mechanisms



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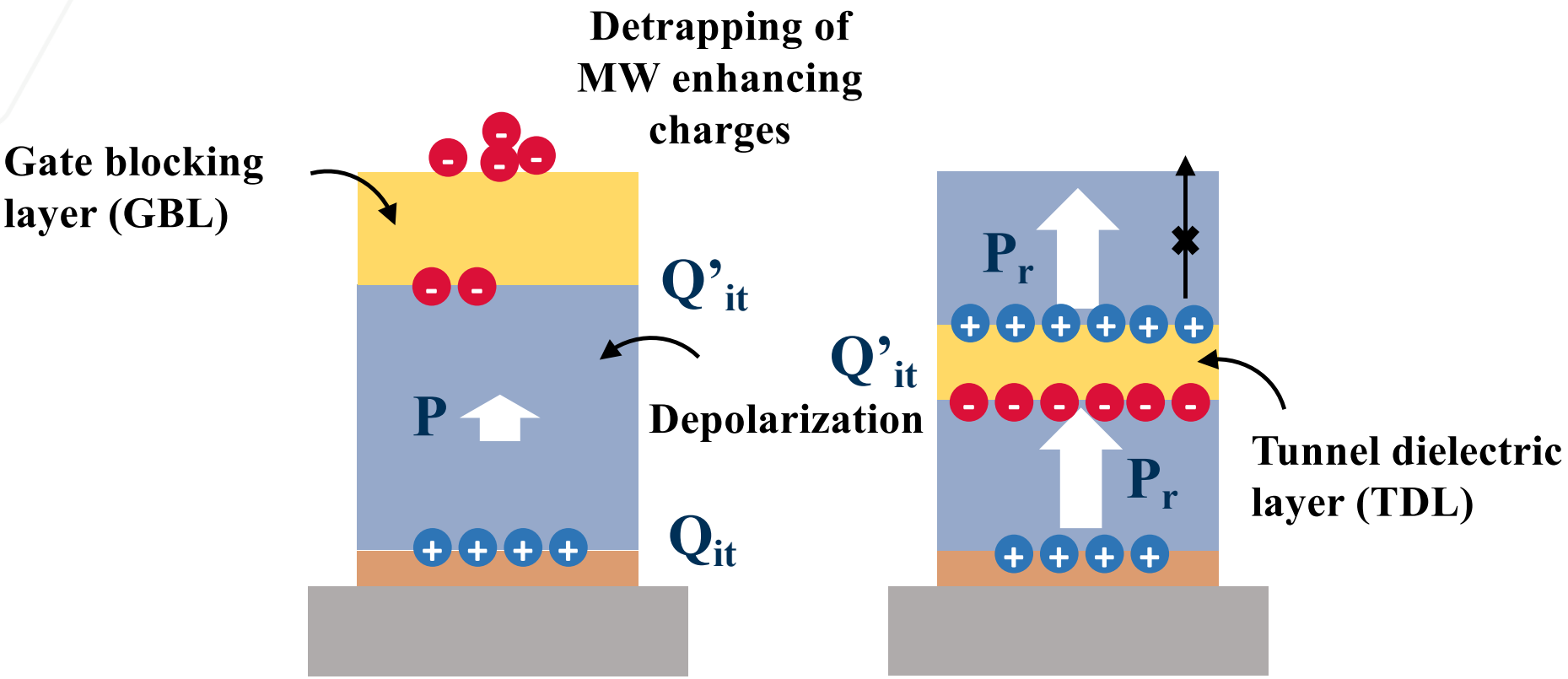
Retention loss mechanisms



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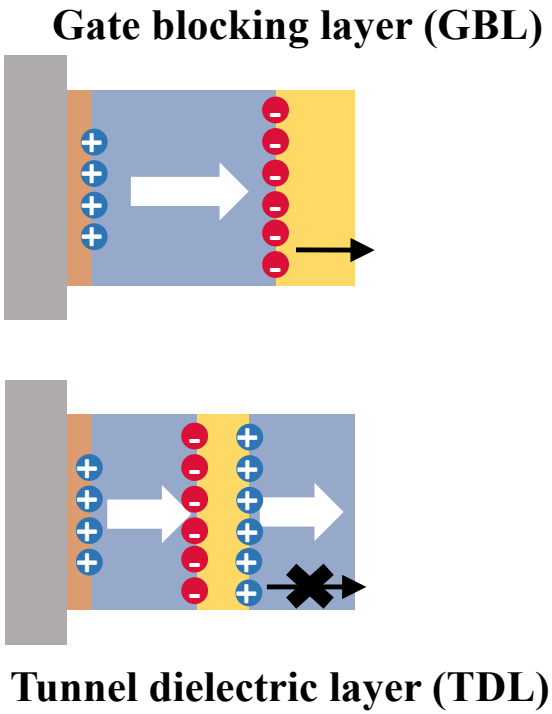
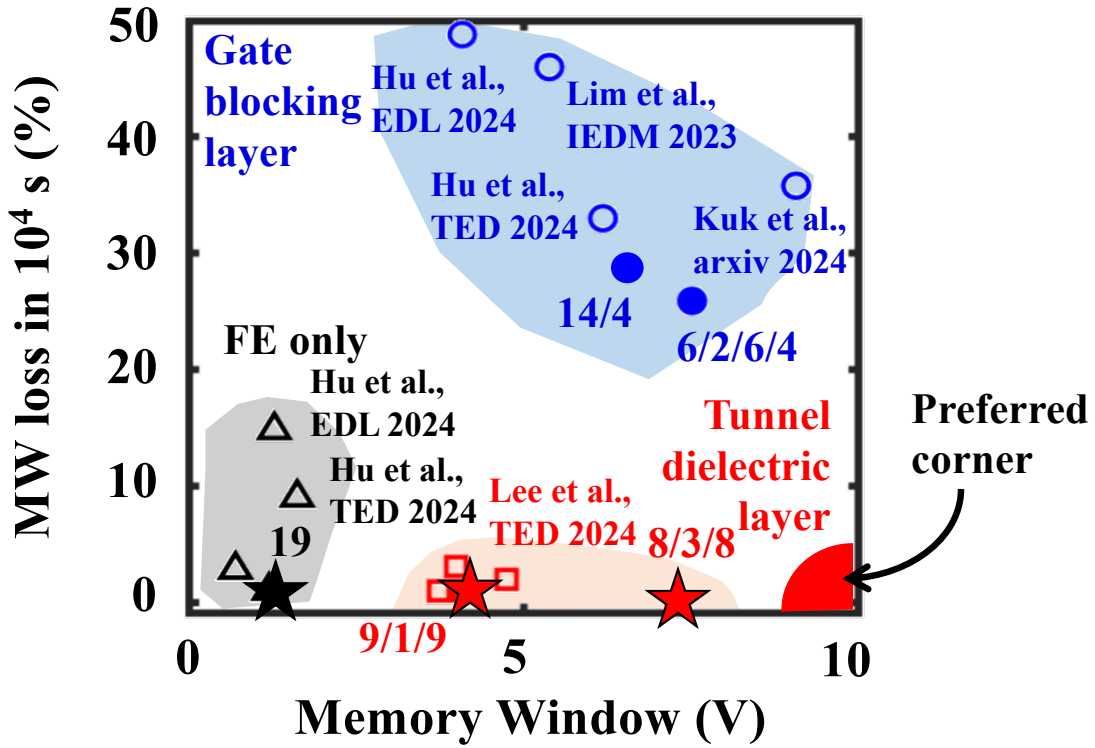
Retention benchmark

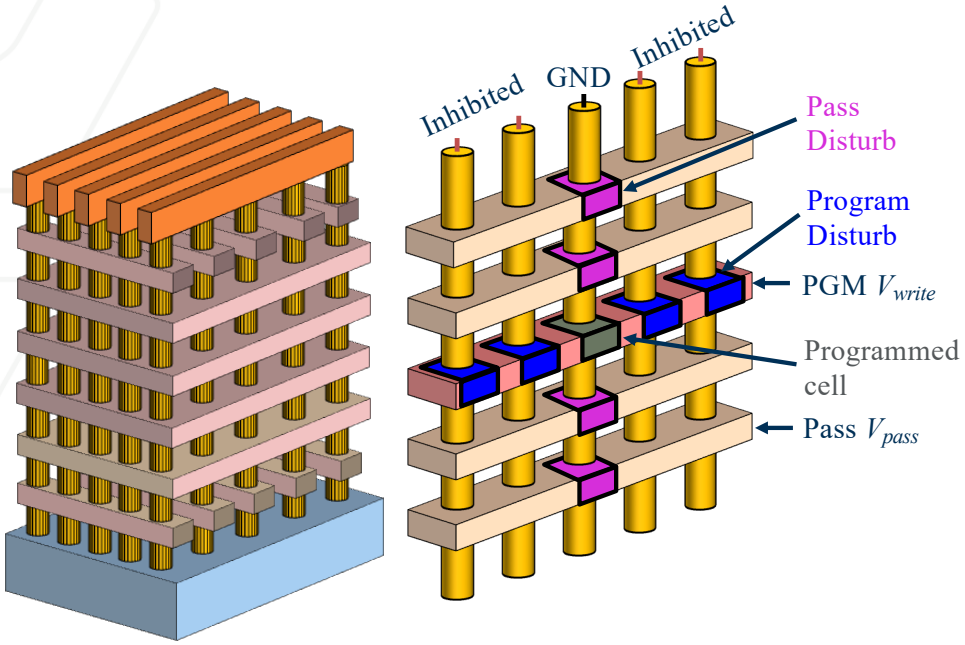




Venkatesan, P., et al.
IRPS 2025

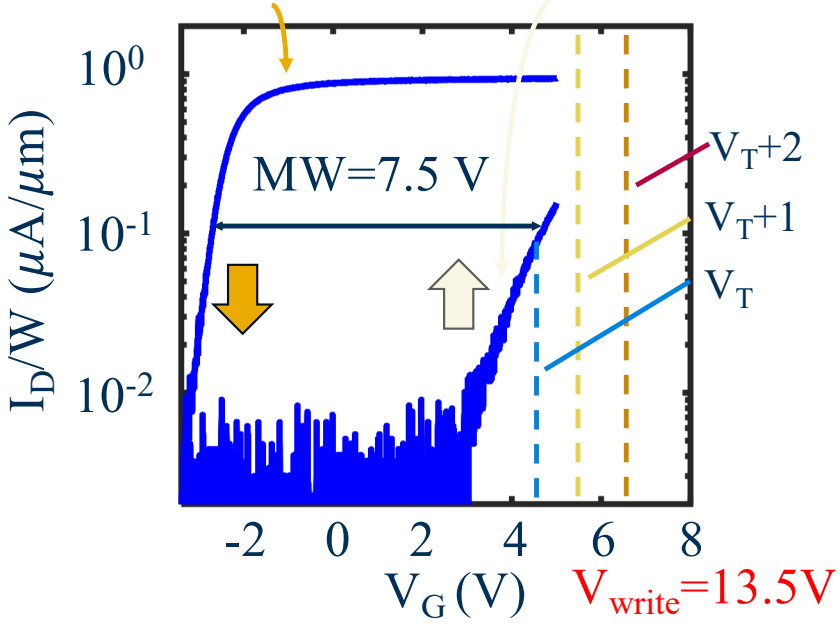
Moving the dielectric to the middle of the FE gate stack, energetically stabilizes the MW.

Pass disturb



PGM state: possibility of electron trapping

ERS state: possibility of polarization back flip

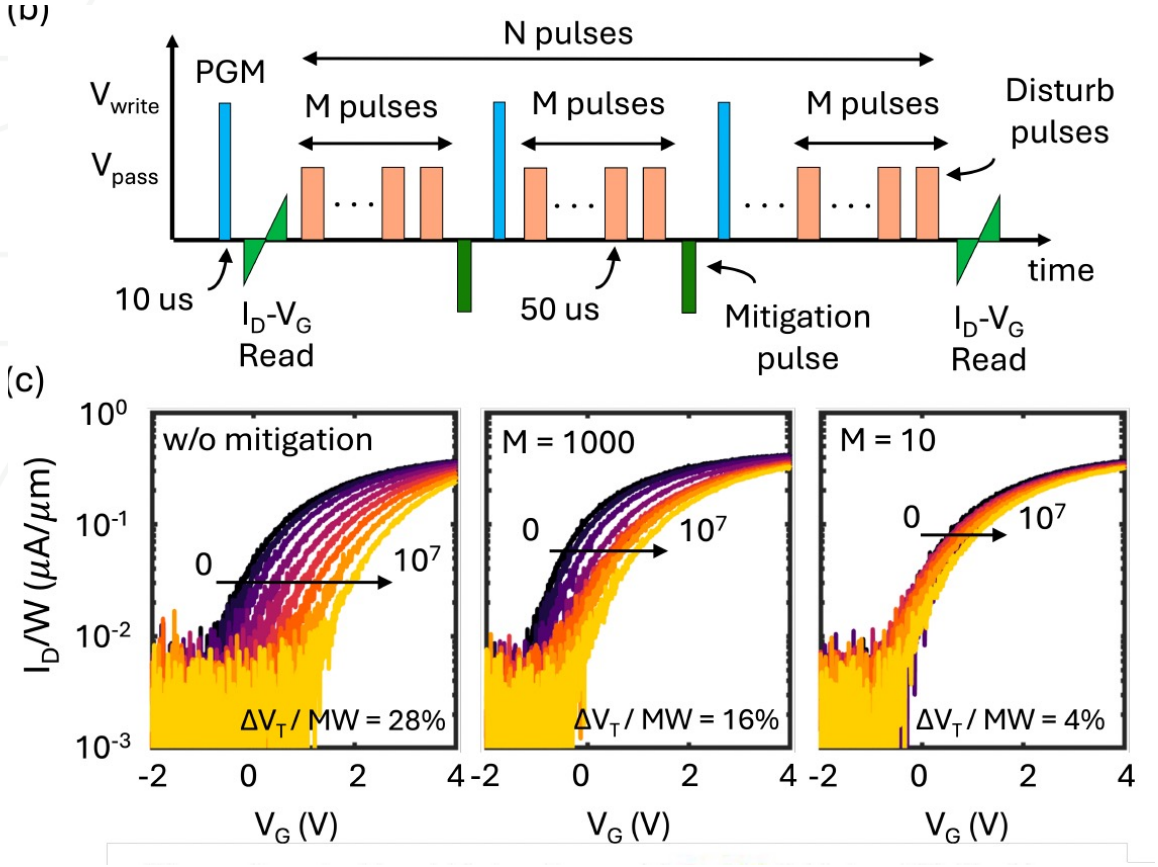


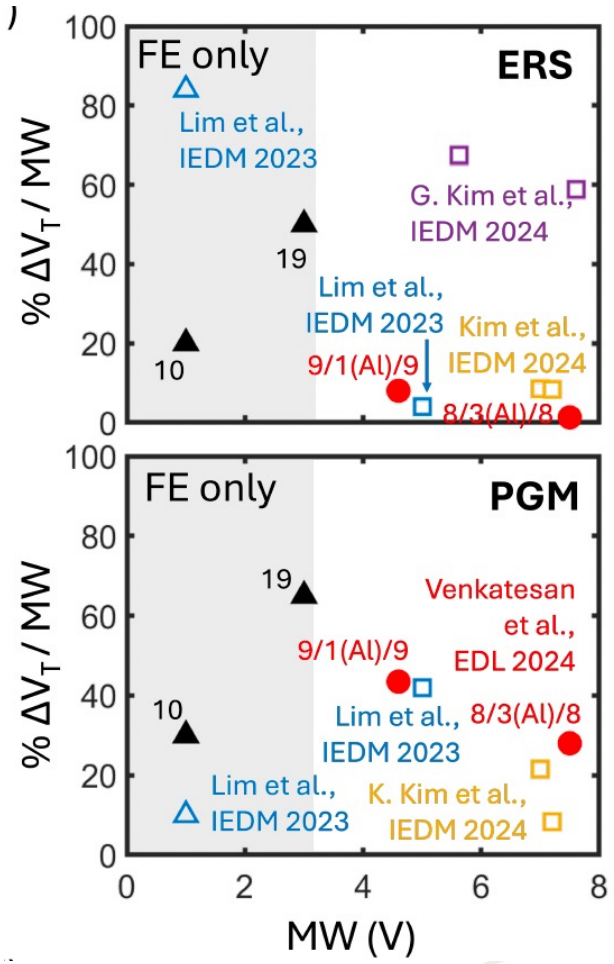
A pass voltage is applied to unaddressed cells while accessing a different cell along the bit line. This pass voltage could disturb the V_T of the cell either due to electron trapping or polarization back switching.

Venkatesan, P., Park, C., Song, T., Fernandes, L., Das, D., Afroze, N., ... & Khan, A. (2024). Disturb and its mitigation in Ferroelectric Field-Effect Transistors with Large Memory Window for NAND Flash Applications. *IEEE Electron Device Letters*. [Editors' Pick]

Georgia Tech

Pass disturb



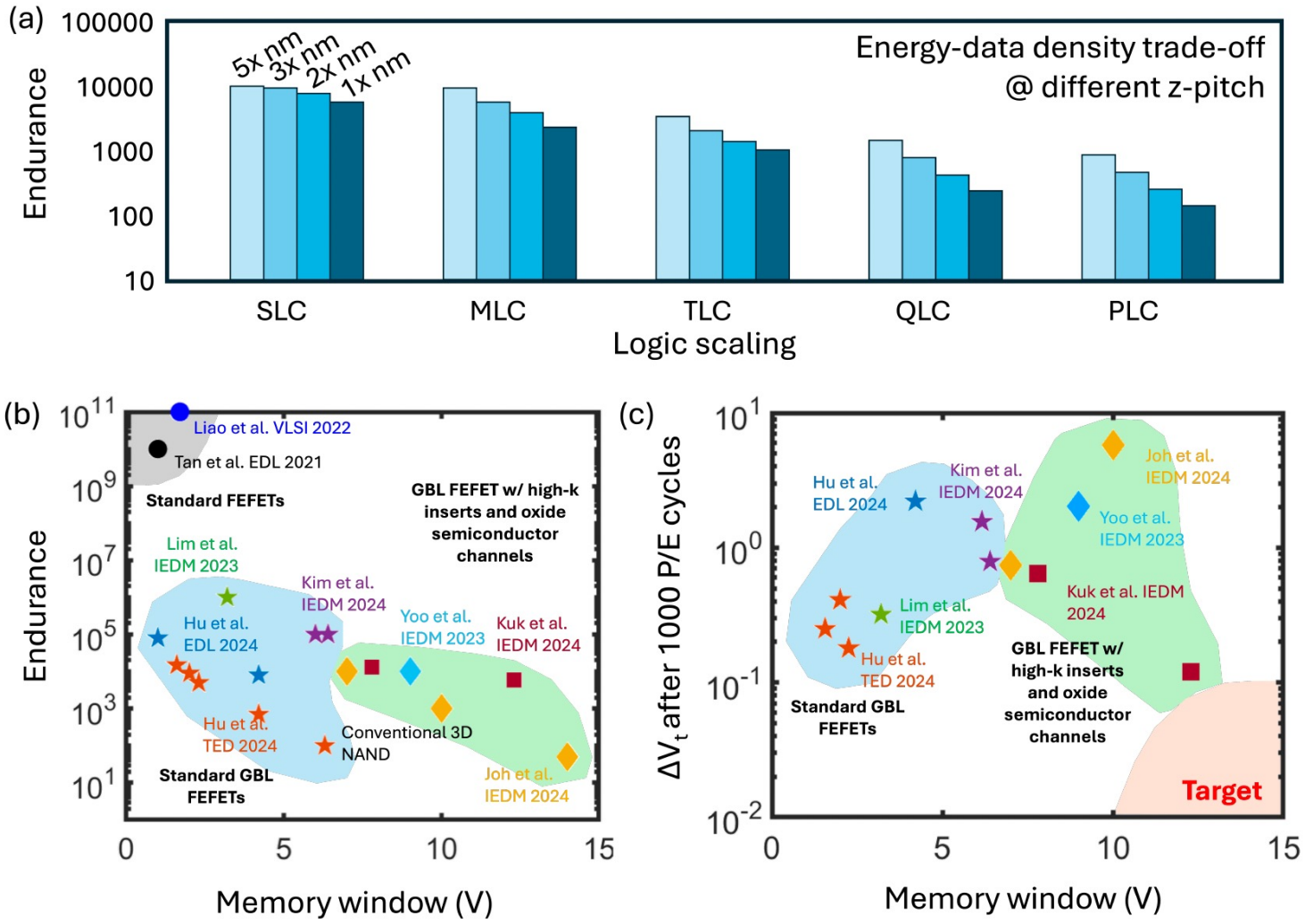


Mitigation scheme reduces pass disturb down to 4%!!

Venkatesan, Khan et al. EDL 2024 (Editor's Pick): [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

Georgia Tech

Write Endurance



Venkatesan, P., et al. IMW 2025

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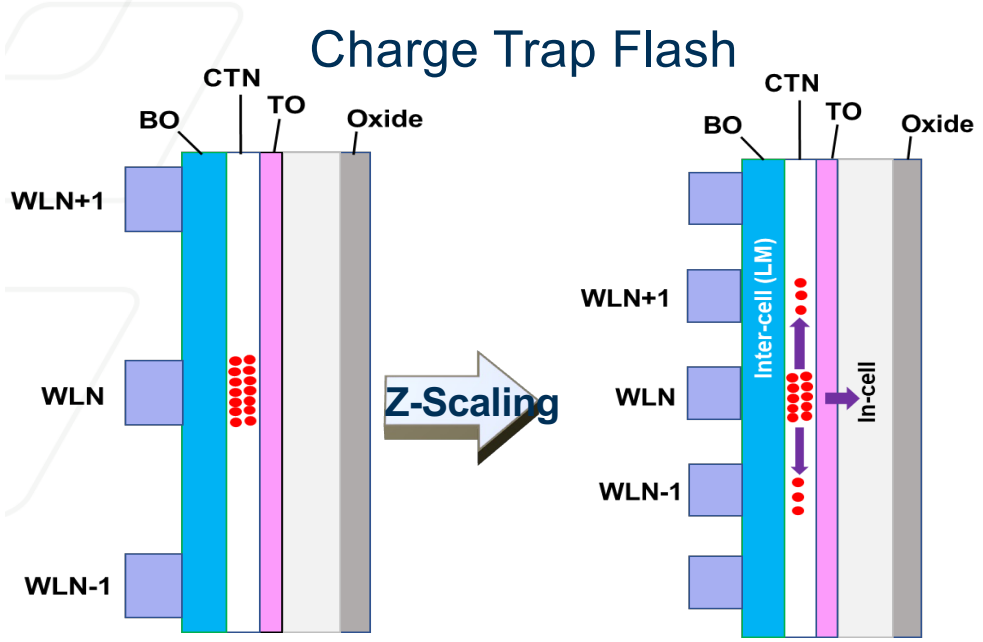
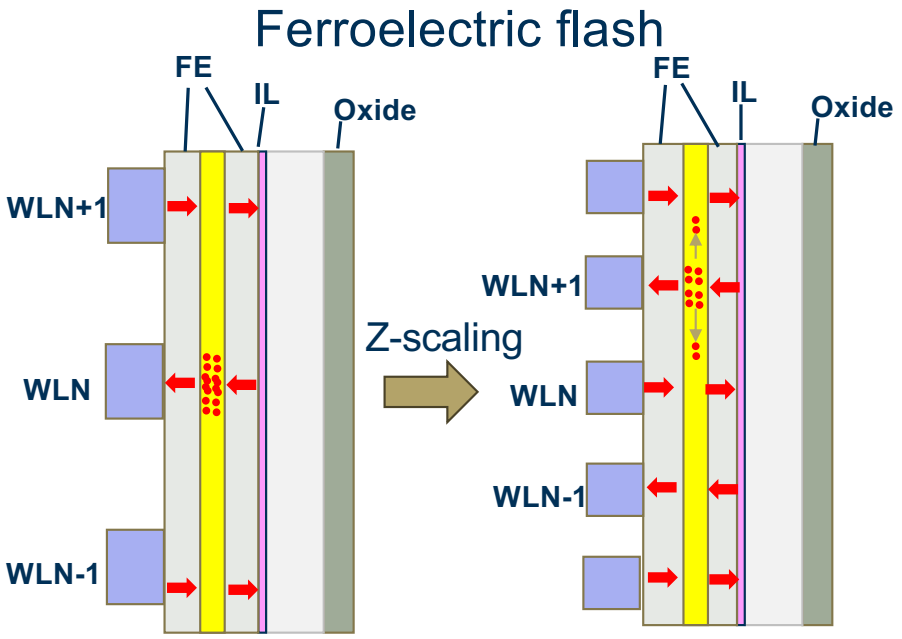
Lateral charge migration



Lateral charge migration prevents aggressive Z-scaling for 3D NAND.



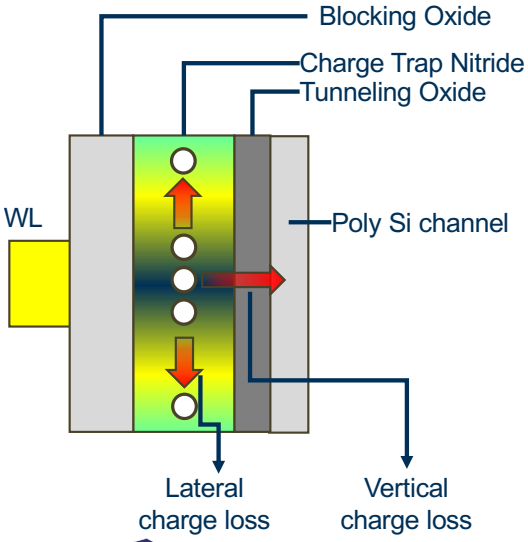
The nature of trapped charges at the ferroelectric—interlayer interface will determine the scaling potential of ferroelectric 3D NAND technology.

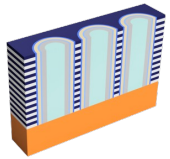
What about reliability of ferroelectric NAND?

❶ Retention	✅ Demonstrated
❷ Disturb	✅ Demonstrated
❸ Write endurance	⚠️ Under Evaluation
❹ Lateral charge migration	⚠️ Under Evaluation
❺ Device-device variation	⚠️ Under Evaluation
⋮	

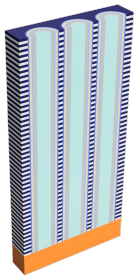
Ferroelectrics for Future NAND Storage Technology

Ferroelectric augmentation can provide enable NAND scaling in future generations

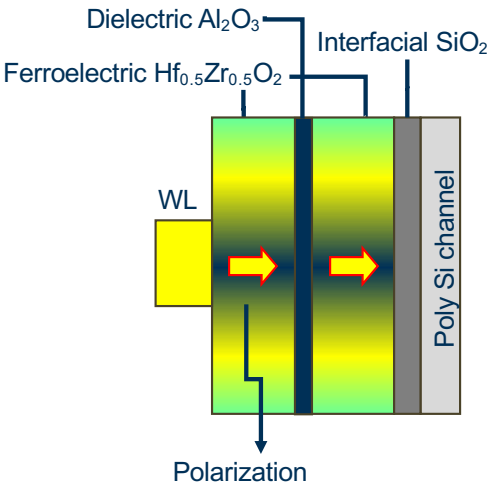


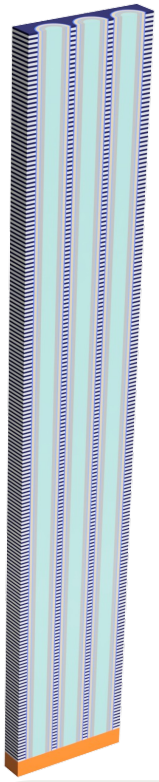


2014:
First 3D NAND
24 Layers, MLC



2025:
300+ Layers, QLC
5 Trillion+ transistors





2030 and
beyond

Georgia Tech

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