Pushing the limits of NAND scaling with *Ferroelectrics*

Asif Khan
Associate Professor and onsemi Junior Professor
School of Electrical and Computer Engineering and of Materials Science and Engineering
Georgia Institute of Technology
akhan40@gatech.edu

Georgia Tech


Georgia Tech
midtown
ATLANTA

Our team


Prasanna Venkatesan


Lance Fernandes


Salma Soliman


Taeyoung Song

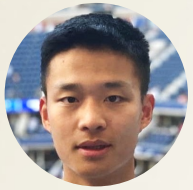

Zekai Wang


Dr. Hang Chen


Yu Hsin Kuo

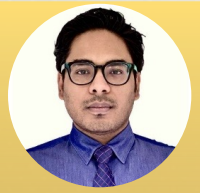

Nashrah Afroze


Priyankka Ravikumar


Jiayi Chen


Dr. Mengkun Tian


Dr. Chinsung Park (SK Hynix)


Dr. Dipjyoti Das (NIT Silchar)


Dr. Zheng Wang (Micron)


Dr. Sarah Lombardo (TEL)


Dr. Nujhat Tasneem (Intel)


Anthony Gaskell (Micron)

Collaborators:
Prof. Andrea Padovani, DIEF, UNIMORE
Dr. Gaurav Thareja, Dr. Luca Larcher, Applied Materials
Prof. Lauren Garten, Prof. Shimeng Yu, Prof. Suman Datta, Georgia Tech

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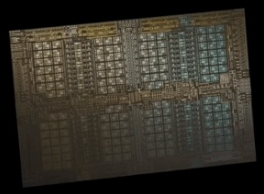
Memory technologies – The state of the art

Memory

Hyperscale AI and High-performance Computing



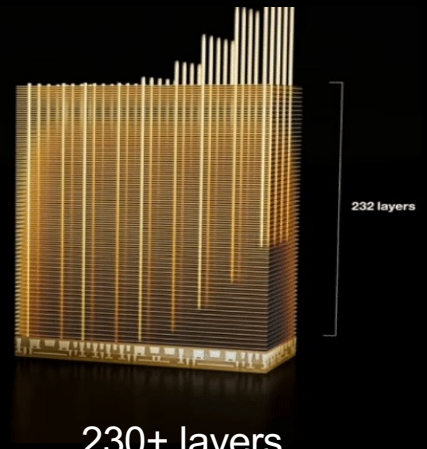
HBM3E: 12-high, 32 GB

1.18 TB/s

Source: NVIDIA

Storage

Client, Mobile, Enterprise



230+ layers

2.4 GB/s

Source: Micron

Embedded

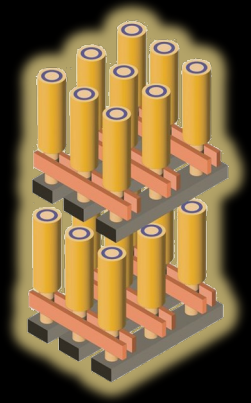
Automotive

14nm eMRAM

16 MB

Source: Forbes

Emerging Memory



Ferroelectric NV-DRAM

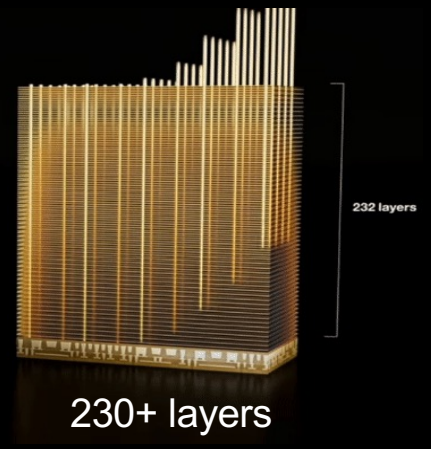
32 Gb, 3D-stacked, multi-layer

Source: IEDM 2023

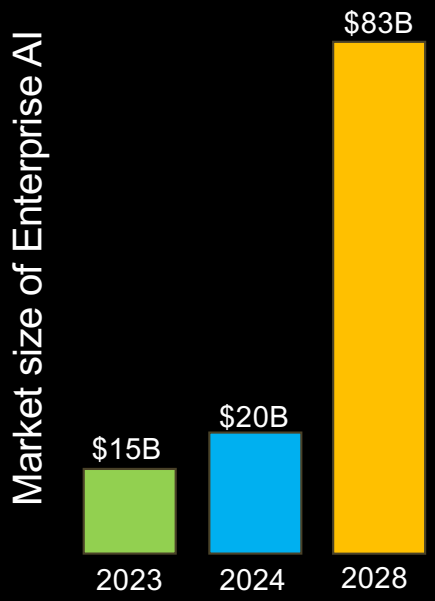
The NAND Storage Technology

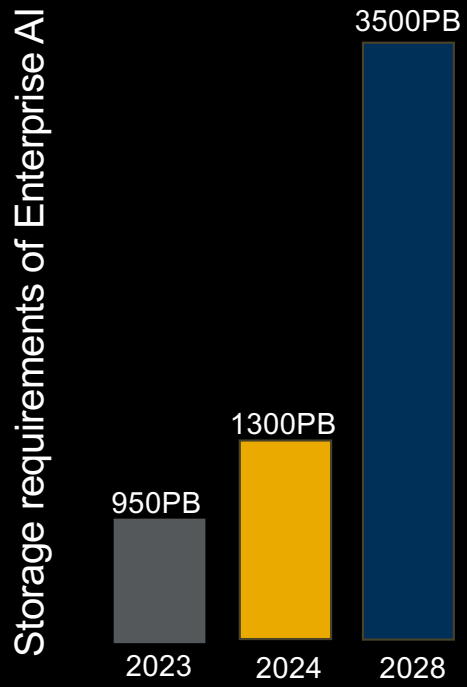
Storage

Client, Mobile, Enterprise



Source: Micron

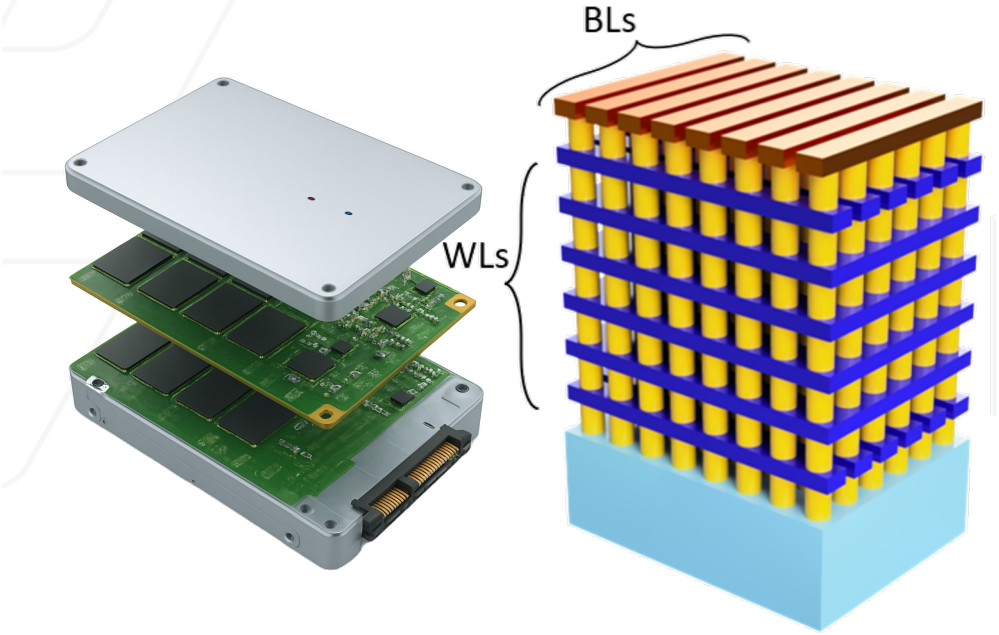


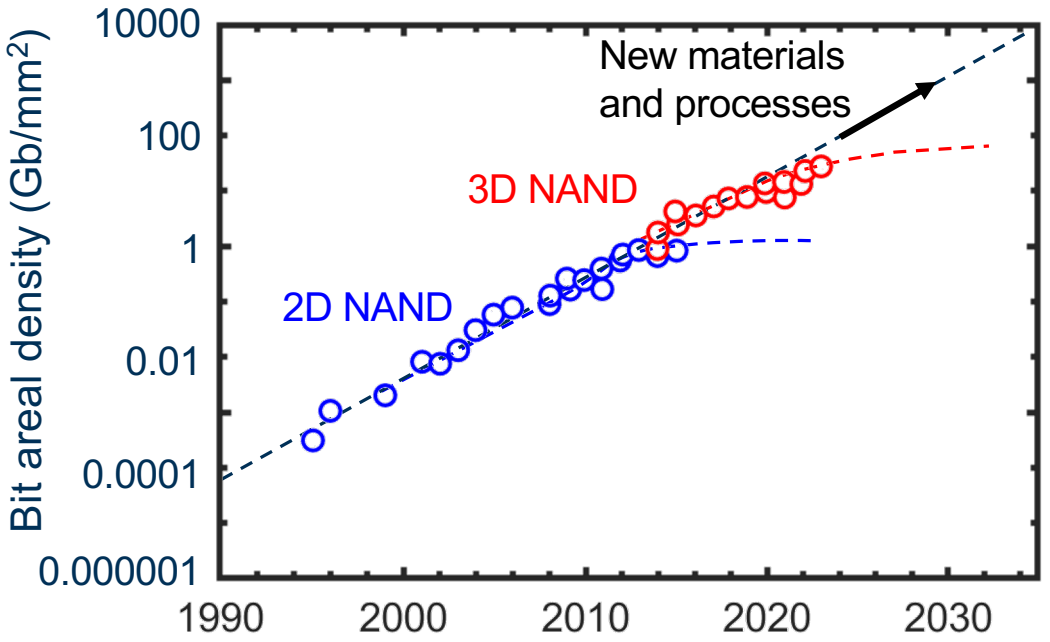


Source: The Business Research Company

Processing and storing data in AI effectively and cost efficiently can require HBM for the actual AI training, but also various types of NAND-based solid-state storage to support the data flows needed to and from the HBM.

Vertical NAND Scaling

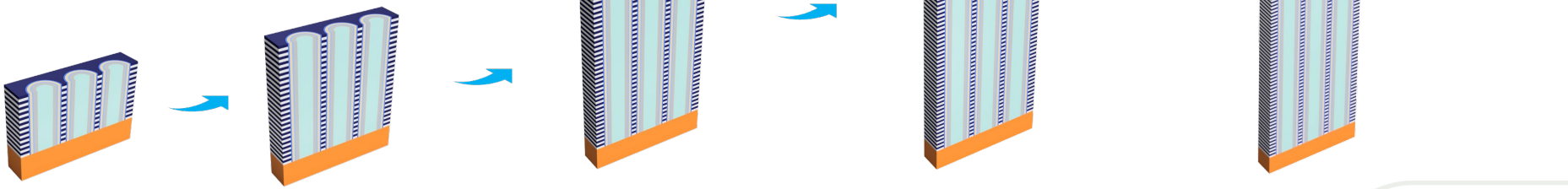




A. Goda, IEDM 2024

Relentless innovations have led to a 50x improvement in bit arial density per decade.

Vertical NAND Scaling



2014:
First 3D NAND
24 Layers, MLC

2019:
128 Layers,
TLC

2025:
300+ Layers, QLC
5 Trillion+ transistors

2030:
1000+ Layers,
QLC, PLC

2040 and
beyond

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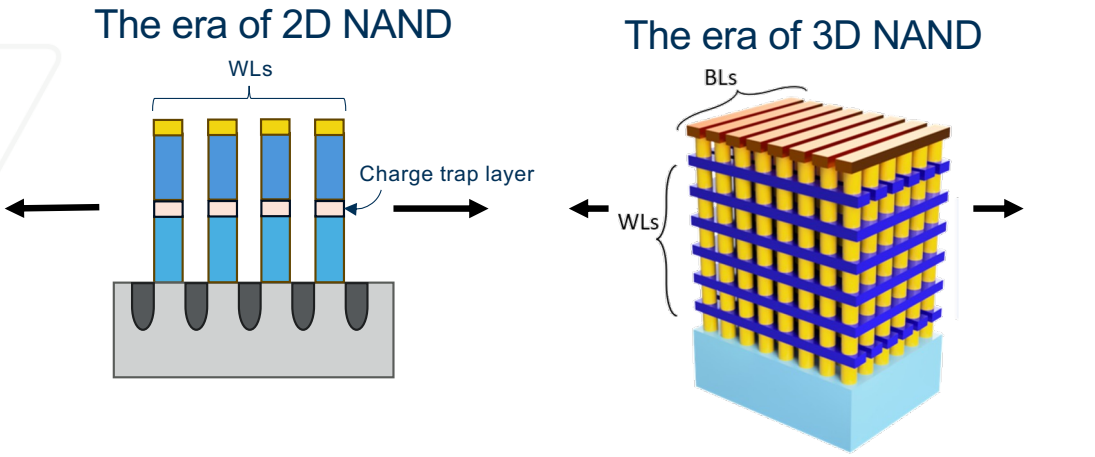
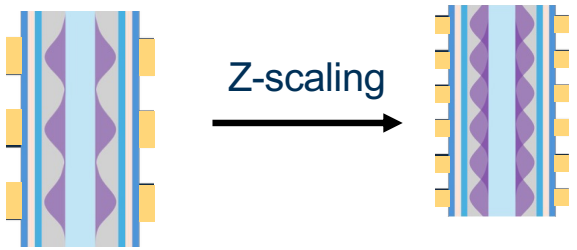
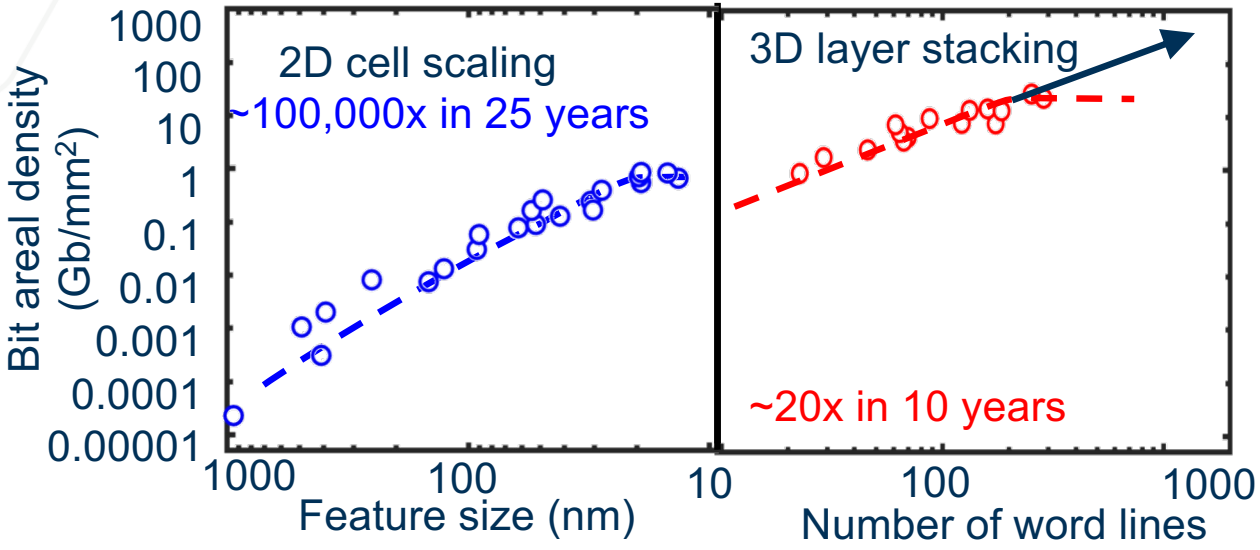
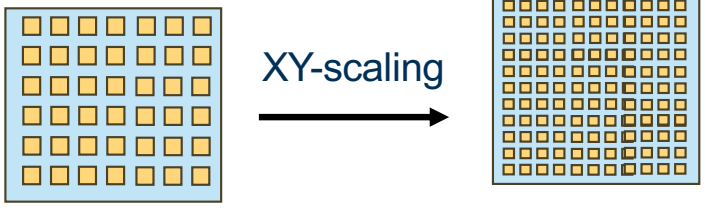
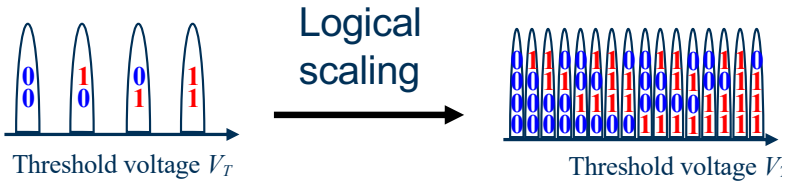
Vertical NAND Scaling



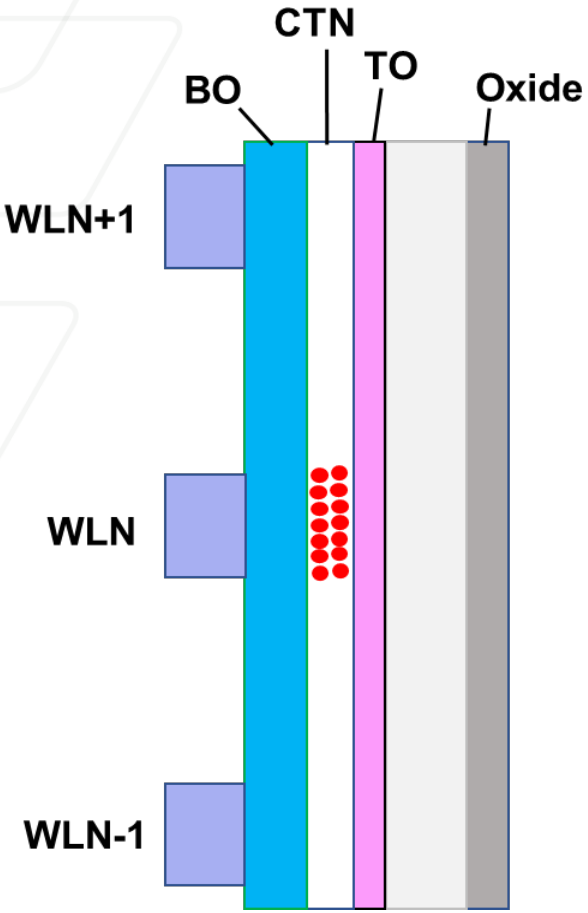






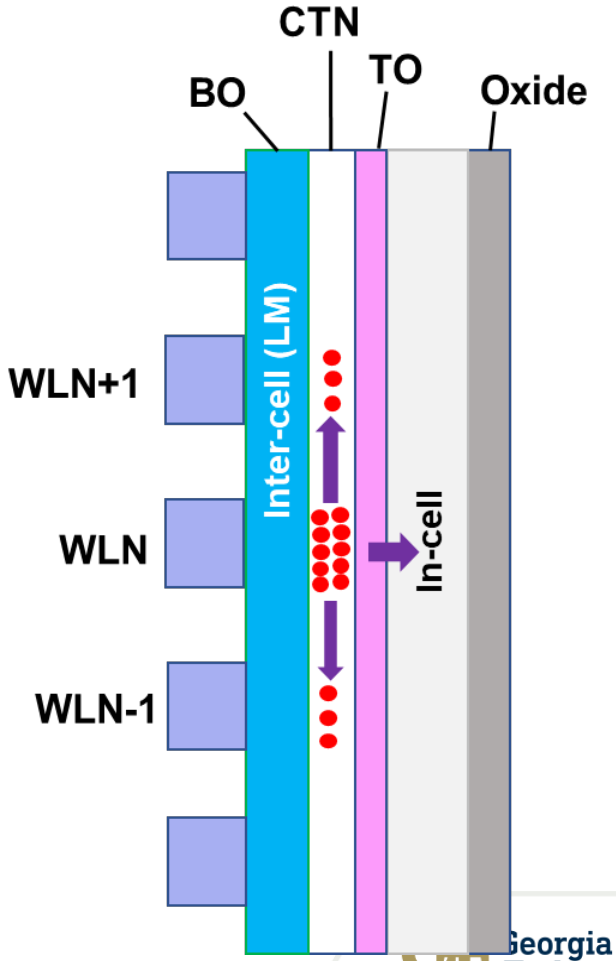


Challenges of vertical NAND flash scaling



Z-scaling

1. Lateral charge migration
2. Inter-WL reliability
3. High write voltage
4. Endurance
5. Device-device variation



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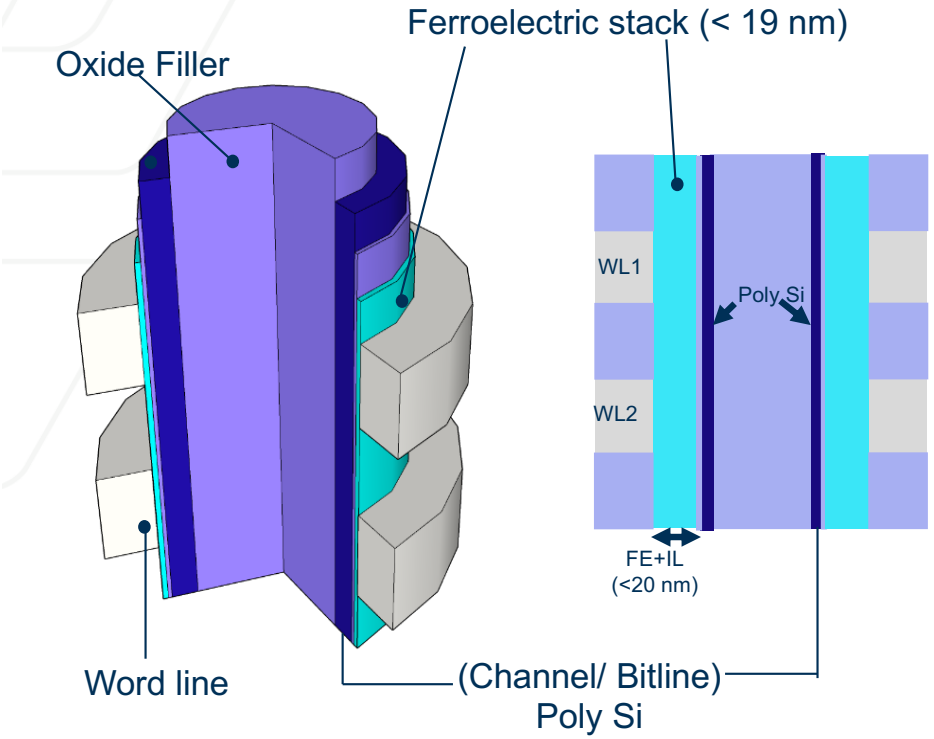
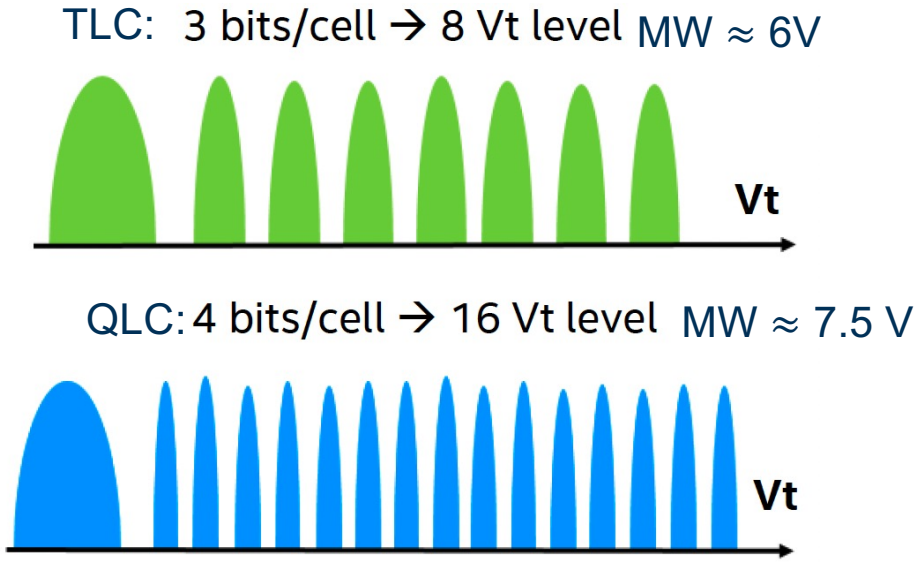
Rethinking NAND flash technology



To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm



Design constraints

Ferroelectric thickness, $t_{FE} \leq 19$ nm

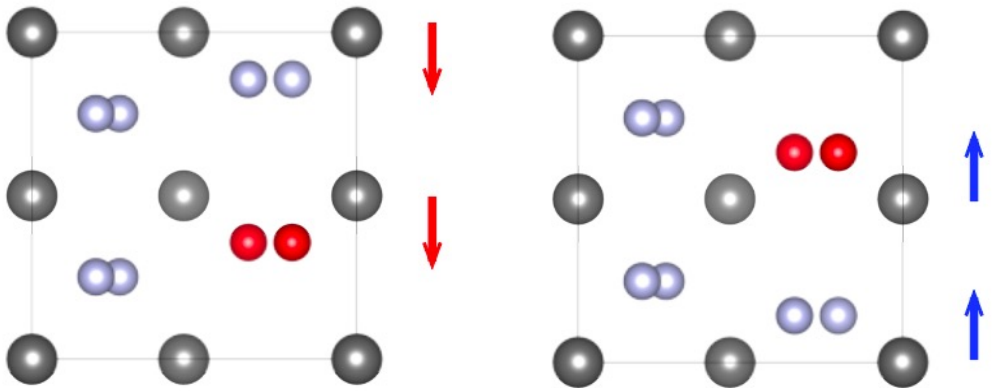
Write voltage ≤ 15 V

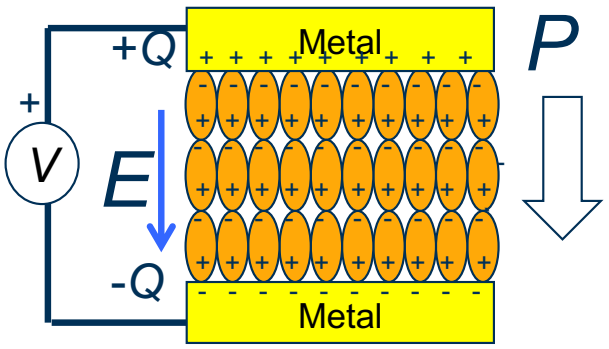
Memory window, MW ≥ 6.5 V

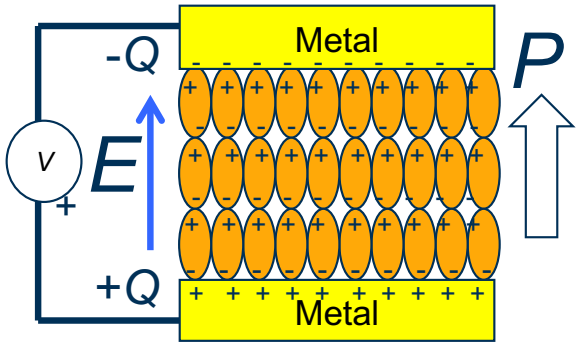
Ferroelectricity

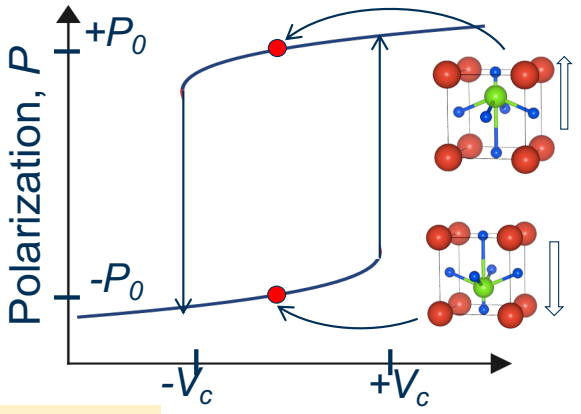
CMOS compatible HfO_2-based fluorite-structure ferroelectric

Orthorhombic *Pca2₁* structure



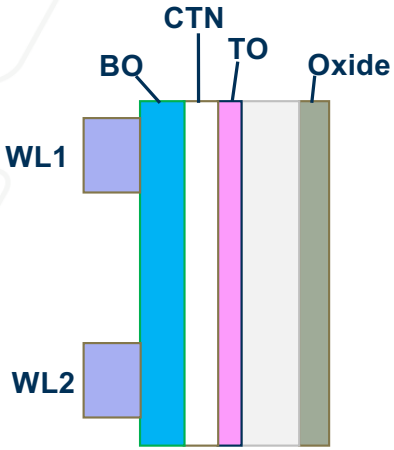


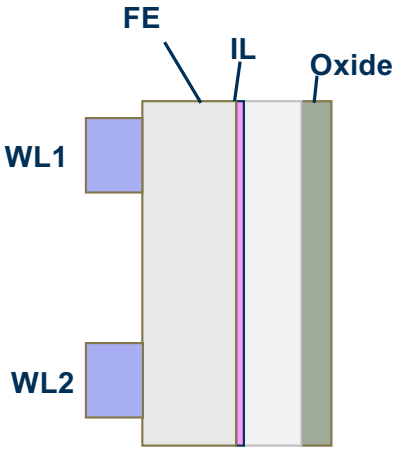




A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

Charge trap flash vs. ferroelectric flash





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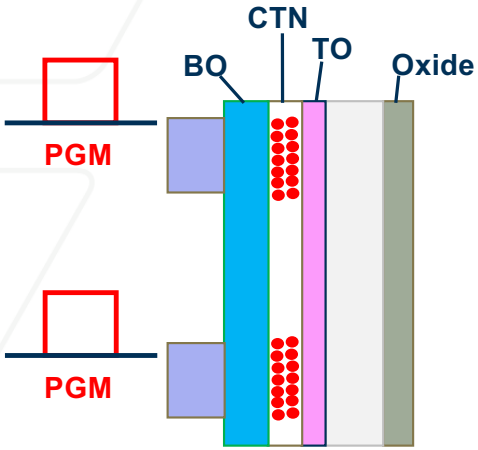
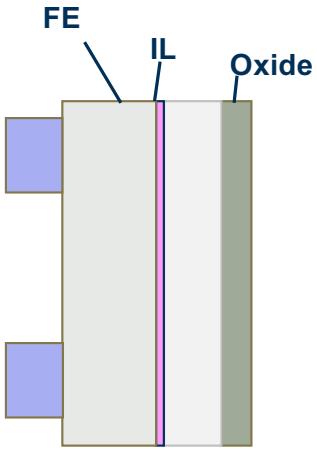
Charge trap flash vs. ferroelectric flash





CTF that stores data in the form of charge

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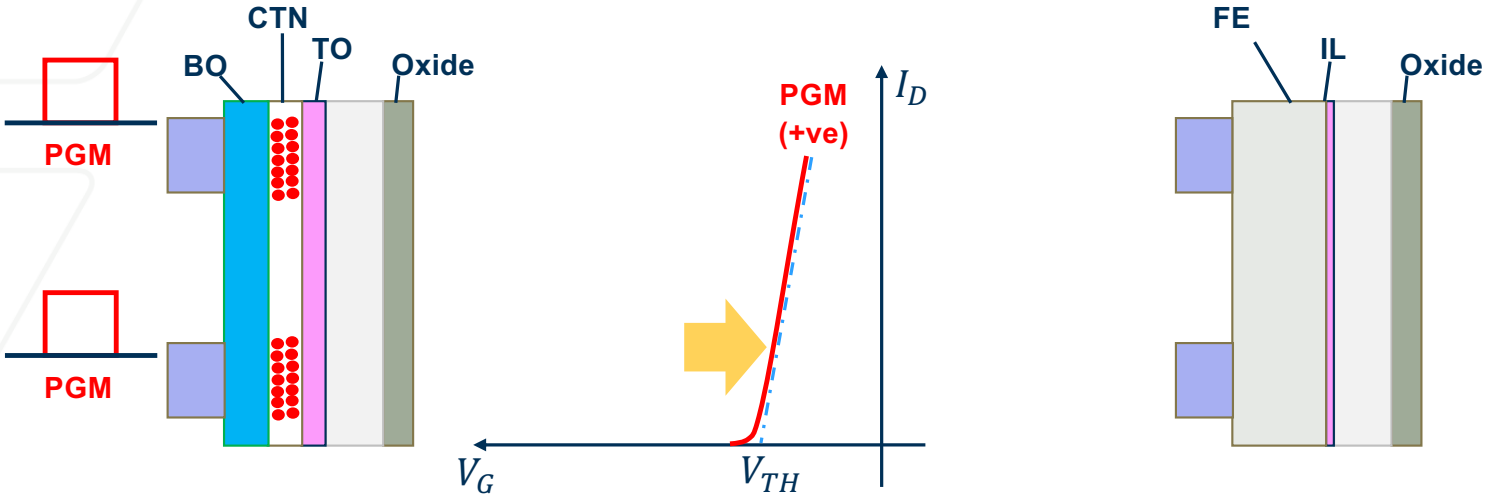
Charge trap flash vs. ferroelectric flash



Positive PGM pulse sets the Vt to high Vt state in CTF

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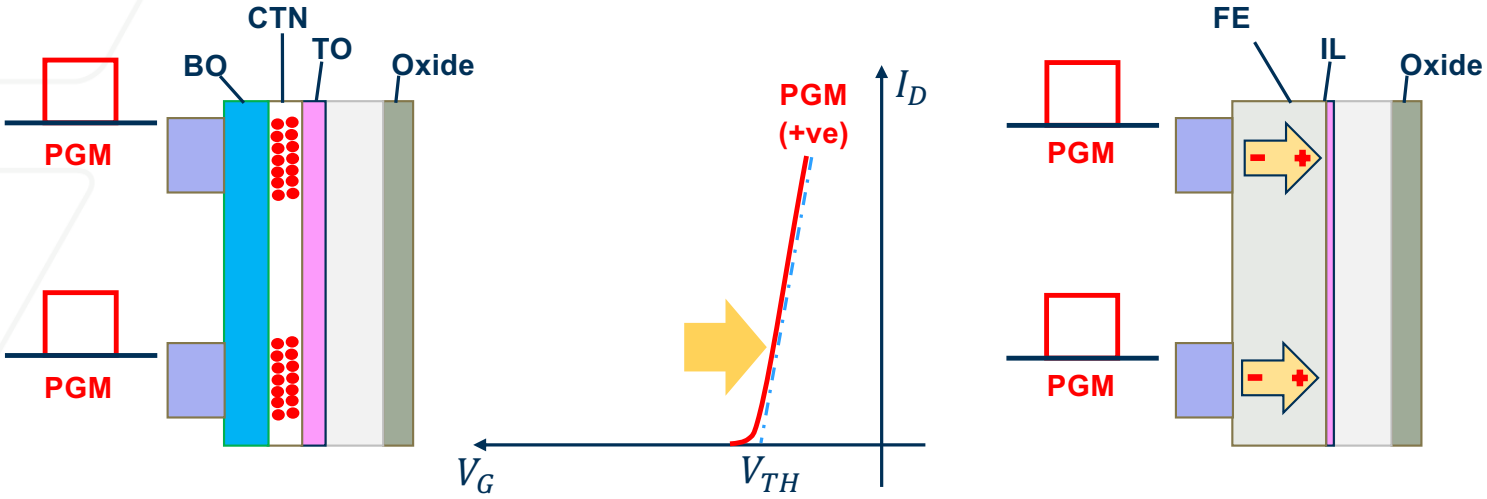
Charge trap flash vs. ferroelectric flash



Positive PGM pulse sets the Vt to high Vt state in CTF

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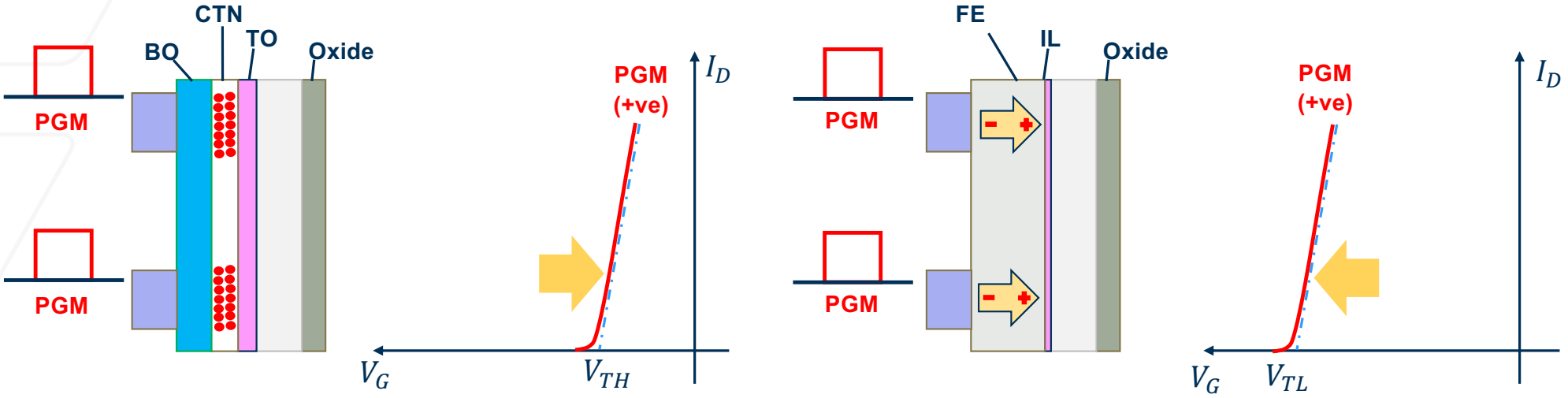
Charge trap flash vs. ferroelectric flash



On the contrary, Positive PGM pulse sets the Vt to low Vt state in FEFET

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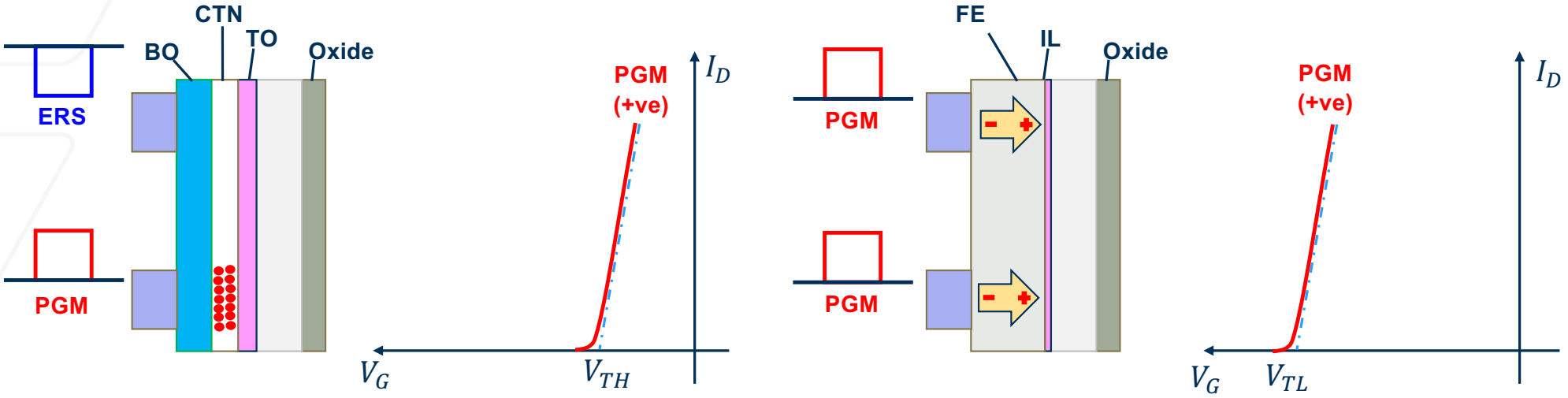
Charge trap flash vs. ferroelectric flash



Negative ERS pulse sets the Vt to low Vt state in CTF

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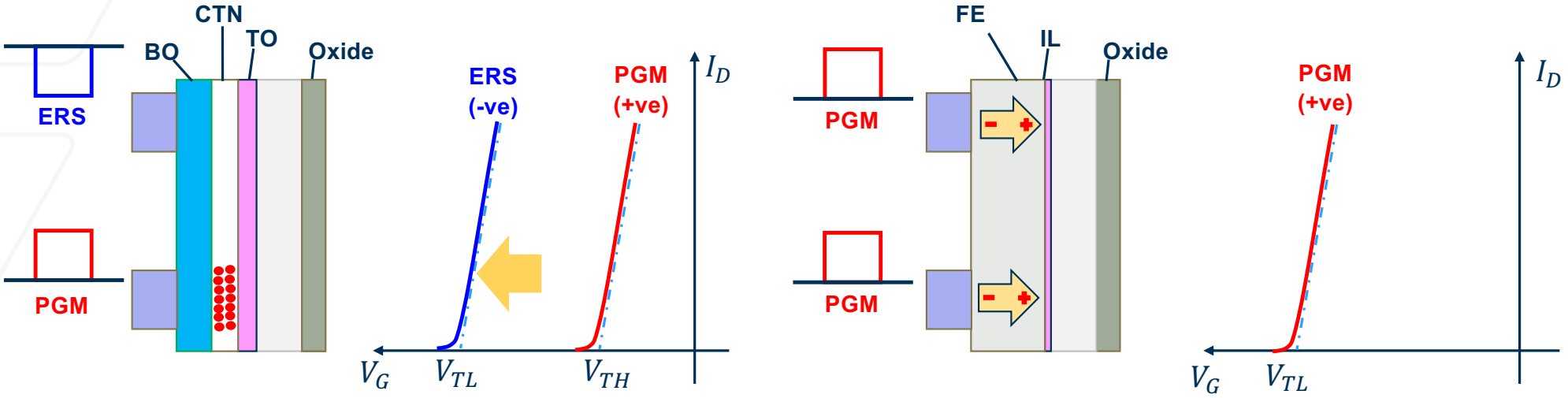
Charge trap flash vs. ferroelectric flash



Negative ERS pulse sets the Vt to low Vt state in CTF

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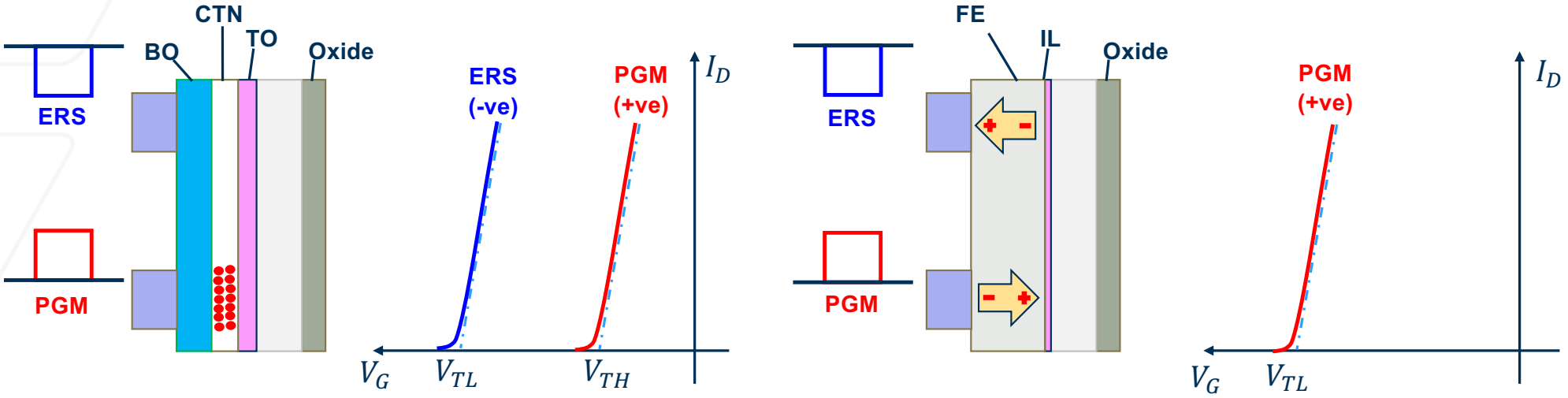
Charge trap flash vs. ferroelectric flash



Negative ERS pulse sets the Vt to high Vt state in FEFET

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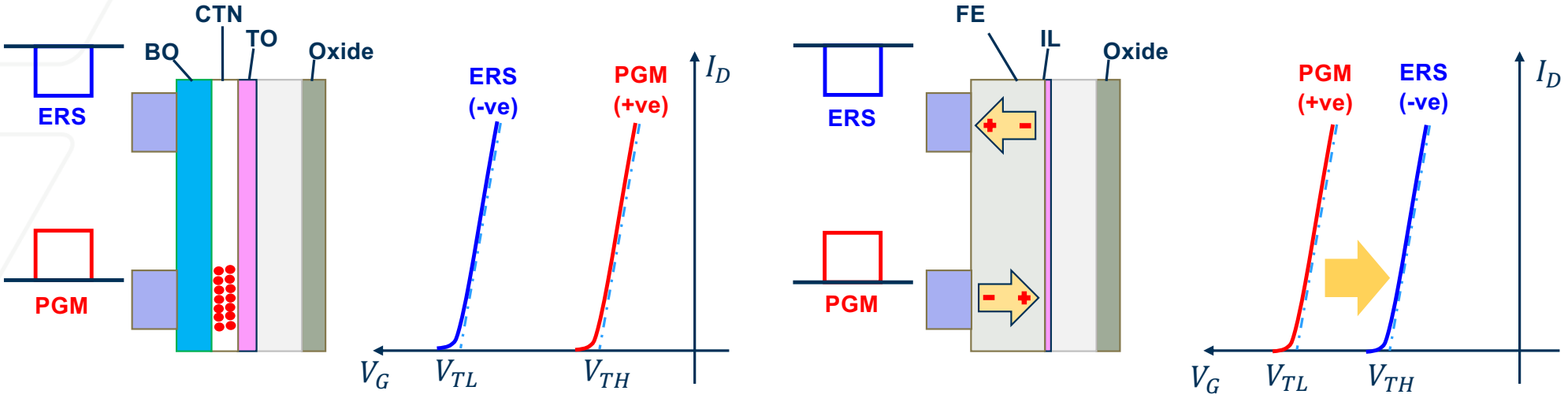
Charge trap flash vs. ferroelectric flash



Negative ERS pulse sets the Vt to high Vt state in FEFET

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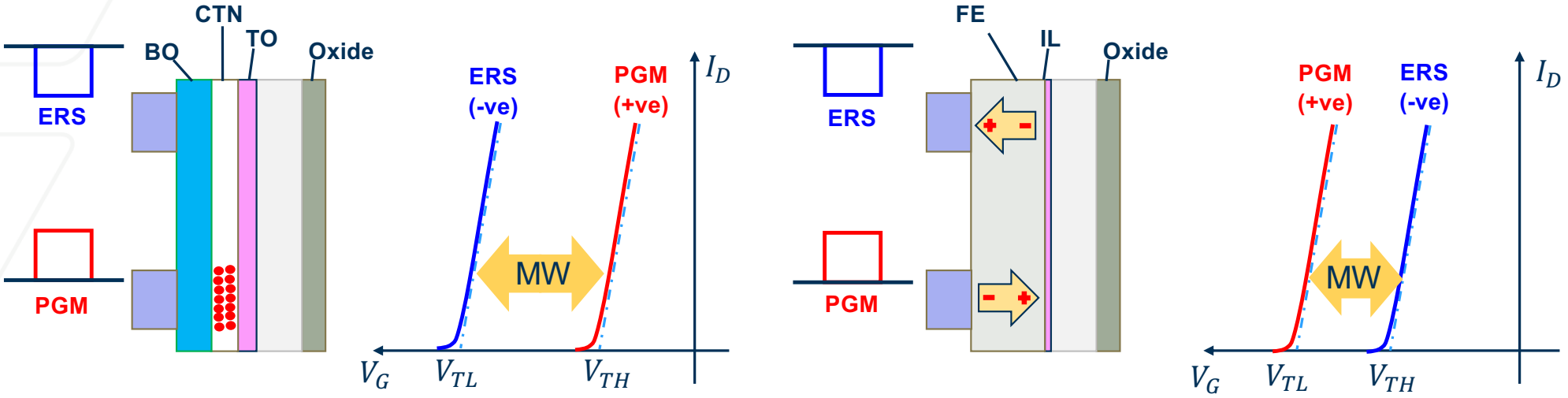
Charge trap flash vs. ferroelectric flash



$$MW = V_{TH} - V_{TL}$$

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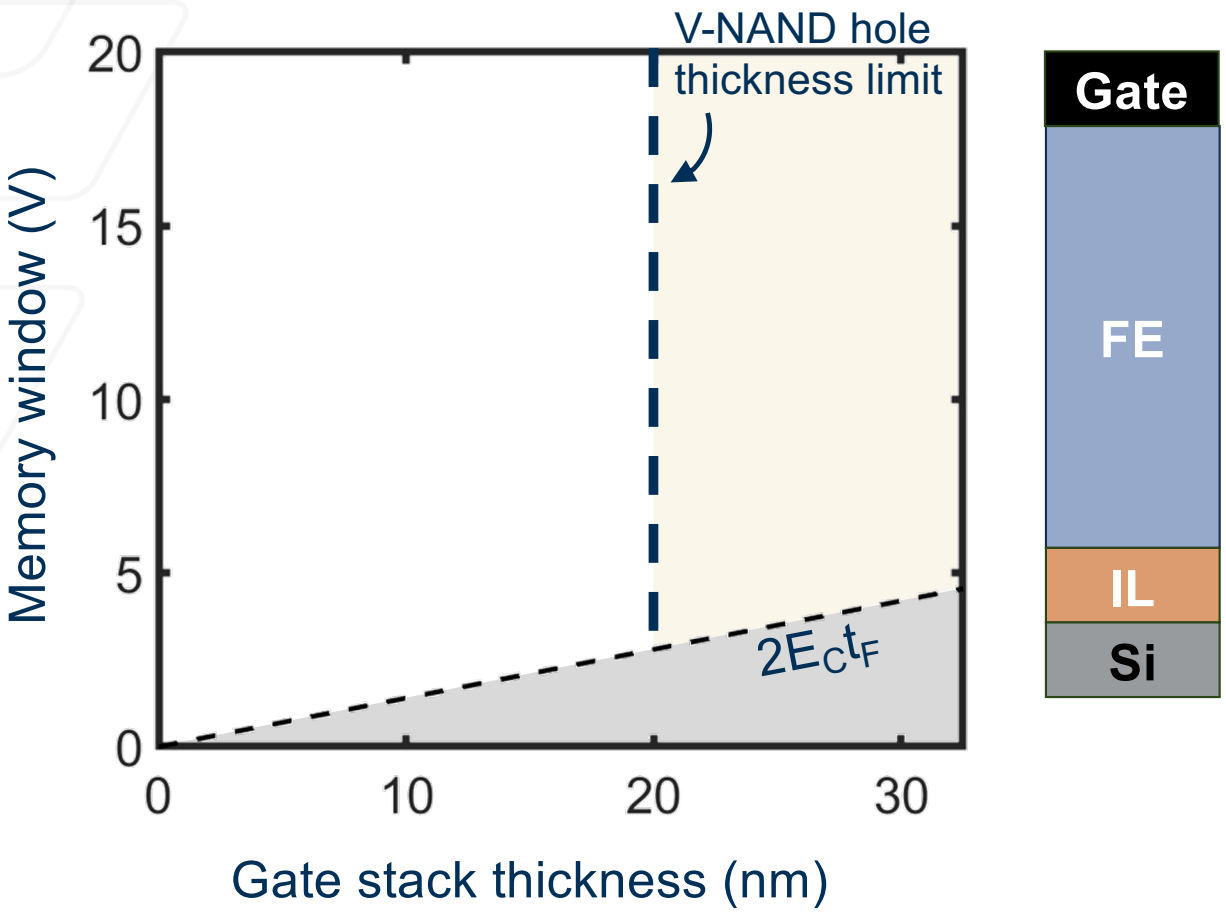
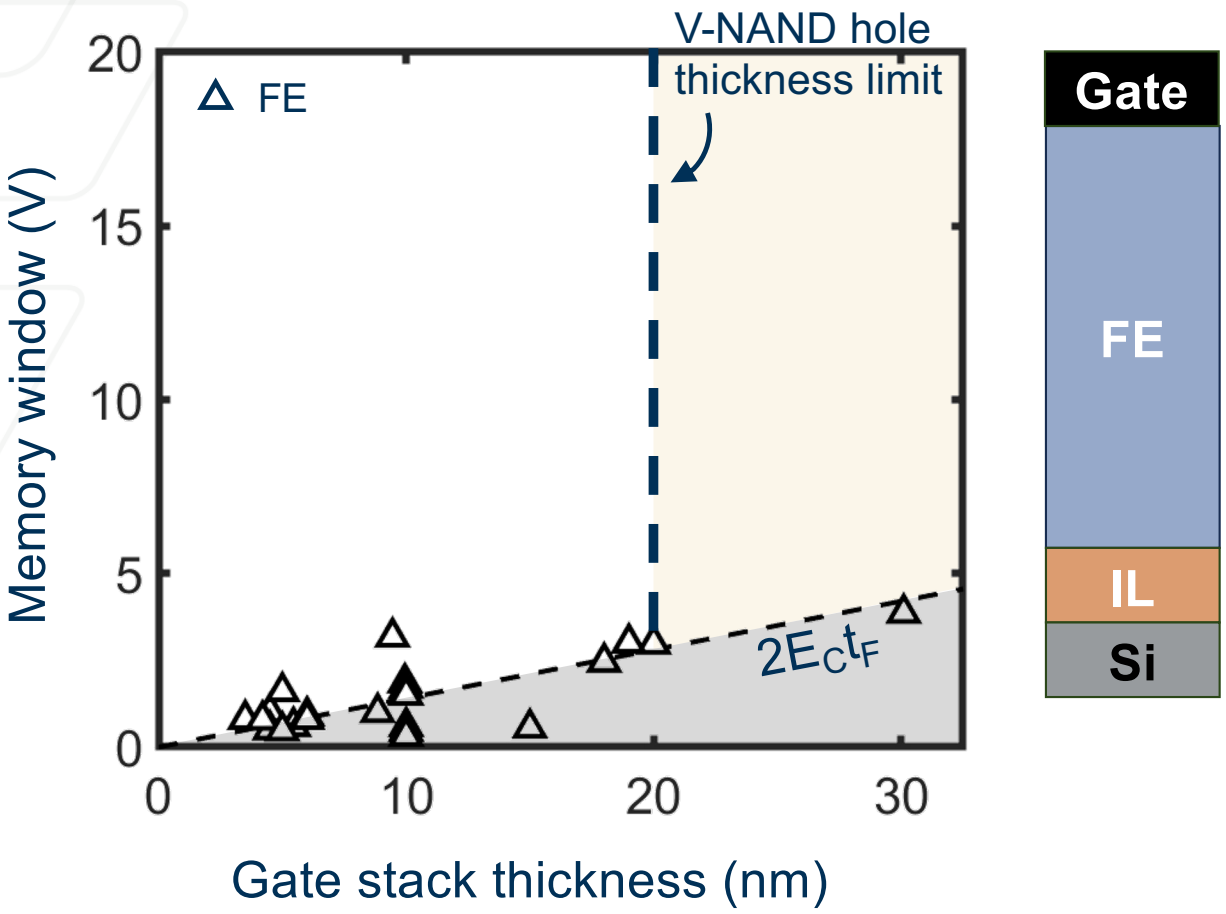
Memory window of FEFETs is limited by V_C

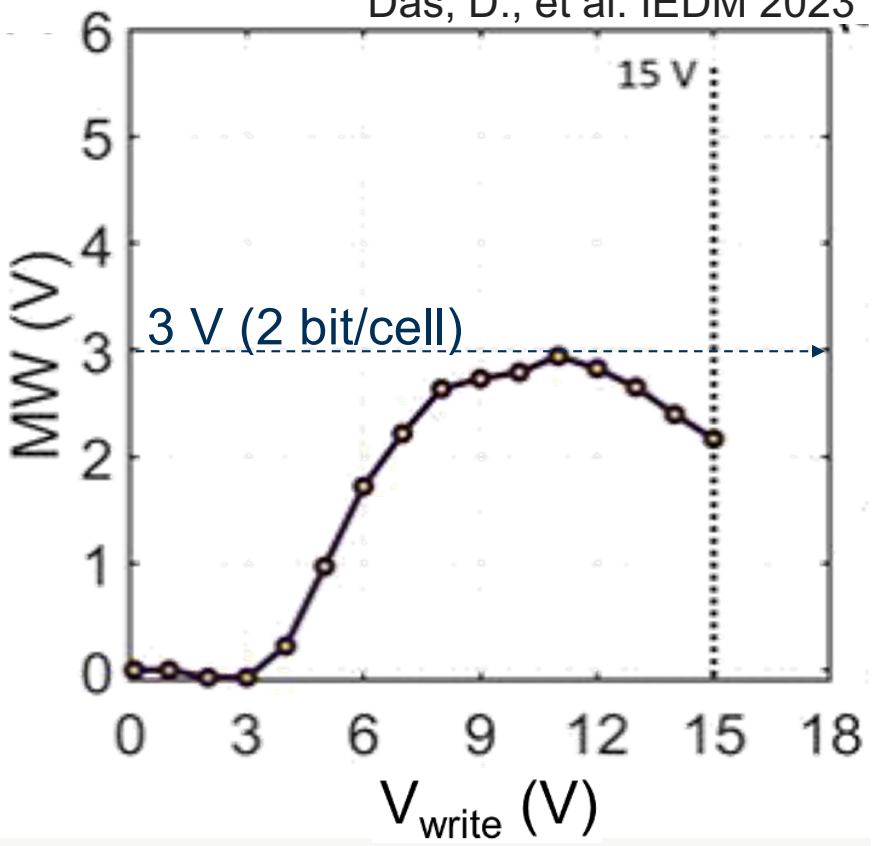


Memory window of FEFETs is limited by V_C



Increasing the MW by dielectric insertion

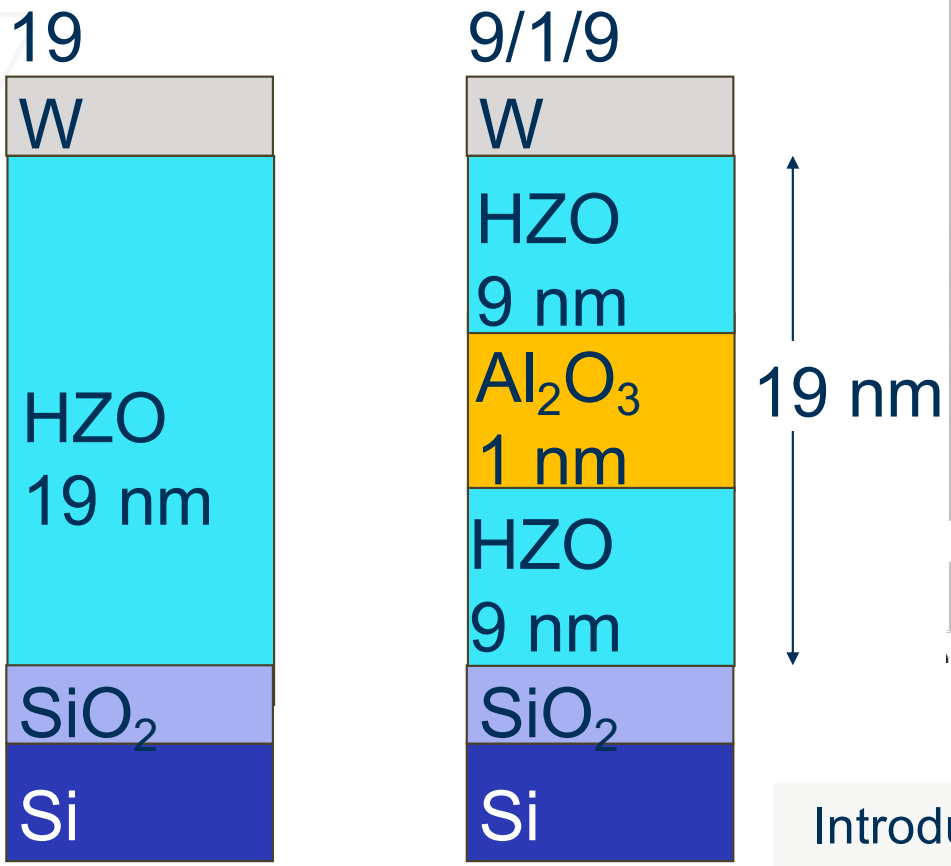
Das, D., et al. IEDM 2023

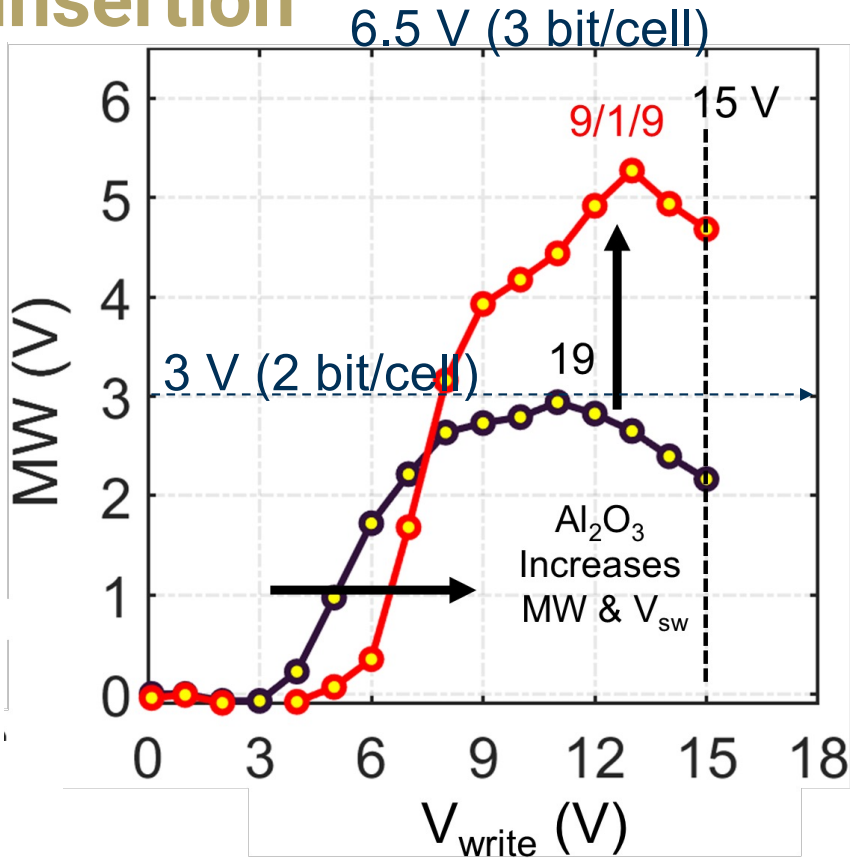


10 nm HZO layer leads to maximum memory window of 2.9 V.

Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion

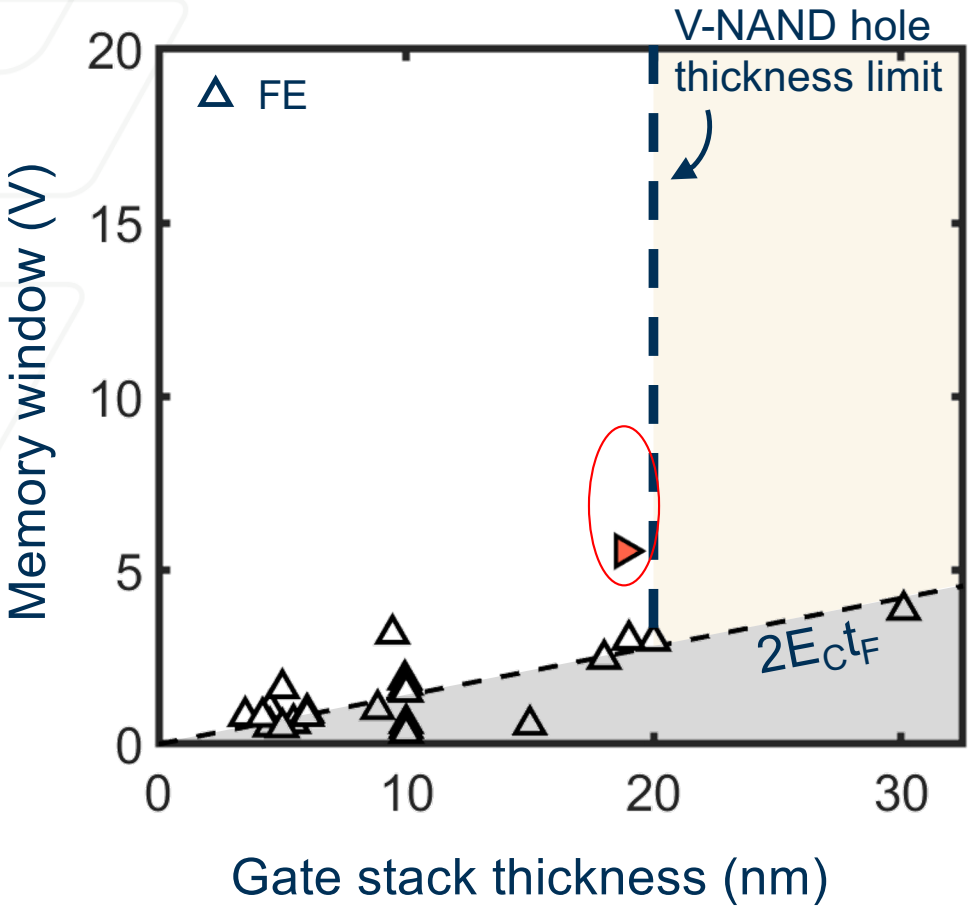


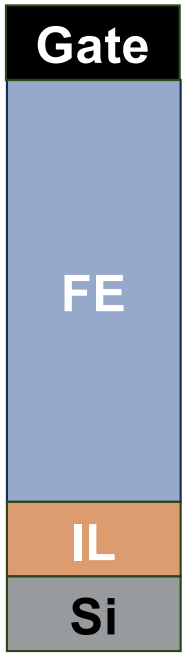


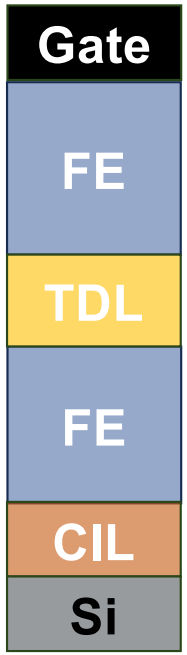
Introducing 1 nm Al_2O_3 intermediate layer dramatically memory window to 5.3 V.

Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

Memory window of FEFETs is limited by V_C

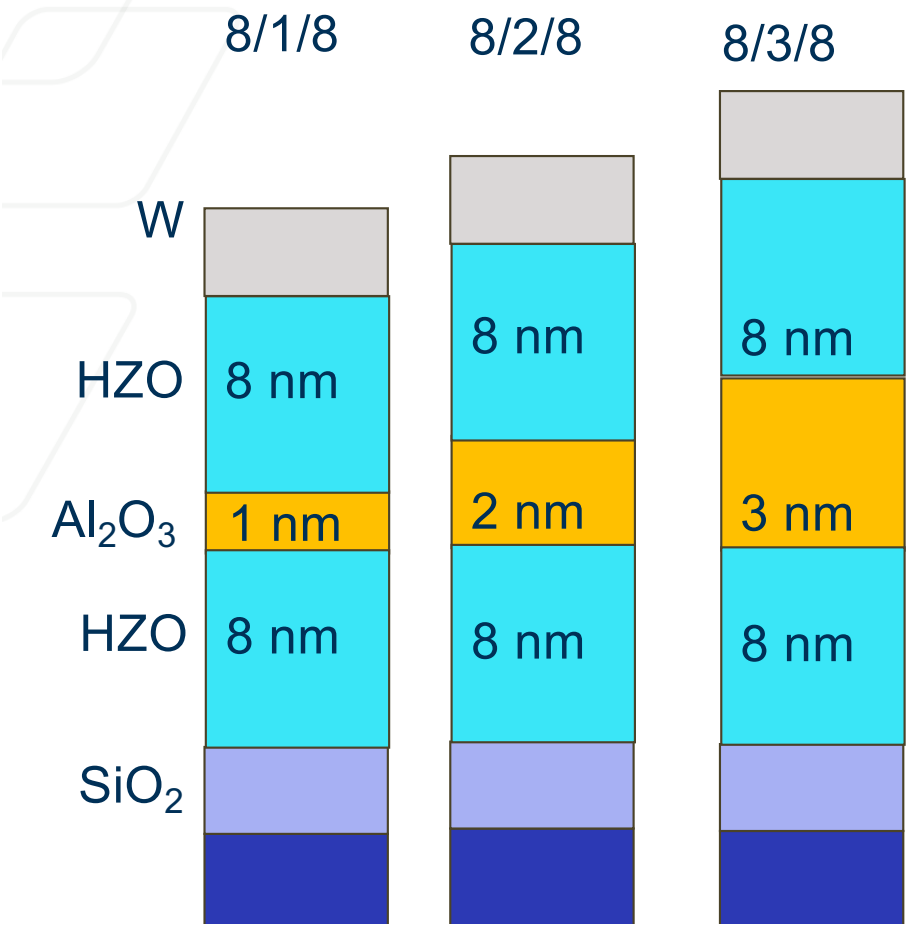


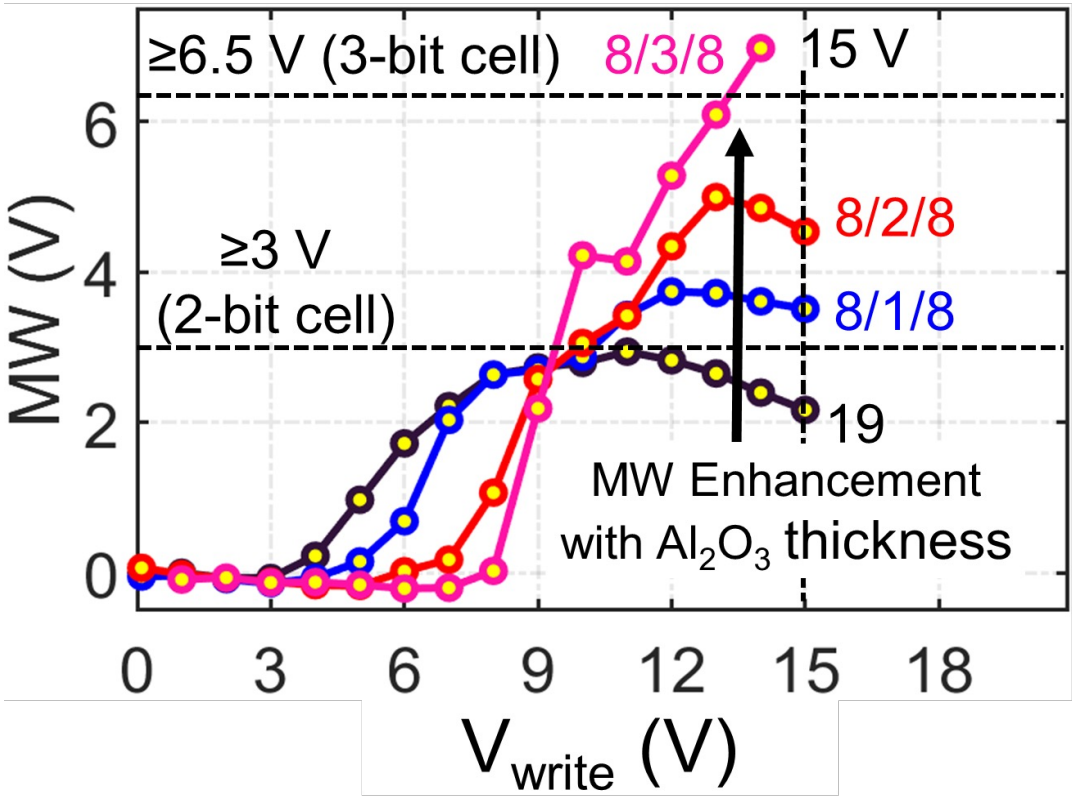




Increasing the MW by dielectric insertion

Das, D., et al. IEDM 2023



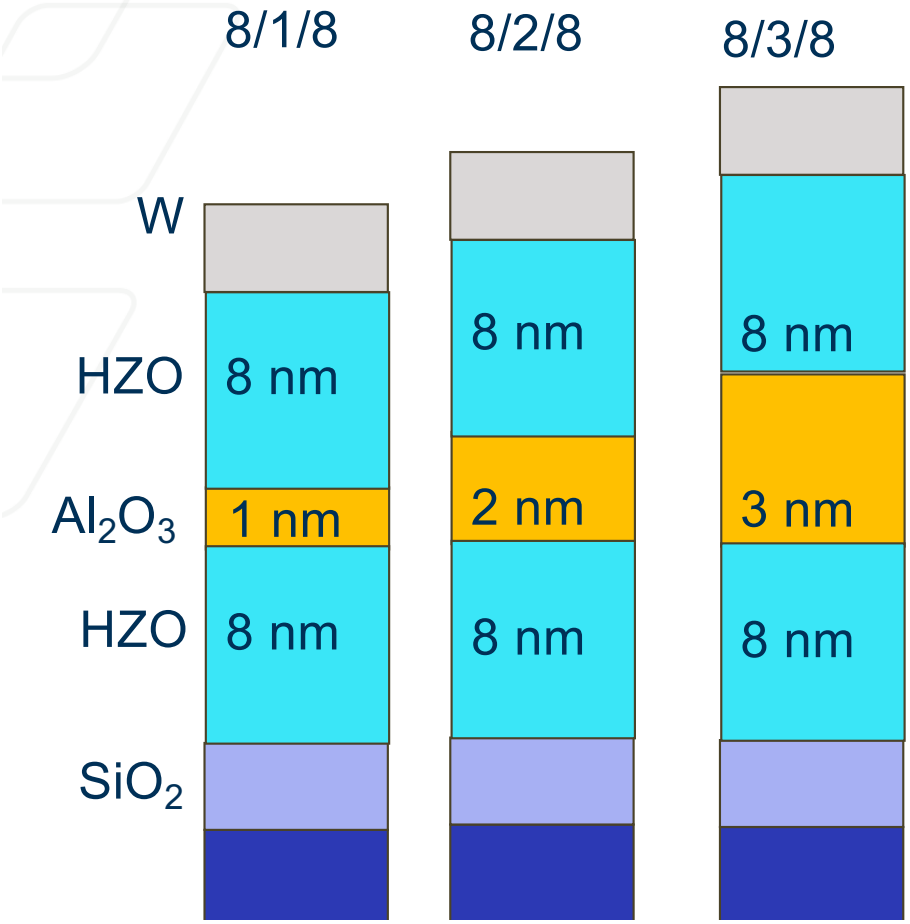


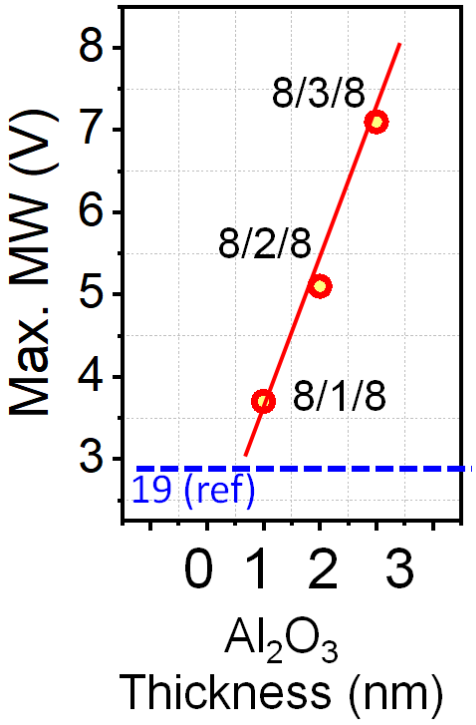
FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

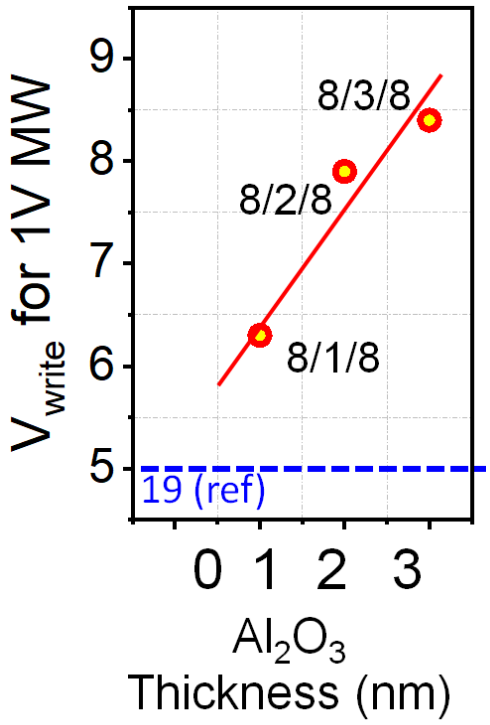
Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion

Das, D., et al. IEDM 2023



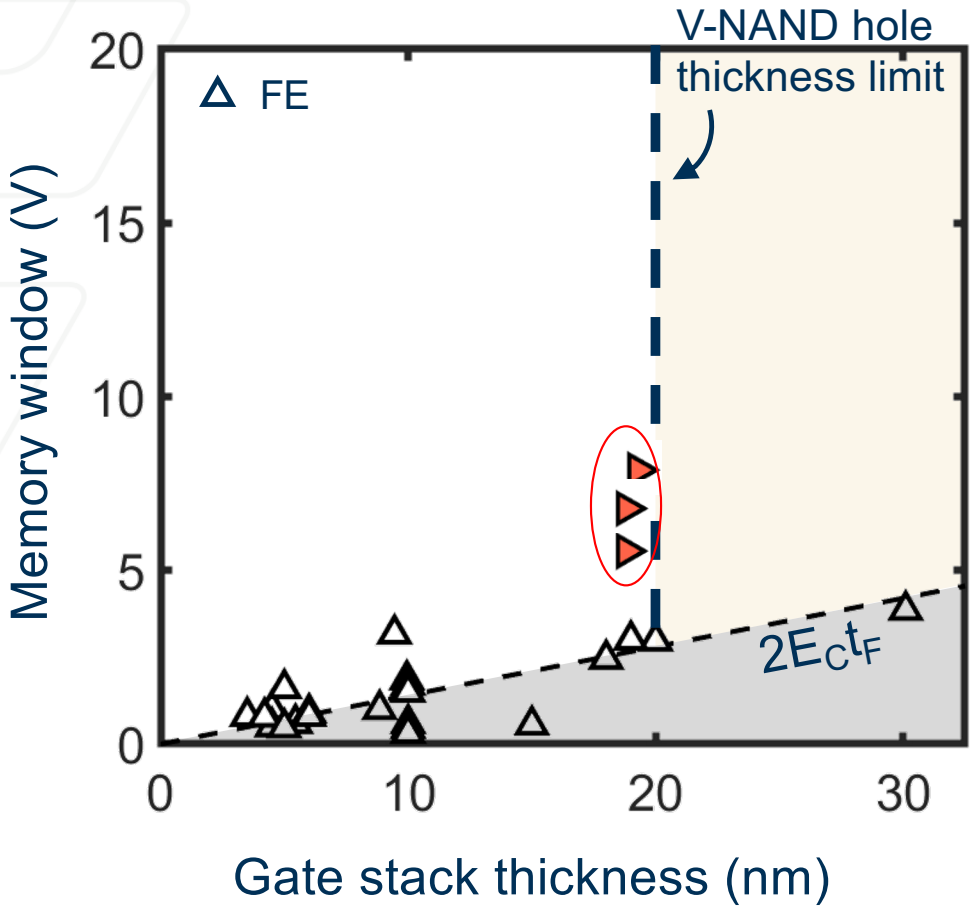


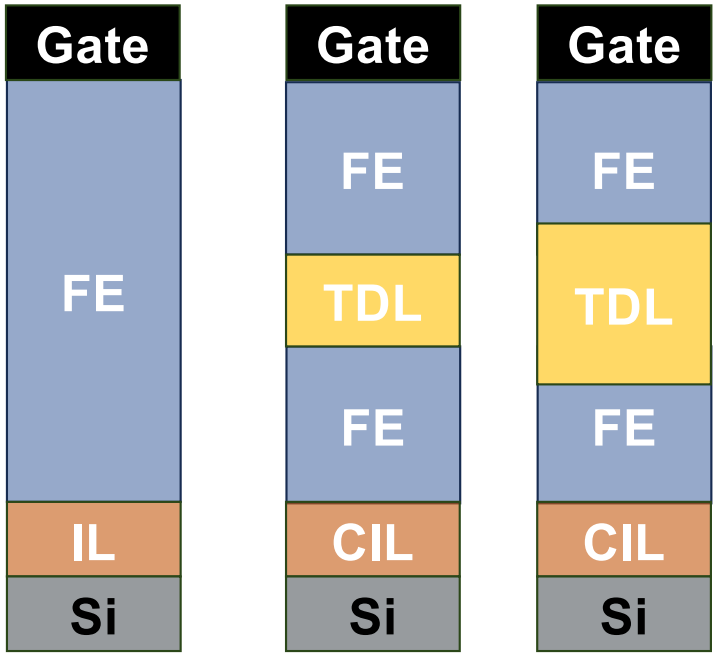


For a fixed FE layer, increase AlO layer increases the MW while increasing the write voltage <15 V.

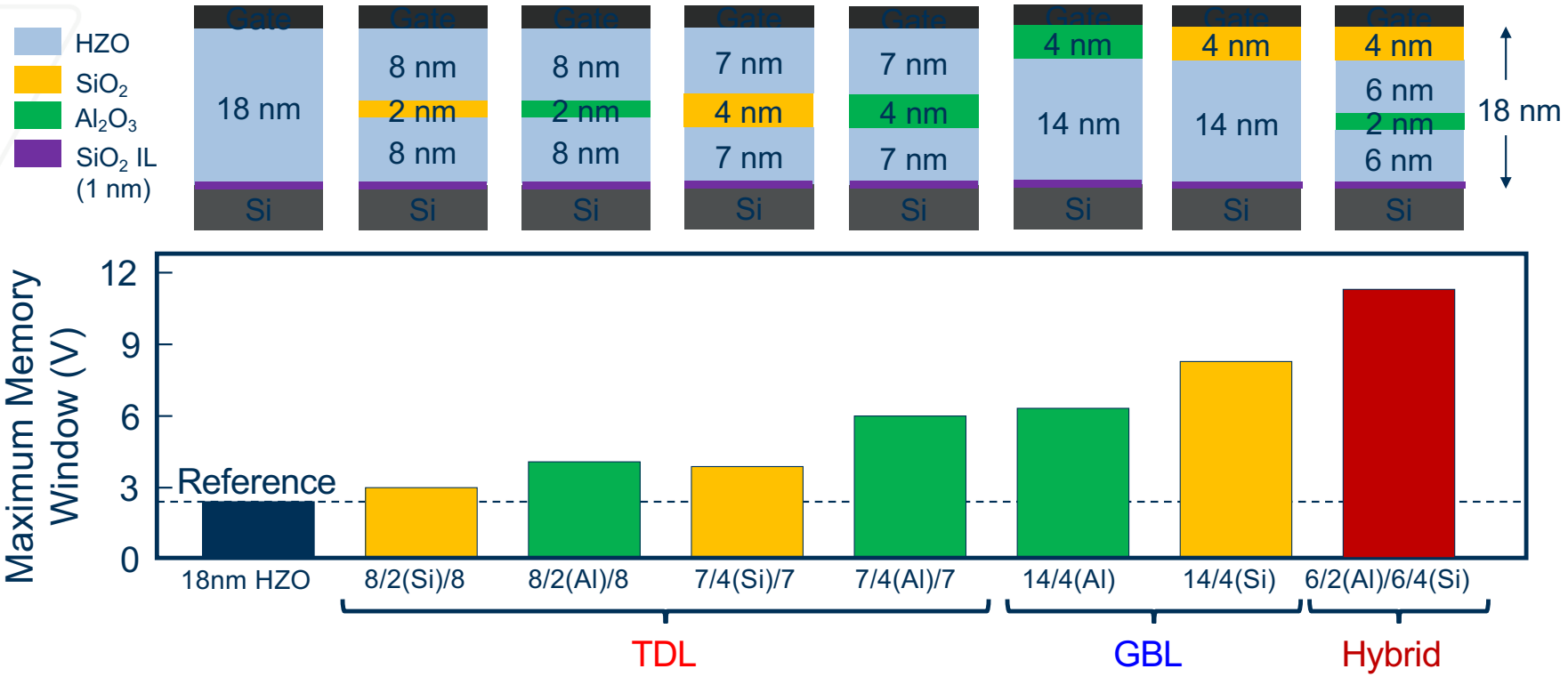
Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

Increasing the MW by dielectric insertion





Position and choice of the dielectric



- GBL stacks have higher MW than TDL stacks for similar thickness and material.
- SiO_2 in GBL and Al_2O_3 in TDL gives higher MW for similar dielectric thickness

Fernandes, L., Ravindran, P. V., Song, T., Das, D., Park, C., Afroze, N., ... & Khan, A. (2024). Material choices for tunnel dielectric layer and gate blocking layer for ferroelectric NAND applications. *IEEE Electron Device Letters*.

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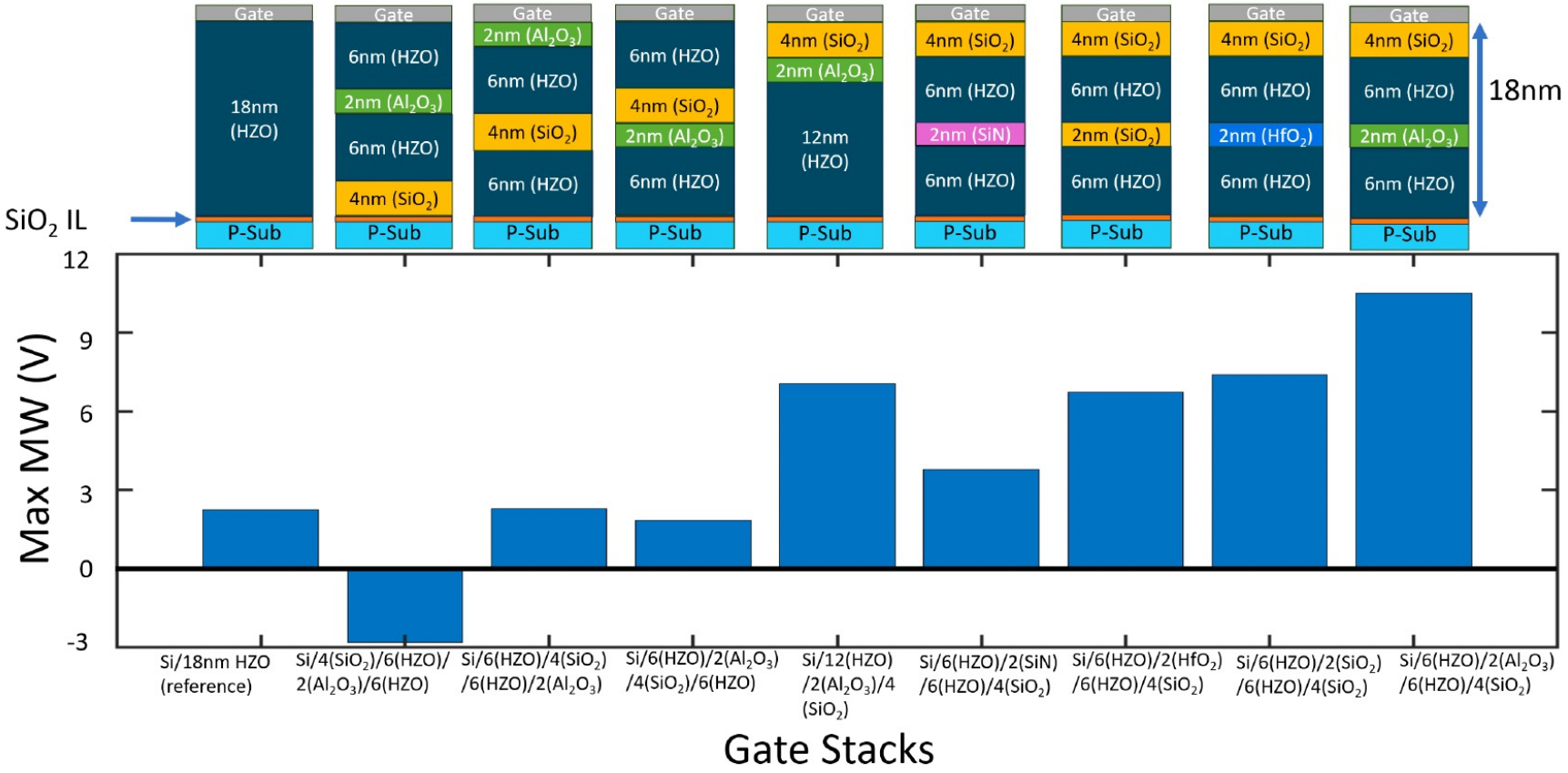
Position and choice of the dielectric



Fernandes, L., Ravindran, P. V., Chen, J., Tian, M., Das, D., Chen, H., ... & Khan, A. (2024). Optimizing Memory Window for Ferroelectric Nand Applications: An Experimental Study on Dielectric Material Selection and Layer Positioning. *IEEE Transactions on Electron Devices*.

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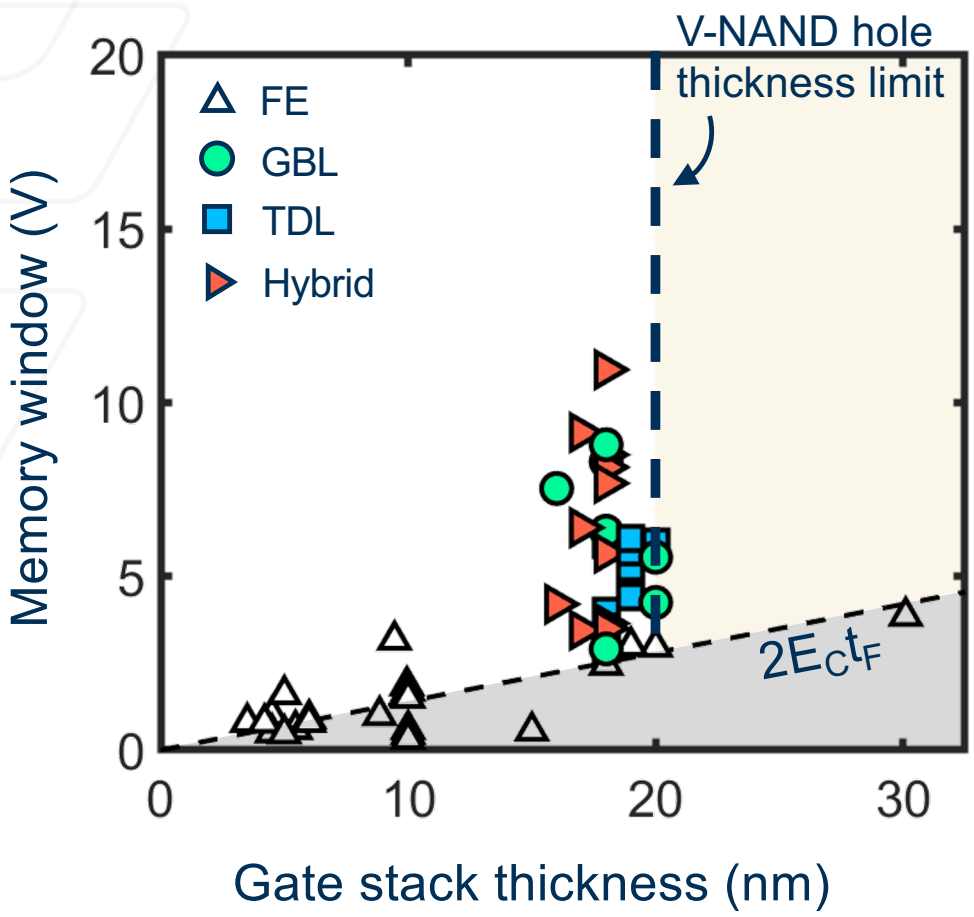
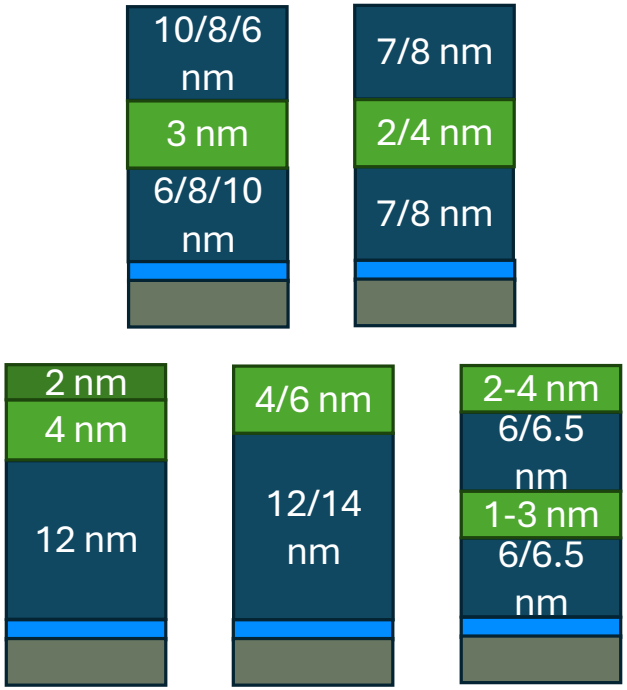




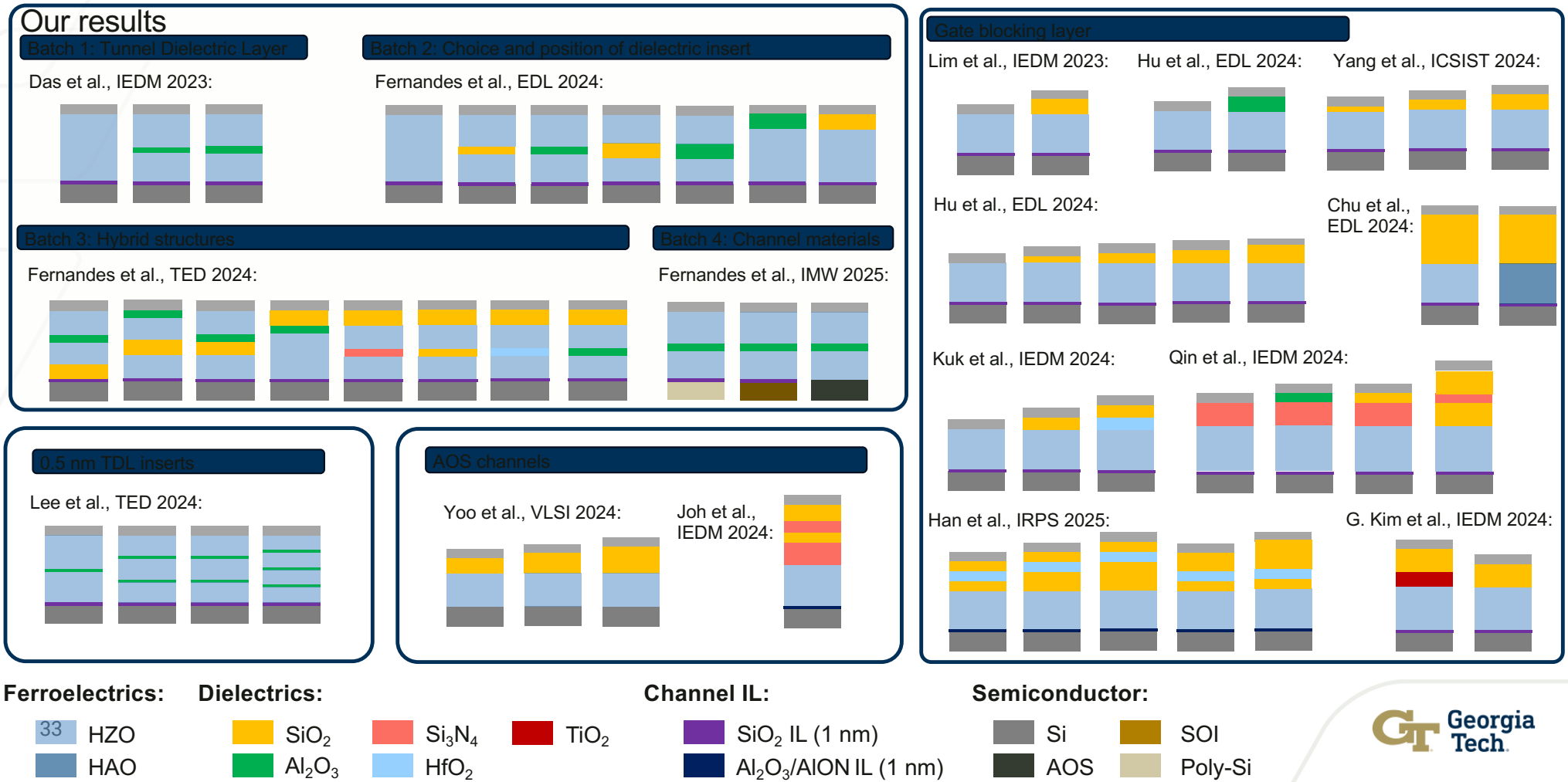
Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$

Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4

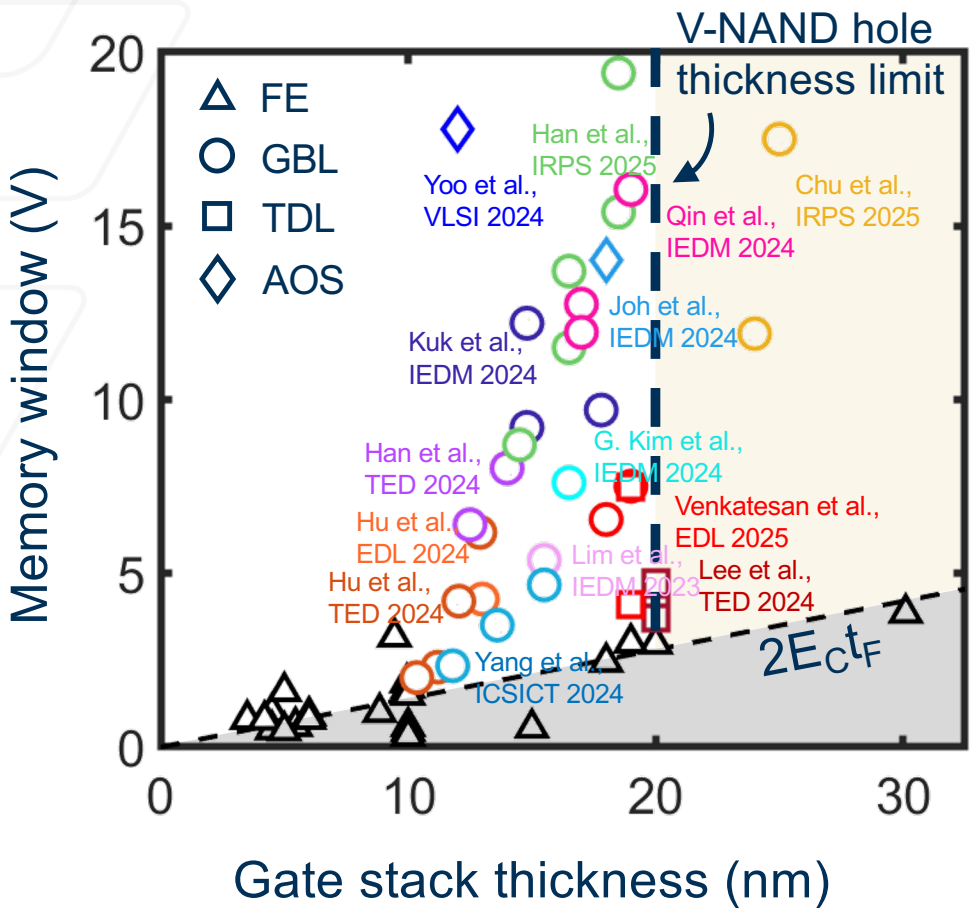
Channel IL: SiO_2

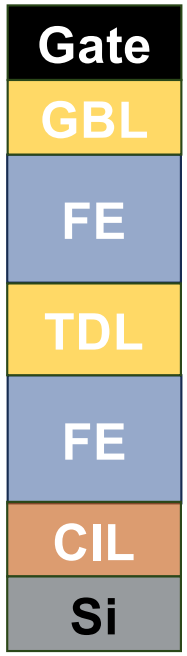
Semiconductor: Bulk Si, Poly Si, SOI, IWO

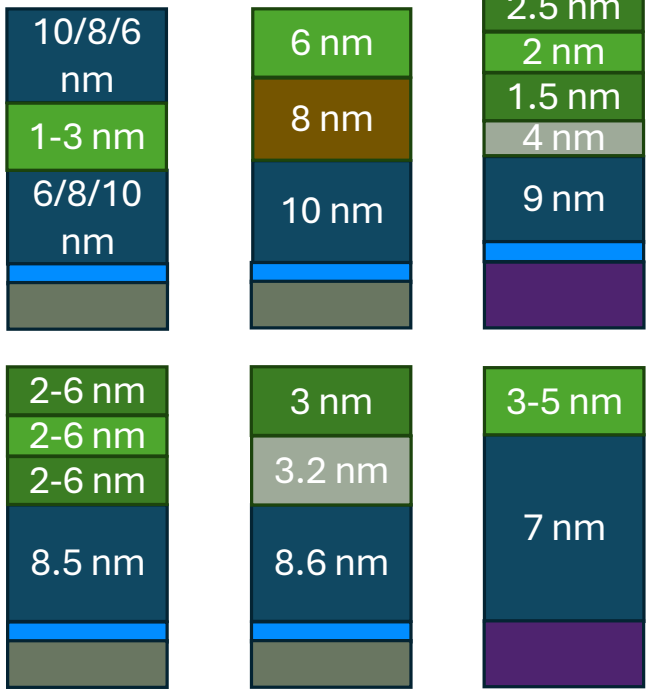
Increasing the MW by dielectric insertion



Increasing the MW by dielectric insertion







Ferroelectric: $Hf_{0.5}Zr_{0.5}O_2$

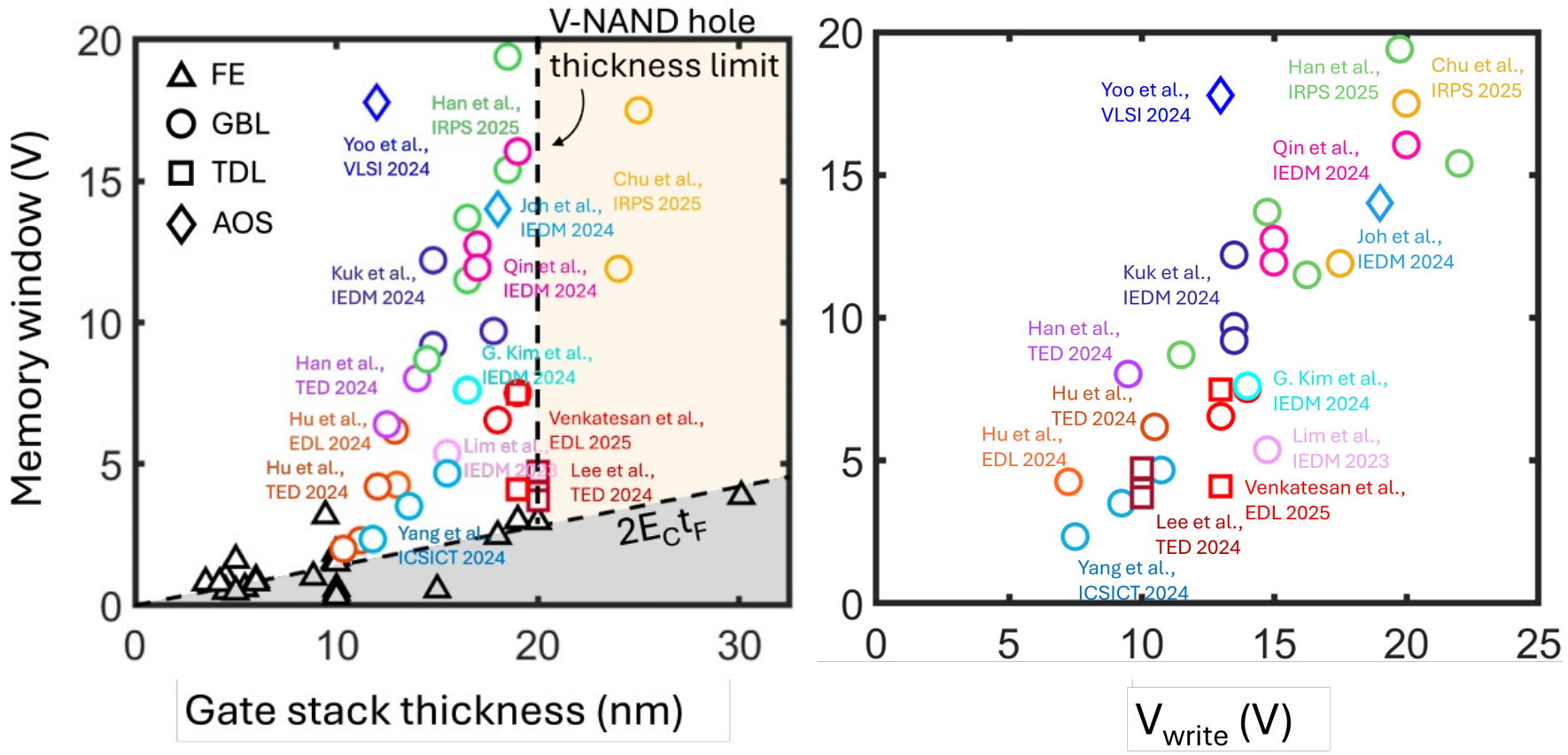
Dielectrics: SiO_2, Al_2O_3, HfO_2, Si_3N_4

High-k interlayer: HfO_2, Si_3N_4

Channel IL: SiO_2

Semiconductor: Bulk Si, Poly Si, SOI, IWO

Increasing the MW by dielectric insertion



Venkatesan, P., et al. IMW 2025

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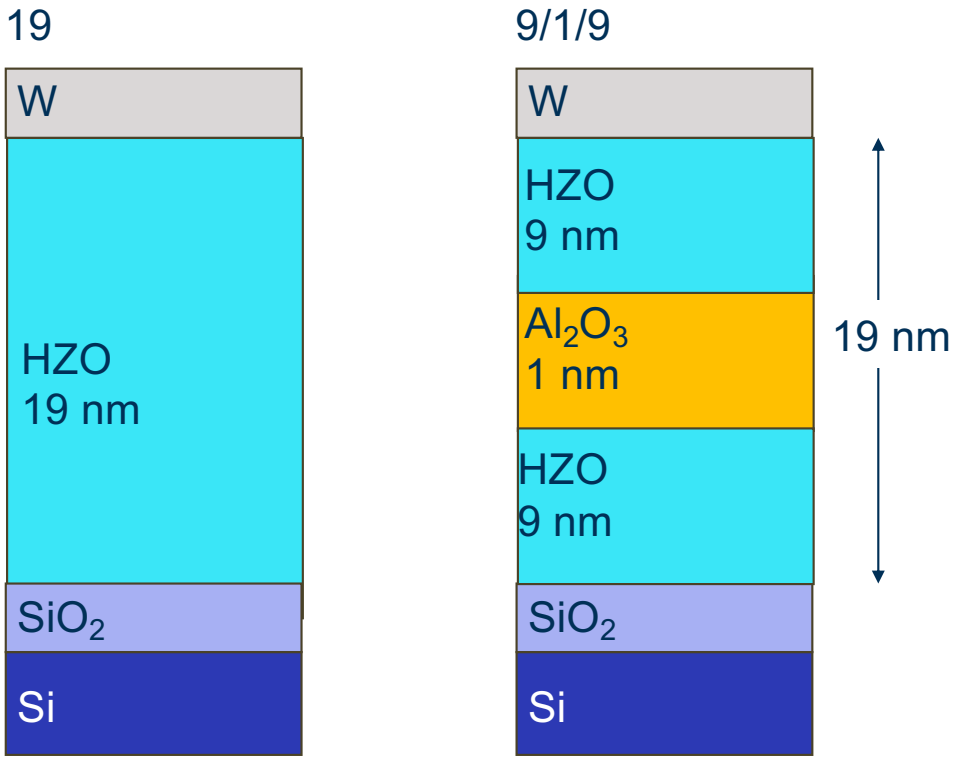
Where is the MW enhancement coming from?



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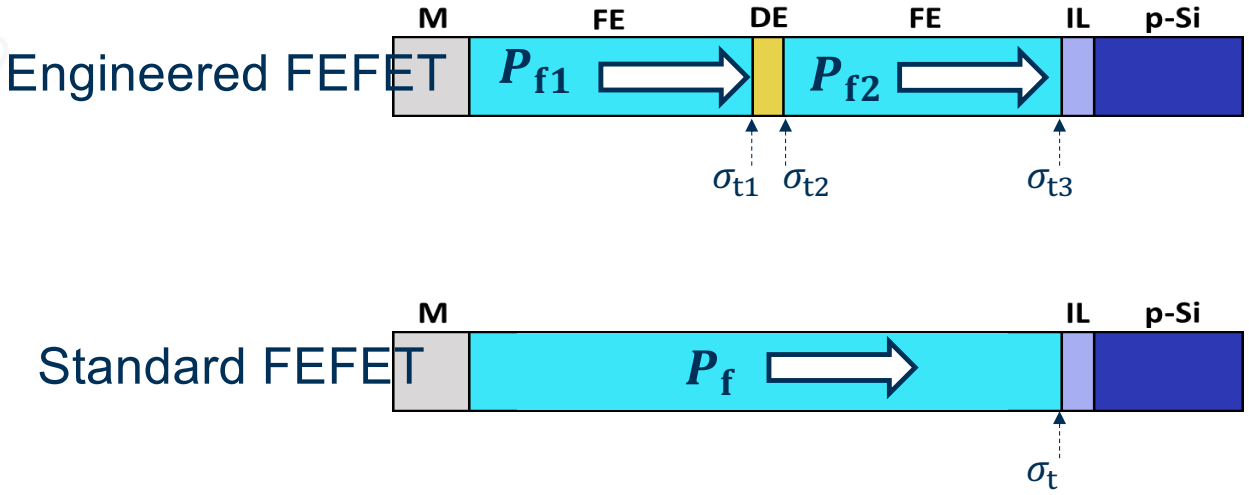

Trapped charges are the key differentiator.

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Modeling framework

1. Ferroelectric switching kinetics

Preisach model was adopted to describe the steady-state characteristics of the ferroelectric polarization.

The saturated polarization hysteresis loop is defined as

$$P^{+}_{\mathrm{sat,i}}(E_\mathrm{i}) = P_{\mathrm{s,i}} \tanh[(E_\mathrm{i} - E_{\mathrm{c,i}})/2\delta_\mathrm{i}] \quad \text{If } dE_\mathrm{i}/dt > 0$$

$$P^{-}_{\mathrm{sat,i}}(E_\mathrm{i}) = -P^{+}_{\mathrm{sat,i}}(-E_\mathrm{i}) \quad \text{If } dE_\mathrm{i}/dt < 0$$

where

$$\delta_\mathrm{i} = E_{\mathrm{c,i}} \left[\ln\left(\frac{1 + P_{\mathrm{r,i}}/P_{\mathrm{s,i}}}{1 - P_{\mathrm{r,i}}/P_{\mathrm{s,i}}} \right) \right]^{-1} \quad \text{For } i = 1,2$$

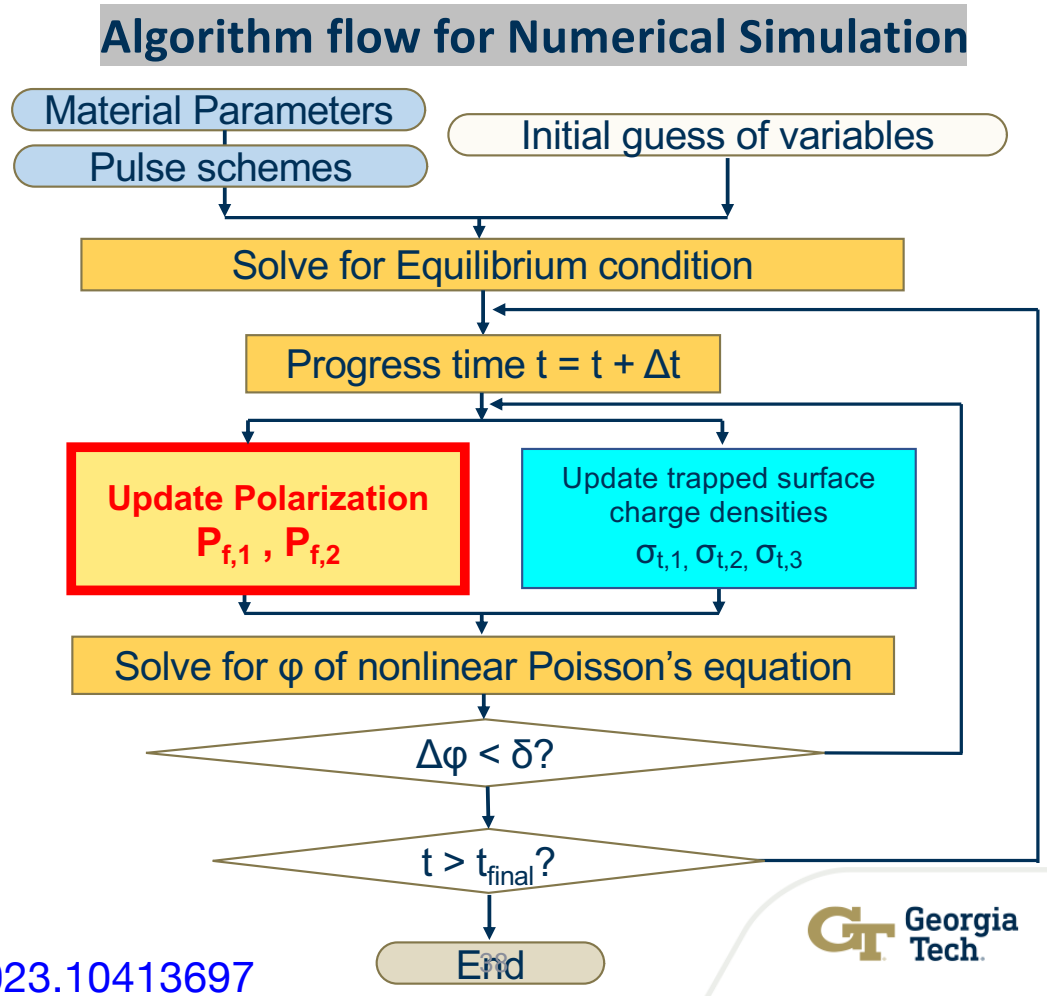
The derivative of the polarization is given by

$$\frac{dP_{\mathrm{f,i}}}{dE_\mathrm{i}} = \Gamma_\mathrm{i} \frac{dP_{\mathrm{sat,i}}}{dE_\mathrm{i}} \quad \text{For } i = 1,2$$

where

$$\Gamma_\mathrm{i} = 1 - \tanh\left[\left(\frac{P_{\mathrm{f,i}} - P_{\mathrm{sat,i}}}{\xi_\mathrm{i} P_{\mathrm{s,i}} - P_{\mathrm{f,i}}} \right)^{1/2} \right]$$

$\xi_\mathrm{i} = +1$ when $dE_\mathrm{i}/dt > 0$ and $\xi = -1$ when $dE_\mathrm{i}/dt < 0$



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Modeling framework

2. Rate equations for trapping and de-trapping

Assuming single level traps, define

$N_{t,1}$ / $P_{t,1}$: Acceptor/Donor-like trap density at HZO/Al_2O_3

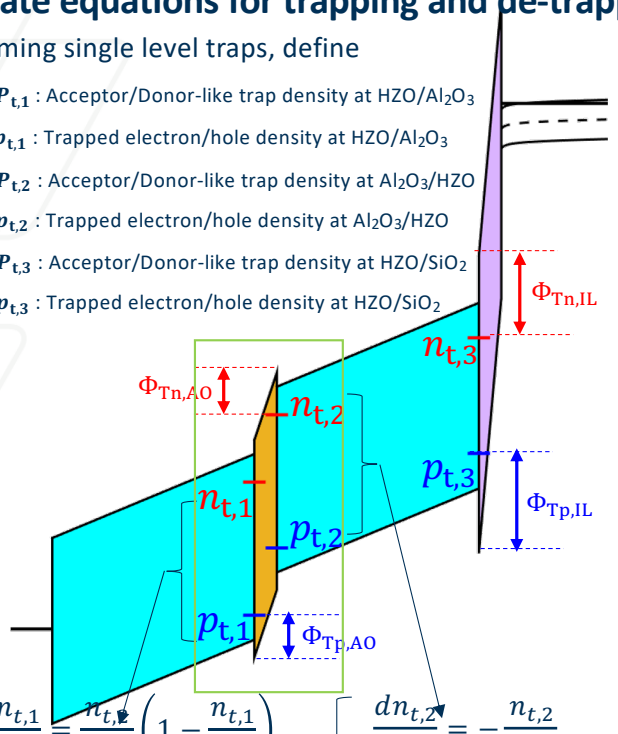
$n_{t,1}$ / $p_{t,1}$: Trapped electron/hole density at HZO/Al_2O_3

$N_{t,2}$ / $P_{t,2}$: Acceptor/Donor-like trap density at Al_2O_3/HZO

$n_{t,2}$ / $p_{t,2}$: Trapped electron/hole density at Al_2O_3/HZO

$N_{t,3}$ / $P_{t,3}$: Acceptor/Donor-like trap density at HZO/SiO_2

$n_{t,3}$ / $p_{t,3}$: Trapped electron/hole density at HZO/SiO_2



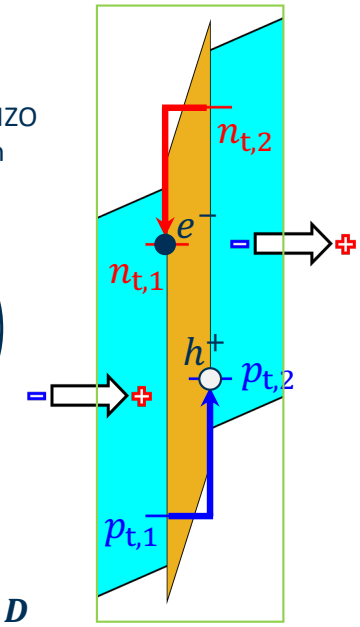
$$\frac{dn_{t,1}}{dt} = \frac{n_{t,2}}{\tau_{cn1}}\left(1 - \frac{n_{t,1}}{N_{t,1}}\right) \qquad \frac{dn_{t,2}}{dt} = -\frac{n_{t,2}}{\tau_{en2}}$$

$$\frac{dp_{t,1}}{dt} = -\frac{p_{t,1}}{\tau_{ep1}} \qquad \frac{dp_{t,2}}{dt} = \frac{p_{t,1}}{\tau_{cp2}}\left(1 - \frac{p_{t,2}}{P_{t,2}}\right)$$

The net trapped charges $\sigma_{t,i}$ are $\sigma_{t,i} = q(p_{t,i} - n_{t,i})$ For $i = 1,2,3$

The emission mechanism of the trapped charges at Al_2O_3/HZO (HZO/Al_2O_3) interfaces are assumed to be Fowler-Nordheim (FN) tunneling → **Al_2O_3 as "Tunnel Dielectric Layer"**

$$\tau_{en(p),i=2(1)} = \tau_{cn(p),i=1(2)} = \tau_0 \exp\left(-\frac{4\sqrt{2m_{AO}\Phi^3_{Tn(p),AO}}}{3q\hbar E_{AO}}\right)$$



3. Nonlinear Poisson-Boltzmann equation

For gate oxides, $\frac{\partial D}{\partial x} = 0$

With boundary conditions of the displacement field $\boldsymbol{D}$ continuity at the interfaces i with given $\boldsymbol{P_{f,i}}$ and $\boldsymbol{\sigma_{t,i}}$

For semiconductors,

$$\frac{\partial^2 \varphi}{\partial x^2} = -\frac{q}{\epsilon_s}\left[p_{po}(\exp(-\beta\varphi) - 1) - n_{po}(\exp(\beta\varphi) - 1)\right]$$

Thus, Flat band voltage is given by

$$V_{FB} = \phi_{MS} - \frac{\sigma_{it}(\psi_s)}{C_{tot}} - \frac{P_{f,1} + \sigma_{t,1} + \sigma_{t,2} + \sigma_{t,3}}{C_{f,1}} - \frac{\sigma_{t,2} + \sigma_{t,3}}{C_d} - \frac{P_{f,2} + \sigma_{t,3}}{C_{f,2}}$$

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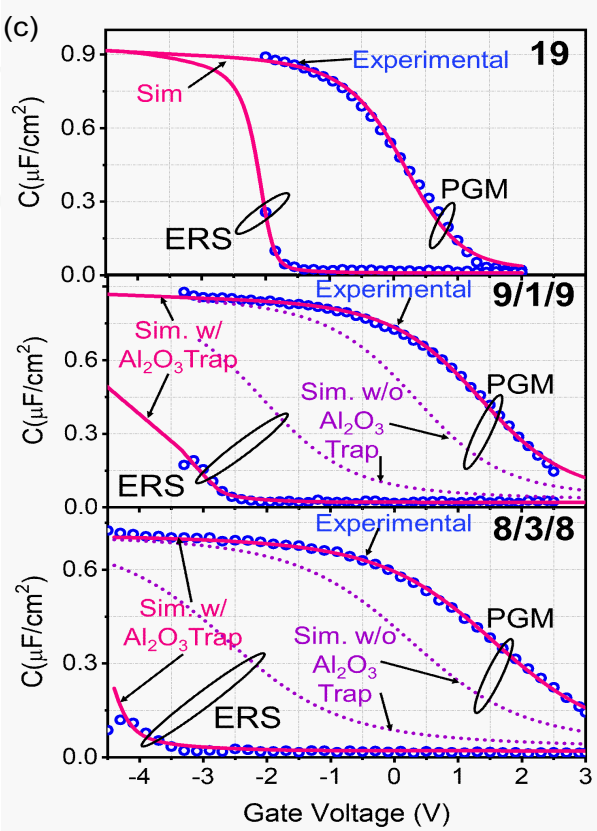
Experimental Calibration



Charge trapping in Al_2O_3 required to match the MW for 8/3/8 and 9/1/9.

Symbols	Description	19	9/1/9	8/3/8
ϵ_i	Dielectric constant of SiO_2	3.9	3.9	3.9
ϵ_d	Dielectric constant of Al_2O_3	-	8.9	8.9
ϵ_f	Dielectric constant of HZO	28	27	26
P_s	Saturated polarization	20 μC/cm²	15 μC/cm²	15 μC/cm²
P_r	Remanent polarization	17 μC/cm²	13 μC/cm²	13 μC/cm²
E_c	Coercive field	1.2 MV/cm	1.2 MV/cm	1.2 MV/cm
m_{AO}	Tunneling mass of Al_2O_3	-	$0.5\ m_0$	$0.5\ m_0$
m_{IL}	Tunneling mass of SiO_2	$0.5\ m_0$	$0.5\ m_0$	$0.5\ m_0$
$\Phi_{Bn,IL}$	SiO_2 electron de-trapping barriers	2.35 eV	2.35 eV	2.35 eV
$\Phi_{Bp,IL}$	SiO_2 hole de-trapping barriers	2.85 eV	2.85 eV	2.85 eV
$\Phi_{Tn,AO}$	Al_2O_3 electron tunneling barriers	-	1.20 eV	1.20 eV
$\Phi_{Tp,AO}$	Al_2O_3 hole tunneling barriers	-	1.40 eV	1.40 eV
N_{t1}, P_{t1}	Electron, hole Trap density at interface 1	-	$6.2\times10^{13}cm^{-2}$	$6.2\times10^{13}cm^{-2}$
N_{t2}, P_{t2}	Electron, hole Trap density at interface 2	-	$6.2\times10^{13}cm^{-2}$	$6.2\times10^{13}cm^{-2}$
N_{t3}, P_{t3}	Electron, hole Trap density at interface 3	$1.2\times10^{14}cm^{-2}$	$1.2\times10^{14}cm^{-2}$	$1.2\times10^{14}cm^{-2}$
D_{it}	Density of states at Si/SiO_2	$1.2\times10^{14}cm^{-2}eV^{-1}$	$1.4\times10^{14}cm^{-2}eV^{-1}$	$1.4\times10^{14}cm^{-2}eV^{-1}$
	Intrinsic time constant for tunneling	1 ns	1 ns	1 ns

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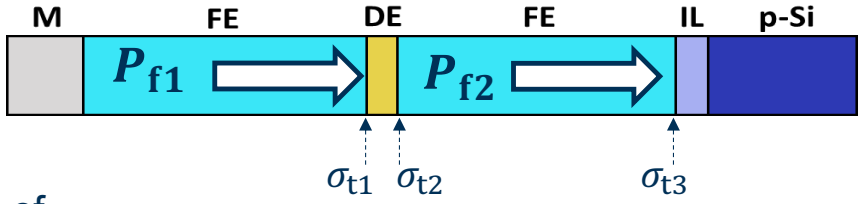
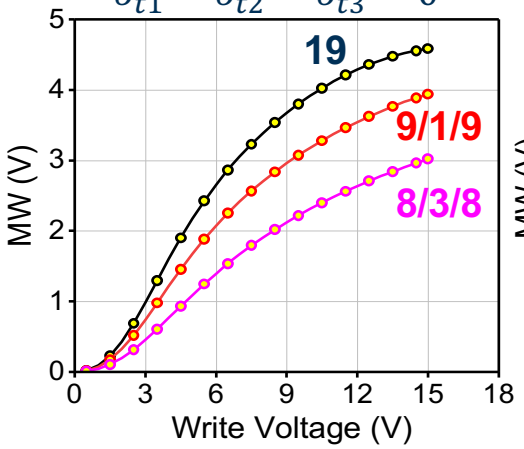
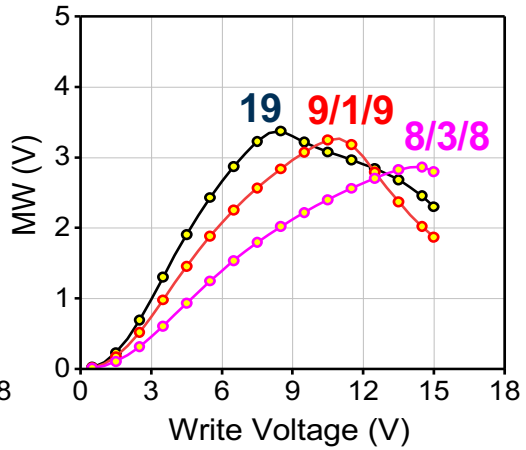
Decoupling the impacts of different trapping mechanisms



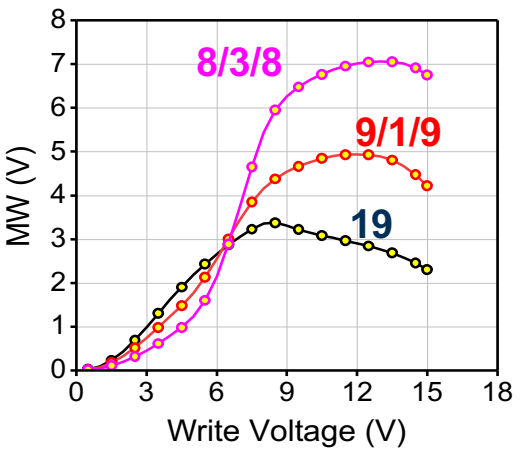
Absence of screening trap charges
$\sigma_{t1} = \sigma_{t2} = \sigma_{t3} = 0$



HZO/SiO_2 Traps only
$\sigma_{t1} = \sigma_{t2} = 0;\ \sigma_{t3} \neq 0$



Al_2O_3/HZO + HZO/SiO_2 Traps
$\sigma_{t1} \neq 0;\ \sigma_{t2} \neq 0;\ \sigma_{t3} \neq 0$



Trap effects are responsible for the observed MW trend
(MW: 8/3/8 >9/1/9>19)

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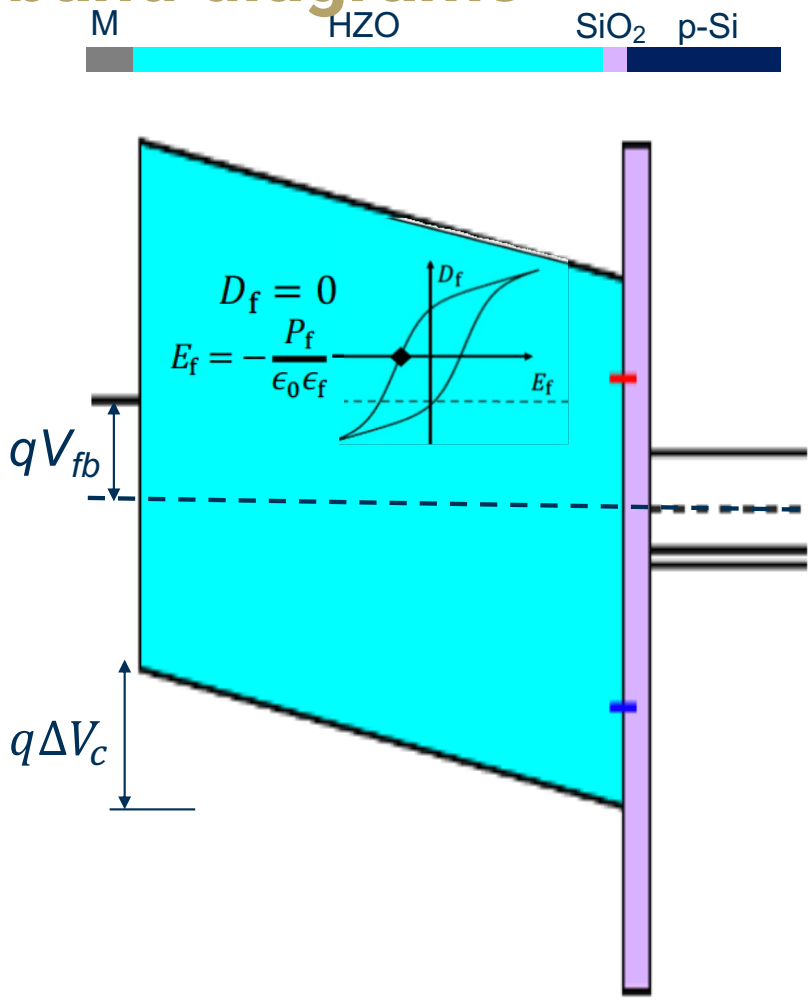
MW enhancement mechanism with band diagrams



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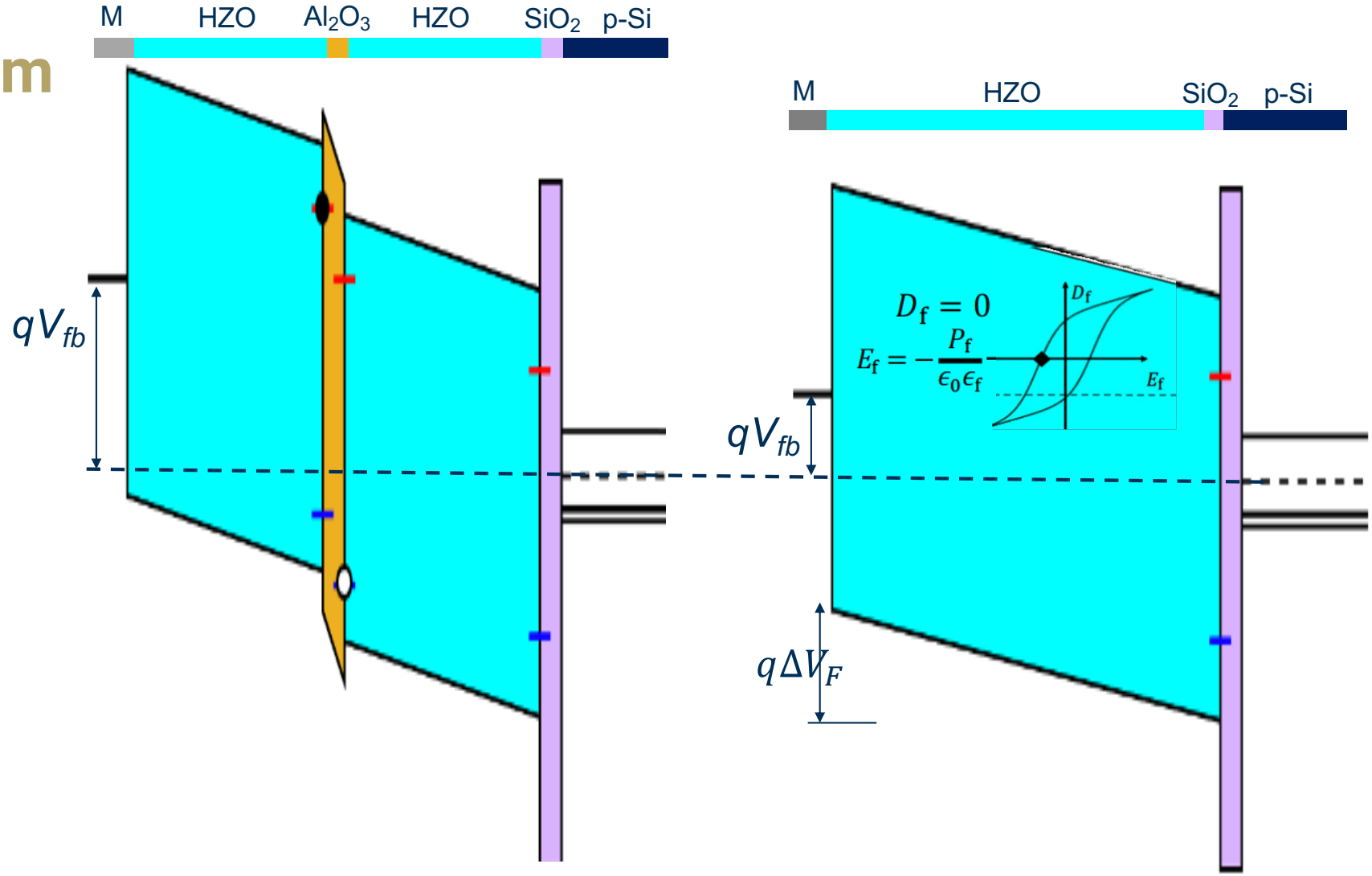
MW mechanism



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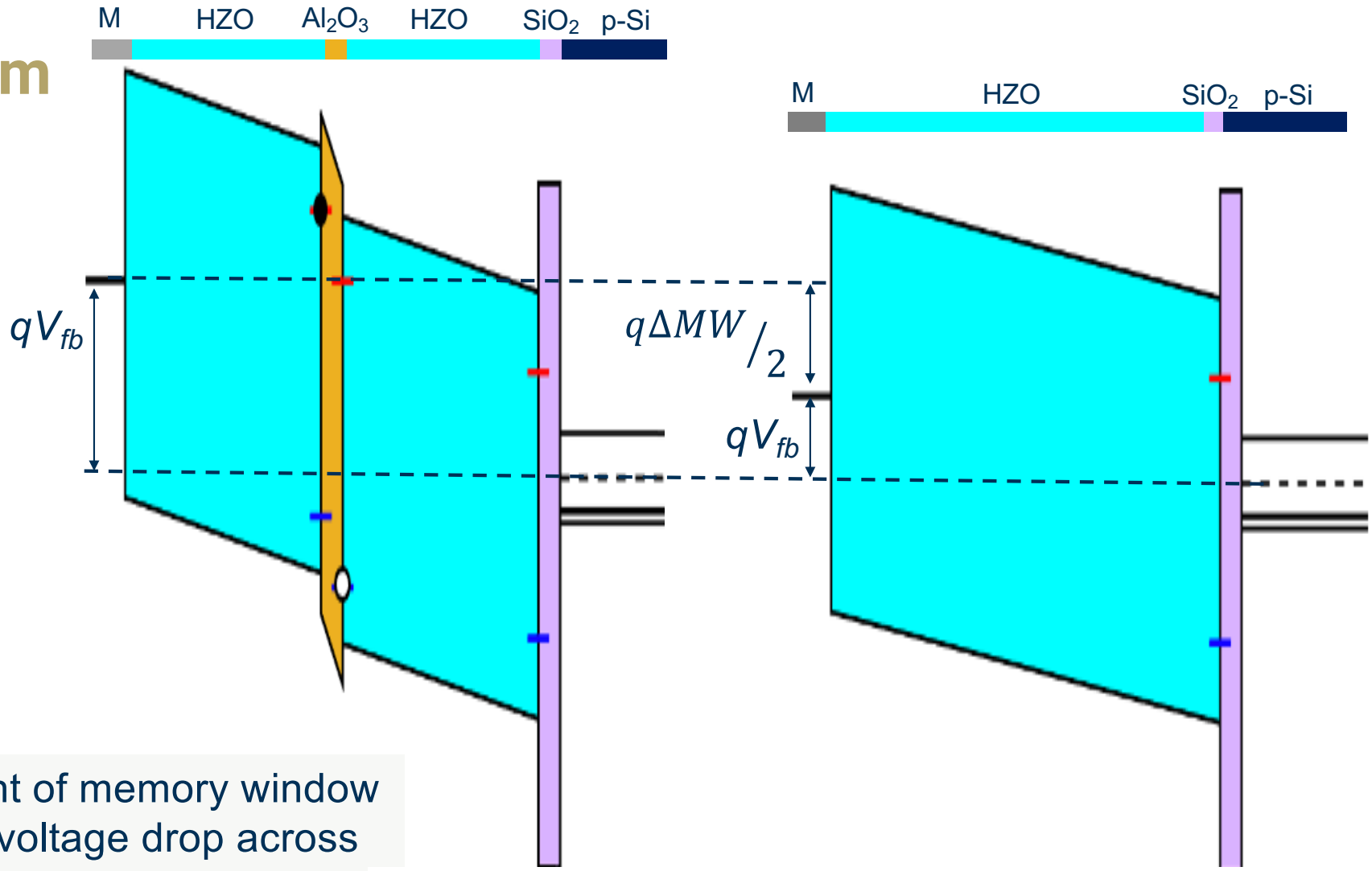
MW mechanism



Enhancement of memory window ΔMW ≈2 x voltage drop across Al_2O_3 at flatband

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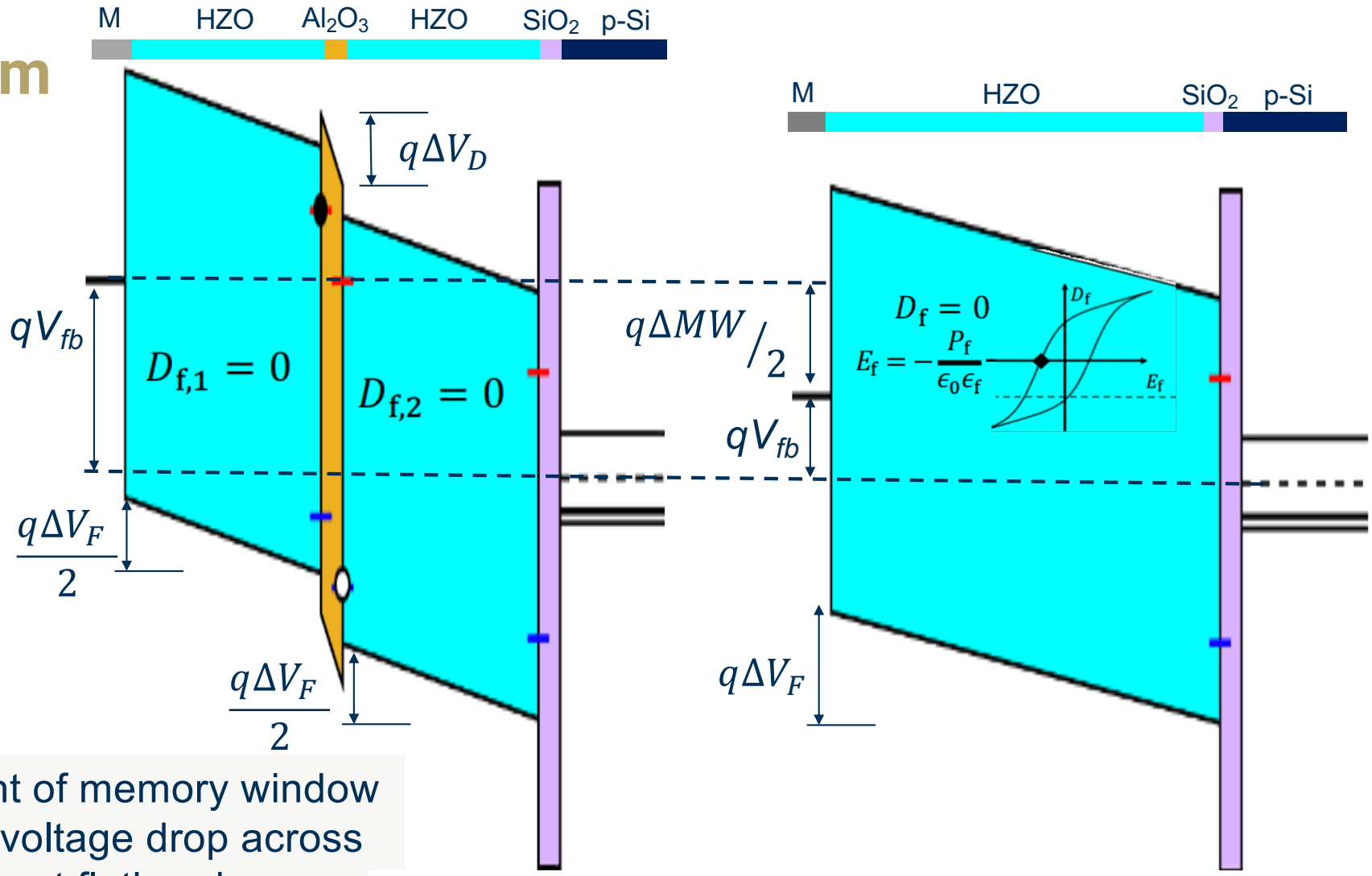
MW mechanism



Enhancement of memory window $\Delta MW \approx 2$ x voltage drop across Al_2O_3 at flatband

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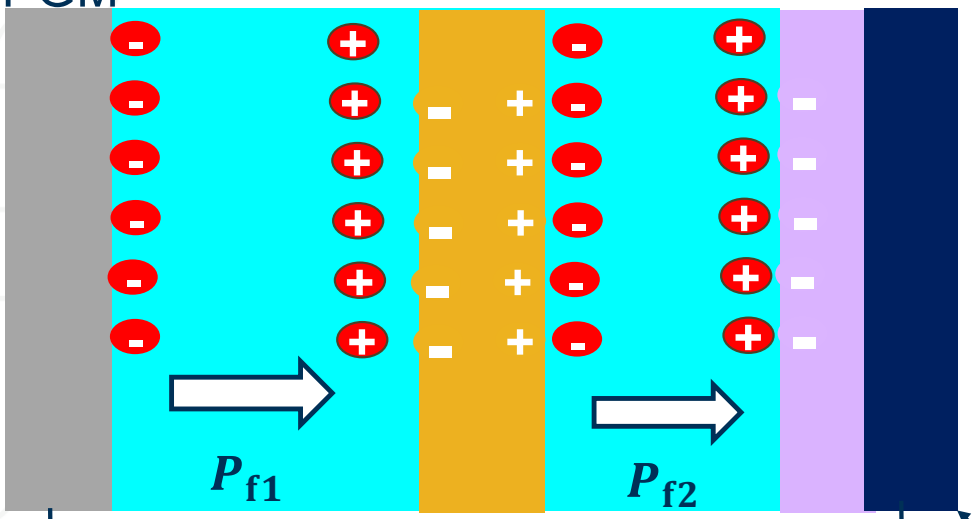
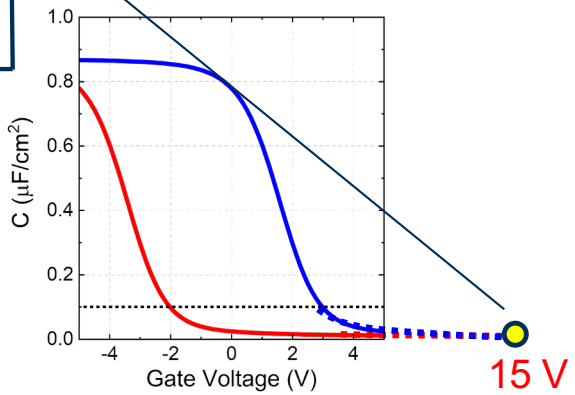
Where does the built-in electric field come from?

PGM





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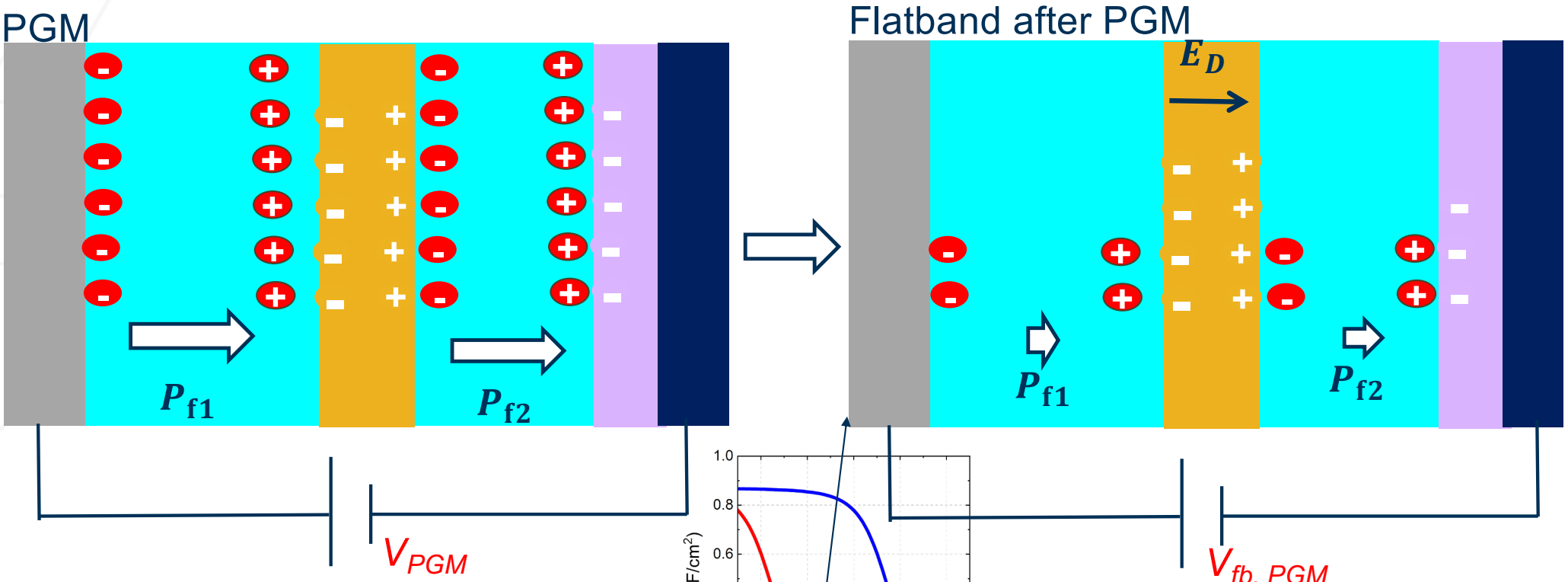

Built-in electric field due to defect dipole in the dielectric induced by the ferroelectric polarization leads to the MW enhancement.

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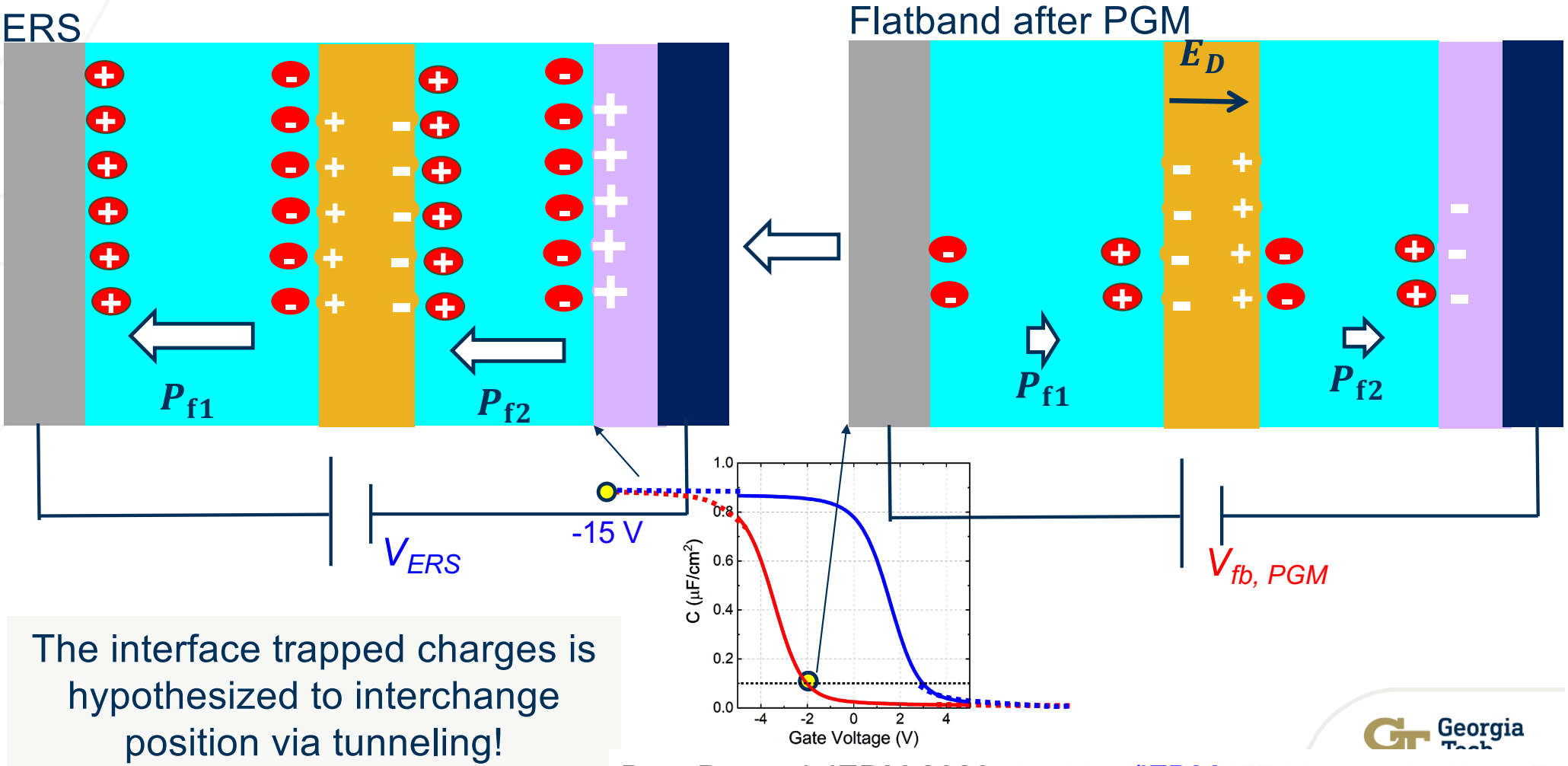
Why do we call it a tunnel dielectric?



The interface trapped charges is hypothesized to interchange position via tunneling!

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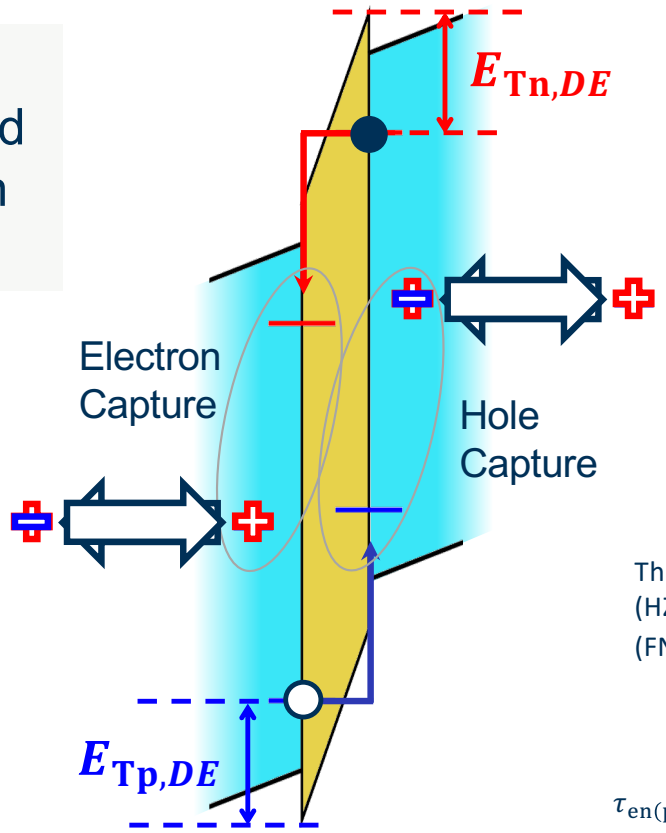

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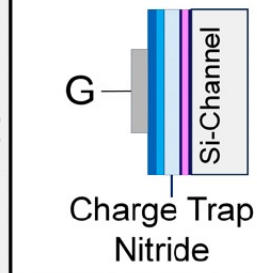
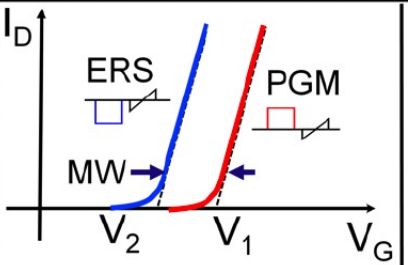
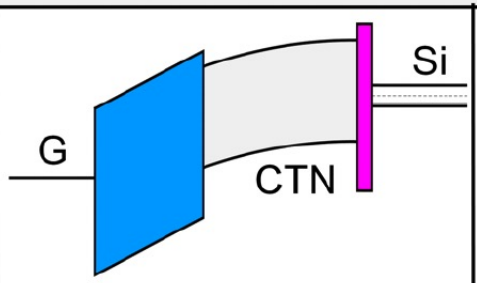
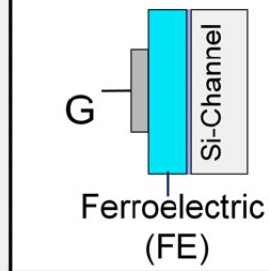
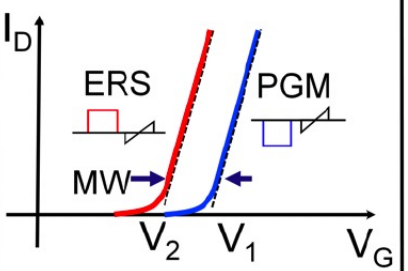
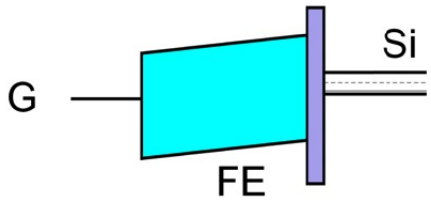
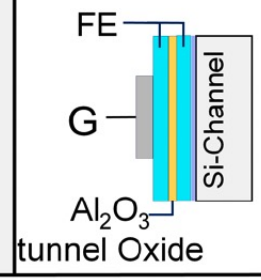
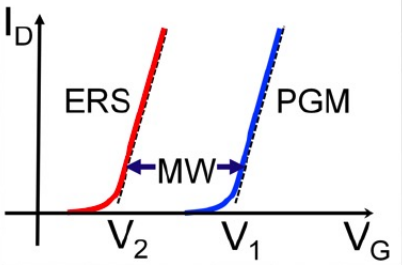
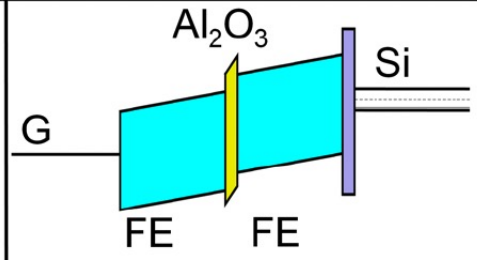
Charge trap flash vs ferroelectric flash

	Structure	Characteristics	Band diagram at FB condition	Attributes
Charge Trap Flash				✓ Large MW × Large Write Voltage Mechanism: Trapping
Conventional FEFET				× Low MW ✓ Low Write Voltage Mechanism: Polarization Switching
Proposed FEFET				✓ Large MW ✓ Moderate Write Voltage Mechanism: Polarization Switching + Trapping + Tunneling

Das, D., et al. IEDM 2023: 10.1109/IEDM45741.2023.10413697

What about reliability of ferroelectric NAND?

1. Retention
2. Disturb
3. Write endurance
4. Lateral charge migration
5. Device-device variation

⋮

What about reliability of ferroelectric NAND?

Performance

Memory window

Device Reliability

Retention

Disturb

Write Endurance

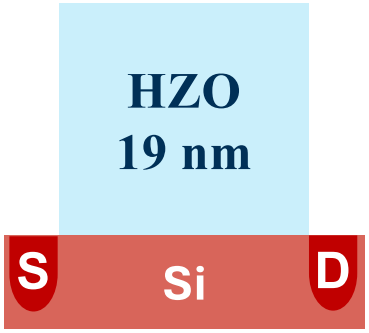
Array-level Reliability

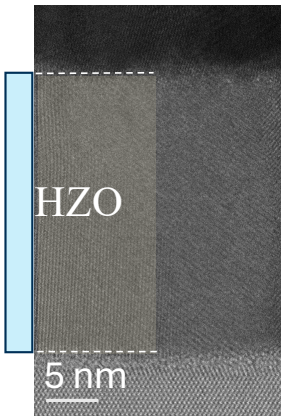
Lateral charge migration

Device-device variation

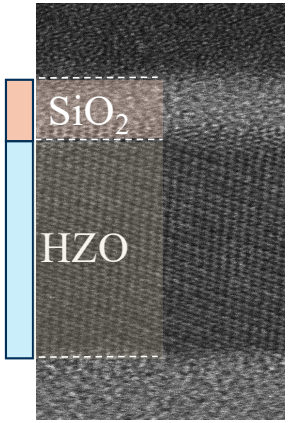
Ferroelectric NAND gate stacks

FE (ref.)
19

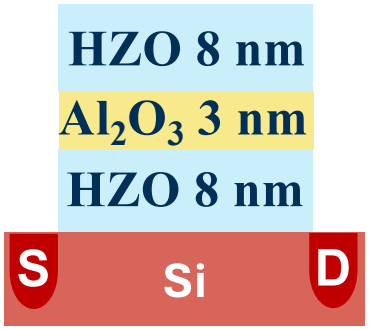


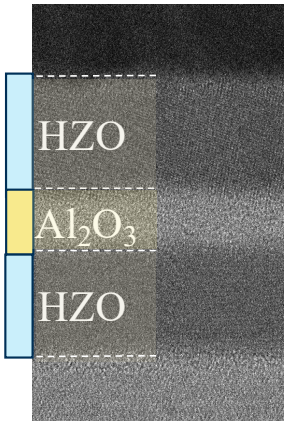


Gate blocking layer (GBL)
14/4(Si)

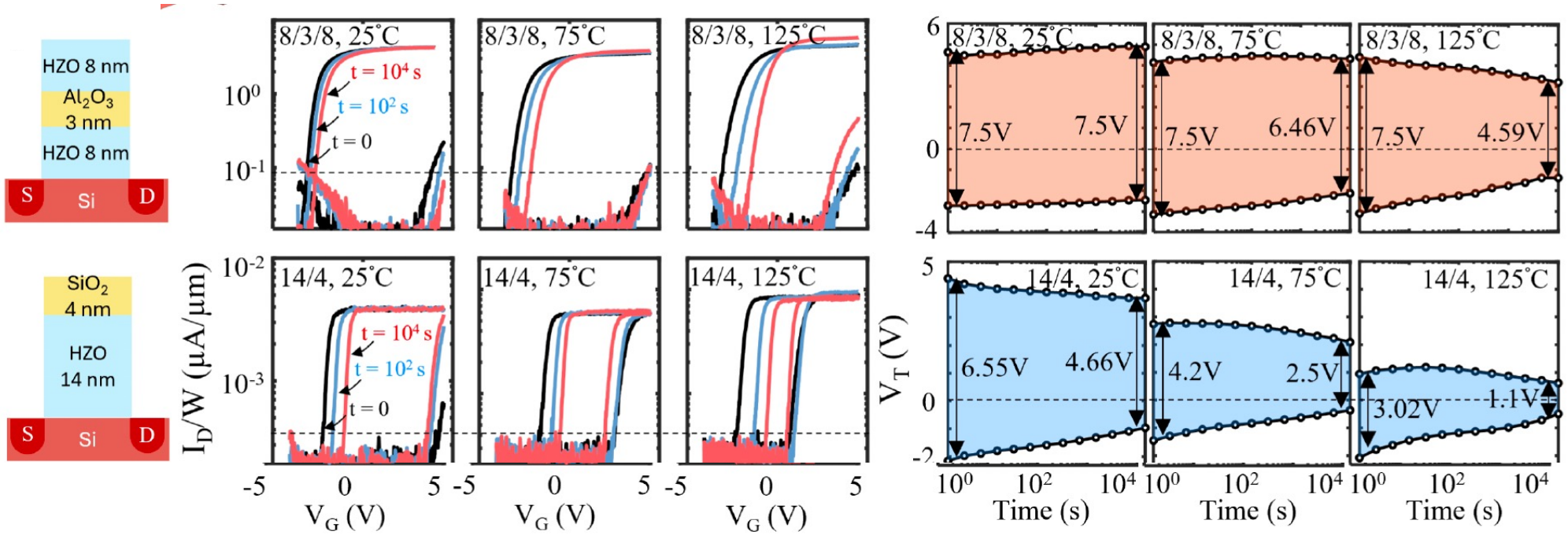


Tunnel dielectric layer (TDL)
8/3(Al)/8



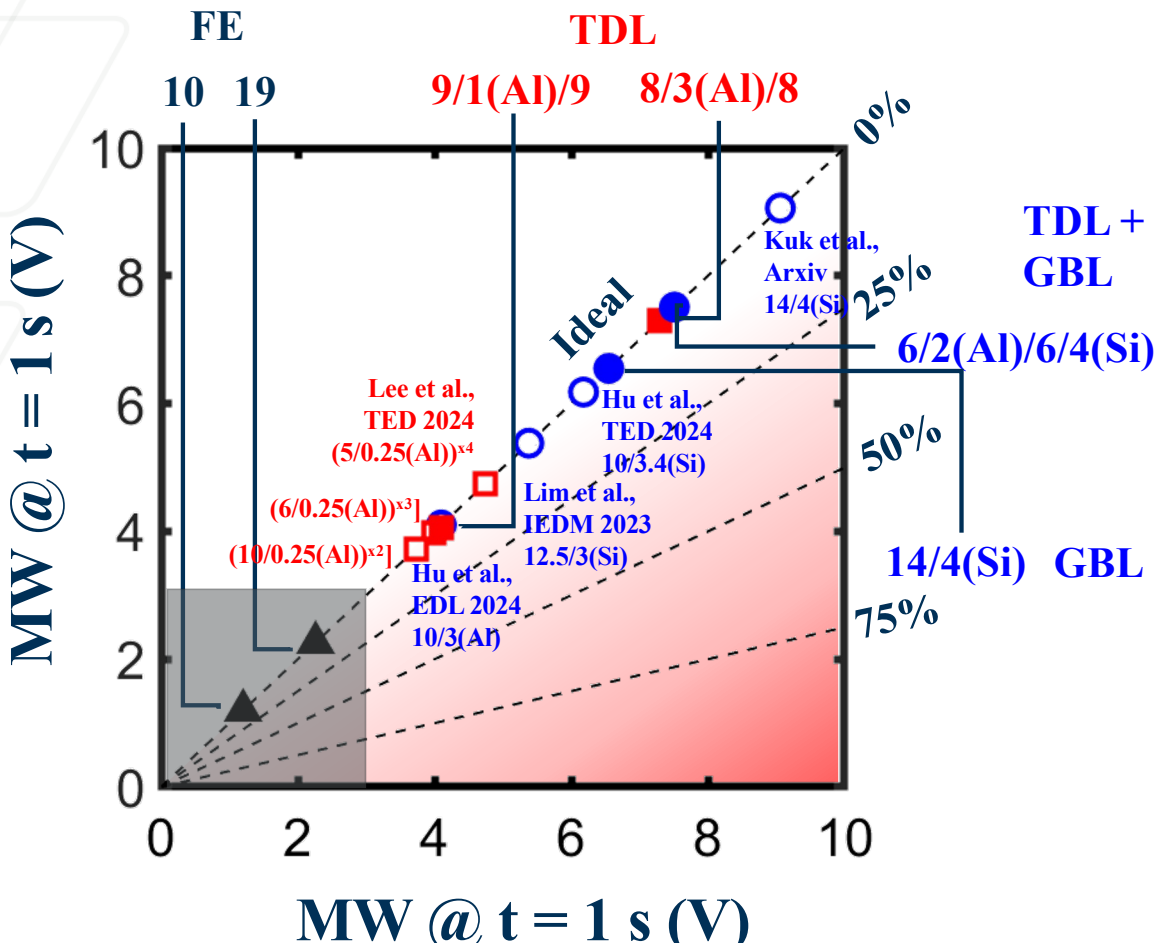


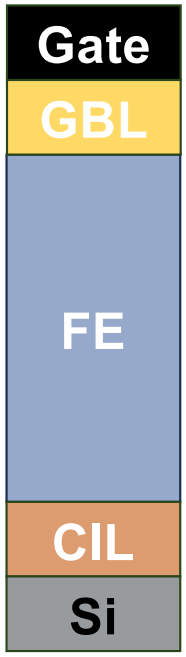
Retention characterization



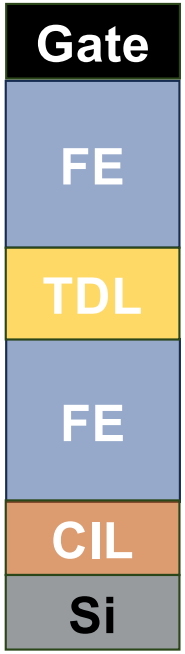
Venkatesan, P., Fernandes, L., Ravikumar, P., Park, C., Tran, H., Wang, Z., ... & Khan, A. (2025). Demonstration of Robust Retention in Band engineered FEFETs for NAND Storage Applications using Tunnel Dielectric Layer. *IEEE Electron Device Letters*.[Editors' Pick]

MW loss in FE-NAND





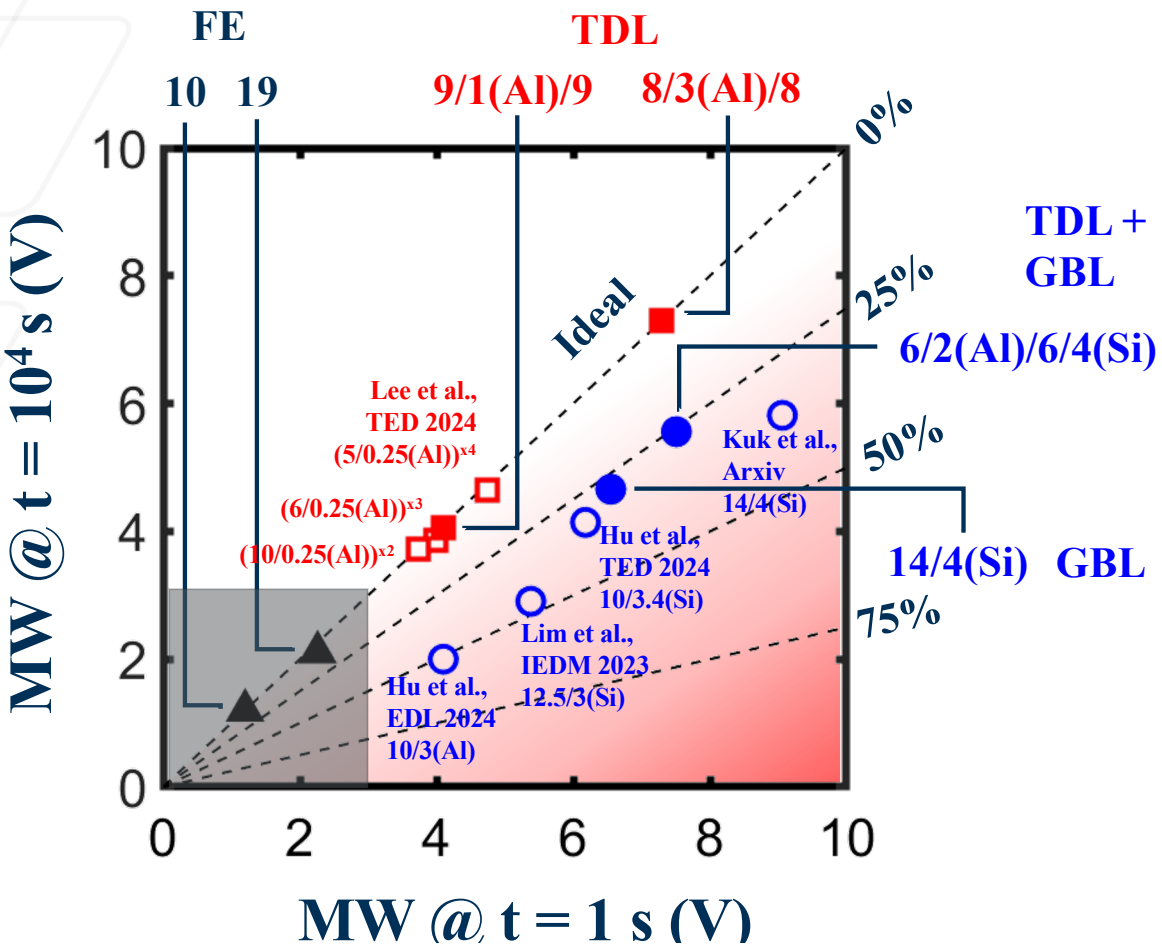
Gate blocking layer (GBL)

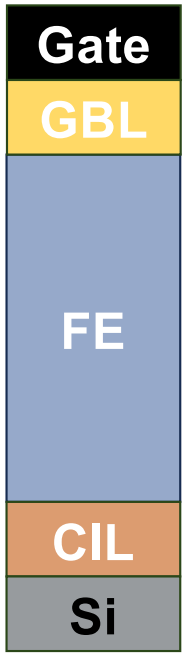


Tunnel dielectric layer (TDL)

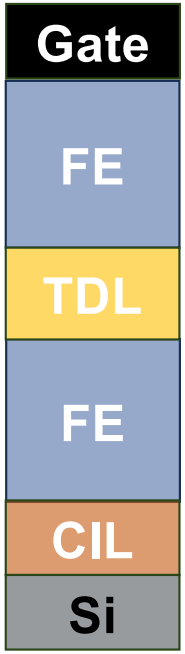
Venkatesan, P., et al. EDL 2025: 10.1109/LED.2024.3523235

MW loss in FE-NAND





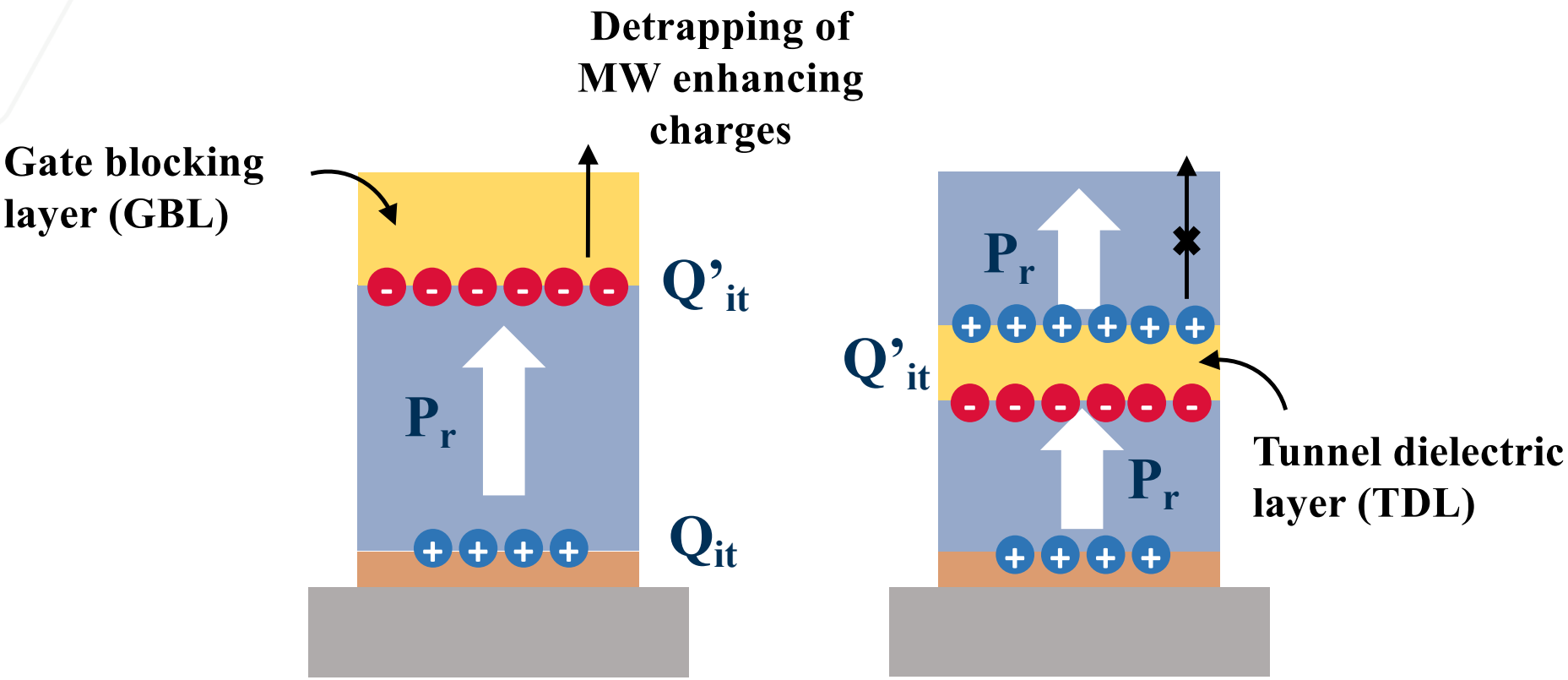
Gate blocking layer (GBL)



Tunnel dielectric layer (TDL)

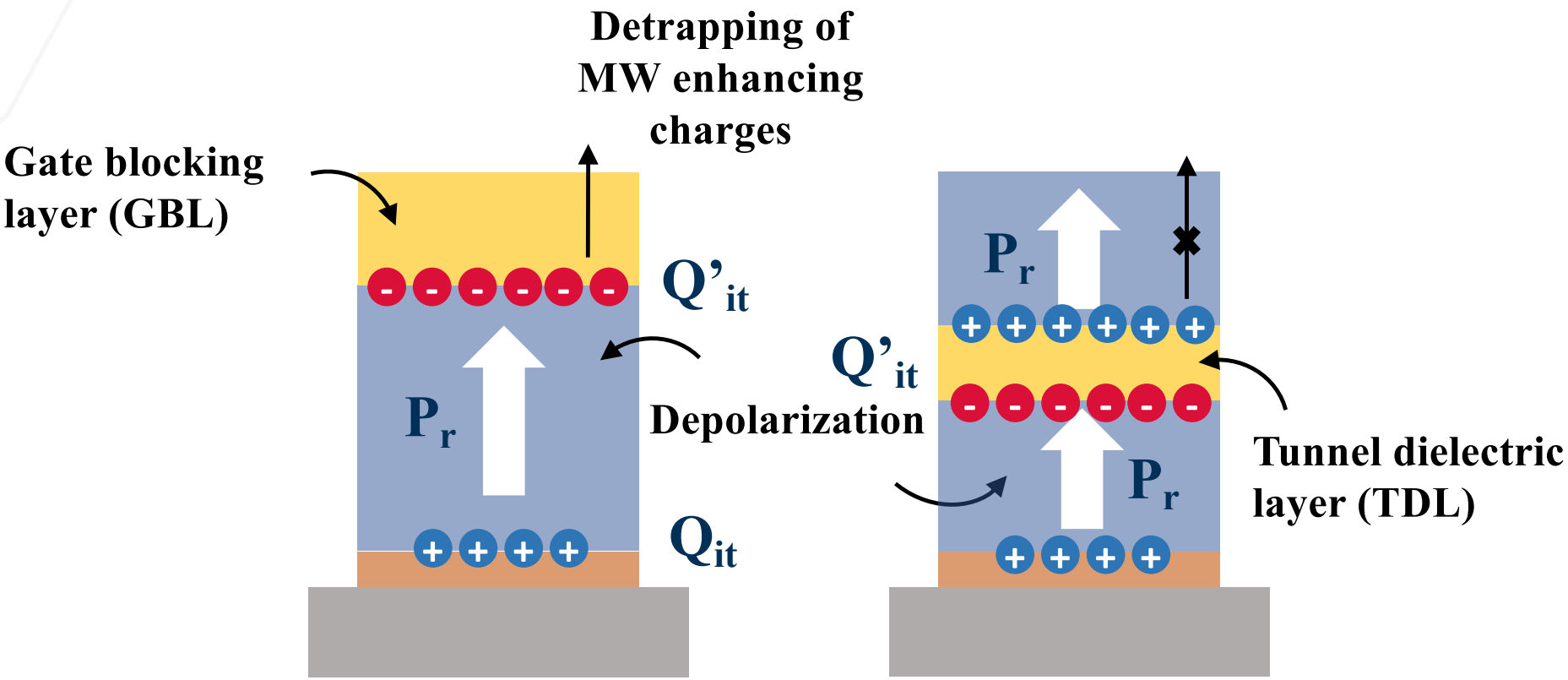
Venkatesan, P., et al. EDL 2025: 10.1109/LED.2024.3523235

Detrapping mechanisms



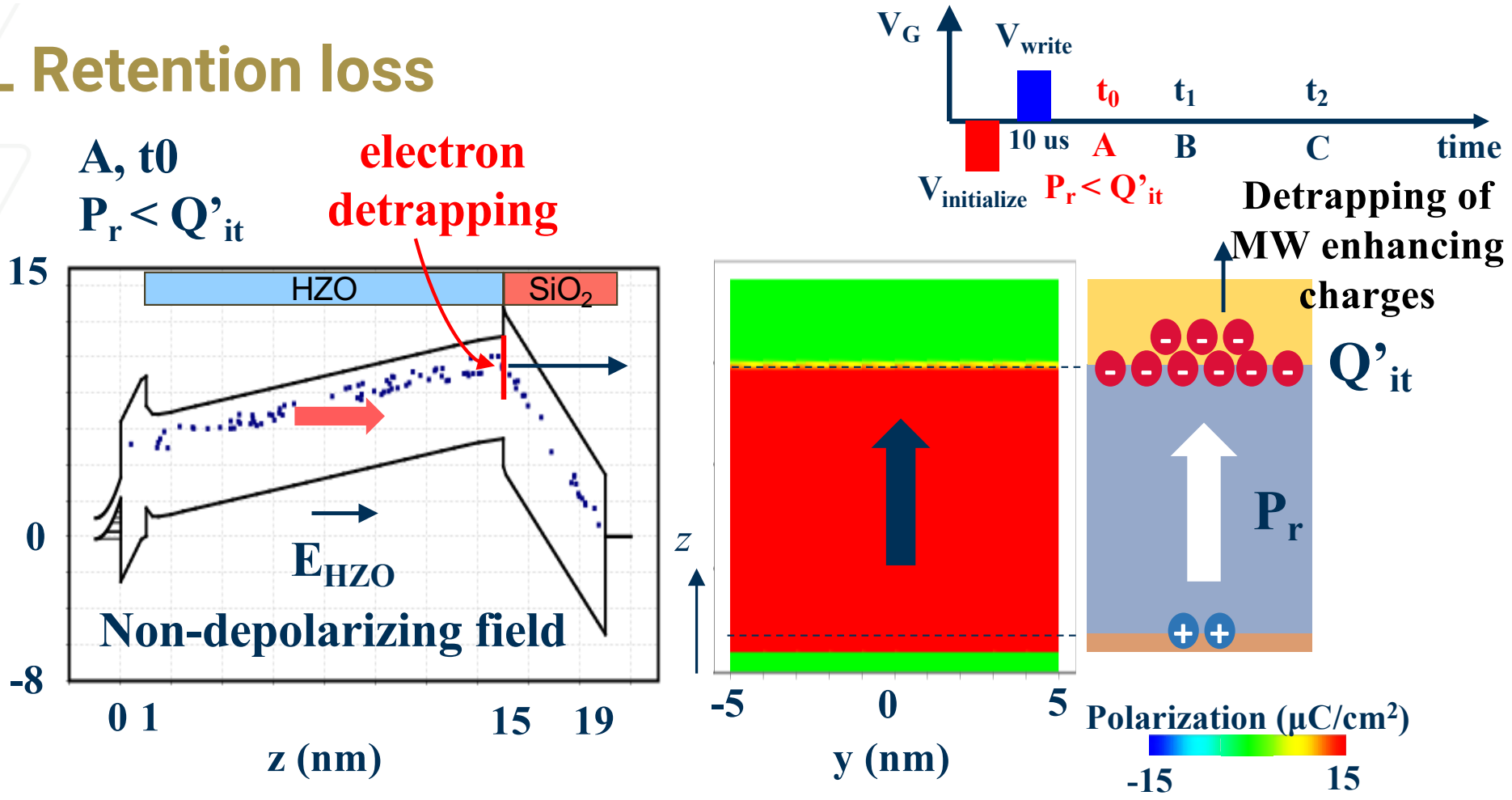
Venkatesan, P., Padovani, A., ... & Khan, A. (2025). Enhanced Memory Performance in Ferroelectric NAND applications: The Role of Tunnel Dielectric position for Robust 10-year Retention. In *2025 IEEE International Reliability Physics Symposium (IRPS)* (pp. 1-6). IEEE. *(Highlighted paper)*

Retention loss mechanisms



Venkatesan, P., et al. IRPS 2025

GBL Retention loss



The high field across the GBL drives out the MW enhancing charges leading to loss of the MW enhancement.

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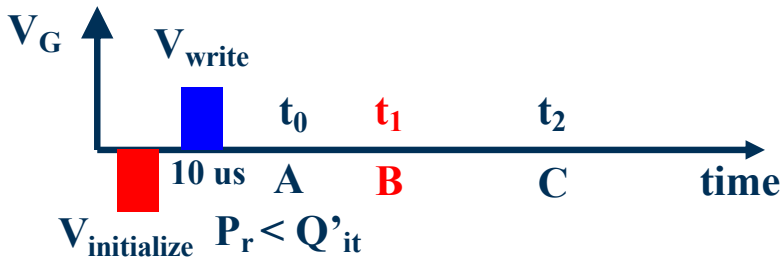
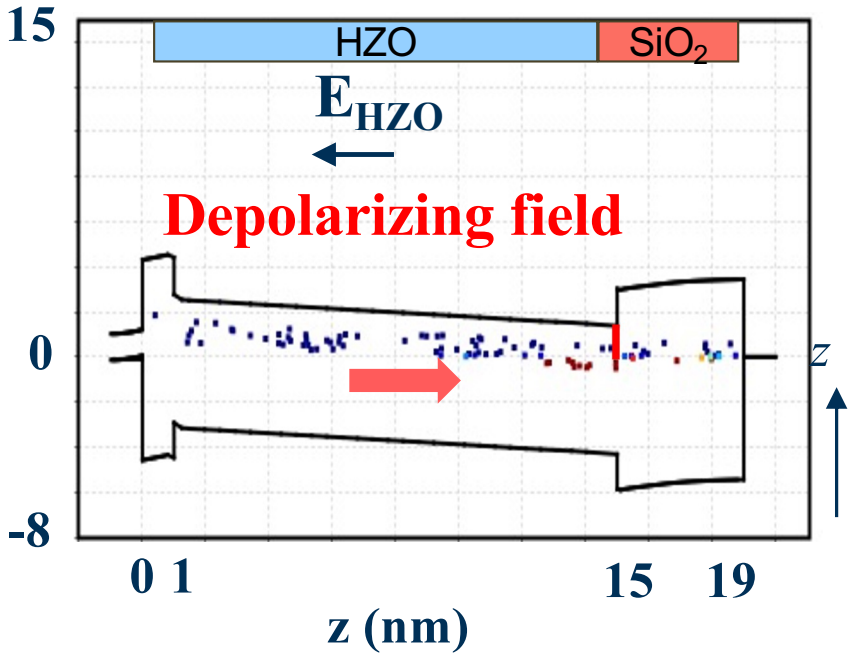
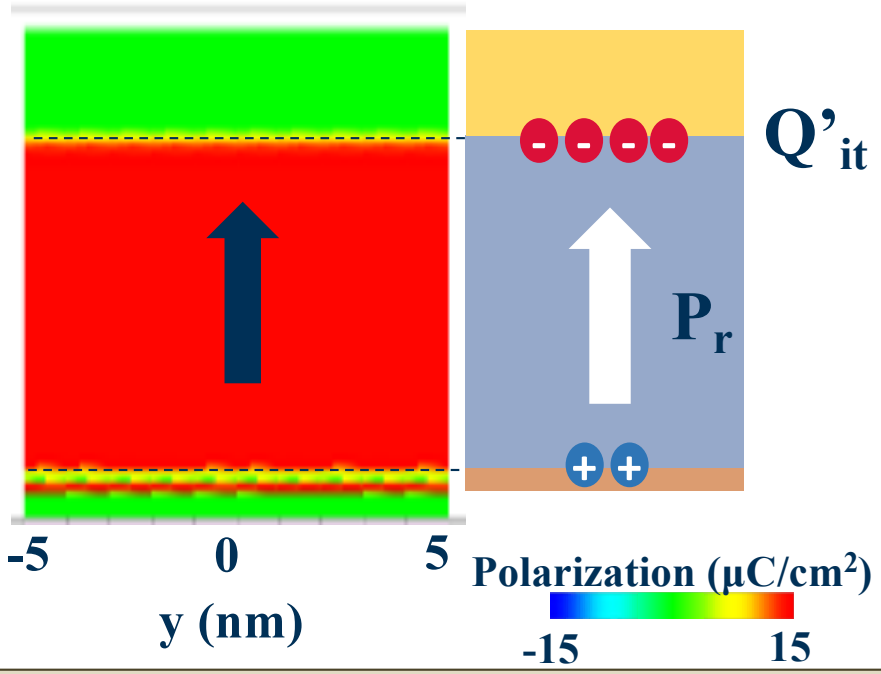
GBL Retention loss



B, t1

$P_r > Q'_{it}$

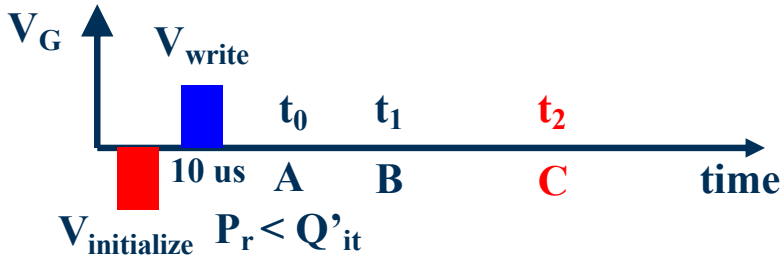




When Q'_{it} reduces below P_r, the field in the ferroelectric layer becomes depolarizing.

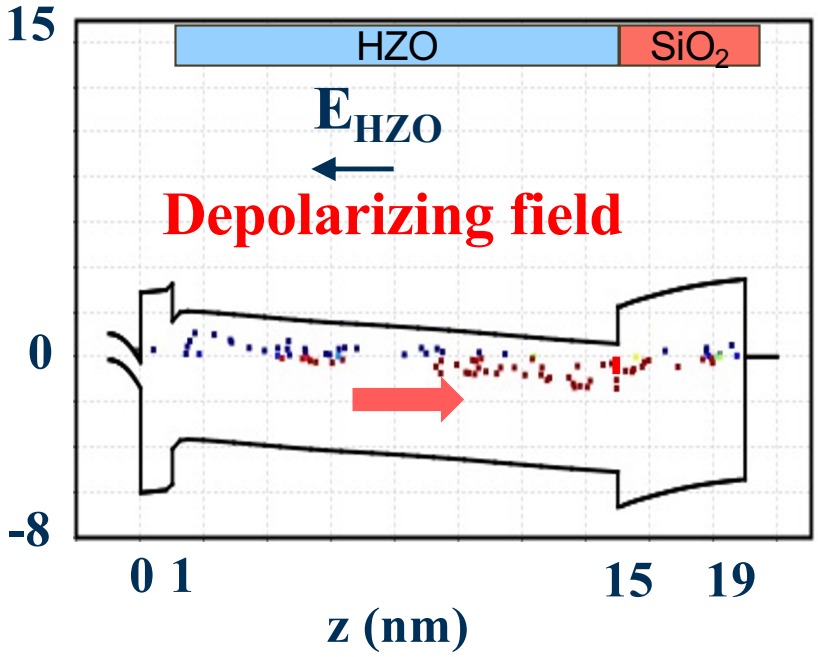
Venkatesan, P., et al. IRPS 2025

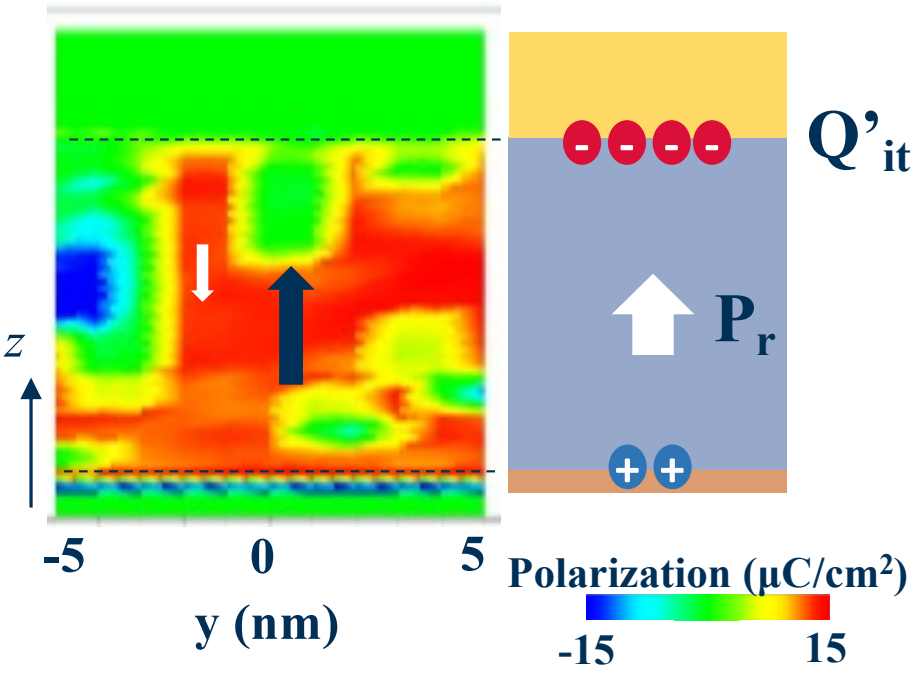
GBL Retention loss



C, t2 > t1

$P_r > Q'_{it}$

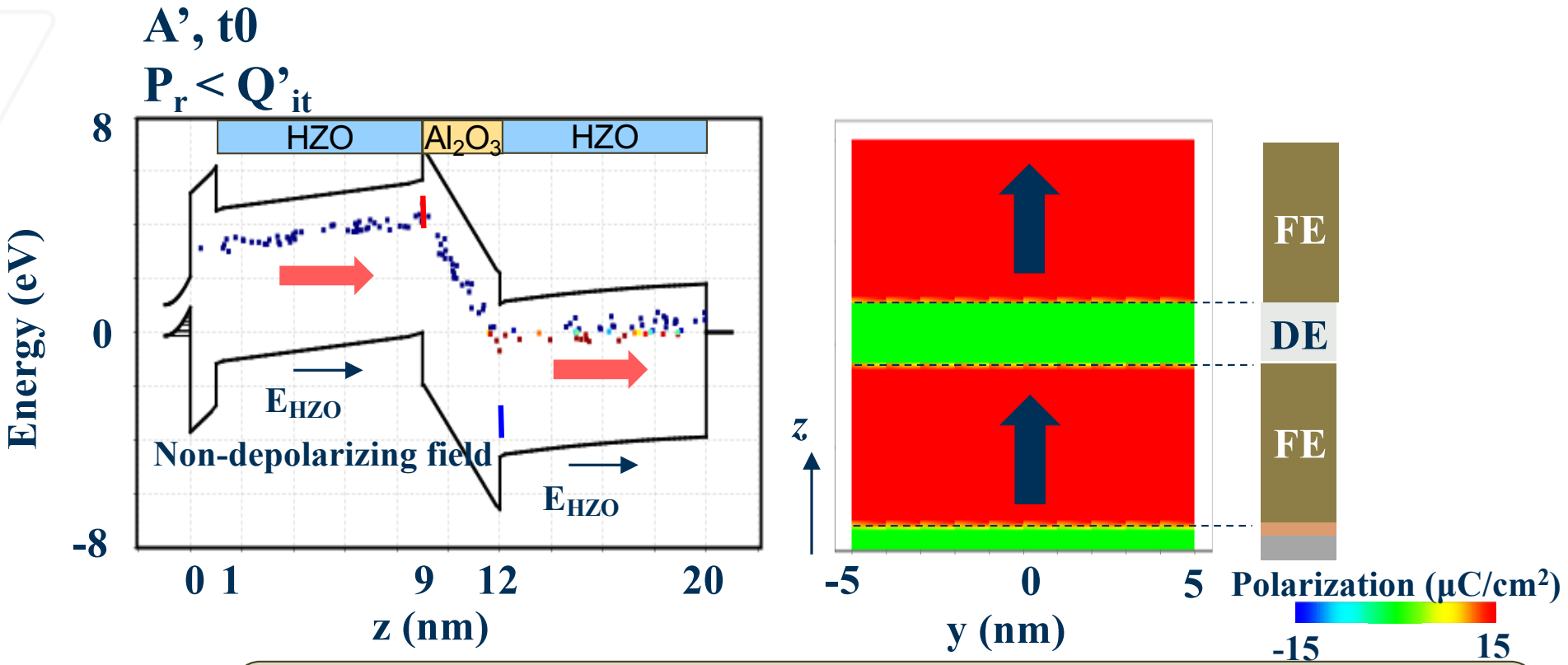




Venkatesan, P., et al.
IRPS 2025

This combination of detrapping of MW enhancing charges and depolarization of ferroelectric layer leads to retention loss

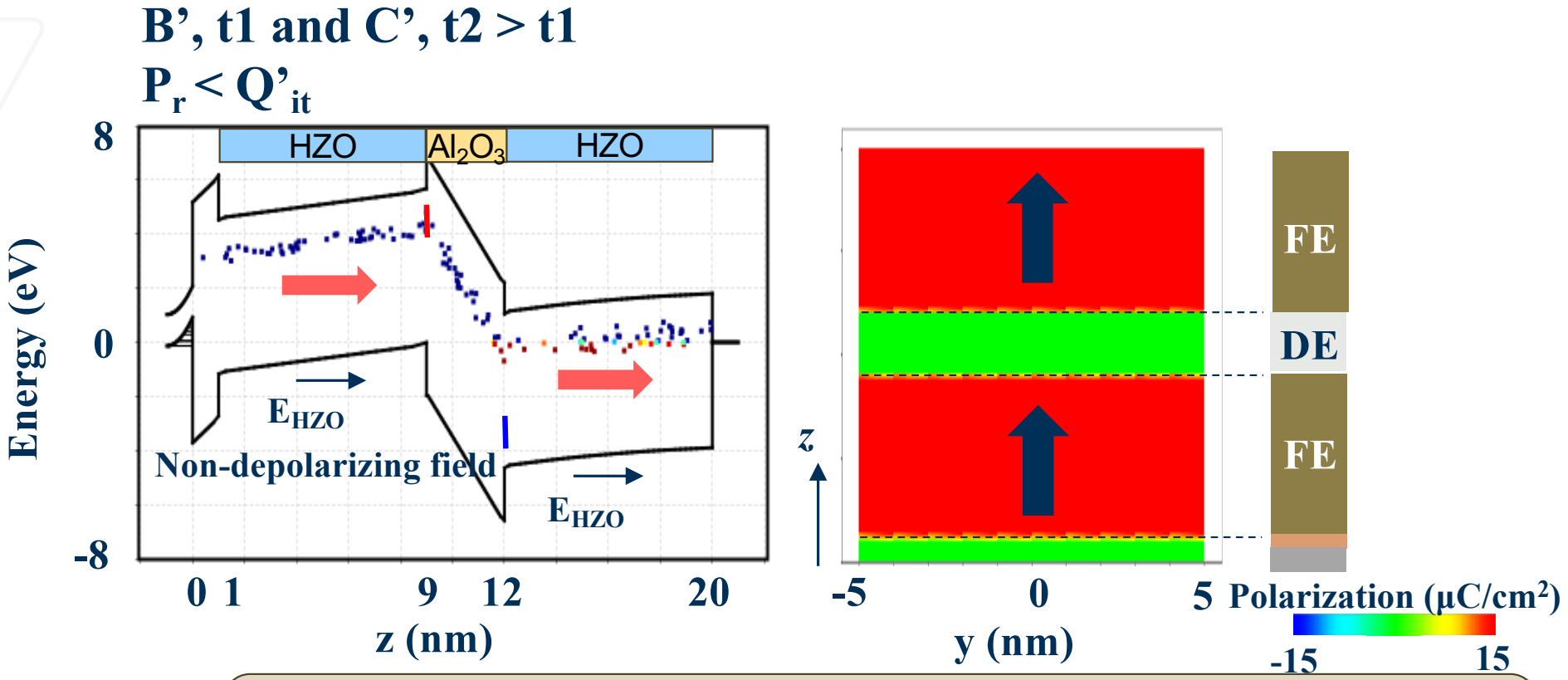
TDL Retention loss



The overcompensated charge density at the FE-TDL interface, protected by the FE layers, maintains the non-depolarizing field across the FE, leading to robust retention.

Venkatesan, P., et al.
IRPS 2025

TDL Retention loss



The overcompensated charge density at the FE-TDL interface, protected by the FE layers, maintains the non-depolarizing field across the FE, leading to robust retention.

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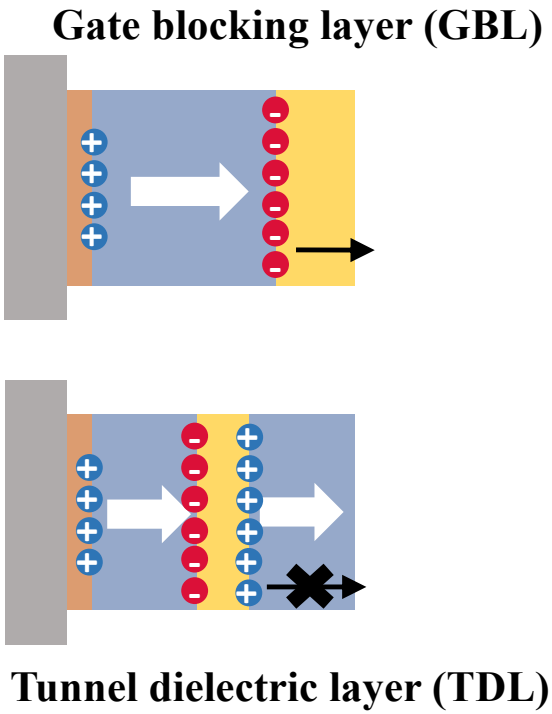
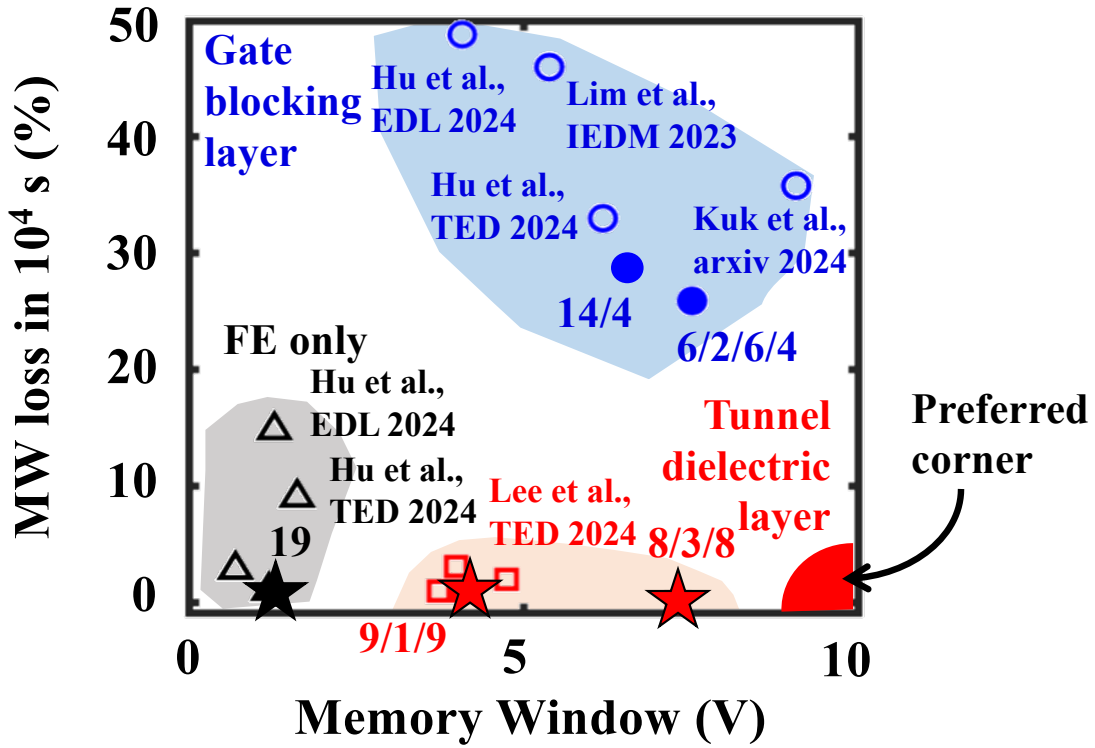
Retention benchmark





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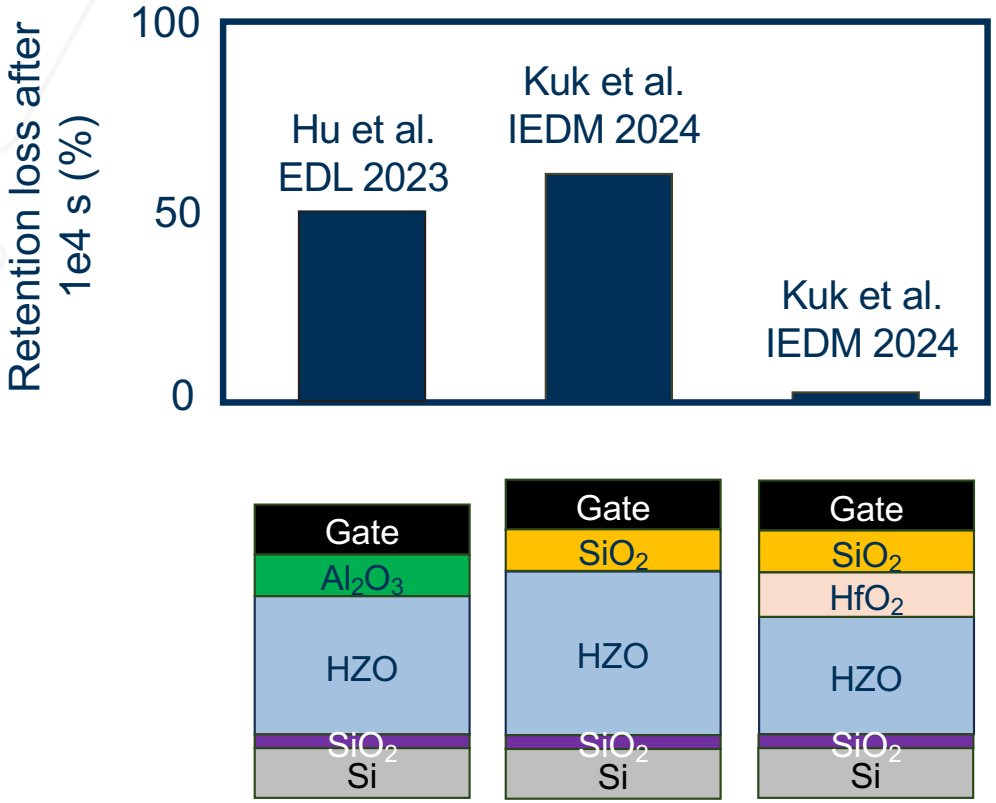
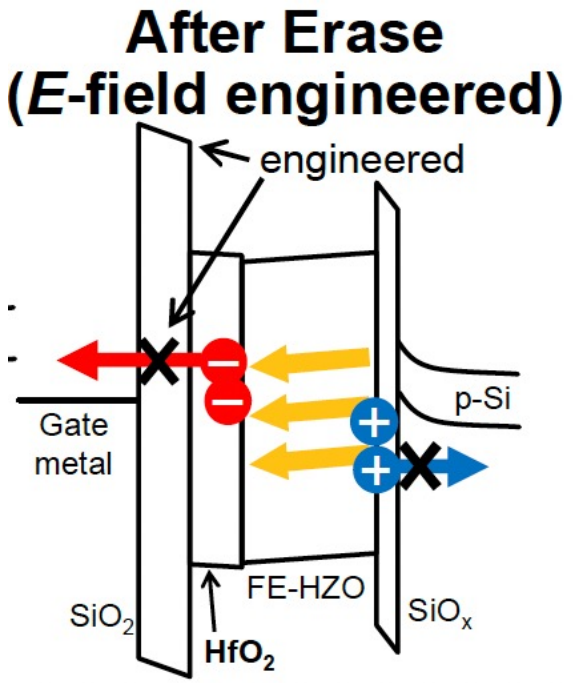
IRPS 2025

Moving the dielectric to the middle of the FE gate stack, energetically stabilizes the MW.

Solving retention degradation in GBL FE-NAND





Kuk et al.
IEDM 2024

What about reliability of ferroelectric NAND?

1. Retention
2. Disturb
3. Write endurance
4. Lateral charge migration
5. Device-device variation

What about reliability of ferroelectric NAND?

Performance

Memory window

Device Reliability

Retention

Disturb

Write Endurance

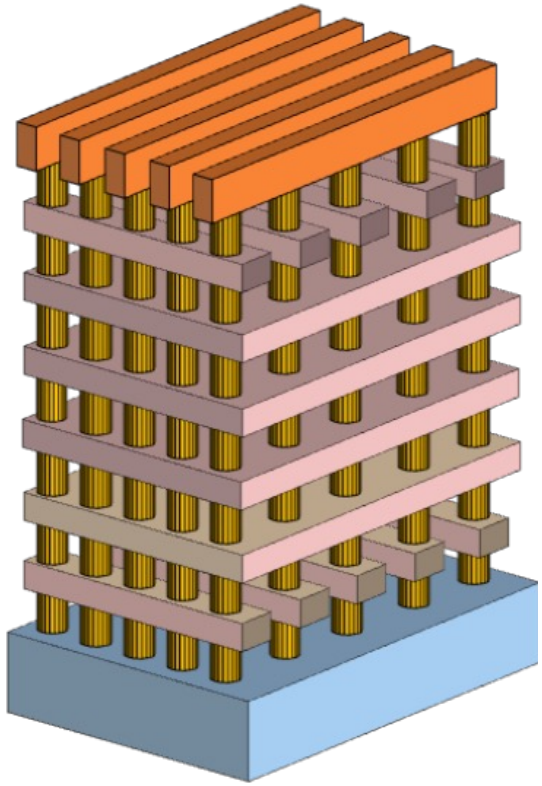
Array-level Reliability

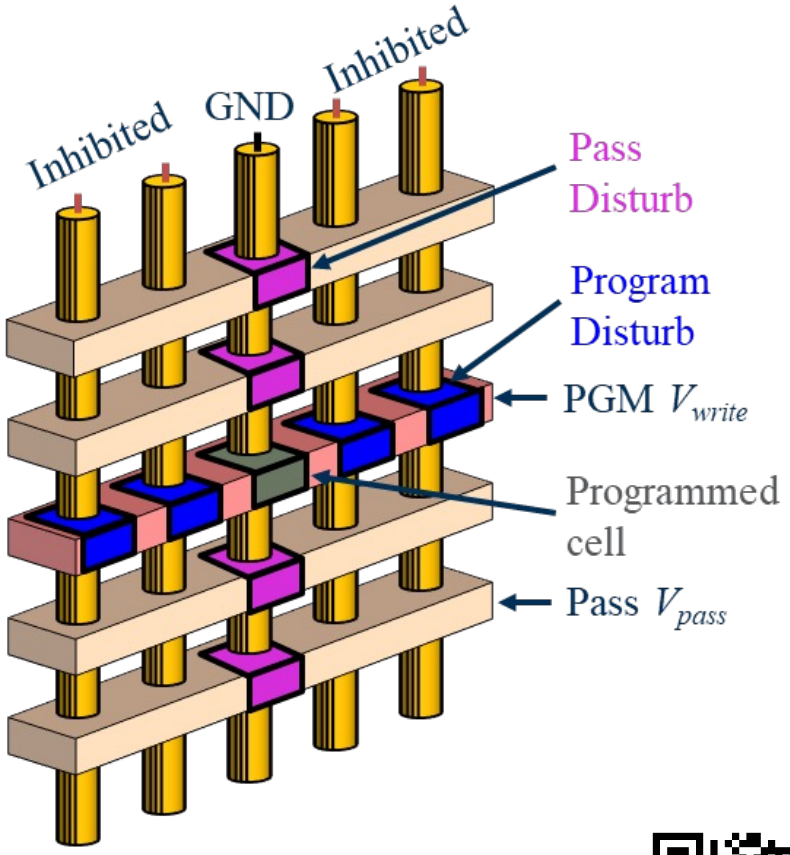
Lateral charge migration

Device-device variation

Georgia Tech

Disturb in Ferroelectric NAND

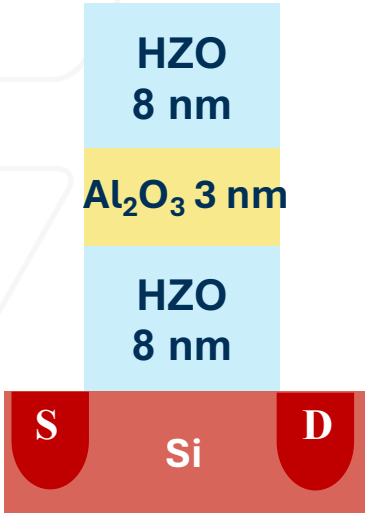


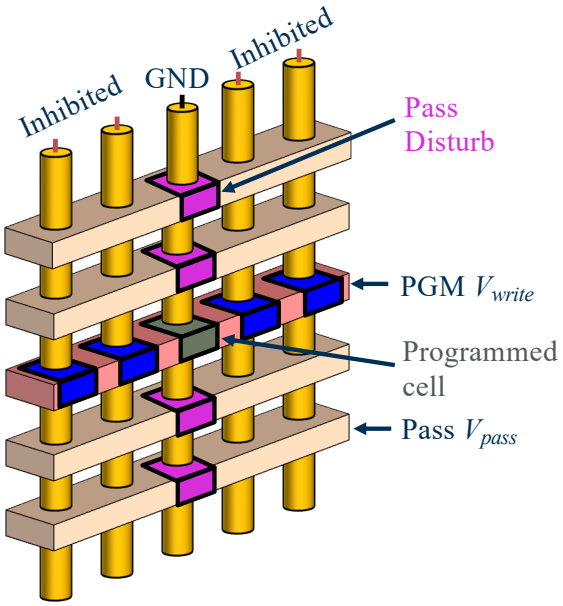


A pass voltage is applied to unaddressed cells while accessing a different cell along the bit line. This pass voltage could disturb the V_T of the cell either due to electron trapping or polarization back switching.

Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

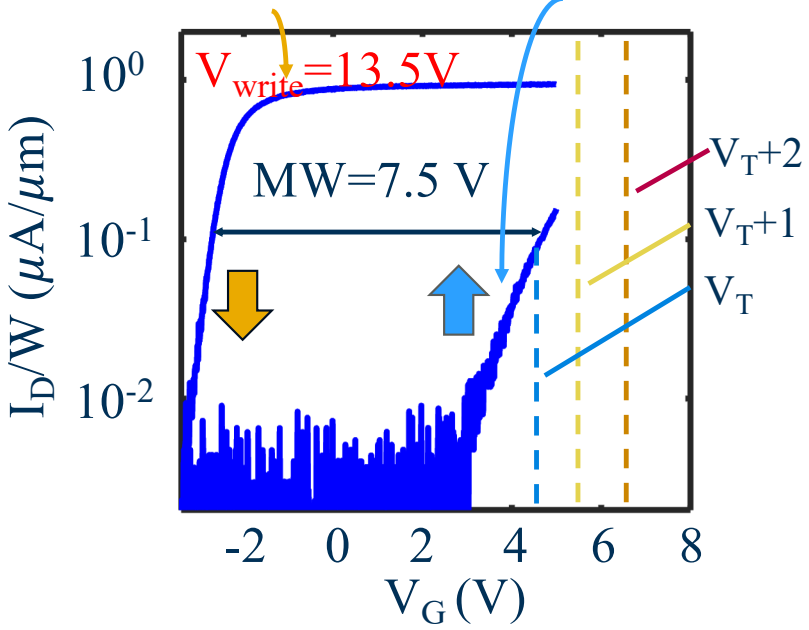
Disturb characterization





PGM state: possibility of electron trapping

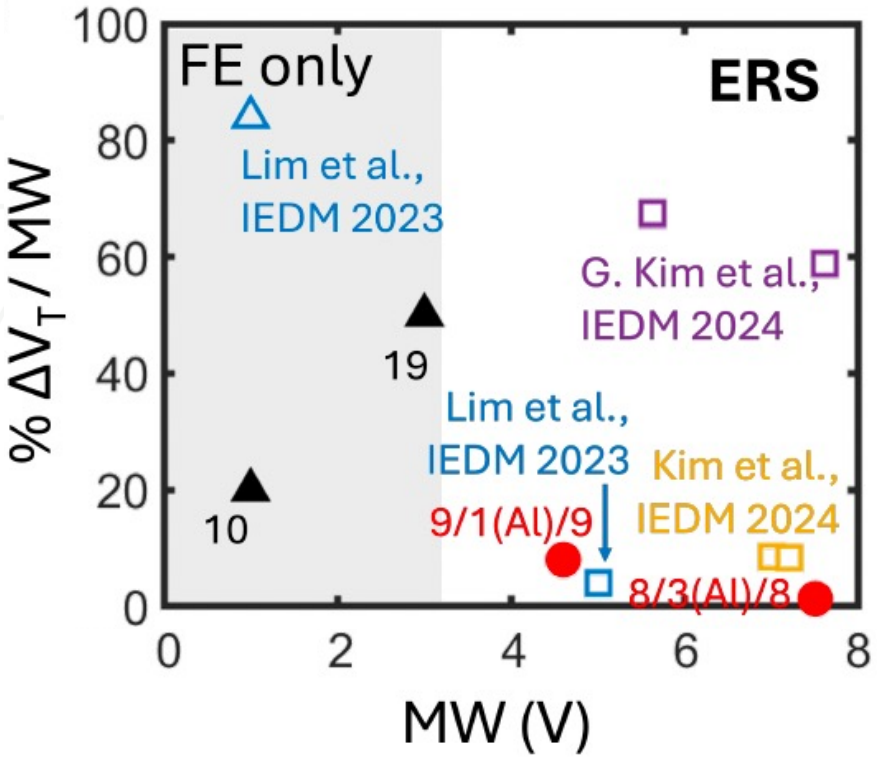
ERS state: possibility of polarization back flip

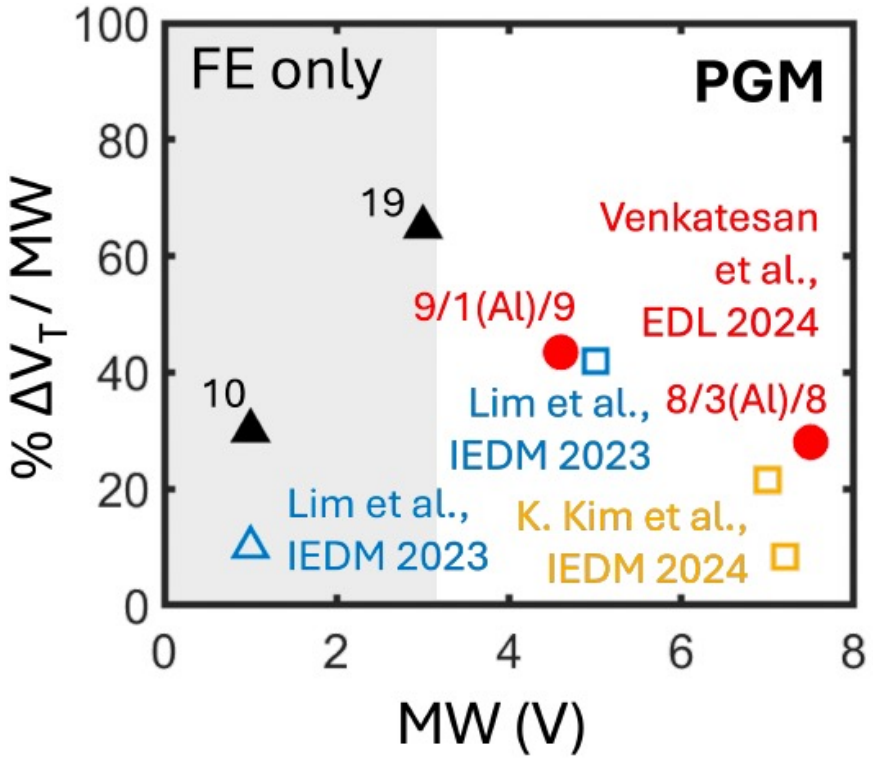


A pass voltage is applied to unaddressed cells while accessing a different cell along the bit line

Venkatesan, P., et al. EDL 2024: 10.1109/LED.2024.3467210

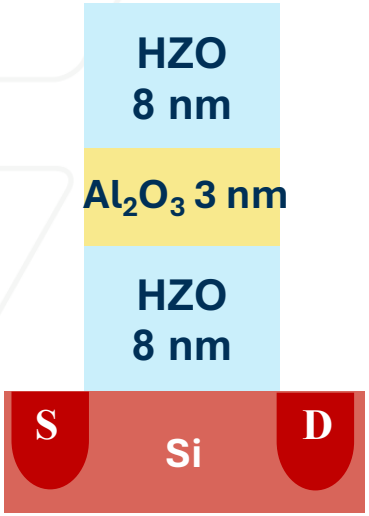
Pass disturb

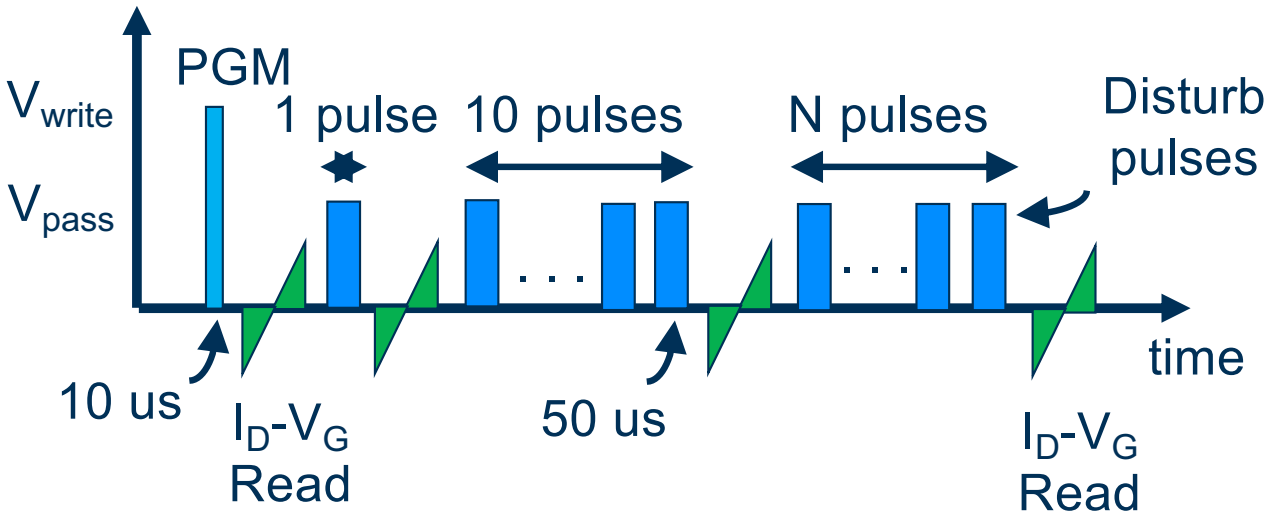




Georgia Tech

Disturb characterization





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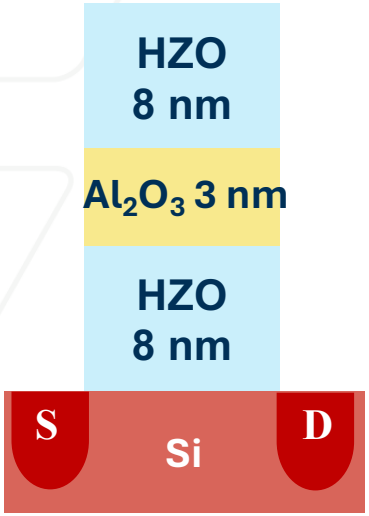
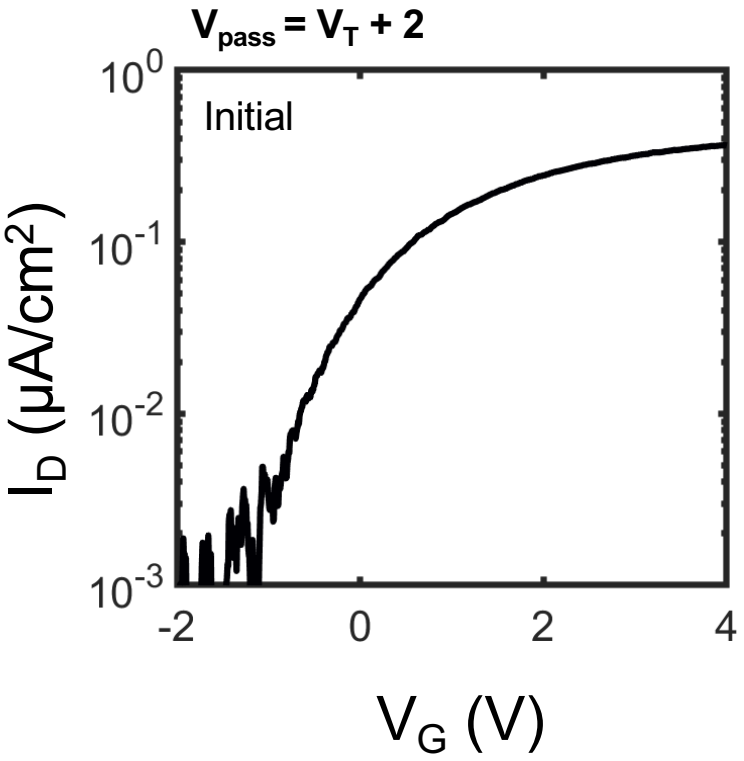
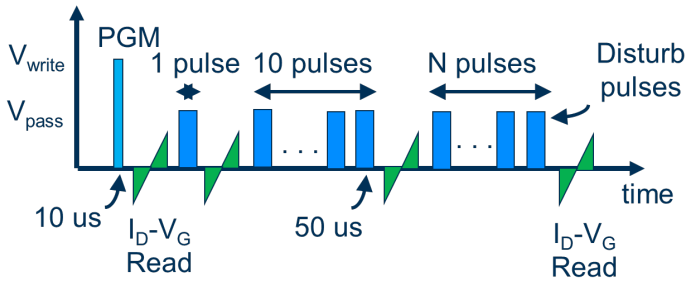
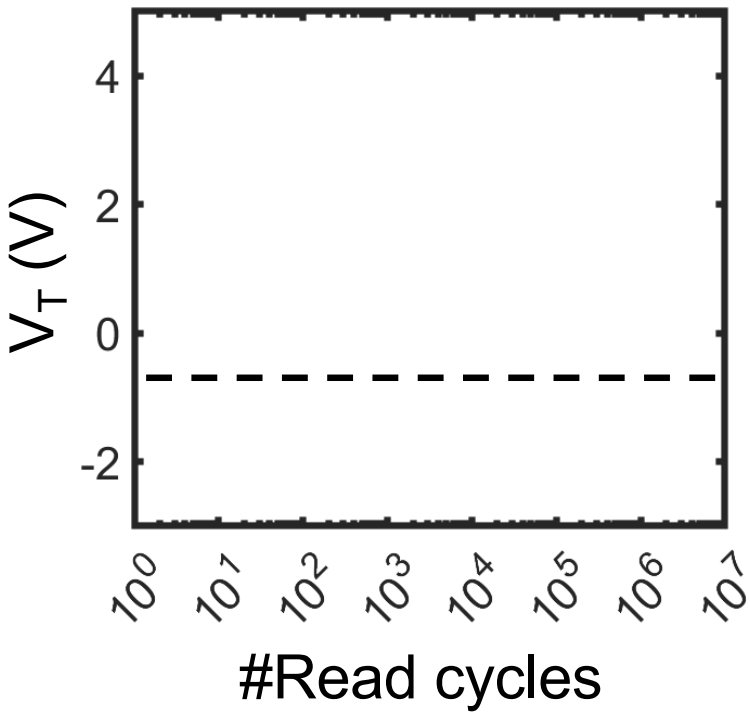
Disturb characterization









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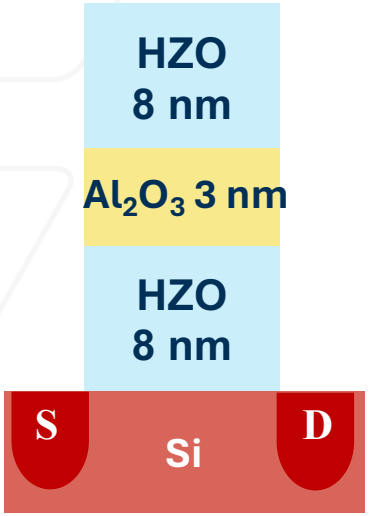
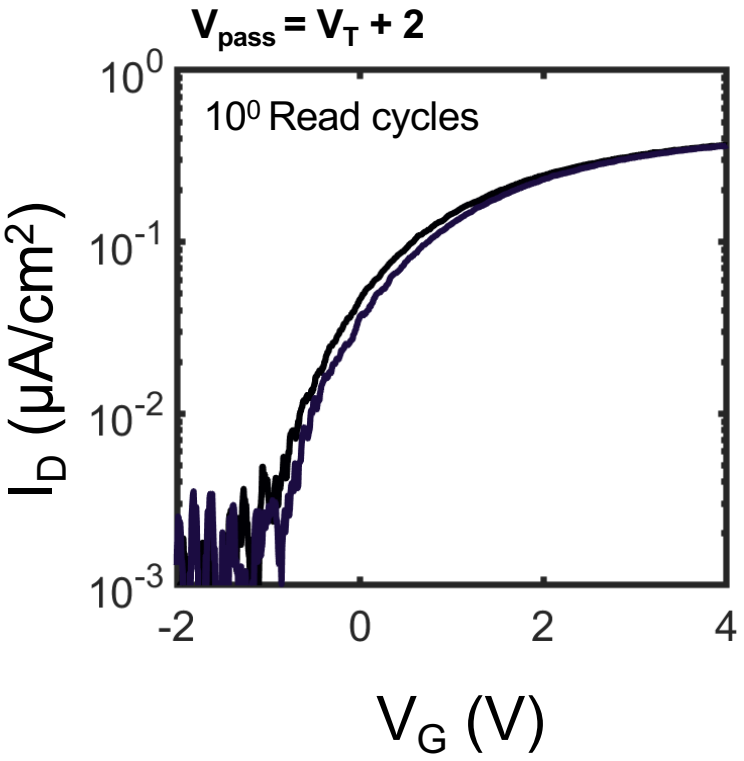
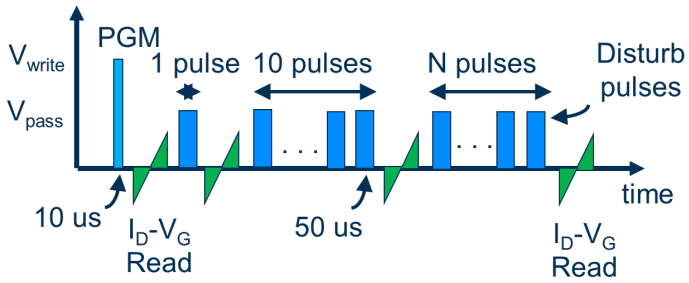
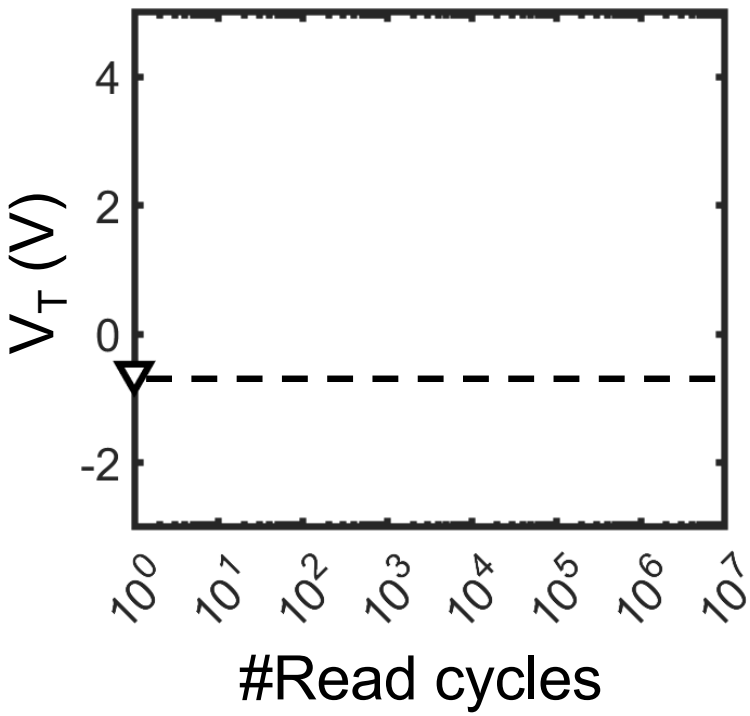
Disturb characterization



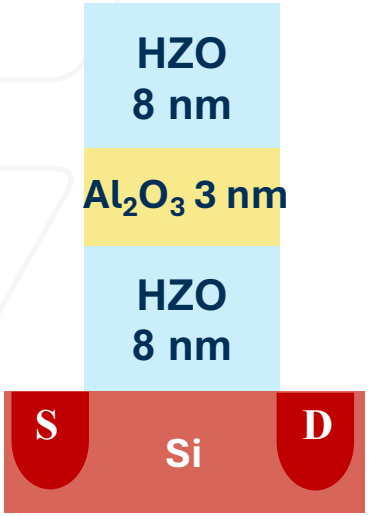


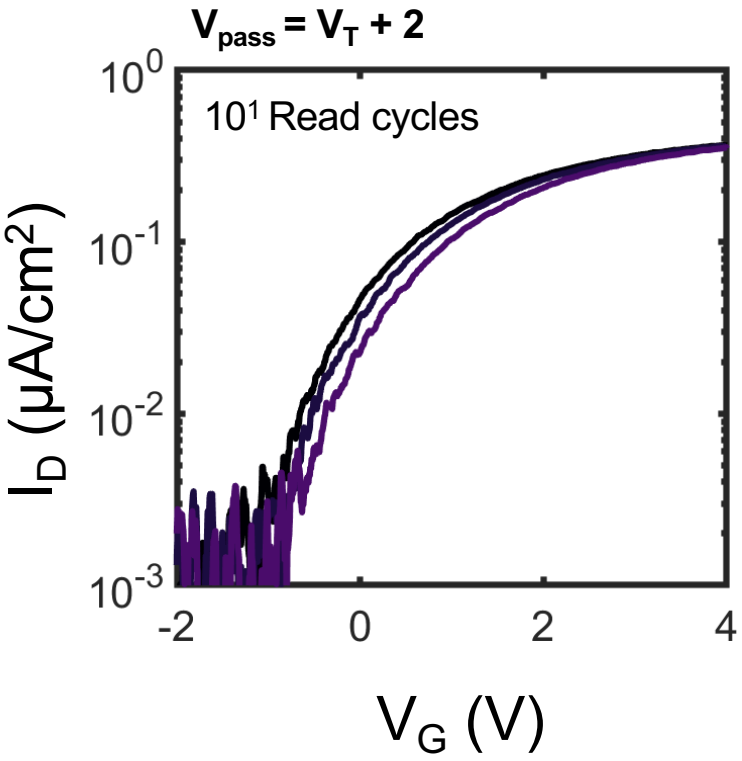


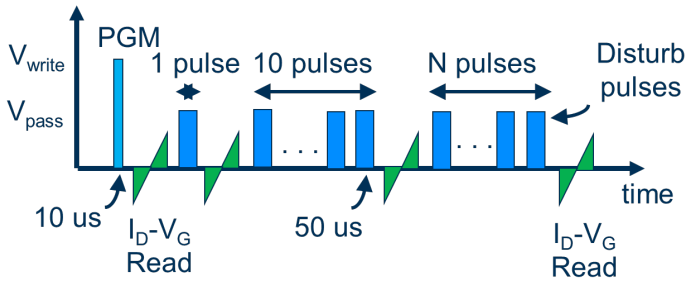


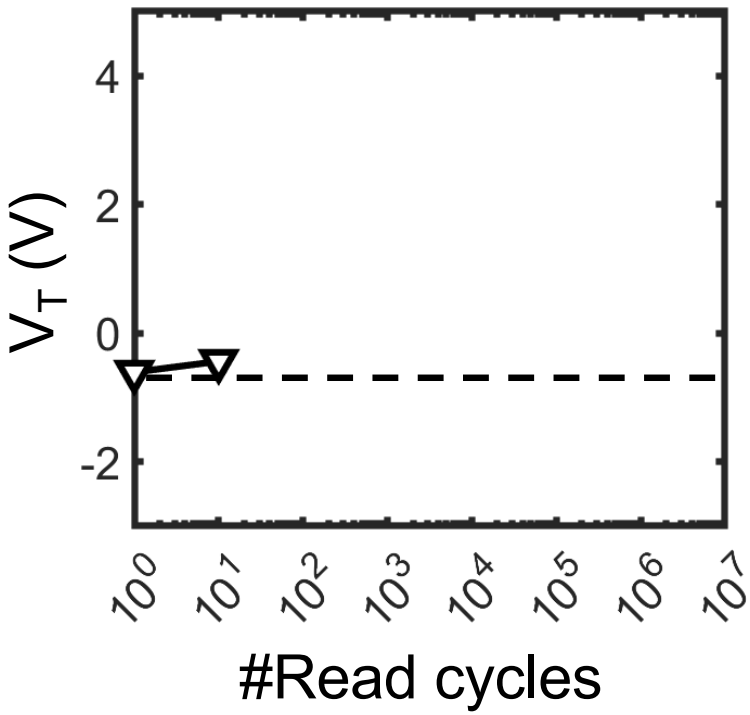
Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

Disturb characterization









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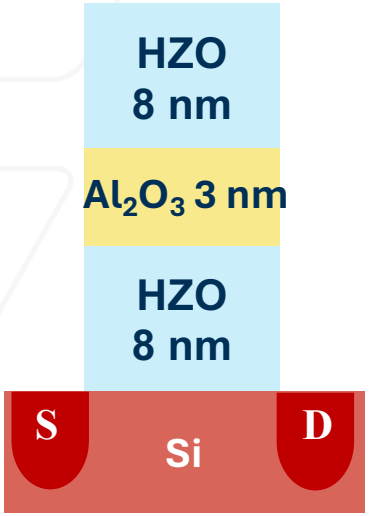

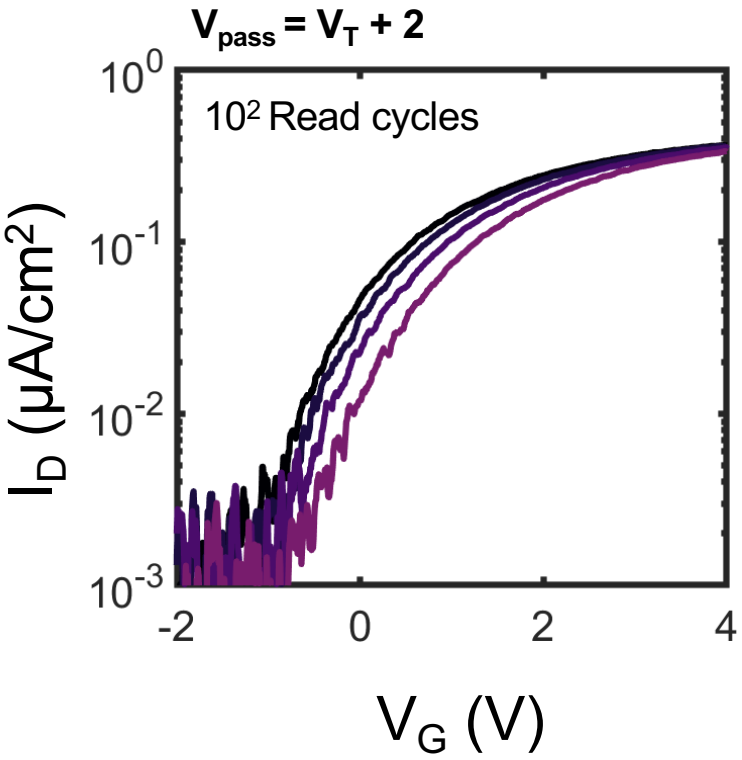

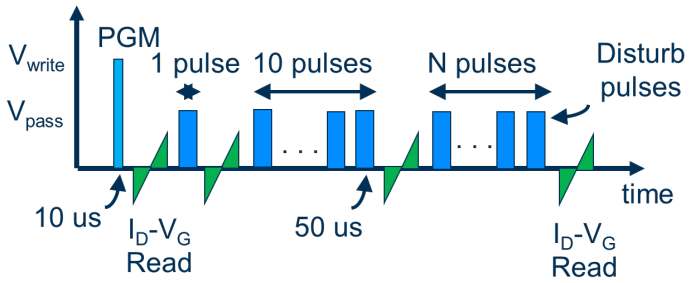

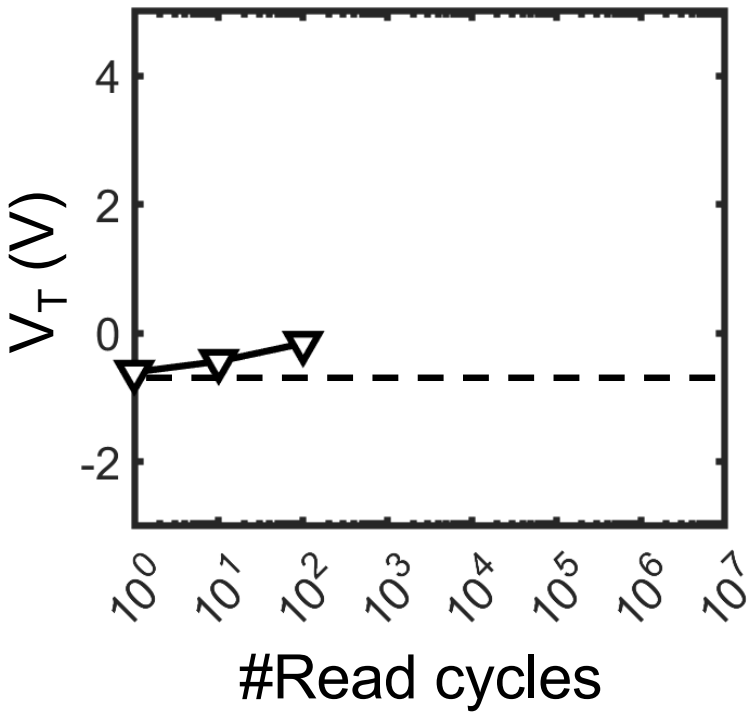

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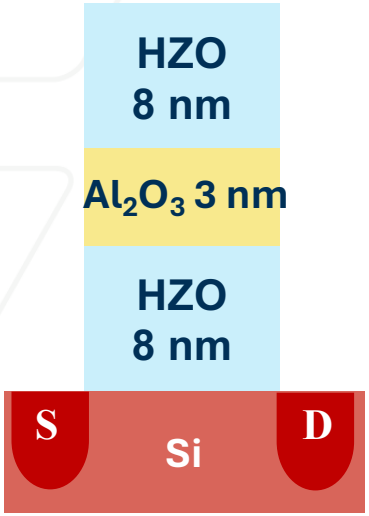
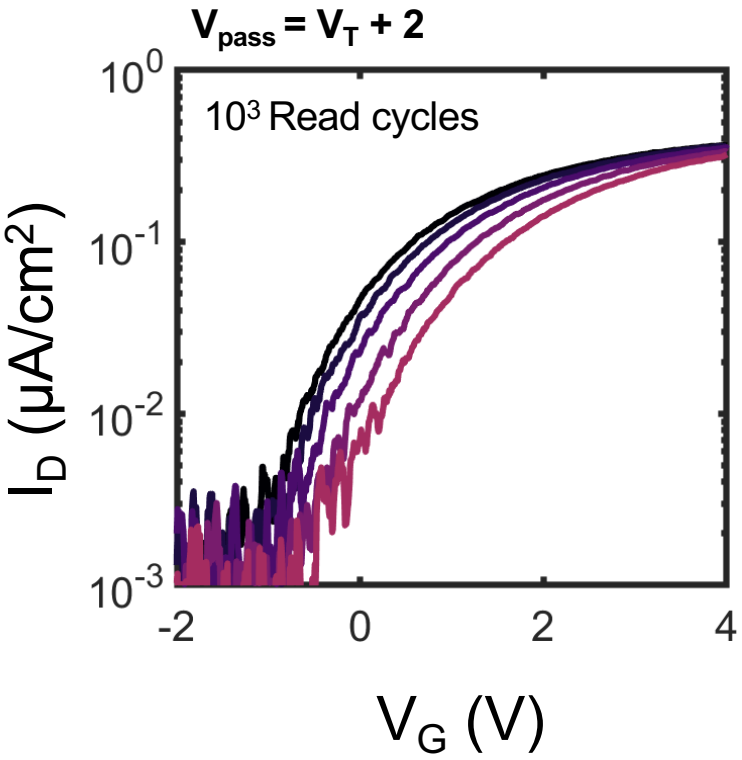
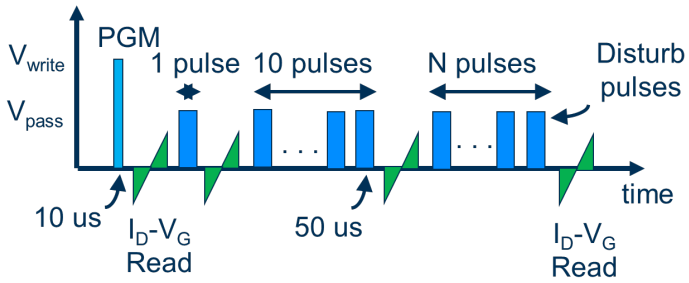
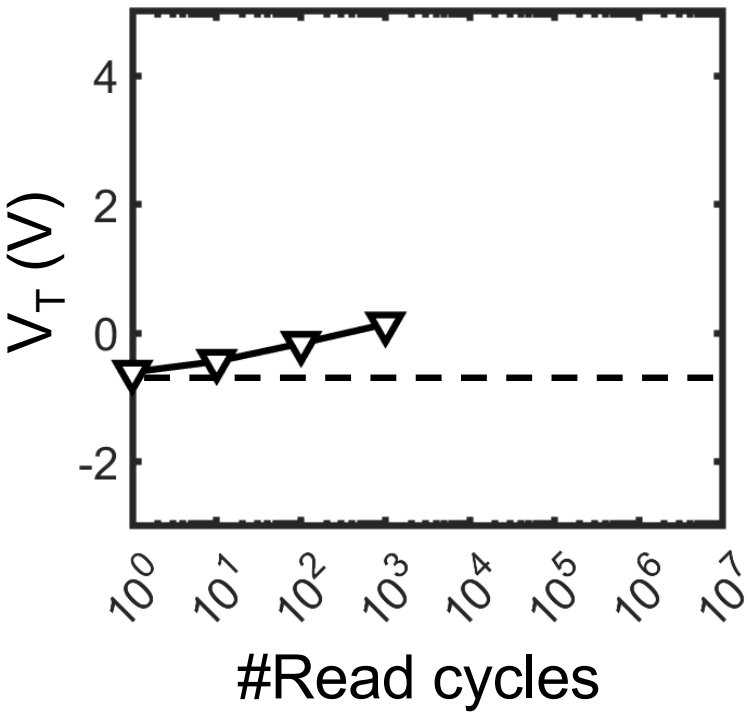
Disturb characterization



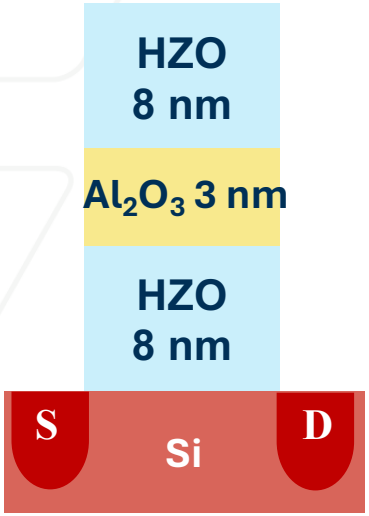


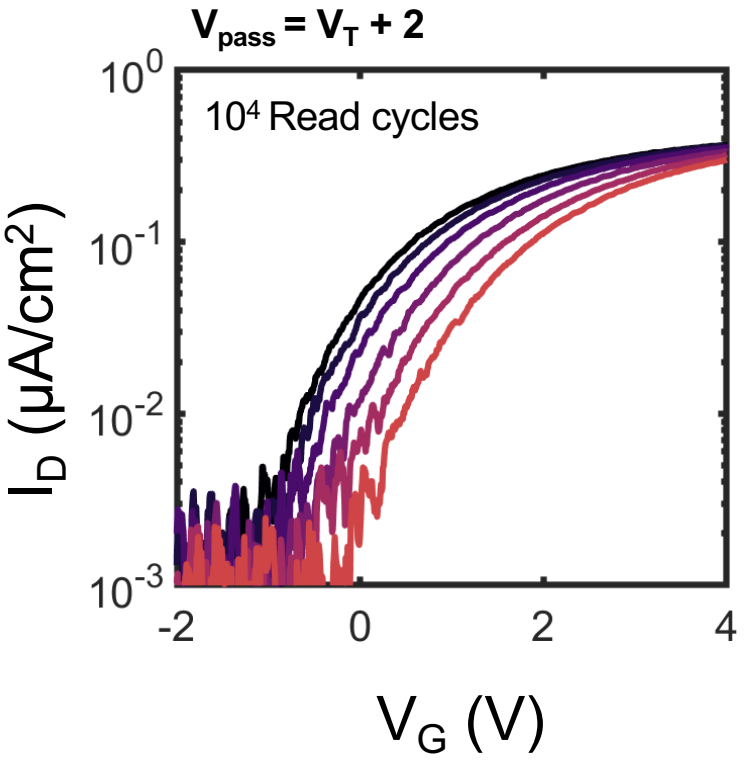


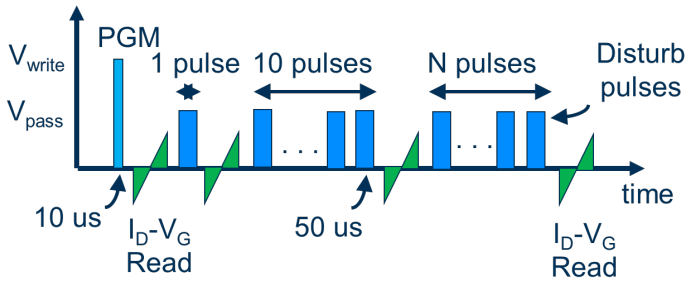


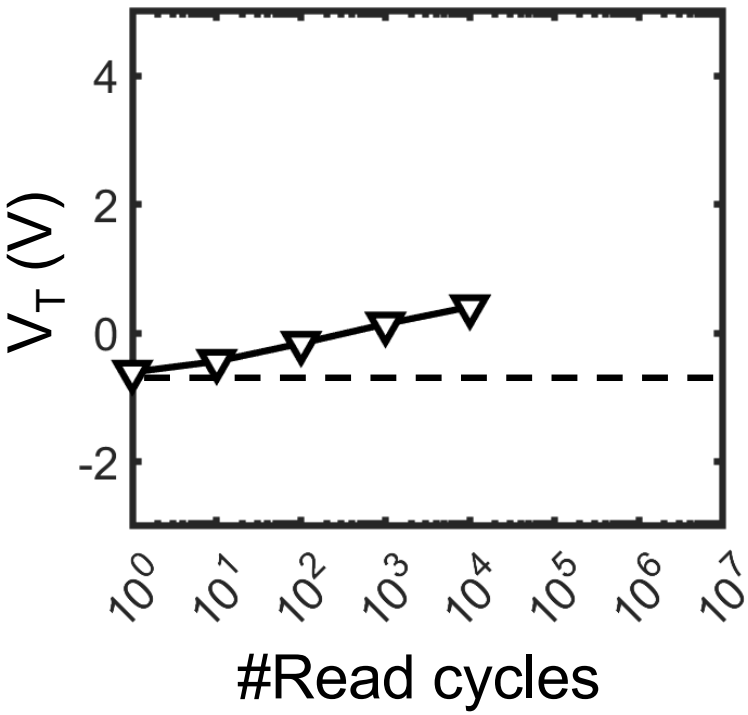
Venkatesan, P., et al. EDL 2024: 10.1109/LED.2024.3467210

Disturb characterization









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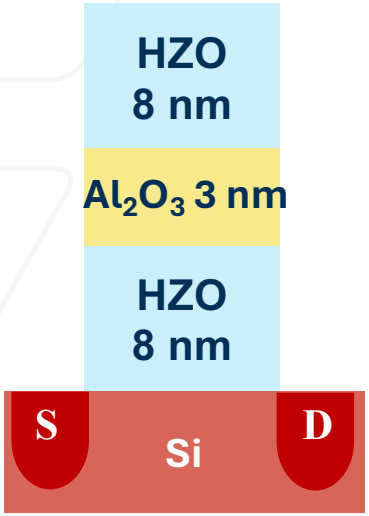
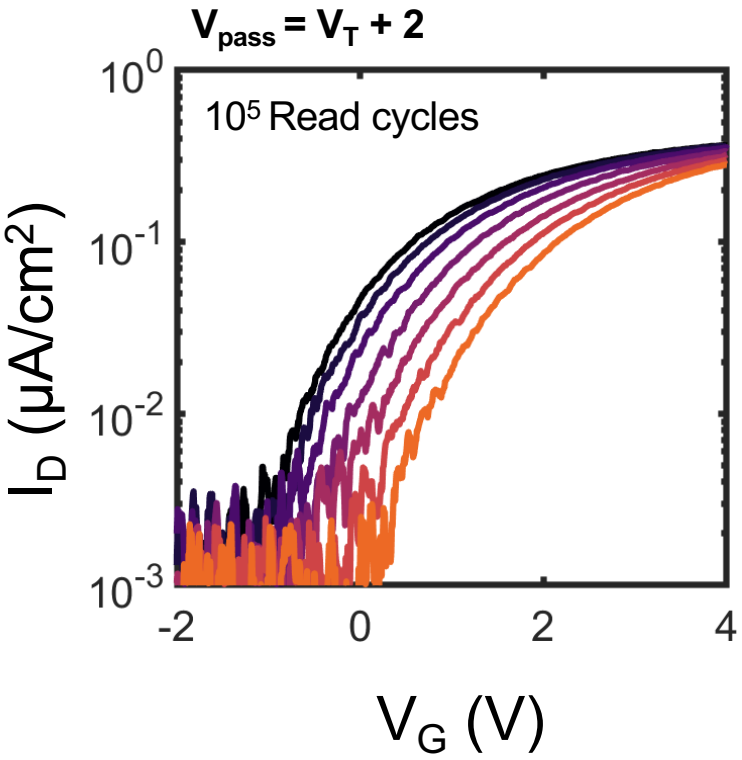
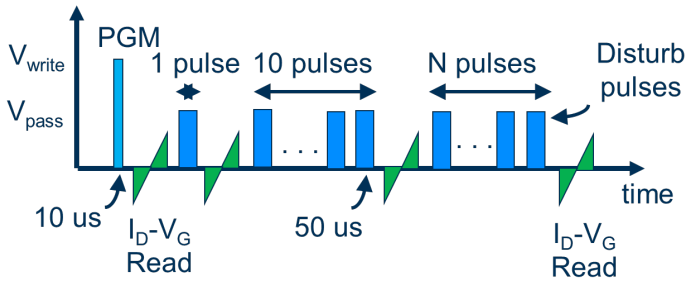
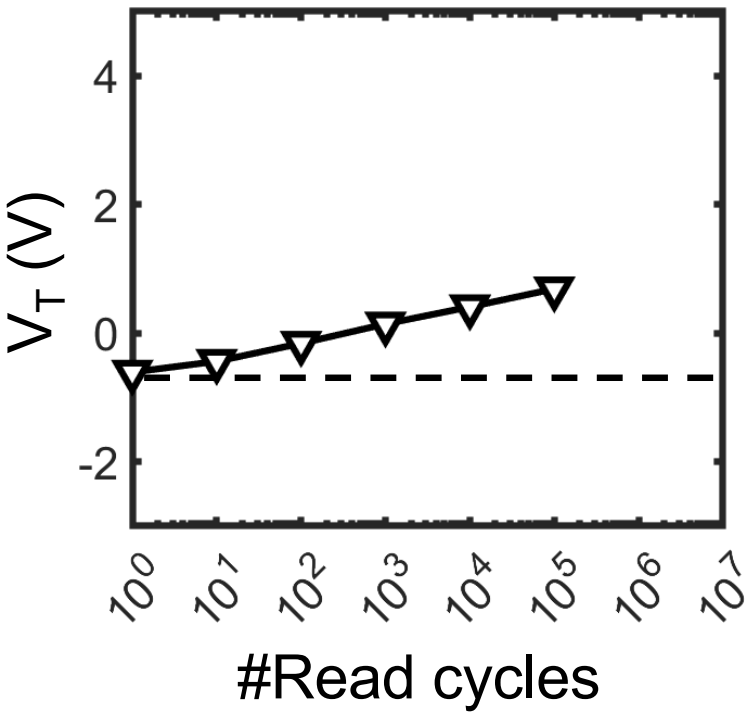
Disturb characterization









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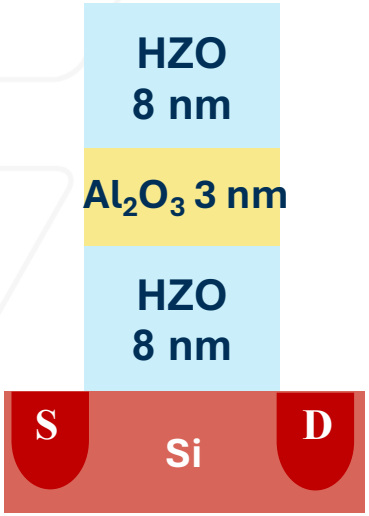
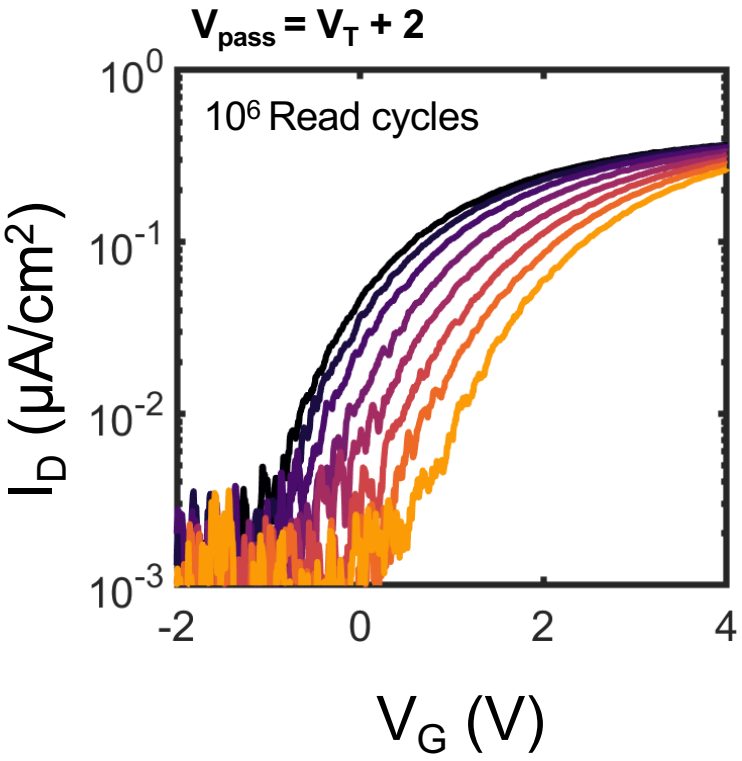
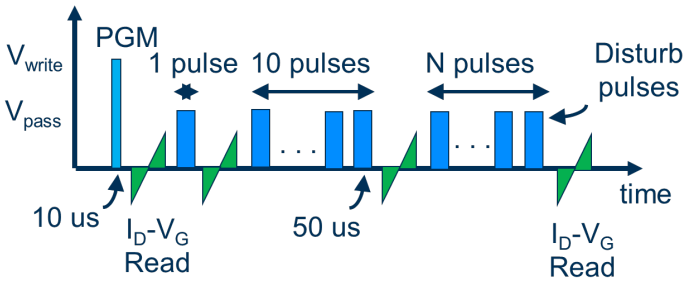
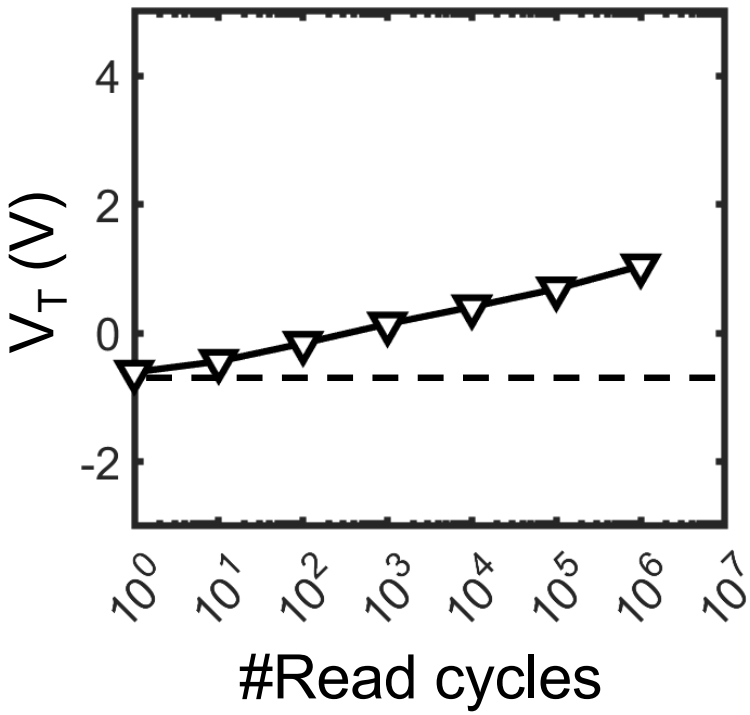
Disturb characterization









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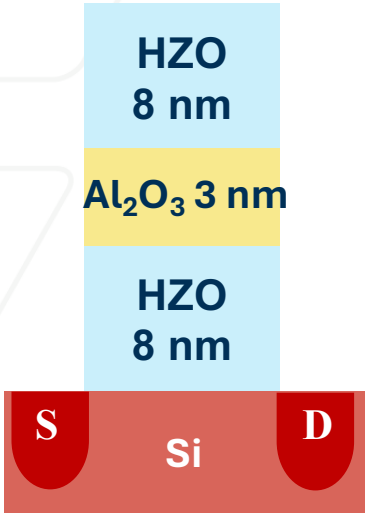
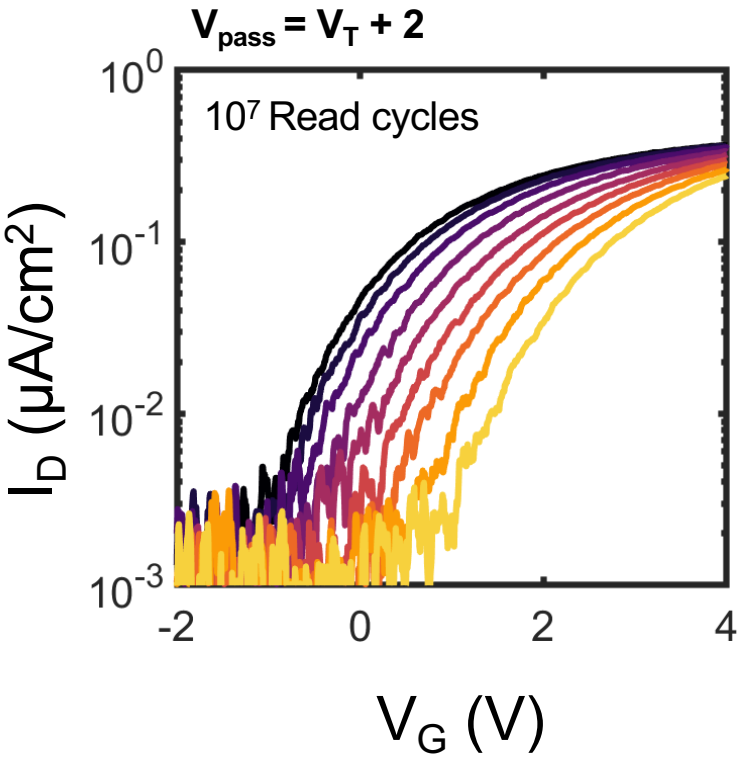
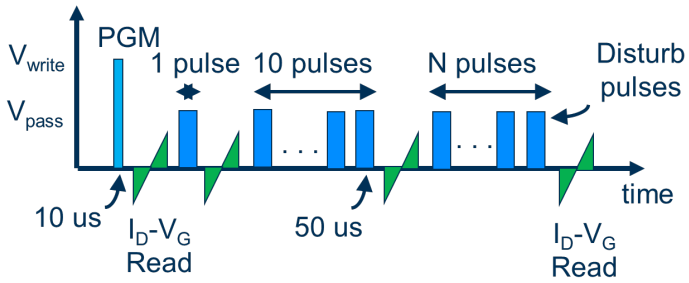
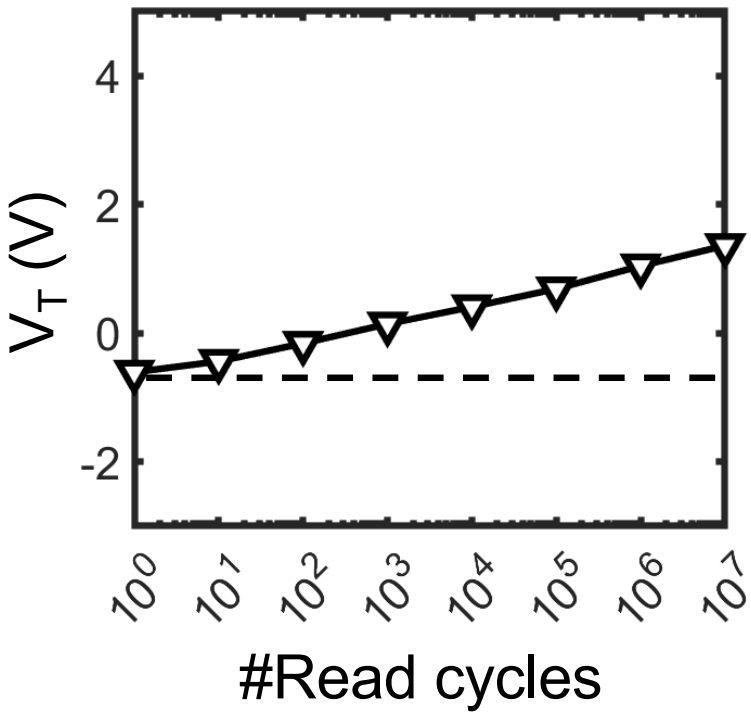
Disturb characterization



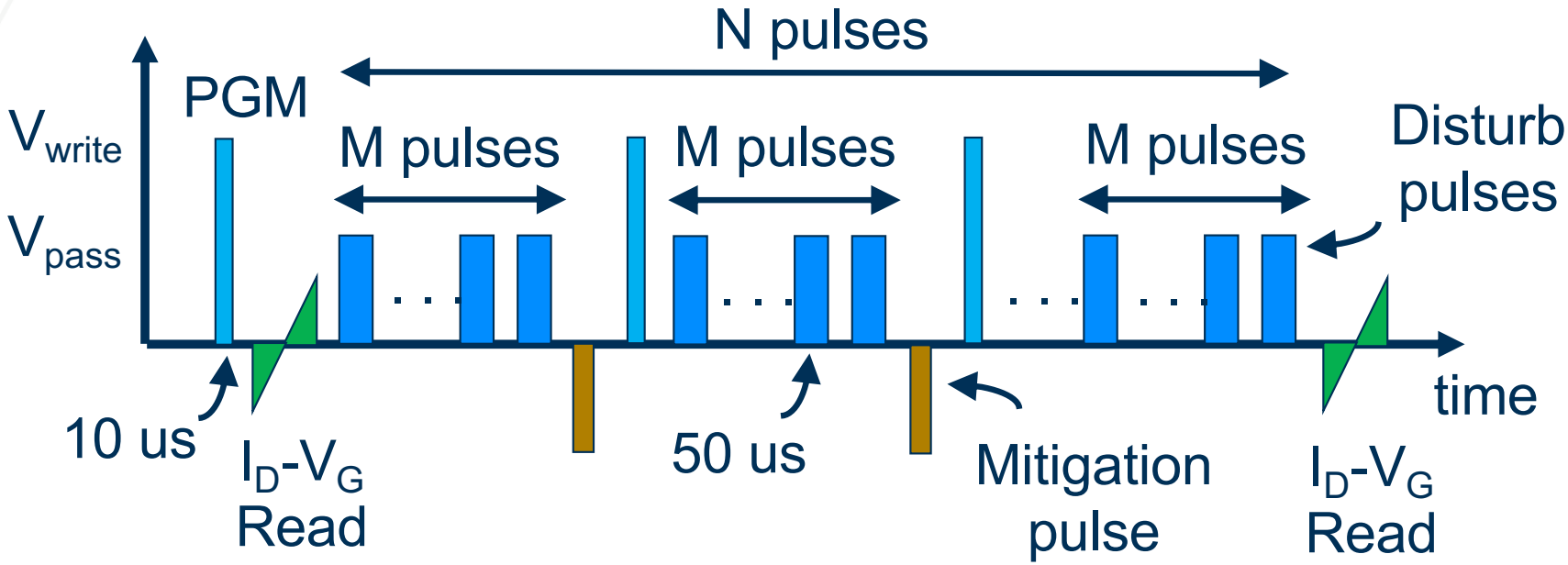






Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

Disturb mitigation



We introduce a mitigation pulse to detrap the electrons trapped due to the disturb pulses

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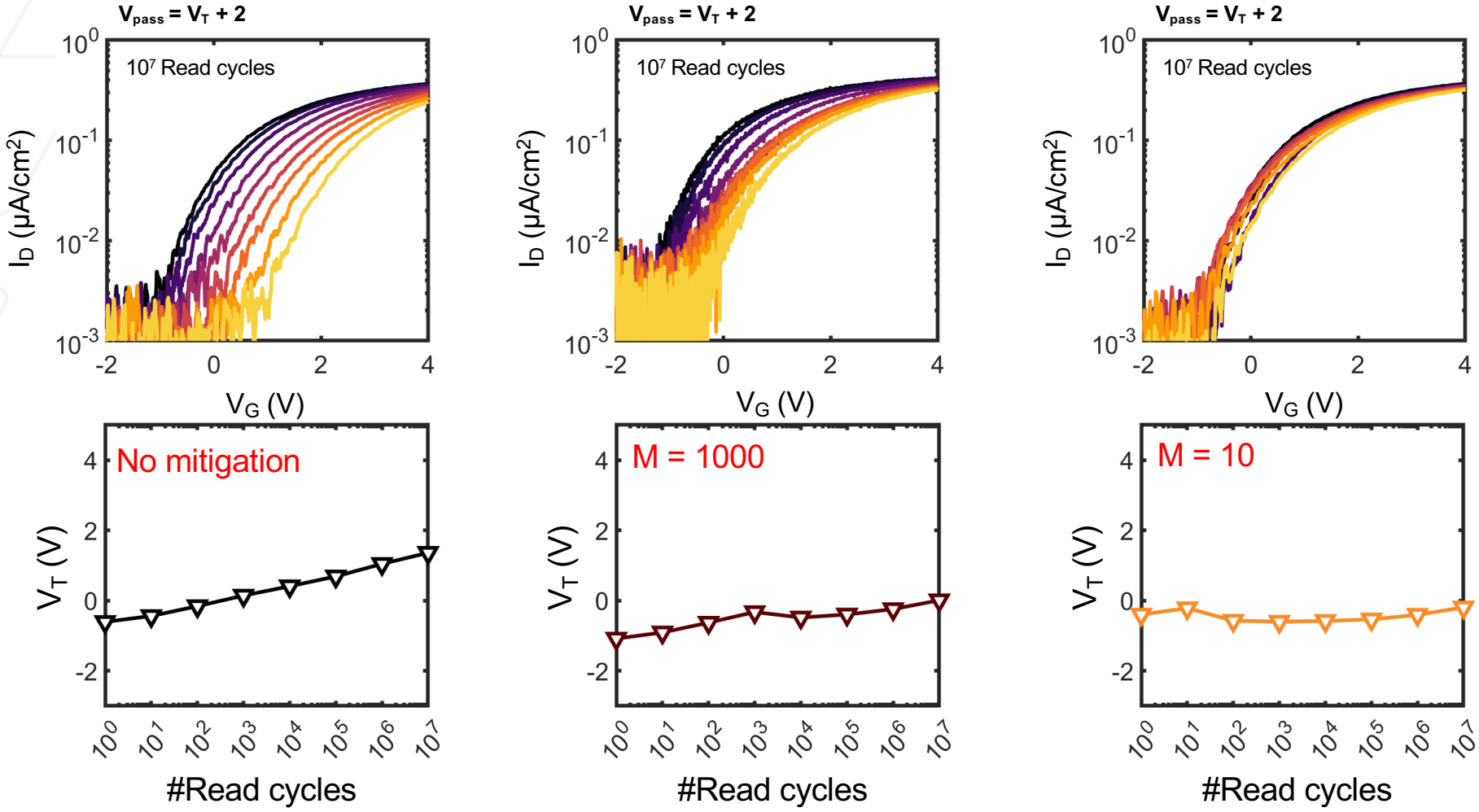
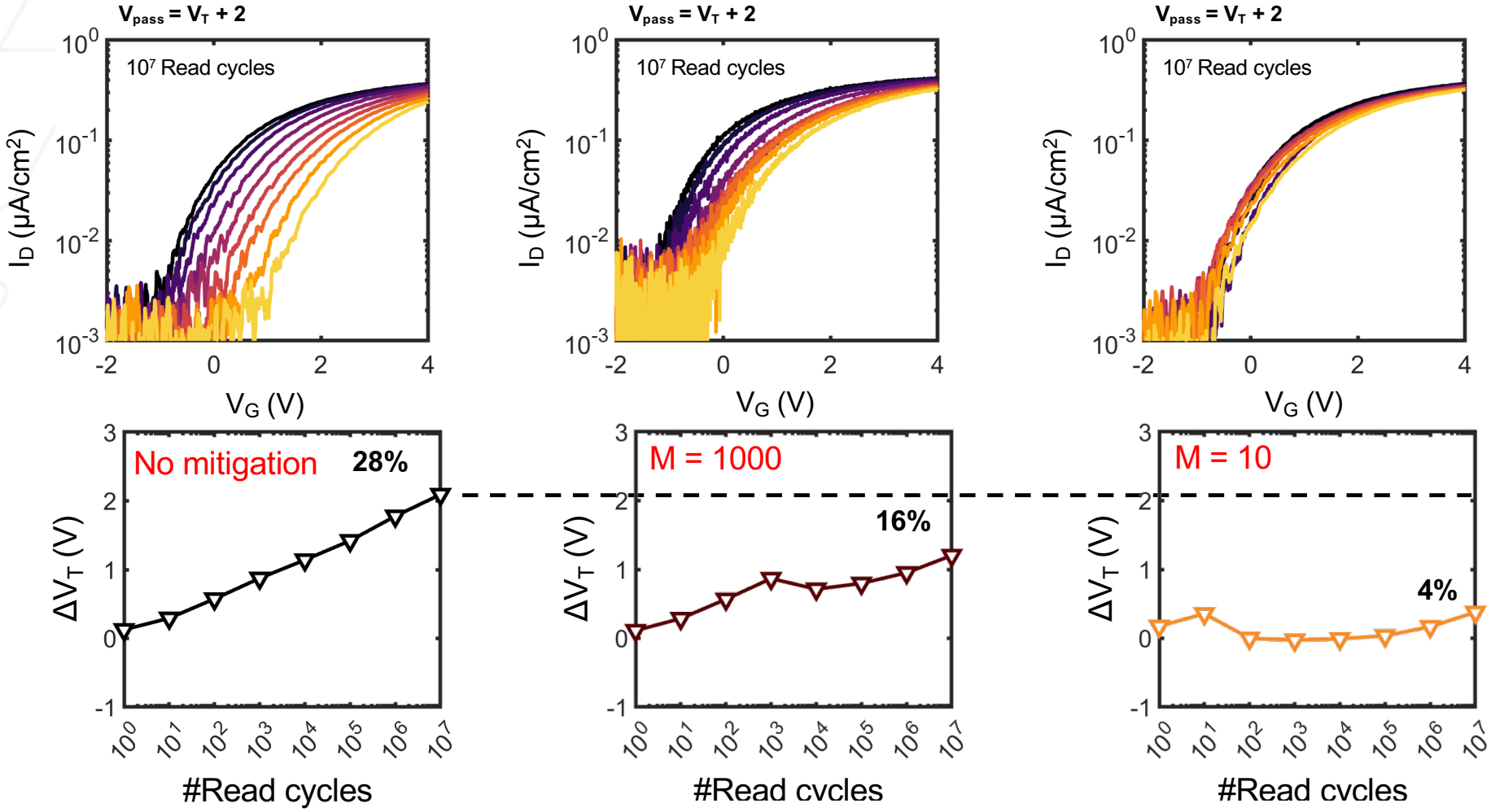
Disturb characterization



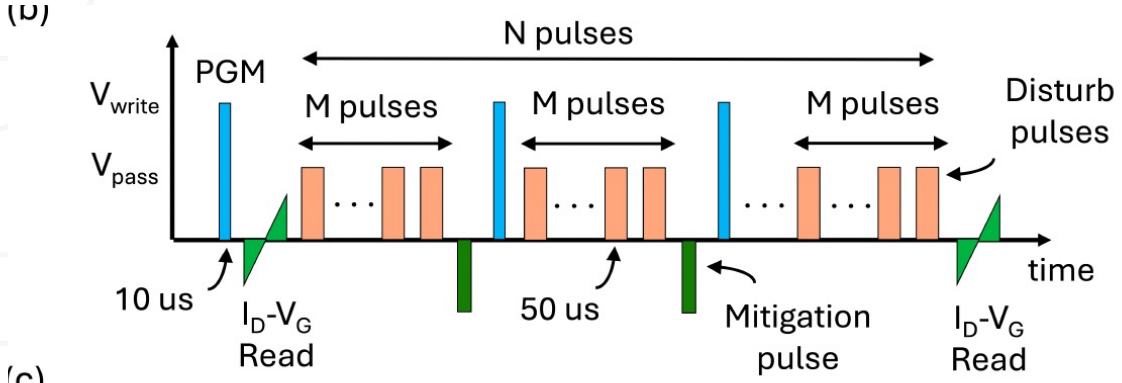
Venkatesan, P., et al. EDL 2024: 10.1109/LED.2024.3467210

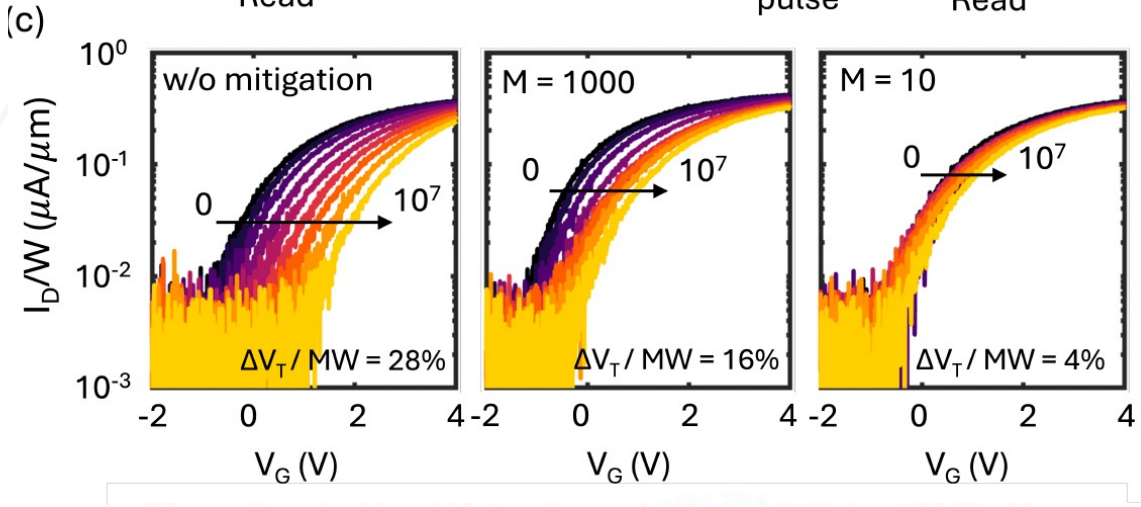
Disturb characterization

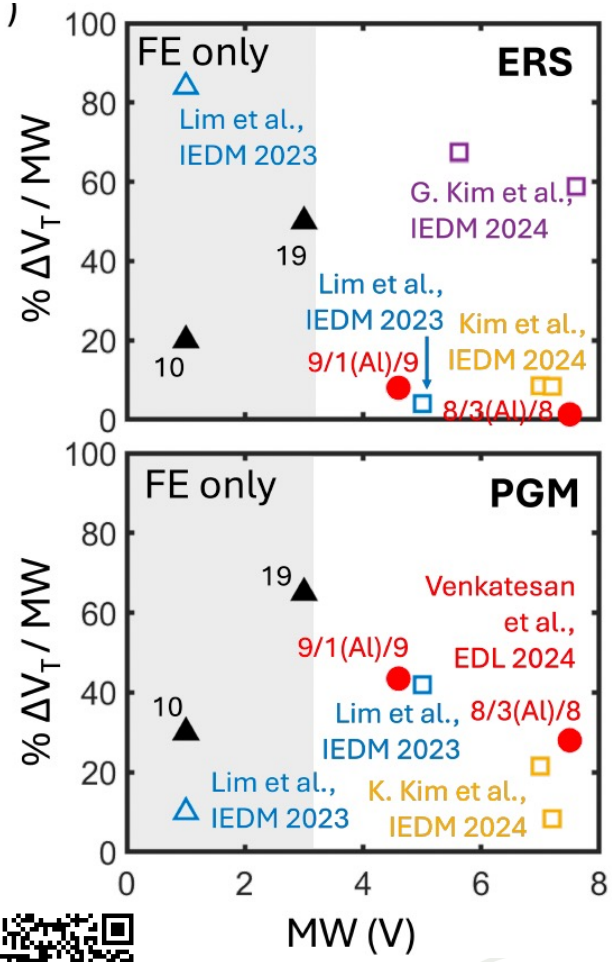


Venkatesan, P., et al. EDL 2024: [10.1109/LED.2024.3467210](https://doi.org/10.1109/LED.2024.3467210)

Summary of Pass disturb







Mitigation scheme reduces pass disturb down to 4%!!

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Georgia Tech

What about reliability of ferroelectric NAND?

Performance

Memory window

Device Reliability

Retention

Disturb

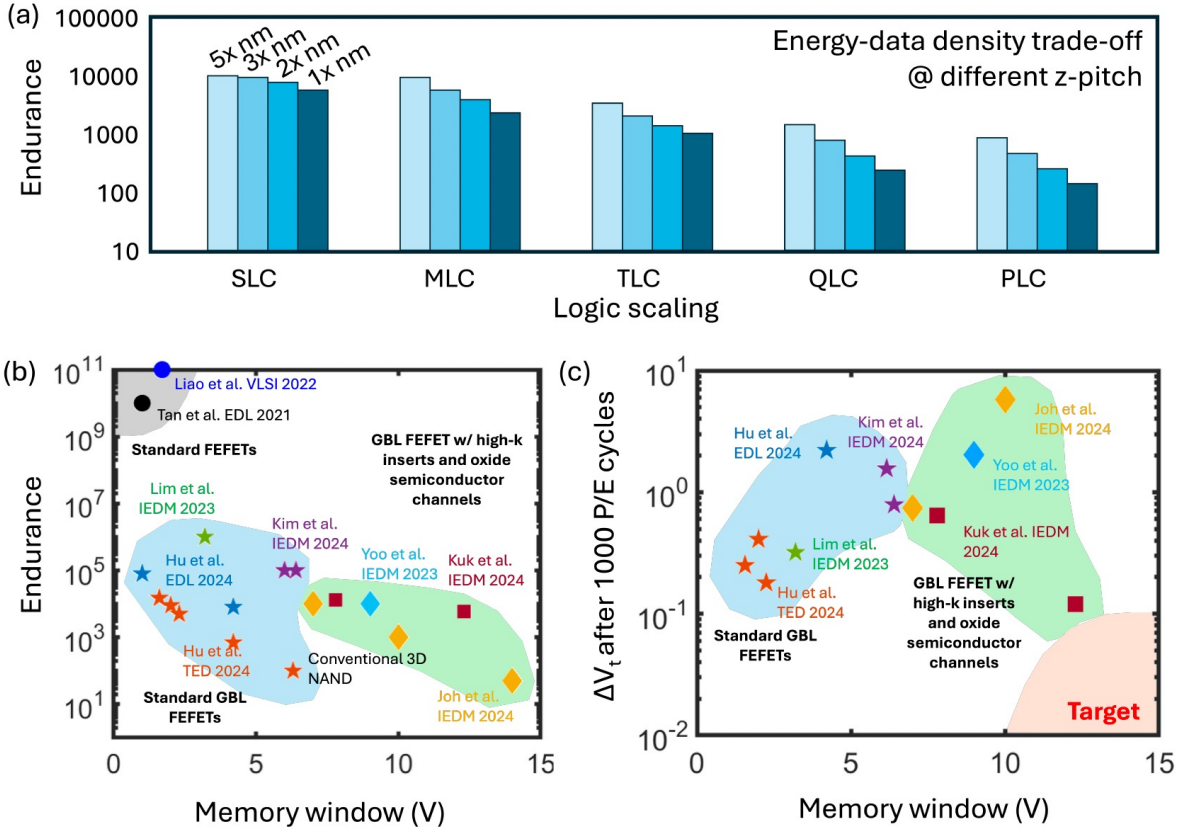
Write Endurance

Array-level Reliability

Lateral charge migration

Device-device variation

Write Endurance



Venkatesan, P., et al. IMW 2025

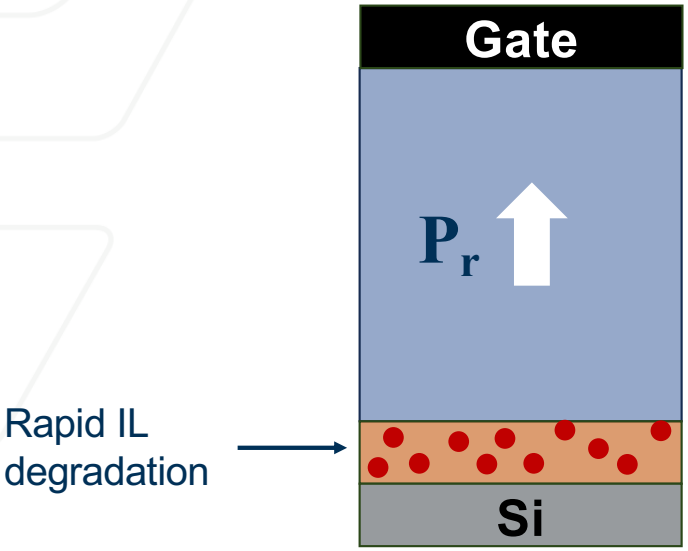
Endurance decreases with increasing MW

IL degradation drives V_t shift in FEFETs

Georgia Tech

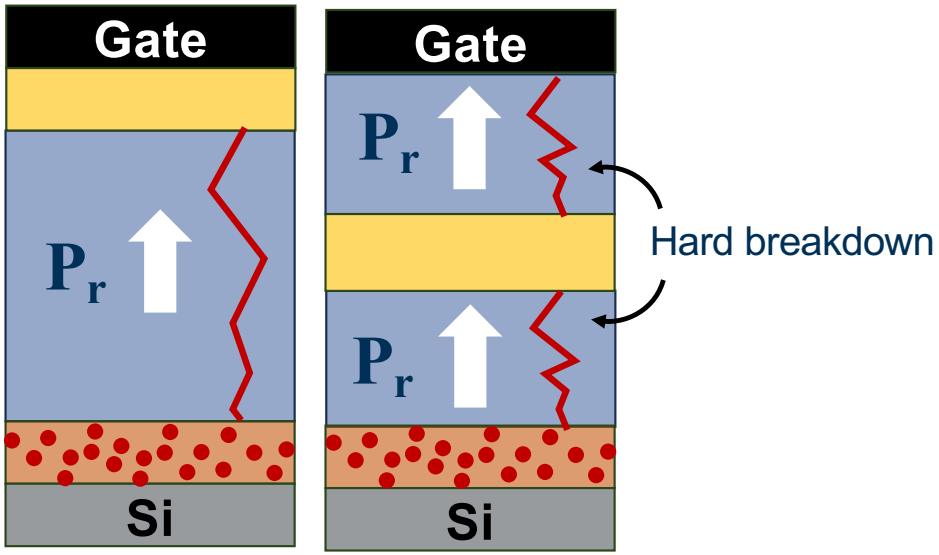
Write Endurance

Standard FEFETs



- Small MW
- V_{write} / V_{BD} lower than 1
- IL degradation dominates
- MW closure
- Minimal FE degradation

Engineered FEFETs



- Large MW
- V_{write} / V_{BD} close to 1
- Rapid IL degradation
- Increased risk of hard breakdown

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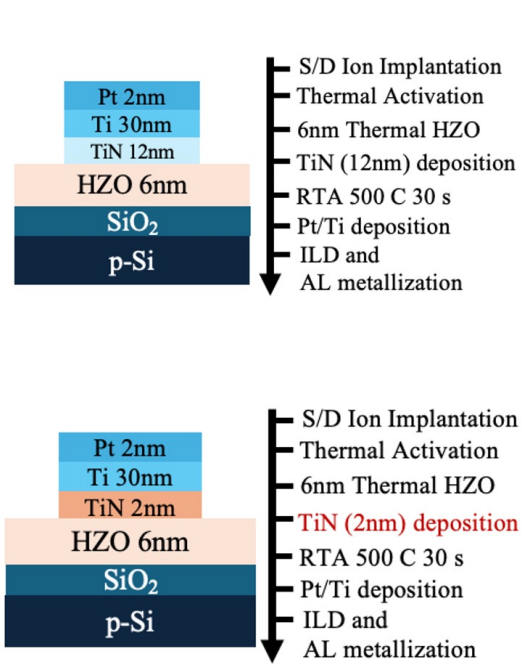
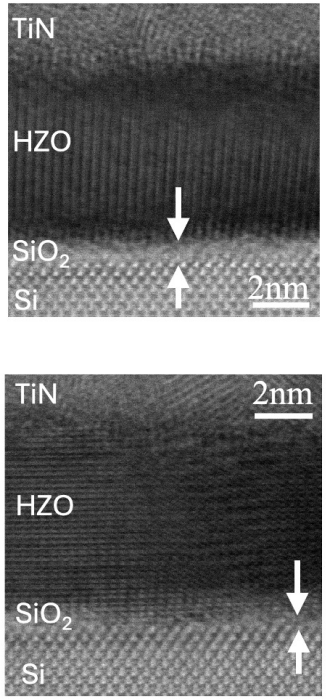
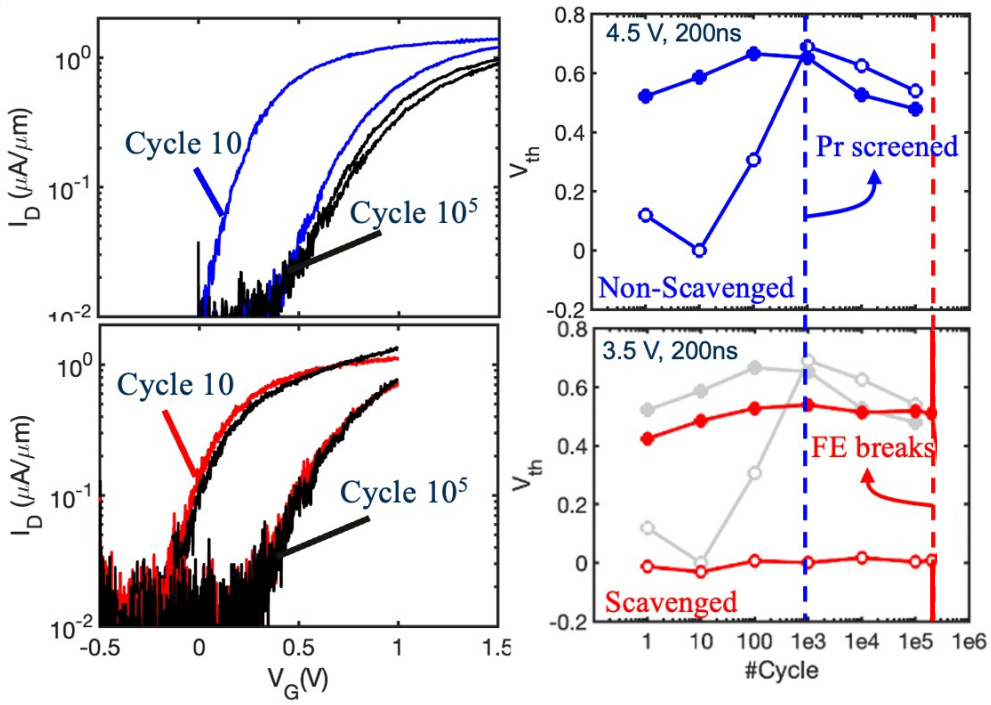
Write Endurance







71st International Electron Devices Meeting

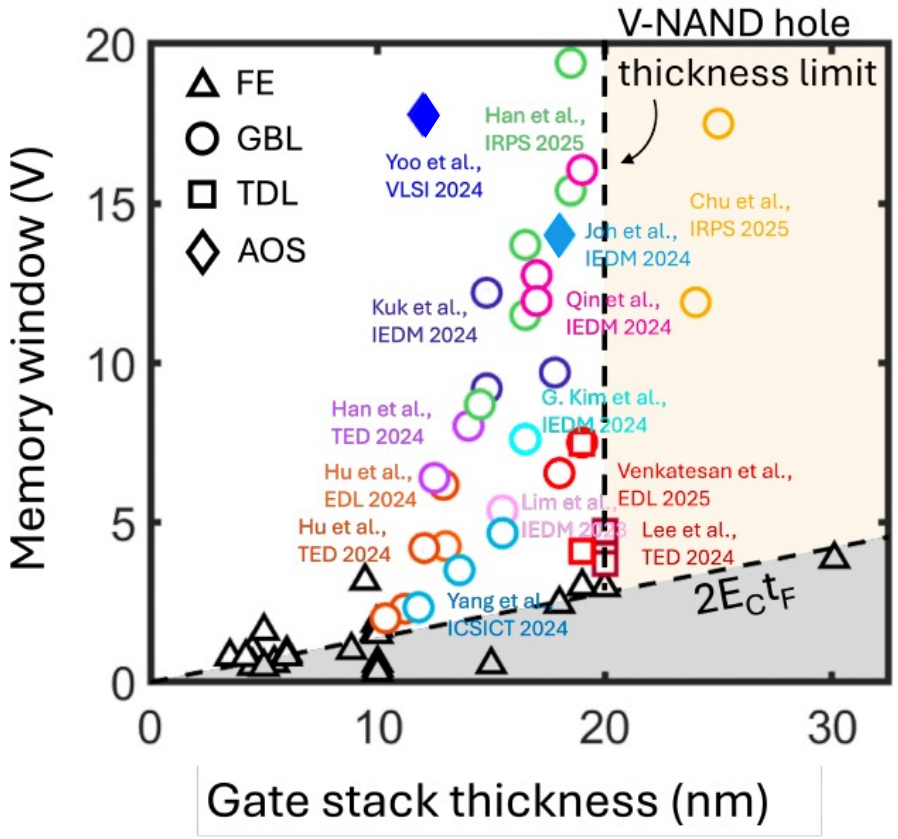
Priyankka Ravikumar, Georgia Tech

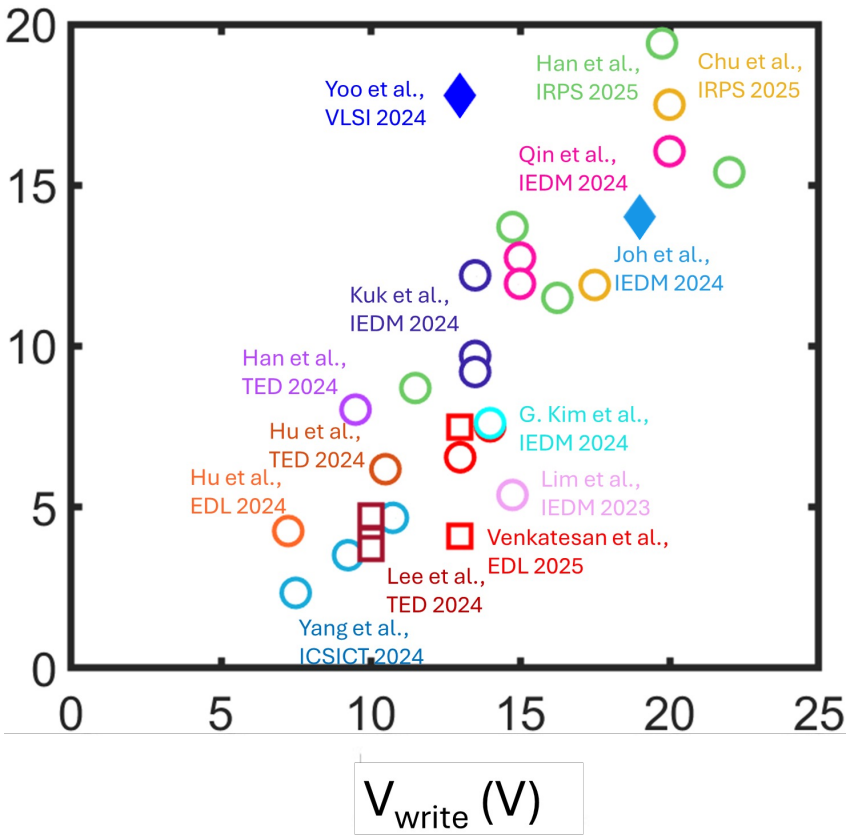
"Experimental Demonstration of Robust High Temperature Operation with 10^4 Endurance and Stable V_{th} at 125 °C Enabled by IL Scavenging in Si Channel FeFETs"

5:15 PM | Session 23-7 Dec. 9, 2025

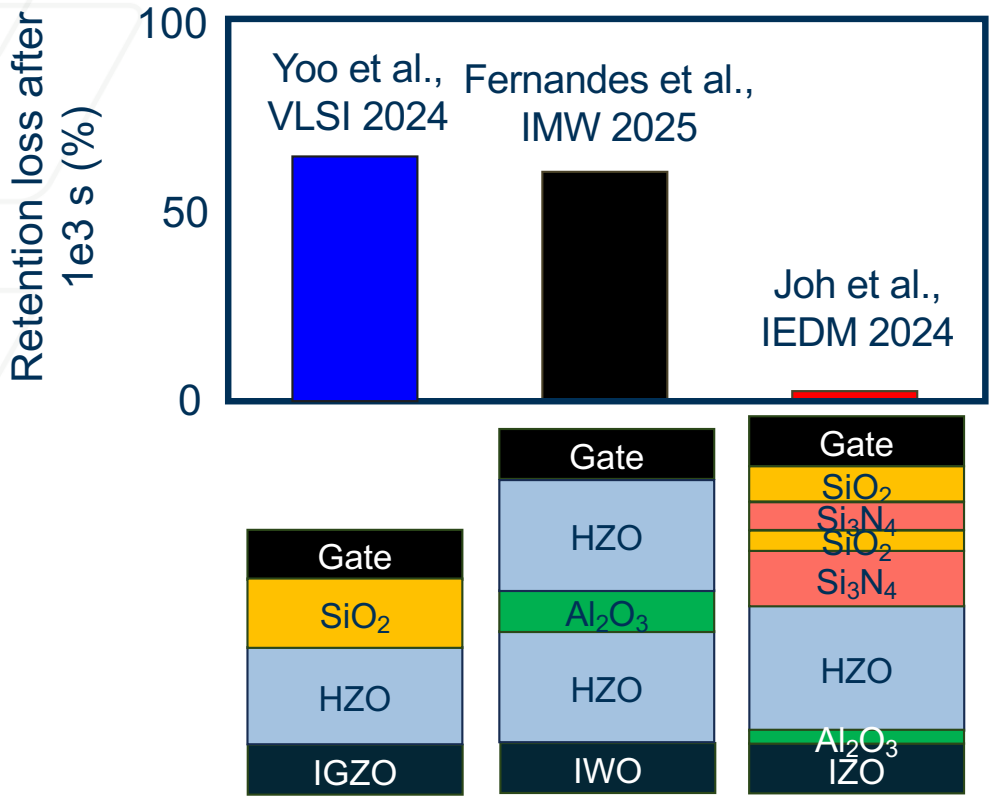
Georgia Tech

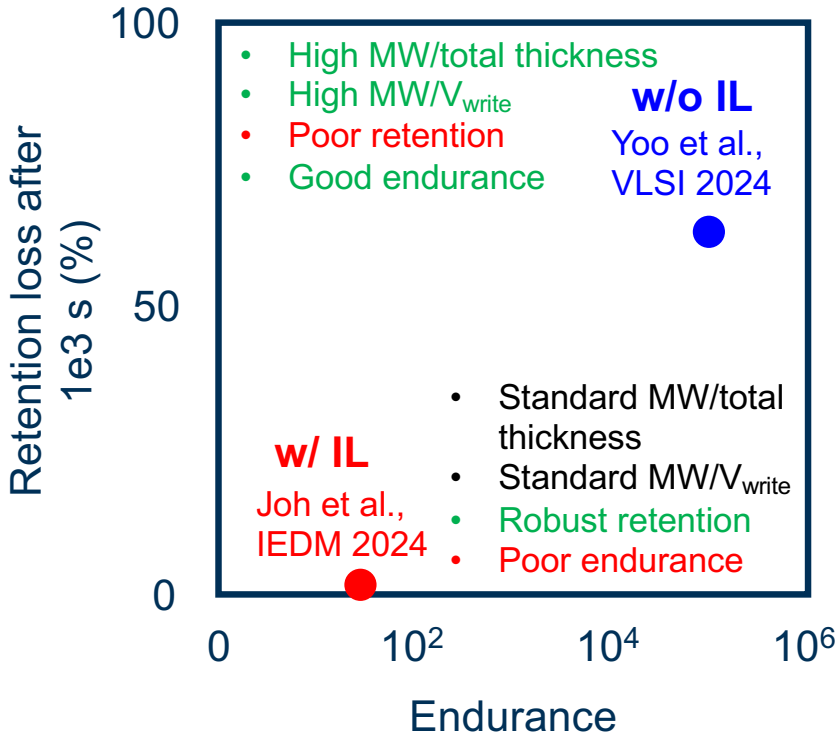
Amorphous oxide semiconductor channel





Retention – endurance trade off





Insertion of IL improves improves retention characteristics

But Introduction of IL leads to poor endurance

What about reliability of ferroelectric NAND?

Performance

Memory window

Device Reliability

Retention

Disturb

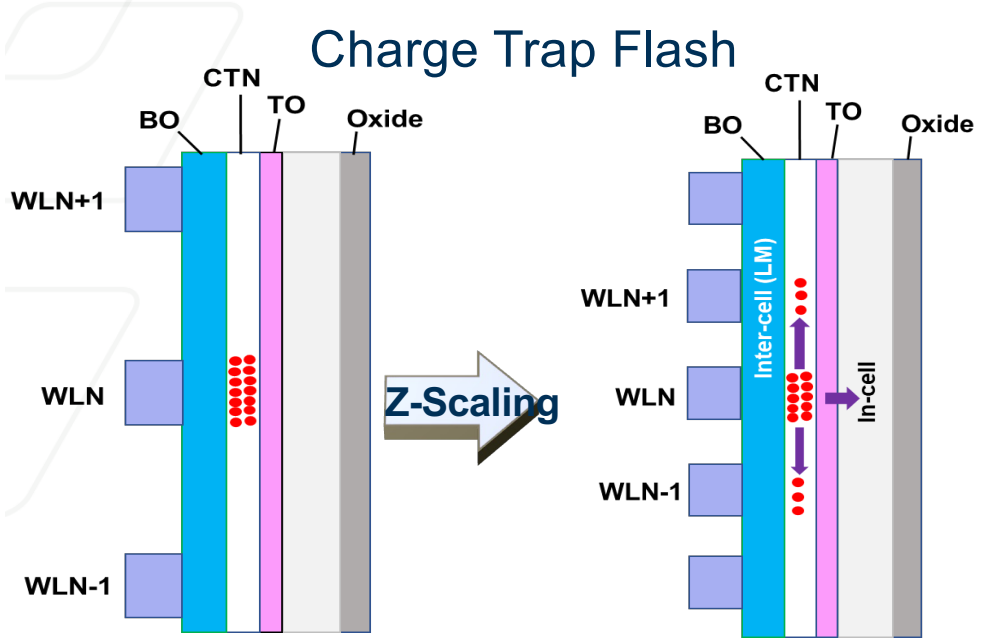
Write Endurance

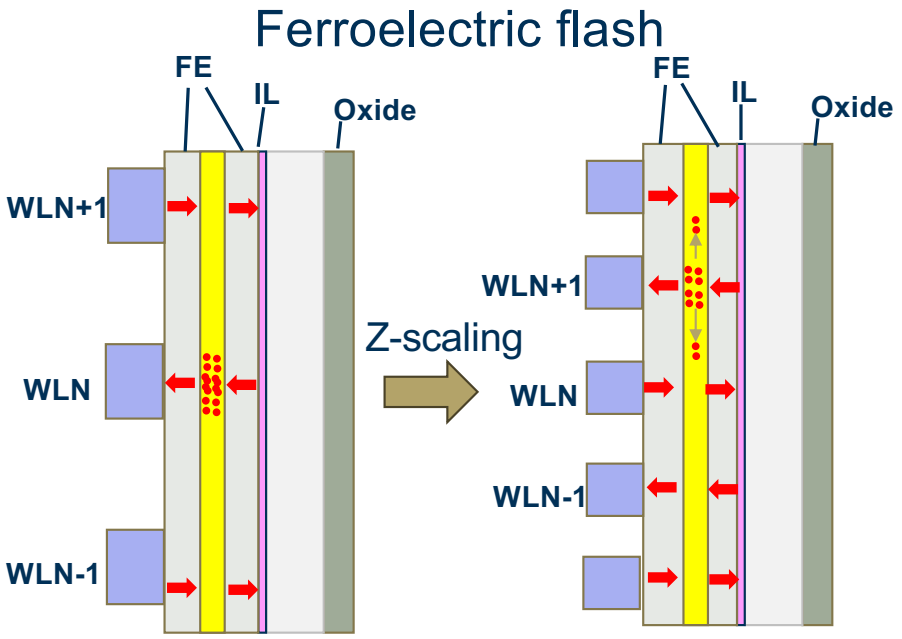
Array-level Reliability

Lateral charge migration

Device-device variation

Lateral charge migration





Lateral charge migration prevents aggressive Z-scaling for 3D NAND.

The nature of trapped charges at the ferroelectric—interlayer interface will determine the scaling potential of ferroelectric 3D NAND technology.

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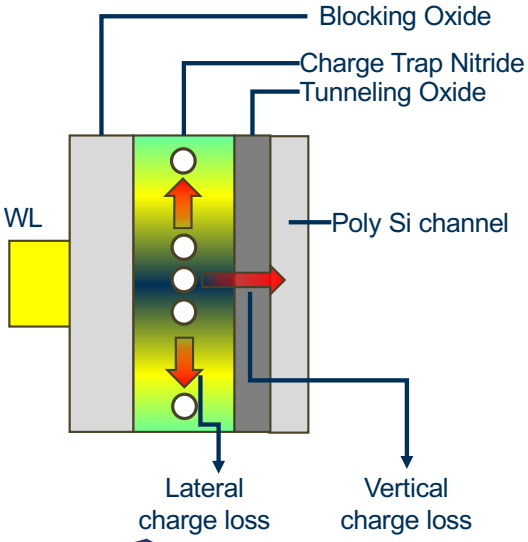
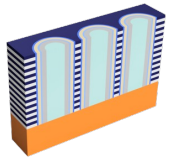
What about reliability of ferroelectric NAND?

❶ Retention	✅ Demonstrated
❷ Disturb	✅ Demonstrated
❸ Write endurance	⚠️ Under Evaluation
❹ Lateral charge migration	⚠️ Under Evaluation
❺ Device-device variation	⚠️ Under Evaluation
⋮	

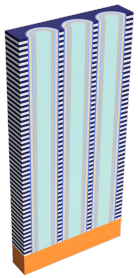
Ferroelectrics for Future NAND Storage Technology

Ferroelectric augmentation can provide enable NAND scaling in future generations

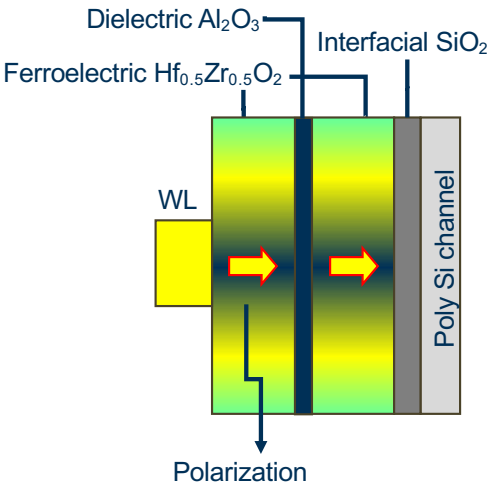


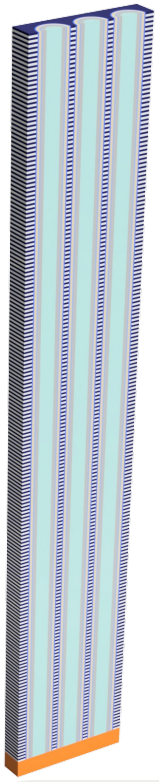


2014:
First 3D NAND
24 Layers, MLC



2025:
300+ Layers, QLC
5 Trillion+ transistors





2030 and
beyond

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Our team


Prasanna Venkatesan


Lance Fernandes


Salma Soliman


Taeyoung Song


Zekai Wang


Dr. Hang Chen


Yu Hsin Kuo


Nashrah Afroze


Priyankka Ravikumar


Jiayi Chen


Dr. Mengkun Tian


Dr. Chinsung Park (SK Hynix)


Dr. Dipjyoti Das (NIT Silchar)


Dr. Zheng Wang (Micron)


Dr. Sarah Lombardo (TEL)


Dr. Nujhat Tasneem (Intel)


Anthony Gaskell (TSMC)

Collaborators:
Prof. Andrea Padovani, DIEF, UNIMORE
Dr. Gaurav Thareja, Dr. Luca Larcher, Applied Materials
Prof. Lauren Garten, Prof. Shimeng Yu, Prof. Suman Datta, Georgia Tech

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