Ferroelectric memories

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Georgia Tech, 2/13/2025

Georgia Tech

High Bandwidth Memory and DRAM

Memory

Hyperscale AI and High-performance Computing

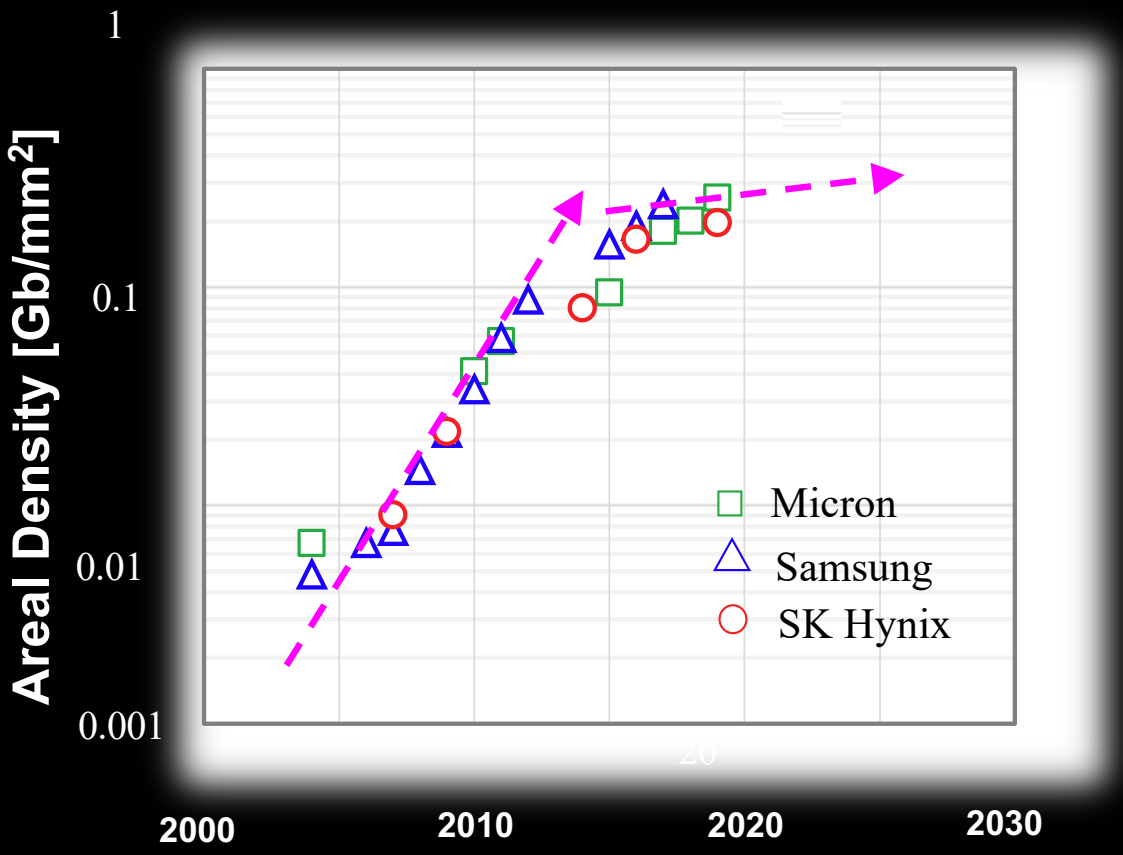
HBM3E: 12-high, 32 GB

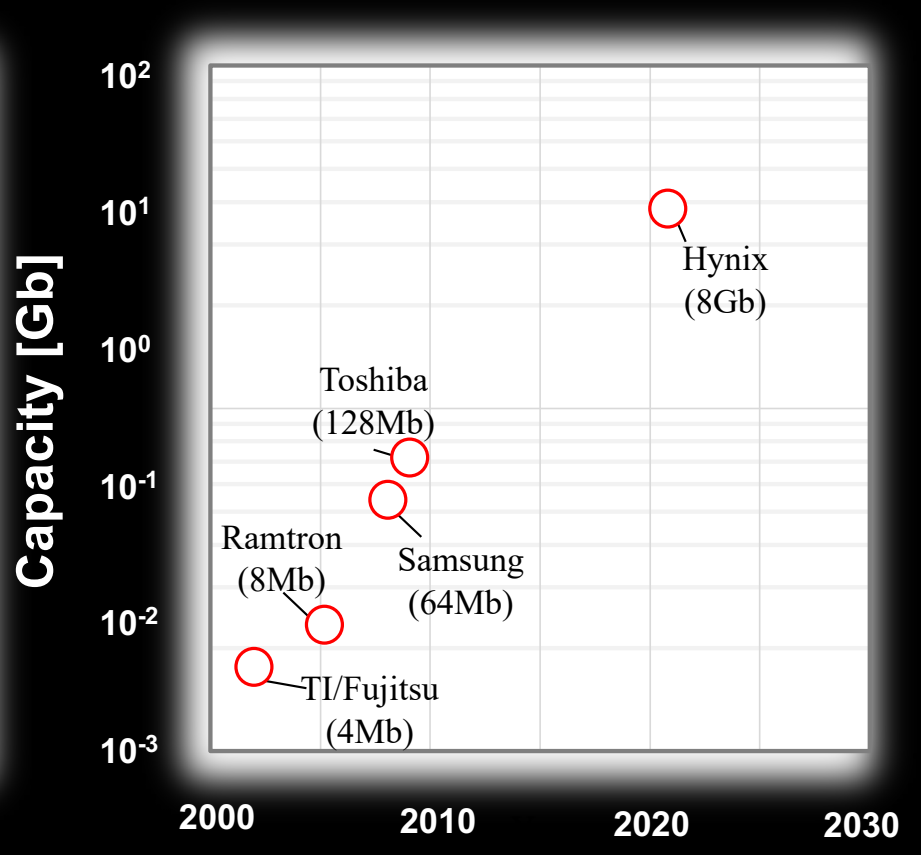
1.18 TB/s

Source: NVIDIA

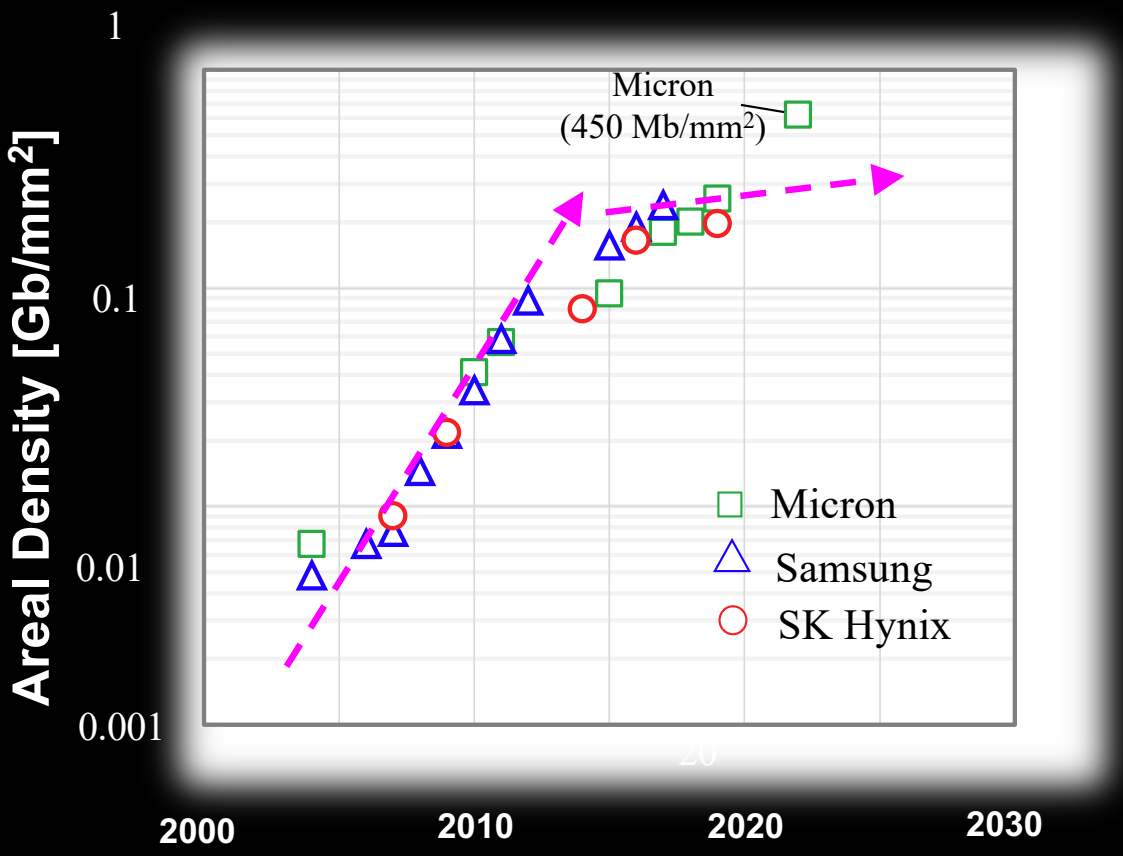
Source: SK hynix

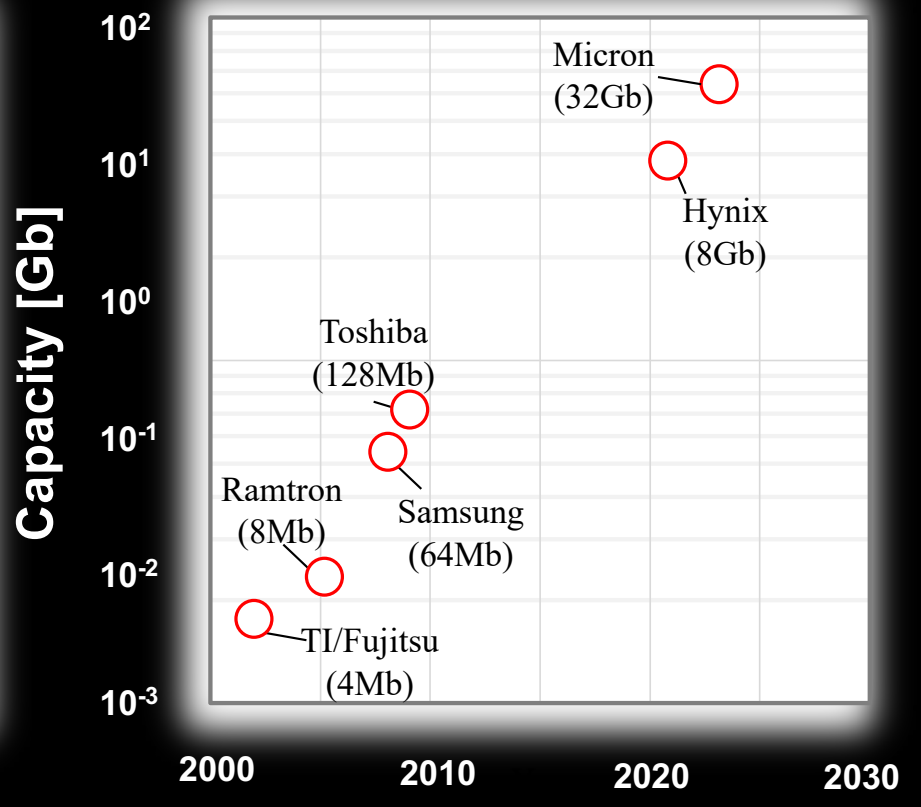
Evolution of DRAM Technology





Evolution of DRAM





Ferroelectricity in CMOS-compatible Materials

APPLIED PHYSICS LETTERS **99**, 112904 (2011)

Phase transitions in ferroelectric silicon doped hafnium oxide

T. S. Böscke,[1,2,a),b)] St. Teichert,[3,b)] D. Bräuhaus,[4] J. Müller,[5] U. Schröder,[2,b)] U. Böttger,[4] and T. Mikolajick[2,6]
[1]*Löberwallgraben 2, 99096 Erfurt, Germany*
[2]*Namlab gGmbH, 01187 Dresden, Germany*
[3]*UAS Jena, Department of SciTec, 07745 Jena, Germany*
[4]*RWTH Aachen, Institut für Werkstoffe der Elektrotechnik, 52062 Aachen, Germany*
[5]*Fraunhofer Center Nanoelectronic Technologies (CNT), 01099 Dresden, Germany*
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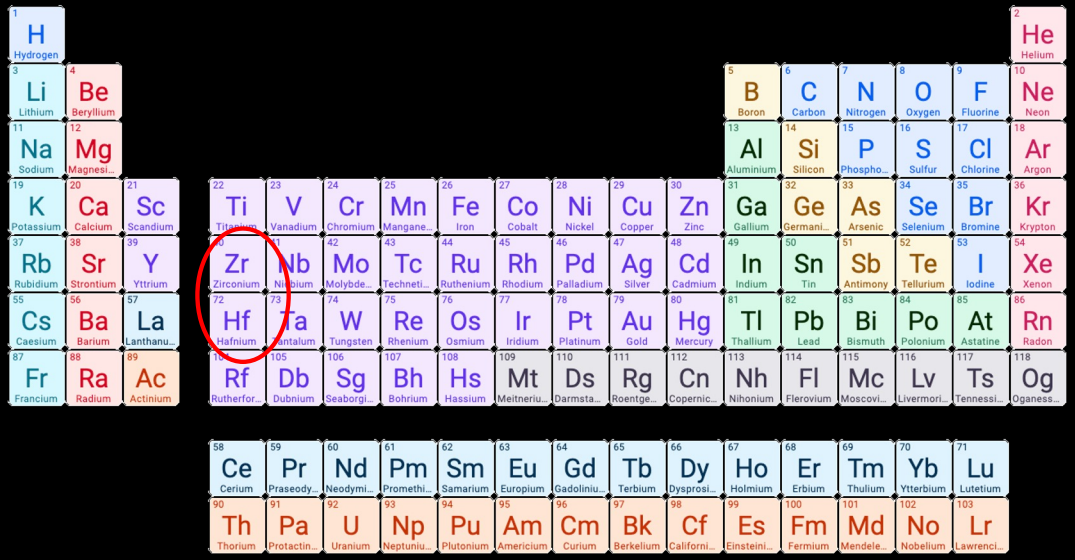
(Received 18 July 2011; accepted 19 August 2011; published online 15 September 2011)

HfO_2-based materials have been in use in Logic and DRAM technology since mid-2000s.



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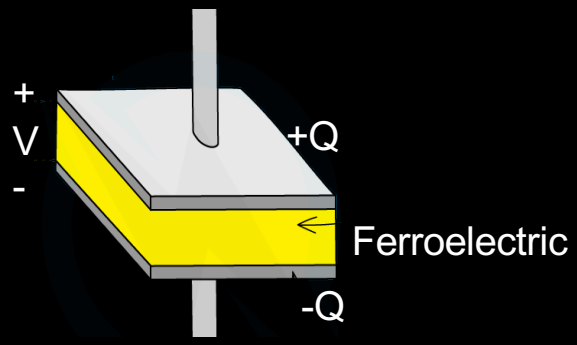
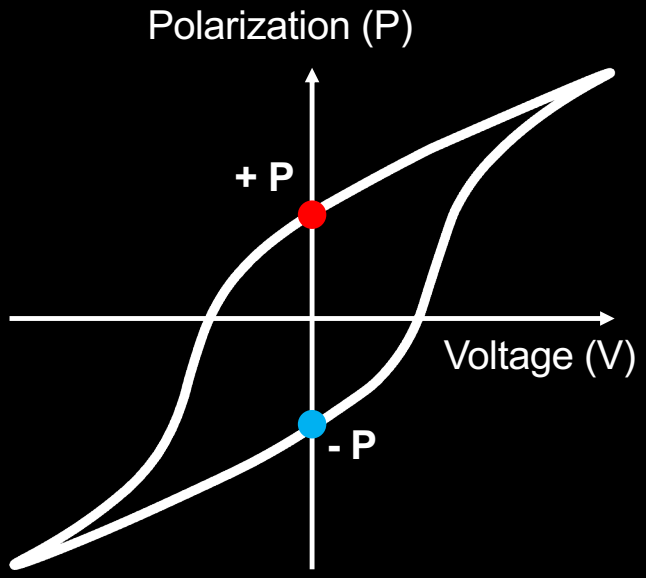
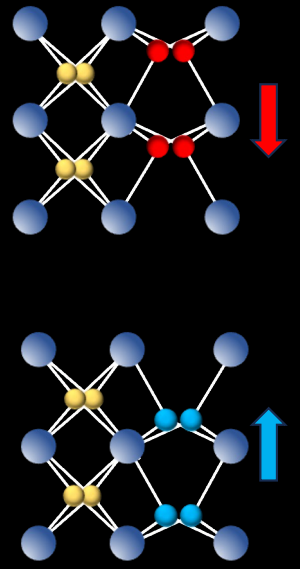
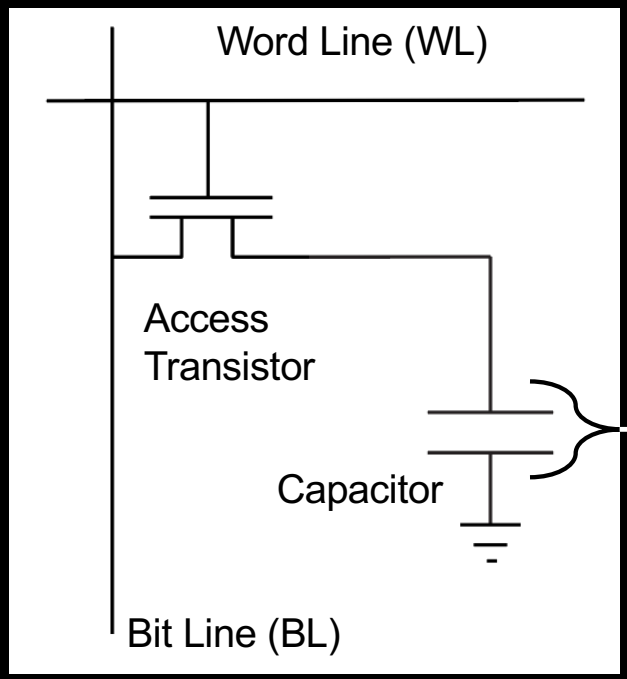
A ferroelectric is an insulator with a spontaneous polarization, which can be switched by a voltage above coercive voltage .





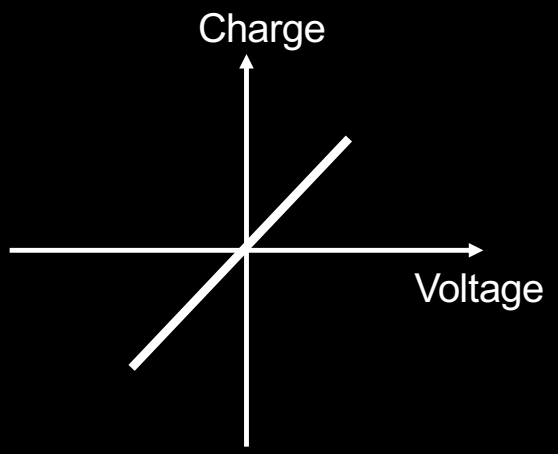


Dynamic RAM vs. Ferroelectric RAM



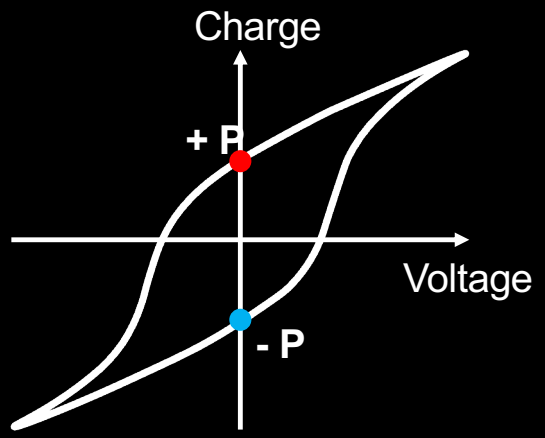
Dynamic RAM

Volatile
Needs Refresh



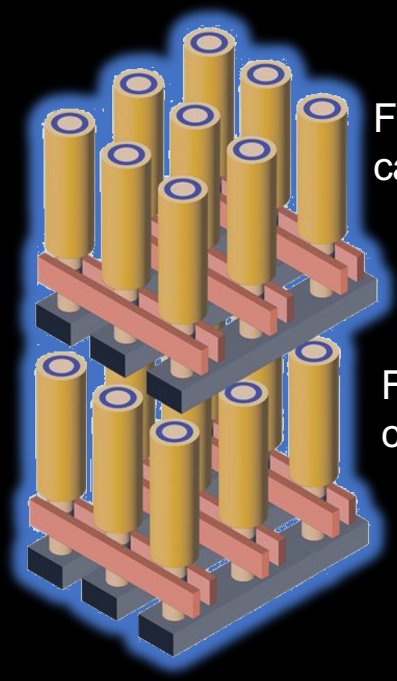
Ferroelectric RAM

Nonvolatile
Refresh-free



The Secret to Achieving 450 Mb/mm^2

3D-stacked, multi-layer Configuration

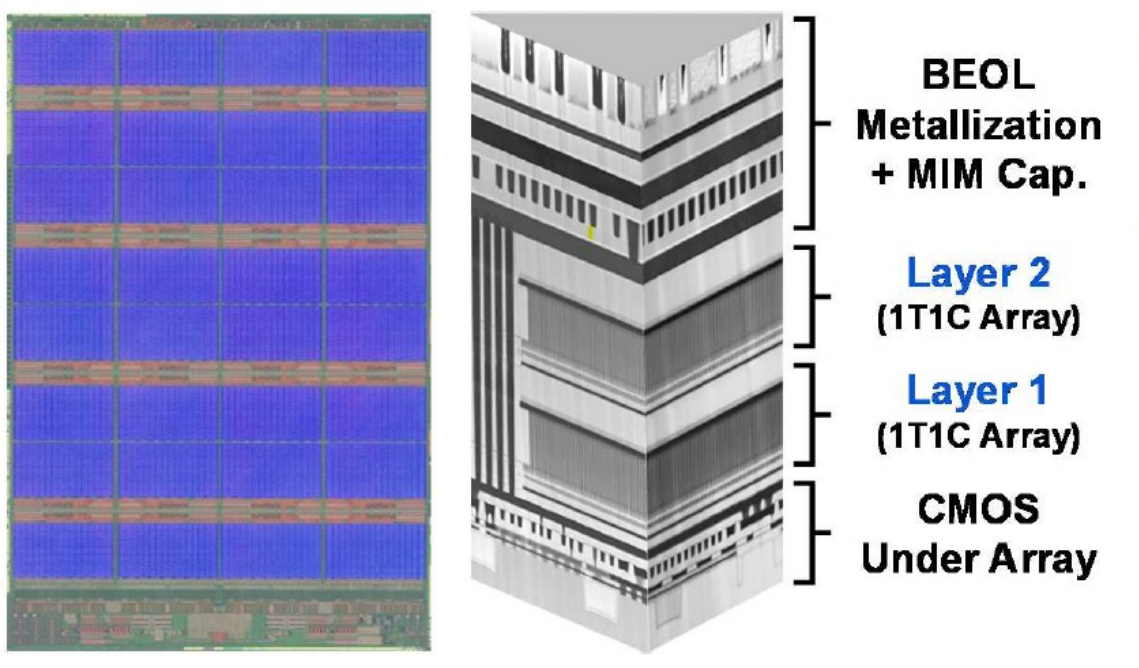


NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads

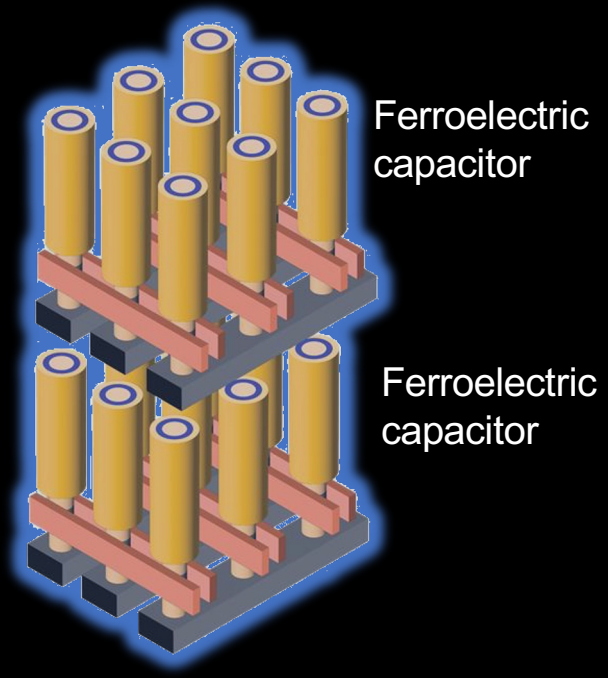
N. Ramaswamy, A. Calderoni, J. Zahurak, G. Servalli, A. Chavan, S. Chhajed, M. Balakrishnan, M. Fischer, M. Hollander, D. P. Ettisserry, A. Liao, K. Karda, M. Jerry, M. Mariani, A. Visconti, B. R. Cook, B. D. Cook, D. Mills, A. Torsi, C. Mouli, E. Byers, M. Helm, S. Pawlowski, S. Shiratake, and N. Chandrasekaran
Micron Technology Inc., Boise, USA, email: dramaswamy@micron.com

Ramaswamy et al. IEDM 2023.

The Secret to Achieving 450 Mb/mm^2



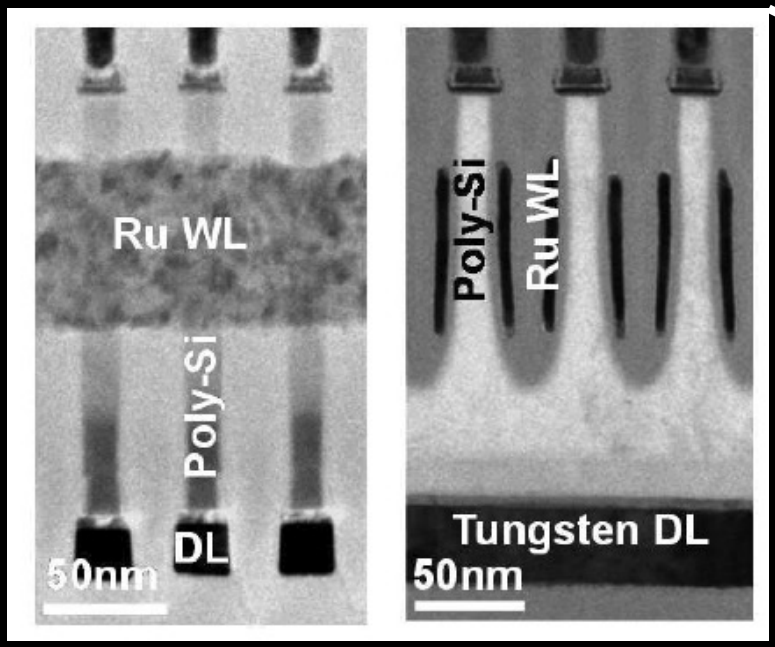
3D-stacked, multi-layer Configuration

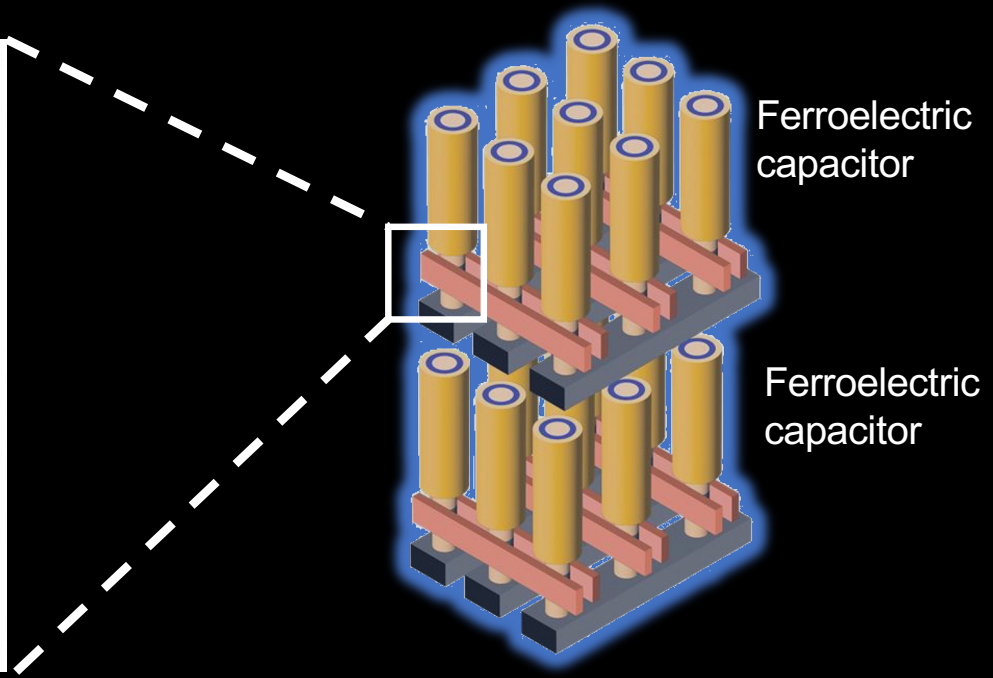


Ramaswamy et al. IEDM 2023.

The Secret to Achieving 450 Mb/mm^2

Non-volatility allows for higher off-state current of poly-Si vertical channel access transistors.





Ramaswamy et al. IEDM 2023.

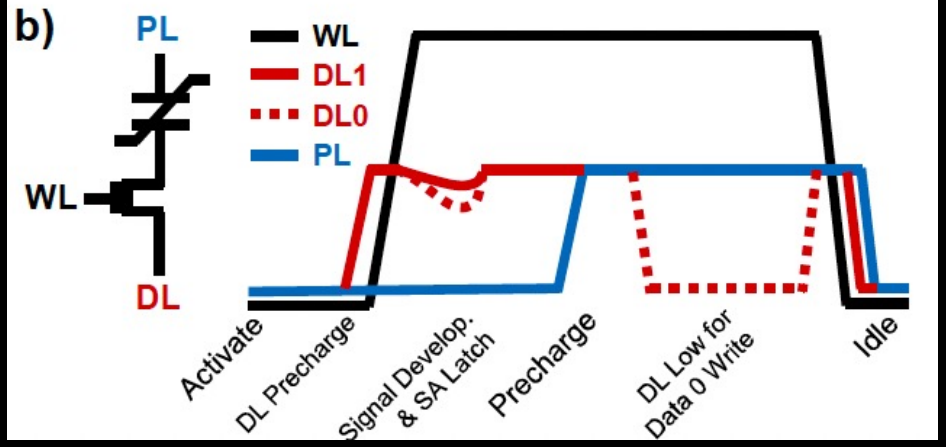
What is the trade-off?

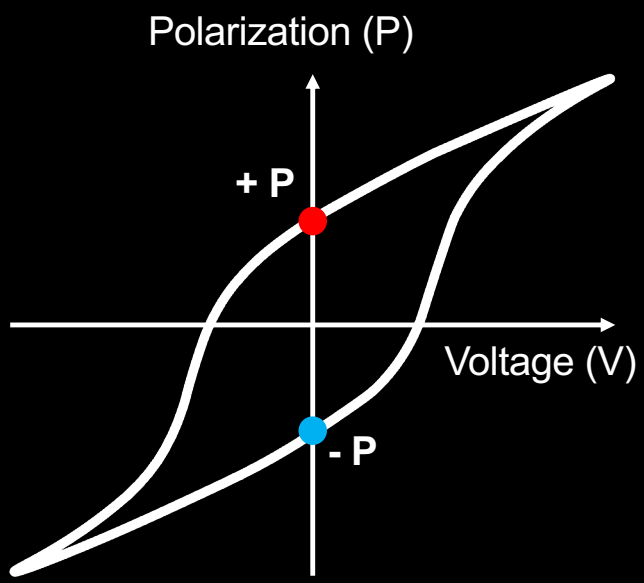
Ferroelectric RAM is slower than standard DRAM.

a)

Timing	LPDDR5	NVDRAM
tRC	60ns	185ns
tRCD	18ns	85ns
tWR	34ns	10ns
tRP	18ns	80ns
tAA	22ns	26ns

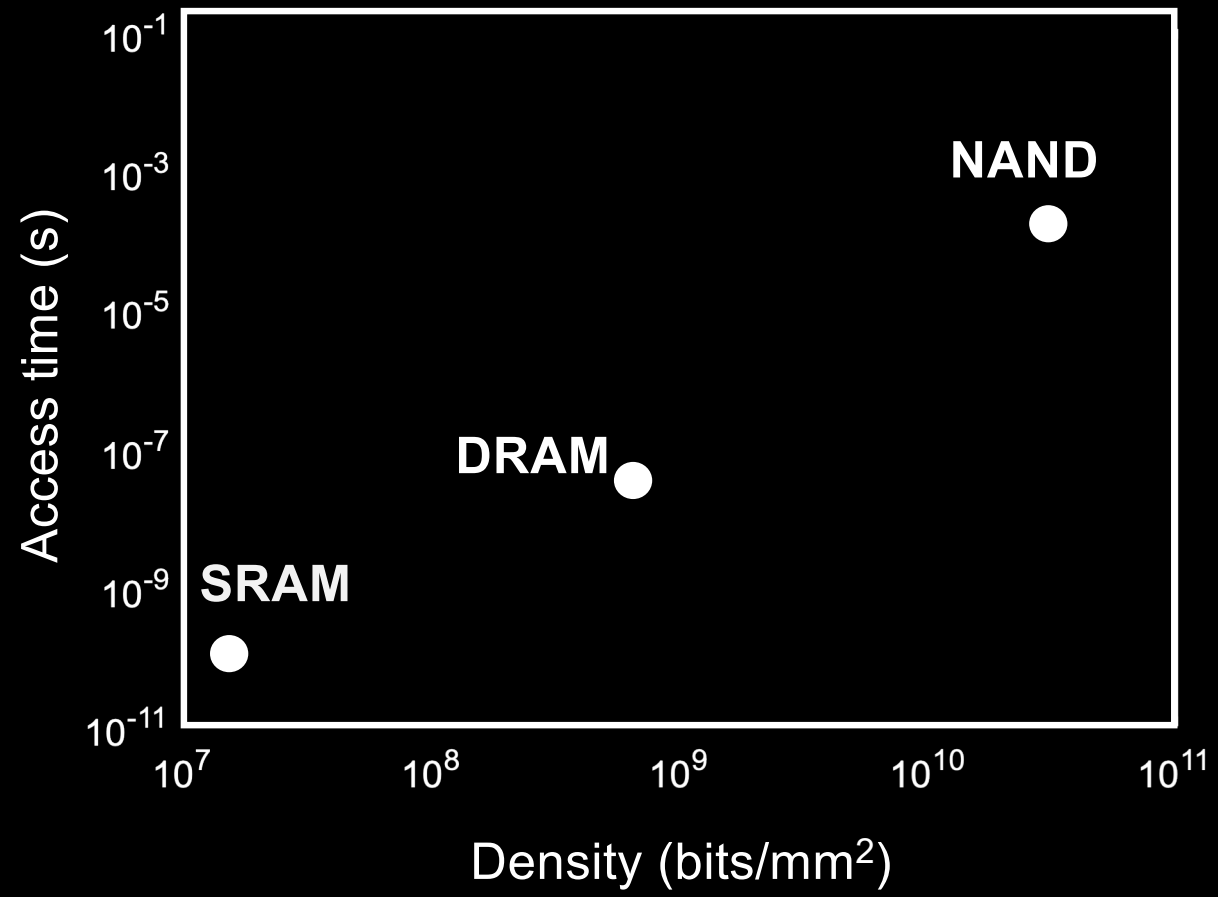
b)



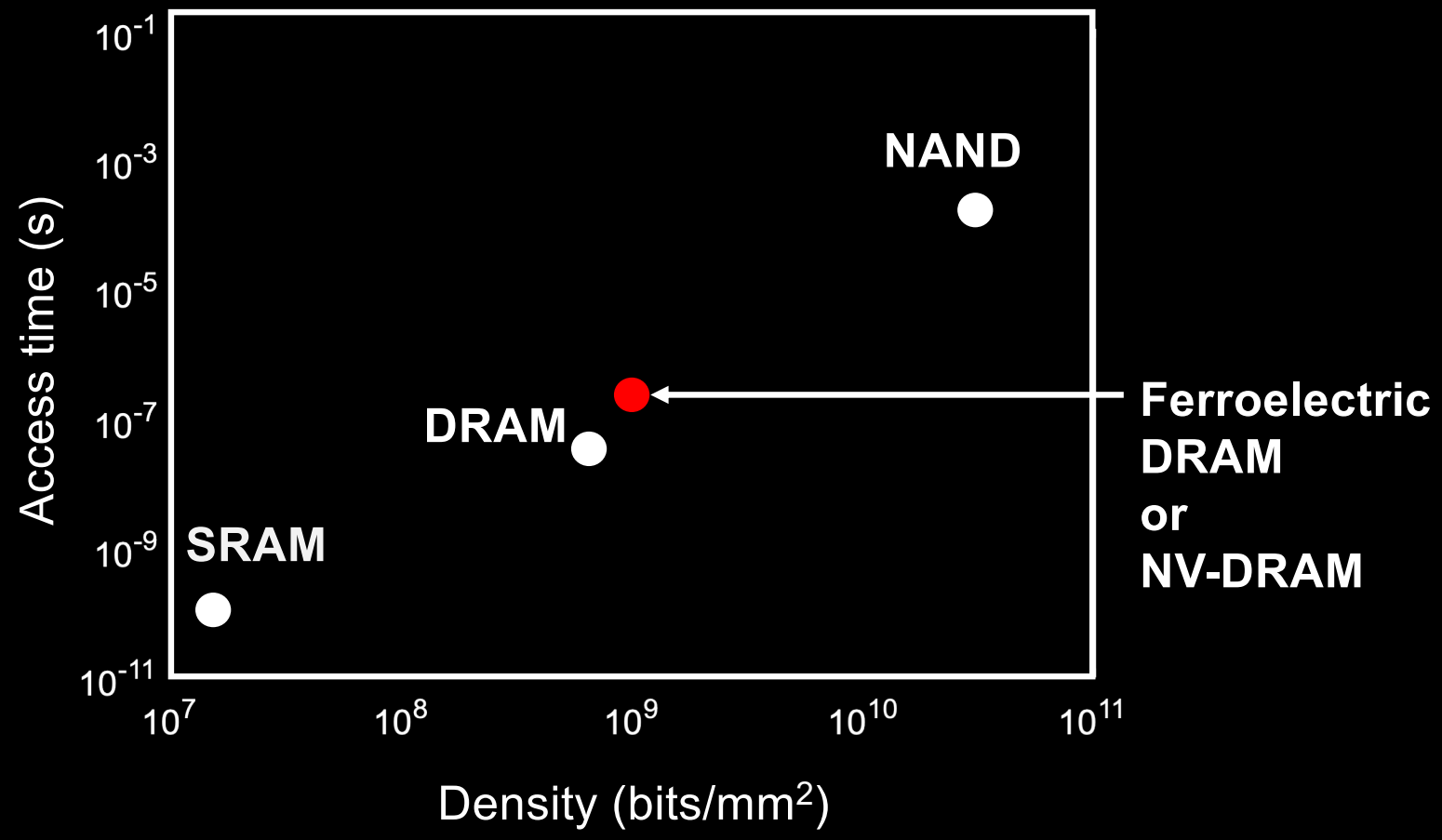


Ramaswamy et al. IEDM 2023.

Memories of the future

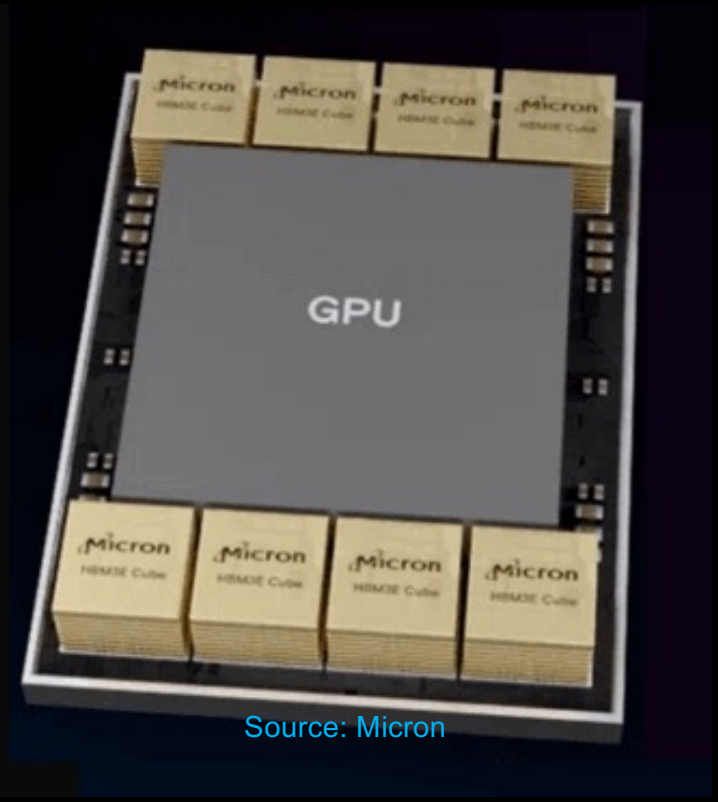


Memories of the future



What’s next?

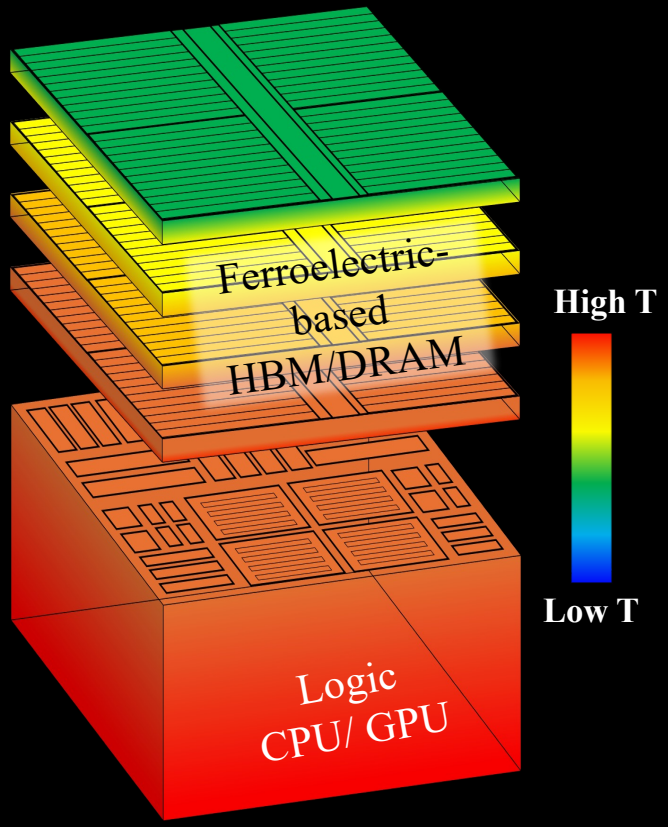
Today’s HBM

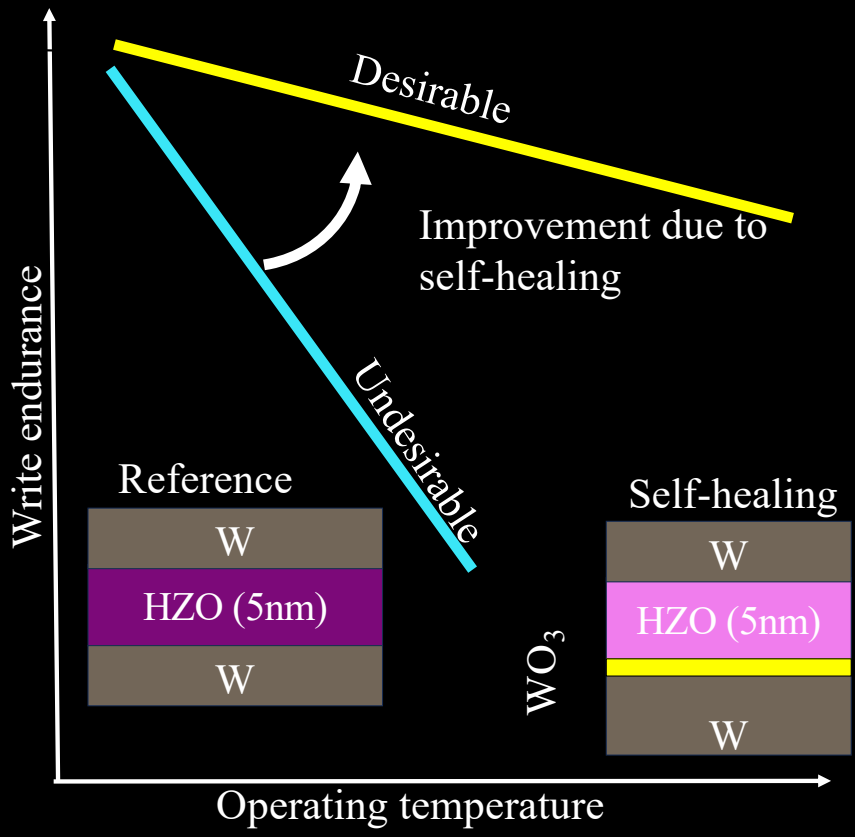


Source: Micron

Future HBM

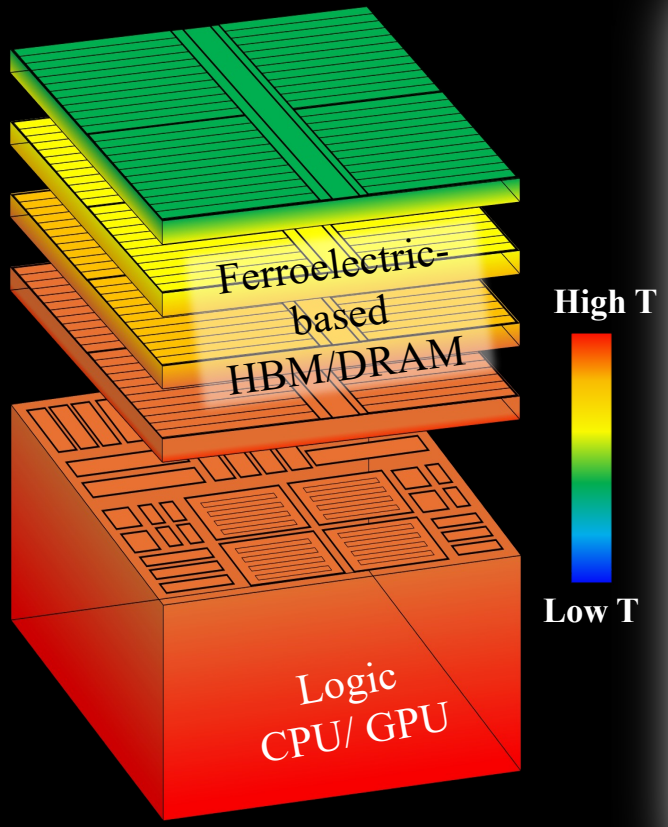
Memories need to be reliable at higher temperatures

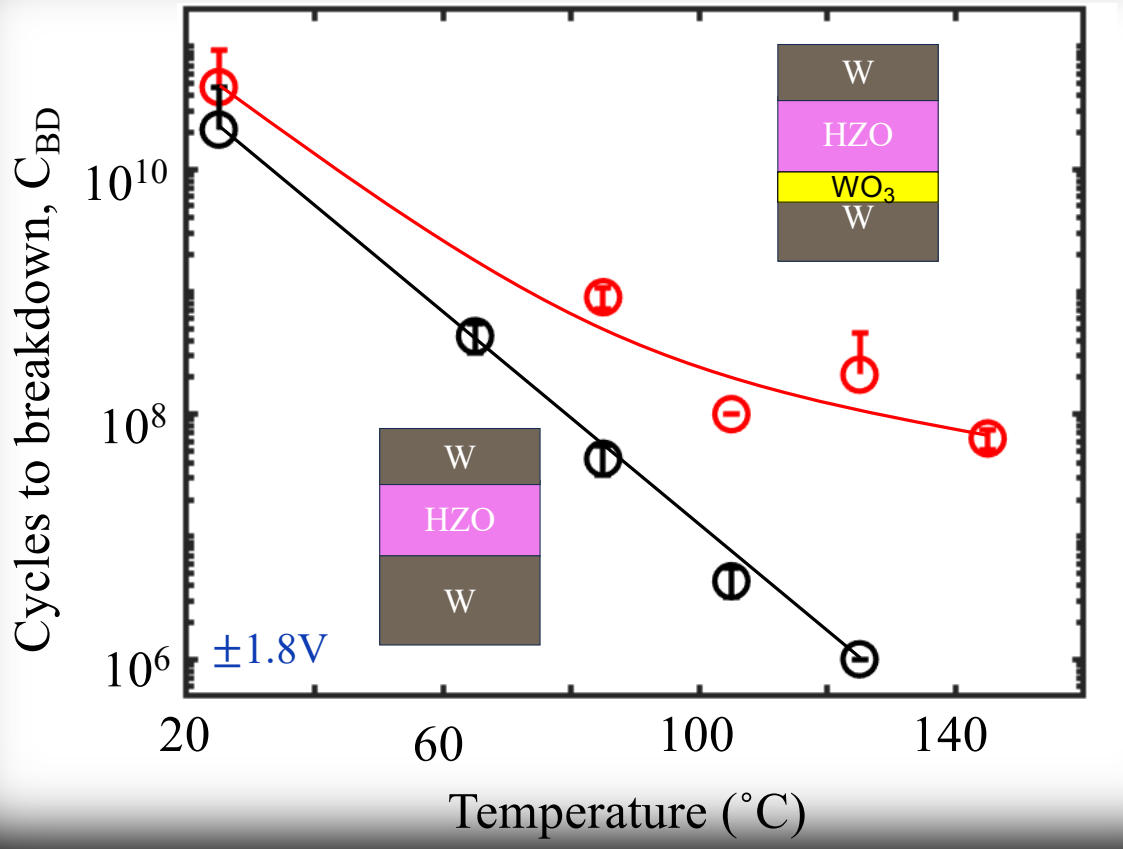




Afroze, Khan et al. IEDM 2024.

Memories need to be reliable at higher temperatures



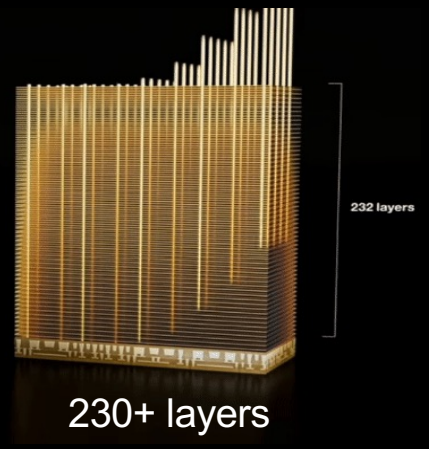


Afroze, Khan et al. IEDM 2024.

The NAND Storage Technology

Storage

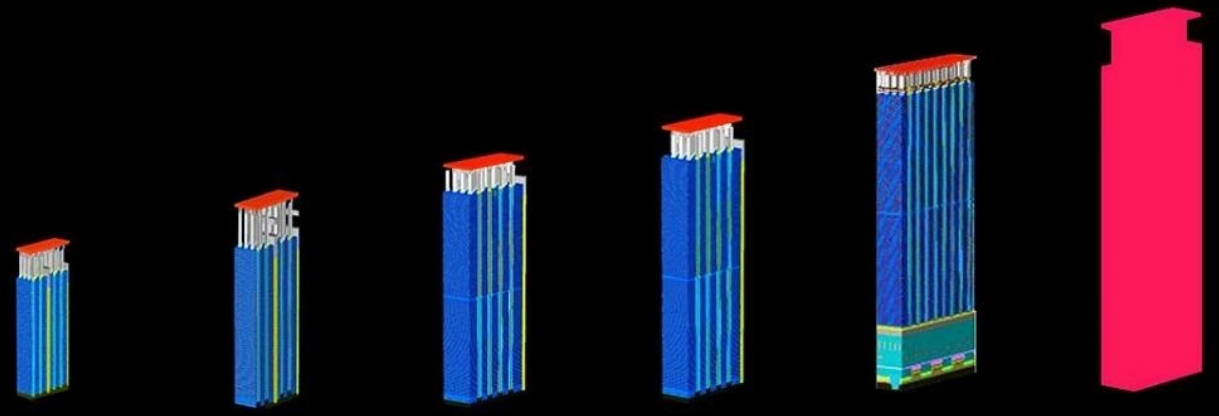
Client, Mobile, Enterprise



230+ layers

2.4 GB/s

Source: Micron



48-Layer (BiCS2) 2016

64-Layer (BiCS3) 2017

96-Layer (BiCS4) 2019

112-Layer (BiCS5) 2020

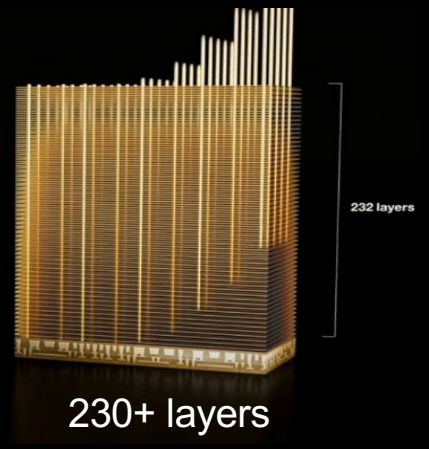
162-Layer (BiCS6) 2022

2xx-Layer (BICS+)

The NAND Storage Technology

Storage

Client, Mobile, Enterprise



230+ layers

2.4 GB/s

Source: Micron

SANDISK™ INVESTOR DAY FUTURE FWD (→) PHASE 01 ///

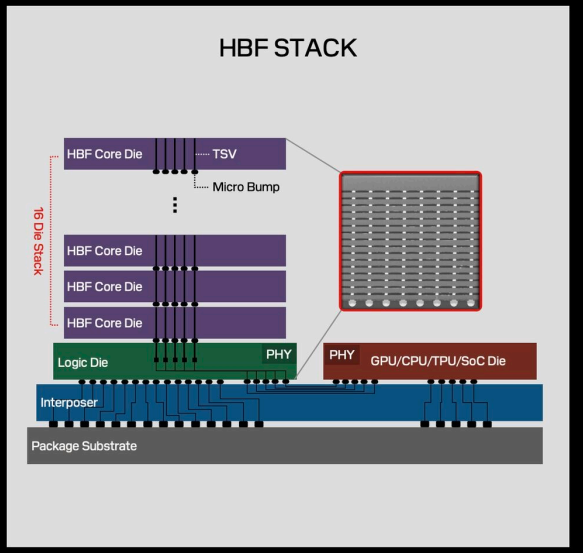
High Bandwidth Flash (HBF™) Augmenting HBM Memory with NAND Flash for AI Inference Workloads

(→) Match HBM Bandwidth
Deliver 8-16X Capacity at Similar Cost

(→) Enabled by BiCS Technology
With CBA Wafer Bonding

(→) Proprietary Stacking Technology
Ultra-Low Die Warpage for 16H Stacking

(→) Architecture Developed Over the Past Year
With Inputs From Major AI Players

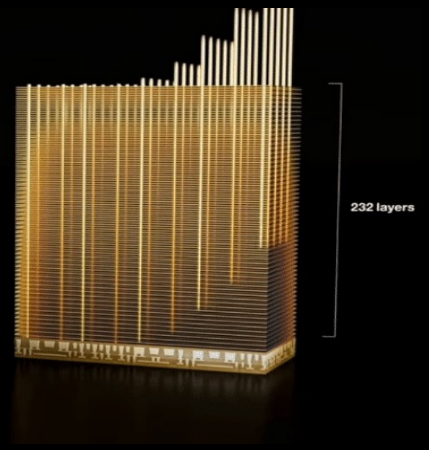


https://blocksandfiles.com/2025/02/12/sandisk-spills-its-technolgy-futures-beans/

The NAND Storage Technology

Storage

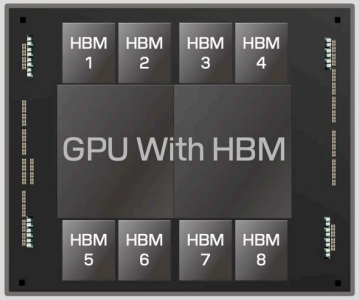
Client, Mobile, Enterprise



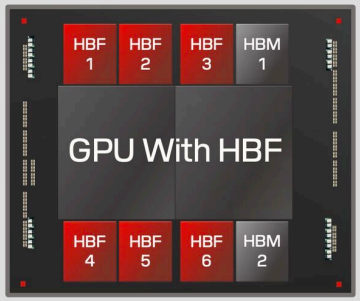
Running Frontier LLM
~1.8T Parameters
16-bit Weights
3,600GB Memory Capacity Needed

SANDISK™ INVESTOR DAY FUTURE FWD (→) PHASE 01 ///

HBM vs. HBF™



192GB Total Memory



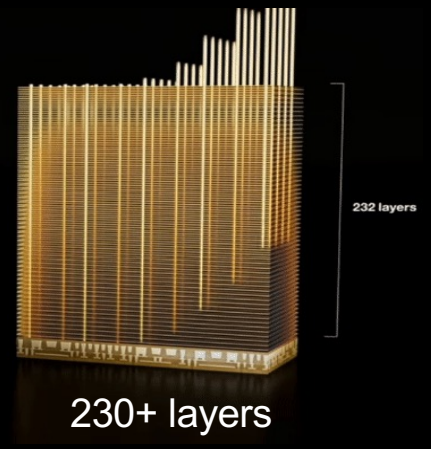
3,120GB Total Memory

https://blocksandfiles.com/2025/02/12/sandisk-spills-its-technolgy-futures-beans/

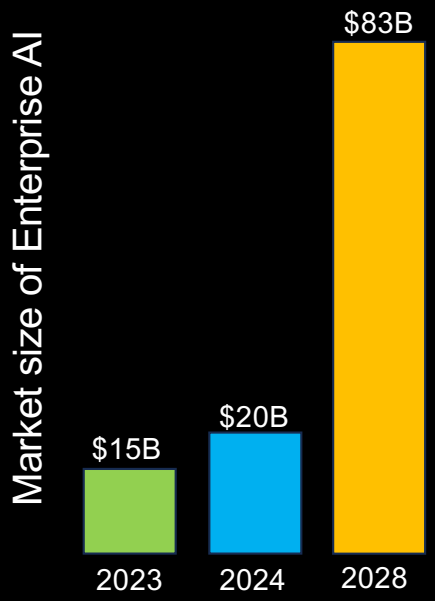
The NAND Storage Technology

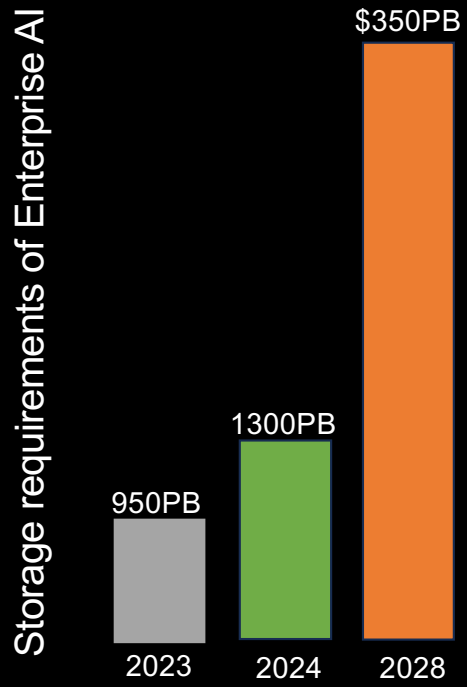
Storage

Client, Mobile, Enterprise



Source: Micron



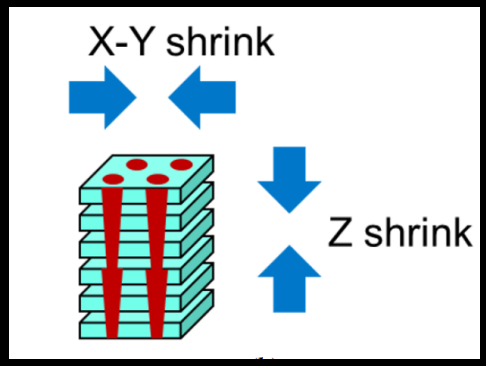


Source: The Business Research Company

Processing and storing data in AI effectively and cost efficiently can require HBM for the actual AI training, but also various types of NAND-based solid-state storage to support the data flows needed to and from the HBM.

Vertical NAND Scaling

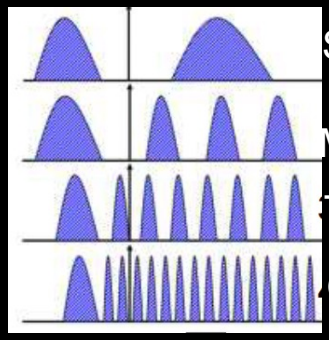
Physical scaling



2013

Samsung 24L MLC

Logical scaling



2022

Samsung 236L TLC
SK Hynix 238L TLC
Micron 232L TLC
192L QLC

?

Vertical NAND scaling toward 1000 layers

Aggressive Z-scaling is required.

Package thickness limits the NAND chip height.

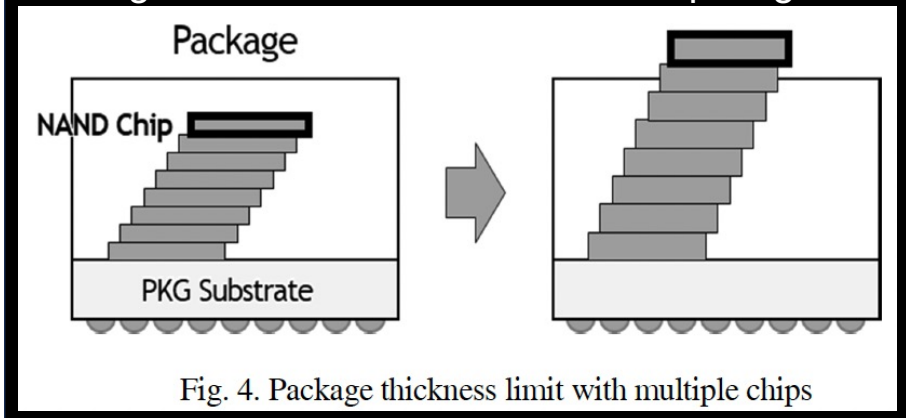
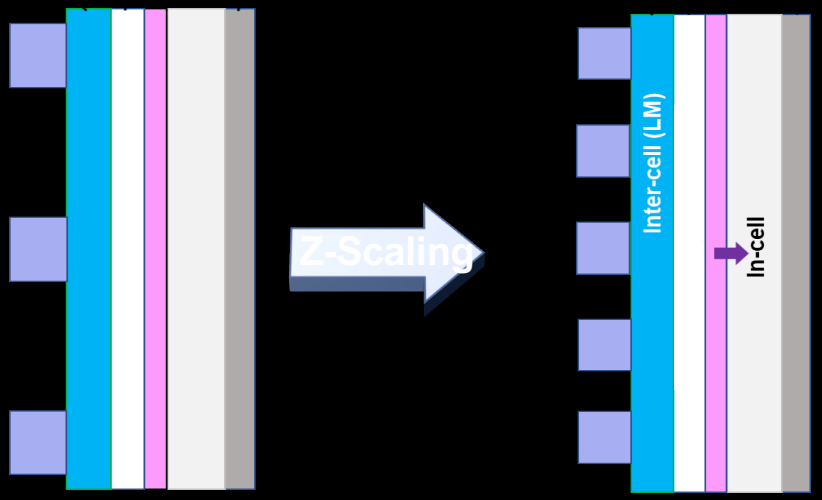


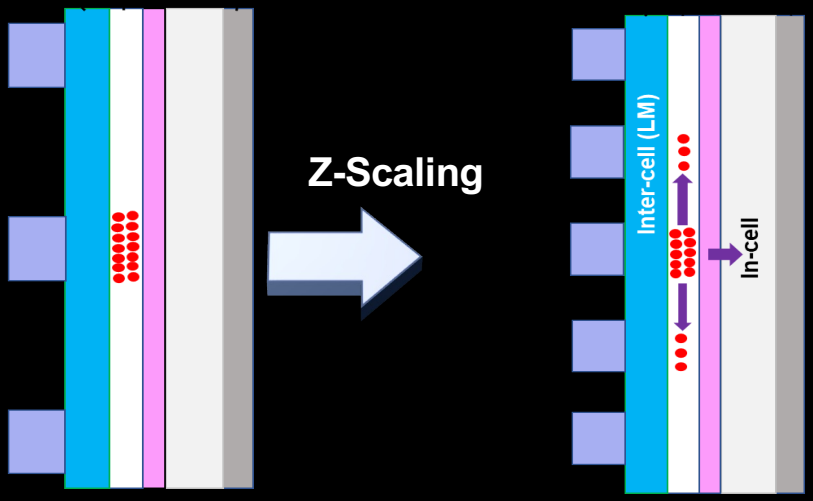
Fig. 4. Package thickness limit with multiple chips



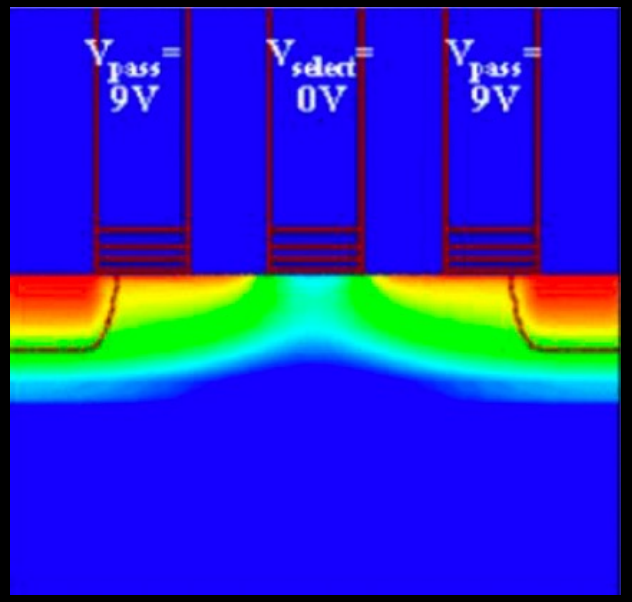
The mold height (cell height) needs to be reduced dramatically.

Challenges for 1000+ layer vertical NAND

1 Lateral charge migration



2 High write voltage

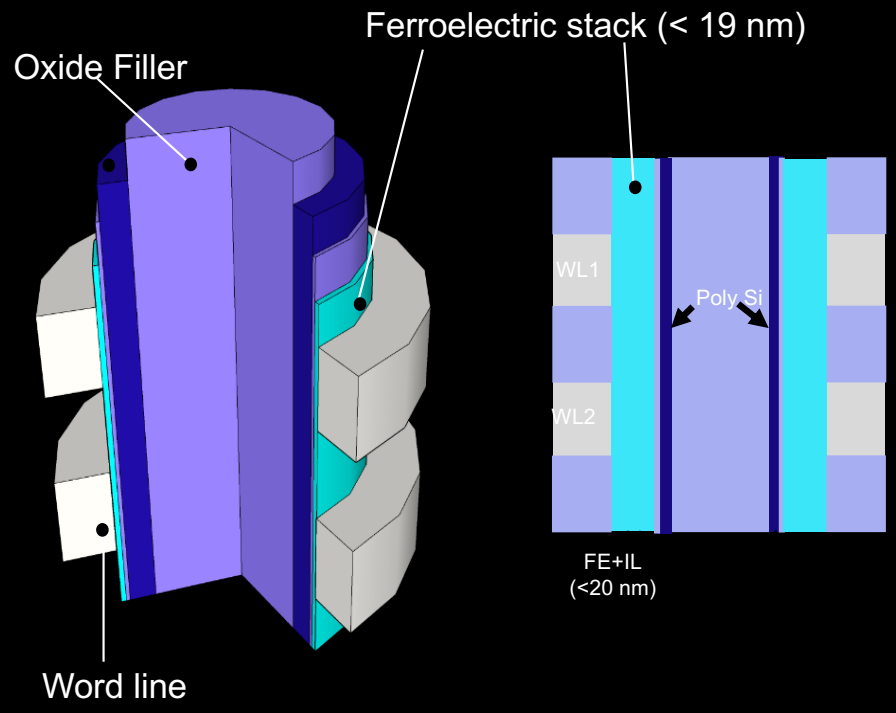


Write voltage of state of the art NAND is >20 V.
Large write voltage affects effective threshold voltage, similar to cell-to-cell interference.

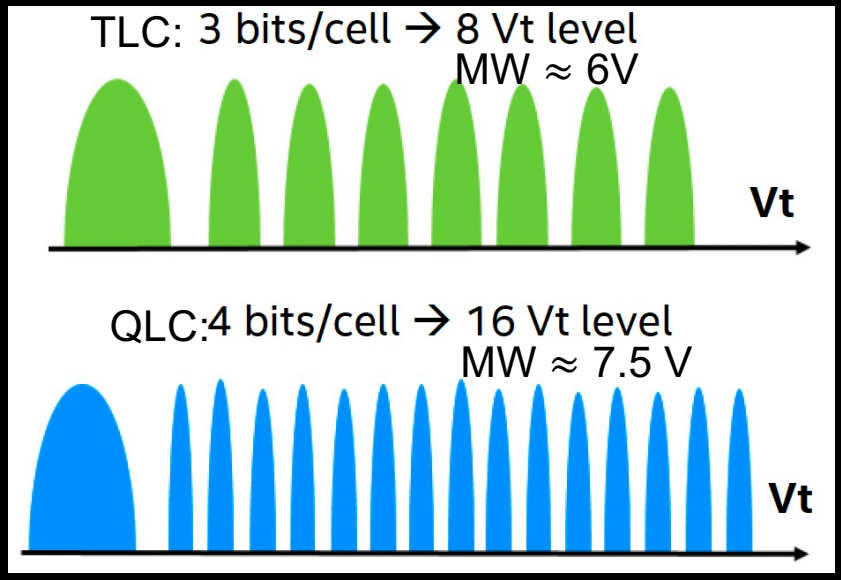
Cell-to-cell interference will significantly increase with aggressive Z-scaling for 1000L VNAND.

23

Ferroelectric as a replacement for Charge Trap Layer



To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm



Design constraints

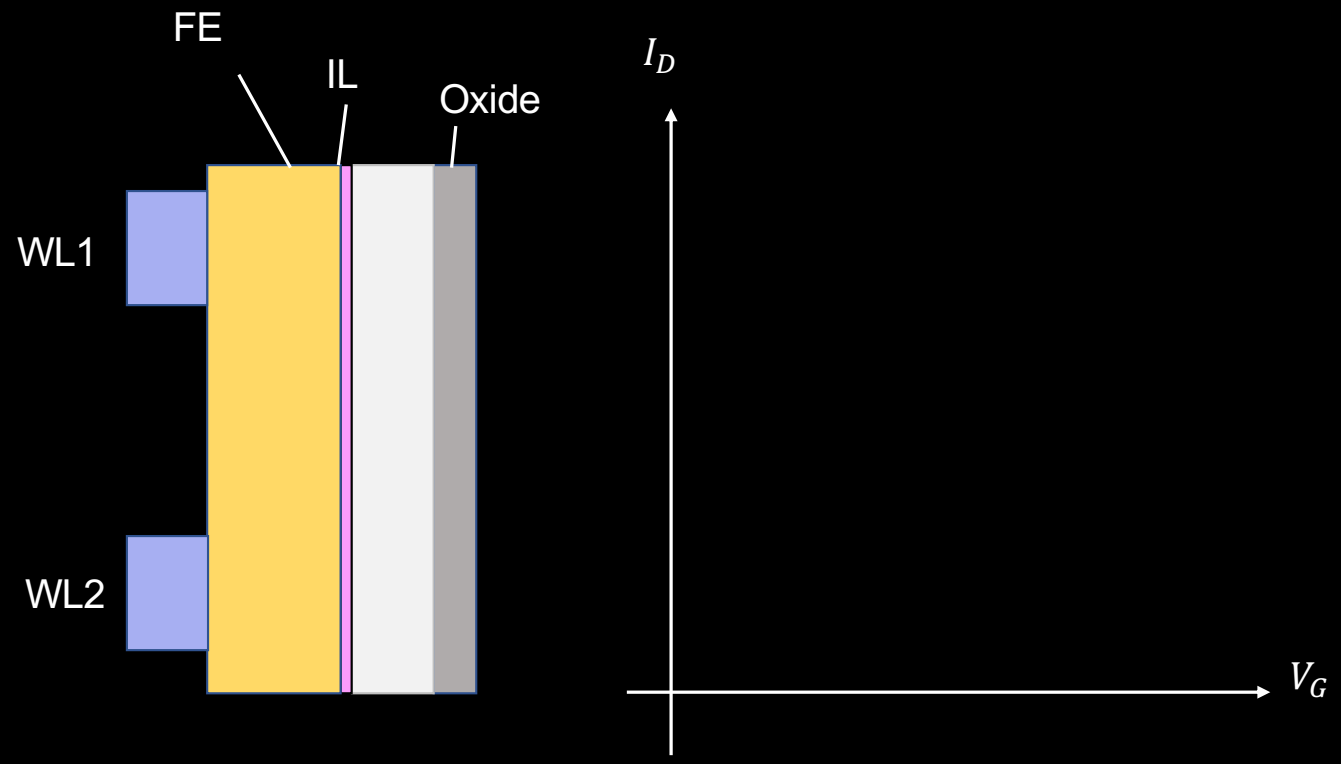
Ferroelectric thickness, $t_{FE} \leq 19$ nm

Write voltage ≤ 15 V

Memory window, MW ≥ 6.5 V

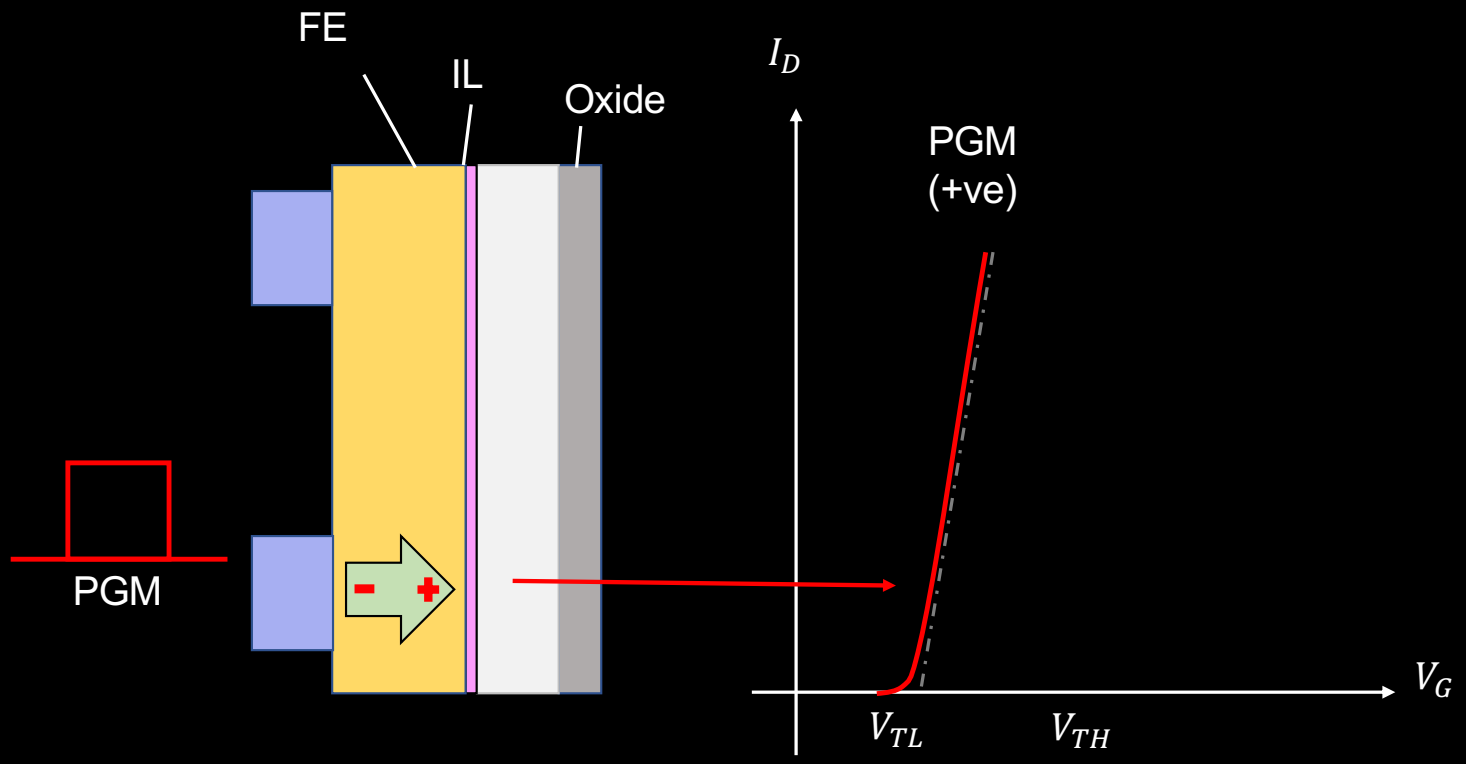
24

Ferroelectric field-effect transistor



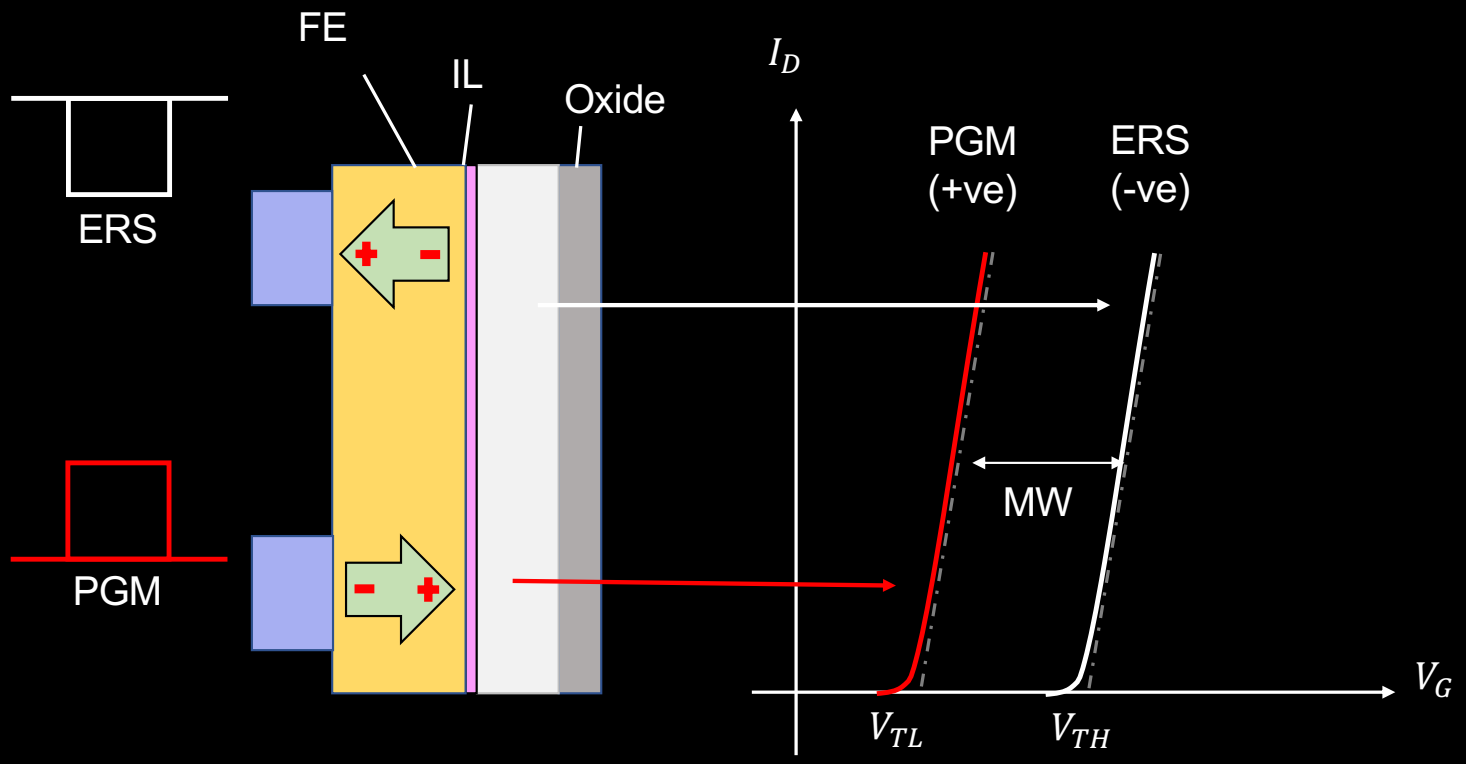
FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the “remnant” polarization.

Ferroelectric field-effect transistor



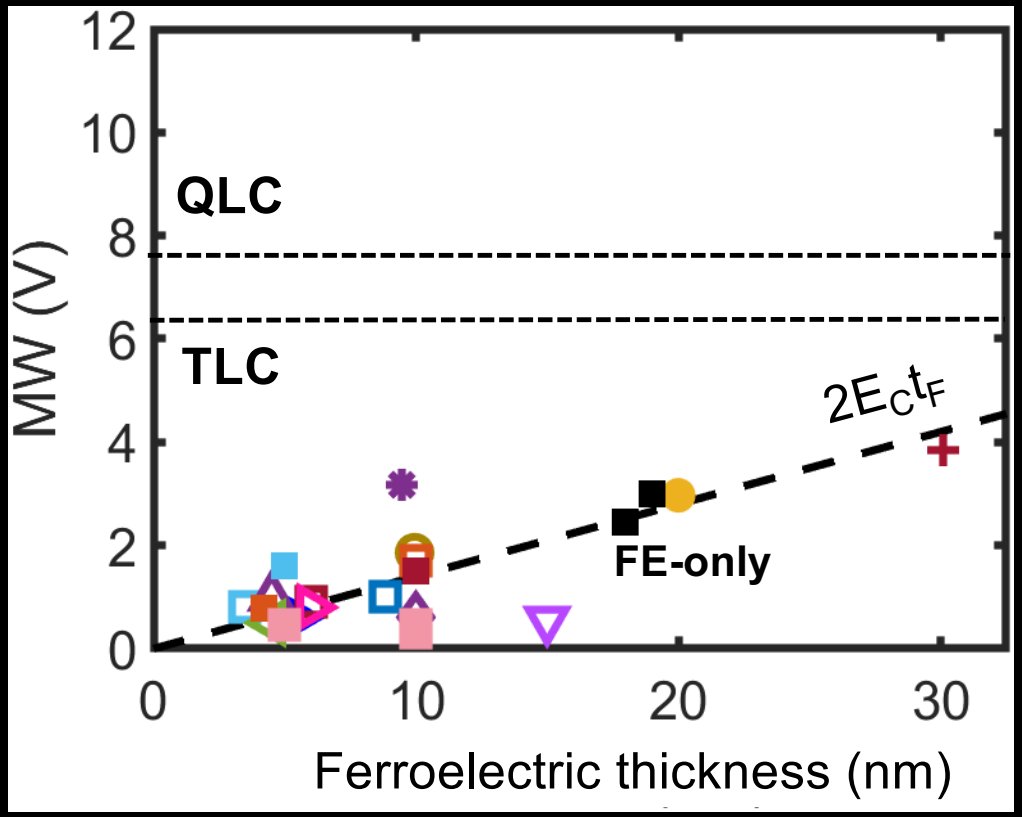
PGM (positive voltage) pulse sets the Vt to high Vt state in FEFET

Ferroelectric field-effect transistor



ERS (negative voltage) pulse sets the Vt to high Vt state in FEFET

“Fundamental limit” of memory window



Mueller et al. EDL, 2019.
Mulaosmanovic et al. TED, 2019.
Chan et al. ISAF, 2013.
Chatterjee et al. EDL, 2017.
Peng et al. EDL, 2019.
Mueller et al. EDL, 2019.
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Dutta et al. EDL, 2022.
Dunkel et al. IEDM, 2017.
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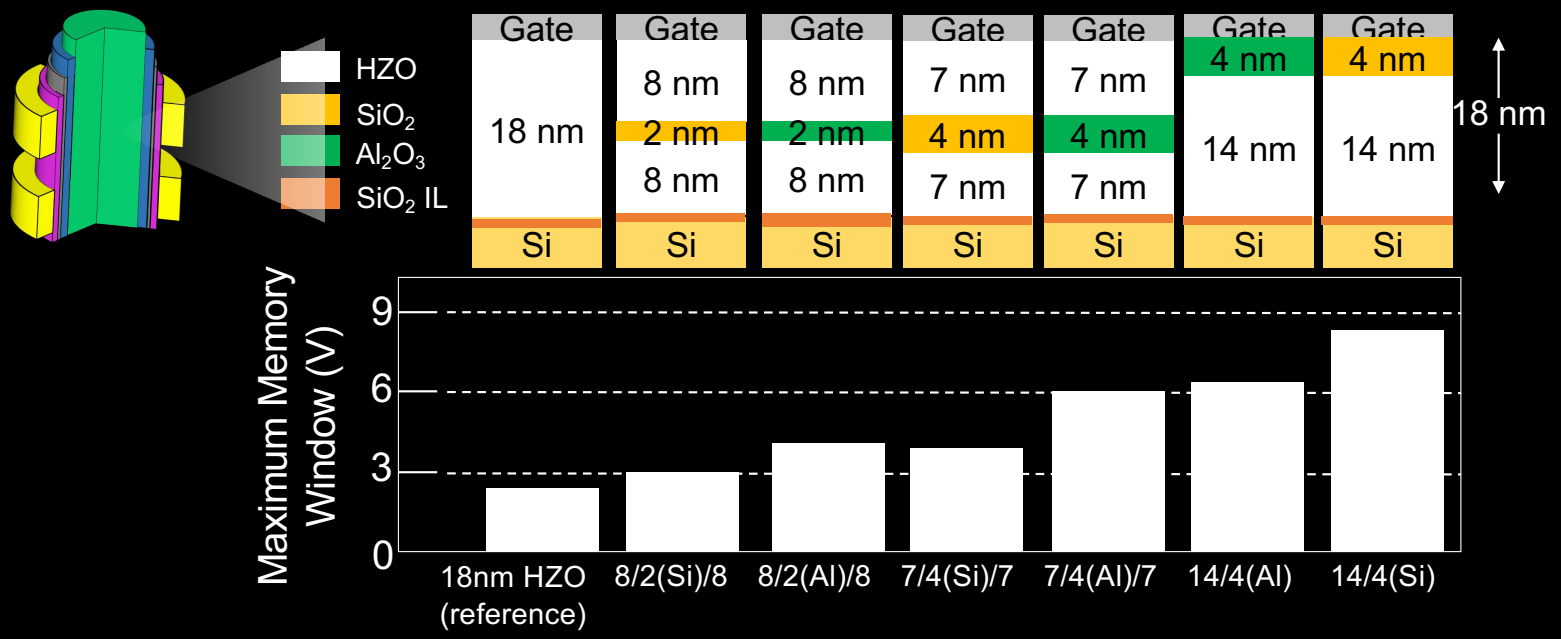
Tasneem et al. IEDM 2021.
Tasneem et al. EDL, 2021.
Khan group

Fundamental limit of the maximum memory window in a ferroelectric FET is $2E_c t_F$

How to engineer MW in FE gate stack?

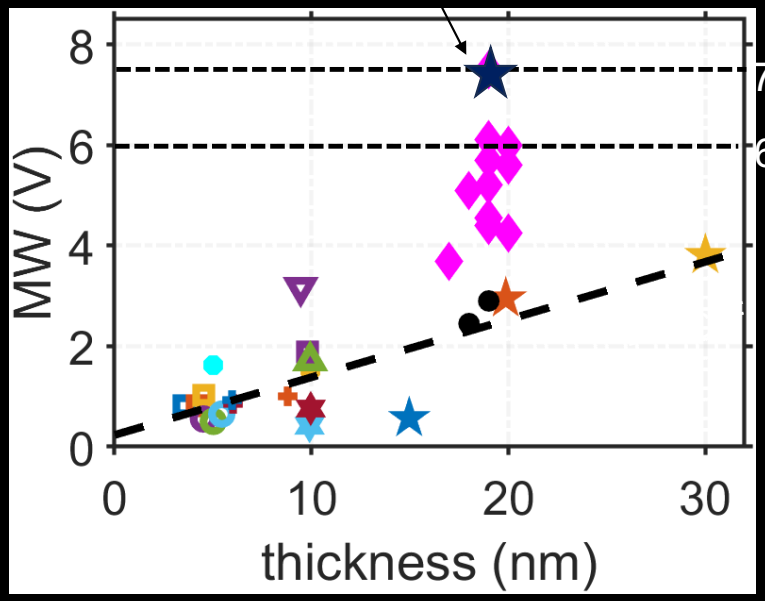


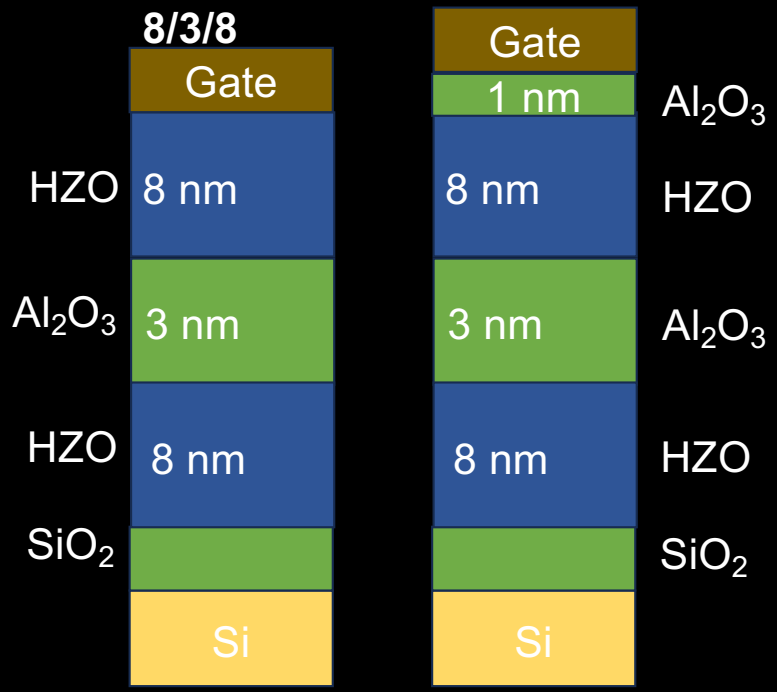
Fernandes, L., Ravindran, P. V., Song, T., Das, D., Park, C., Afroze, N., ... & Khan, A. (2024). Material choices for tunnel dielectric layer and gate blocking layer for ferroelectric NAND applications. *IEEE Electron Device Letters*.

Fernandes, L., Ravindran, P. V., Chen, J., Tian, M., Das, D., Chen, H., ... & Khan, A. (2024). Optimizing Memory Window for Ferroelectric Nand Applications: An Experimental Study on Dielectric Material Selection and Layer Positioning. *IEEE Transactions on Electron Devices*.

Engineered FEFETs for enhanced MW

8nm/3nm(Al_2O_3)/8nm/1nm(Al_2O_3) → **8/3/8/1**





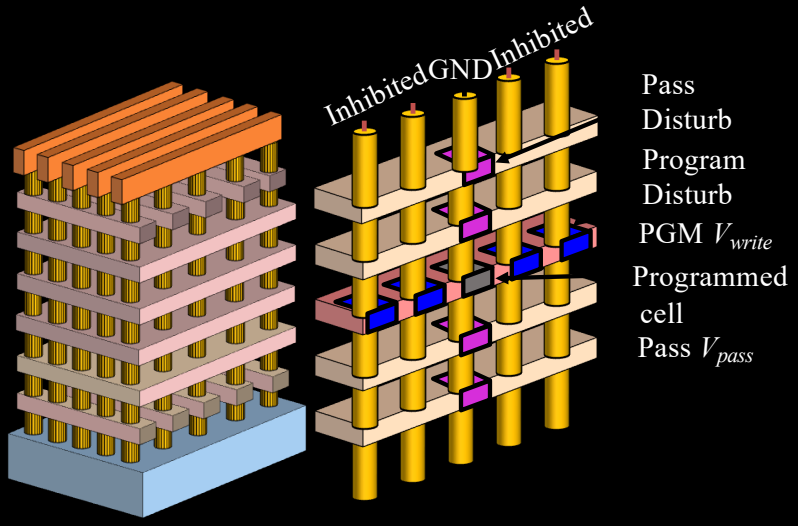
A ferroelectric-dielectric gate stack offers several tuning knobs to engineer the MW properties

Fernandes, L., Ravindran, P. V., Song, T., Das, D., Park, C., Afroze, N., ... & Khan, A. (2024). Material choices for tunnel dielectric layer and gate blocking layer for ferroelectric NAND applications. *IEEE Electron Device Letters*.

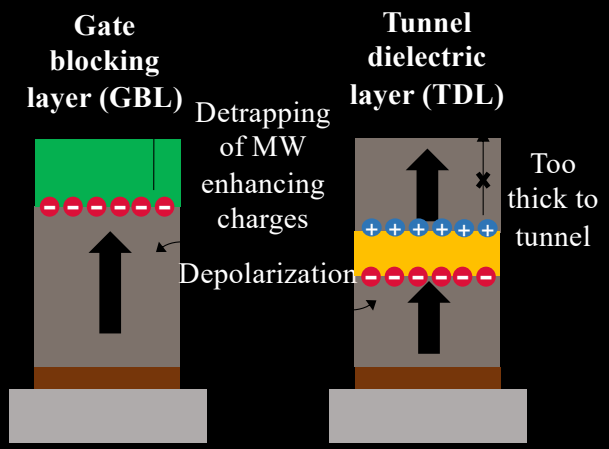
Fernandes, L., Ravindran, P. V., Chen, J., Tian, M., Das, D., Chen, H., ... & Khan, A. (2024). Optimizing Memory Window for Ferroelectric Nand Applications: An Experimental Study on Dielectric Material Selection and Layer Positioning. *IEEE Transactions on Electron Devices*.

Key challenges

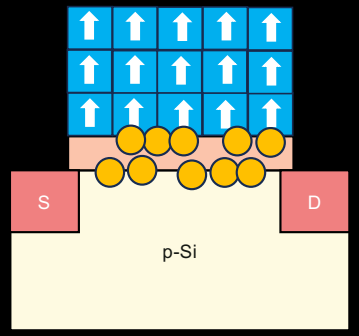
Disturb



Retention

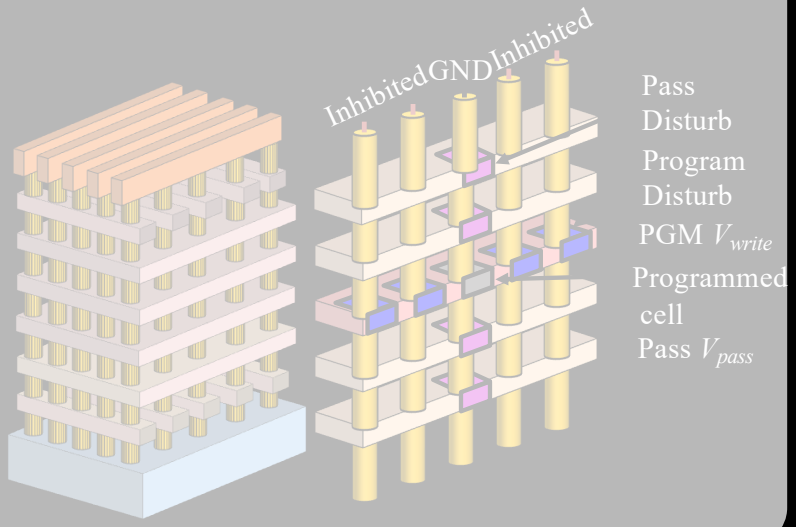


Write Endurance



Key challenges

Disturb



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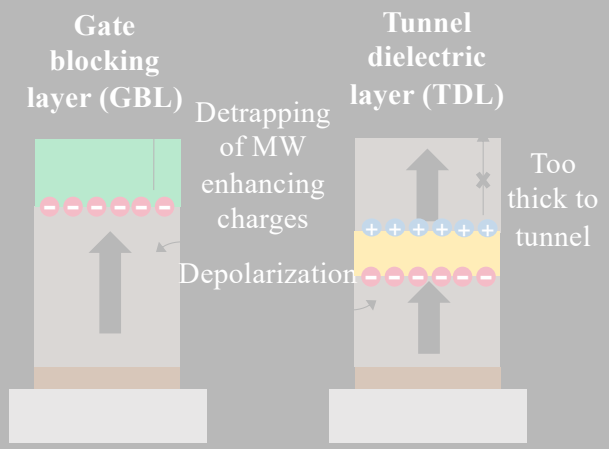
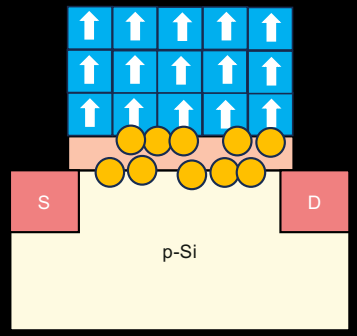
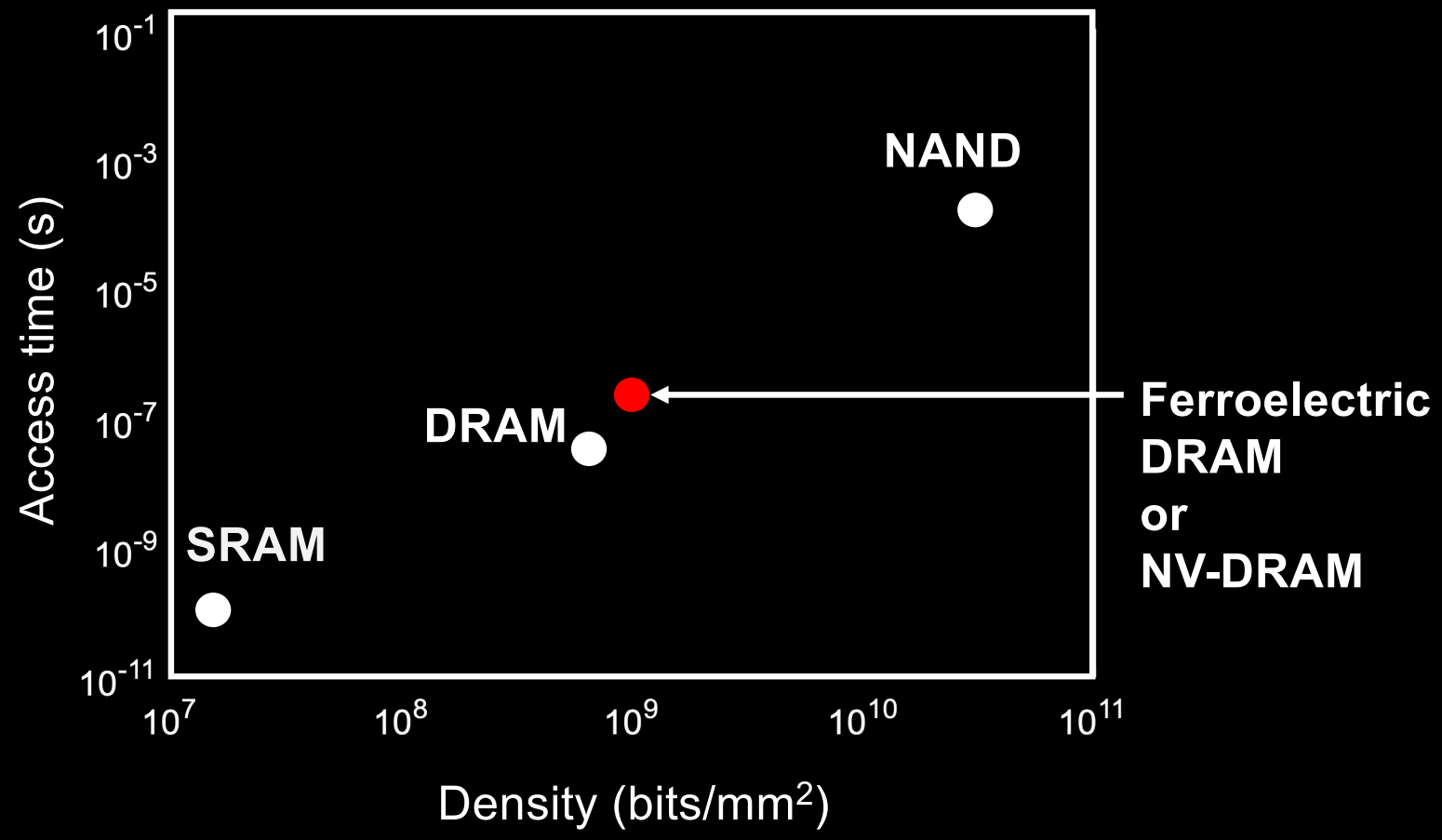


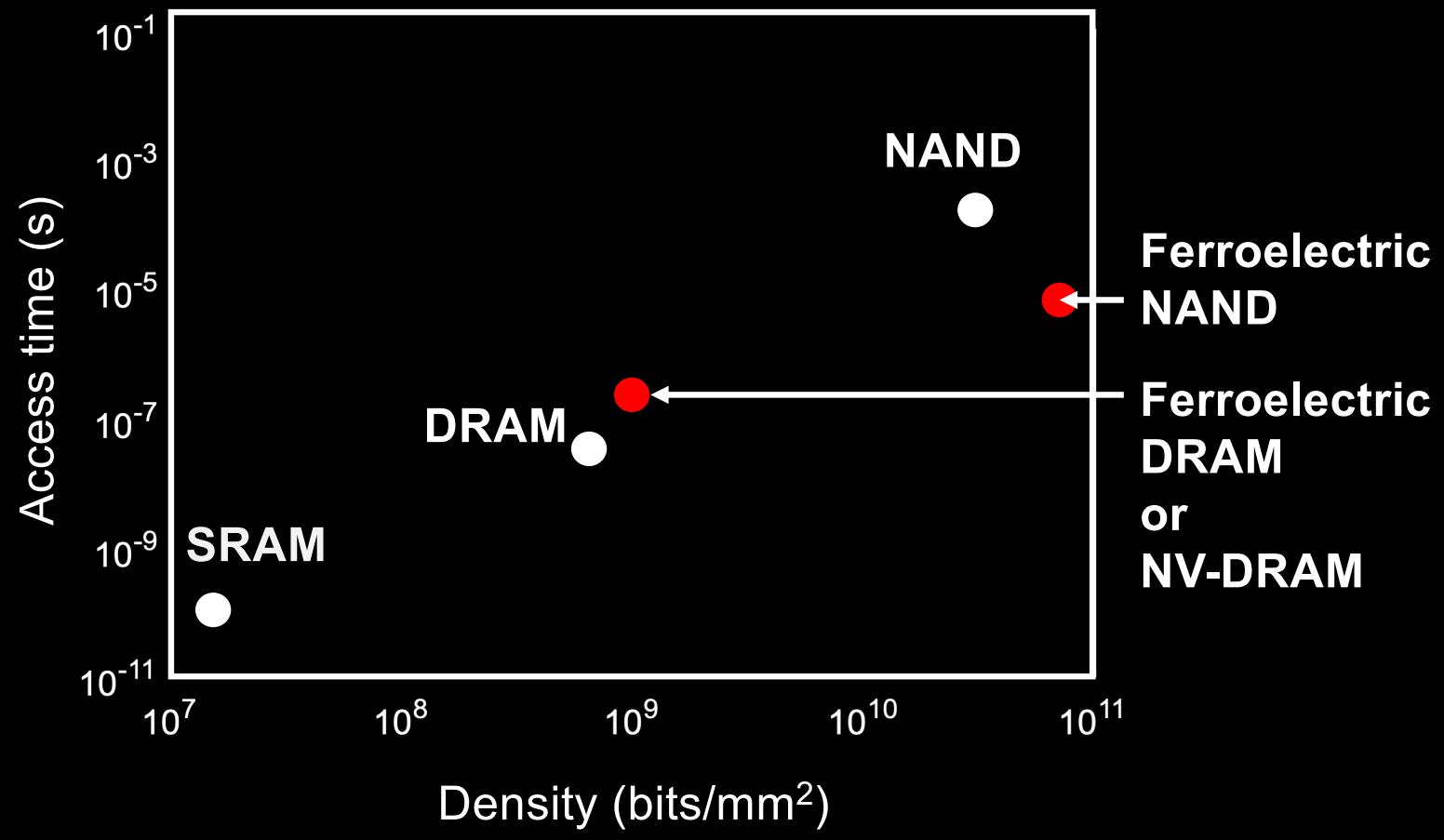
Write Endurance



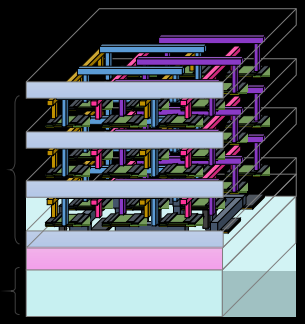
Memories of the future



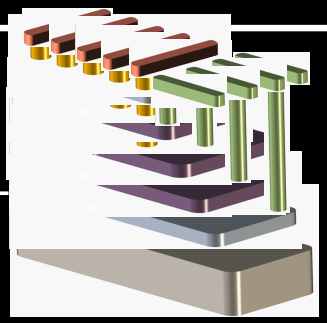
Memories of the future



Memories of the future



High-speed
Embedded
FEFET



NOR-Like
3D FEFET

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