Ferroelectrics for storage applications

Asif Khan

Associate Professor
School of Electrical and Computer Engineering
School of Materials Science and Engineering
Georgia Institute of Technology
akhan40@gatech.edu

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1/30/2025

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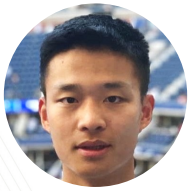
Our team


Nashrah Afroze


Priyankka Ravikumar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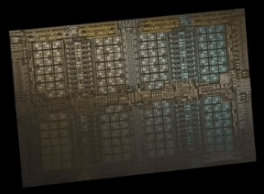
Memory technologies – The state of the art

Memory

Hyperscale AI and High-performance Computing



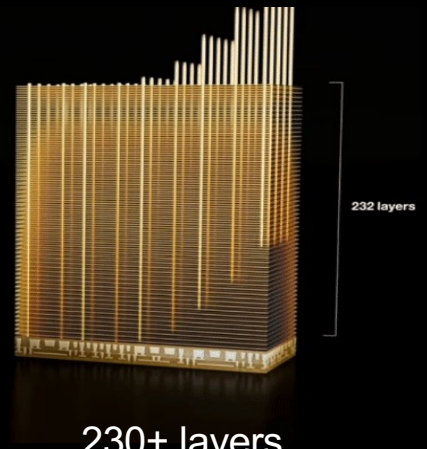
HBM3E: 12-high, 32 GB

1.18 TB/s

Source: NVIDIA

Storage

Client, Mobile, Enterprise



230+ layers

2.4 GB/s

Source: Micron

Embedded

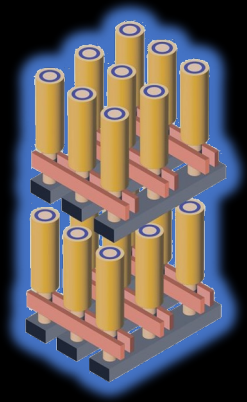
Automotive

14nm eMRAM

16 MB

Source: Forbes

Emerging Memory



Ferroelectric NV-DRAM

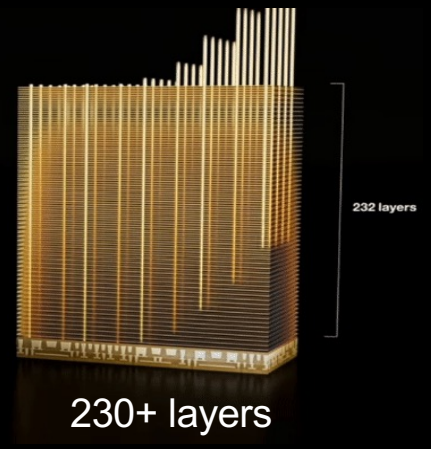
32 Gb, 3D-stacked, multi-layer

Source: IEDM 2023

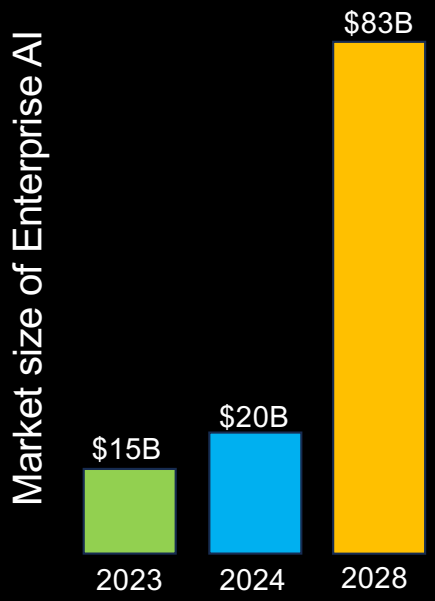
The NAND Storage Technology

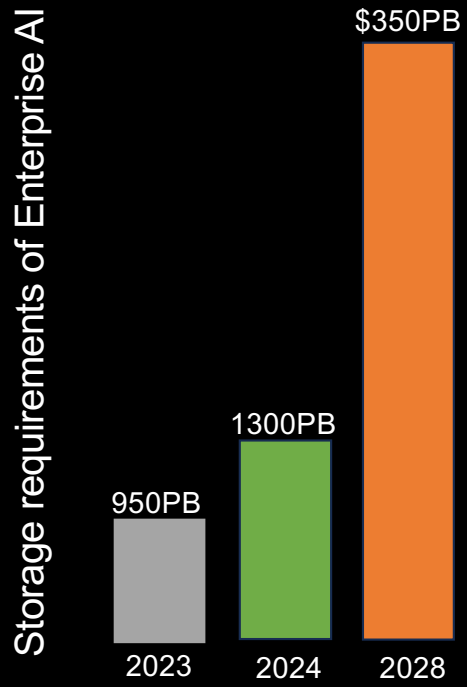
Storage

Client, Mobile, Enterprise



Source: Micron

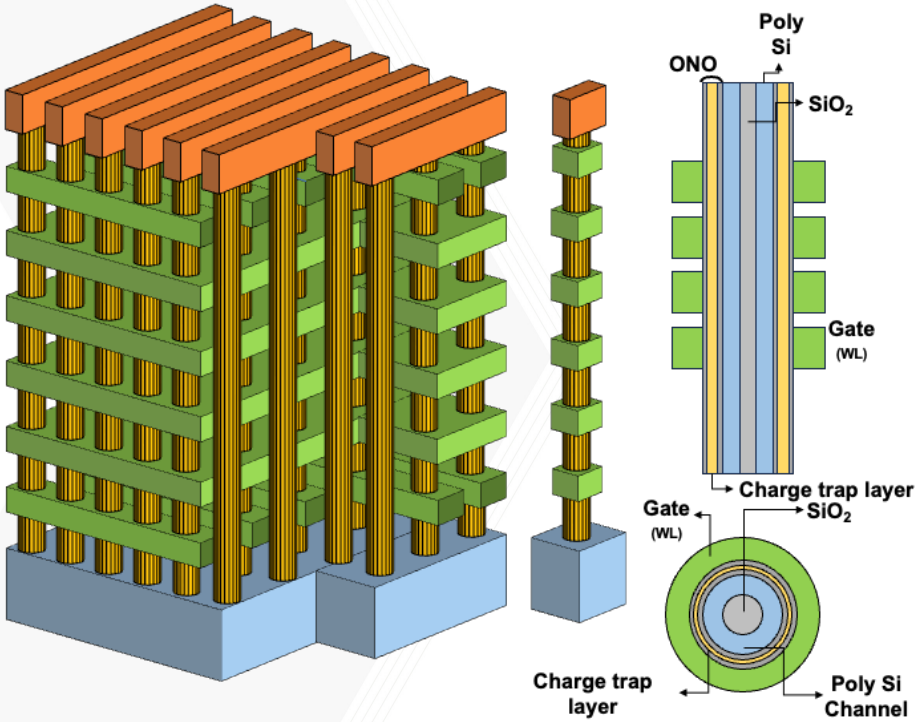


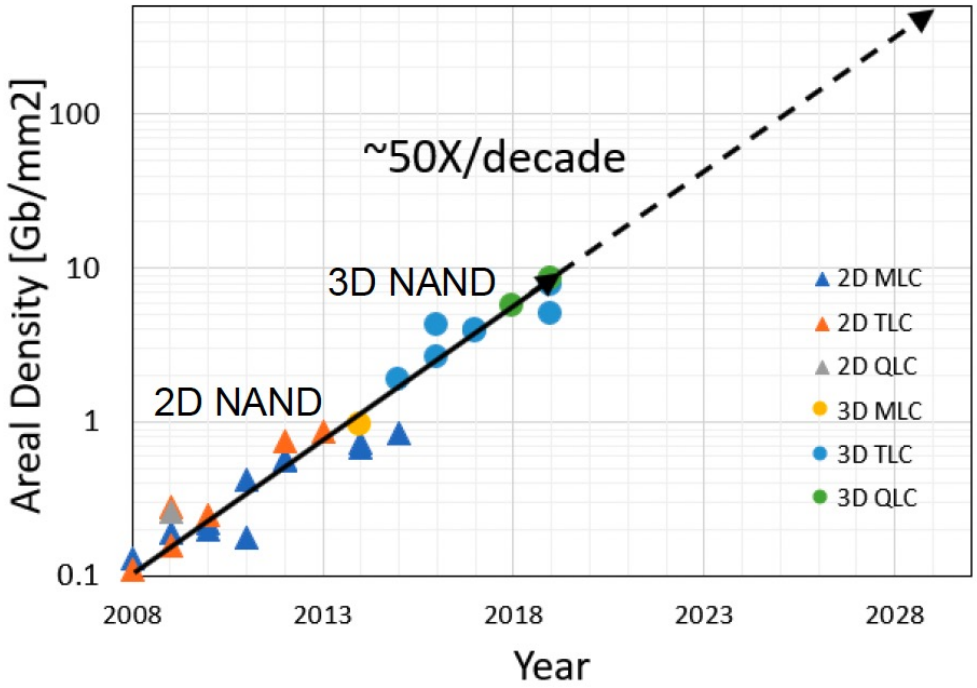


Source: The Business Research Company

Processing and storing data in AI effectively and cost efficiently can require HBM for the actual AI training, but also various types of NAND-based solid-state storage to support the data flows needed to and from the HBM.

Vertical NAND Scaling





A. Goda, IEEE, TED 2020

Relentless innovations have led to a 50x improvement in bit areal density per decade.

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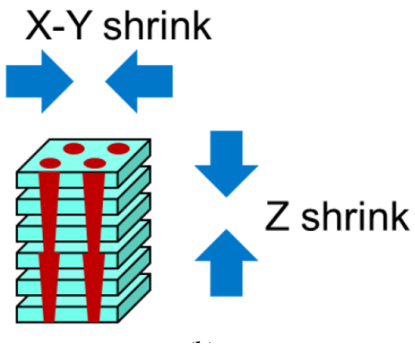
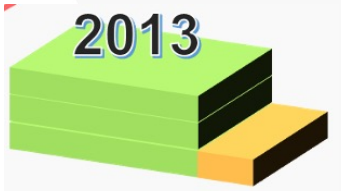
Vertical NAND Scaling

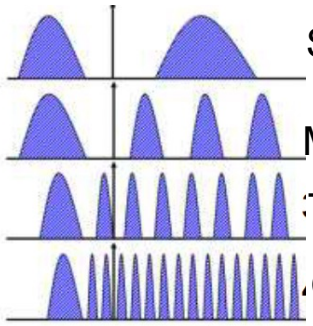
Physical scaling

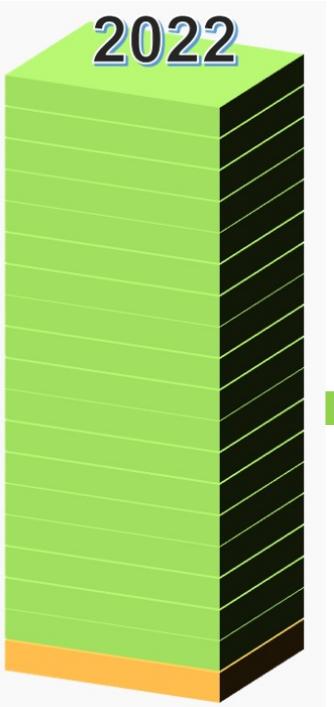




Samsung 24L MLC

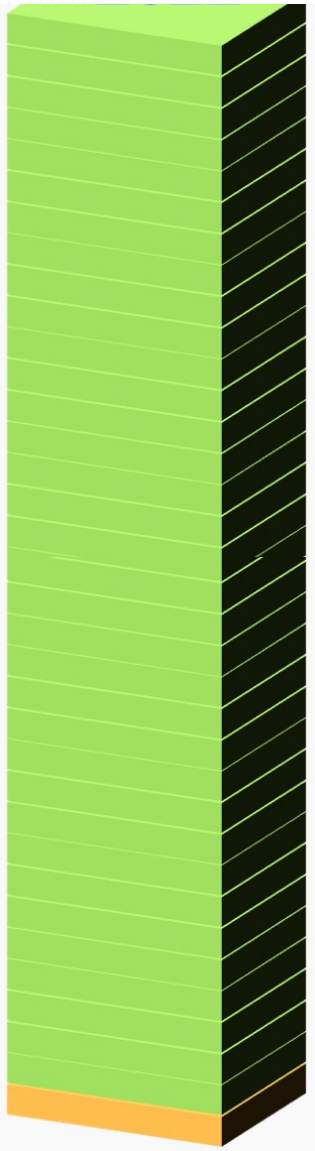
Logical scaling





Samsung 236L TLC
SK Hynix 238L TLC
Micron 232L TLC
192L QLC

?



Vertical NAND scaling toward 1000 layers

Layer stacking trend

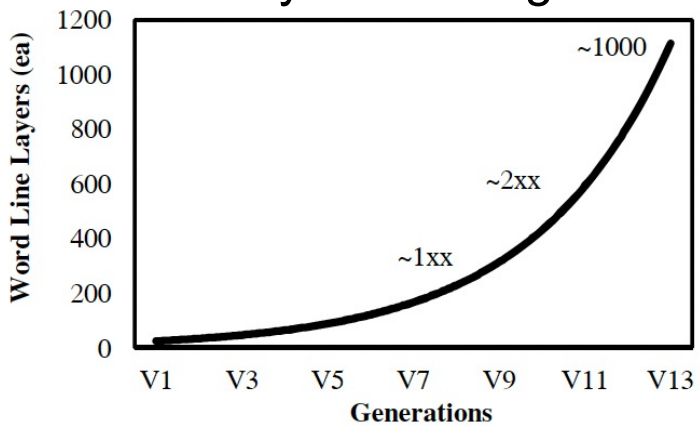


Fig. 1. Number of word line layers by generation

Package thickness limits the NAND chip height.

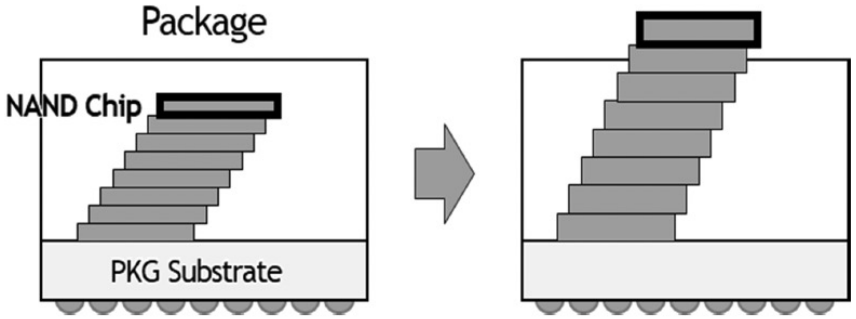
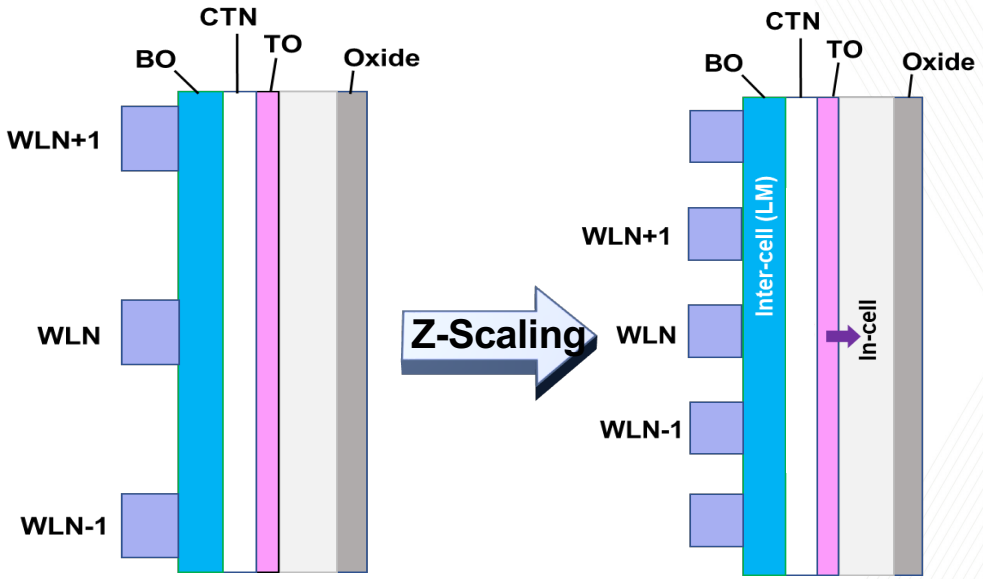


Fig. 4. Package thickness limit with multiple chips

Aggressive Z-scaling is required.

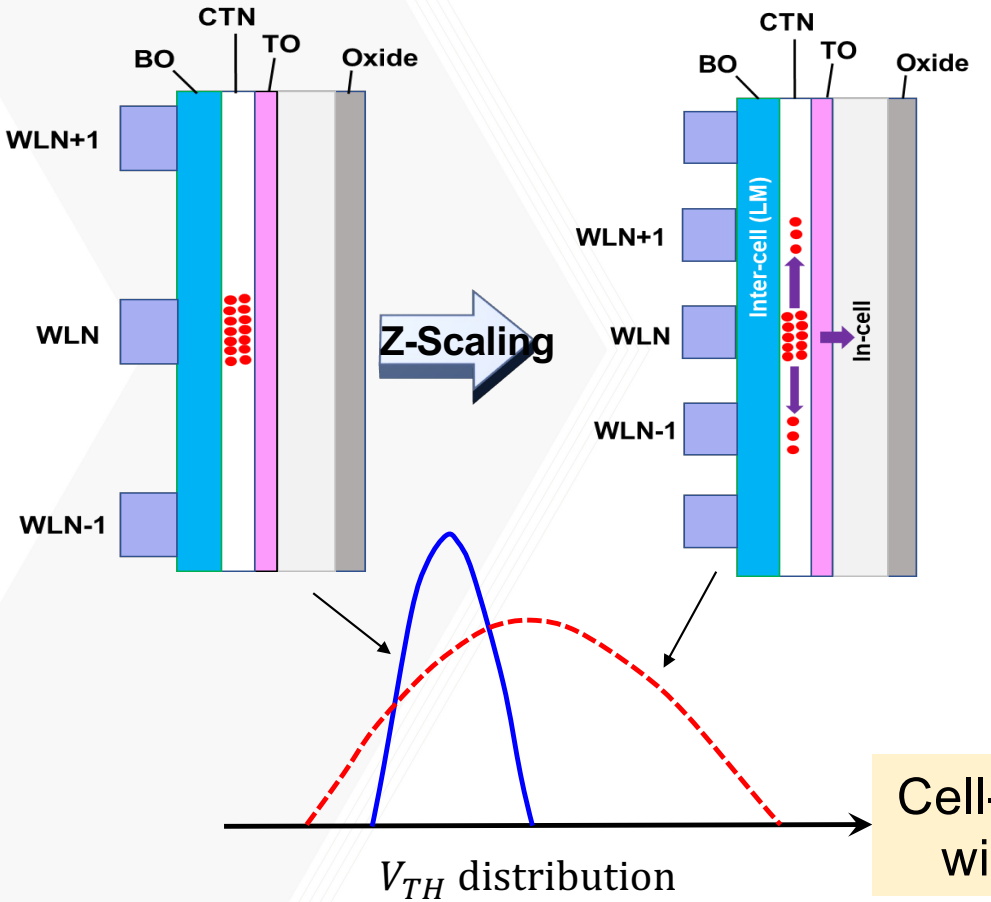


The mold height (cell height) needs to be reduced dramatically.

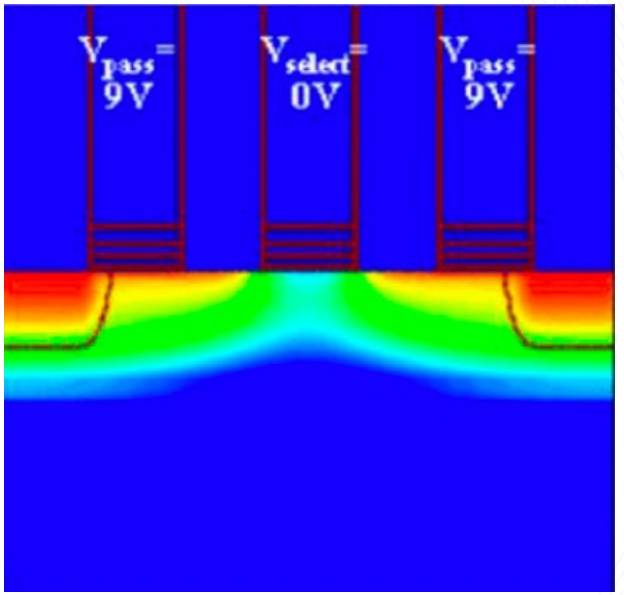
Han et al. Fundamental Issues in VNAND Integration Toward More Than 1K Layers. IEDM 2023. Paper 35.1

Challenges for 1000+ layer vertical NAND

1 Lateral charge migration



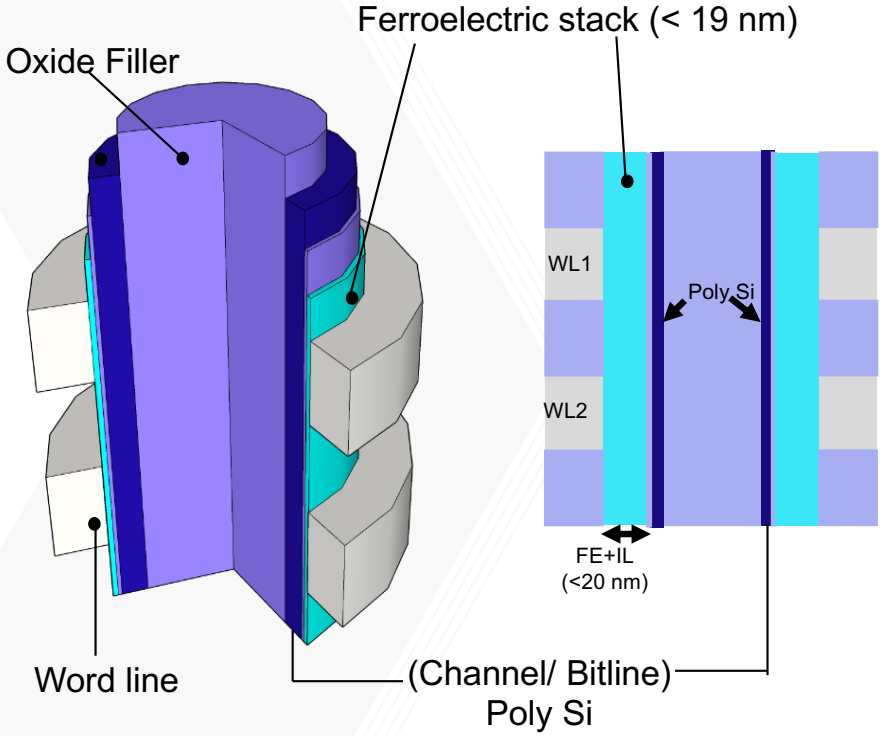
2 High write voltage



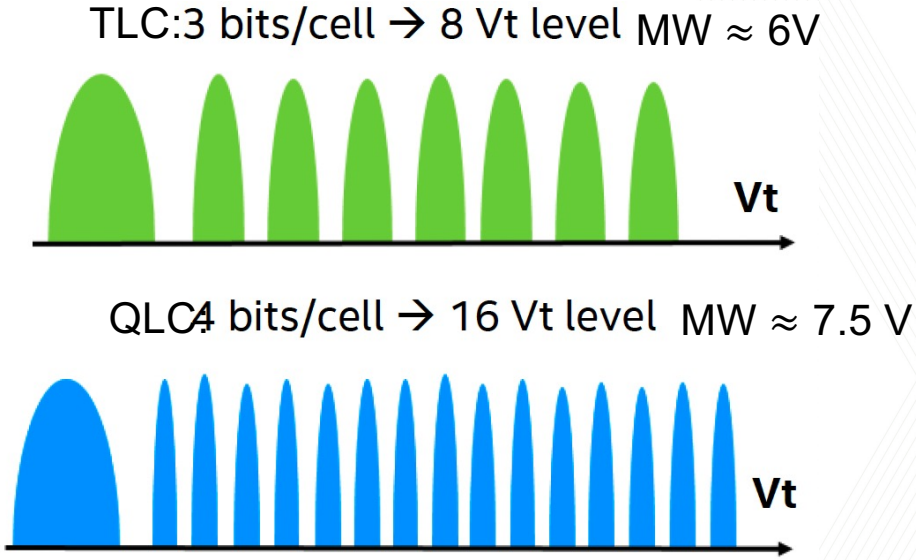
Write voltage of state of the art NAND is >20 V.
Large write voltage affects effective threshold voltage, similar to cell-to-cell interference.

Cell-to-cell interference will significantly increase with aggressive Z-scaling for 1000L VNAND.

Ferroelectric as a replacement for Charge Trap Layer



To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm



Design constraints

Ferroelectric thickness, $t_{FE} \leq 19$ nm

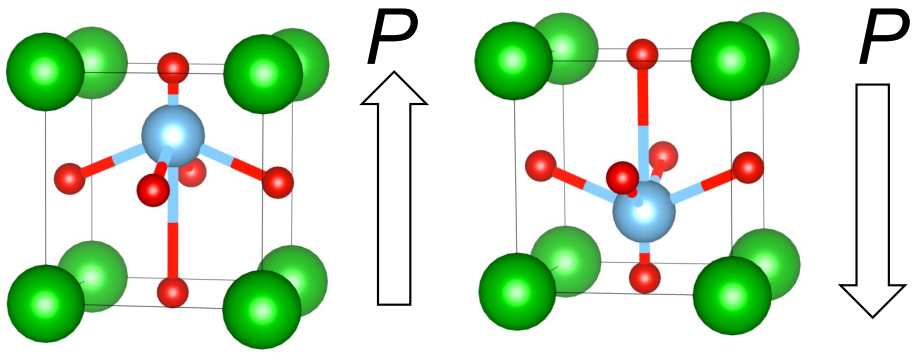
Write voltage ≤ 15 V

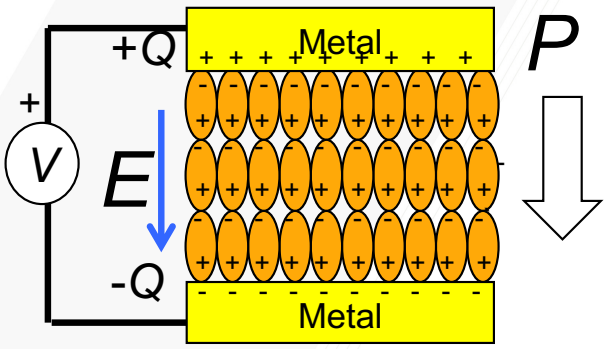
Memory window, MW ≥ 6.5 V

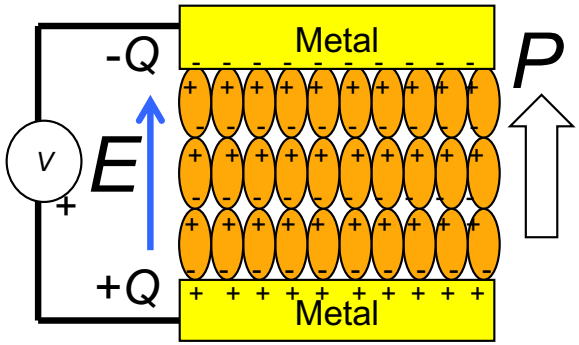
Ferroelectricity

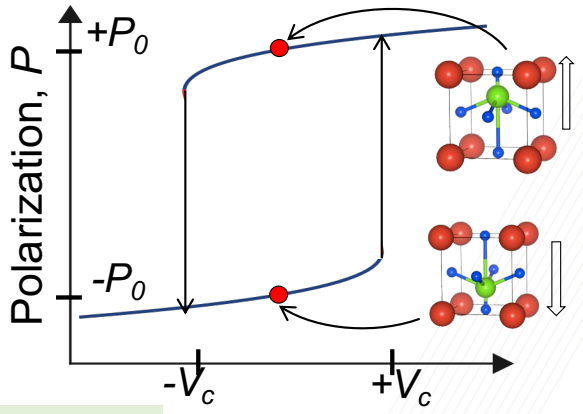
Classical Ferroelectric
$PbTiO_3$, $BaTiO_3$ etc.

Emerging CMOS compatible
Ferroelectrics:
Doped HfO_2









A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

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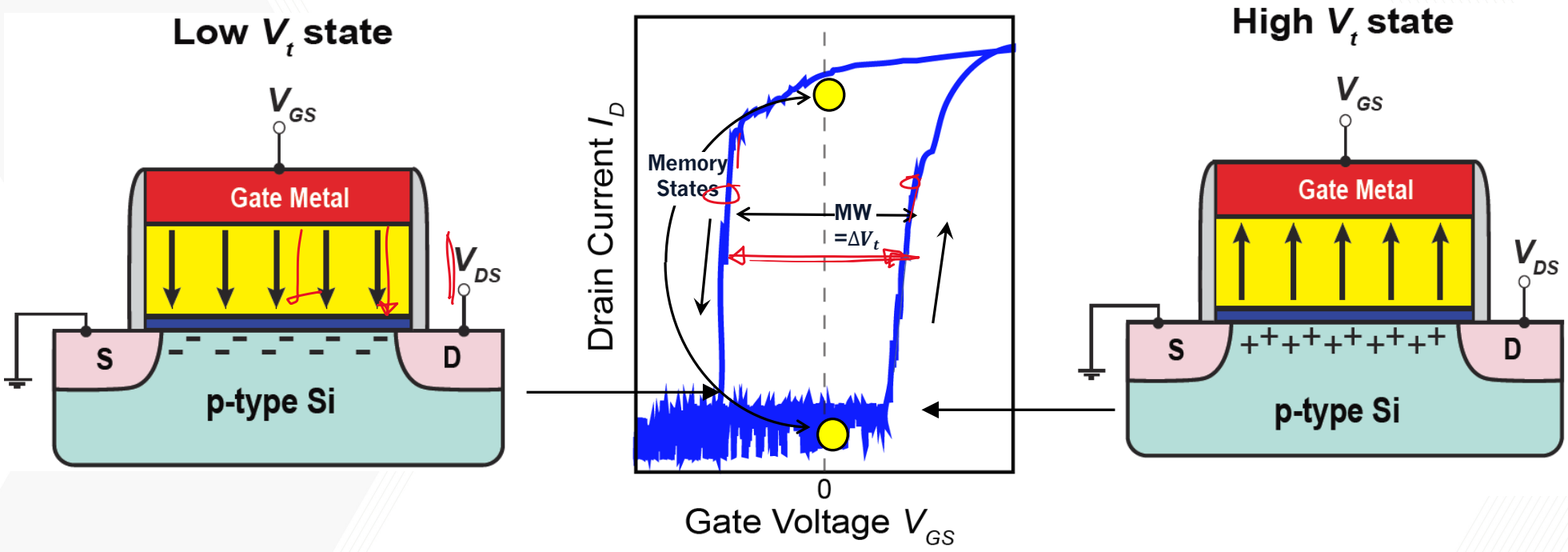
Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the “remnant” polarization.

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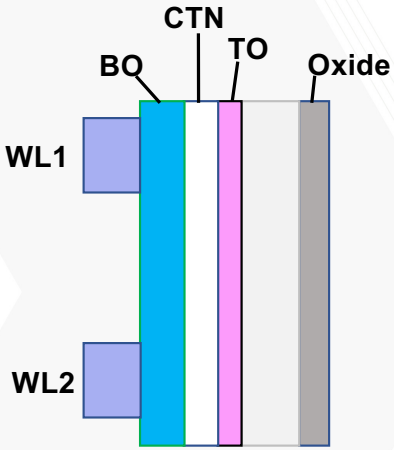
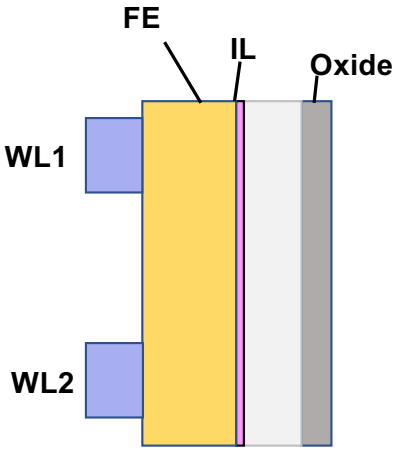
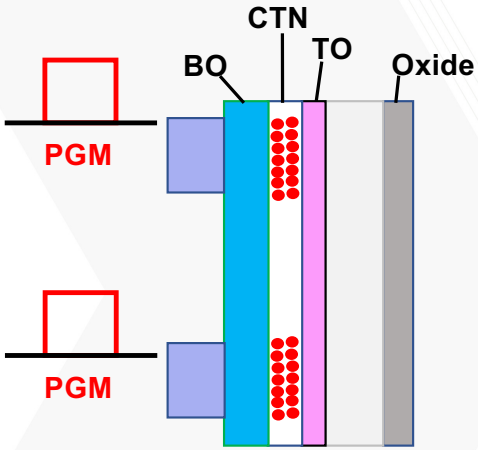
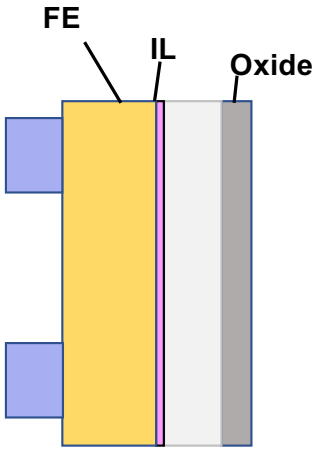
CTF vs FEFET





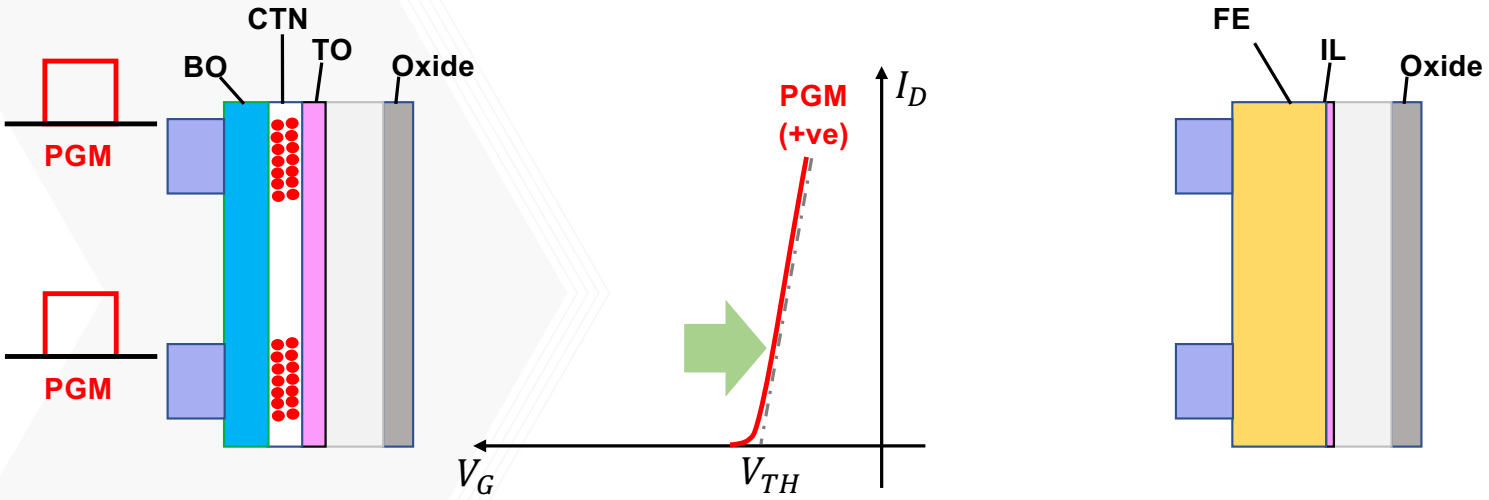
CTF vs FEFET (Program)





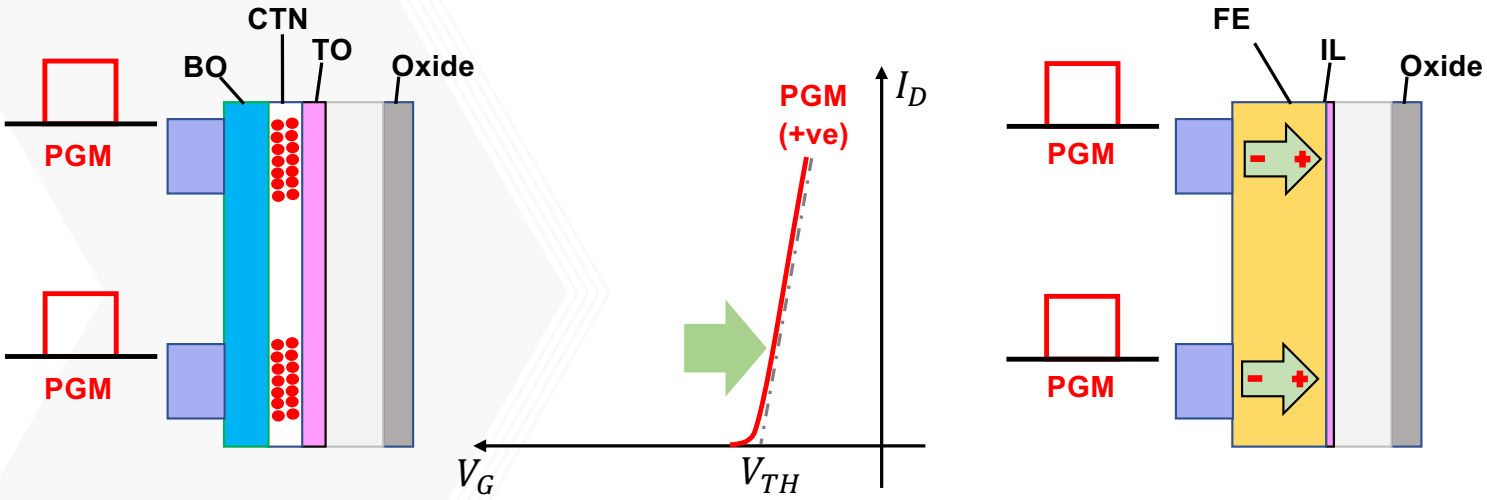
CTF that stores data in the form of charge

CTF vs FEFET (Program)



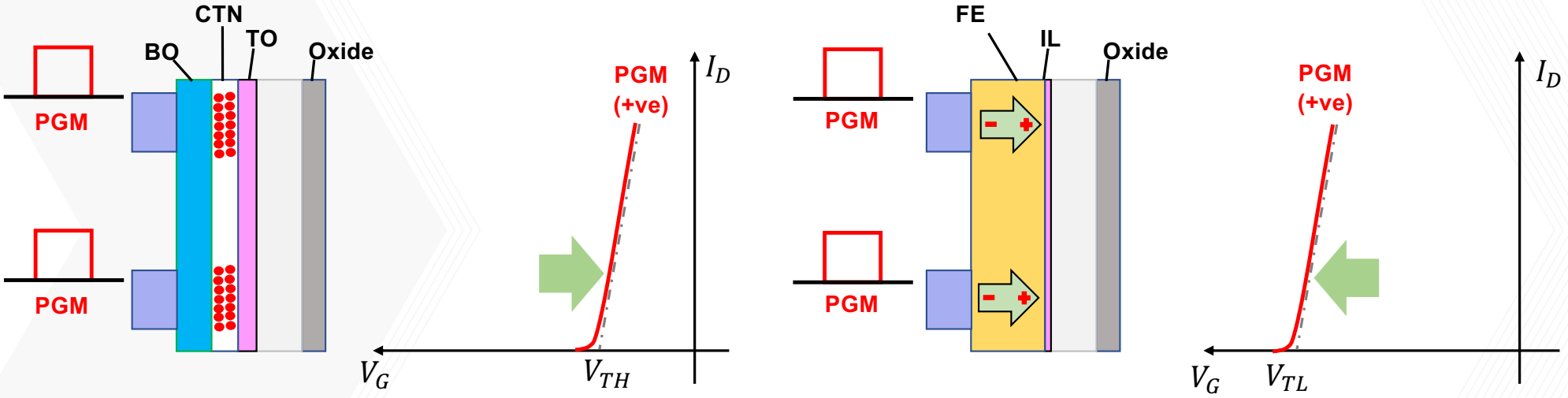
Positive PGM pulse sets the Vt to high Vt state in CTF

CTF vs FEFET (Program)



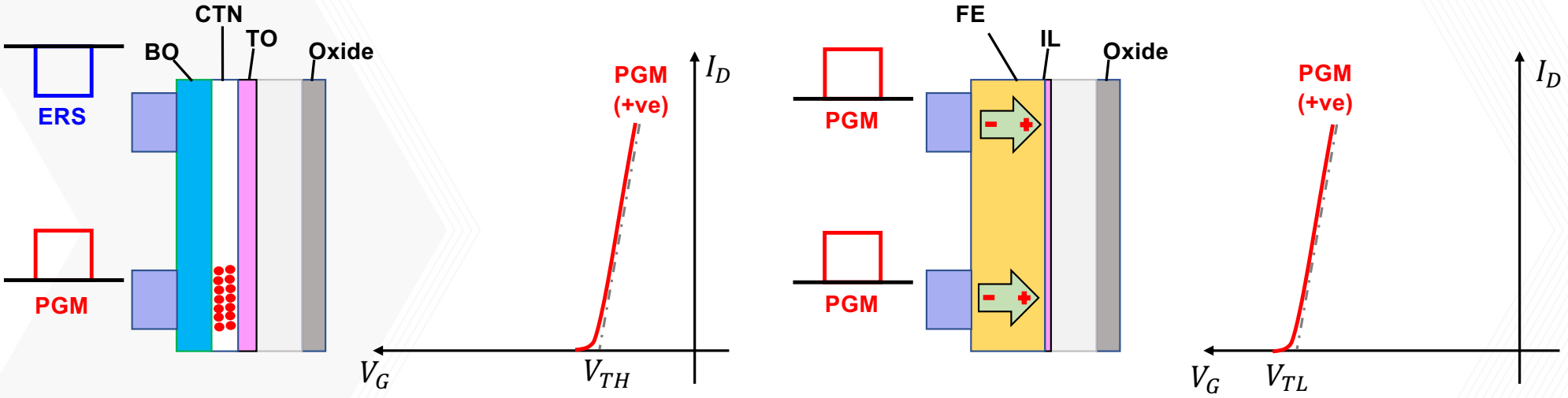
Positive PGM pulse sets the Vt to high Vt state in CTF

CTF vs FEFET (Program)



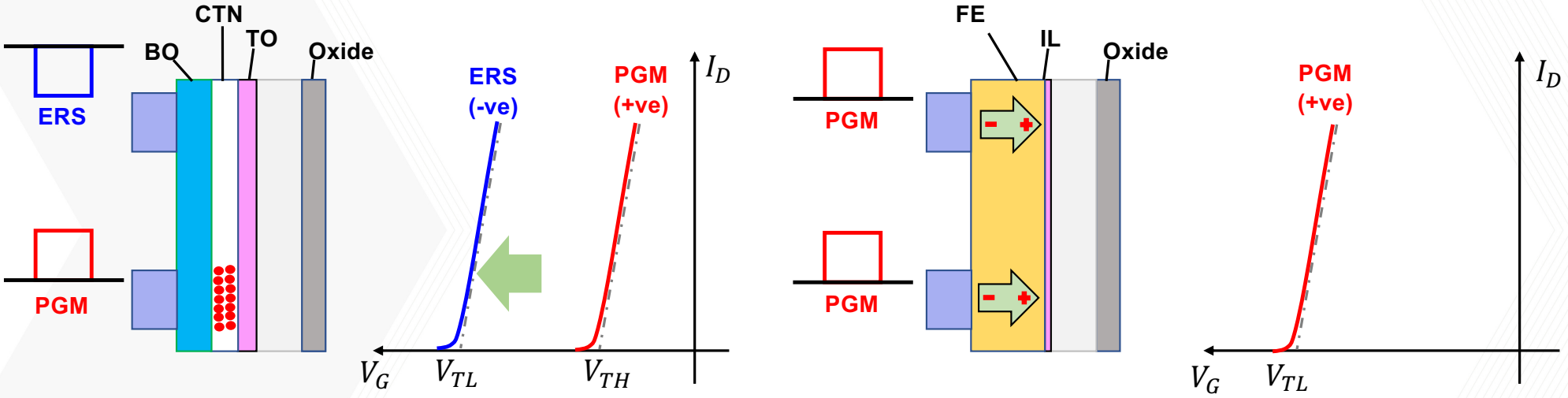
On the contrary, Positive PGM pulse sets the Vt to low Vt state in FEFET

CTF vs FEFET (Erase)



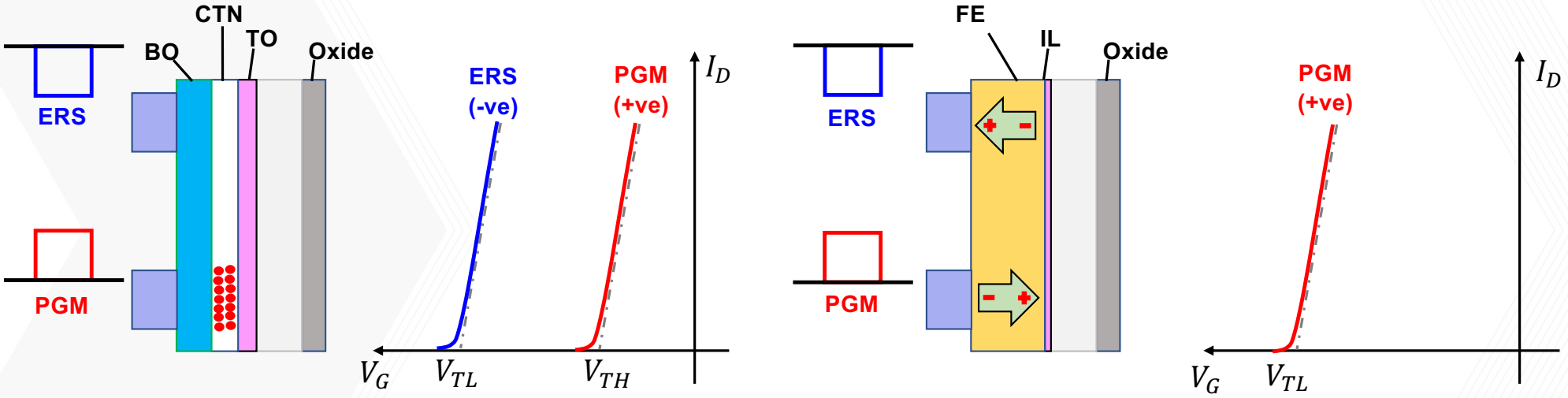
Negative ERS pulse sets the Vt to low Vt state in CTF

CTF vs FEFET (Erase)



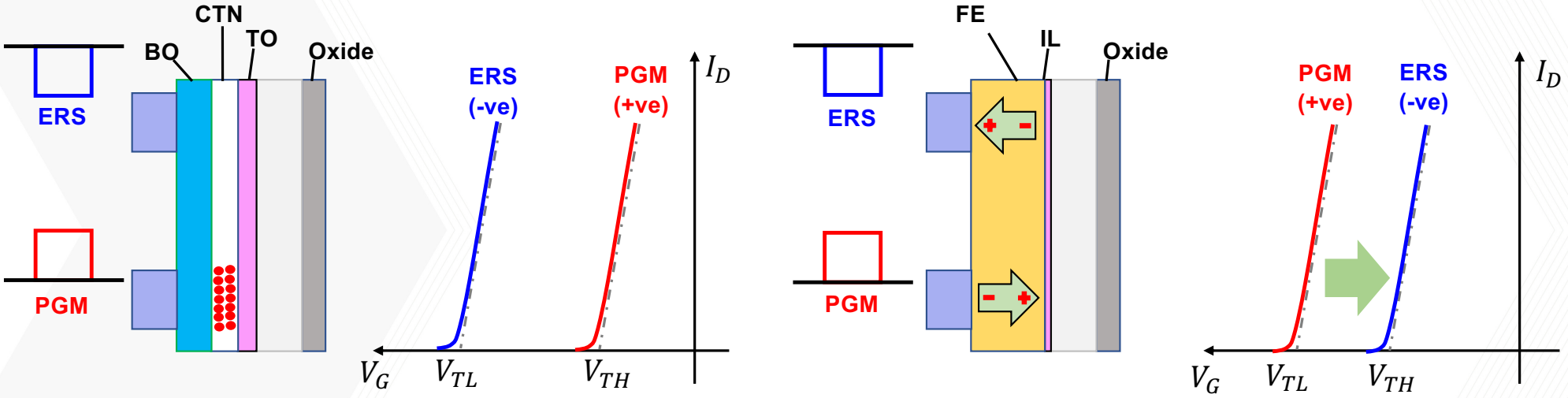
Negative ERS pulse sets the Vt to low Vt state in CTF

CTF vs FEFET (Erase)



Negative ERS pulse sets the Vt to high Vt state in FEFET

CTF vs FEFET (Erase)



Negative ERS pulse sets the Vt to high Vt state in FEFET

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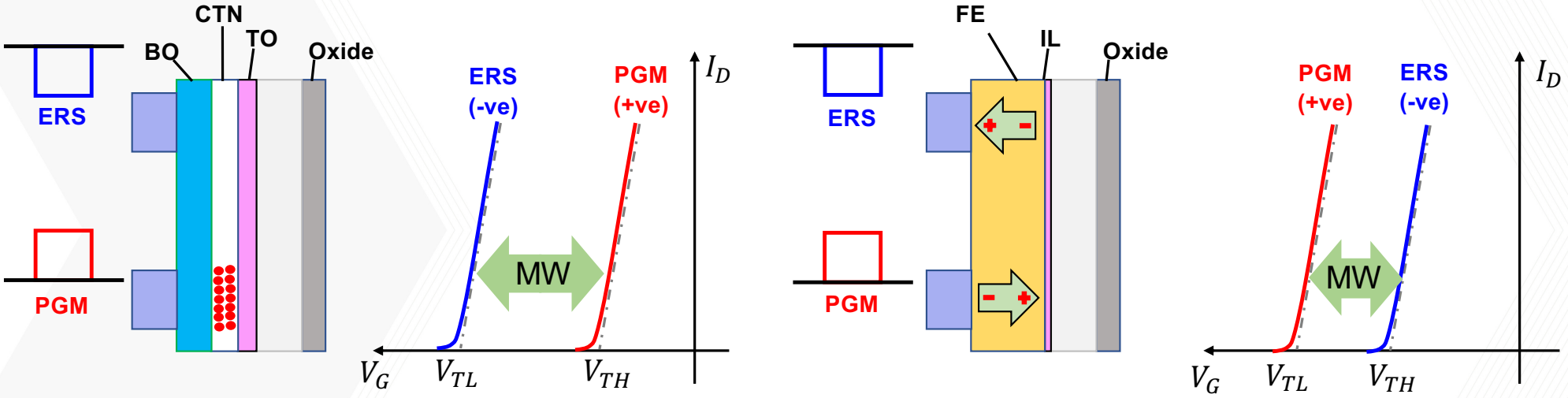
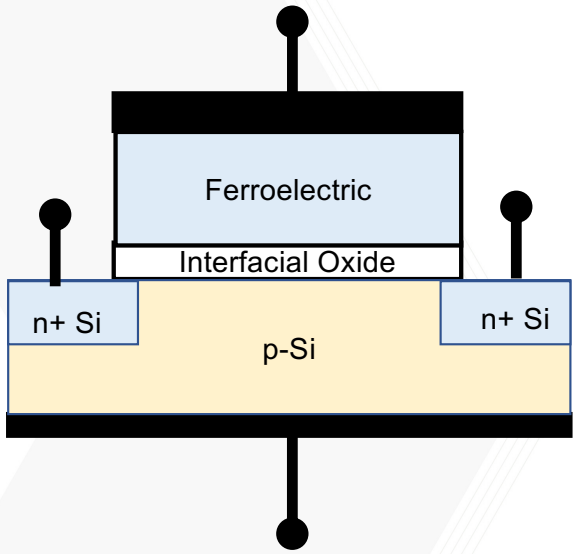
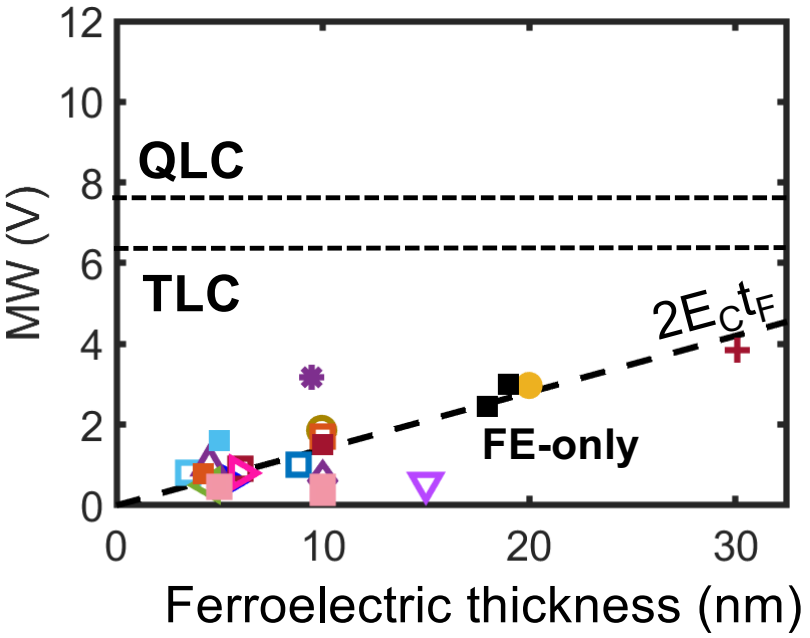
CTF vs FEFET (MW)



$$MW = V_{TH} - V_{TL}$$

“Fundamental limit” of memory window





- Mueller et al. EDL, 2019.
- Mulaosmanovic et al. TED, 2019.
- Chan et al. ISAF, 2013.
- Chatterjee et al. EDL, 2017.
- Peng et al. EDL, 2019.
- Mueller et al. EDL, 2019.
- Yurchuk et al. IRPS, 2014.
- Chan et al. ISAF, 2013.
- Mueller et al. EDL, 2019.
- Mulaosmanovic et al. TED, 2019.
- Wang et al. APL, 2020.
- Tan et al. EDL, 2021.
- Tan et al. VLSI, 2020.
- Das et al. EDL, 2022.
- Dutta et al. EDL, 2022.
- Dunkel et al. IEDM, 2017.
- Nguyen et al. EDL, 2021.
- Liu et al. EDL, 2019.
- Zacharaki et al. ACS AEM, 2022.
- Tasneem et al. IEDM 2021.
- Tasneem et al. EDL, 2021.
- Khan group

Fundamental limit of the maximum memory window in a ferroelectric FET is $2E_c t_F$.

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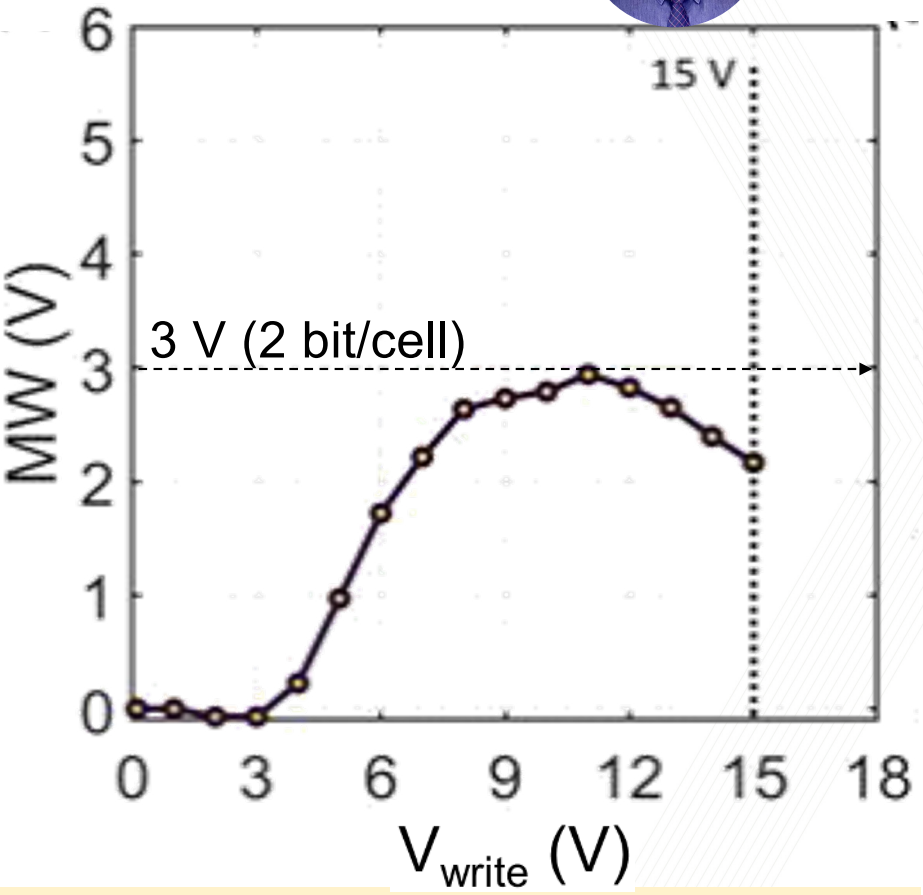
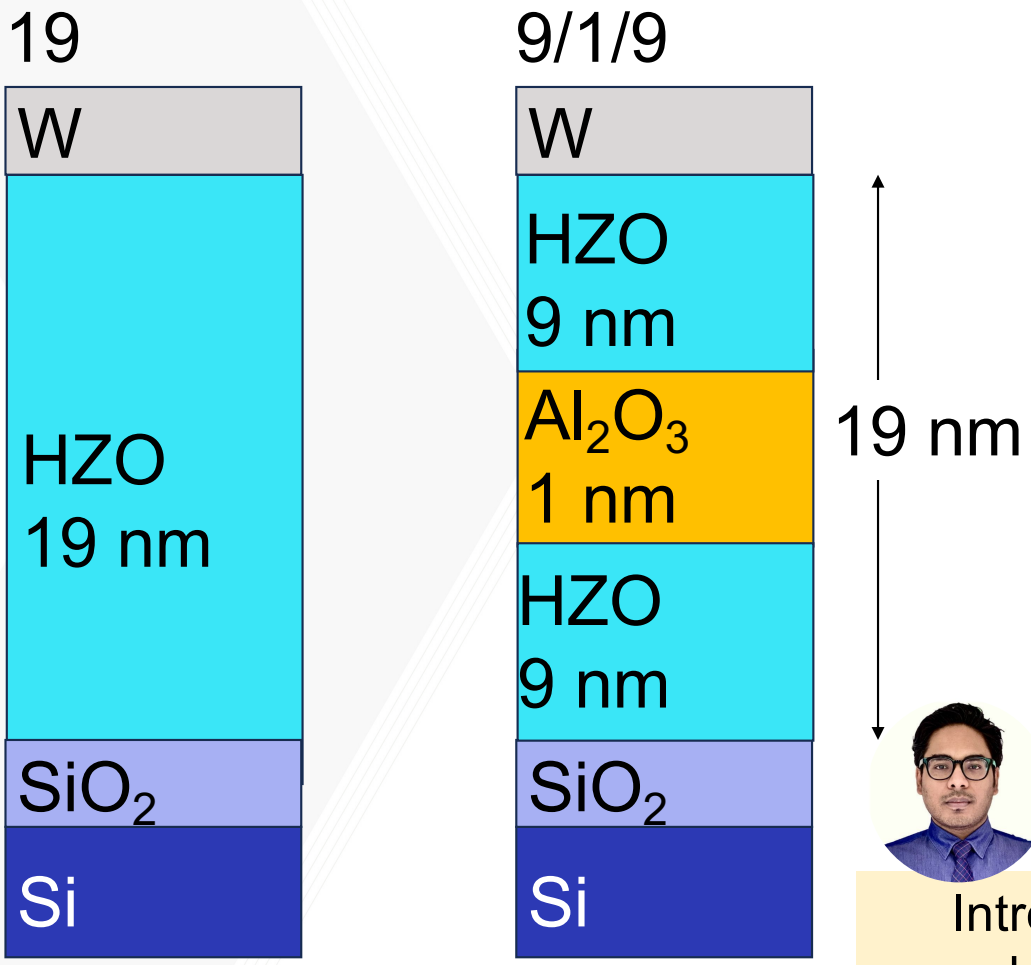
Impact of tunnel dielectric insertion

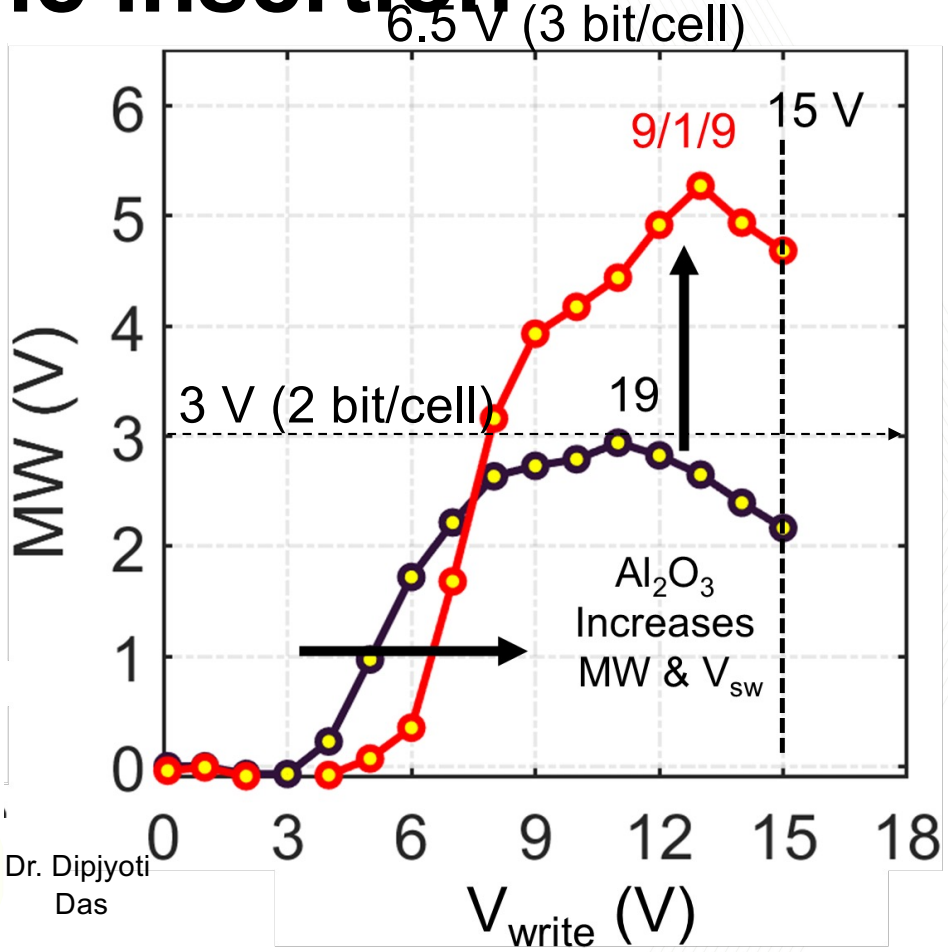
Dr. Dipjyoti Das



10 nm HZO layer leads to maximum memory window of 2.9 V.

Impact of tunnel dielectric insertion

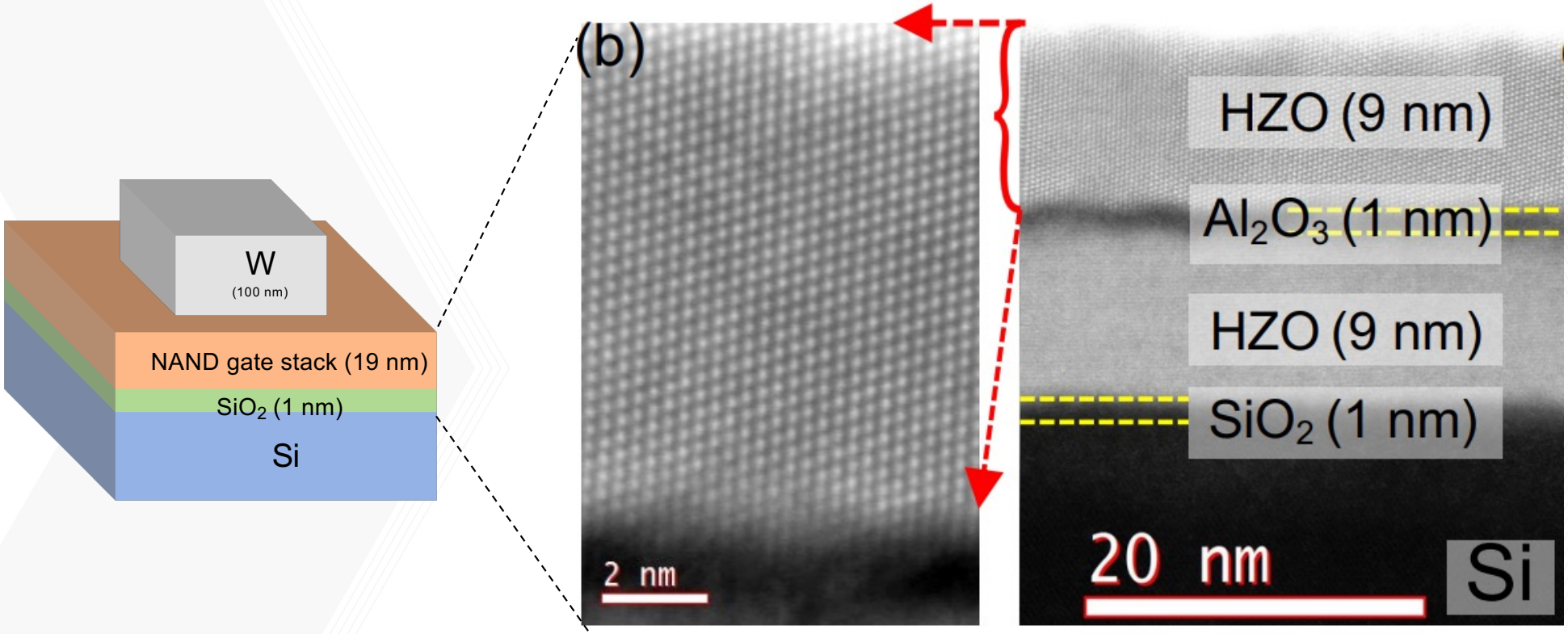




Dr. Dipjyoti Das

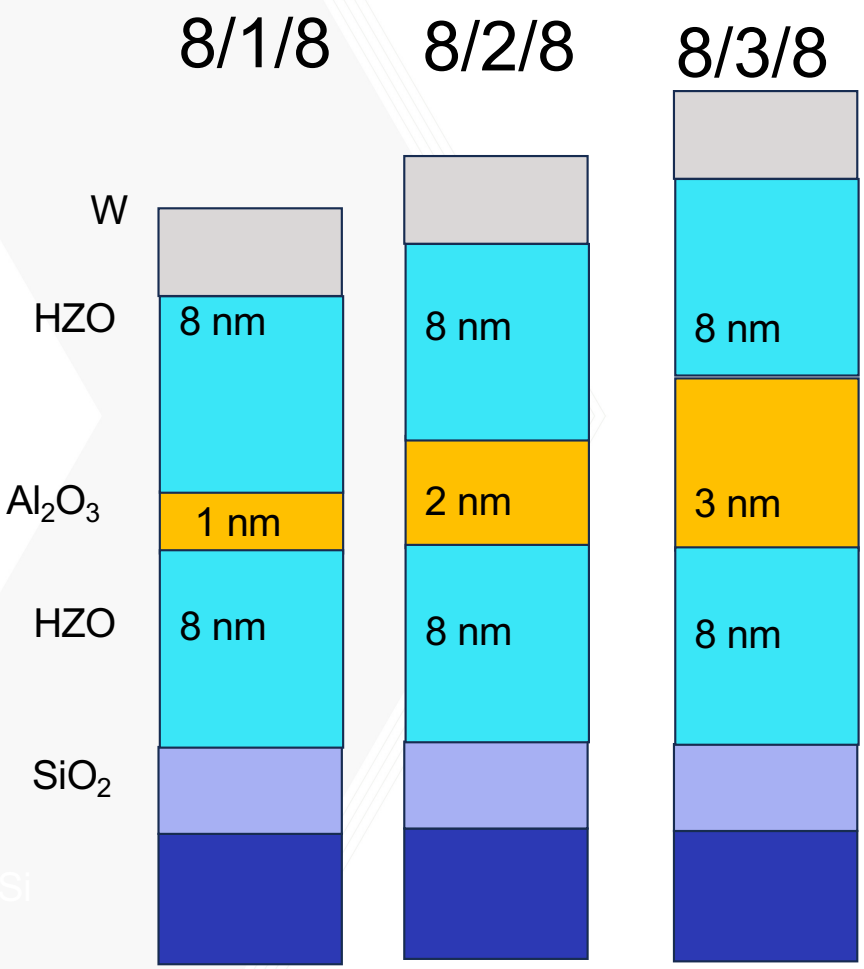
Introducing 1 nm Al_2O_3 intermediate layer dramatically memory window to 5.3 V.

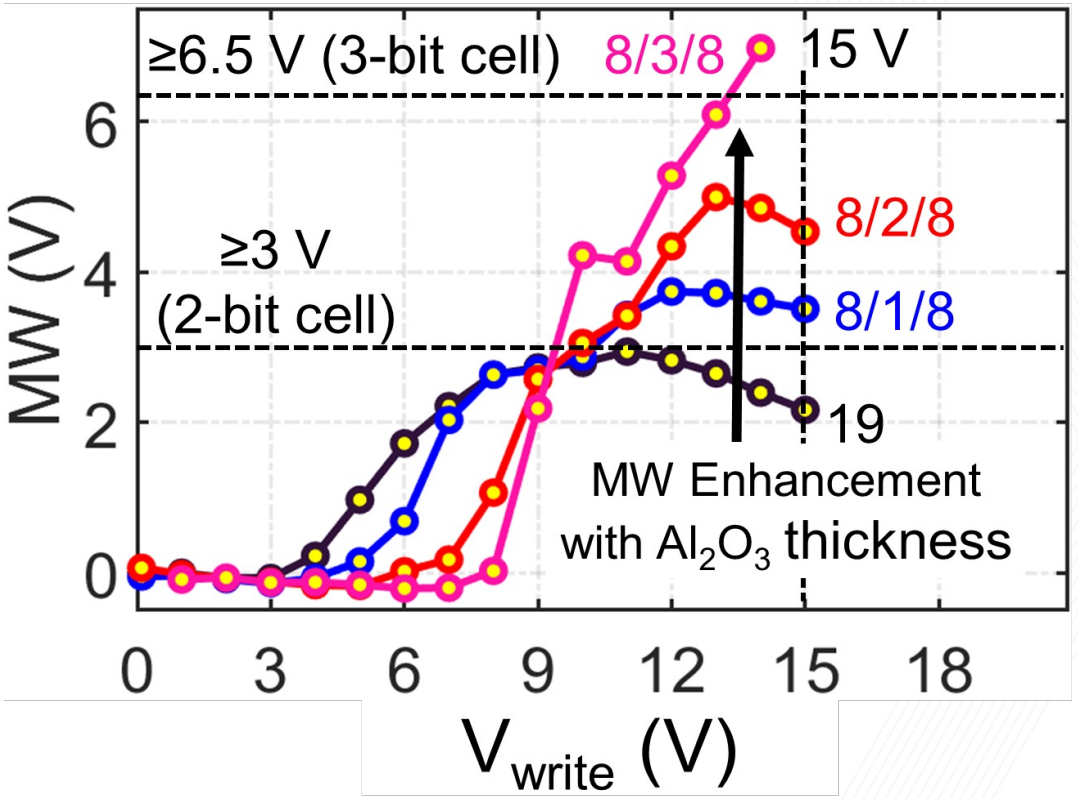
Impact of tunnel dielectric insertion



Full coverage of 1 nm Al_2O_3 is observed.

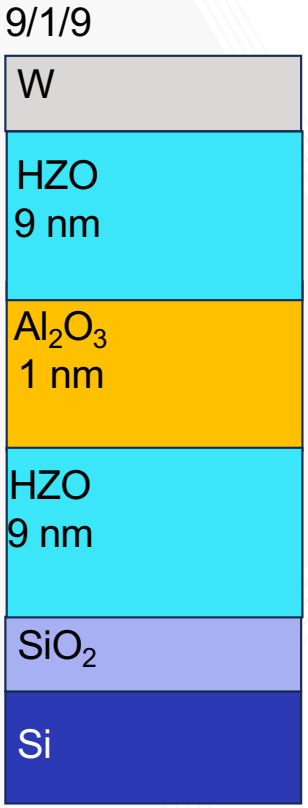
Impact of tunnel dielectric insertion

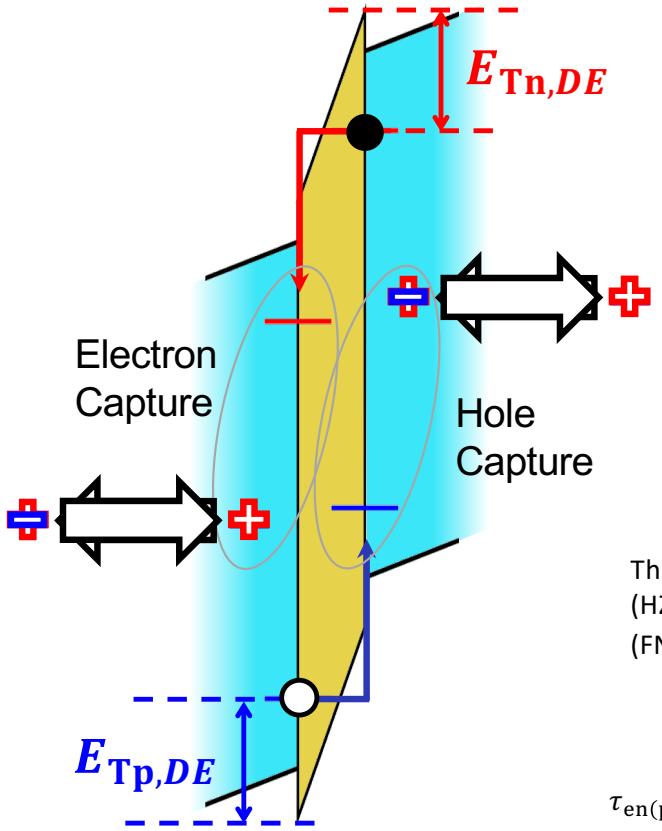




FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

Why do we call it a tunnel dielectric?





The emission mechanism of the trapped charges at Al_2O_3/HZO (HZO/Al_2O_3) interfaces are assumed to be Fowler-Nordheim (FN) tunneling → **Al_2O_3 as "Tunnel Dielectric Layer"**

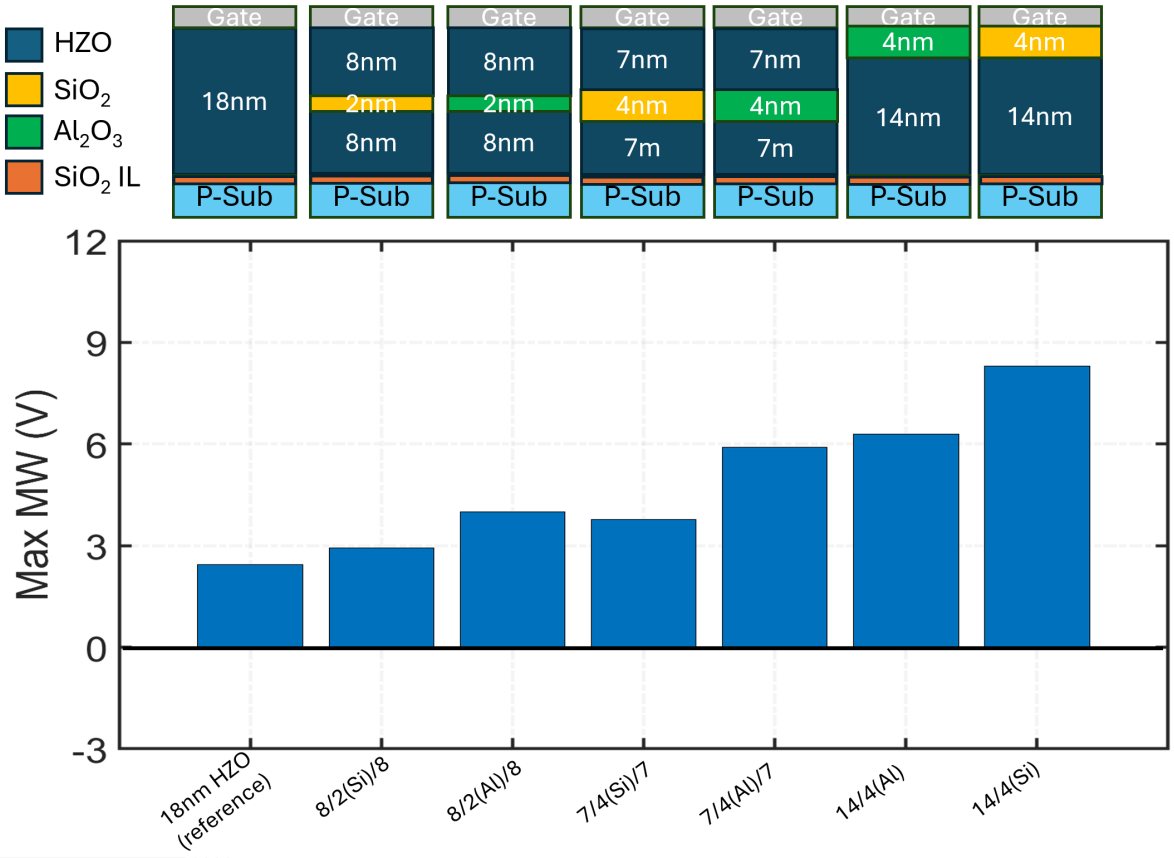
$$\tau_{en(p),i=2(1)} = \tau_{cn(p),i=1(2)} = \tau_0 \exp\left(-\frac{4\sqrt{2m_{AO}\Phi^3_{Tn(p),AO}}}{3q\hbar E_{AO}}\right)$$

The interface trapped charges is hypothesized to interchange position via tunneling!

Impact of the position of the dielectric layer


Prasanna Ravindran


Lance Fernandes



- GBL stacks have higher MW than TDL stacks for similar thickness and material.
- SiO_2 in GBL and Al_2O_3 in TDL gives higher MW for similar dielectric thickness

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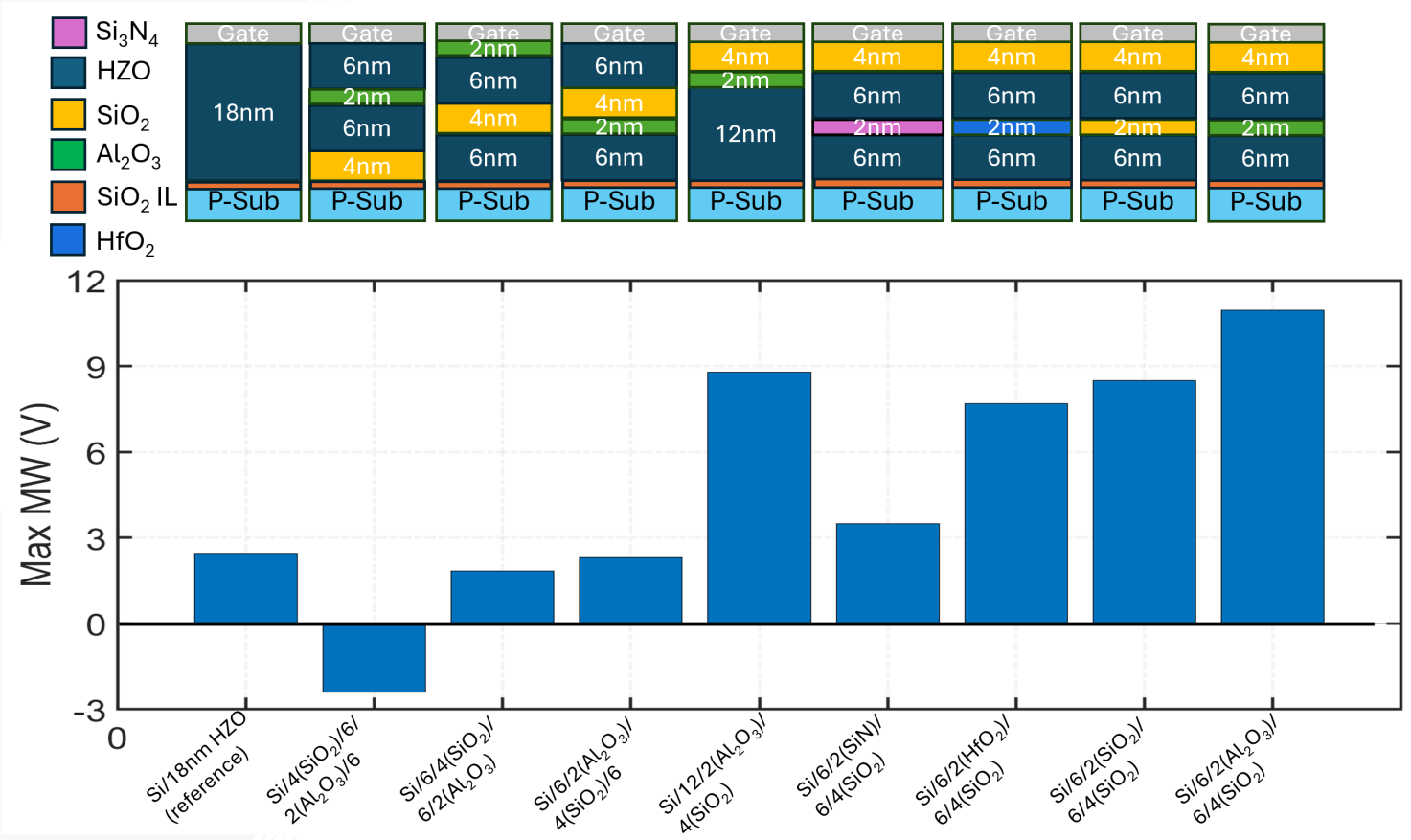
Fernandes, L., Ravindran, P. V., Song, T., Das, D., Park, C., Afroze, N., ... & Khan, A. (2024). Material choices for tunnel dielectric layer and gate blocking layer for ferroelectric NAND applications. *IEEE Electron Device Letters*.

Impact of the position of the dielectric layer


Prasanna Ravindran


Lance Fernandes



A hybrid with 4 nm GBL: SiO_2 and 2 nm TDL: Al_2O_3 gives a maximum MW of 11 V

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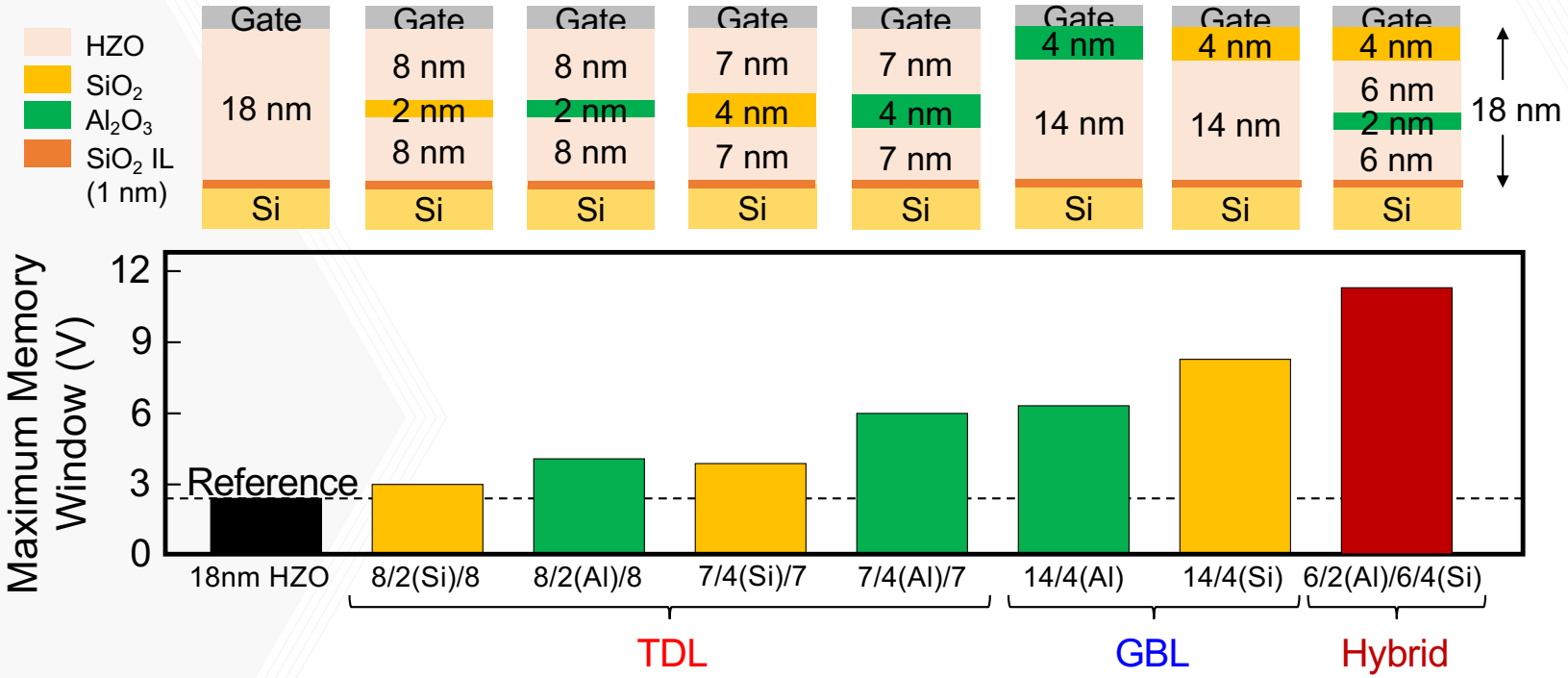
Fernandes, L., Ravindran, P. V., Chen, J., Tian, M., Das, D., Chen, H., ... & Khan, A. (2024). Optimizing Memory Window for Ferroelectric Nand Applications: An Experimental Study on Dielectric Material Selection and Layer Positioning. *IEEE Transactions on Electron Devices*.

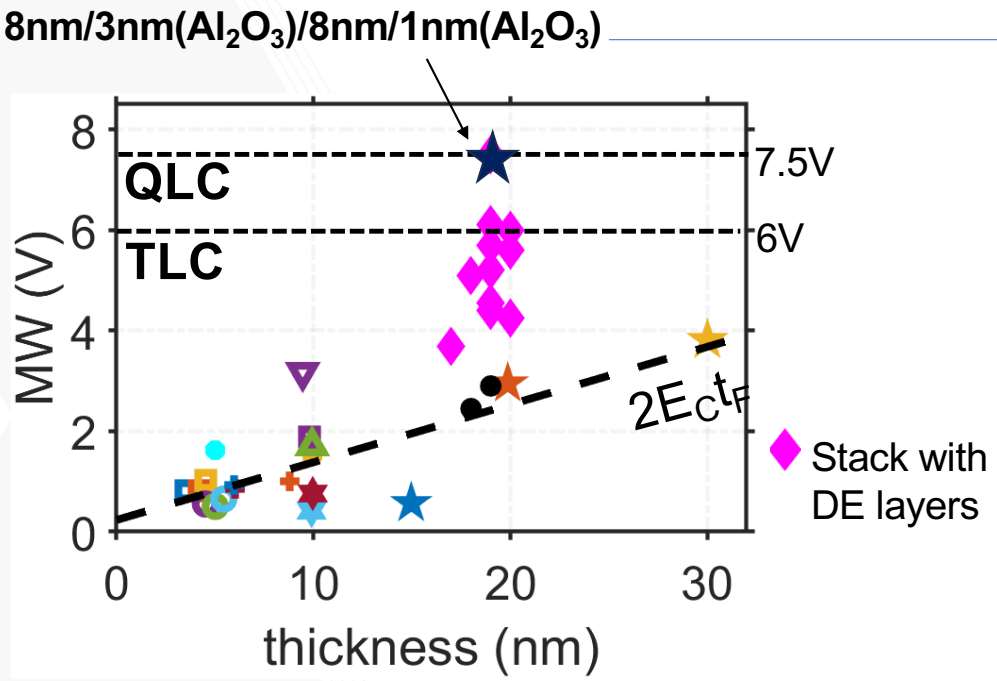
How to engineer MW in FE gate stack?

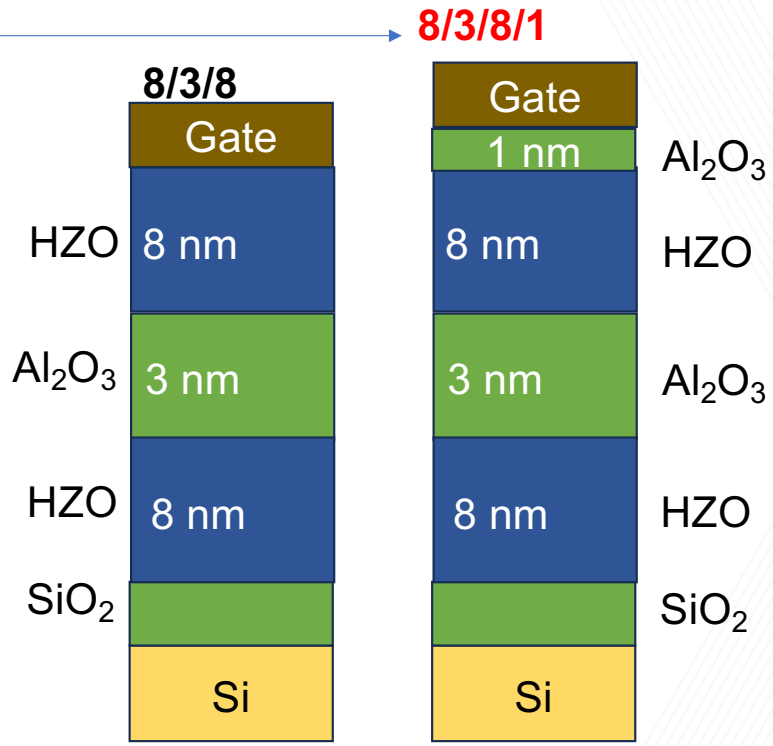


Fernandes, L., Ravindran, P. V., Song, T., Das, D., Park, C., Afroze, N., ... & Khan, A. (2024). Material choices for tunnel dielectric layer and gate blocking layer for ferroelectric NAND applications. *IEEE Electron Device Letters*.

Fernandes, L., Ravindran, P. V., Chen, J., Tian, M., Das, D., Chen, H., ... & Khan, A. (2024). Optimizing Memory Window for Ferroelectric Nand Applications: An Experimental Study on Dielectric Material Selection and Layer Positioning. *IEEE Transactions on Electron Devices*.

Engineered FEFETs for enhanced MW





A ferroelectric-dielectric gate stack offers several tuning knobs to engineer the MW properties

Das, D., Fernandes, L., Ravindran, P. V., Song, T., Park, C., Afroze, N., ... & Khan, A. (2024, May). Design Framework for Ferroelectric Gate Stack Engineering of Vertical NAND Structures for Efficient TLC and QLC Operation. In *2024 IEEE International Memory Workshop (IMW)* (pp. 1-4). IEEE.

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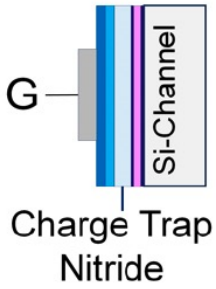
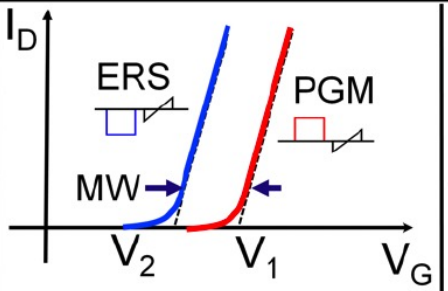
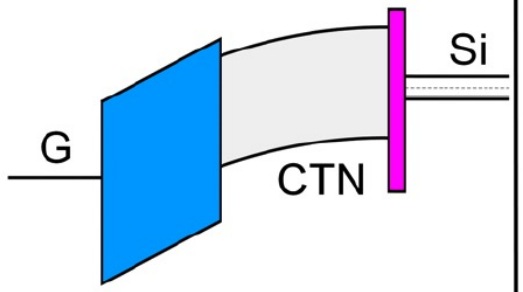
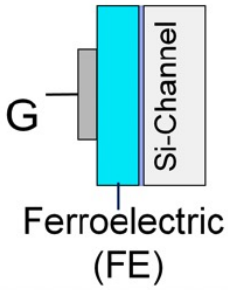
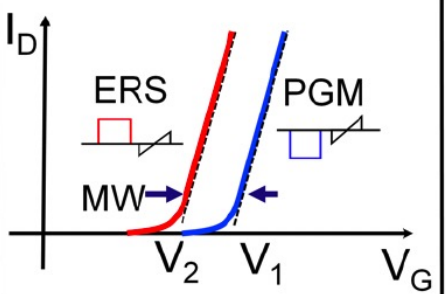
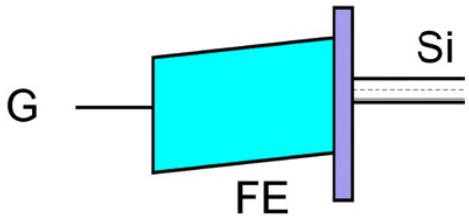
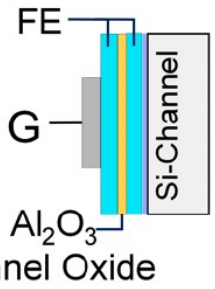
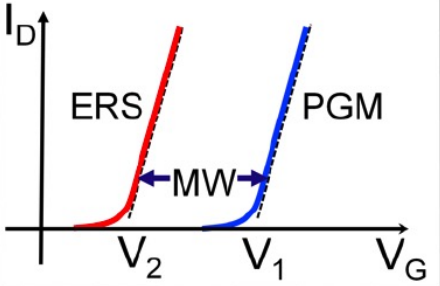
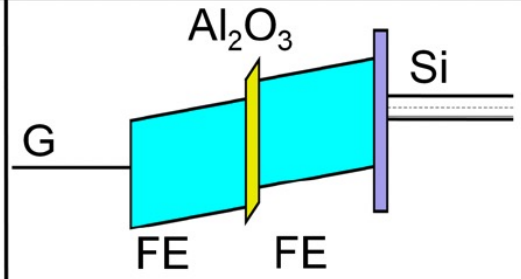
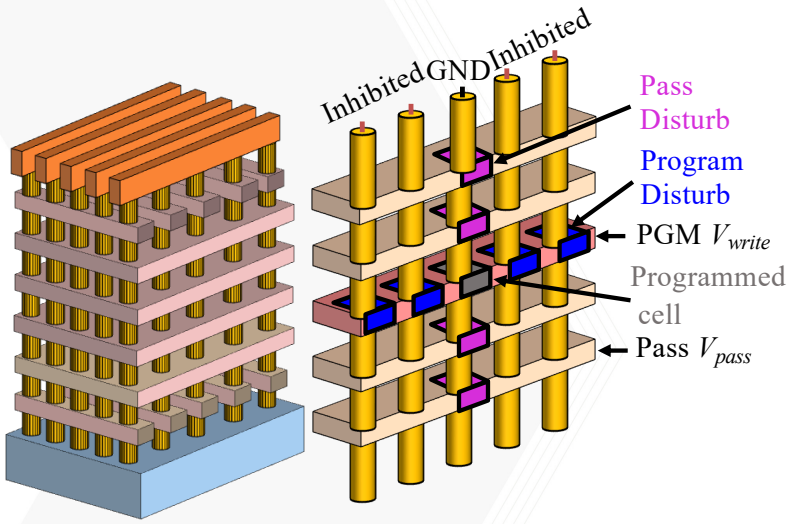
Conclusions

	Structure	Characteristics	Band diagram at FB condition	Attributes
Charge Trap Flash				✓ Large MW × Large Write Voltage Mechanism: Trapping
Conventional FEFET				× Low MW ✓ Low Write Voltage Mechanism: Polarization Switching
Proposed FEFET				✓ Large MW ✓ Moderate Write Voltage Mechanism: Polarization Switching + Trapping + Tunneling

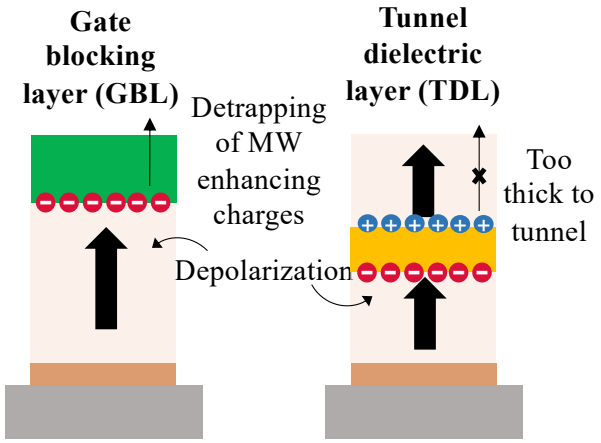
What are the key challenges of Ferroelectric NAND?

Key challenges

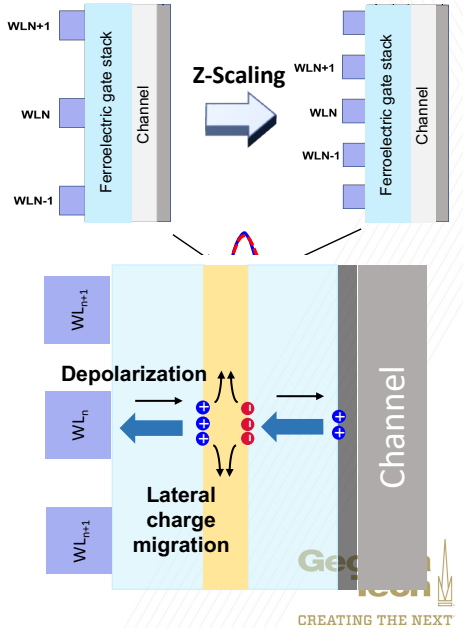
Disturb



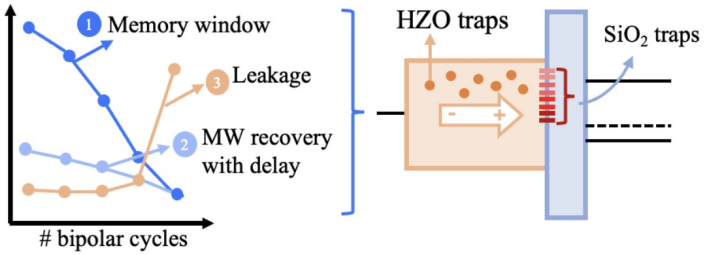
Retention



Z-scaling



Write Endurance



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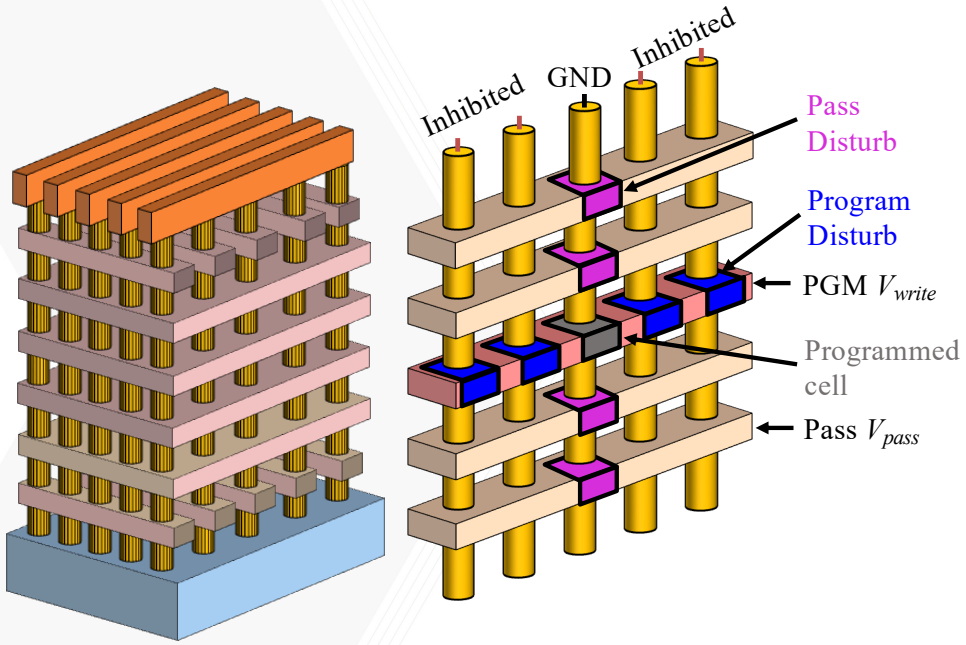
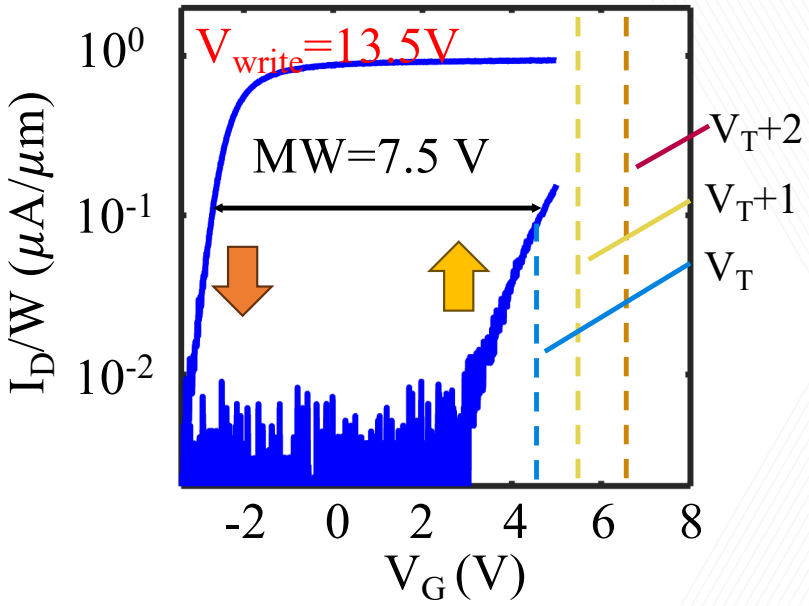
Lance Fernandes

Priyankka Ravikumar

Pass disturb





A pass voltage is applied to unaddressed cells while accessing a different cell along the bit line

Venkatesan, P., Park, C., Song, T., Fernandes, L., Das, D., Afroze, N., ... & Khan, A. (2024). Disturb and its mitigation in Ferroelectric Field-Effect Transistors with Large Memory Window for NAND Flash Applications. *IEEE Electron Device Letters*. [Editors' Pick]

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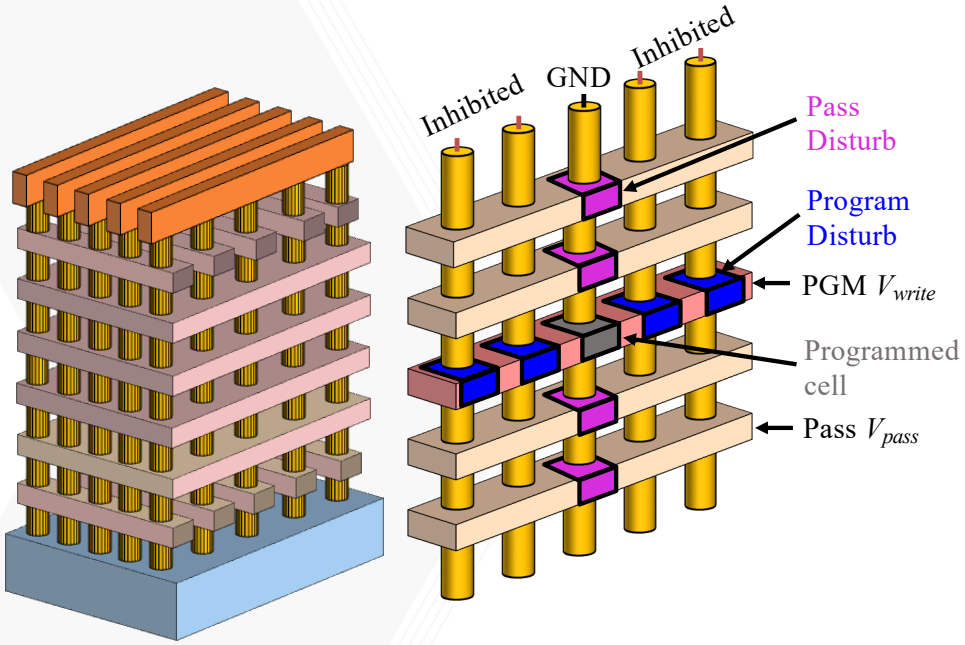
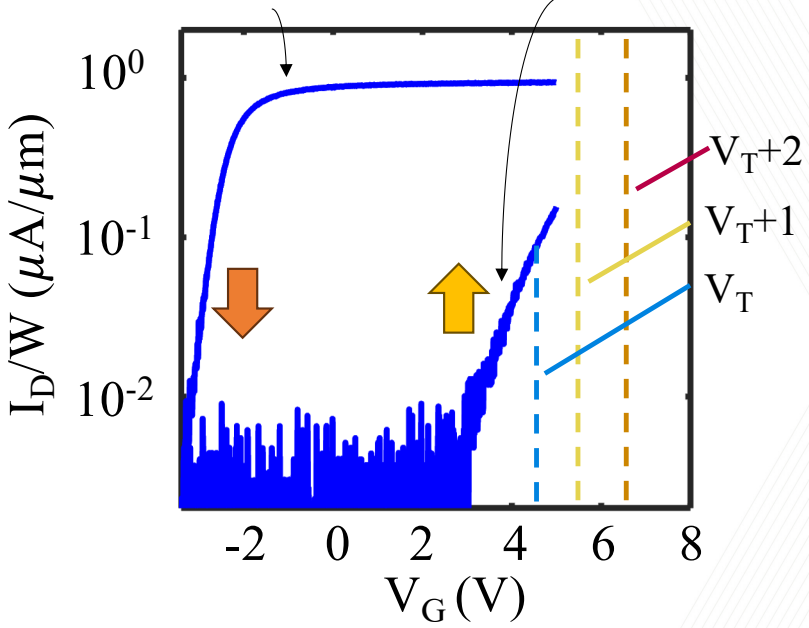
Pass disturb



PGM state: possibility of electron trapping

ERS state: possibility of polarization back flip



This pass voltage could disturb the V_T of the cell either due to electron trapping or polarization back switching.

Venkatesan, P., Park, C., Song, T., Fernandes, L., Das, D., Afroze, N., ... & Khan, A. (2024). Disturb and its mitigation in Ferroelectric Field-Effect Transistors with Large Memory Window for NAND Flash Applications. *IEEE Electron Device Letters*. [Editors' Pick]

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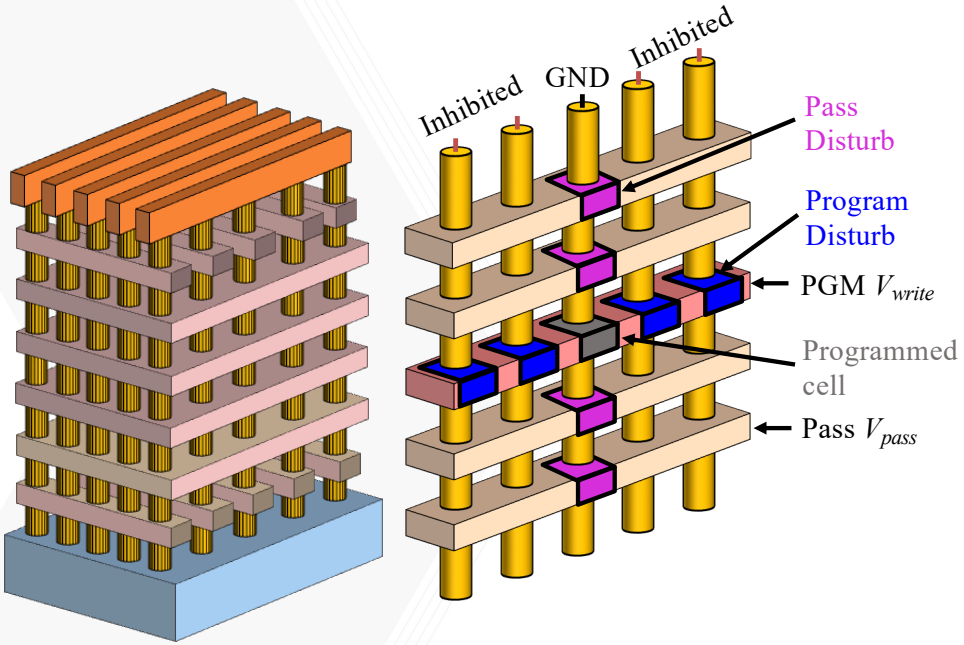
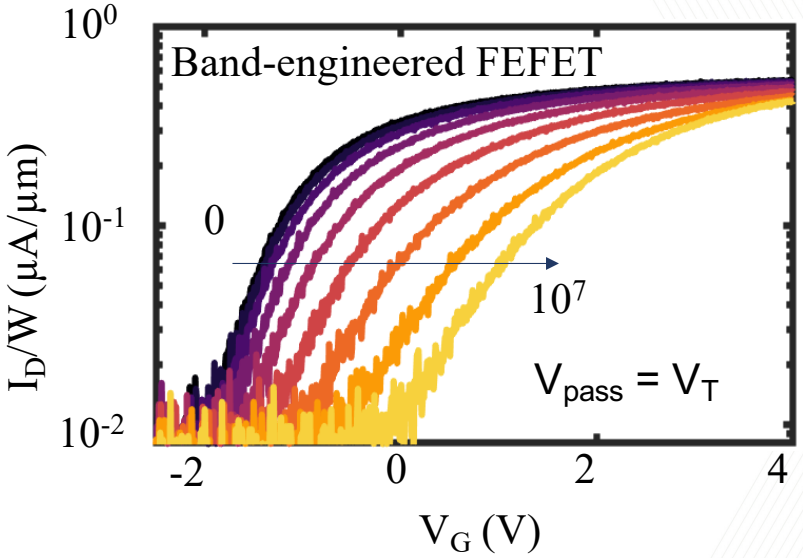
Pass disturb





Electron trapping leads to significant pass disturb in the PGM state

Venkatesan, P., Park, C., Song, T., Fernandes, L., Das, D., Afroze, N., ... & Khan, A. (2024). Disturb and its mitigation in Ferroelectric Field-Effect Transistors with Large Memory Window for NAND Flash Applications. *IEEE Electron Device Letters*. [Editors' Pick]

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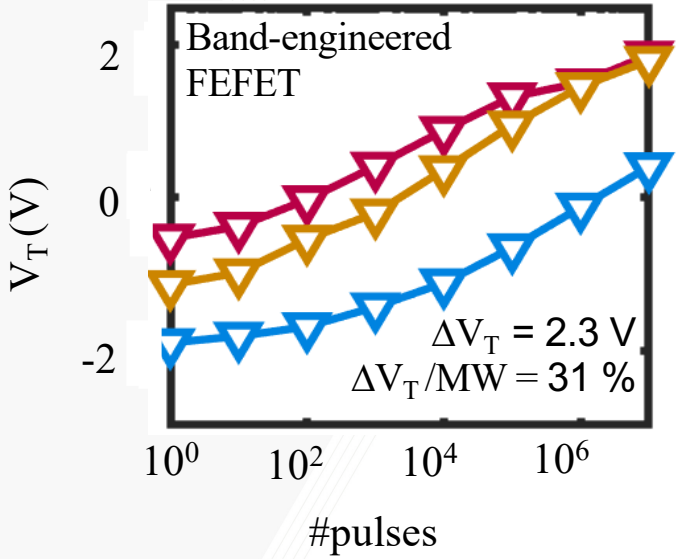
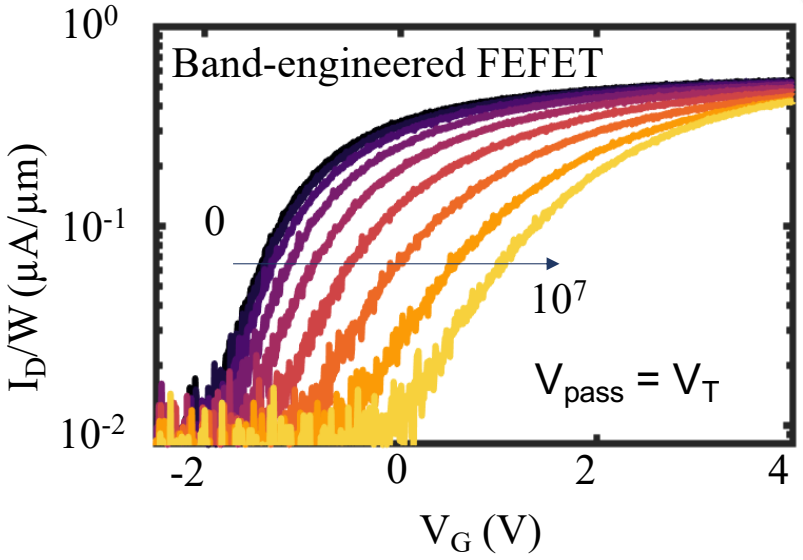
Pass disturb





Electron trapping leads to significant pass disturb in the PGM state

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Mitigating pass disturb

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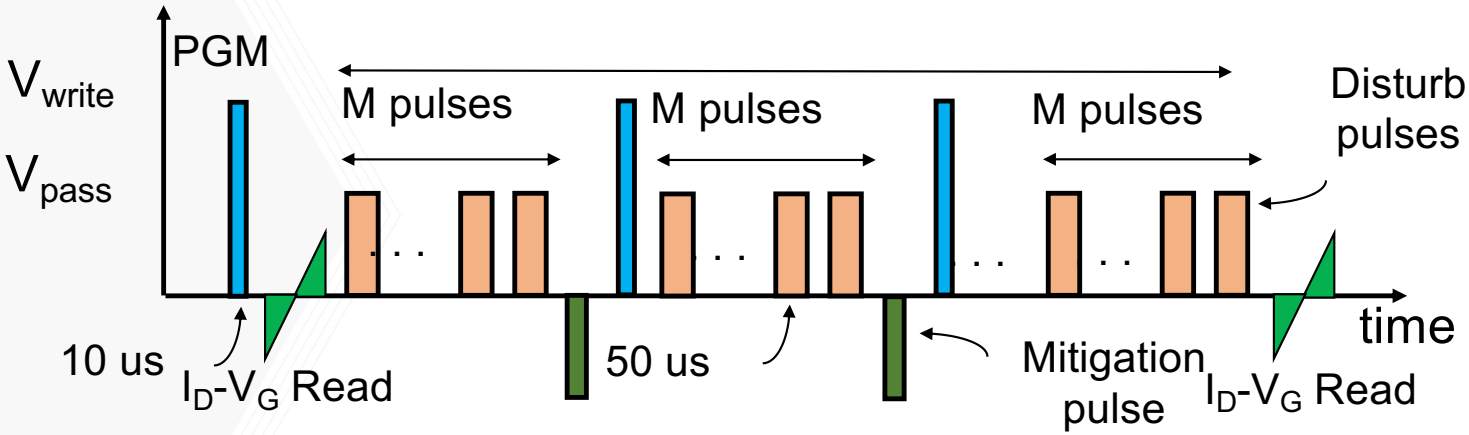
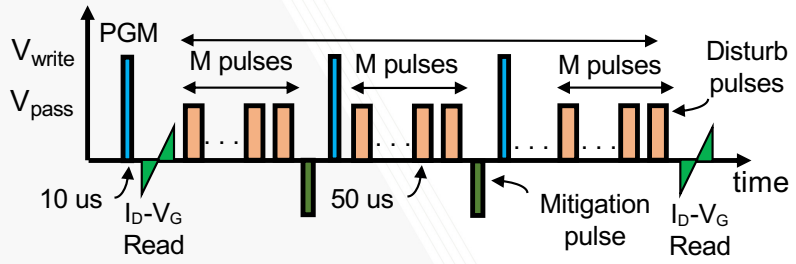
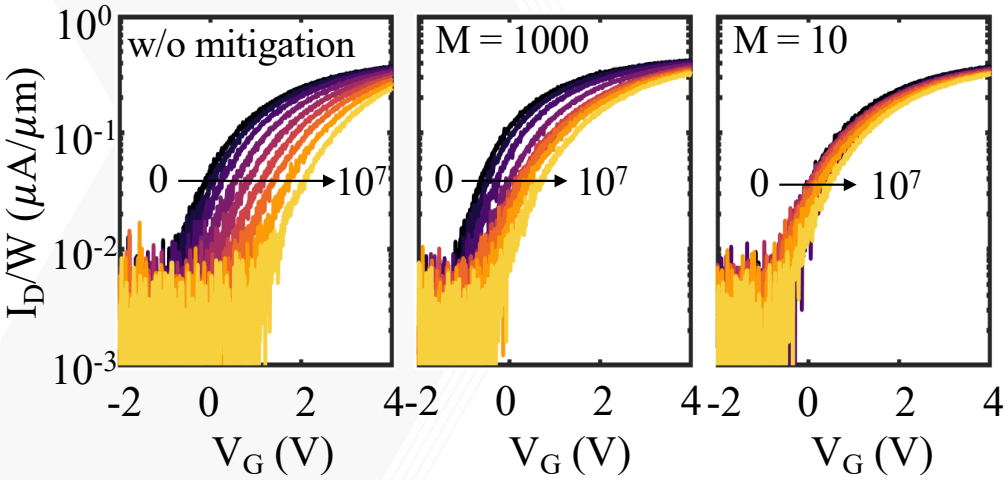


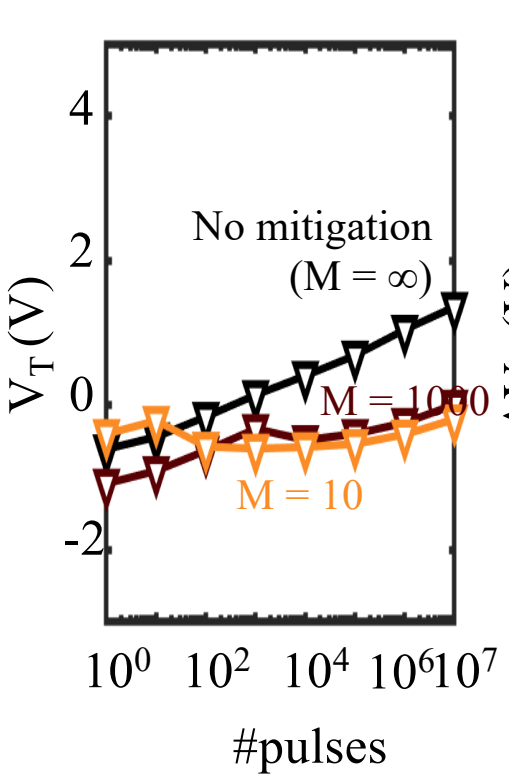
Mitigation scheme reduces pass disturb down to 4%!!

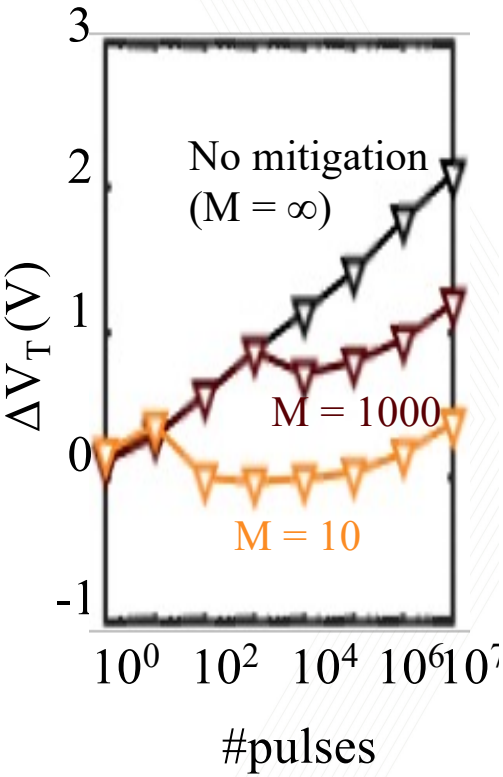
Venkatesan, P., Park, C., Song, T., Fernandes, L., Das, D., Afroze, N., ... & Khan, A. (2024). Disturb and its mitigation in Ferroelectric Field-Effect Transistors with Large Memory Window for NAND Flash Applications. *IEEE Electron Device Letters*. [Editors' Pick]

Mitigating pass disturb









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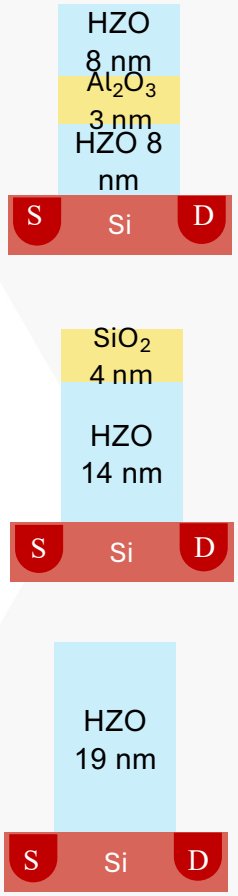
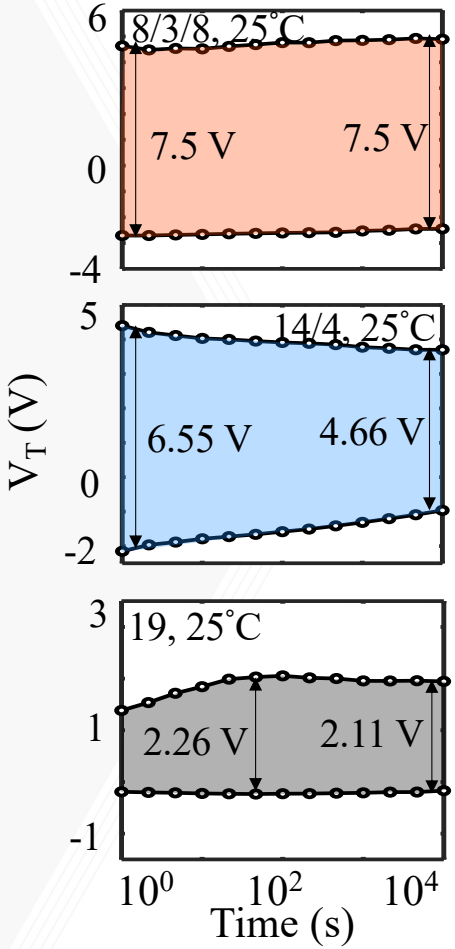
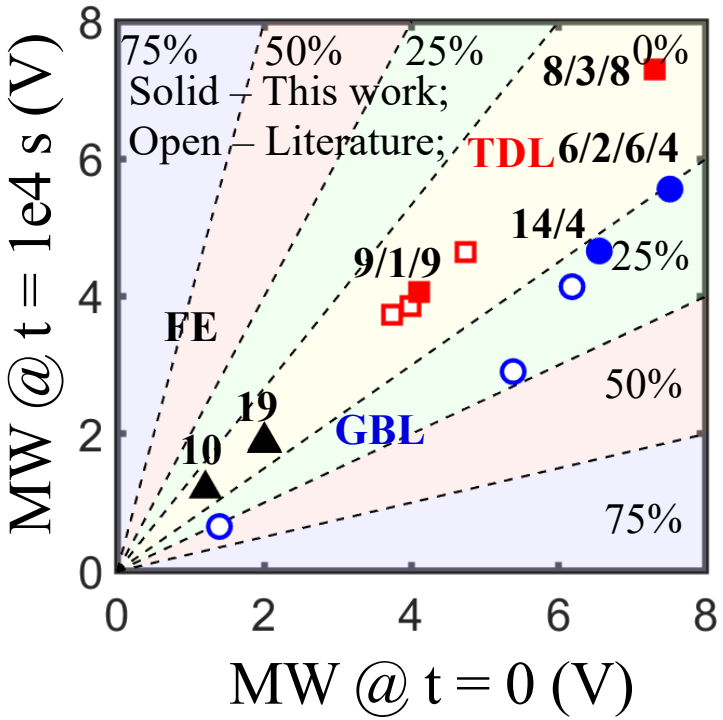
Band engineering for robust retention





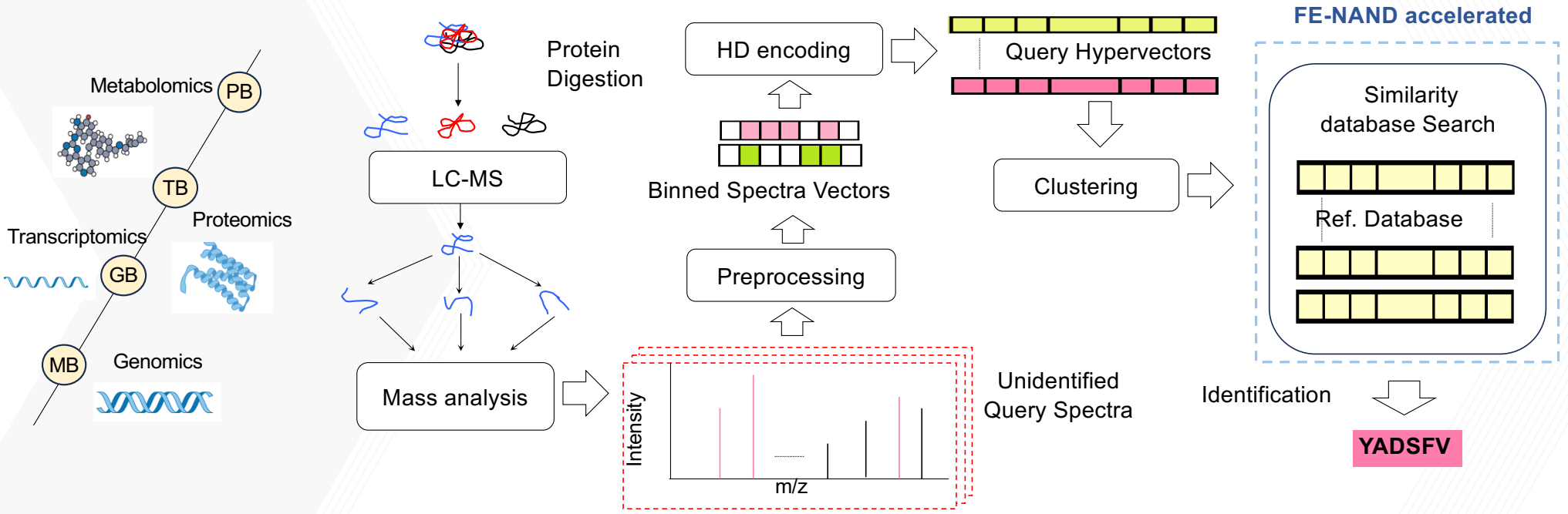


- Laminated gate stack with TDL results in robust retention and high MW
- Gate stack with GBL results in 25-50% degradation.

Venkatesan, P., Fernandes, L., Ravikumar, P., Park, C., Tran, H., Wang, Z., ... & Khan, A. (2024). Demonstration of Robust Retention in Band engineered FEFETs for NAND Storage Applications using Tunnel Dielectric Layer. *IEEE Electron Device Letters*.

In-storage Compute using FE-NAND for large data processing

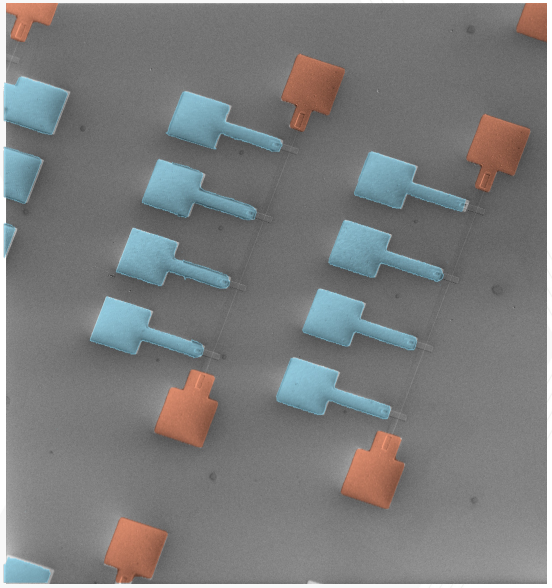
Hyperdimensional computing using FE-NAND

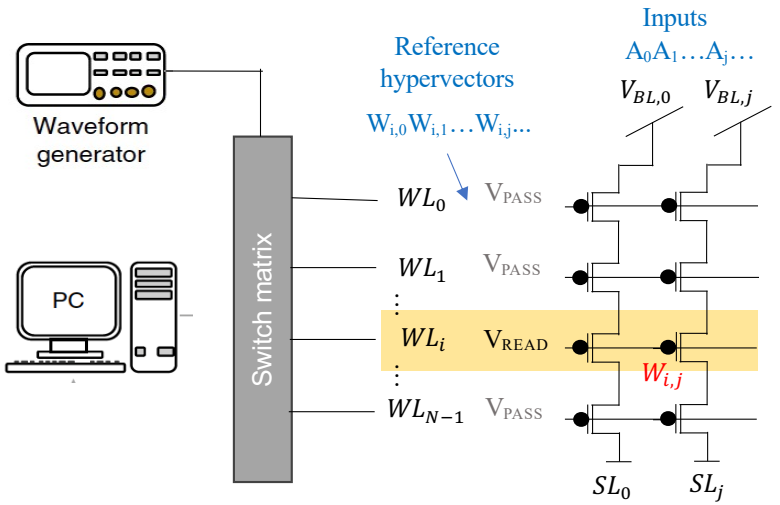


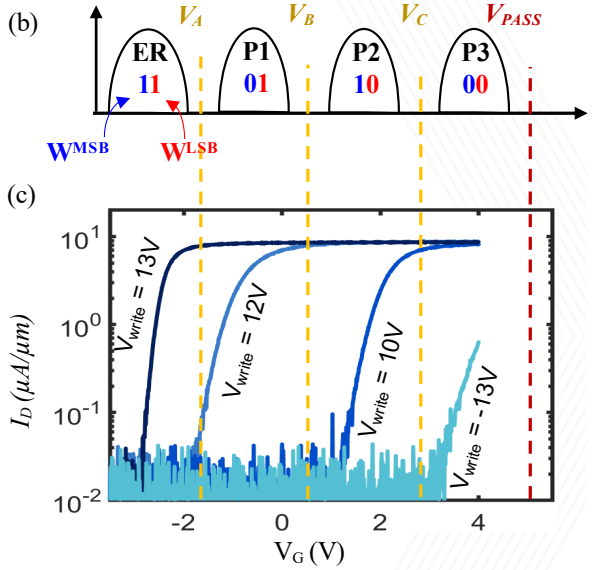
Open-modification search used to identify proteins involves TBs of data

Collaboration with Dr. Tajana Rosing and Dr. Mingu Kang, UCSD

Hyperdimensional computing using FE-NAND







We made FE-NAND strings to demonstrate array level operation.

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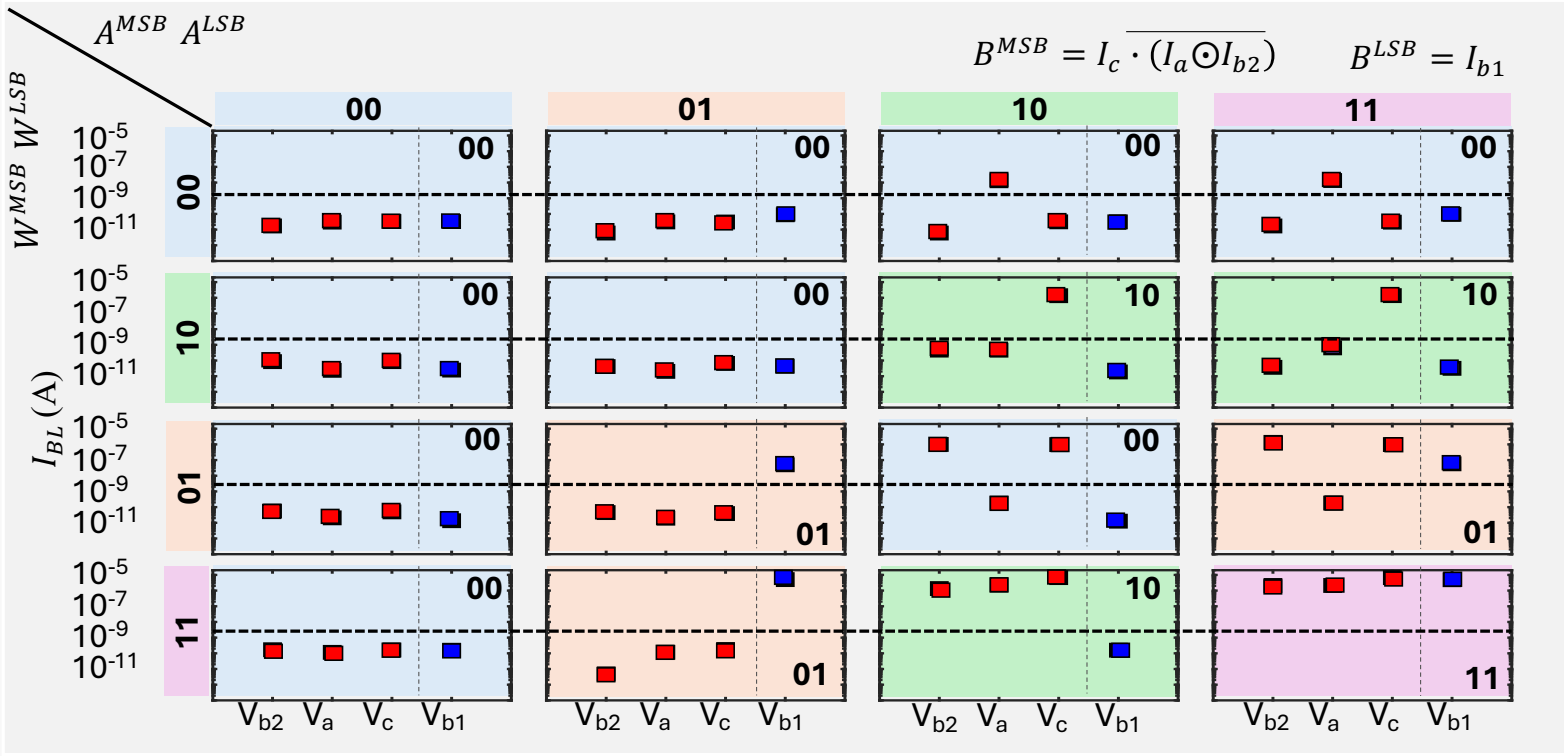
Dot product using FE-NAND strings



MLC dot product truth table was demonstrated for the first time!

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Dot product using FE-NAND strings

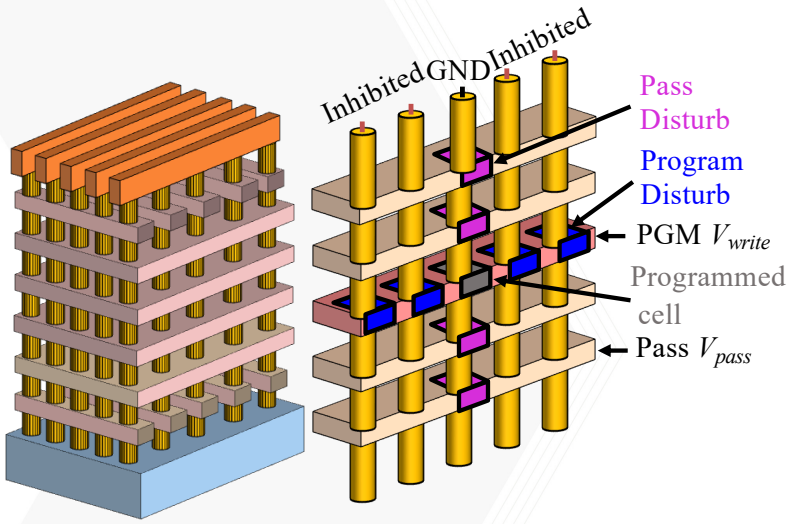
Architecture	GPU [7] (HDC)	FPGA [8] (HDC)	DRAM [9] (HDC)	3D NAND (HDC) [11]	FeNAND (this work)
Compute type	-	RapidOMS	Near-memory	In-memory	In-memory
Algorithm	HOMS-TC		HyperOMS-PIM-DRAM	HyperOMS-3DNAND	HyperOMS
Technology Node	RTX 4090 (5nm)	Versal Prime VM1802 (7nm) - SmartSSD 2.0	22nm DRAM (DDR4) 28nm node-compute	NAND: 14nm ASIC: 7nm FinFET	FeNAND: 14nm ASIC:7nm FinFET
Read latency per cell			10 – 40 ns	4-60 us	4-60 us
Read energy (pJ/byte)			30 - 40	60-200	7.5-25
Inference Speed*	1x (23min)	1.1x (25.7)	2.43x	423x	737x
Inference Energy Efficiency*	1x(454kJ)	11.0625x	101x	7230x	22146x
Capacity Limit (per module)	24GB	32GB	128GB	16TB	>100TB
Data density - Volume	-	-	-	20-30 GB/mm^3	>100 GB/mm^3

FE-NAND offers a high speed, low energy compute platform coupled with large data densities

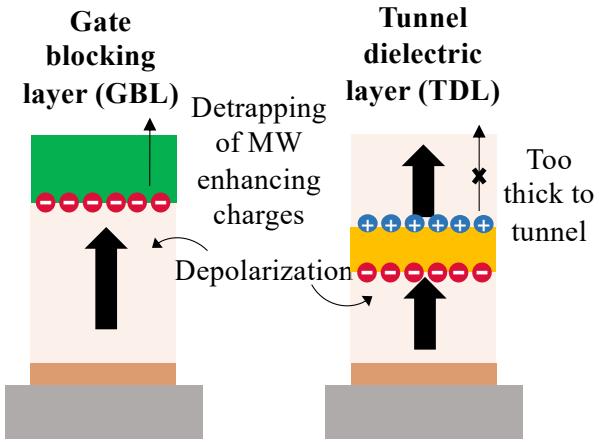
What are the future challenges for technological adoption of Ferroelectric NAND?

Key challenges

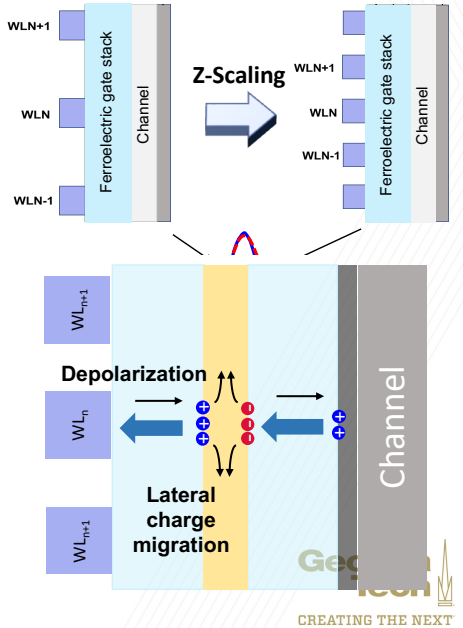
Disturb



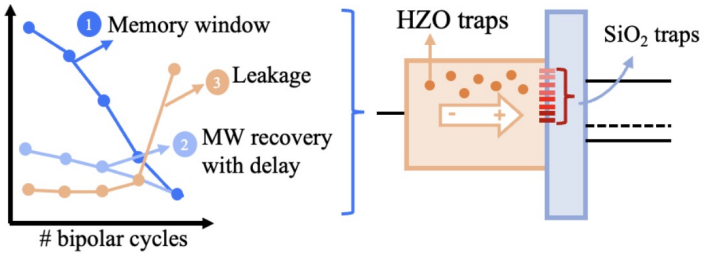
Retention



Z-scaling



Write Endurance



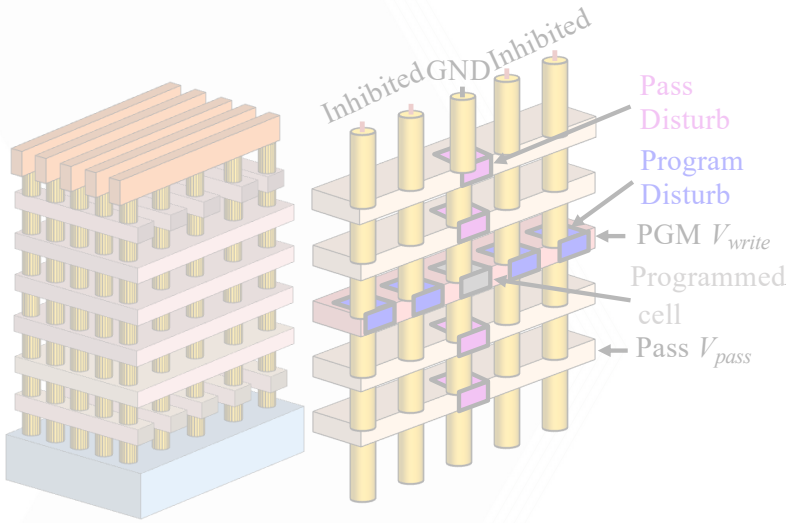
Prasanna Ravindran

Lance Fernandes

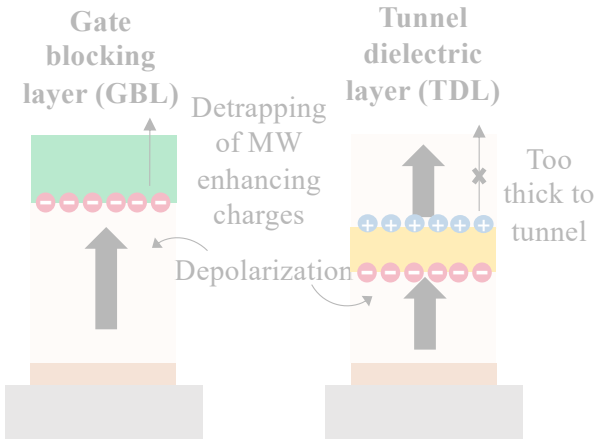
Priyankka Ravikumar

Key challenges

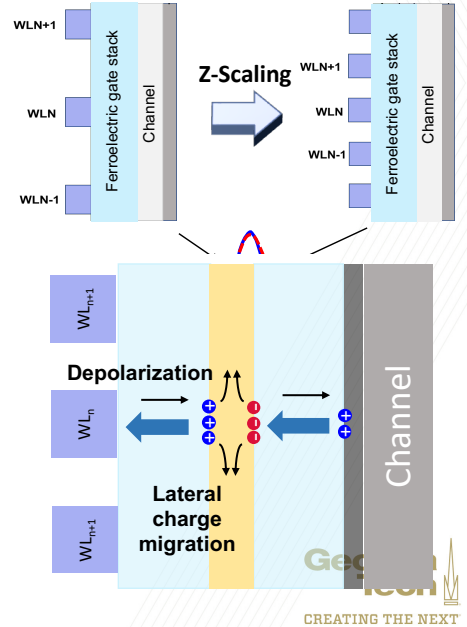
Disturb



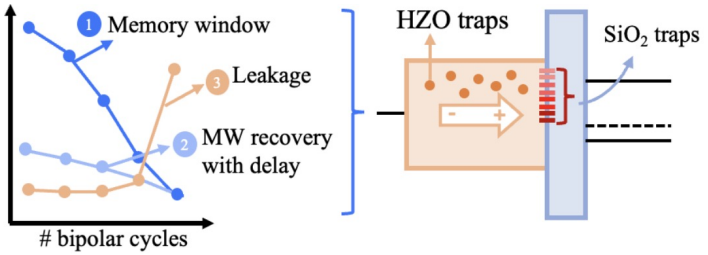
Retention



Z-scaling



Write Endurance



Prasanna Ravindran

Lance Fernandes

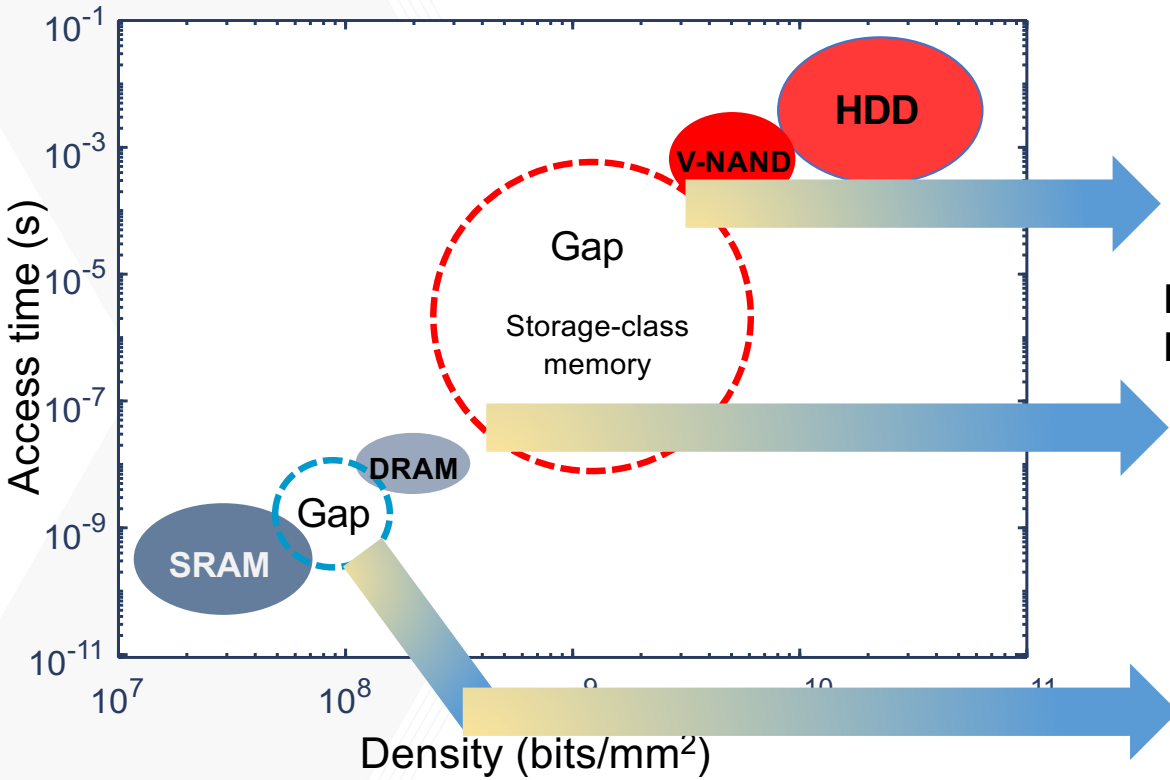
Priyankka Ravikumar

Conclusions

- Ferroelectricity presents opportunities for NAND storage technologies.
  - Write voltage reduction and memory window enhancement.
  - Potential for QLC by stack engineering.
  - Vertical scaling towards 1000 layers.

- Further exploration and engineering required for
  - Write endurance
  - Vertical scaling

Ferroelectrics for memory and storage



Ferroelectrics for flash

- Voltage scaling below 15 V
- Z-scaling

Ferroelectrics for the DRAM/Storage class space

Ramaswamy et al. Micron, IEDM 2024

- Dual Layer 3-D stacked FRAM
- Capacity – 32 Gb (Sk Hynix DRAM –-8 Gb)
- Latency – 180 ns (LPDDR5 – 60 ns)
- Density – 450 Mb/mm^2

Ferroelectrics for embedded memories/cache

- Density
- BEOL compatibility
- Fast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midtown
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