Ferroelectric Memories

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IEEE 2024 IRDS and International Nanodevices & Computing Conference
9/26/2024

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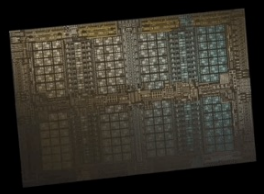
Memory

Hyperscale AI and High-performance Computing



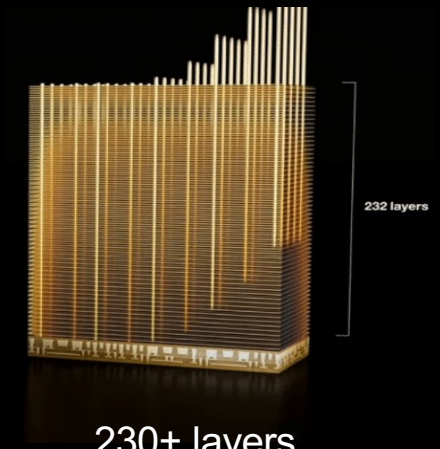
HBM3E: 12-high, 32 GB

1.18 TB/s

Source: NVIDIA

Storage

Client, Mobile, Enterprise



230+ layers

2.4 GB/s

Source: Micron

Embedded

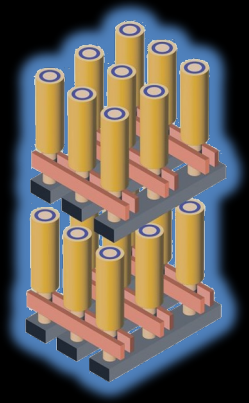
Automotive

14nm eMRAM

16 MB

Source: Forbes

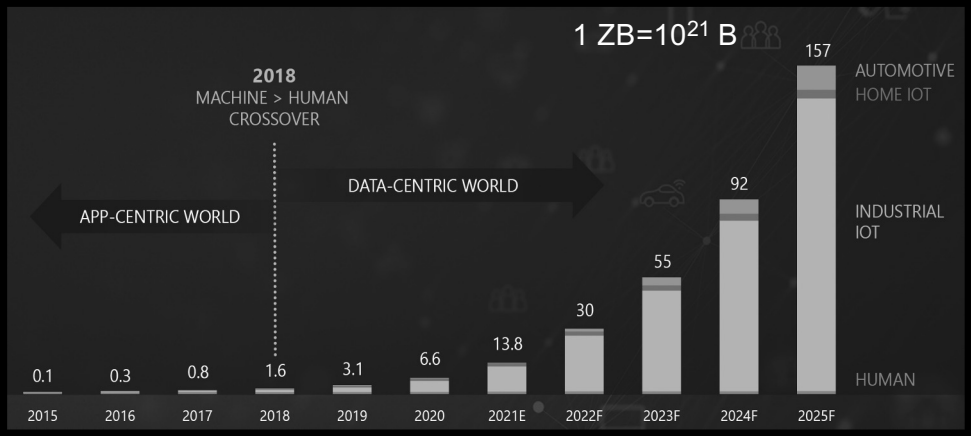
Emerging Memory



Ferroelectric NV-DRAM

32 Gb, 3D-stacked, multi-layer

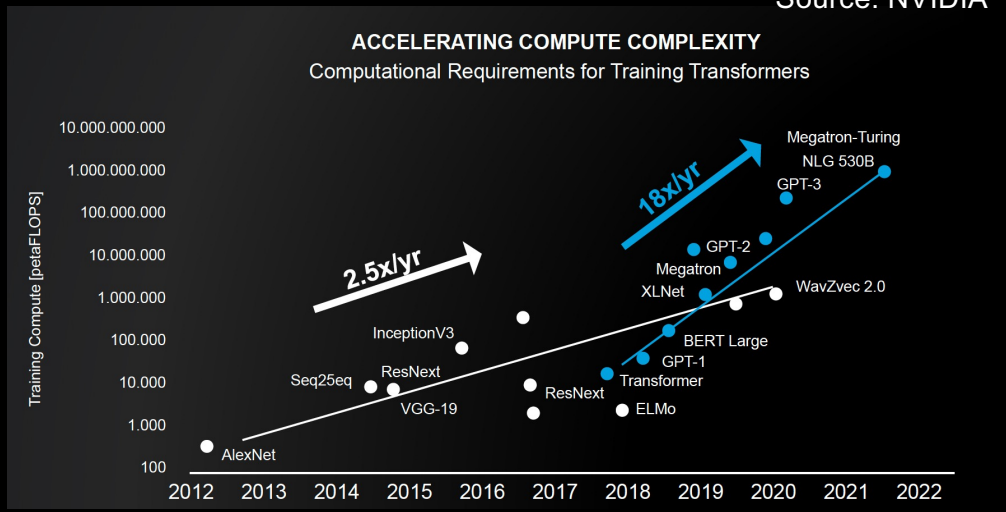
Source: IEDM 2023



Source: AMAT

Machined data generation is on an exponential path!

Source: NVIDIA

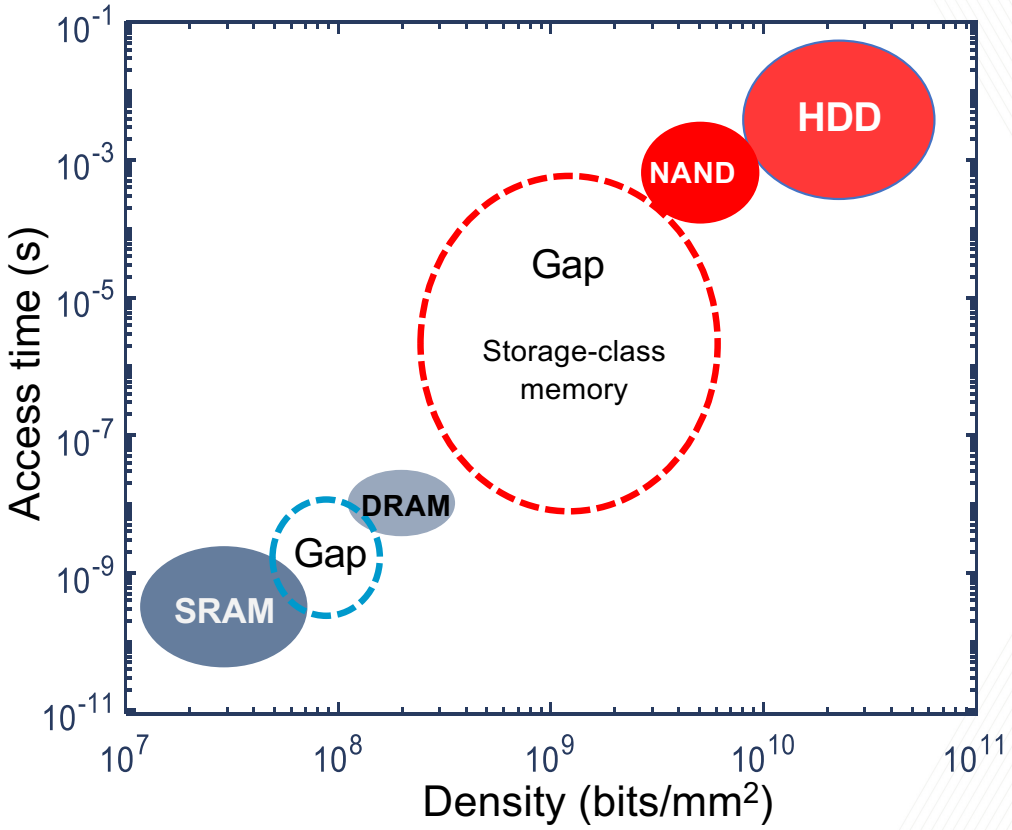


The explosion of AI requires more data crunching and, consequently, more memory.

Generational challenges in memory

What are the opportunities for new memories?

1. Continue scaling.
2. Fill the gaps.



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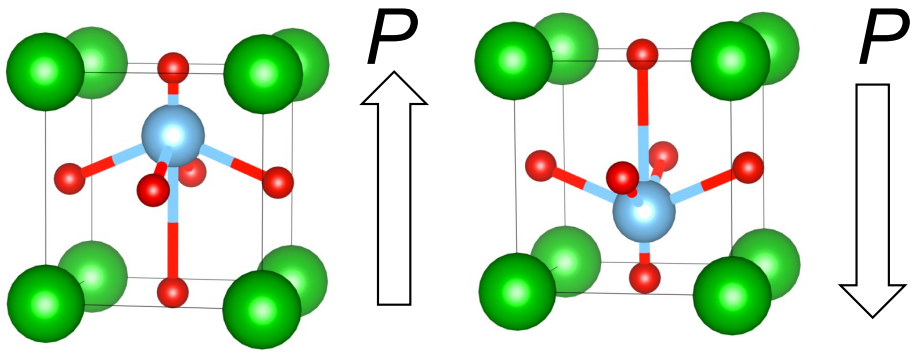
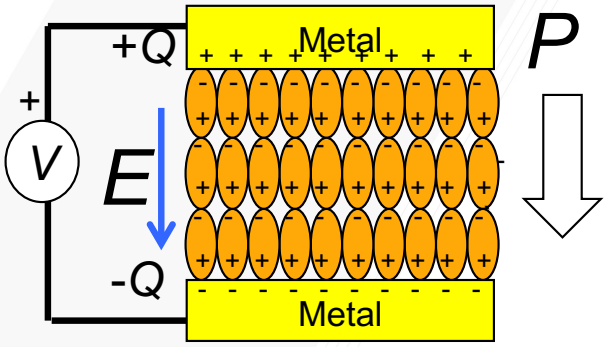
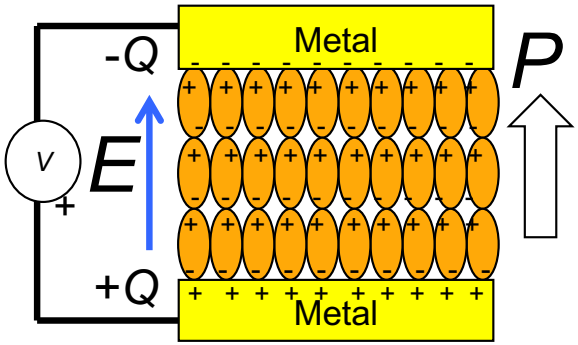
Ferroelectricity

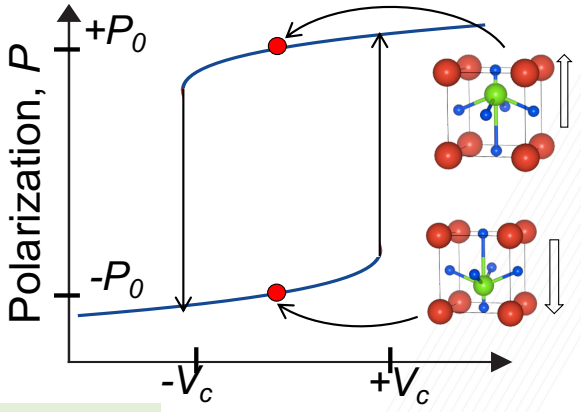
Classical Ferroelectric
$PbTiO_3$, $BaTiO_3$ etc.

Emerging CMOS compatible
Ferroelectrics:
Doped HfO_2









A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

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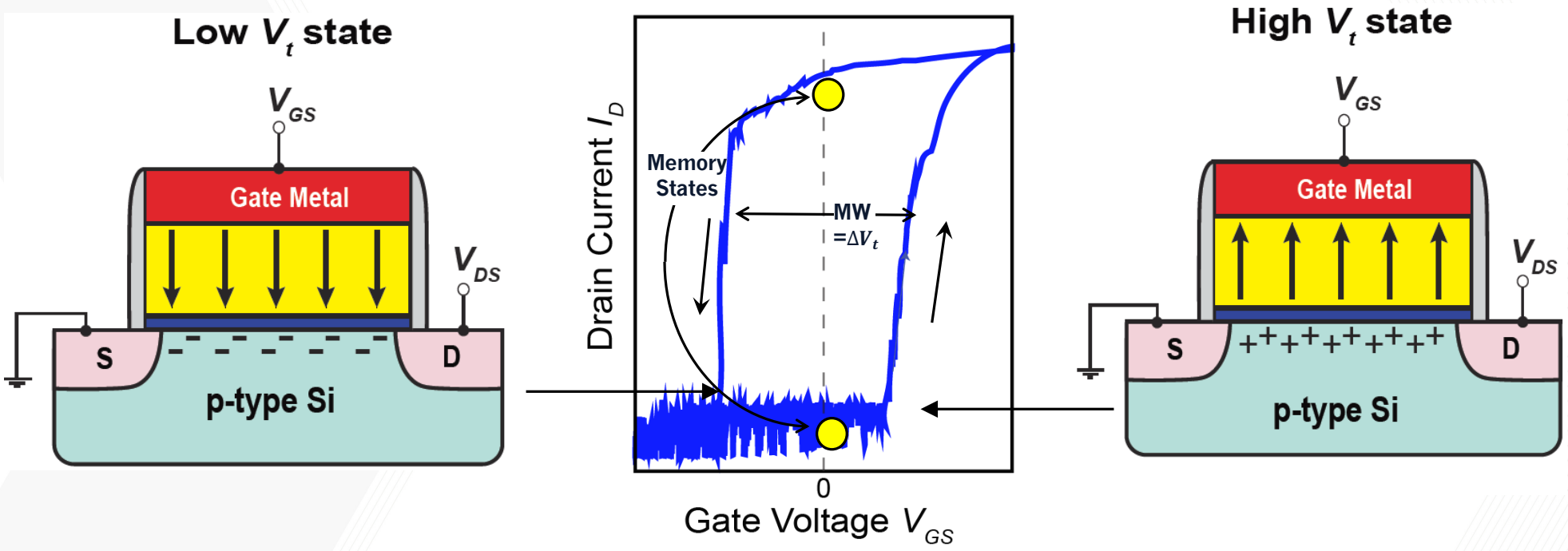
Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the "remnant" polarization.

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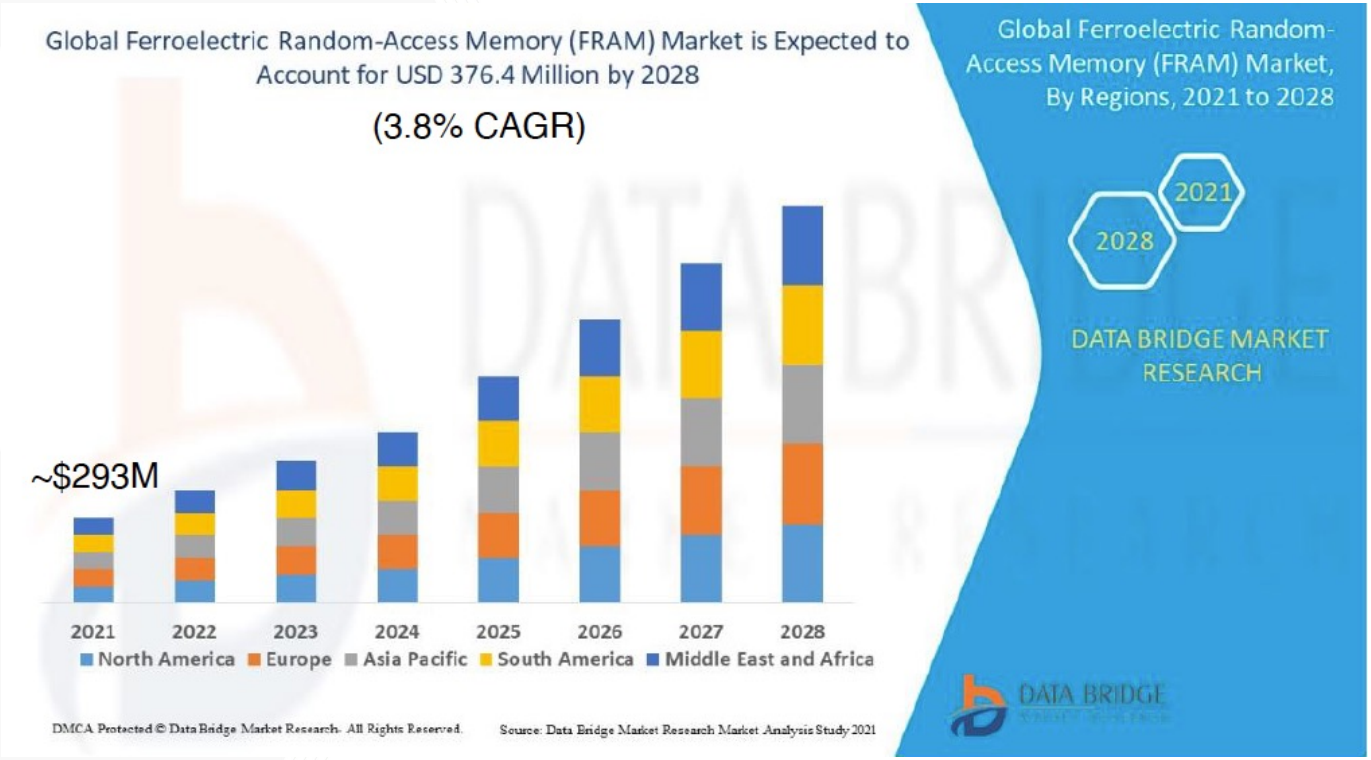
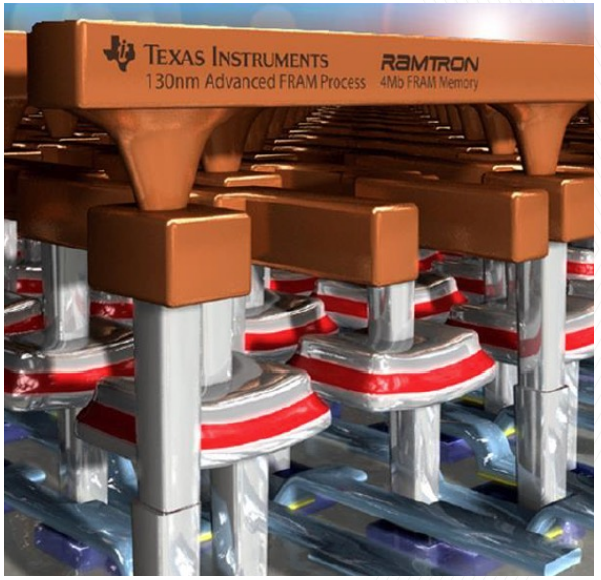
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for for code storage in microcontrollers.





Courtesy: Ted Moise, UT Dallas

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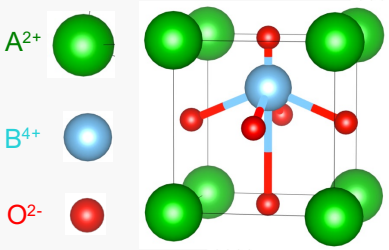
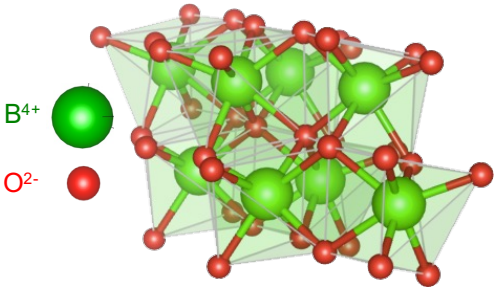
2. Annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al. Appl. Phys. Lett*. 99, 112904 (2011)
- Boscke *et al. 2011 IEEE Int. Electron Devices Meeting.* p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al. Nano Lett.* 12, 4318 (2012)

Perovskite-structure ferroelectric oxide (ABO_3)



Fluorite-structure ferroelectric oxide (BO_2)



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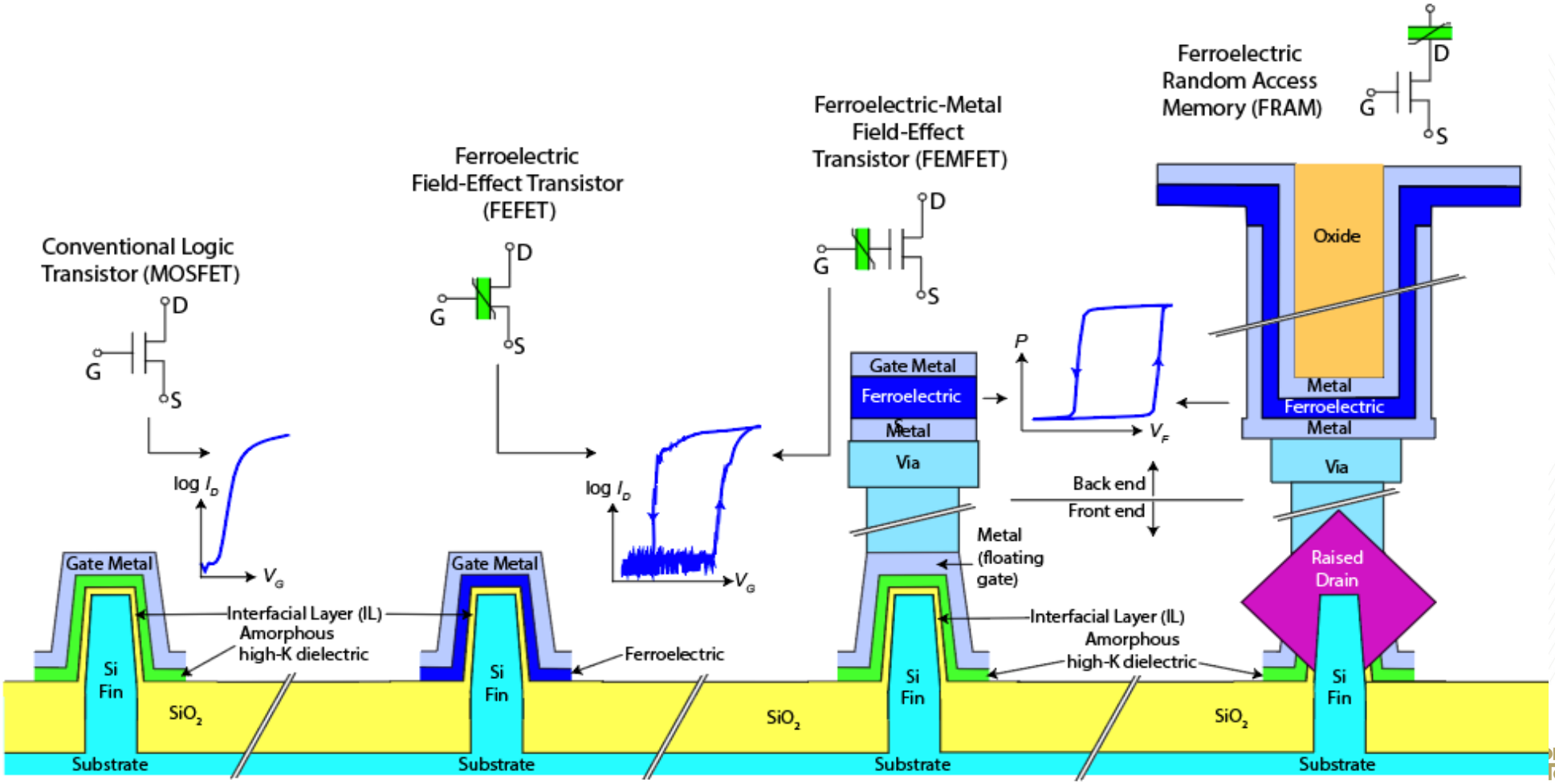
Ferroelectric memories



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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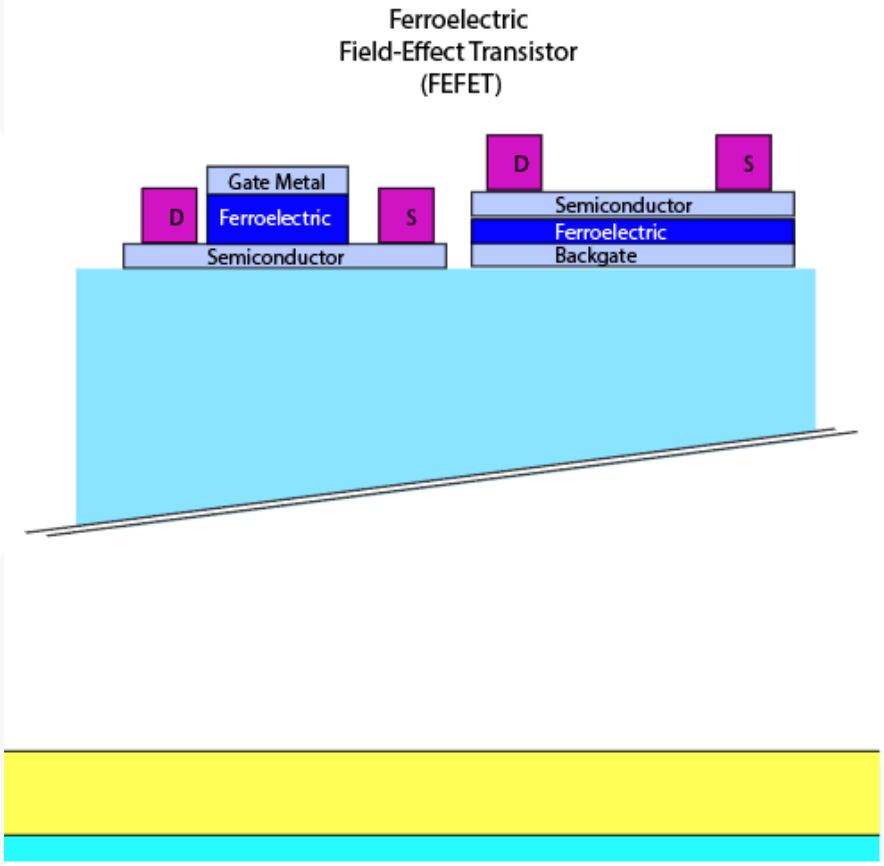
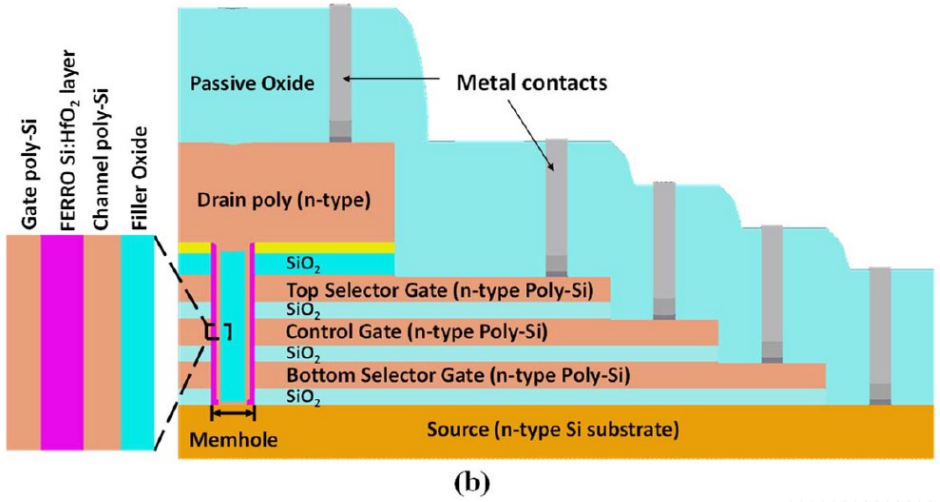
Ferroelectric memories

BEOL FEFET



Vertical FEFET for NAND Storage



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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2011→2023

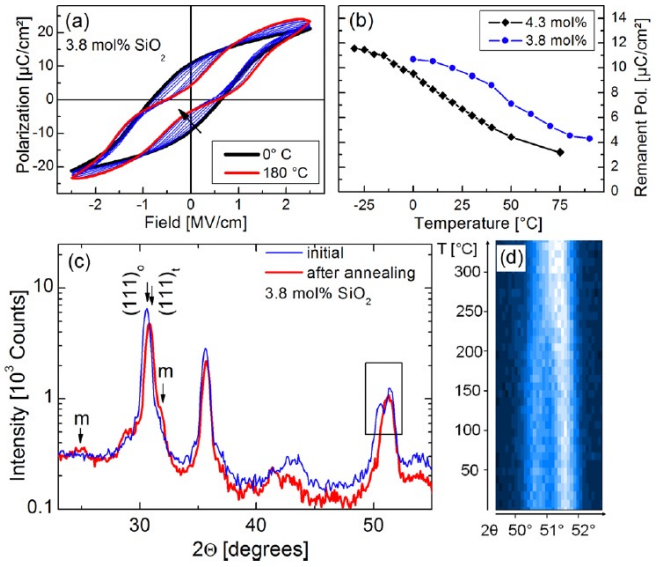
Discovery of Ferroelectricity in HfO2

APPLIED PHYSICS LETTERS **99**, 112904 (2011)

Phase transitions in ferroelectric silicon doped hafnium oxide

T. S. Böscke,[1,2,a),b)] St. Teichert,[3,b)] D. Bräuhaus,[4] J. Müller,[5] U. Schröder,[2,b)] U. Böttger,[4] and T. Mikolajick[2,6]
[1]*Löberwallgraben 2, 99096 Erfurt, Germany*
[2]*Namlab gGmbH, 01187 Dresden, Germany*
[3]*UAS Jena, Department of SciTec, 07745 Jena, Germany*
[4]*RWTH Aachen, Institut für Werkstoffe der Elektrotechnik, 52062 Aachen, Germany*
[5]*Fraunhofer Center Nanoelectronic Technologies (CNT), 01099 Dresden, Germany*
[6]*Department of Nanoelectronic Materials, University of Technology Dresden, 01062 Dresden, Germany*

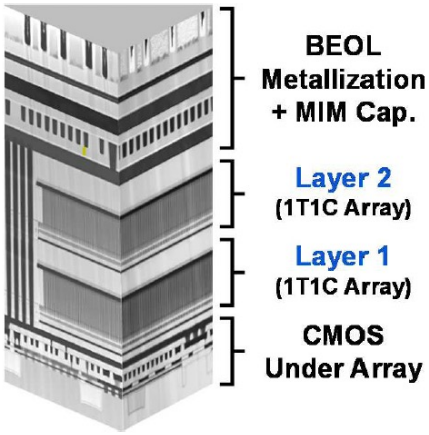
(Received 18 July 2011; accepted 19 August 2011; published online 15 September 2011)

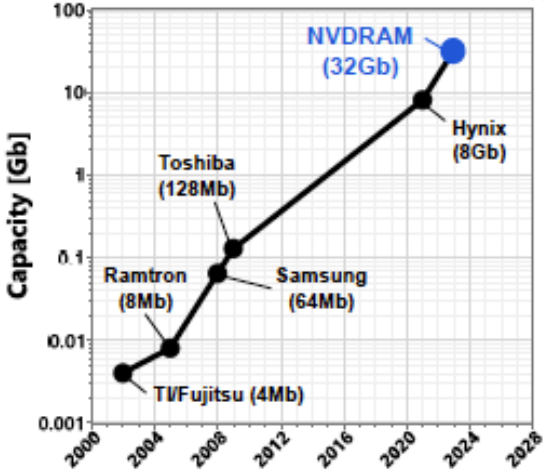


Demonstration of high-density Ferroelectric RAM

NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads

N. Ramaswamy, A. Calderoni, J. Zahurak, G. Servalli, A. Chavan, S. Chhajed, M. Balakrishnan, M. Fischer, M. Hollander, D. P. Ettisserry, A. Liao, K. Karda, M. Jerry, M. Mariani, A. Visconti, B. R. Cook, B. D. Cook, D. Mills, A. Torsi, C. Mouli, E. Byers, M. Helm, S. Pawlowski, S. Shiratake, and N. Chandrasekaran
Micron Technology Inc., Boise, USA, email: dramaswamy@micron.com





Ramaswamy et al. IEDM 2023

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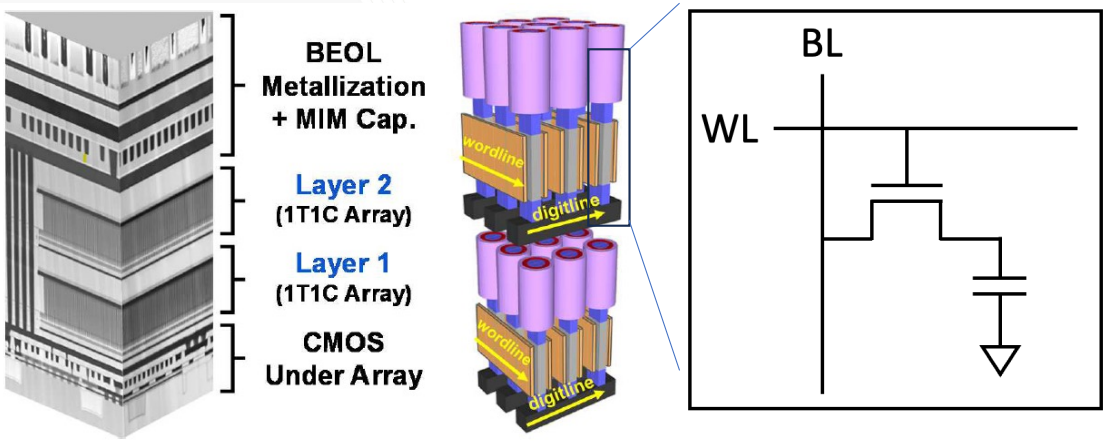
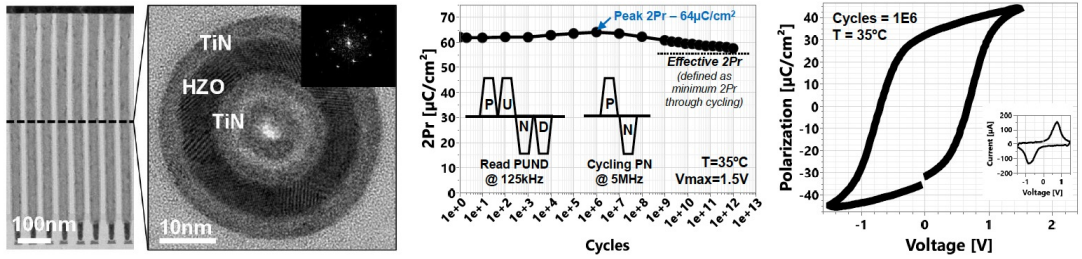
Ferroelectric Random Access Memory

1T-1C structure



Dense 3-D structure, high read/write endurance



Latency

a)

Timing	LPDDR5	NVDRAM
tRC	60ns	185ns
tRCD	18ns	85ns
tWR	34ns	10ns
tRP	18ns	80ns
tAA	22ns	26ns

b)

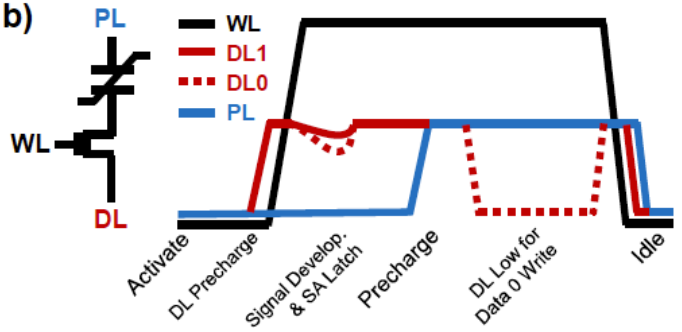


Figure 13. (a) Timing comparison to typical LPDDR5 DRAM. (b) Diagram of basic array operation. Data 1 shown with solid line. Data 0 shown with dashed line. Sensing is destructive to Data 0. Data 0 writeback occurs during precharge.

Ramaswamy et al. IEDM 2023
Chavan et al. IMW 2024
Ettisserry et al. IRPS 2024

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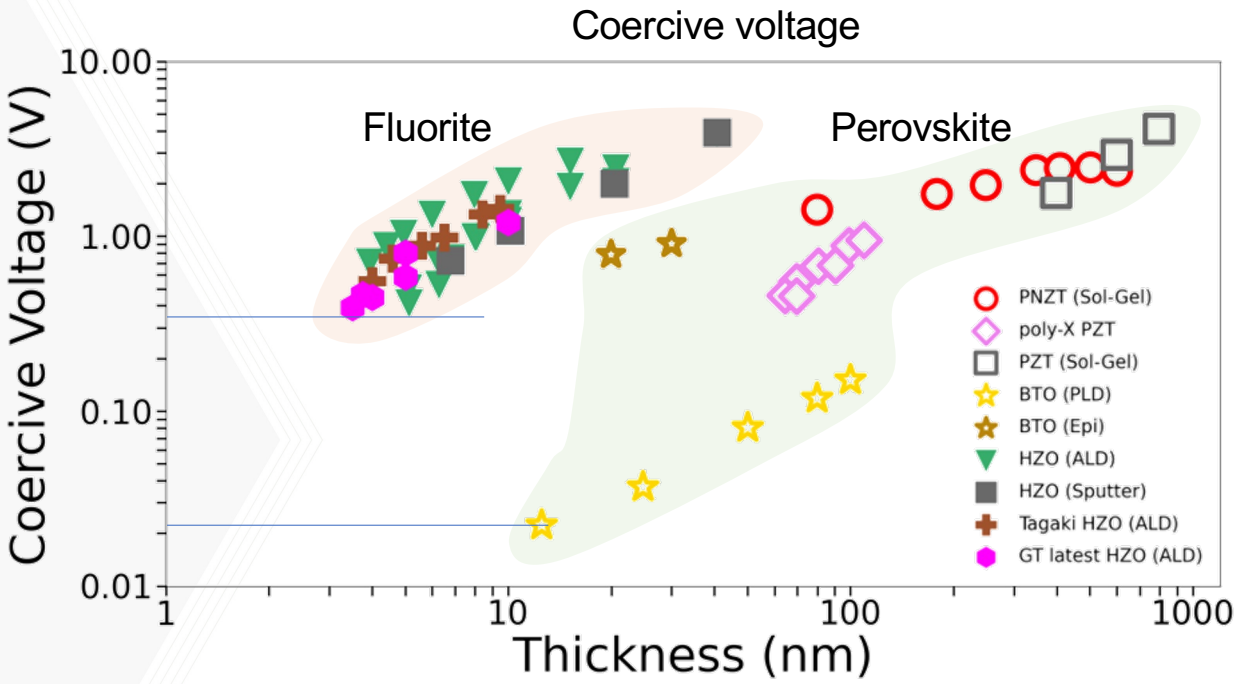
Ferroelectric Random Access Memory



A lower coercive field (<<1 MV/cm) is required to solve the speed-voltage challenge.

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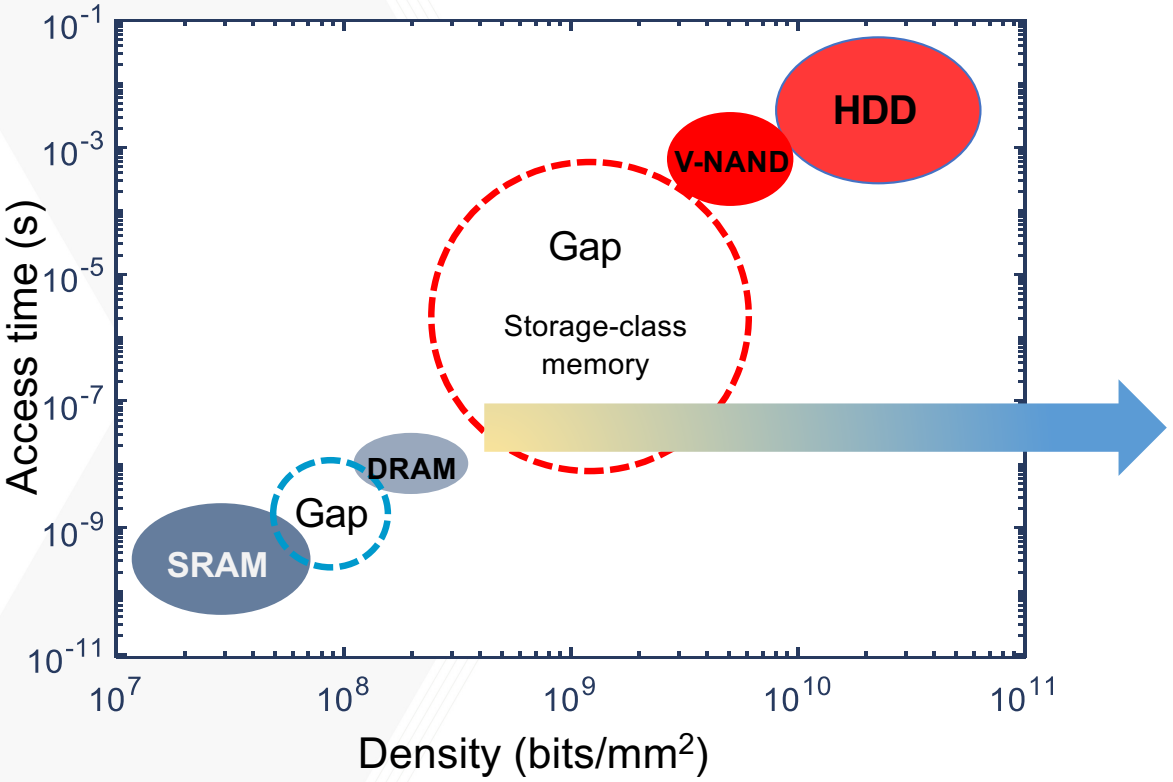
Ferroelectric memories



Ferroelectrics for the DRAM/Storage class space

Micron
Dual Layer 3-D stacked FRAM
Capacity – 32 Gb (Sk Hynix DRAM –-8 Gb)
Latency – 180 ns (LPDDR5 – 60 ns)
Density – 450 Mb/mm^2
Challenge: Speed-voltage trade-off

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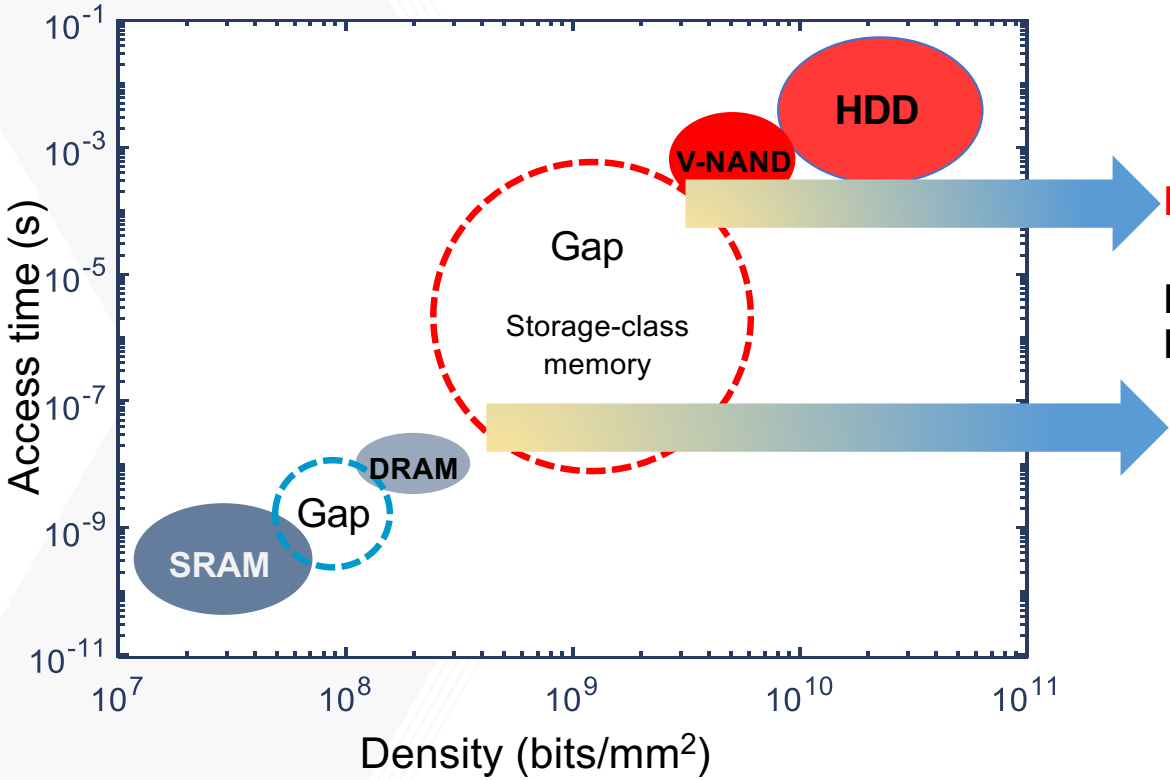
Ferroelectric memories

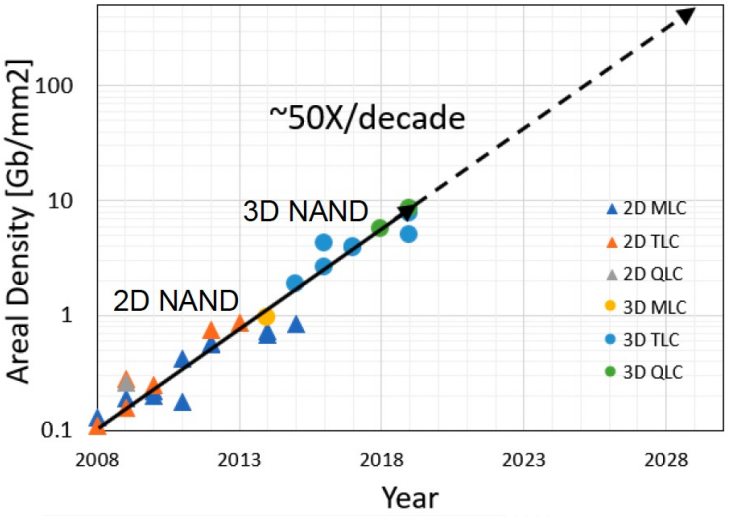


Ferroelectrics for flash?

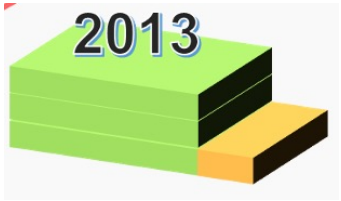
Ferroelectrics for the DRAM/Storage class space

Ramaswamy et al. Micron, IEDM 2024
Dual Layer 3-D stacked FRAM
Capacity – 32 Gb (Sk Hynix DRAM –-8 Gb)
Latency – 180 ns (LPDDR5 – 60 ns)
Density – 450 Mb/mm^2
Challenge: Speed-voltage trade-off

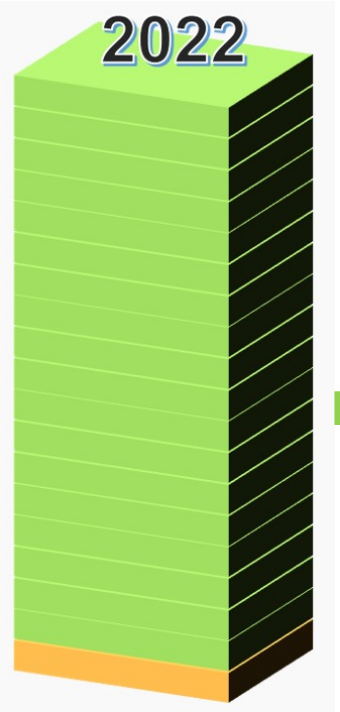
Vertical NAND Scaling



A. Goda, IEEE, TED 2020

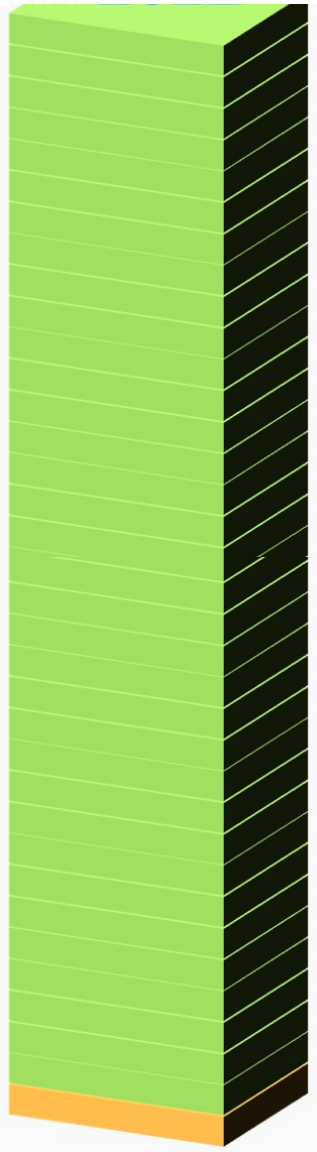


Samsung 24L MLC



?

Samsung 236L TLC
SK Hynix 238L TLC
Micron 232L TLC
192L QLC



Relentless innovations have led to a 50x improvement in bit areal density per decade.

Vertical NAND scaling toward 1000 layers

Layer stacking trend

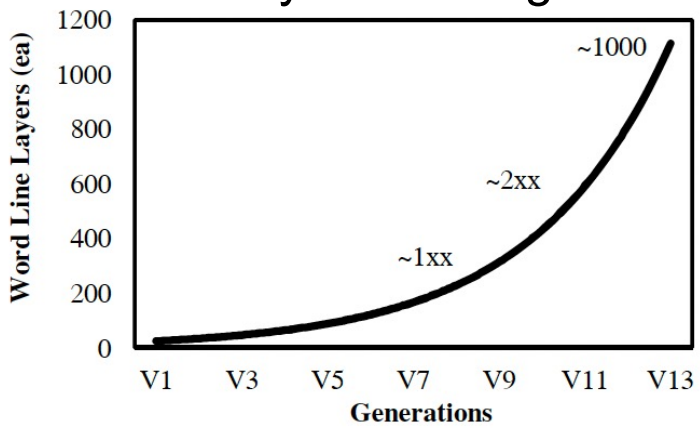


Fig. 1. Number of word line layers by generation

Package thickness limits the NAND chip height.

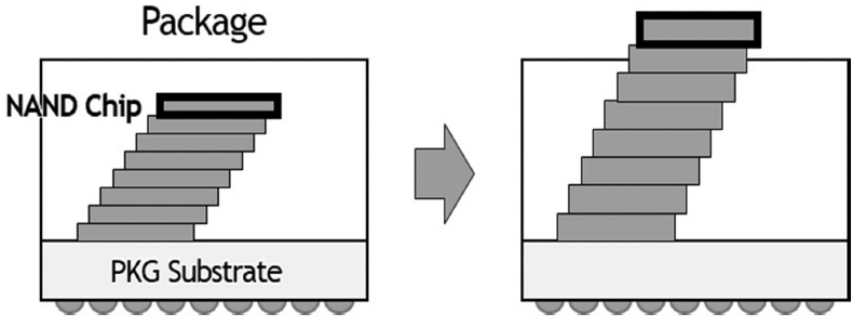
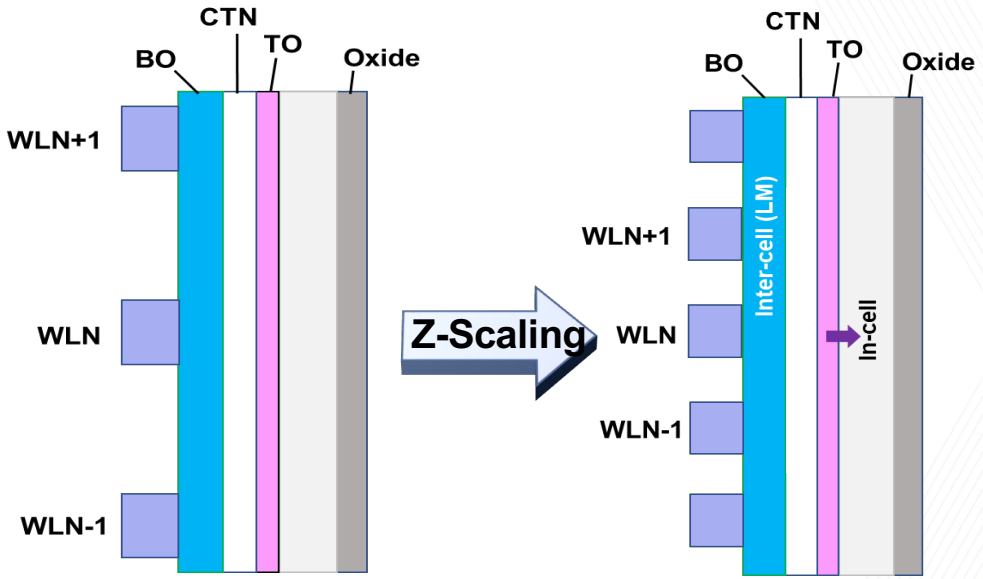


Fig. 4. Package thickness limit with multiple chips

Aggressive Z-scaling is required.

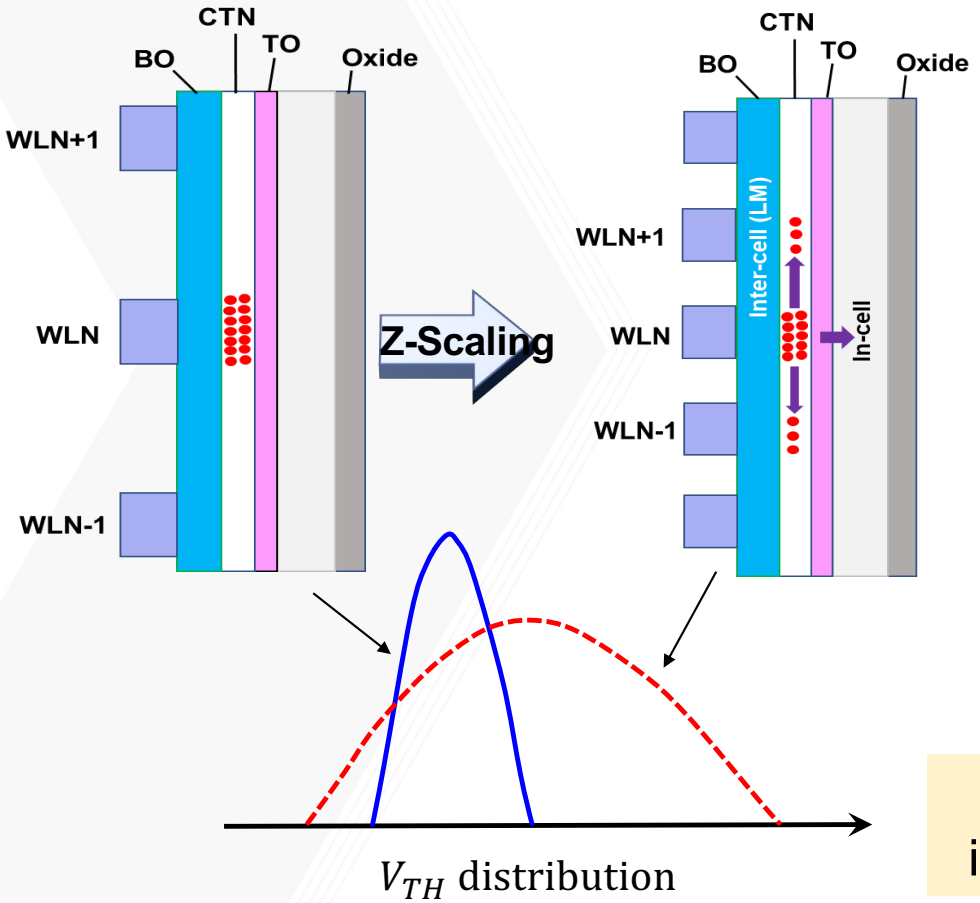


The mold height (cell height) needs to be reduced dramatically.

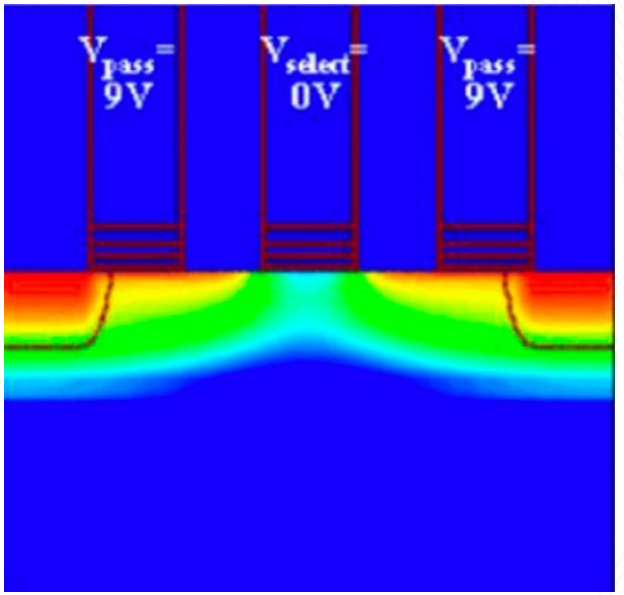
Han et al. Fundamental Issues in VNAND Integration Toward More Than 1K Layers. IEDM 2023. Paper 35.1

Challenges for 1000+ layer vertical NAND

1 Lateral charge migration



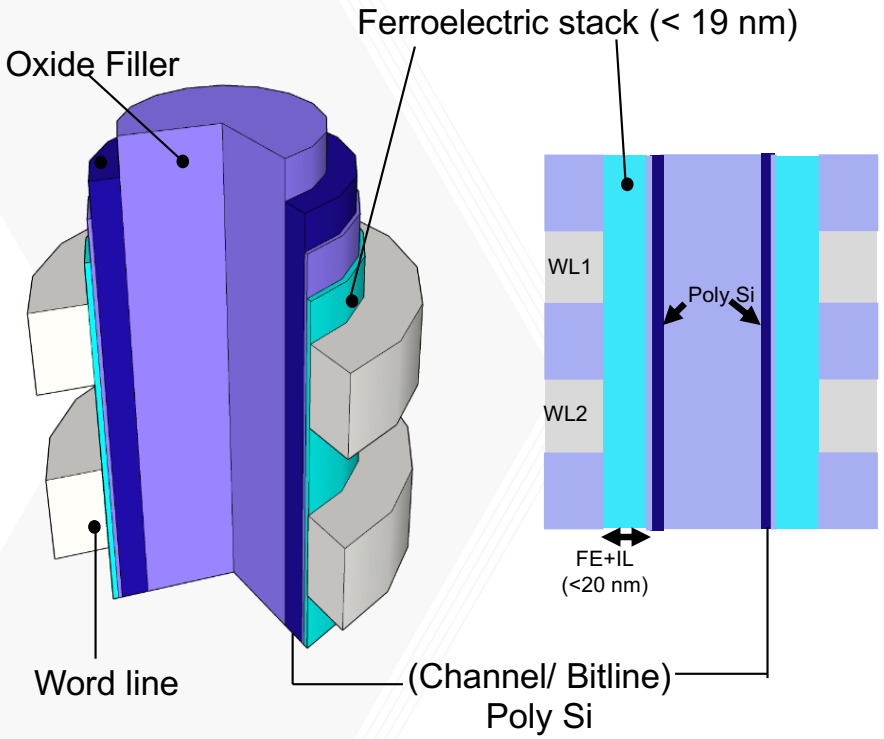
2 High write voltage



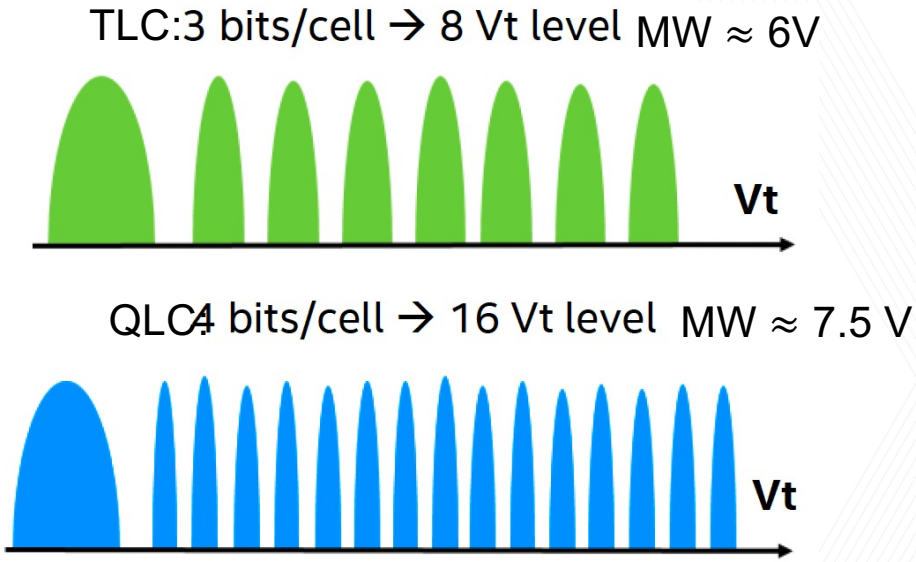
Write voltage of state of the art NAND is >20 V.
Large write voltage affects effective threshold voltage, similar to cell-to-cell interference.

Cell-to-cell interference will significantly increase with aggressive Z-scaling for 1000L VNAND.

Ferroelectricity for NAND storage



To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm



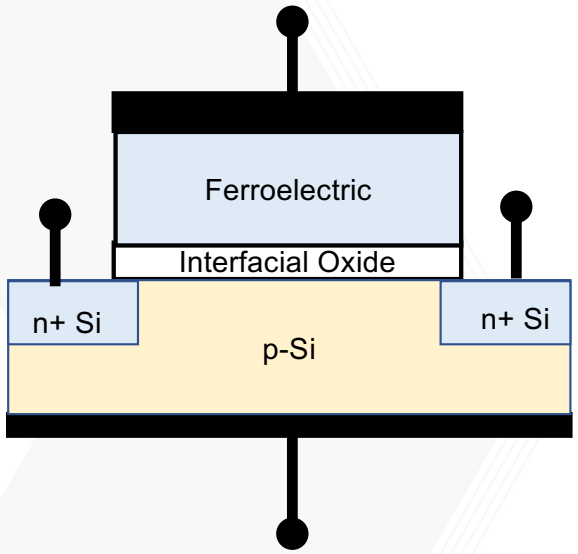
Design constraints

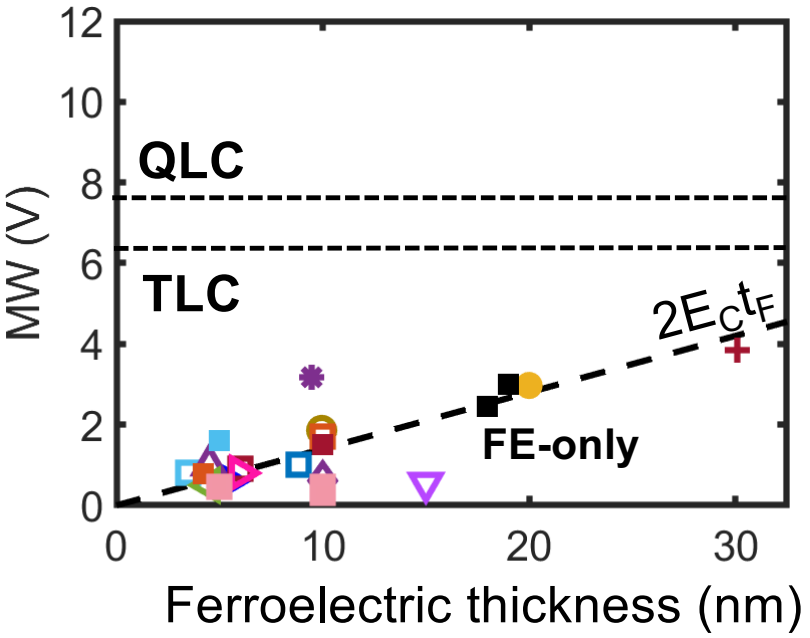
Ferroelectric thickness, $t_{FE} \leq 19$ nm

Write voltage ≤ 15 V

Memory window, MW ≥ 6.5 V

“Fundamental limit” of memory window





- Mueller et al. EDL, 2019.
- Mulaosmanovic et al. TED, 2019.
- Chan et al. ISAF, 2013.
- Chatterjee et al. EDL, 2017.
- Peng et al. EDL, 2019.
- Mueller et al. EDL, 2019.
- Yurchuk et al. IRPS, 2014.
- Chan et al. ISAF, 2013.
- Mueller et al. EDL, 2019.
- Mulaosmanovic et al. TED, 2019.
- Wang et al. APL, 2020.
- Tan et al. EDL, 2021.
- Tan et al. VLSI, 2020.
- Das et al. EDL, 2022.
- Dutta et al. EDL, 2022.
- Dunkel et al. IEDM, 2017.
- Nguyen et al. EDL, 2021.
- Liu et al. EDL, 2019.
- Zacharaki et al. ACS AEM, 2022.
- Tasneem et al. IEDM 2021.
- Tasneem et al. EDL, 2021.
- Khan group

Fundamental limit of the maximum memory window in a ferroelectric FET is $2E_c t_F$.

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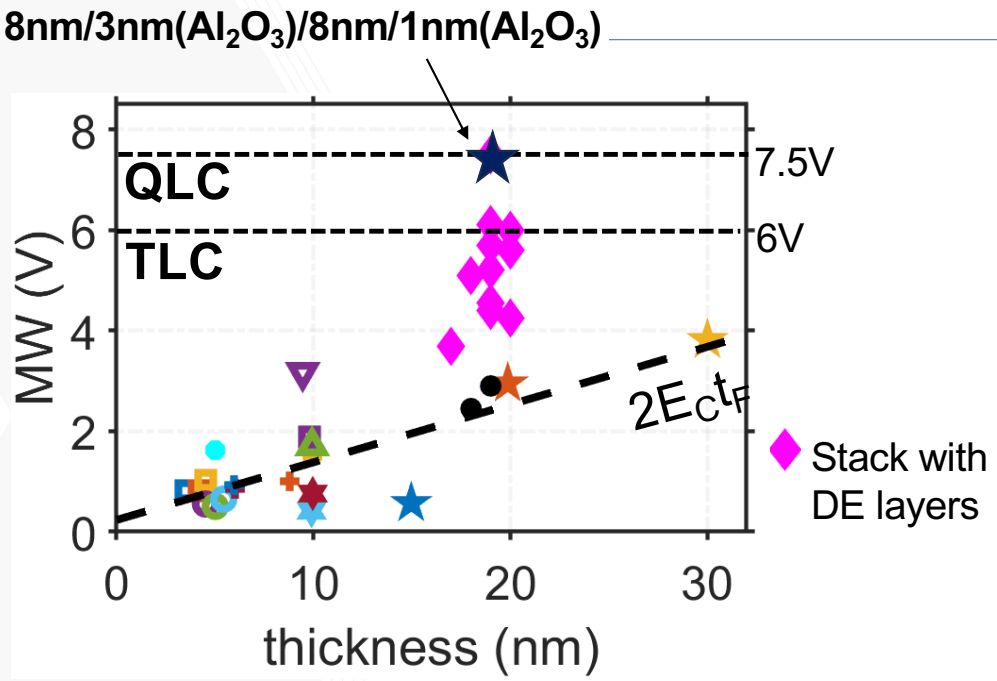
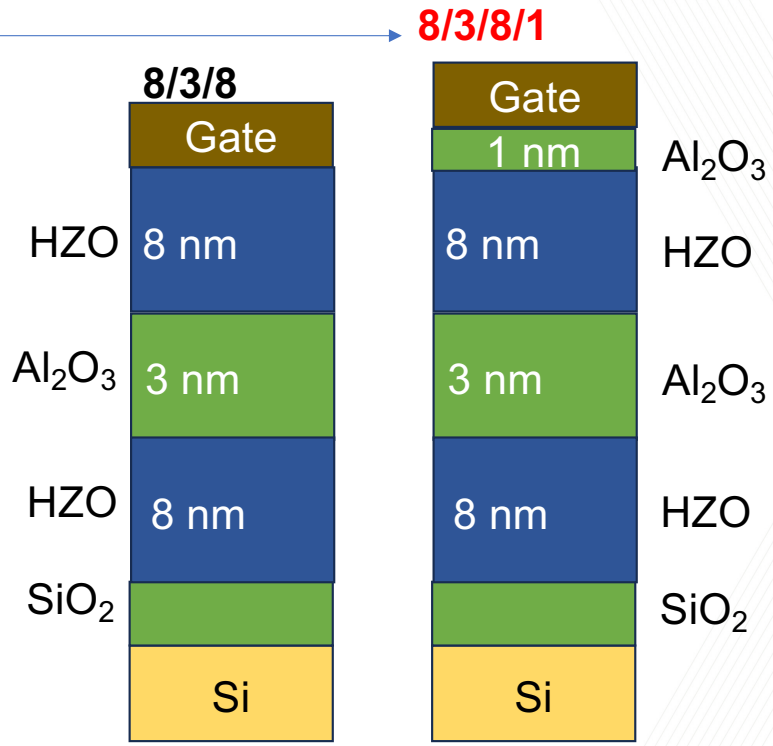
Engineered FEFETs for enhanced MW





A ferroelectric-dielectric gate stack offers several tuning knobs to engineer the MW properties

Das,, et al. "Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications." IEEE, 2023.

Yoon, Sunghyun, et al. "QLC programmable 3D ferroelectric NAND Flash memory by memory window expansion using cell stack engineering." *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. IEEE, 2023.

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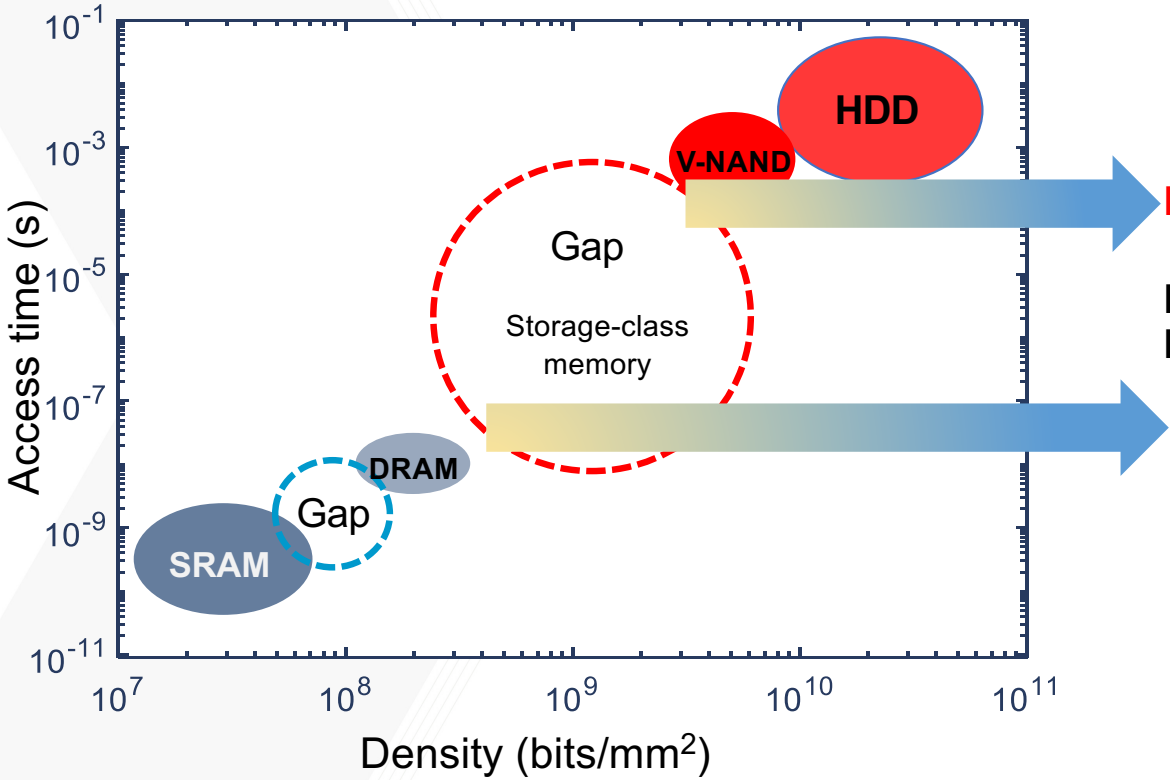
Ferroelectric memories



Ferroelectrics for flash?

Ferroelectrics for the DRAM/Storage class space

Ramaswamy et al. Micron, IEDM 2024
Dual Layer 3-D stacked FRAM
Capacity – 32 Gb (Sk Hynix DRAM –-8 Gb)
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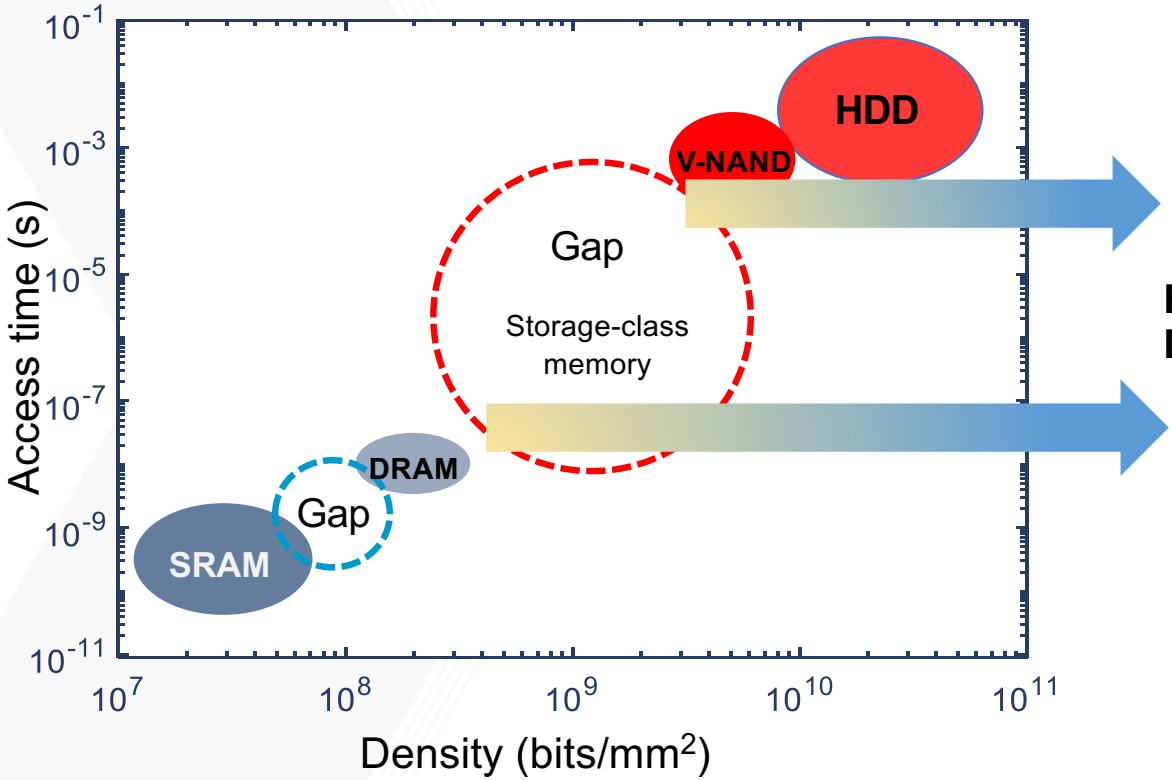
Density – 450 Mb/mm^2
Challenge: Speed-voltage trade-off

Ferroelectric memories



Ferroelectrics for flash

- Voltage scaling below 15 V
- Z-scaling
- Challenge: Disturb and reliability

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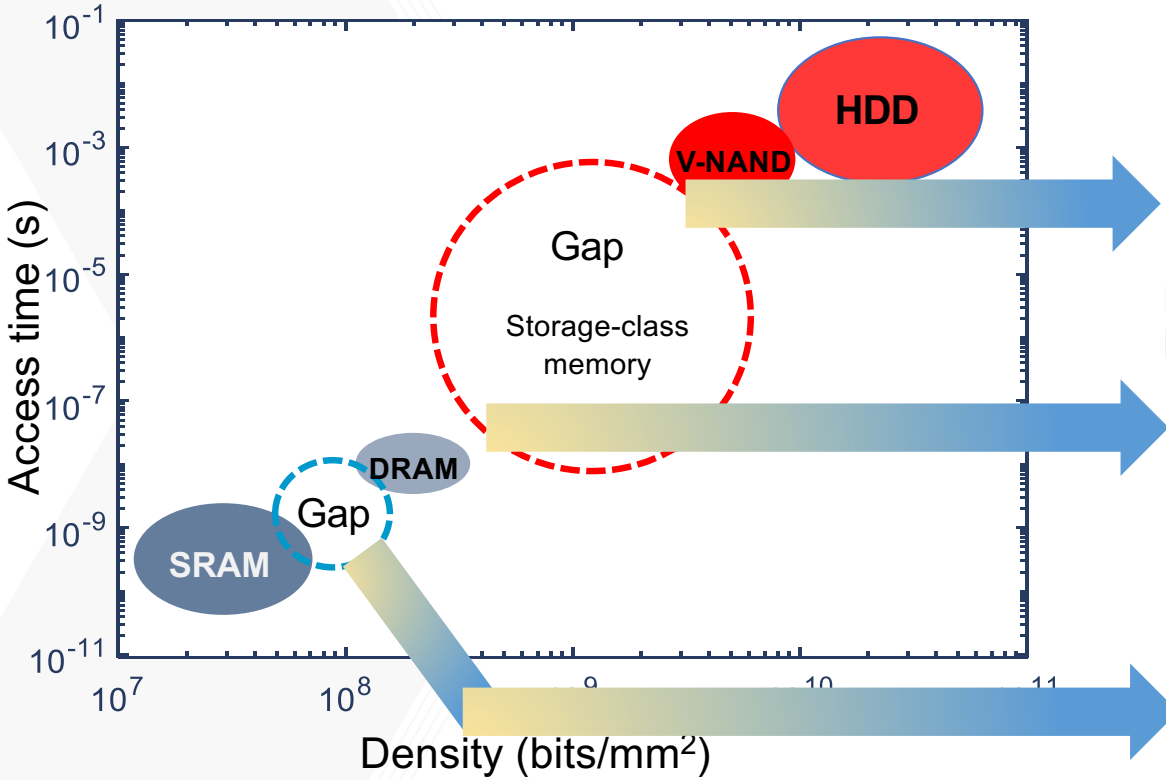

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Ferroelectrics for embedded memories/cache

Ferroelectric Field-Effect Transistor as an embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM[70]	eFlash (FG)	eFlash (SG MONOS)[42]	eFlash (SONOS)[41]	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based)[67]
Cell size	120–150F^2	40F^2	40–60F^2	40–50F^2	50–60F^2	10–30F^2	10–30F^2	30–40F^2	50–60F^2
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 µs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	$>10^{16}$	$>10^{16}$	$\sim10^4$	$\sim10^5$	$\sim10^6$	10^5–10^9	$>10^{10}$	$>10^{12}$	$>10^{14}$

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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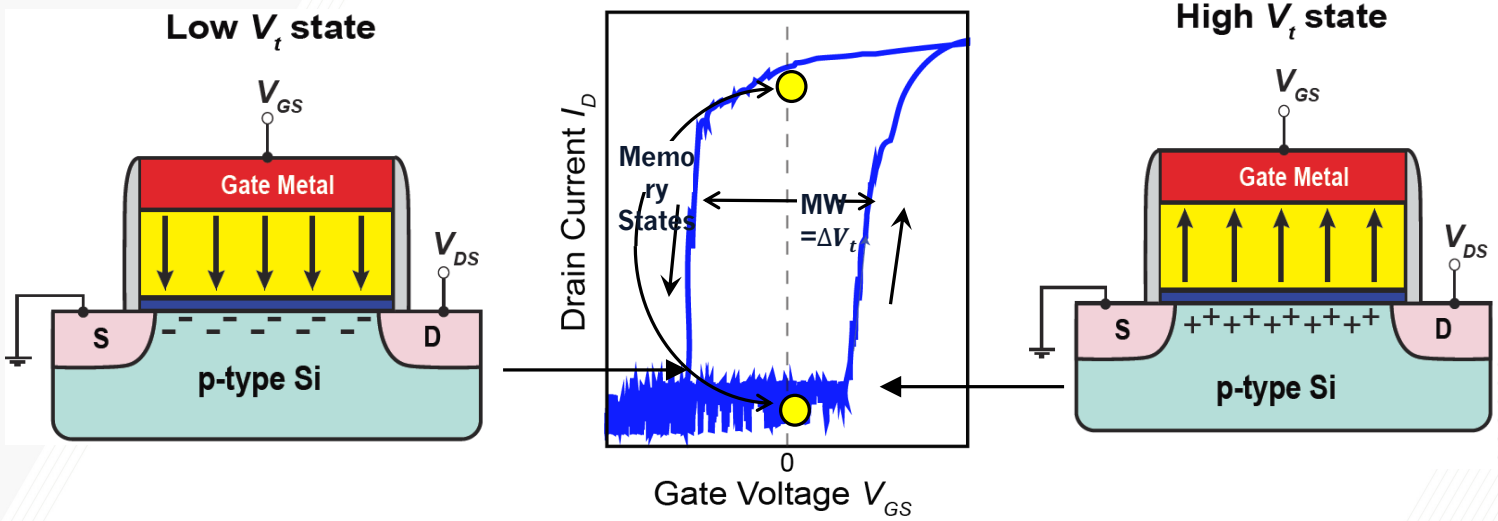
Progress in FEFET technology

1	2	3	4
Write voltage and Memory Window	Read/Write Speed	Device-to-device variation	Reliability and endurance

Specs

<1.5 V write voltage >0.5 V memory window	<10 ns write speed <10 ns read-after-write delay	$\Delta V_{t,3\sigma}$ = 20-50 mV (7 nm node)	>10^{12} cycles



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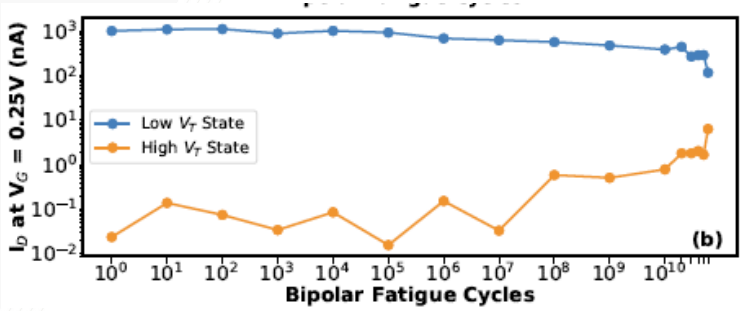
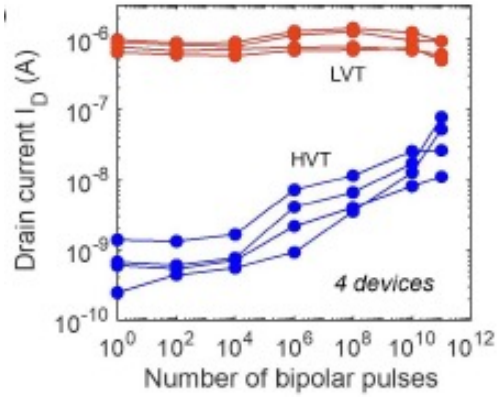


Tan et al. IEEE EDL 42, 994 (2021).



Dutta et al. IEEE EDL 43, 383 (2022).

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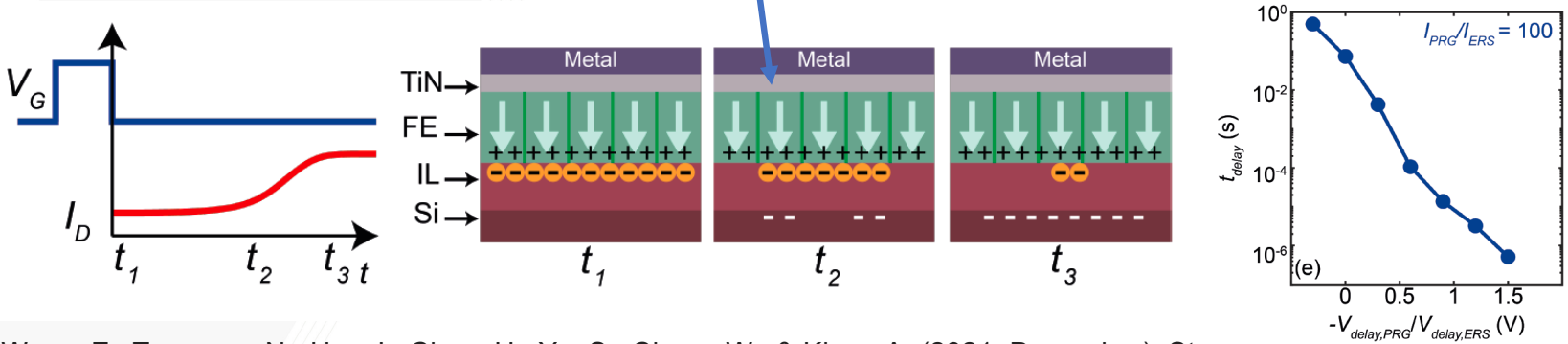

Wang, Z., Tasneem, N., Hur, J., Chen, H., Yu, S., Chern, W., & Khan, A. (2021, December). Standby bias improvement of read after write delay in ferroelectric field effect transistors. In *2021 IEEE International Electron Devices Meeting (IEDM)* (pp. 19-3). IEEE.

Dahan, Yalon, et al. "Sub-nanosecond switching of Si: HfO2 ferroelectric field-effect transistor." *Nano Letters* 23.4 (2023): 1395-1400.

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Progress in FEFET technology

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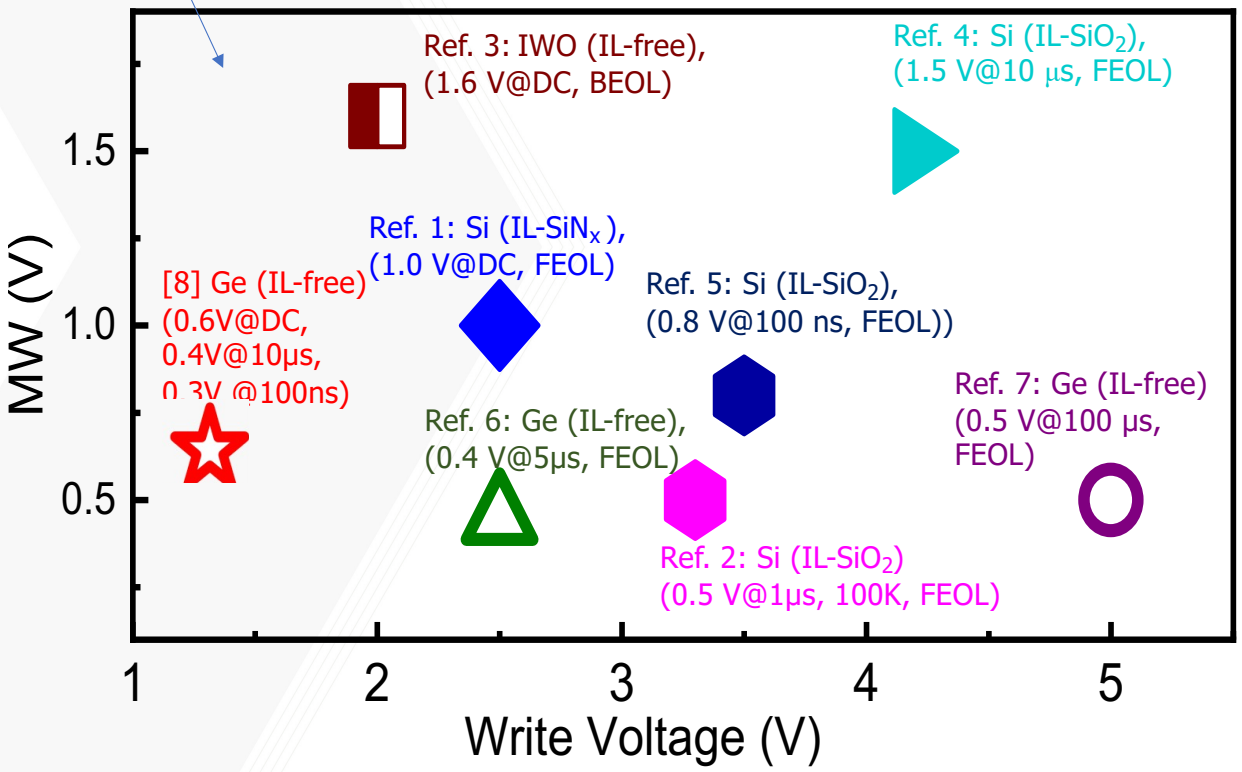
2 Read/Write Speed

3 Device-to-device variation

4 Reliability and endurance



[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
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[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).
[8] Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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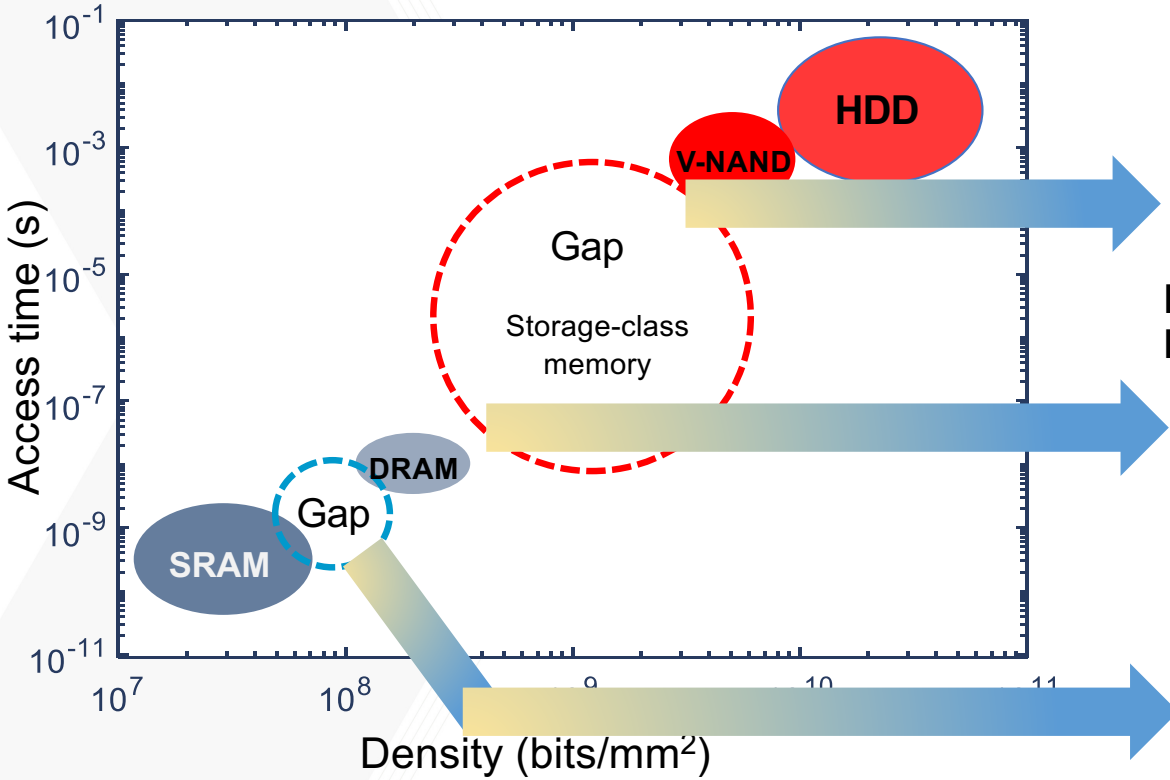
Ferroelectric memories



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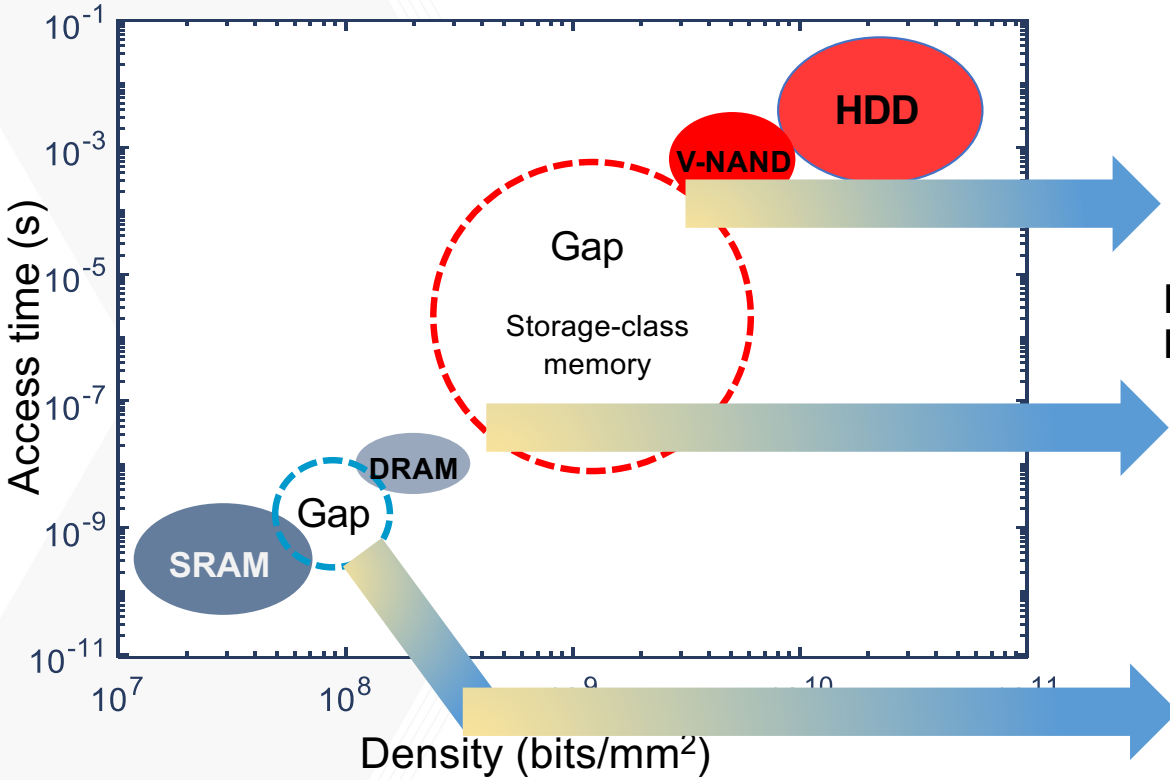

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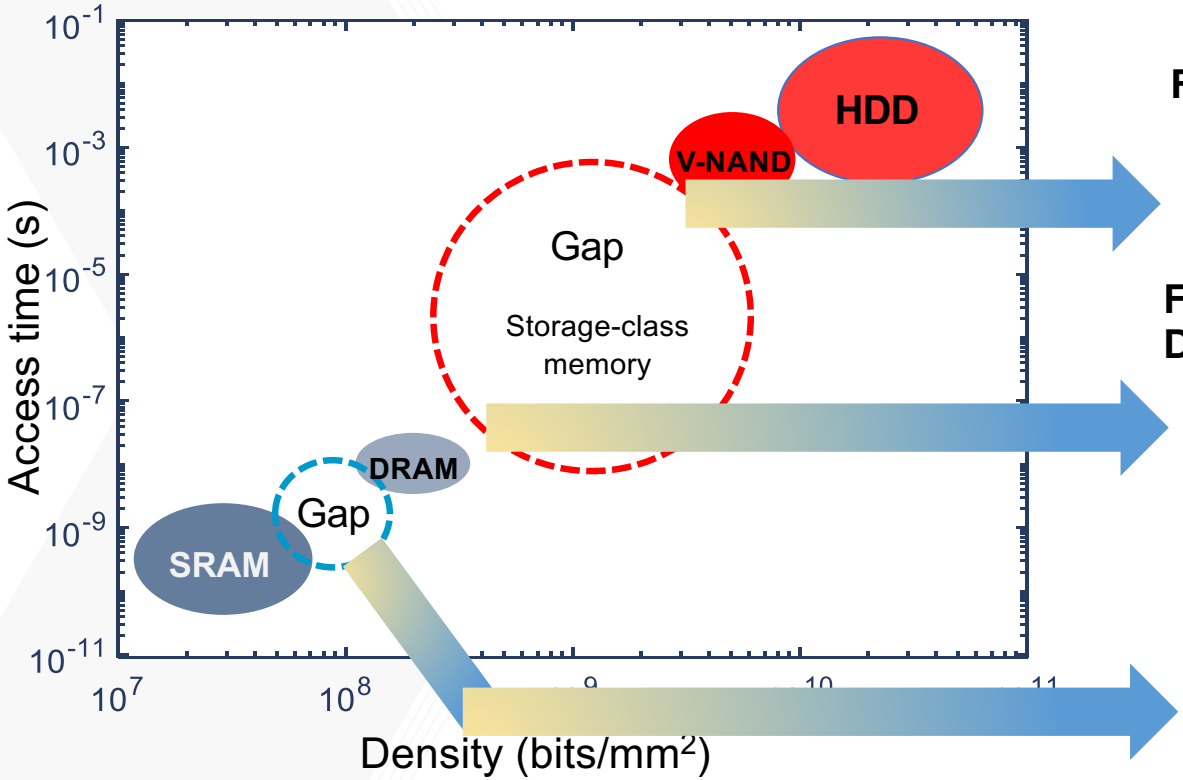
- Density and speed
- Challenge: Speed-voltage trade-off, reliability, variation

Ferroelectric memories



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Also worth noting two other technologies:
1/ Ferroelectric tunnel junctions (FTJ)
2/ Ferroelectric Non-volatile Capacitors (nVCaps)

Thank you!


Prasanna Ravindran


Chinsung Park

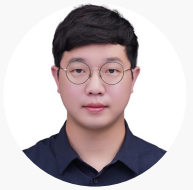

Nashrah Afroze


Jiayi Chen


Priyankka G R


Zekai Wang


Lance Fernandes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