Ferroelectrics for storage applications

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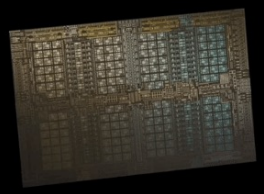
Honolulu, Hawaii 6/15/2024

Georgia Tech

Memory

Hyperscale AI and High-performance Computing



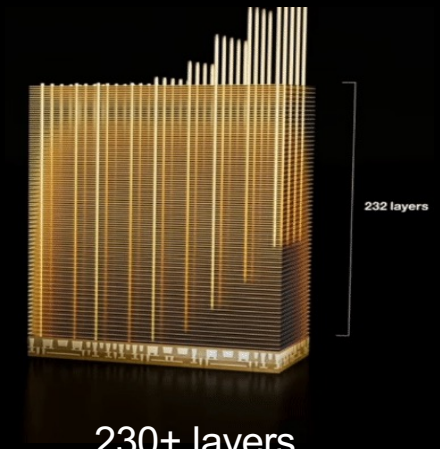
HBM3E: 12-high, 32 GB

1.18 TB/s

Source: NVIDIA

Storage

Client, Mobile, Enterprise



230+ layers

2.4 GB/s

Source: Micron

Embedded

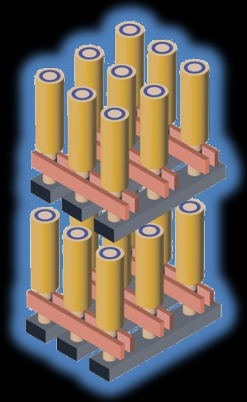
Automotive

14nm eMRAM

16 MB

Source: Forbes

Emerging Memory

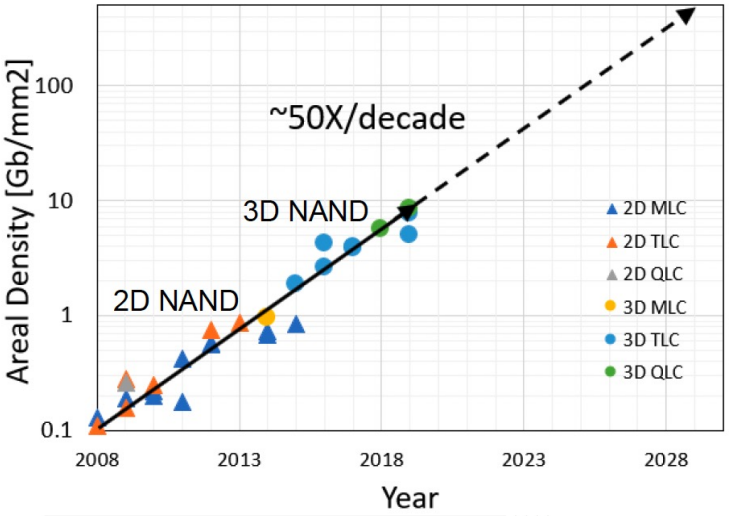


Ferroelectric NV-DRAM

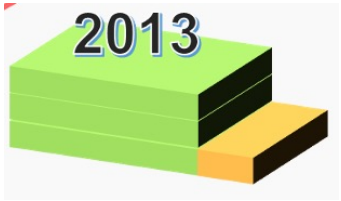
32 Gb, 3D-stacked, multi-layer

Source: IEDM 2023

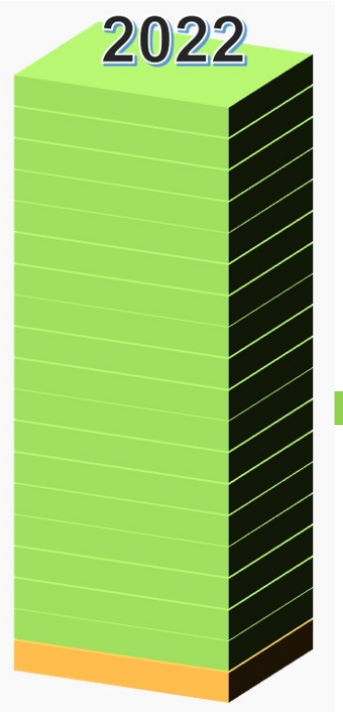
Vertical NAND Scaling



A. Goda, IEEE, TED 2020

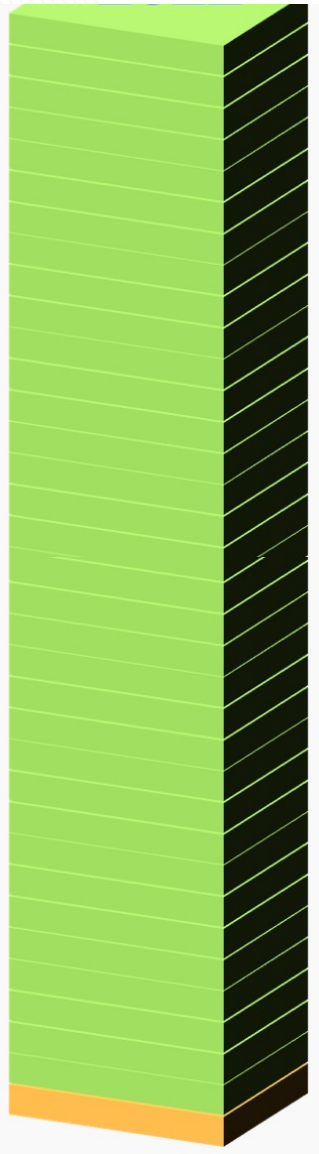


Samsung 24L MLC



Samsung 236L TLC
SK Hynix 238L TLC
Micron 232L TLC
192L QLC

?



Relentless innovations have led to a 50x improvement in bit areal density per decade.

Vertical NAND scaling toward 1000 layers

Layer stacking trend

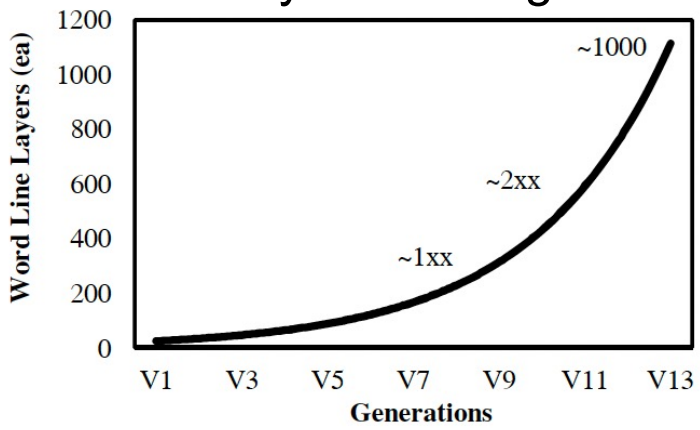


Fig. 1. Number of word line layers by generation

Package thickness limits the NAND chip height.

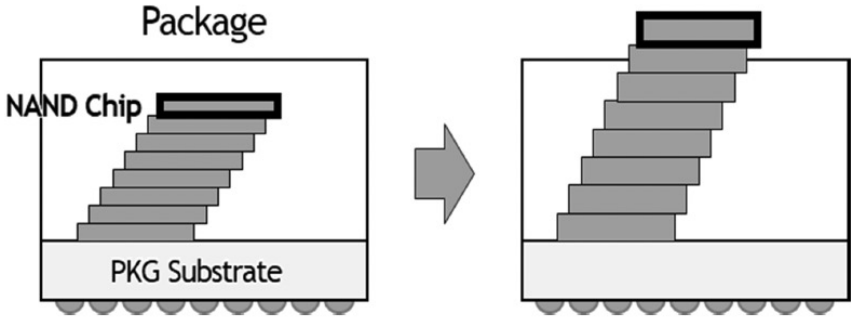
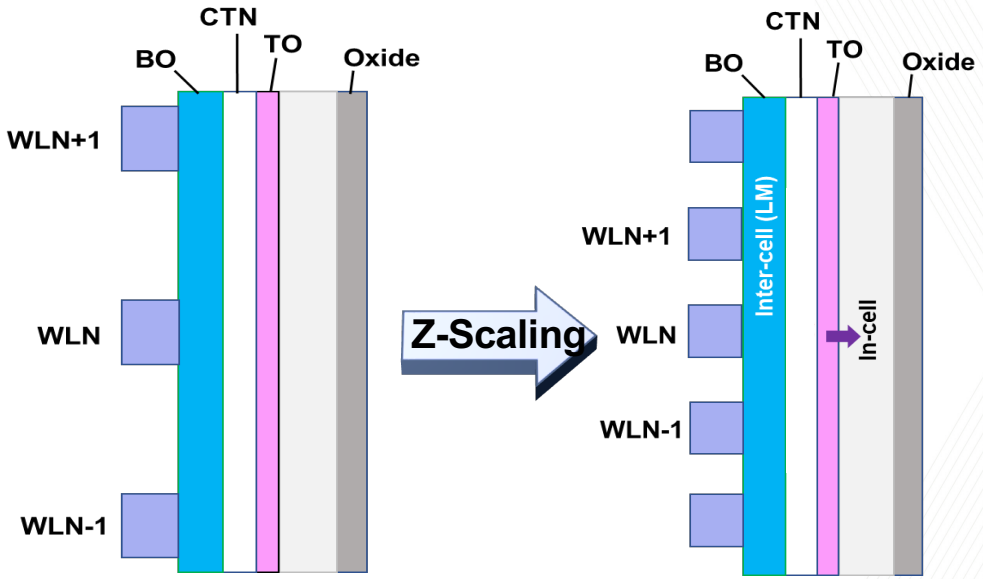


Fig. 4. Package thickness limit with multiple chips

Aggressive Z-scaling is required.

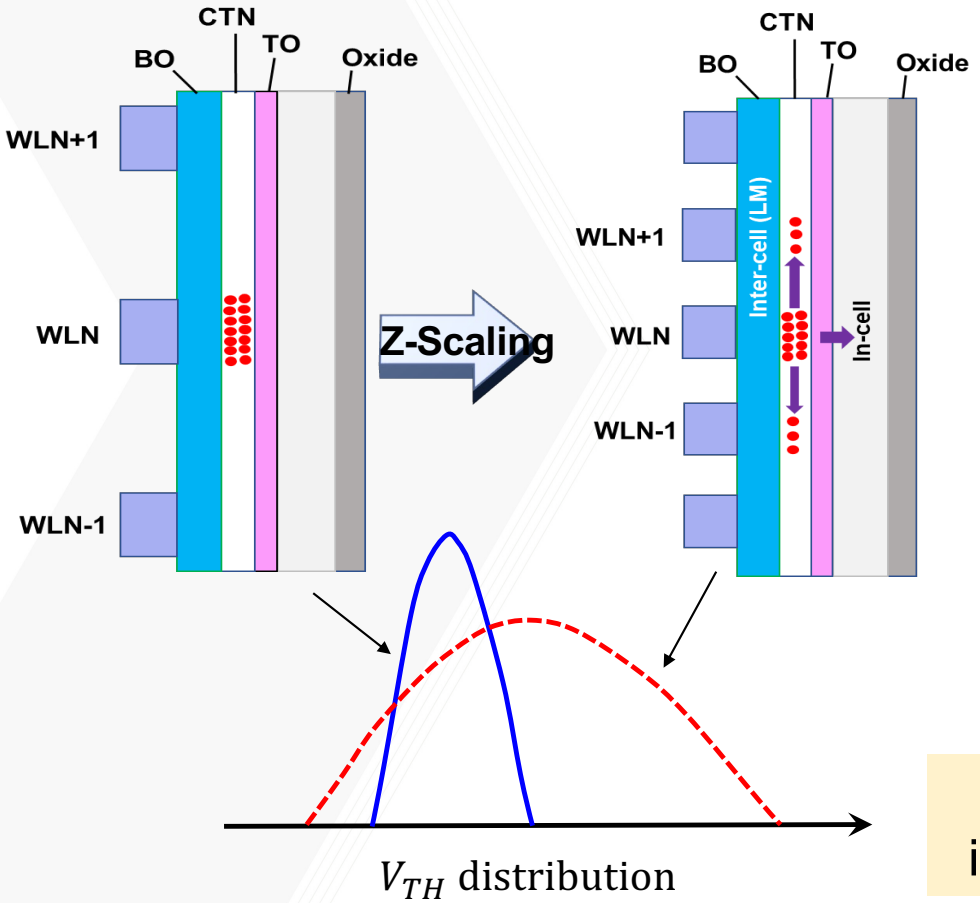


The mold height (cell height) needs to be reduced dramatically.

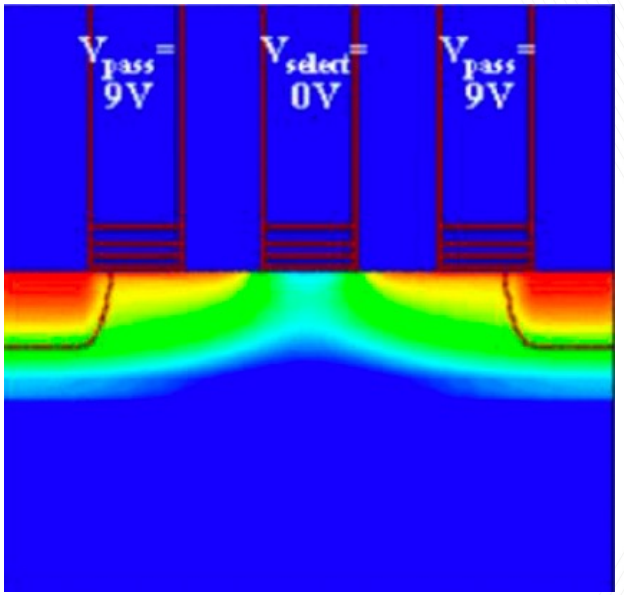
Han et al. Fundamental Issues in VNAND Integration Toward More Than 1K Layers. IEDM 2023. Paper 35.1

Challenges for 1000+ layer vertical NAND

1 Lateral charge migration



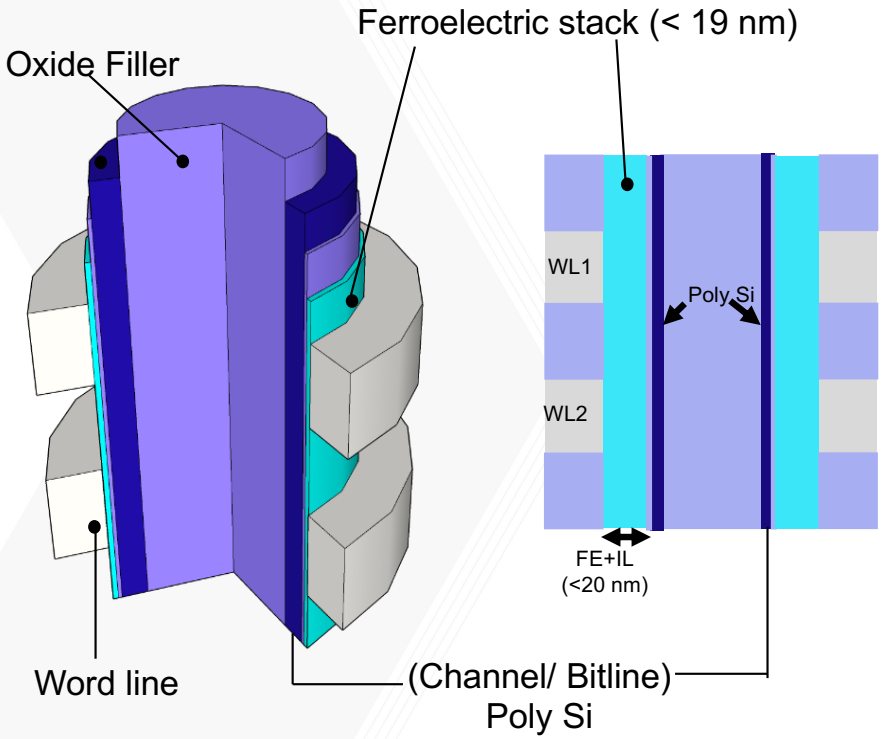
2 High write voltage



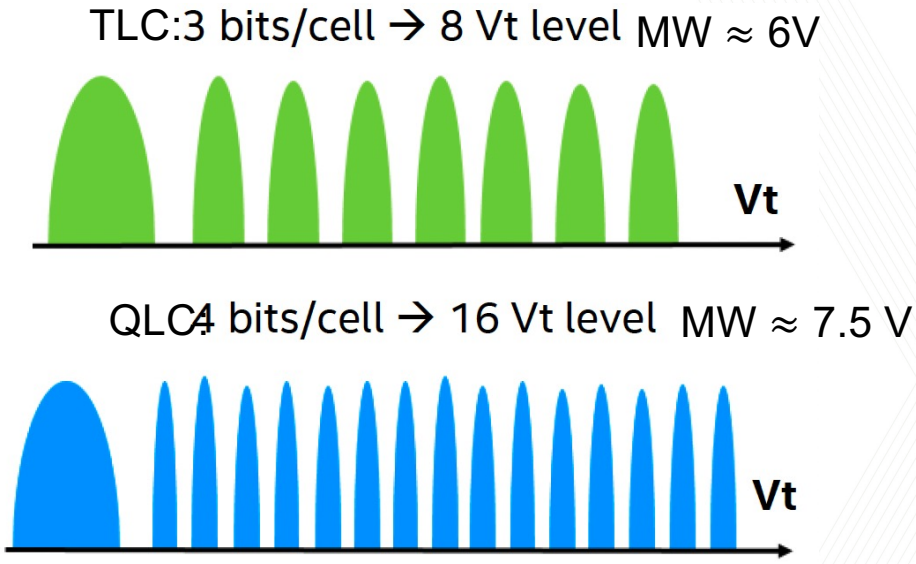
Write voltage of state of the art NAND is >20 V.
Large write voltage affects effective threshold voltage, similar to cell-to-cell interference.

Cell-to-cell interference will significantly increase with aggressive Z-scaling for 1000L VNAND.

Ferroelectricity for NAND storage



To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm



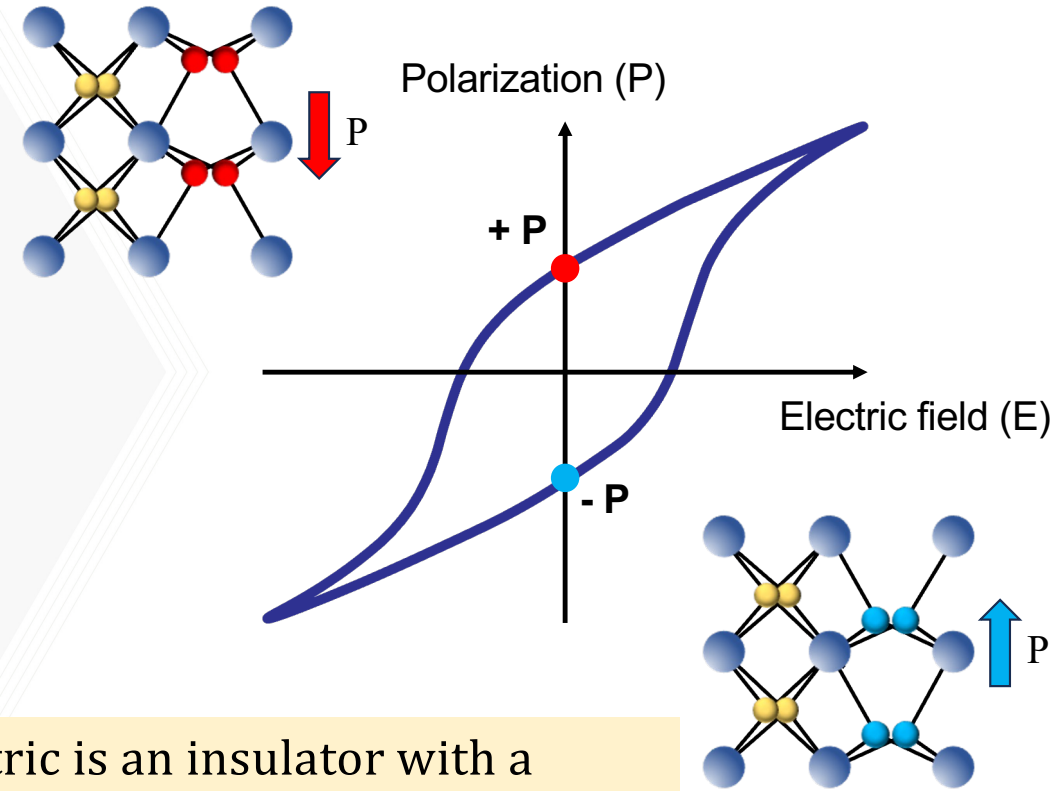
Design constraints

Ferroelectric thickness, $t_{FE} \leq 19$ nm

Write voltage ≤ 15 V

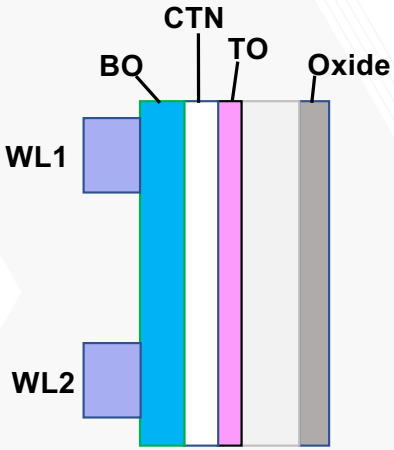
Memory window, MW ≥ 6.5 V

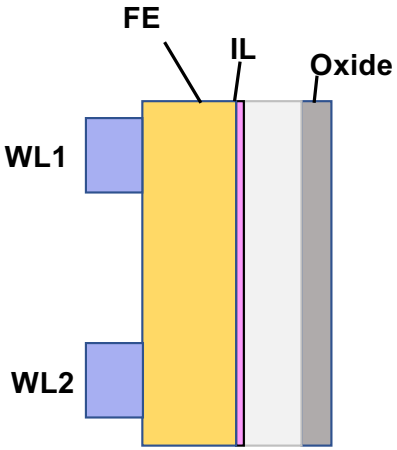
Ferroelectricity



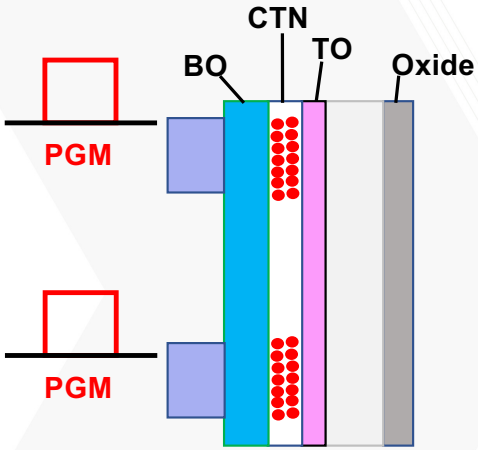
A ferroelectric is an insulator with a spontaneous polarization, which can be switched by a voltage above coercive voltage .

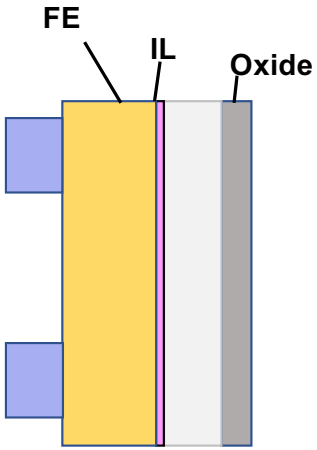
CTF vs FEFET





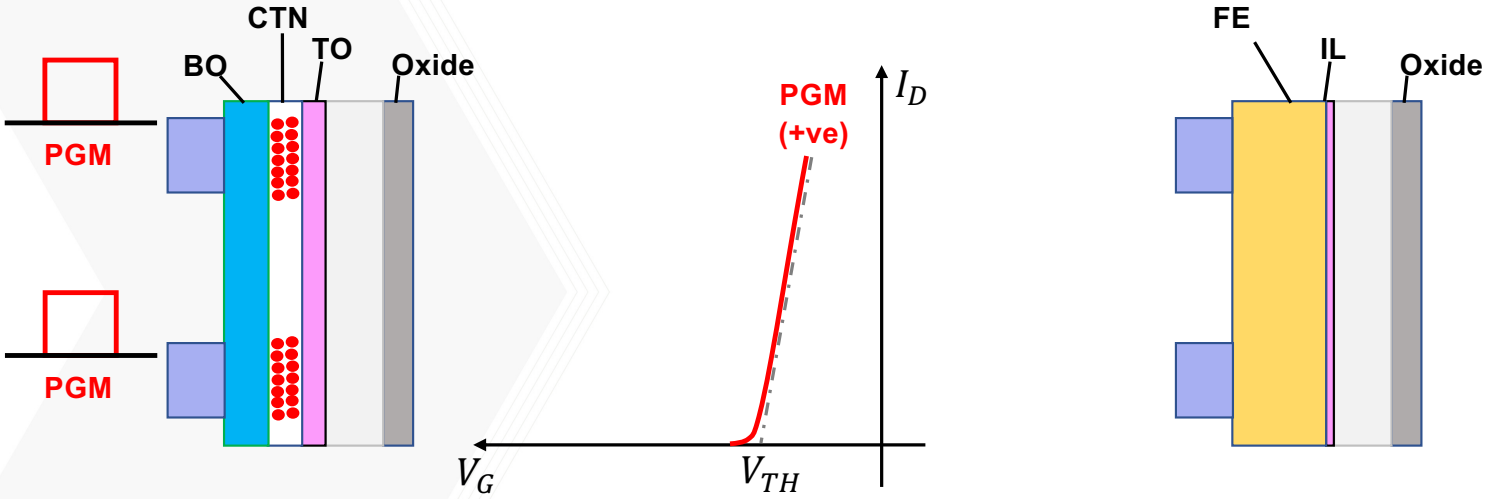
CTF vs FEFET (Program)





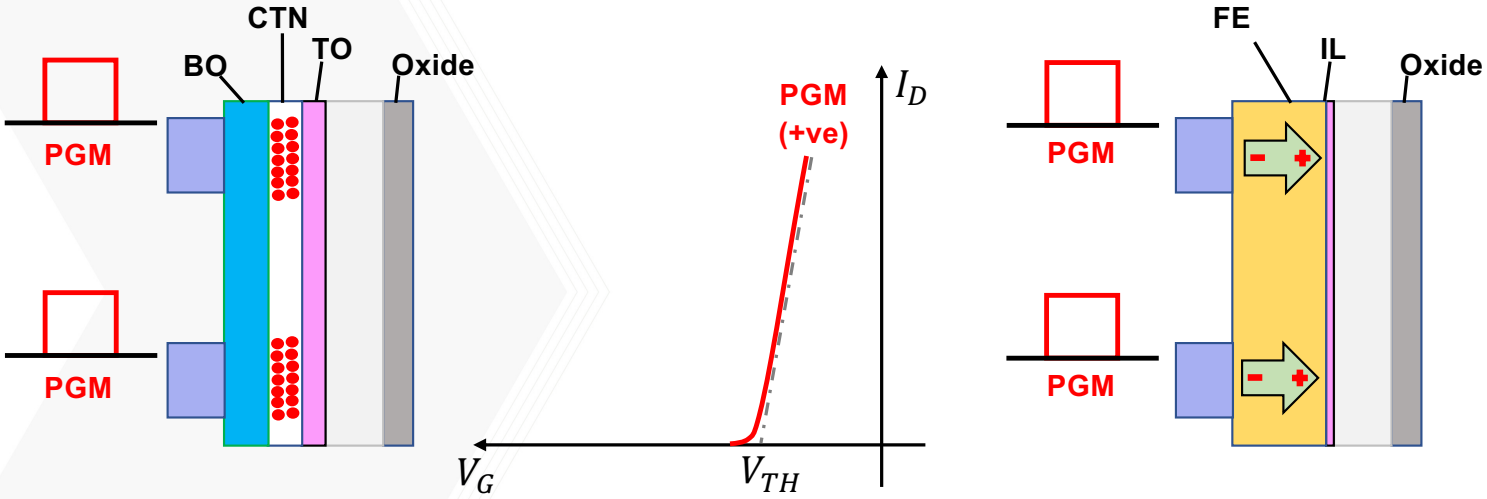
CTF that stores data in the form of charge

CTF vs FEFET (Program)



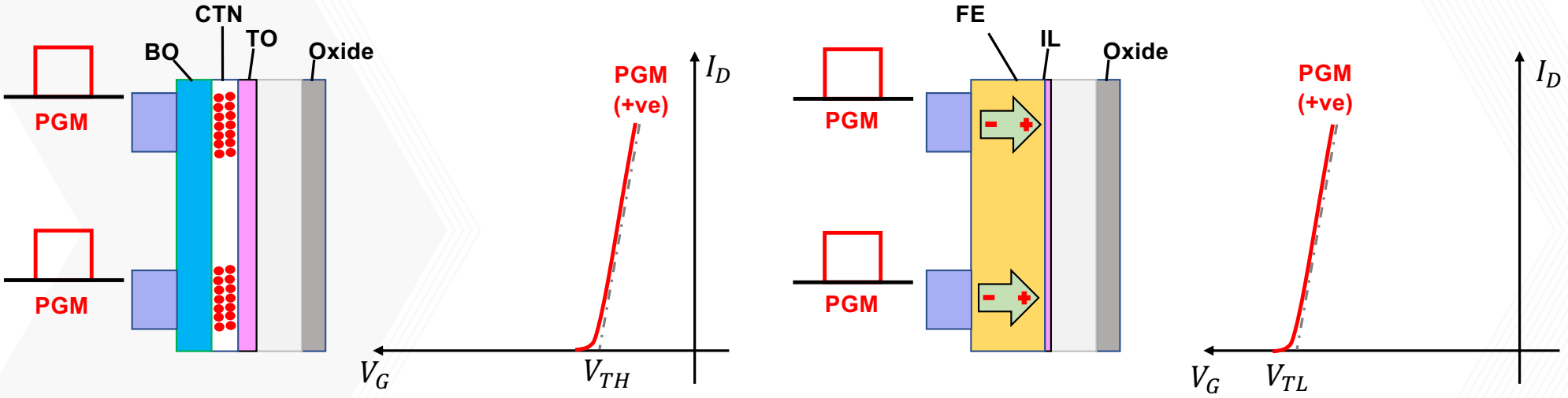
Positive PGM pulse sets the Vt to high Vt state in CTF

CTF vs FEFET (Program)



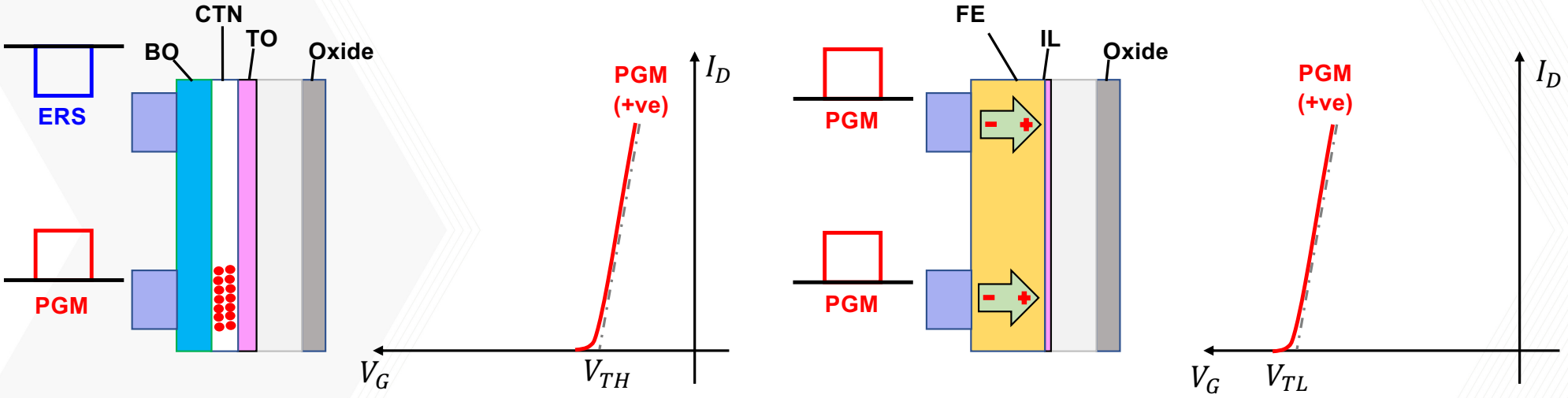
Positive PGM pulse sets the Vt to high Vt state in CTF

CTF vs FEFET (Program)



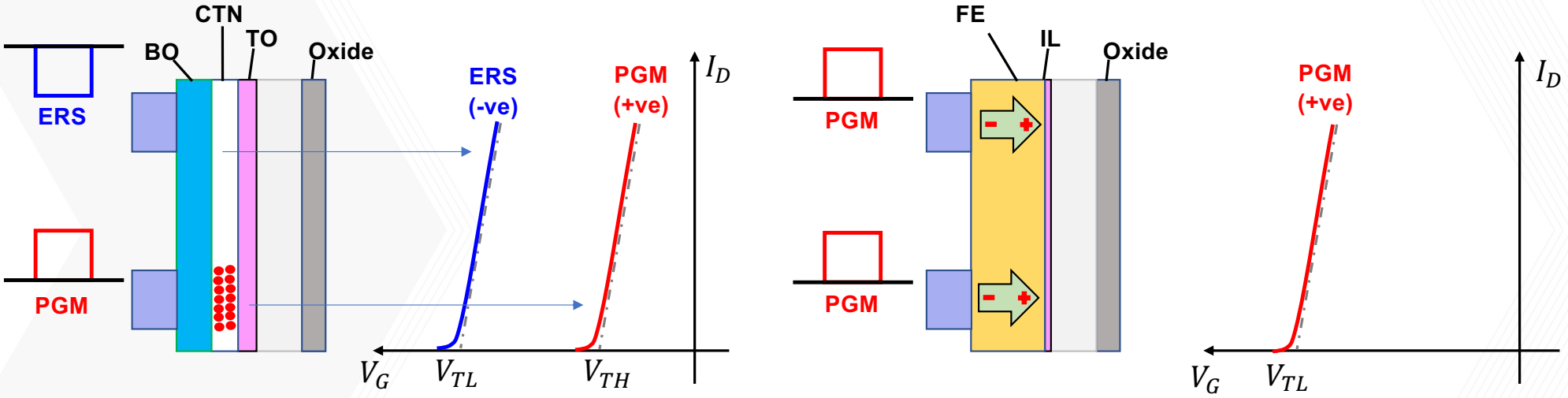
On the contrary, Positive PGM pulse sets the Vt to low Vt state in FEFET

CTF vs FEFET (Erase)



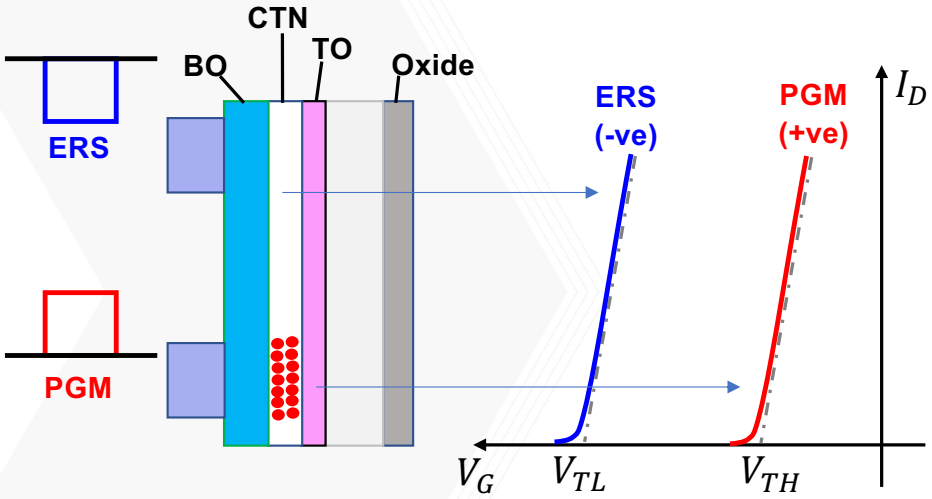
Negative ERS pulse sets the Vt to low Vt state in CTF

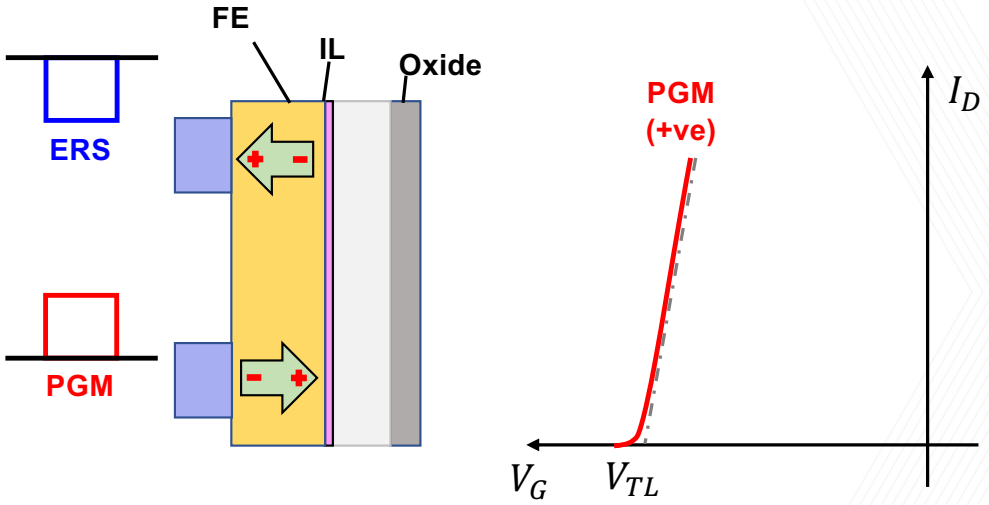
CTF vs FEFET (Erase)



Negative ERS pulse sets the Vt to low Vt state in CTF

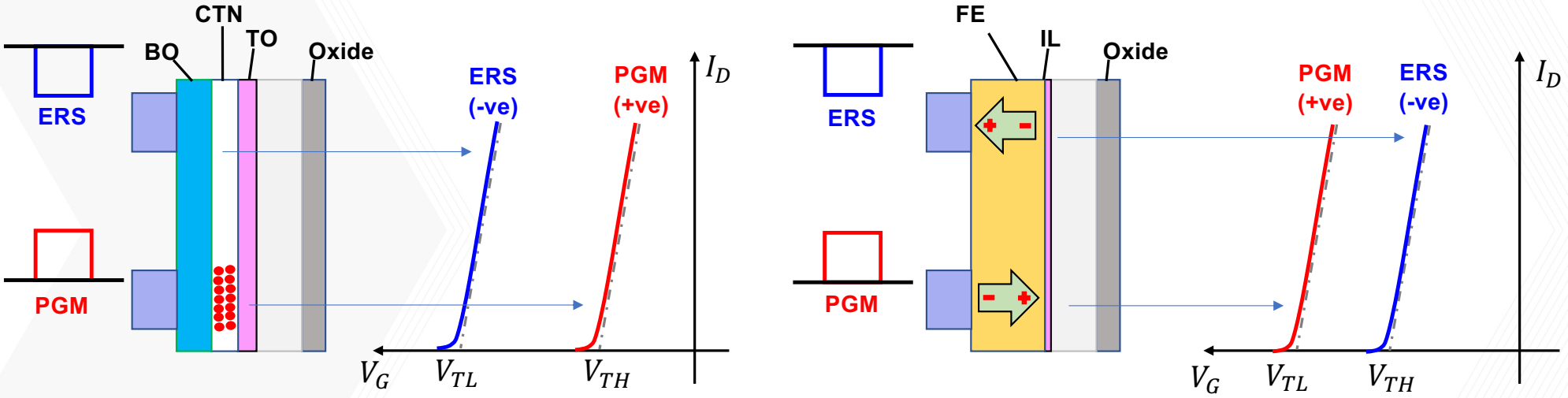
CTF vs FEFET (Erase)





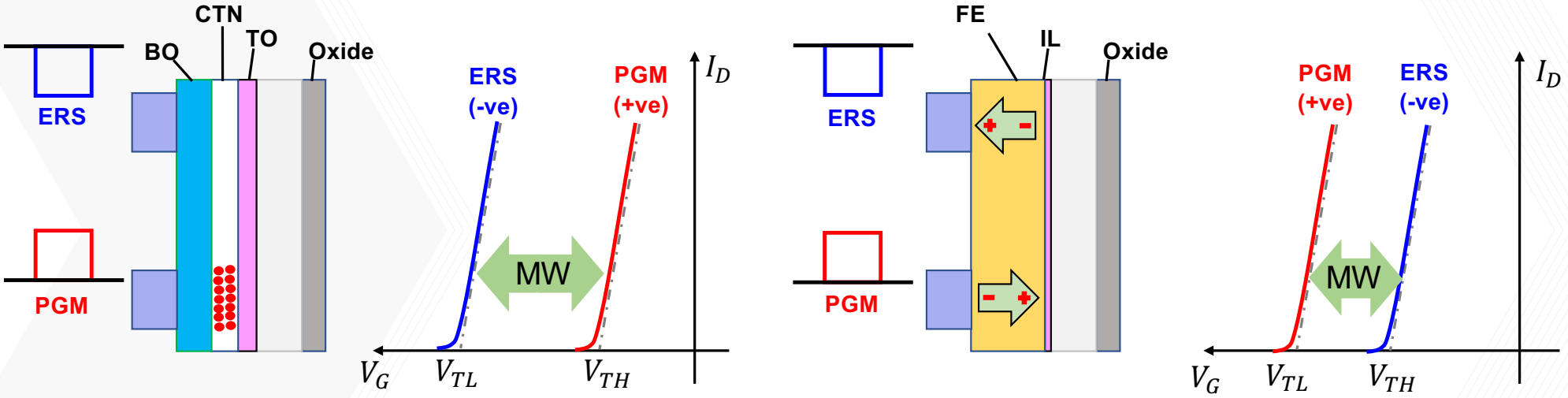
Negative ERS pulse sets the Vt to high Vt state in FEFET

CTF vs FEFET (Erase)



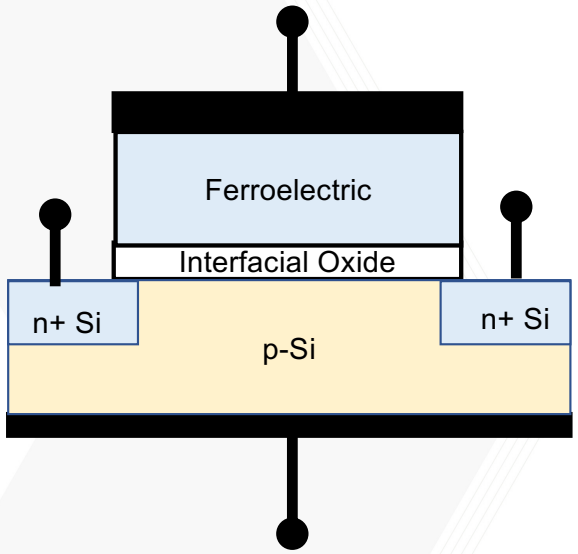
Negative ERS pulse sets the Vt to high Vt state in FEFET

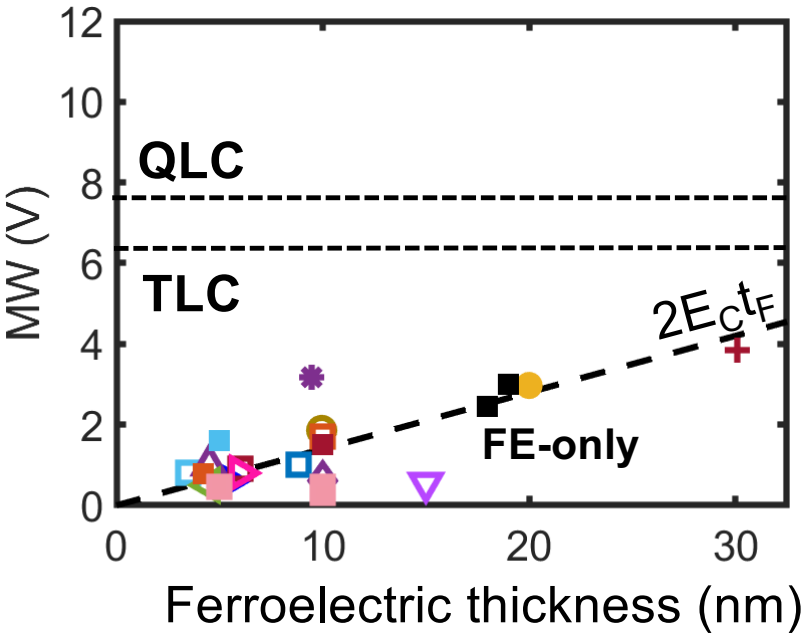
CTF vs FEFET (MW)



$$MW = V_{TH} - V_{TL}$$

“Fundamental limit” of memory window





- Mueller et al. EDL, 2019.
- Mulaosmanovic et al. TED, 2019.
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- Peng et al. EDL, 2019.
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- Das et al. EDL, 2022.
- Dutta et al. EDL, 2022.
- Dunkel et al. IEDM, 2017.
- Nguyen et al. EDL, 2021.
- Liu et al. EDL, 2019.
- Zacharaki et al. ACS AEM, 2022.
- Tasneem et al. IEDM 2021.
- Tasneem et al. EDL, 2021.
- Khan group

Fundamental limit of the maximum memory window in a ferroelectric FET is $2E_c t_F$.

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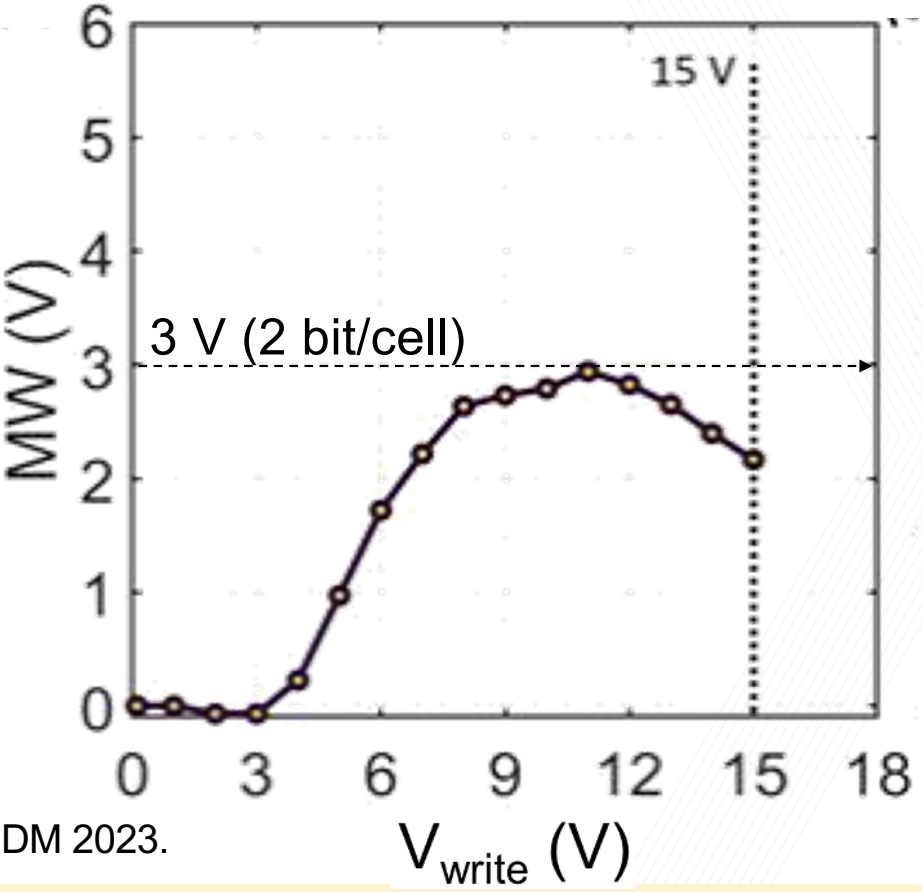
Impact of tunnel dielectric insertion

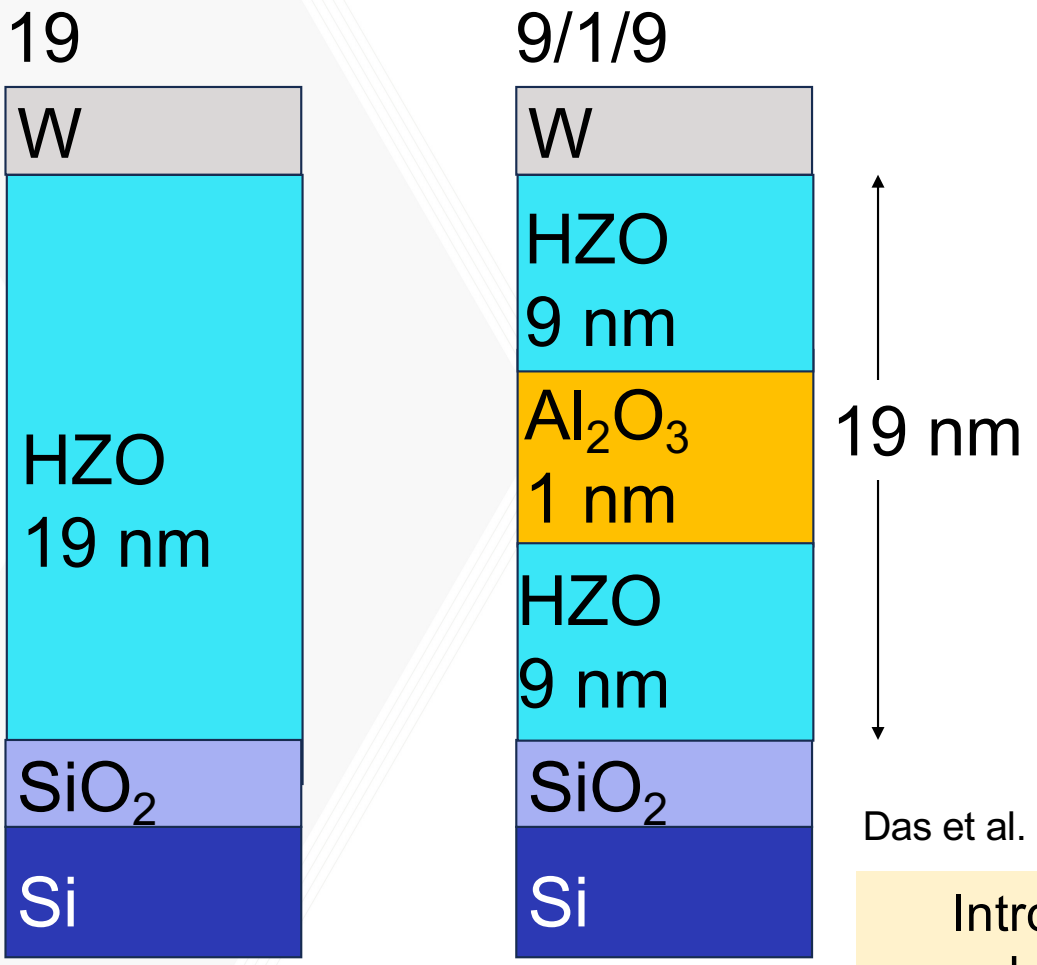
19

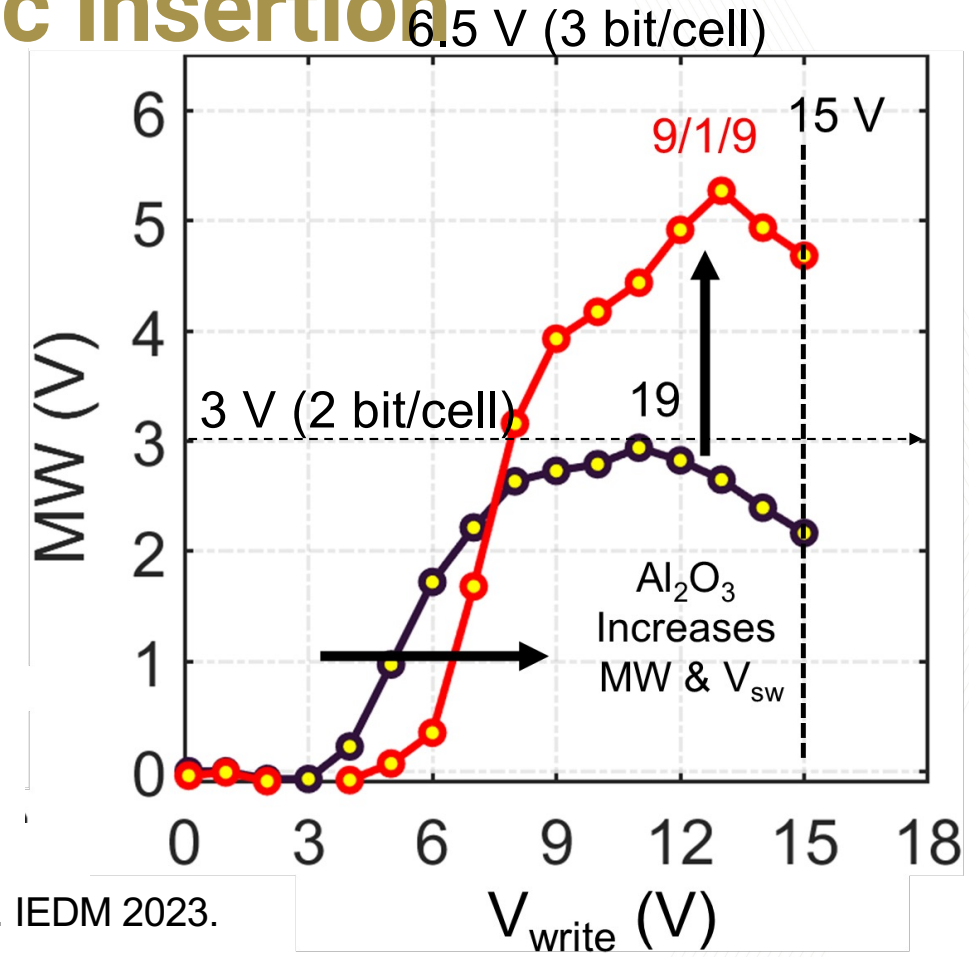


Das et al. IEDM 2023.

10 nm HZO layer leads to maximum memory window of 2.9 V.

Impact of tunnel dielectric insertion

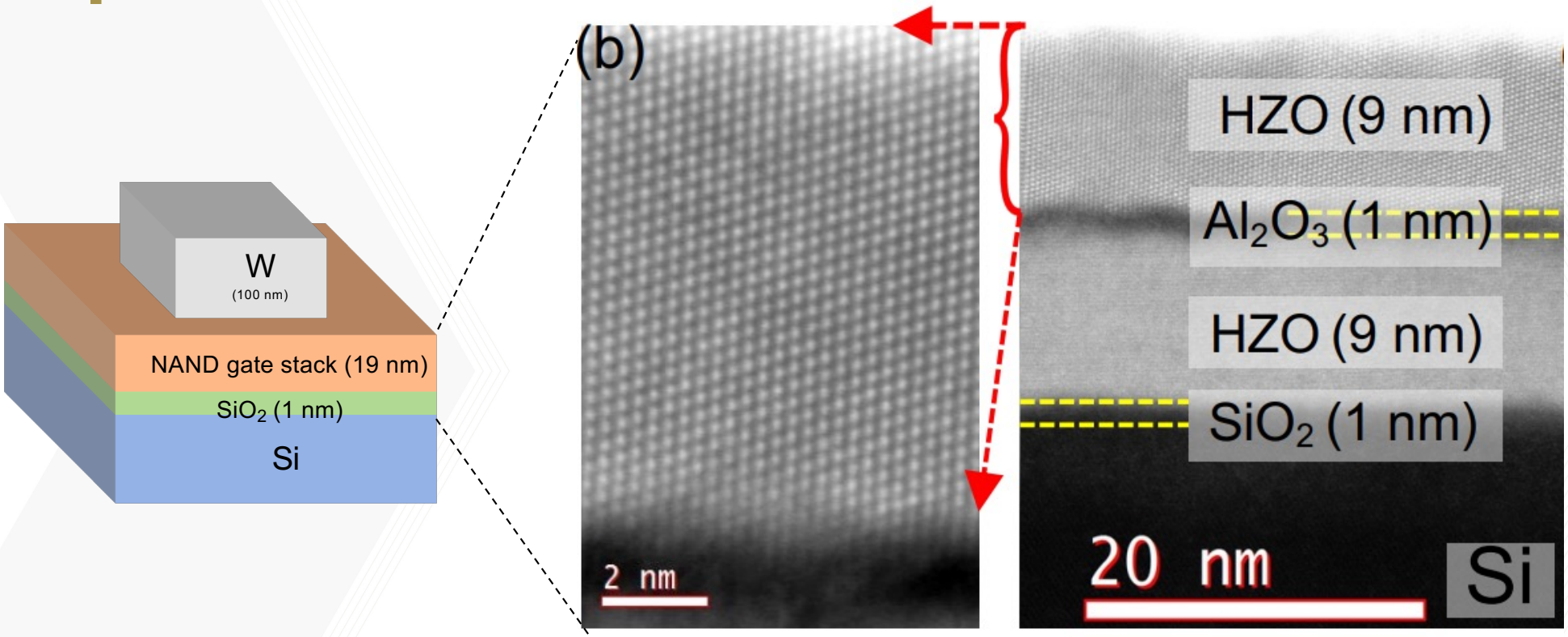




Das et al. IEDM 2023.

Introducing 1 nm Al_2O_3 intermediate layer dramatically memory window to 5.3 V.

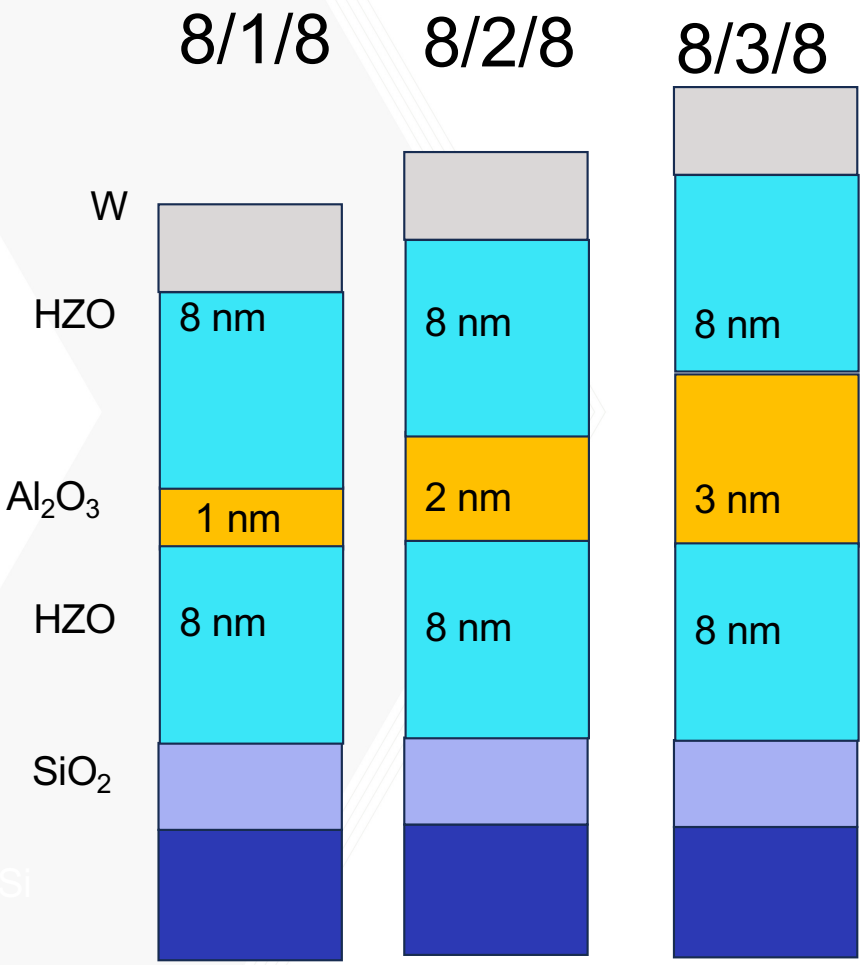
Impact of tunnel dielectric insertion

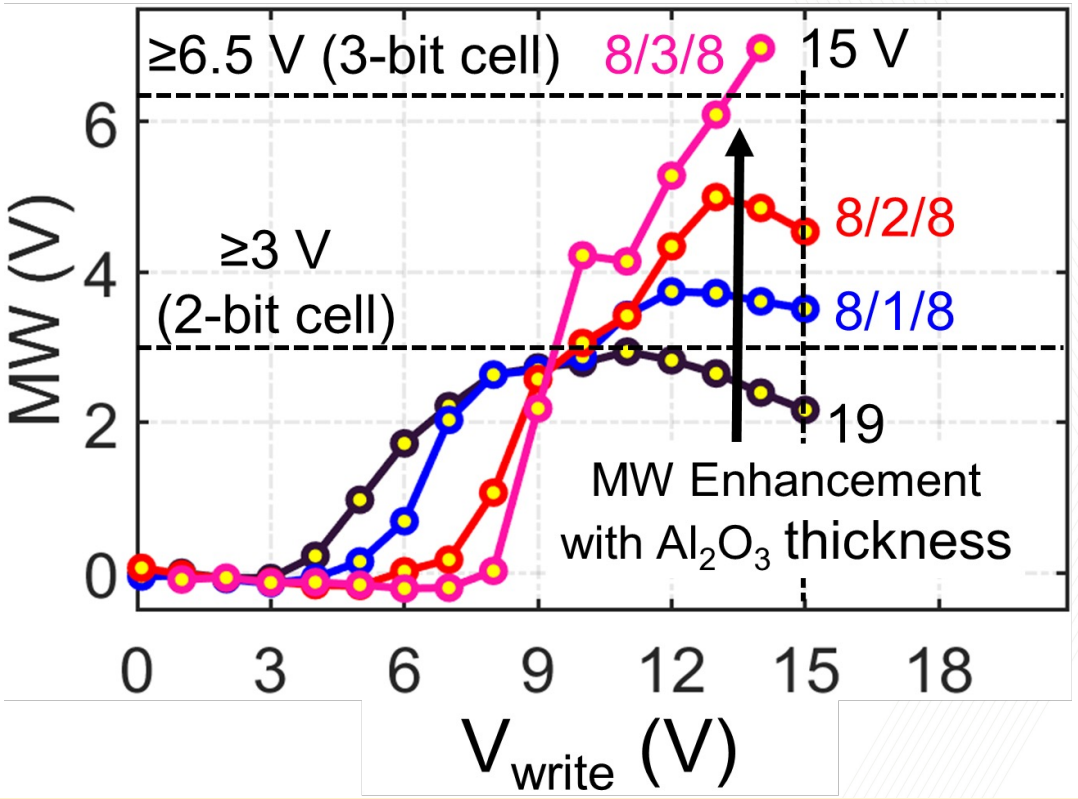


Full coverage of 1 nm Al_2O_3 is observed.

Das et al. Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications. IEDM 2023.

Impact of tunnel dielectric insertion

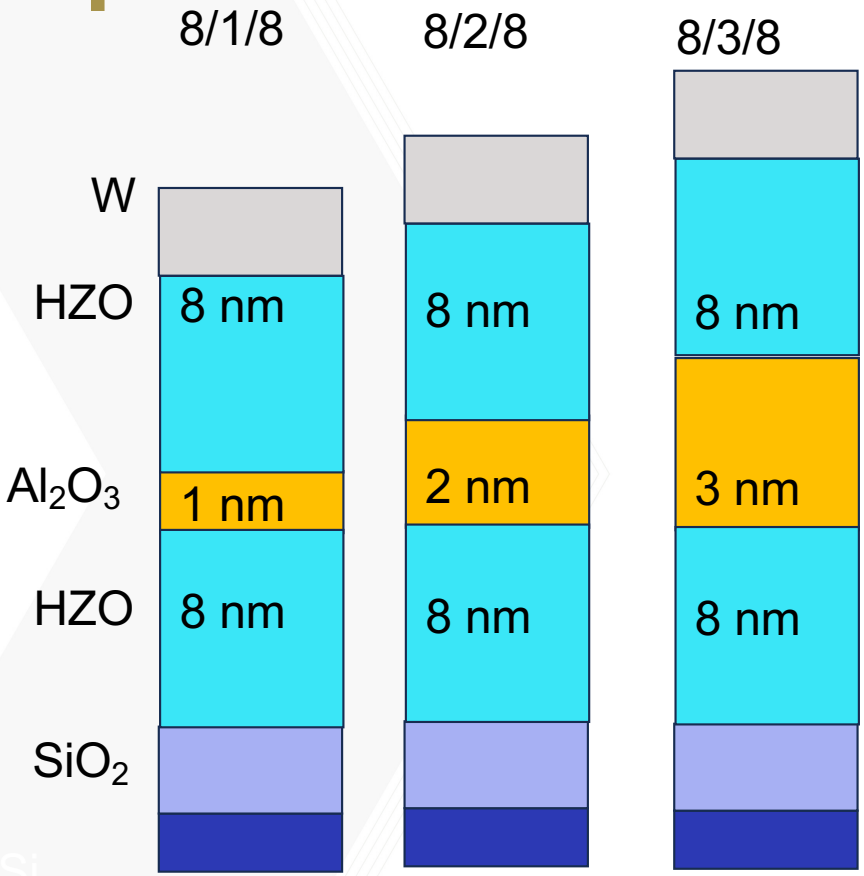




FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

Das et al. IEDM 2023.

Impact of tunnel dielectric insertion



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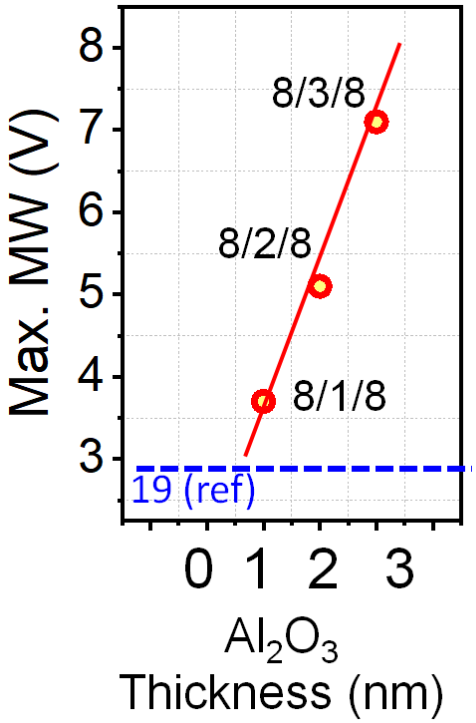
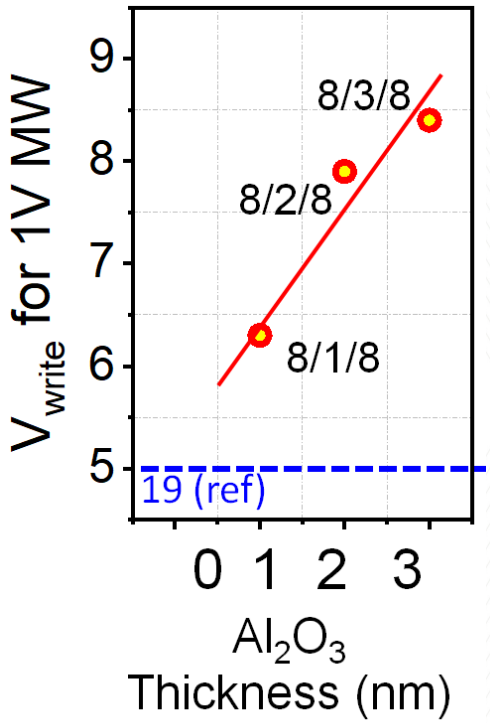
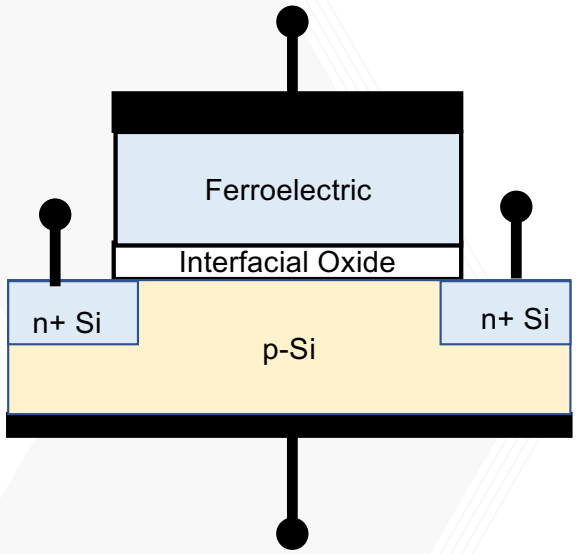
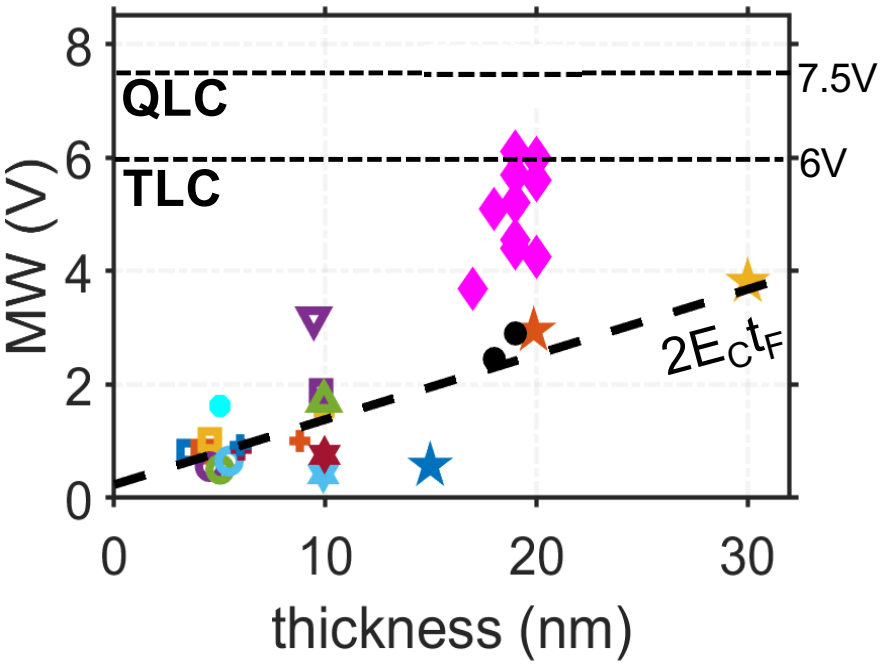




For a fixed FE layer, increase AlO layer increases the MW while increasing the write voltage <15 V.

“Fundamental limit” of memory window





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- Khan group

Fundamental limit of the maximum memory window can be overcome by gate stack design.

Das et al. IEDM 2023.

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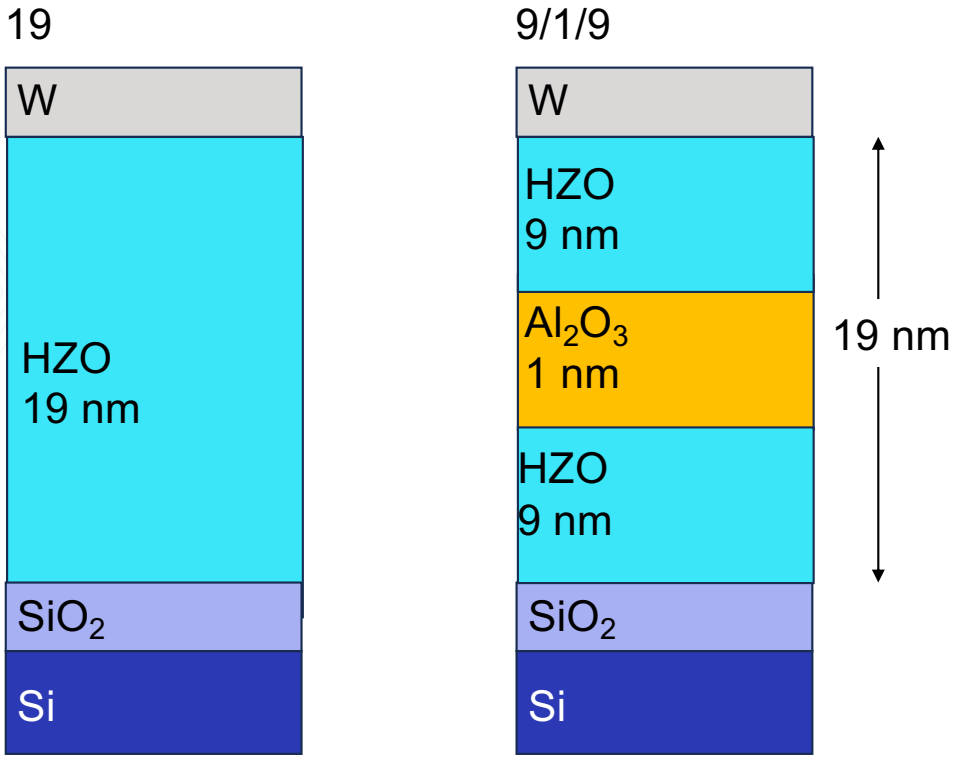
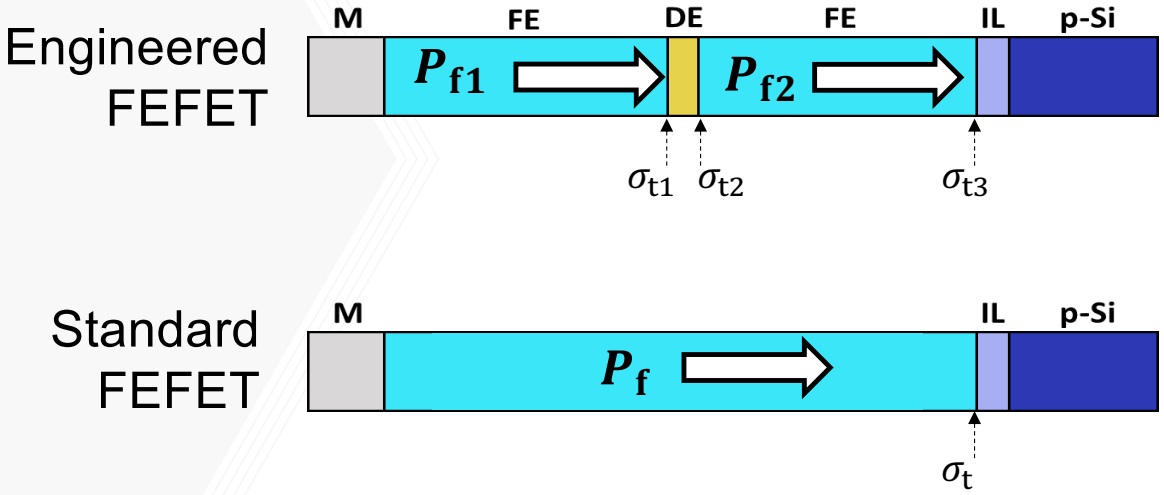
Where is the MW enhancement coming from?



Das et al. Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications. IEDM 2023.

Where is the MW enhancement coming from?



Trapped charges are the key differentiator.

Das et al. Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications. IEDM 2023.

Modeling framework

1. Ferroelectric switching kinetics

Preisach model was adopted to describe the steady-state characteristics of the ferroelectric polarization.

The saturated polarization hysteresis loop is defined as

$$P^{+}_{\mathrm{sat,i}}(E_\mathrm{i}) = P_{\mathrm{s,i}} \tanh[(E_\mathrm{i} - E_{\mathrm{c,i}})/2\delta_\mathrm{i}] \quad \text{If } dE_\mathrm{i}/dt > 0$$

$$P^{-}_{\mathrm{sat,i}}(E_\mathrm{i}) = -P^{+}_{\mathrm{sat,i}}(-E_\mathrm{i}) \quad \text{If } dE_\mathrm{i}/dt < 0$$

where

$$\delta_\mathrm{i} = E_{\mathrm{c,i}} \left[\ln\left(\frac{1 + P_{\mathrm{r,i}}/P_{\mathrm{s,i}}}{1 - P_{\mathrm{r,i}}/P_{\mathrm{s,i}}} \right) \right]^{-1} \quad \text{For } i = 1,2$$

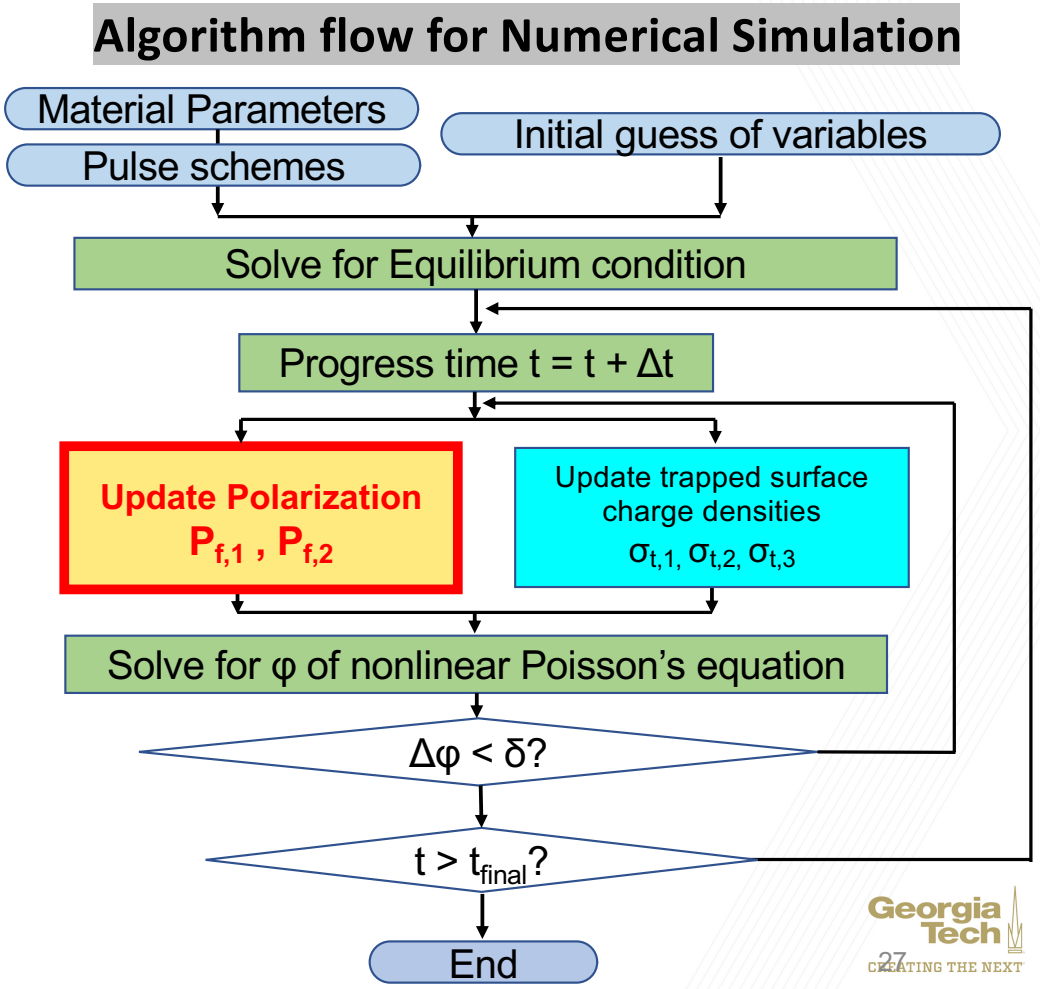
The derivative of the polarization is given by

$$\frac{dP_{\mathrm{f,i}}}{dE_\mathrm{i}} = \Gamma_\mathrm{i} \frac{dP_{\mathrm{sat,i}}}{dE_\mathrm{i}} \quad \text{For } i = 1,2$$

where

$$\Gamma_\mathrm{i} = 1 - \tanh\left[\left(\frac{P_{\mathrm{f,i}} - P_{\mathrm{sat,i}}}{\xi_\mathrm{i} P_{\mathrm{s,i}} - P_{\mathrm{f,i}}} \right)^{1/2} \right]$$

$\xi_\mathrm{i} = +1$ when $dE_\mathrm{i}/dt > 0$ and $\xi = -1$ when $dE_\mathrm{i}/dt < 0$



Modeling framework

2. Rate equations for trapping and de-trapping

Assuming single level traps, define

$N_{t,1}$ / $P_{t,1}$: Acceptor/Donor-like trap density at HZO/Al_2O_3

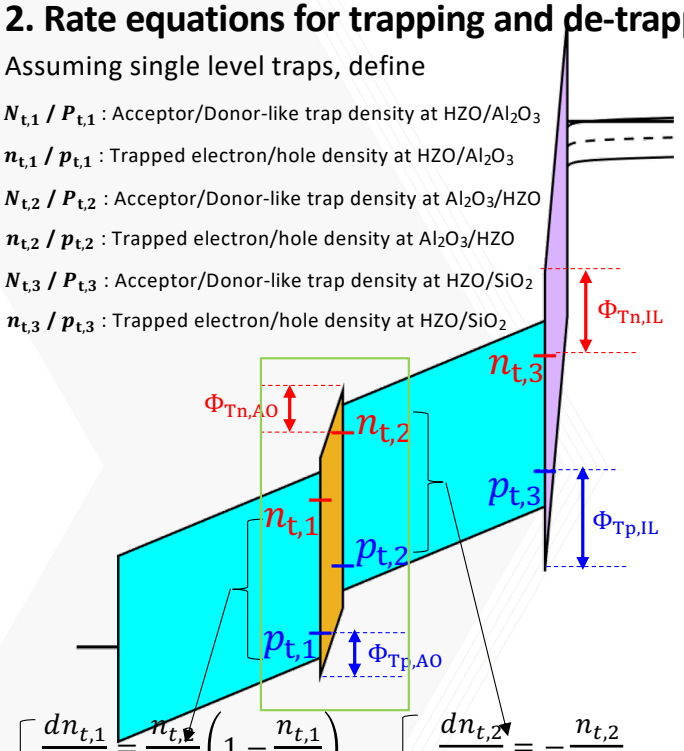
$n_{t,1}$ / $p_{t,1}$: Trapped electron/hole density at HZO/Al_2O_3

$N_{t,2}$ / $P_{t,2}$: Acceptor/Donor-like trap density at Al_2O_3/HZO

$n_{t,2}$ / $p_{t,2}$: Trapped electron/hole density at Al_2O_3/HZO

$N_{t,3}$ / $P_{t,3}$: Acceptor/Donor-like trap density at HZO/SiO_2

$n_{t,3}$ / $p_{t,3}$: Trapped electron/hole density at HZO/SiO_2



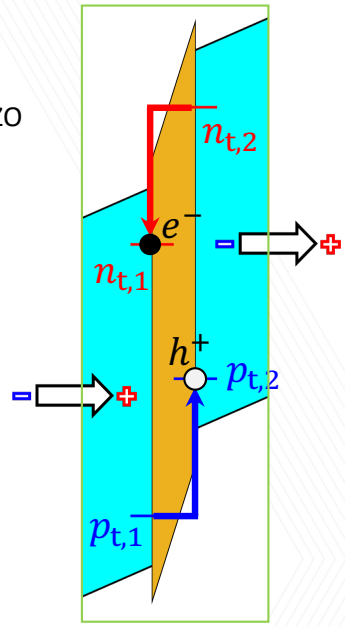
$$\begin{cases} \dfrac{dn_{t,1}}{dt} = \dfrac{n_{t,2}}{\tau_{cn1}}\left(1-\dfrac{n_{t,1}}{N_{t,1}}\right) \\ \dfrac{dp_{t,1}}{dt} = -\dfrac{p_{t,1}}{\tau_{ep1}} \end{cases} \qquad \begin{cases} \dfrac{dn_{t,2}}{dt} = -\dfrac{n_{t,2}}{\tau_{en2}} \\ \dfrac{dp_{t,2}}{dt} = \dfrac{p_{t,1}}{\tau_{cp2}}\left(1-\dfrac{p_{t,2}}{P_{t,2}}\right) \end{cases}$$

The net trapped charges $\sigma_{t,i}$ are

$$\sigma_{t,i} = q(p_{t,i} - n_{t,i}) \qquad \text{For } i = 1,2,3$$

The emission mechanism of the trapped charges at Al_2O_3/HZO (HZO/Al_2O_3) interfaces are assumed to be Fowler-Nordheim (FN) tunneling → **Al_2O_3 as "Tunnel Dielectric Layer"**

$$\tau_{en(p),i=2(1)} = \tau_{cn(p),i=1(2)} = \tau_0 \exp\left(-\frac{4\sqrt{2m_{AO}\Phi^3_{Tn(p),AO}}}{3q\hbar E_{AO}}\right)$$



3. Nonlinear Poisson-Boltzmann equation

For gate oxides, $\dfrac{\partial D}{\partial x} = 0$

With boundary conditions of the displacement field $\boldsymbol{D}$ continuity at the interfaces i with given $\boldsymbol{P_{f,i}}$ and $\boldsymbol{\sigma_{t,i}}$

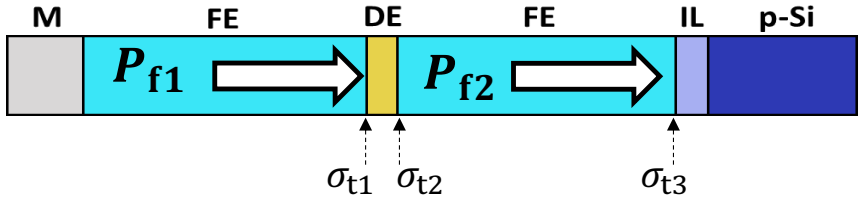
For semiconductors,

$$\frac{\partial^2 \varphi}{\partial x^2} = -\frac{q}{\epsilon_s}\left[p_{po}(\exp(-\beta\varphi)-1) - n_{po}(\exp(\beta\varphi)-1)\right]$$

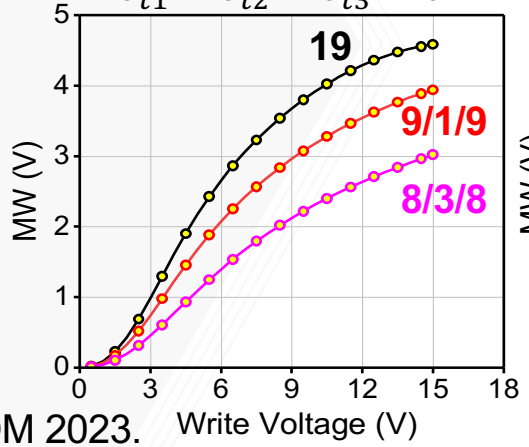
Thus, Flat band voltage is given by

$$V_{FB} = \phi_{MS} - \frac{\sigma_{it}(\psi_s)}{C_{tot}} - \frac{P_{f,1}+\sigma_{t,1}+\sigma_{t,2}+\sigma_{t,3}}{C_{f,1}} - \frac{\sigma_{t,2}+\sigma_{t,3}}{C_d} - \frac{P_{f,2}+\sigma_{t,3}}{C_{f,2}}$$

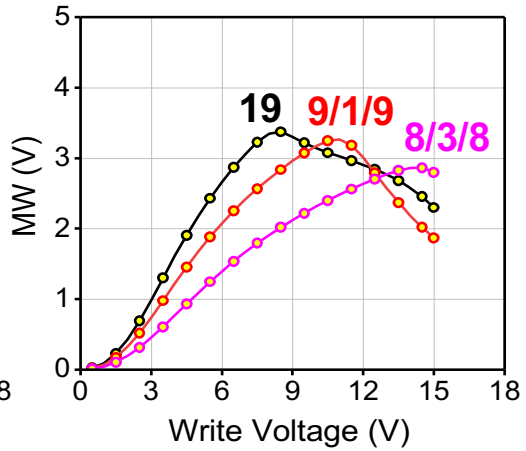
Decoupling the impacts of different trapping mechanisms



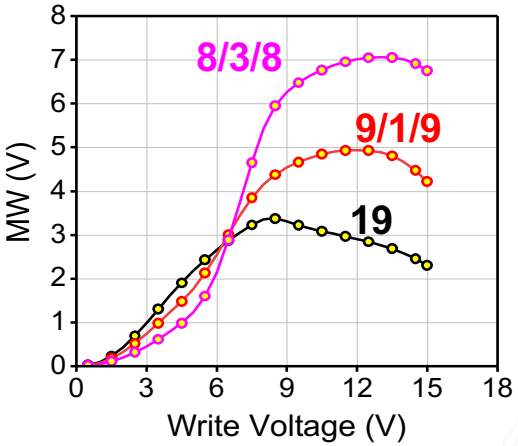
Absence of screening trap charges
$\sigma_{t1} = \sigma_{t2} = \sigma_{t3} = 0$



HZO/SiO_2 Traps only
$\sigma_{t1} = \sigma_{t2} = 0;\ \sigma_{t3} \neq 0$



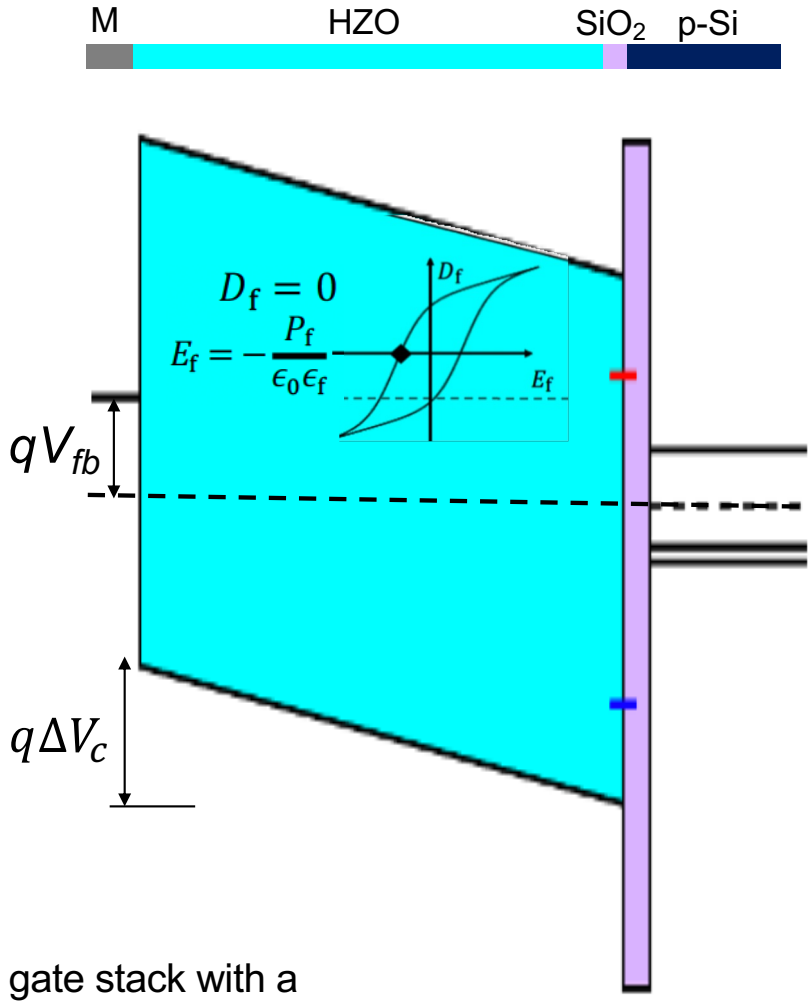
Al_2O_3/HZO + HZO/SiO_2 Traps
$\sigma_{t1} \neq 0;\ \sigma_{t2} \neq 0;\ \sigma_{t3} \neq 0$



Das et al. IEDM 2023.

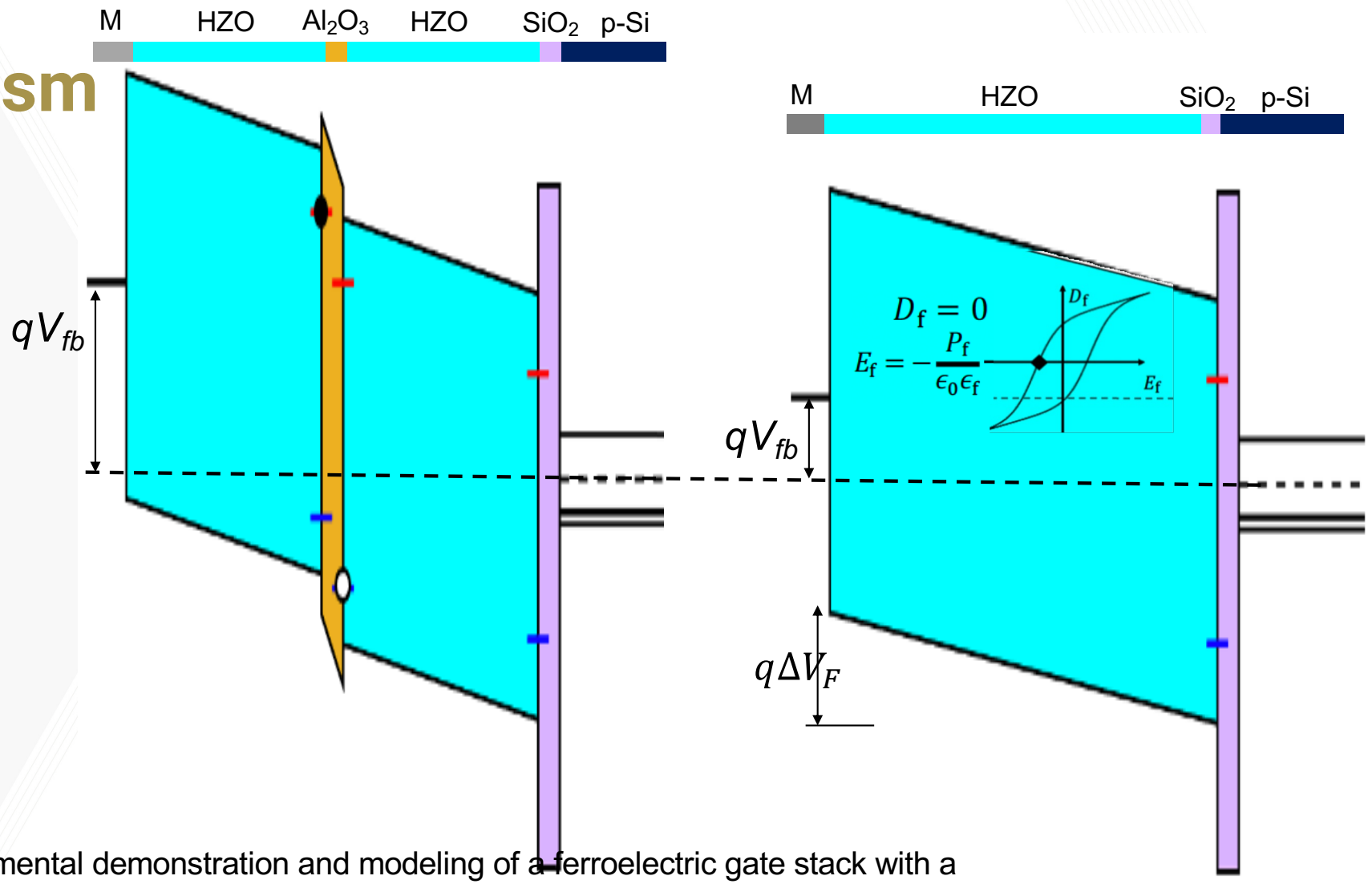
Trap effects are responsible for the observed MW trend
(MW: 8/3/8 >9/1/9>19)

MW enhancement mechanism with band diagrams



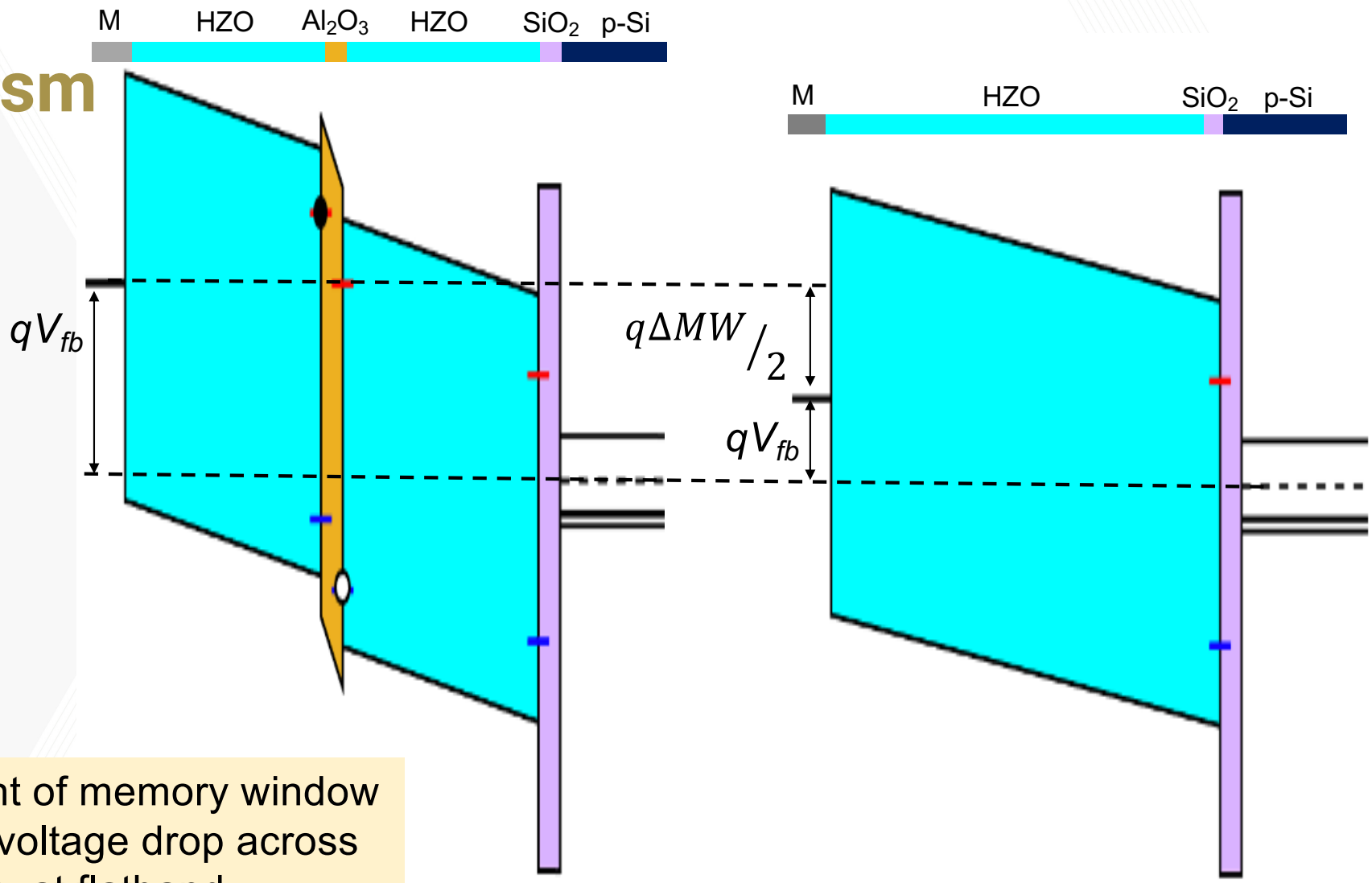
Das et al. Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications. IEDM 2023.

MW mechanism



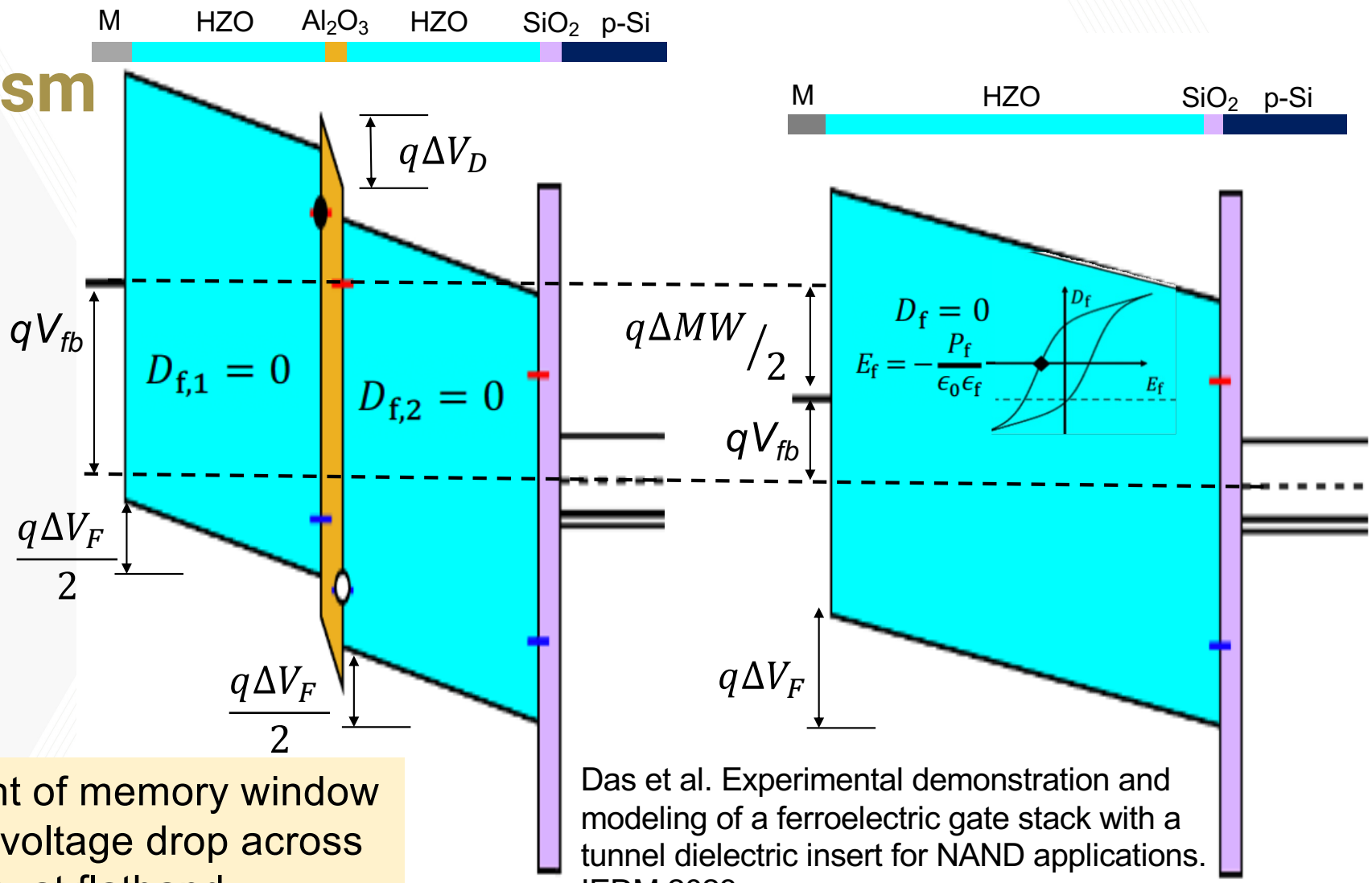
Das et al. Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications. IEDM 2023.

MW mechanism



Enhancement of memory window ΔMW ≈2 x voltage drop across Al_2O_3 at flatband

MW mechanism

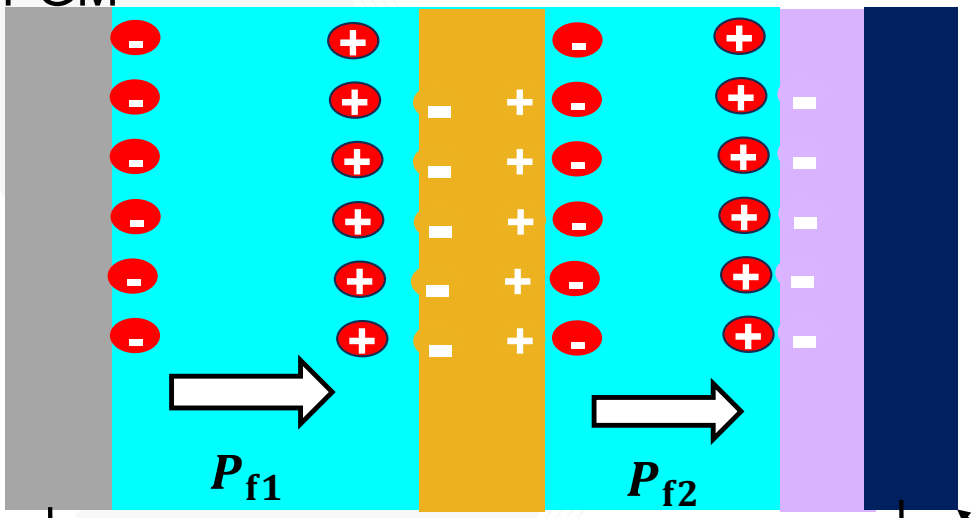


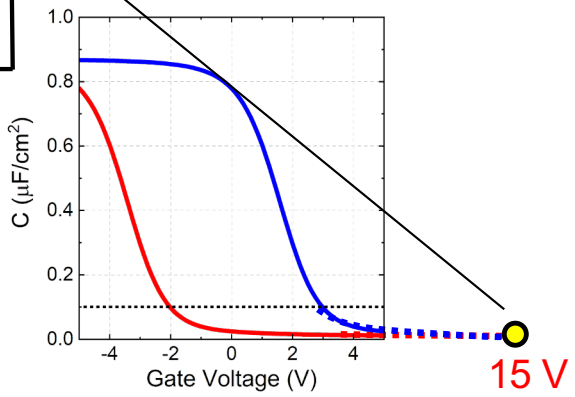
Enhancement of memory window $\Delta MW \approx 2$ x voltage drop across Al_2O_3 at flatband

Das et al. Experimental demonstration and modeling of a ferroelectric gate stack with a tunnel dielectric insert for NAND applications. IEDM 2023.

Where does the built-in E-field come from?

PGM





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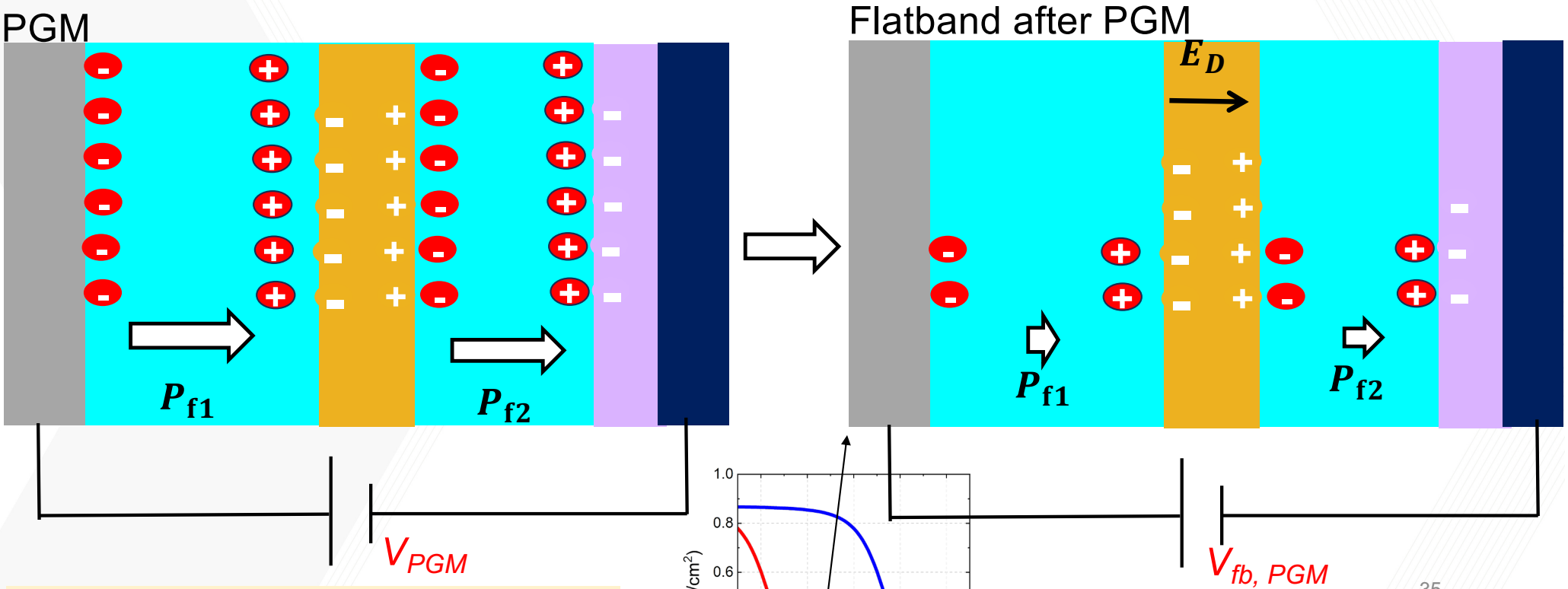
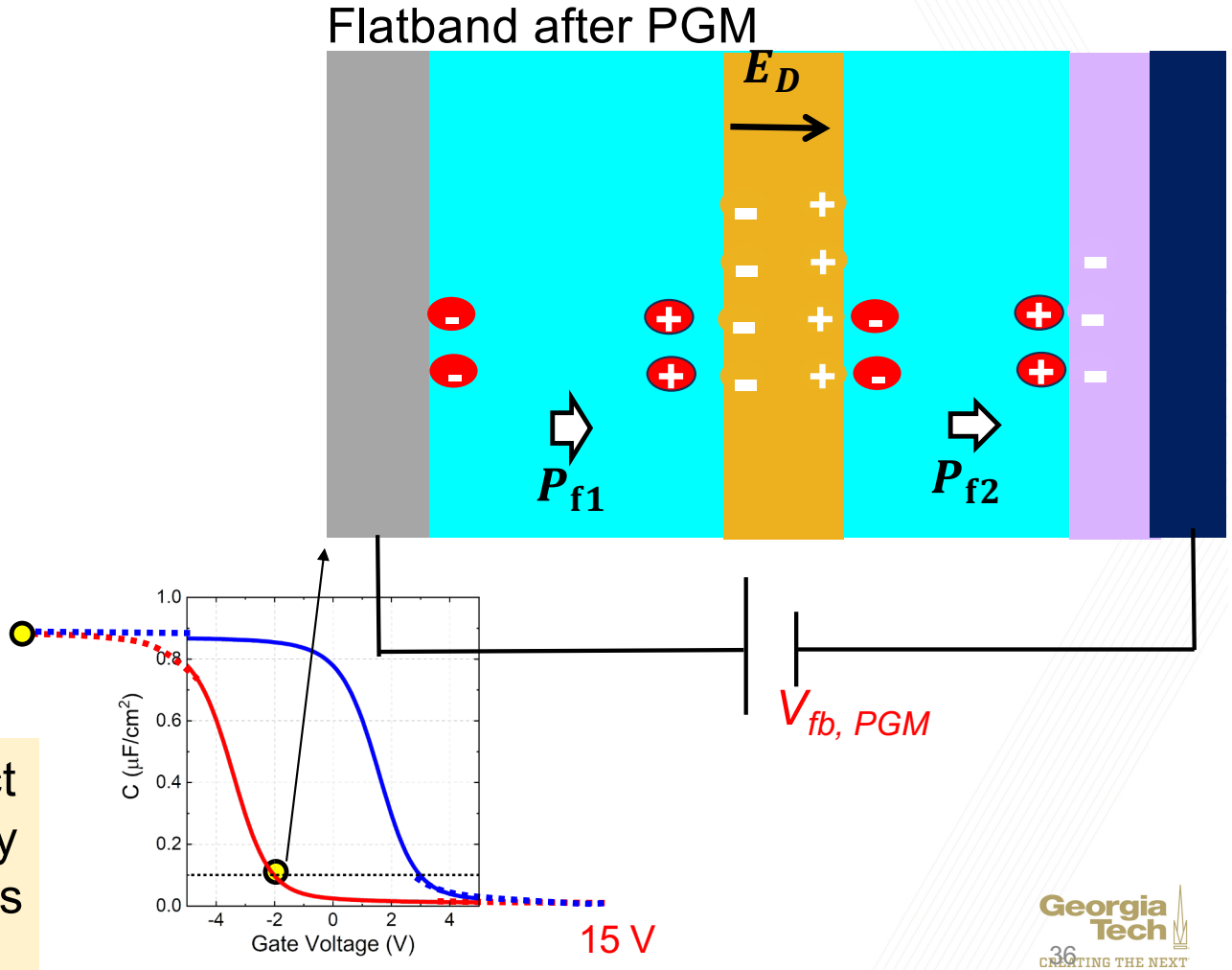


Built-in electric field due to defect dipole in the dielectric induced by the ferroelectric polarization leads to the MW enhancement.

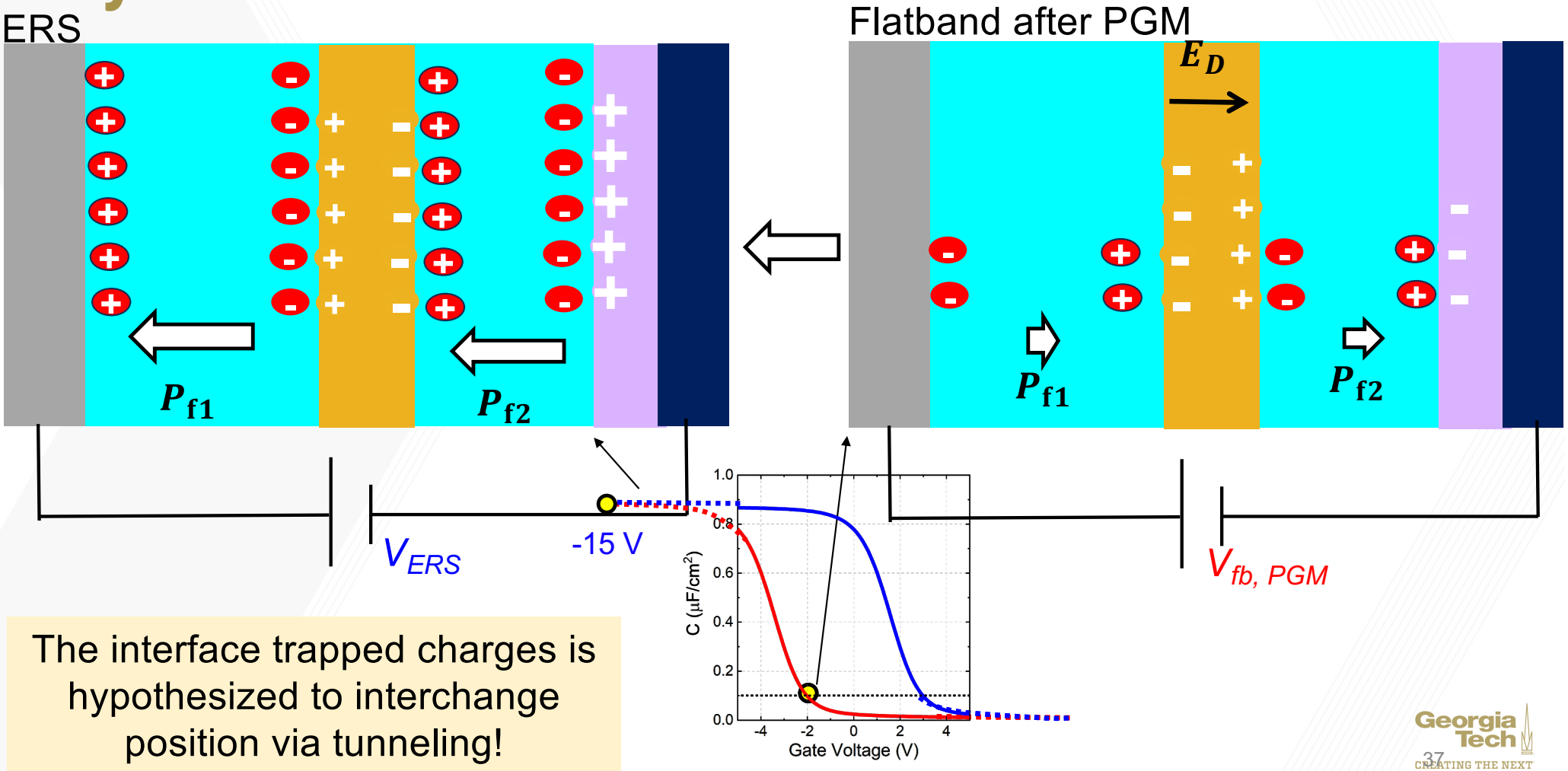
35

Where does the built-in E-field come from?



Built-in electric field due to defect dipole in the dielectric induced by the ferroelectric polarization leads to the MW enhancement.

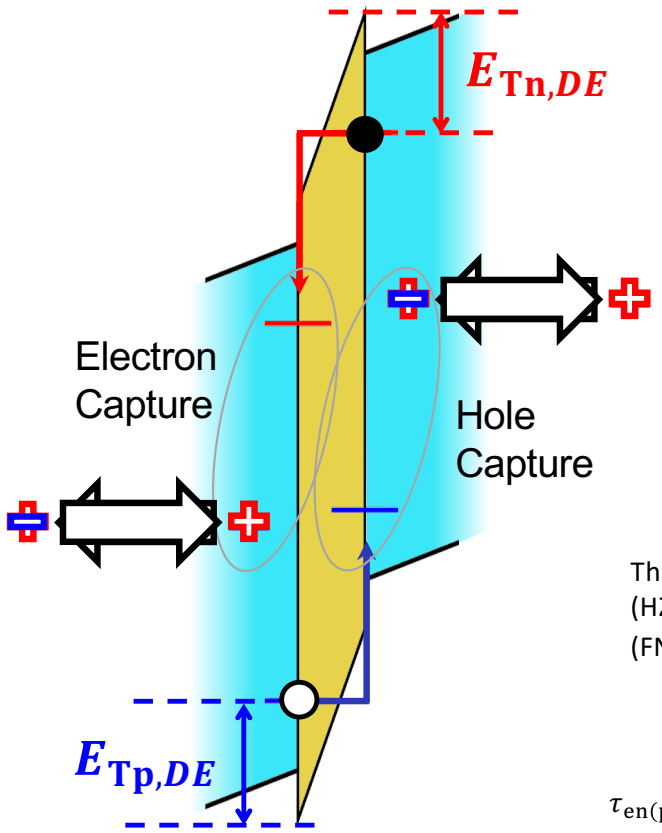
Why the build-in E-field direction switches?



The interface trapped charges is hypothesized to interchange position via tunneling!

Is it a tunnel dielectric?

chanism

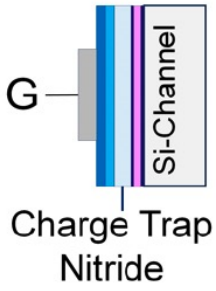
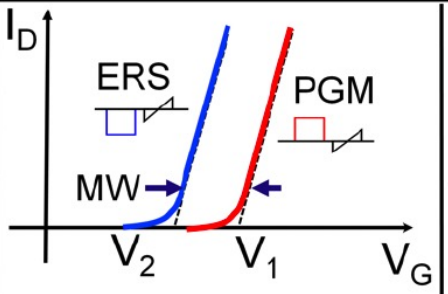
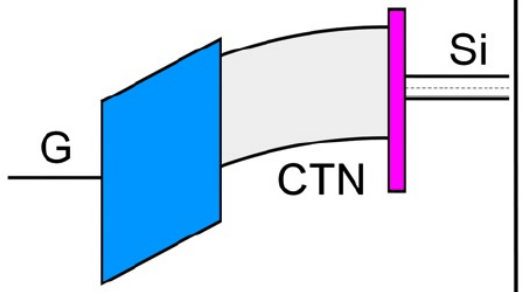
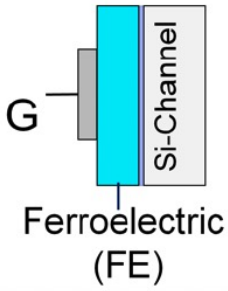
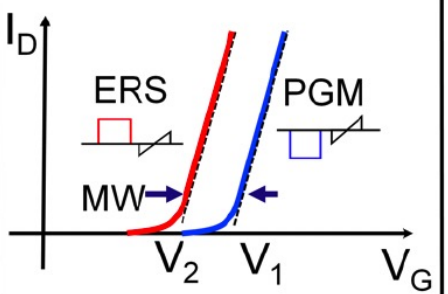
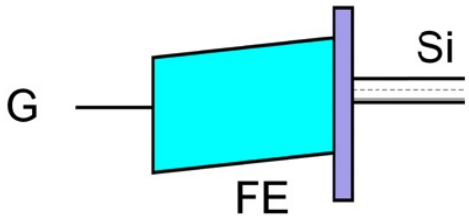
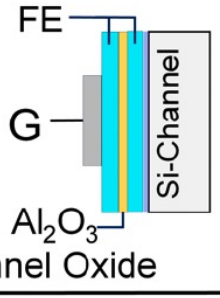
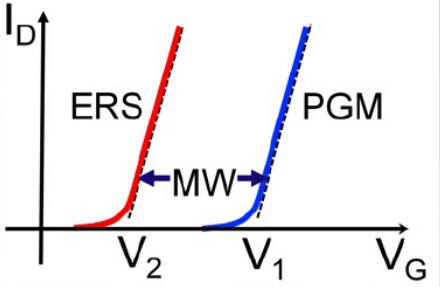
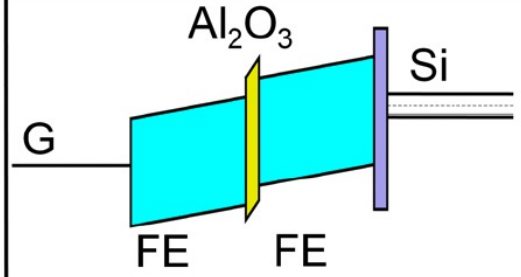


The emission mechanism of the trapped charges at Al_2O_3/HZO (HZO/Al_2O_3) interfaces are assumed to be Fowler-Nordheim (FN) tunneling → **Al_2O_3 as "Tunnel Dielectric Layer"**

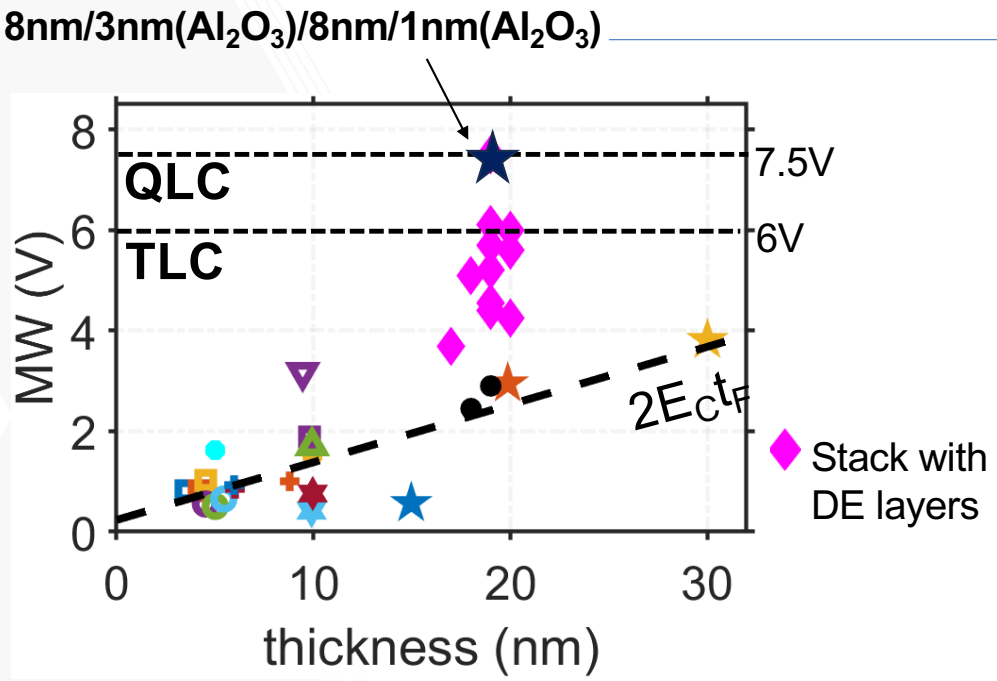
$$\tau_{\mathrm{en(p)},i=2(1)} = \tau_{\mathrm{cn(p)},i=1(2)} = \tau_0 \exp\left(-\frac{4\sqrt{2m_{AO}\Phi^3_{\mathrm{Tn(p)},AO}}}{3q\hbar E_{AO}}\right)$$

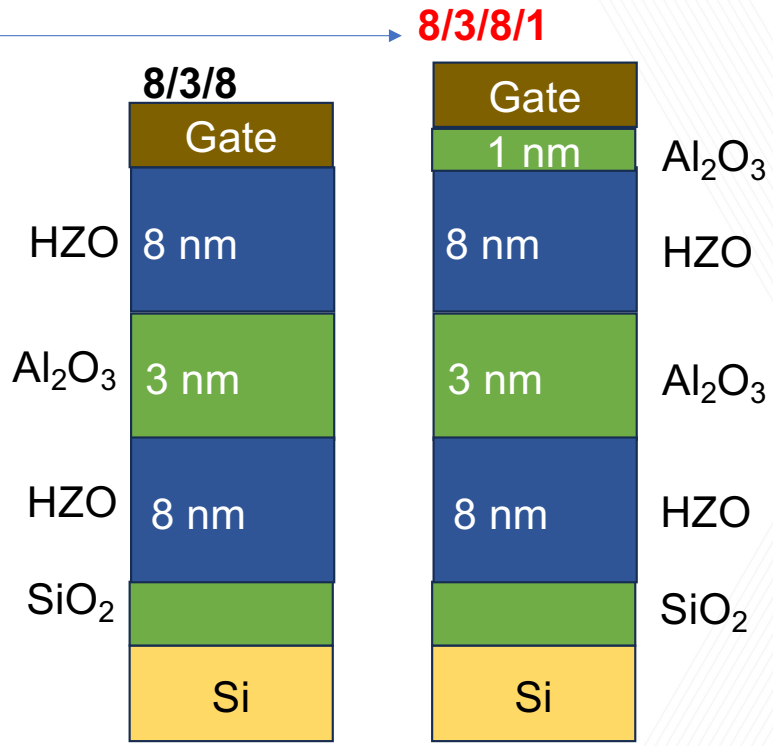
Hypothesis: The interface trapped charges interchange position via tunneling!

Conclusions

	Structure	Characteristics	Band diagram at FB condition	Attributes
Charge Trap Flash				✓ Large MW × Large Write Voltage Mechanism: Trapping
Conventional FEFET				× Low MW ✓ Low Write Voltage Mechanism: Polarization Switching
Proposed FEFET				✓ Large MW ✓ Moderate Write Voltage Mechanism: Polarization Switching + Trapping + Tunneling

Engineered FEFETs for enhanced MW





A ferroelectric-dielectric gate stack offers several tuning knobs to engineer the MW properties

Das, D., Fernandes, L., Ravindran, P. V., Song, T., Park, C., Afroze, N., ... & Khan, A. (2024, May). Design Framework for Ferroelectric Gate Stack Engineering of Vertical NAND Structures for Efficient TLC and QLC Operation. In *2024 IEEE International Memory Workshop (IMW)* (pp. 1-4). IEEE.

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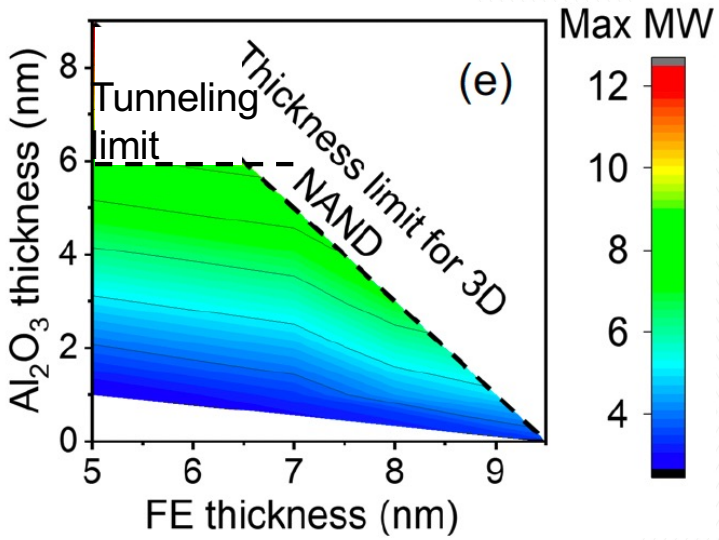
Conclusions

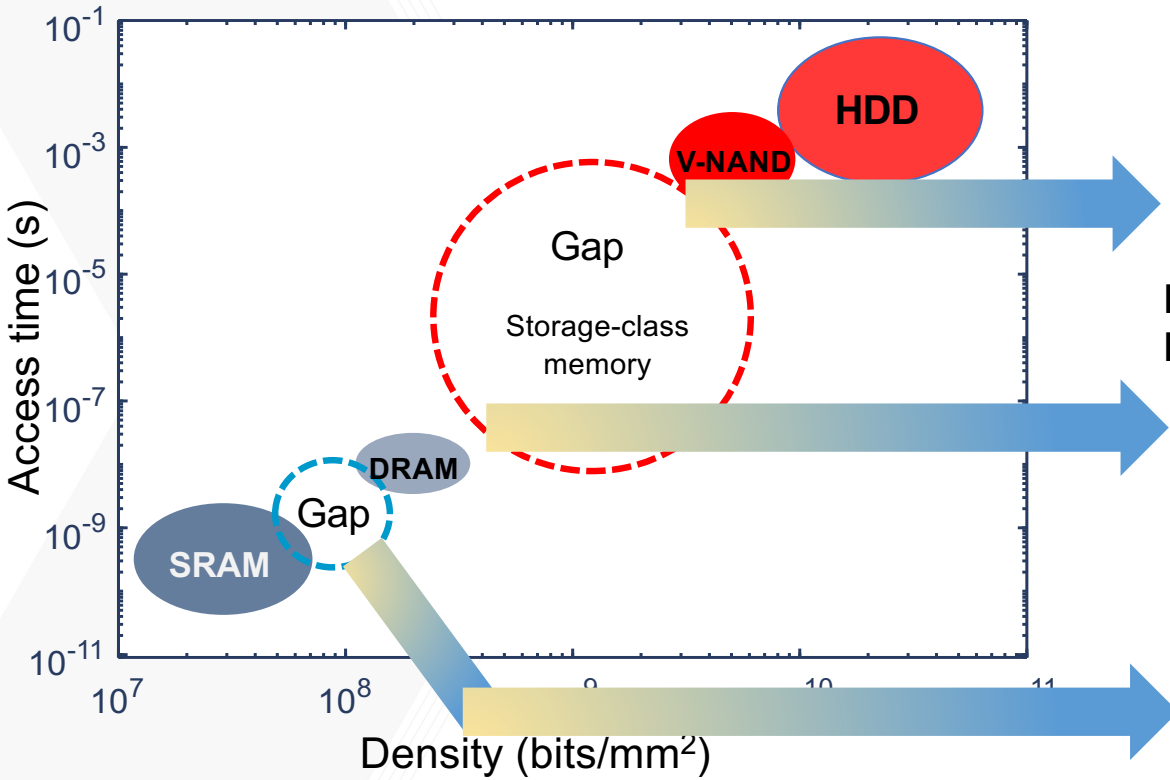
- Ferroelectricity presents opportunities for NAND storage technologies.
  - Write voltage reduction and memory window enhancement.
  - Potential for QLC by stack engineering.
  - Vertical scaling towards 1000 layers.



- Further exploration and engineering required for
  - Tunneling mechanism
  - Disturb characteristics and mitigation.

- Alternative structures can also lead to MW enhancement via gate side injection through blocking layer.
  - See: Lim et al. Comprehensive Design Guidelines of Gate Stack for QLC and Highly Reliable Ferroelectric VNAND. IEDM 2023 paper 35.4.

Ferroelectrics for memory and storage



Ferroelectrics for flash

- Voltage scaling below 15 V
- Z-scaling

Ferroelectrics for the DRAM/Storage class space

Ramaswamy et al. Micron, IEDM 2024

- Dual Layer 3-D stacked FRAM
- Capacity – 32 Gb (Sk Hynix DRAM –-8 Gb)
- Latency – 180 ns (LPDDR5 – 60 ns)
- Density – 450 Mb/mm^2

Ferroelectrics for embedded memories/cache

- Density
- BEOL compatibility
- Fast

Our team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Chinsung Park

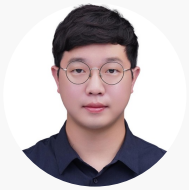

Priyankka Ravikumar


Jiayi Chen


Prasanna Ravindran


Zekai Wang


Lance Fernandes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