

Ferroelectric memories

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3/1/2024





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Our team



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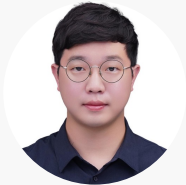
Priyanka
G R



Zekai
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Kuo



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Eknath
Sarkar



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Das (NIT Silchar)



Dr. Zheng
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Dr. Sarah
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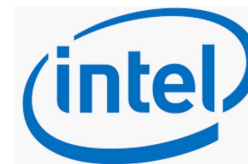


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TECHNOLOGY | ARTIFICIAL INTELLIGENCE

Sam Altman Seeks Trillions of Dollars to Reshape Business of Chips and AI

OpenAI chief pursues investors including the U.A.E. for a project possibly requiring up to \$7 trillion

Forbes

Artificial General Intelligence (AGI) And The Coming Wave

Randy Bean Contributor 

Randy Bean is a noted Author, Speaker, Founder, CEO, & Senior Advisor.

Follow



ChatGPT



Examples

"Explain quantum computing in simple terms"

"Got any creative ideas for a 10 year old's birthday?"

"How do I make an HTTP request in Javascript?"



Capabilities

Remembers what user said earlier in the conversation

Allows user to provide follow-up corrections

Trained to decline inappropriate requests



Limitations

May occasionally generate incorrect information

May occasionally produce harmful instructions or biased content

Limited knowledge of world and events after 2021



Try SemiconductorGPT at

<https://chat.openai.com/g/g-Wz4h6XhrV-semiconductorgpt>



GT ECE 3030 Course Assistant

ChatGPT ▾

You

Consider an n-type MOSFET with $N_A = 7 \times 10^{18} \text{ m}^{-3}$. The gate length of the MOSFET $L = 2 \text{ } \mu\text{m}$, width $W = 12 \text{ } \mu\text{m}$ and the oxide thickness $t_{ox} = 8 \text{ nm}$.

Take $N_C = N_V = 1 \times 10^{25} \text{ m}^{-3}$, $E_G = 1.12 \text{ eV}$, $n_i = 1.5 \times 10^{16} \text{ m}^{-3}$, $kT = 0.026 \text{ eV}$.

Calculate the numerical values of following quantities.

- (1) $\phi_B = |E_F - E_{il}|$,
- (2) the oxide capacitance C_{ox} ,
- (3) the maximum depletion width W_{max} , and
- (4) the threshold voltage V_t .

ChatGPT

To calculate the quantities ●

Message ChatGPT...



Creating video from text

Sora is an AI model that can create realistic and imaginative scenes from text instructions.

All videos on this page were generated directly by Sora without modification.

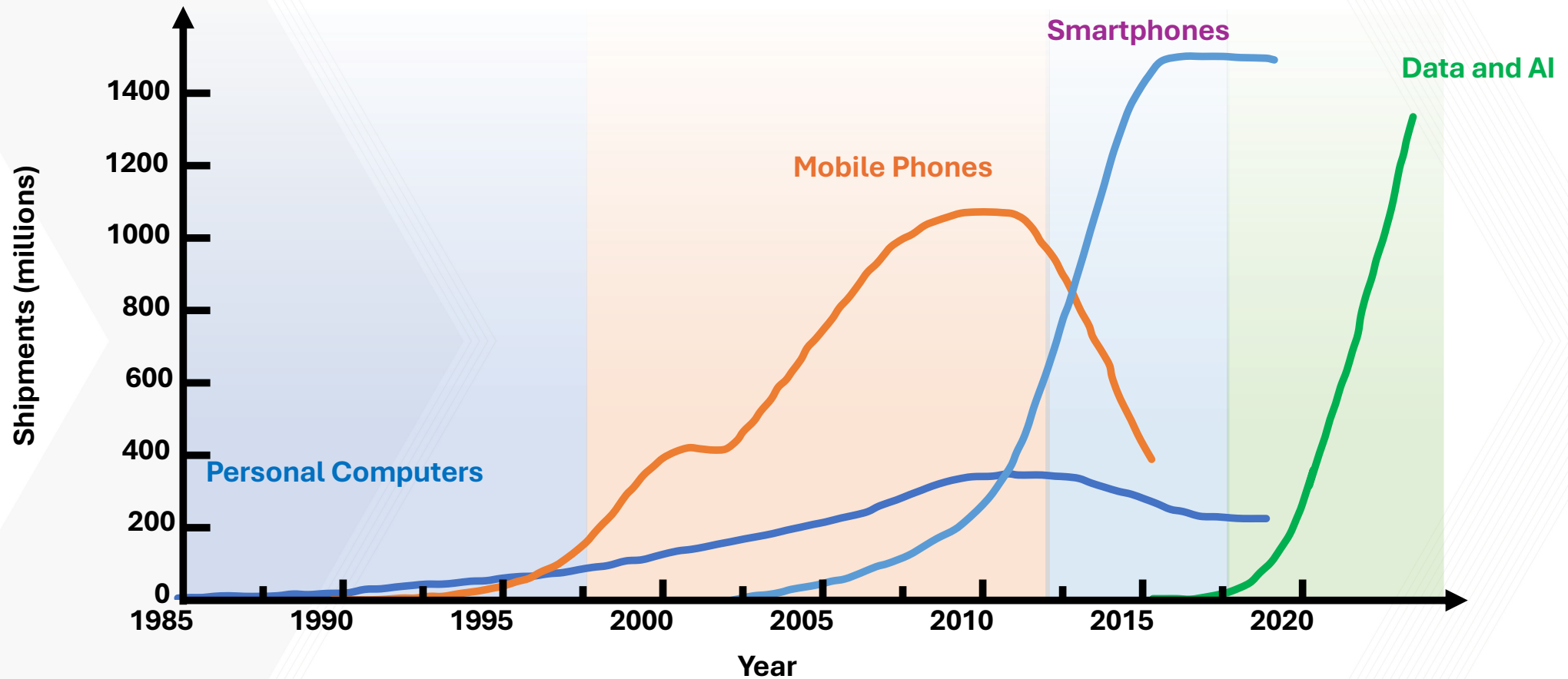
[Capabilities](#)

[Safety](#)

[Research](#)

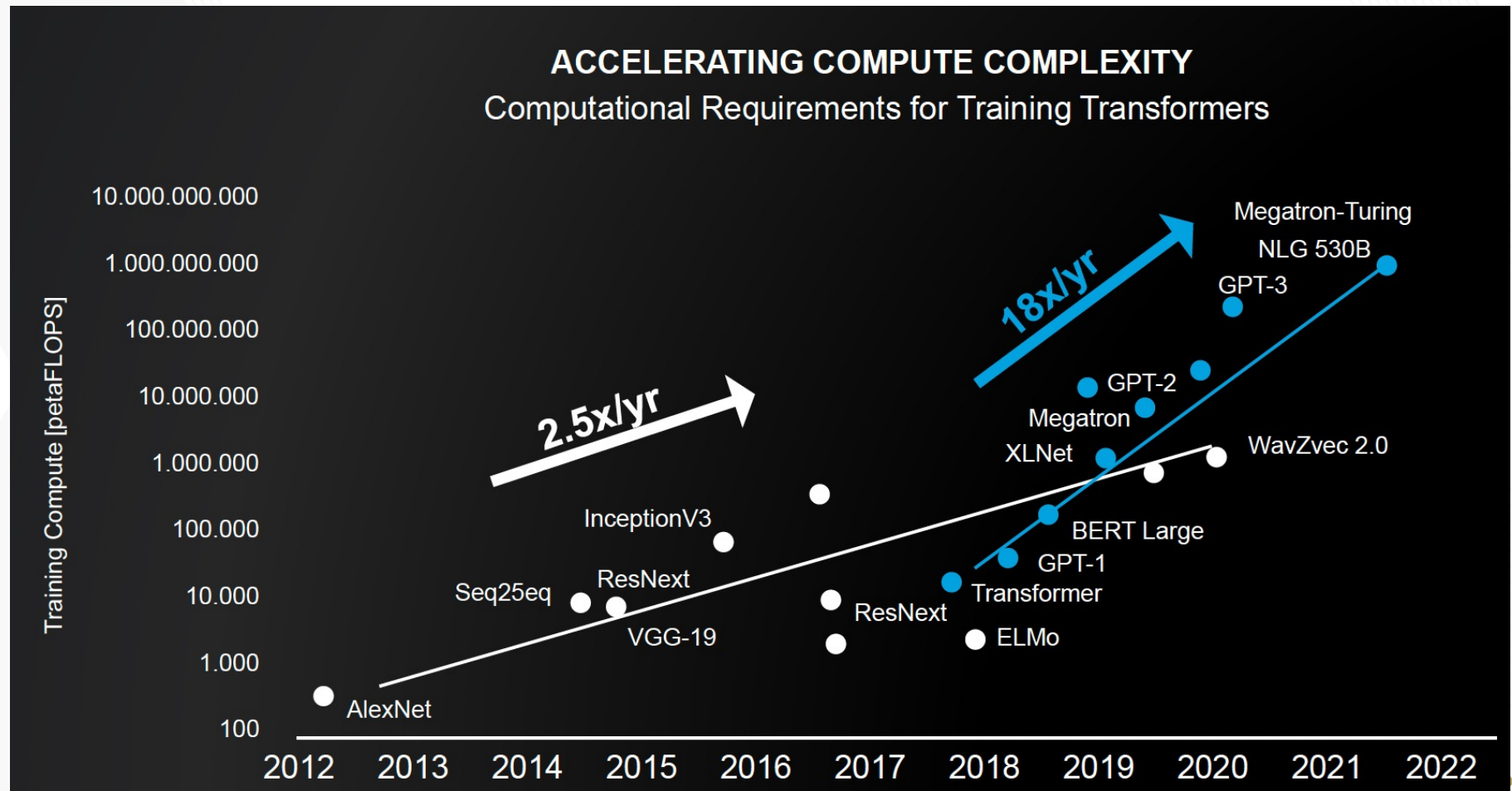


How the computing paradigms have evolved



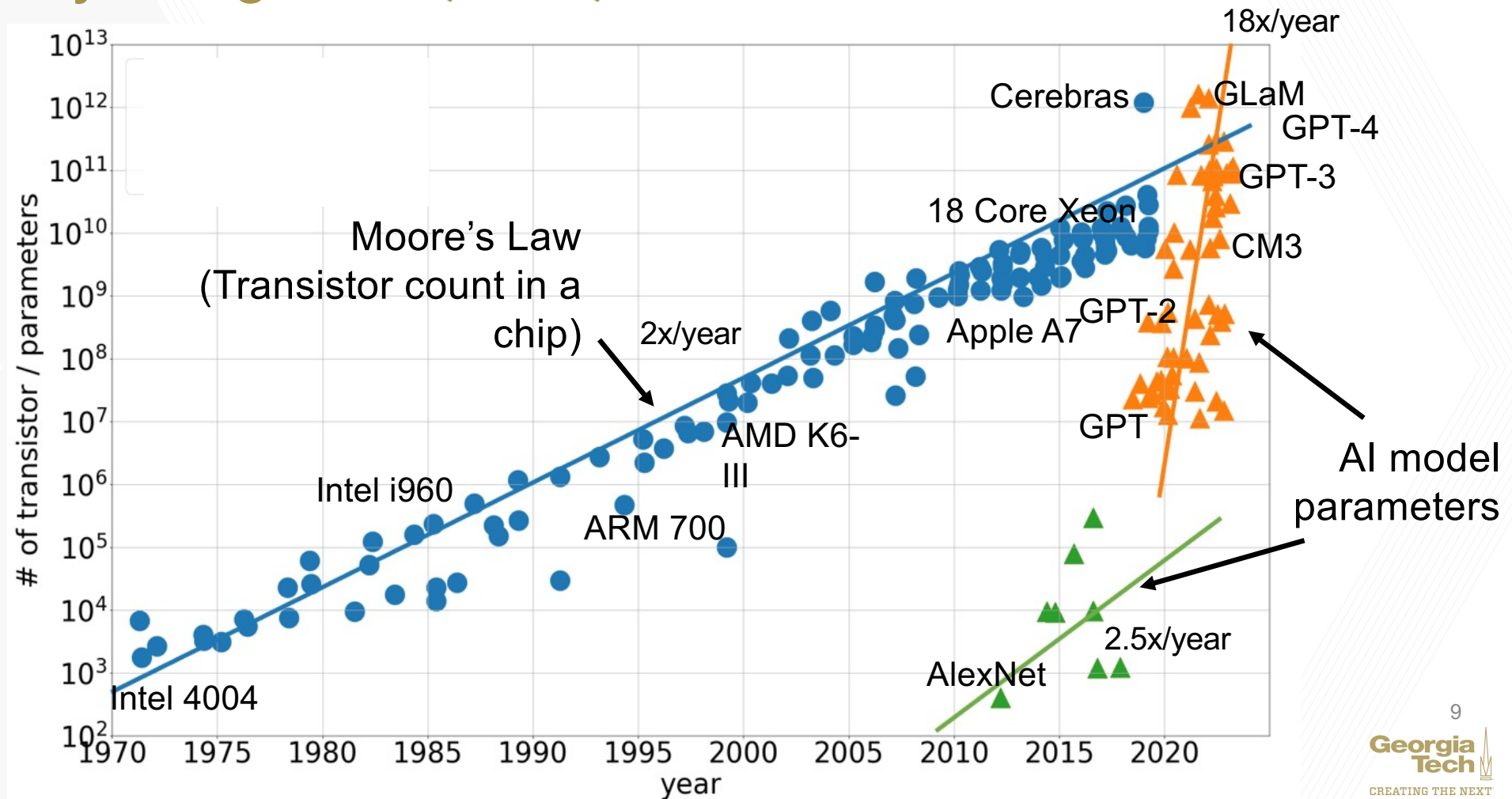
<https://www.economist.com/briefing/2015/02/26/the-truly-personal-computer>
<https://www.statista.com/chart/12798/global-smartphone-shipments/>

Evolution of AI

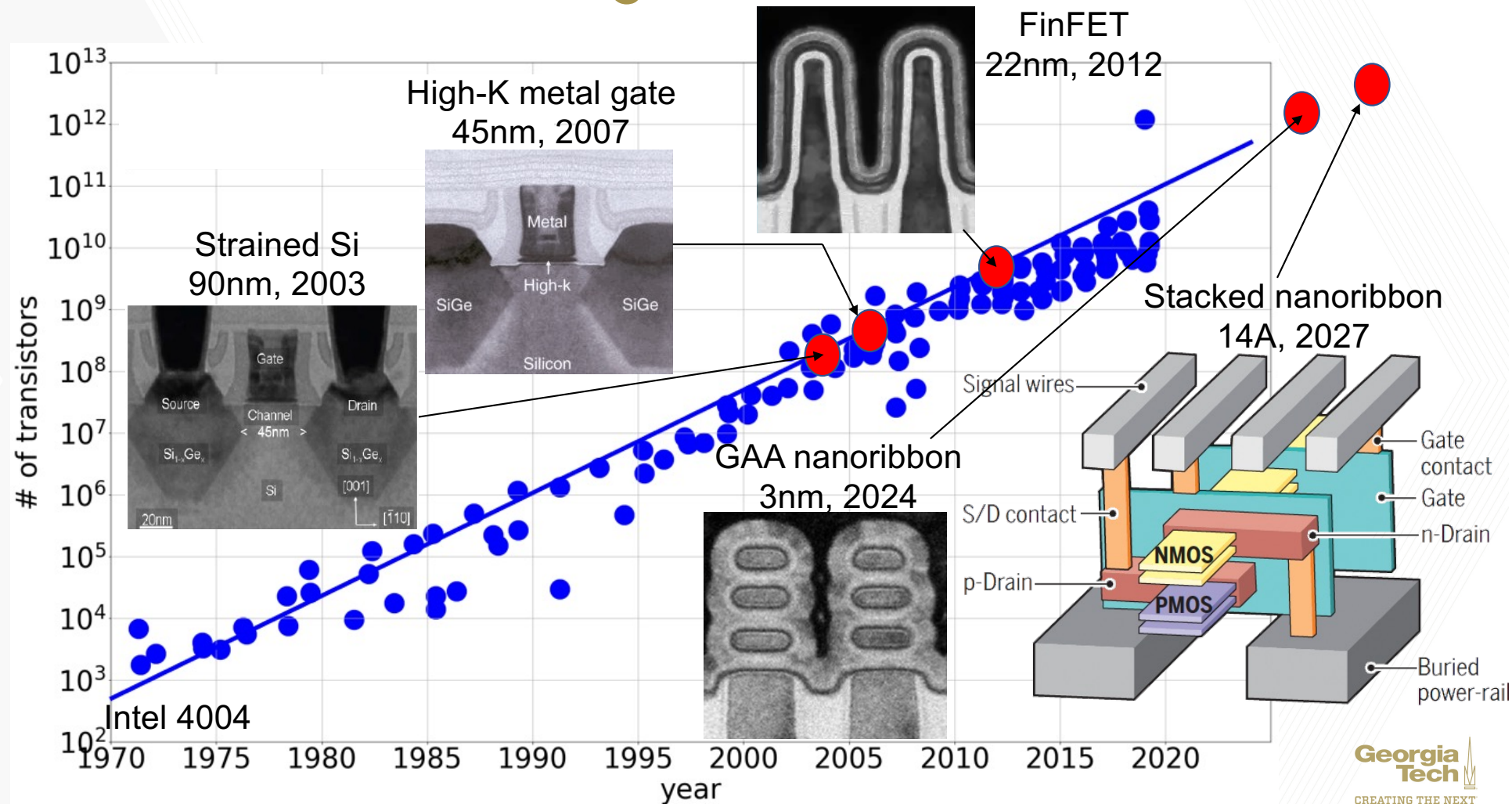


Source: NVIDIA

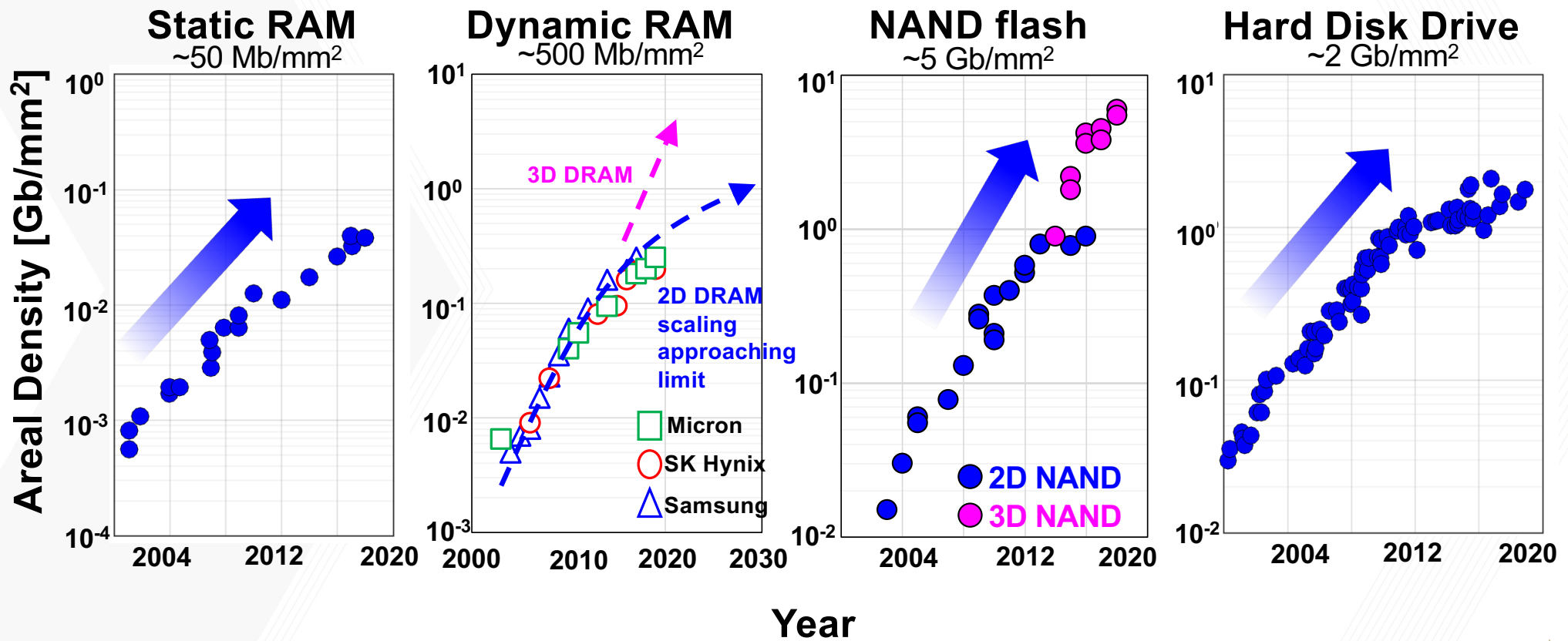
A story of algorithm, data, and silicon



Innovation at the core – Logic transistor

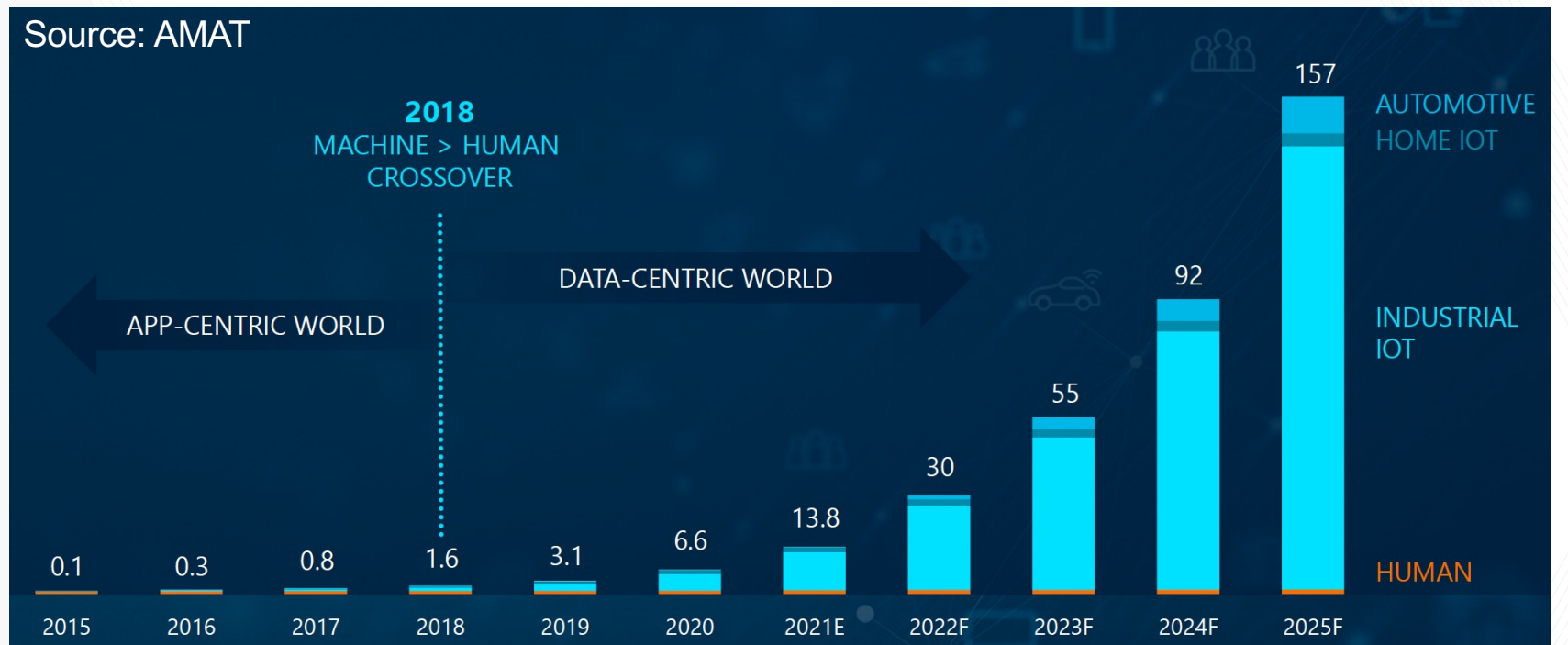


Innovation at the core – Memory



Inflection and Data centric world

Source: AMAT



Human generated data
An individual created an average of
120 MB of data per hour in 2020.



Machine generated data
A connected car create up to
25 GB of data per hour.

Sustainability of computation

1.3 GWh of energy
552 metric ton of CO₂ emission
413 accelerator years
Required for training GPT-3



An American household consumes
11 MWh per year.



To train a large AI model like GPT-3 requires the same amount of energy consumption as an American household would consume in 120 years.

<https://www.bloomberg.com/news/articles/2023-03-09/how-much-energy-do-ai-and-chatgpt-use-no-one-knows-for-sure>
Patterson, David, et al. "Carbon emissions and large neural network training." *arXiv preprint arXiv:2104.10350* (2021).

Sustainability of computation



0.0003 kWh per search¹

8.5B searches per day²

912 GWh per year

Enough for 90,000 US household



ChatGPT

0.001 – 0.01 kWh per query

15 TWh per year for 8B search per day

Enough for 1.5M US household

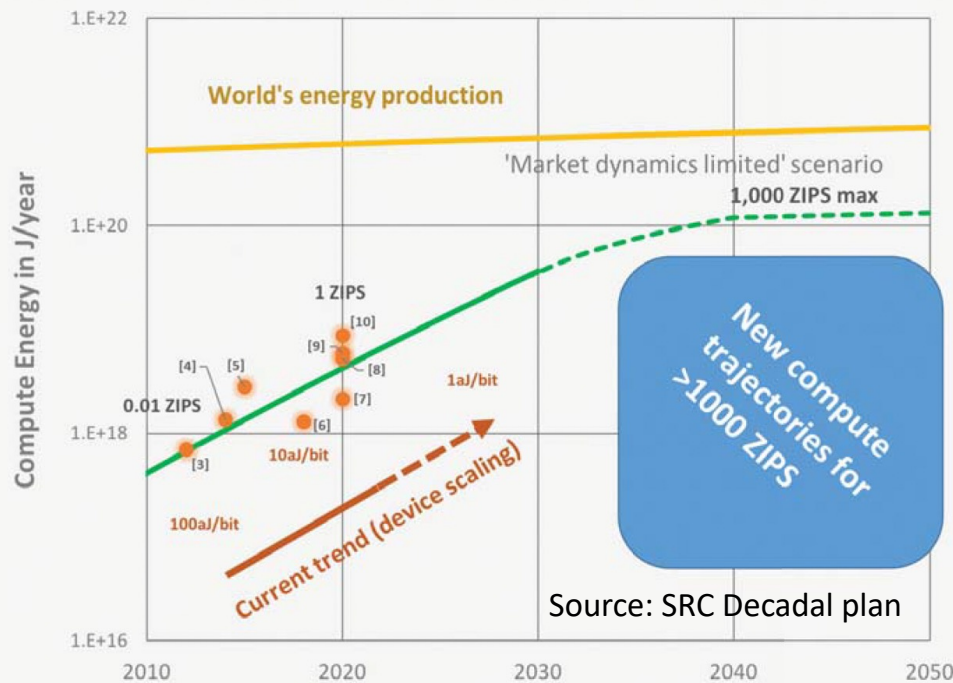
The energy required to perform a search using a large language model (LLM) like we do with Google Search would be ten times higher!

¹[AI and its carbon footprint: How much water does ChatGPT consume? | Mint Lounge \(livemint.com\)](#)

²[How Many People Use Google? Statistics & Facts \(2024\) \(seo.ai\)](#)

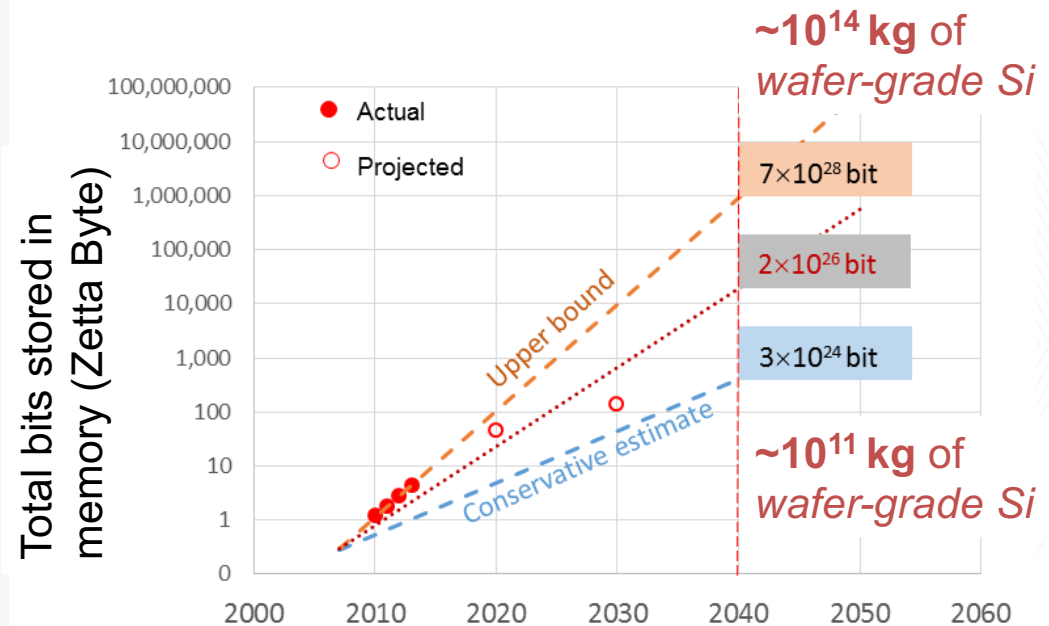
Sustainability of computation

Projected energy cost of computation



Compute energy rises exponentially, while global energy production grows linearly.

Projected Si supply

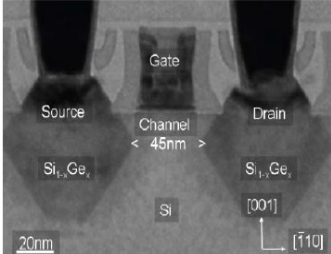


Projected annual global supply of Silicon wafers: $10^7 - 10^8 \text{ kg}$ in 2040.

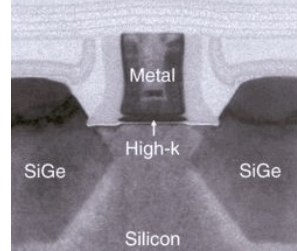
Materials are central to *Future Electronics*

Logic
Technology

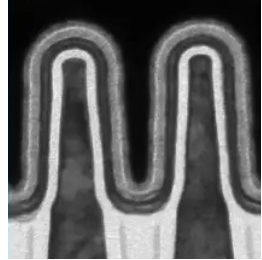
Strained Si
90nm - 2003



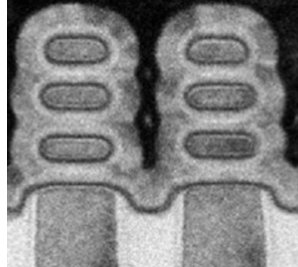
High-K metal gate
45nm - 2007



FinFET
22nm - 2012

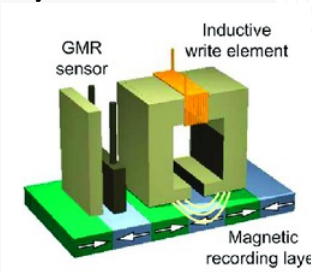


Ribbon FET
20A - 2024

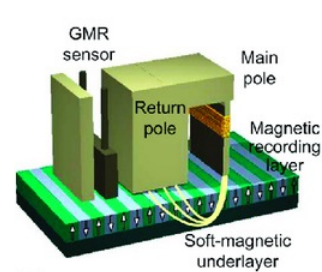


HDD
Technology

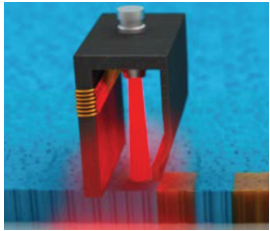
Giant Magnetoresistance (GMR) Heads - 1990s



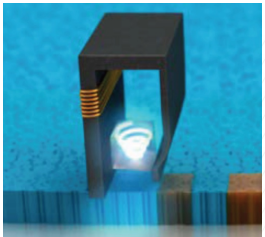
Perpendicular Magnetic Recording (PMR) - 2005



Heat-Assisted Magnetic Recording (HAMR) - 2010s

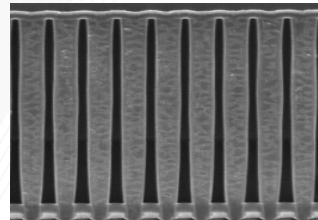


Microwave-Assisted Magnetic Recording (MAMR) - 2010s

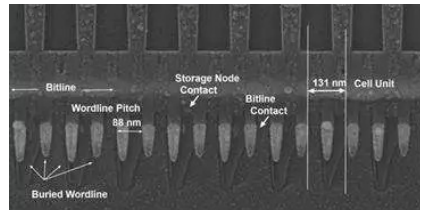


DRAM
Technology

Stacked capacitor - 2003



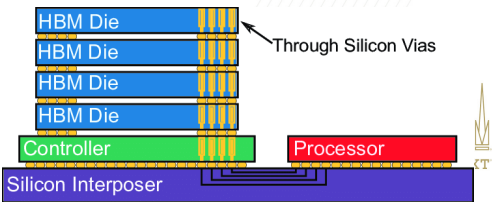
Buried Word-line Saddle Fin - 2009s



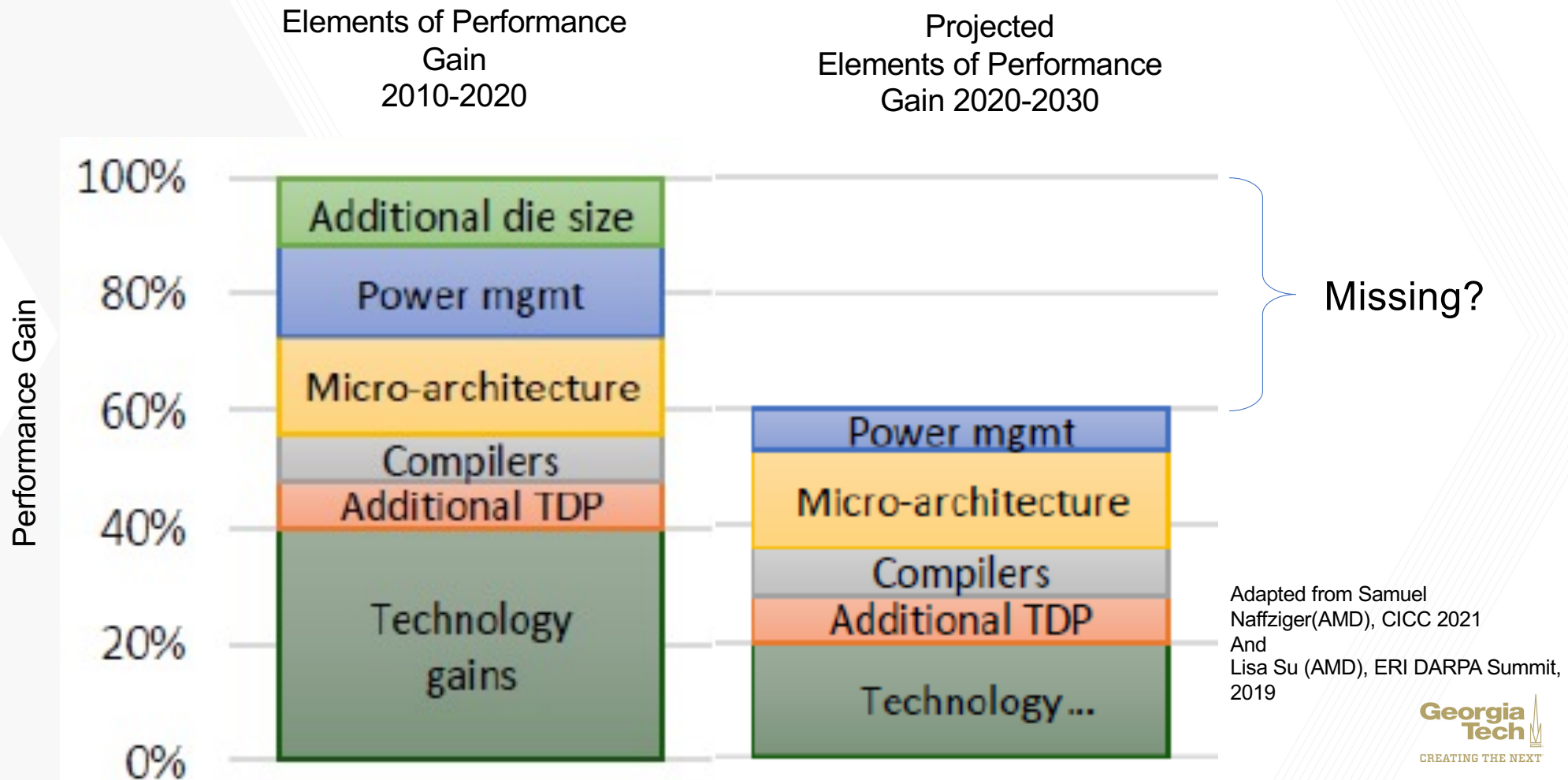
High-K Metal Gate



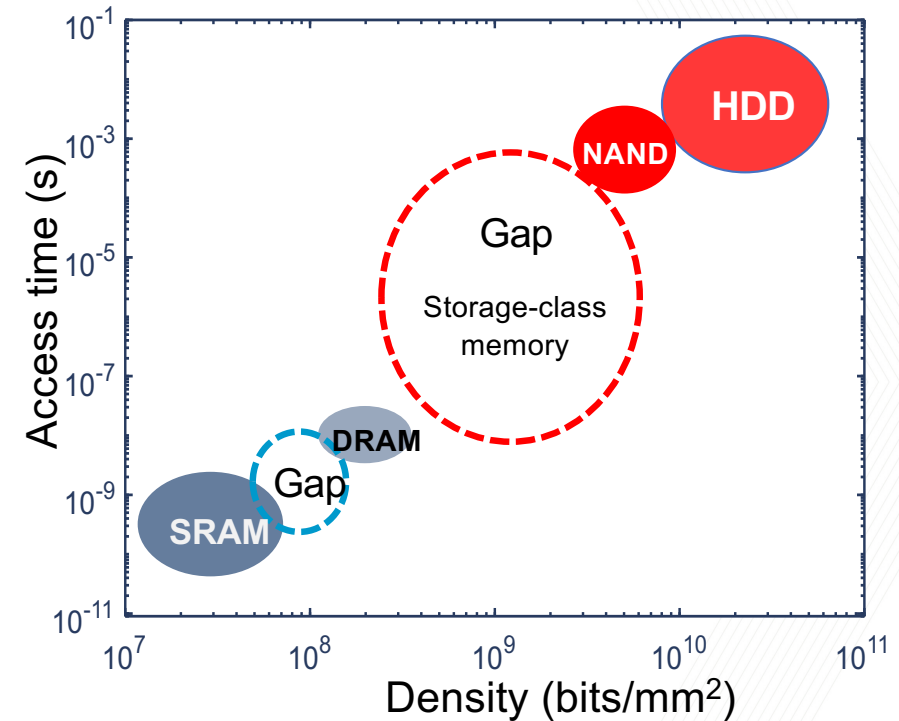
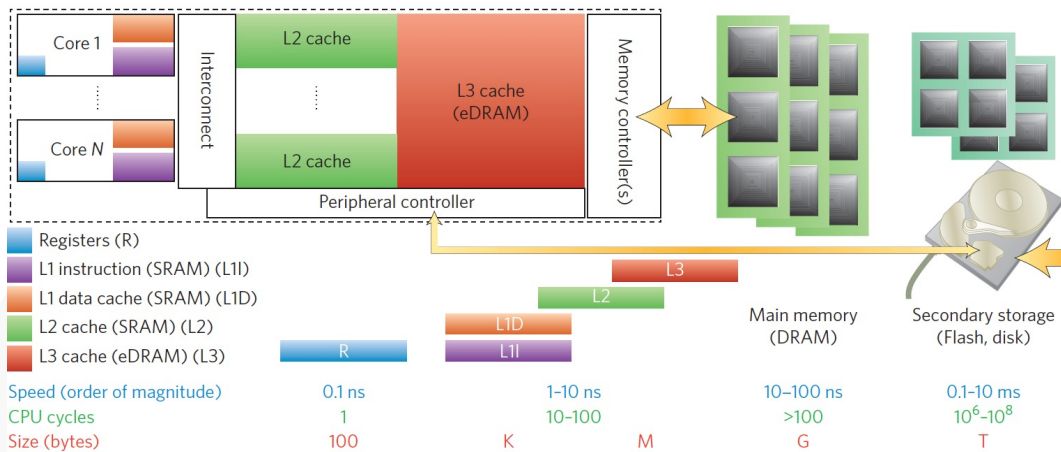
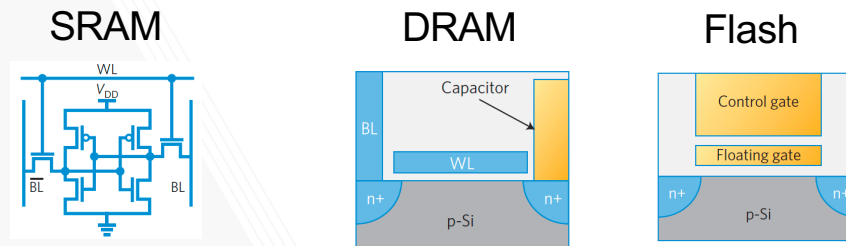
High Bandwidth Memory- 2015



Materials are central to *Future Electronics*

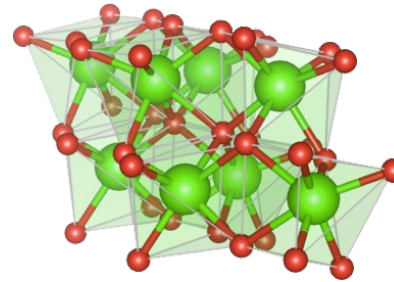


Generational challenges in memory



1. Scaling challenges
2. Gaps in the memory hierarchy

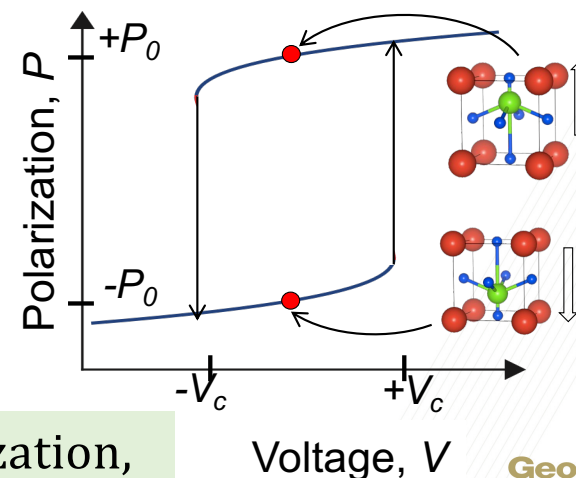
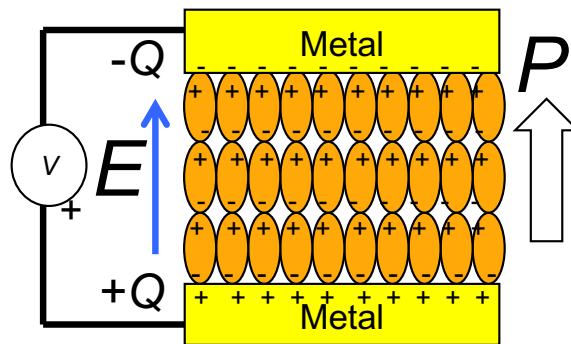
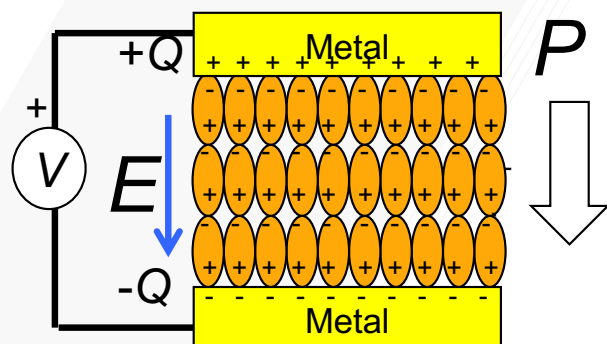
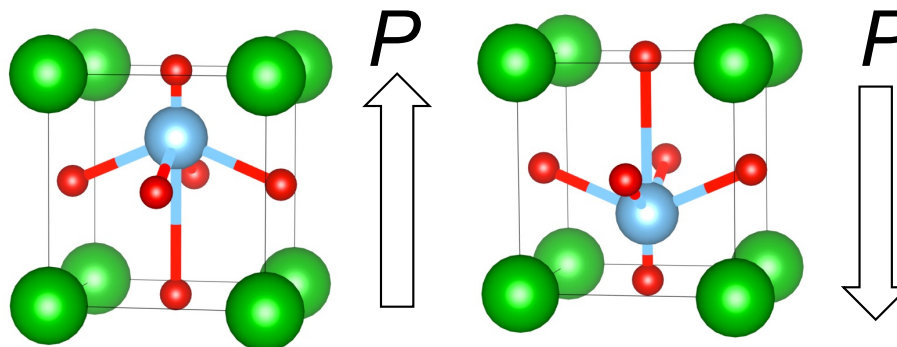
Let's dive down to devices and materials



Ferroelectricity

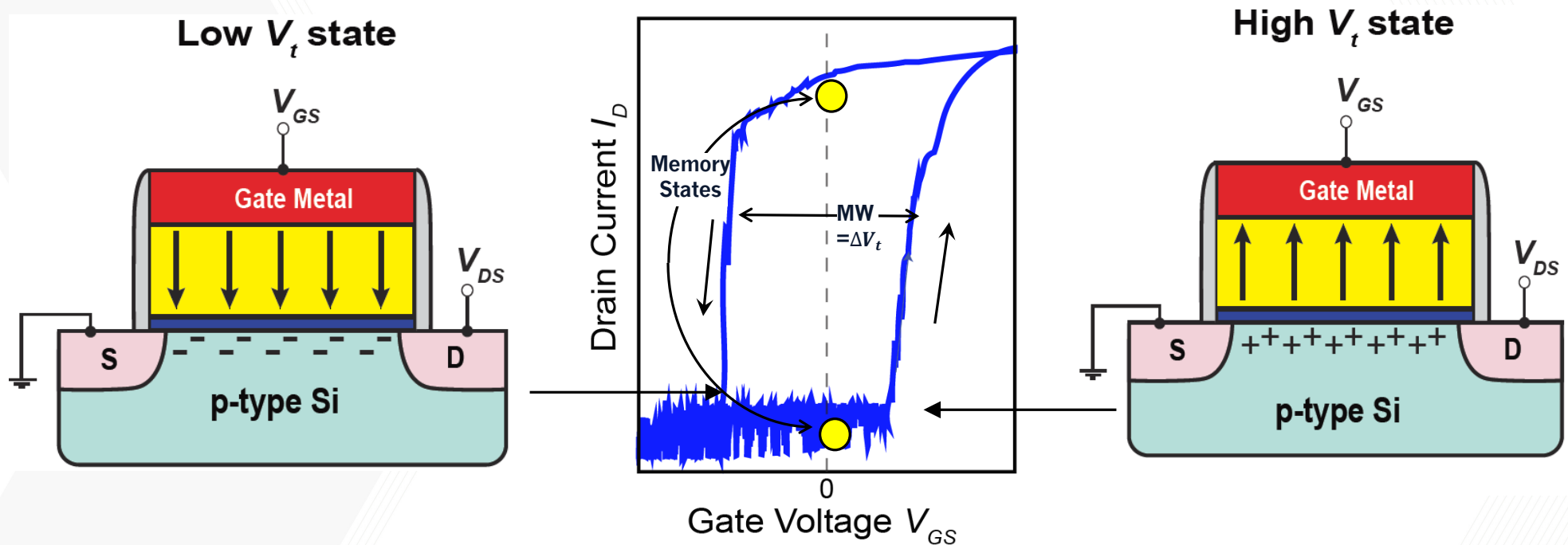
Classical Ferroelectric
 PbTiO_3 , BaTiO_3 etc.

Emerging CMOS compatible
Ferroelectrics:
Doped HfO_2



A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the “remnant” polarization.

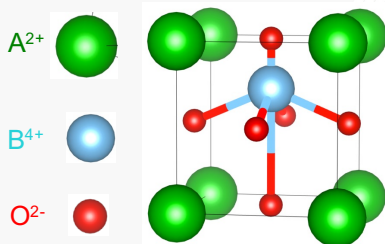
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for code storage in microcontrollers.

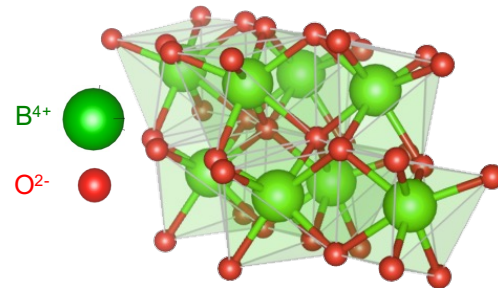
2. Controlled annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al.* *Appl. Phys. Lett.* 99, 112904 (2011)
- Boscke *et al.* *2011 IEEE Int. Electron Devices Meeting*. p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al.* *Nano Lett.* 12, 4318 (2012)

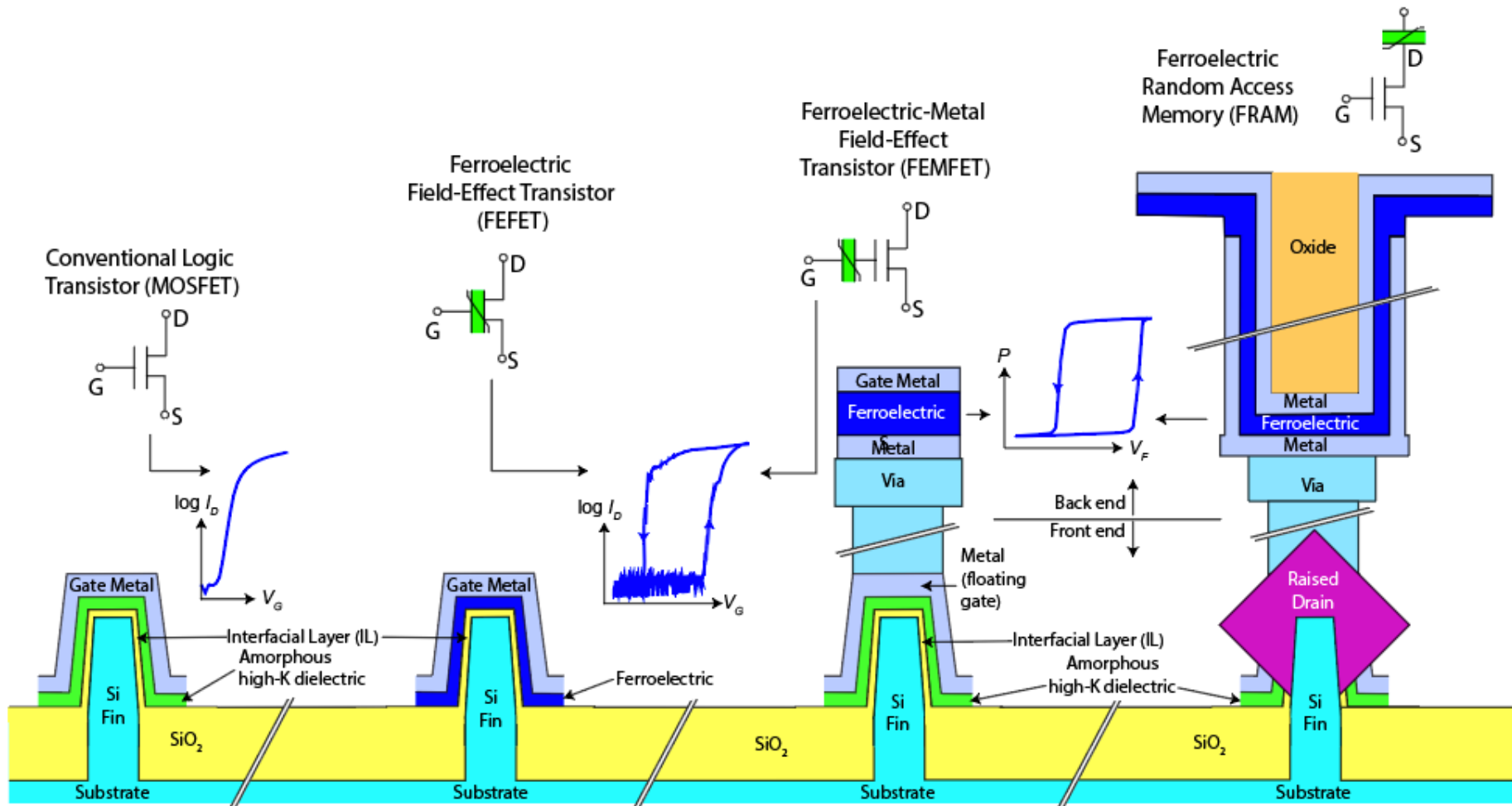
Perovskite-structure
ferroelectric oxide
(ABO_3)



Fluorite-structure
ferroelectric oxide
(BO_2)



Ferroelectric devices



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

Progress in FEFET technology

1

Write voltage
and Memory Window

2

Read/Write
Speed

3

Device-to-device
variation

4

Reliability and endurance

Specs

<1.5 V write voltage
>0.5 V memory window

<10 ns write speed
<10 ns read-after-write delay

$\Delta V_{t,3\sigma} = 20\text{-}50\text{ mV}$
(7 nm node)

>10¹² cycles

Progress in FEFET technology

1

Write voltage
and Memory Window

2

Read/Write
Speed

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Device-to-device
variation

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Reliability and endurance

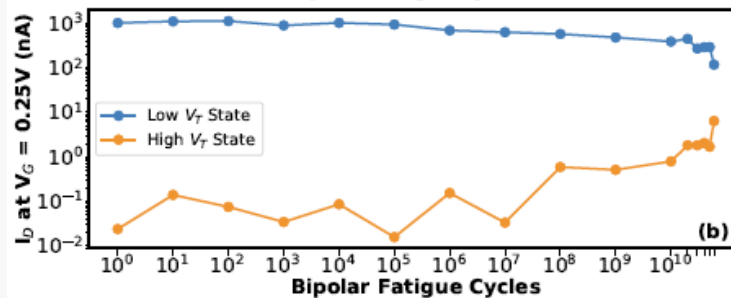
Specs

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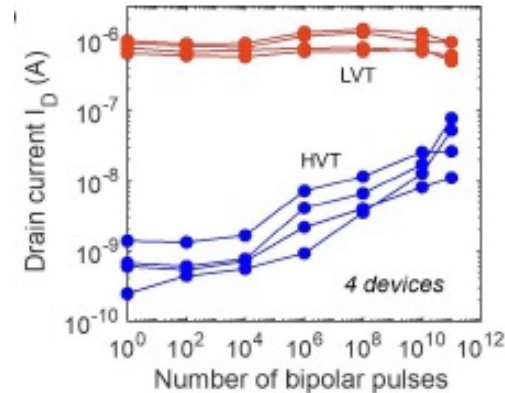
<10 ns write speed
<10 ns read-after-write delay

$\Delta V_{t,3\sigma} = 20\text{-}50\text{ mV}$
(7 nm node)

> 10^{12} cycles

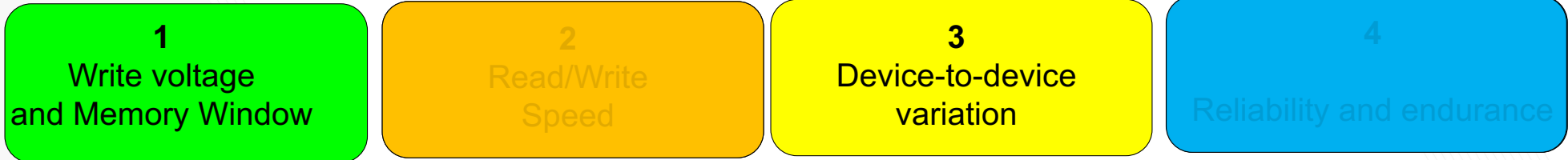


Tan et al. IEEE EDL 42, 994 (2021).



Dutta et al. IEEE EDL 43, 383 (2022).

Progress in FEFET technology



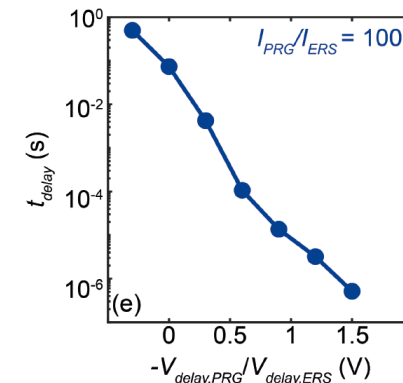
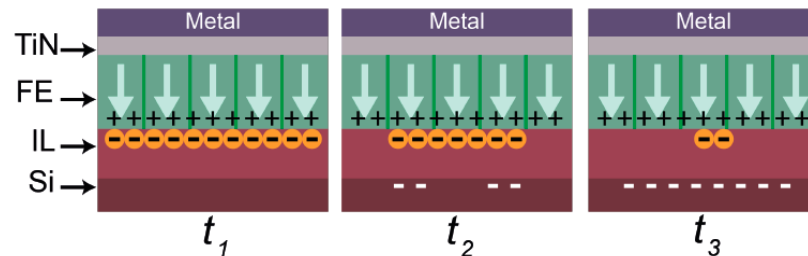
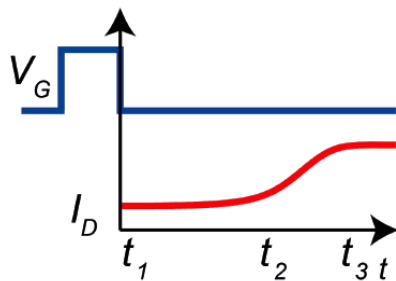
Specs

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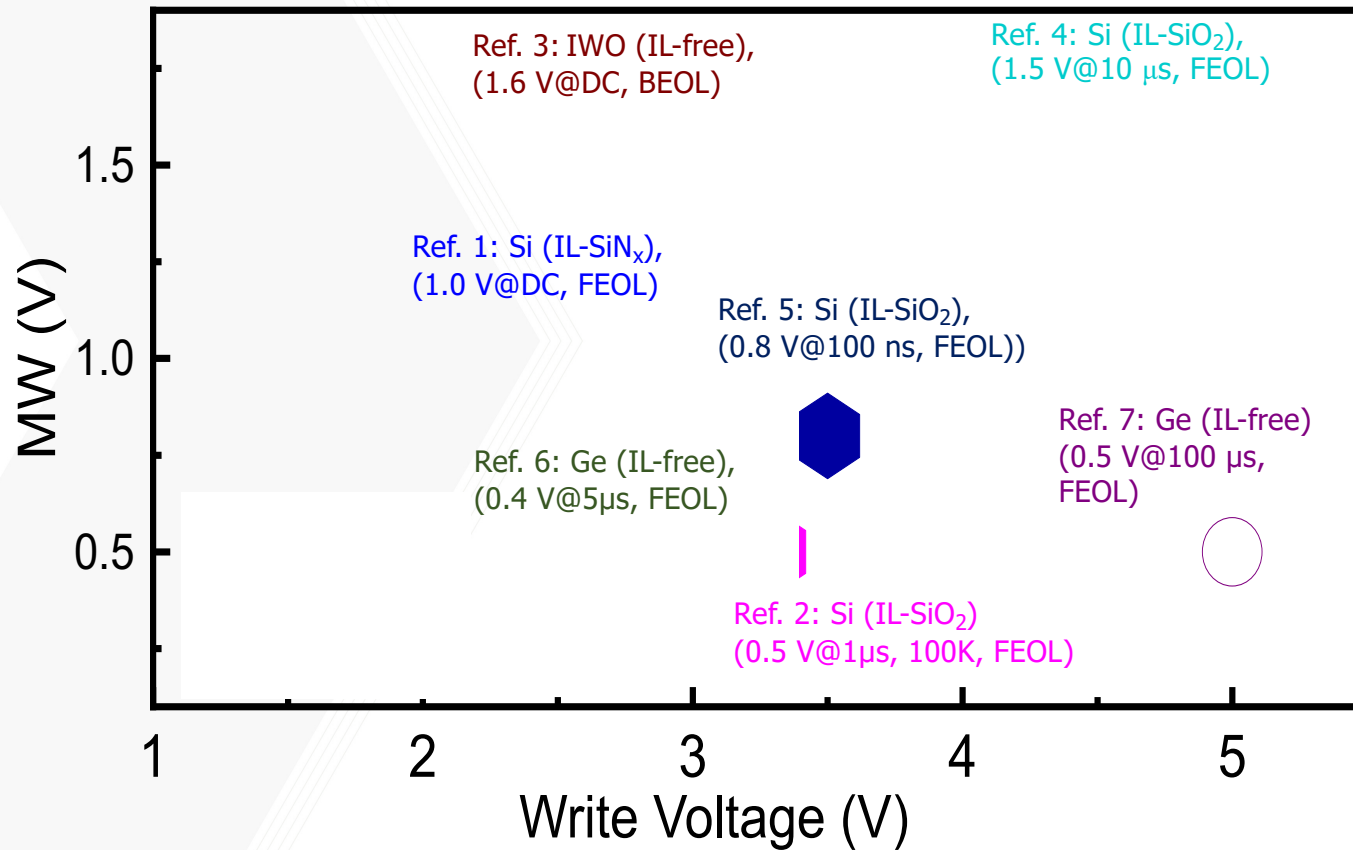
$\Delta V_{t,3\sigma} = 20\text{-}50\text{ mV}$
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> 10^{12} cycles



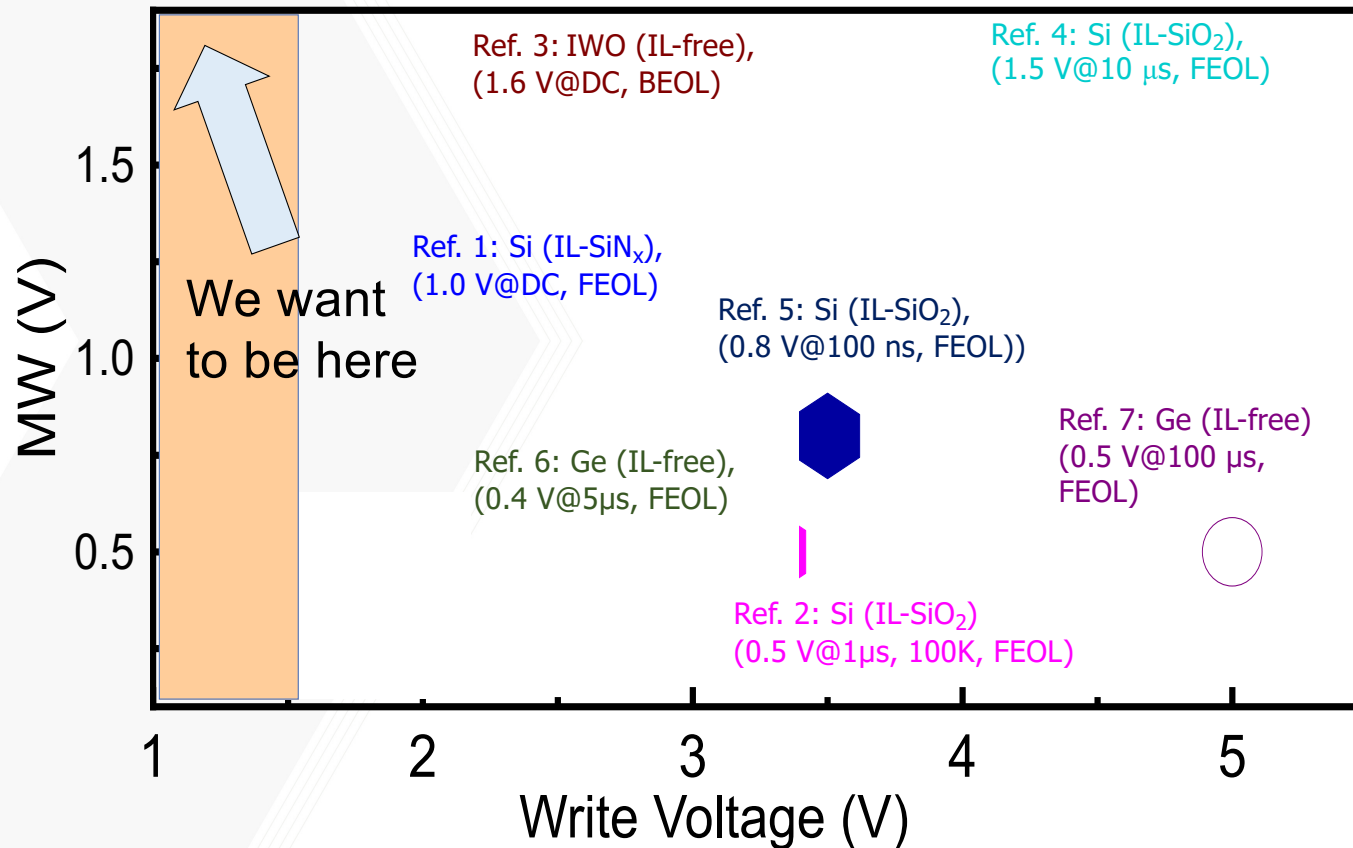
Wang, Z., Tasneem, N., Hur, J., Chen, H., Yu, S., Chern, W., & Khan, A. (2021, December). Standby bias improvement of read after write delay in ferroelectric field effect transistors. In *2021 IEEE International Electron Devices Meeting (IEDM)* (pp. 19-3). IEEE.

Benchmarking Memory Window v. Write Voltage Tradeoff



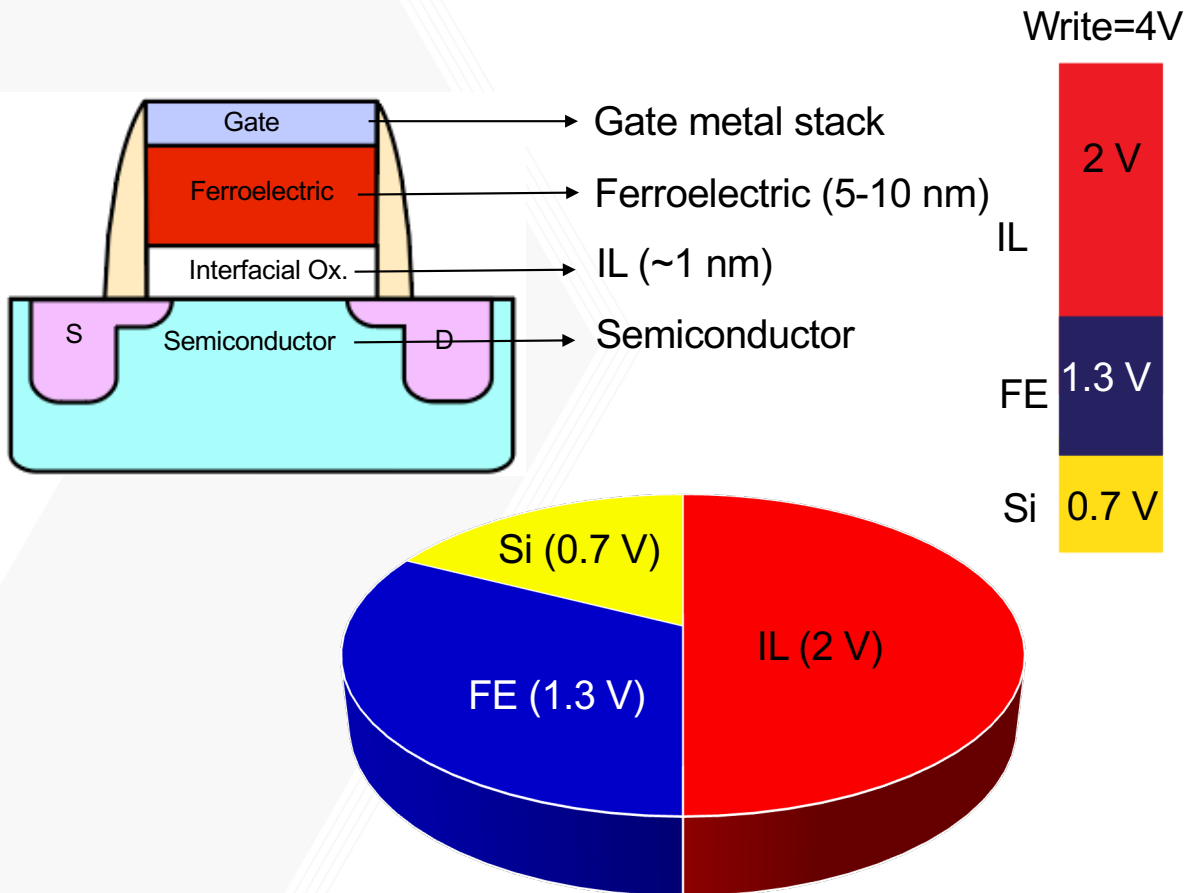
- [1] Tan *et al.*, *IEEE EDL*, 42, 994, (2021).
- [2] Tan *et al.*, *2020 IEEE Symposium on VLSI Technology* (2020).
- [3] Dutta *et al.*, *IEEE EDL*, 43, 382 (2022).
- [4] Dünkel *et al.*, *IEDM* (2017).
- [5] Nguyen *et al.*, *IEEE EDL*, 42, 1295, (2021).
- [6] Liu *et al.*, *IEEE EDL*, 40, 1419, (2019).
- [7] Zacharaki *et al.*, *ACS Appl. Electron. Mater.*, 4, (2022).

Benchmarking Memory Window v. Write Voltage Tradeoff

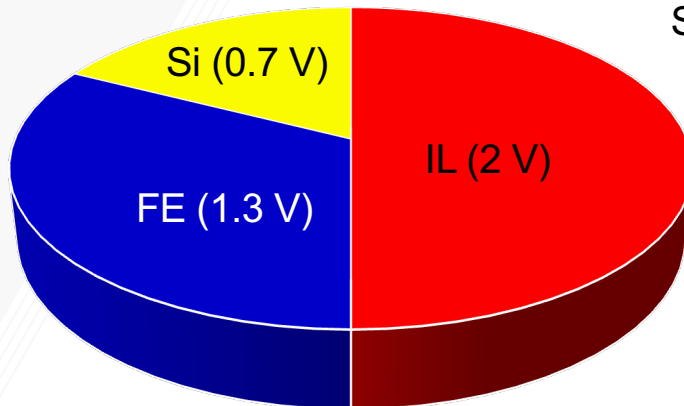
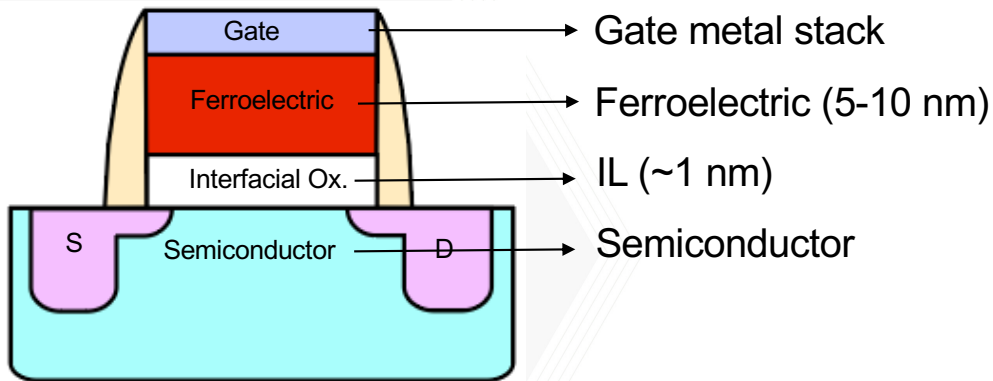


- [1] Tan *et al.*, *IEEE EDL*, 42, 994, (2021).
- [2] Tan *et al.*, *2020 IEEE Symposium on VLSI Technology* (2020).
- [3] Dutta *et al.*, *IEEE EDL*, 43, 382 (2022).
- [4] Dünkler *et al.*, *IEDM* (2017).
- [5] Nguyen *et al.*, *IEEE EDL*, 42, 1295, (2021).
- [6] Liu *et al.*, *IEEE EDL*, 40, 1419, (2019).
- [7] Zacharaki *et al.*, *ACS Appl. Electron. Mater.*, 4, (2022).

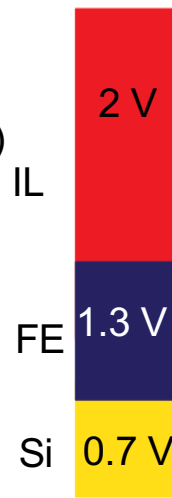
Write voltage vs. memory window trade-off



Write voltage vs. memory window trade-off



Write=4V

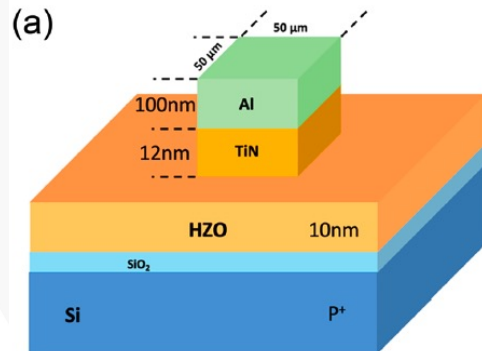


Reducing the thickness of the IL or increasing the K of the IL.

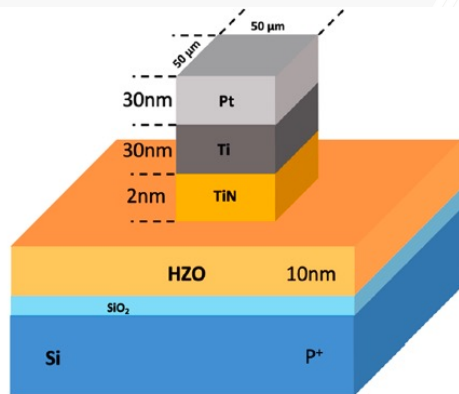
Reducing FE thickness reduces MW.
 $MW_{\max} = 2V_C$

Changing the band-gap of the semiconductor By changing the channel material from Si to SiGe or Ge.

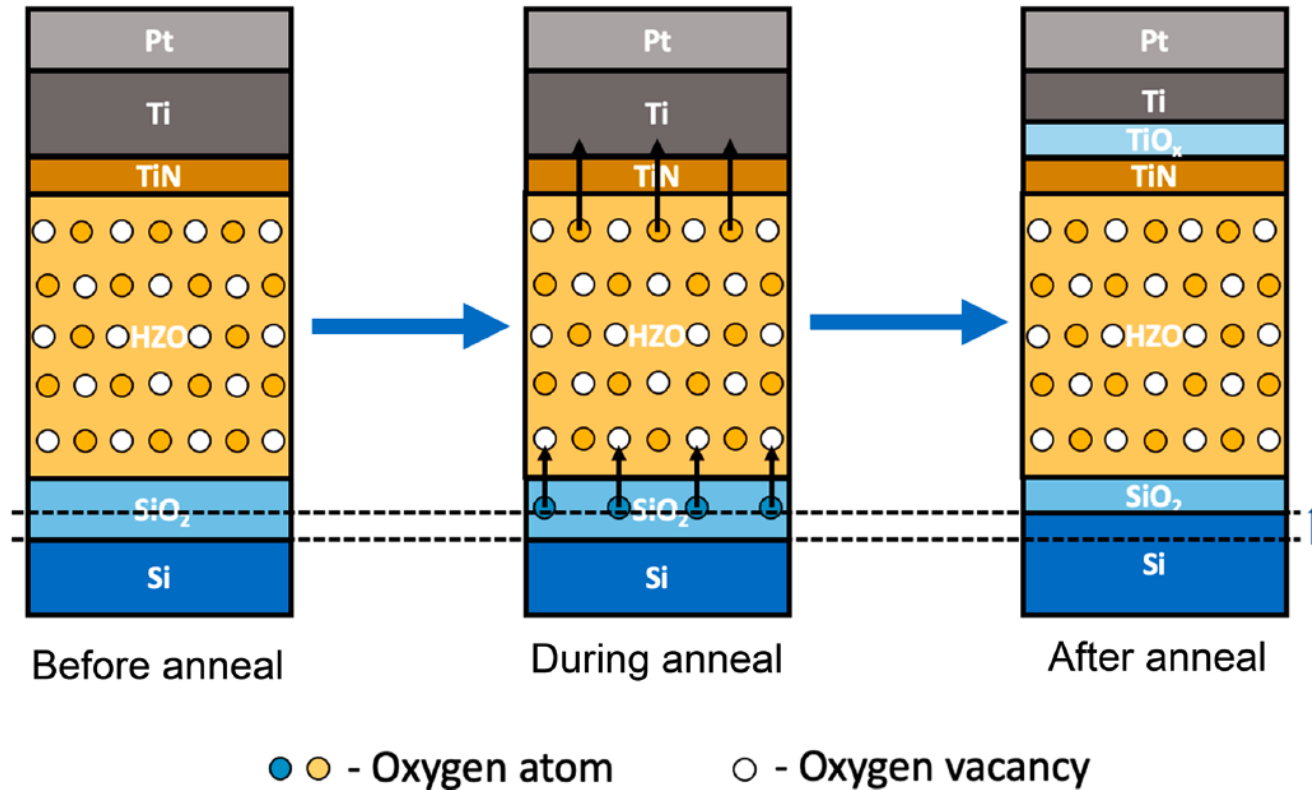
Remote oxygen scavenging to reduce IL thickness



Non-Scavenging



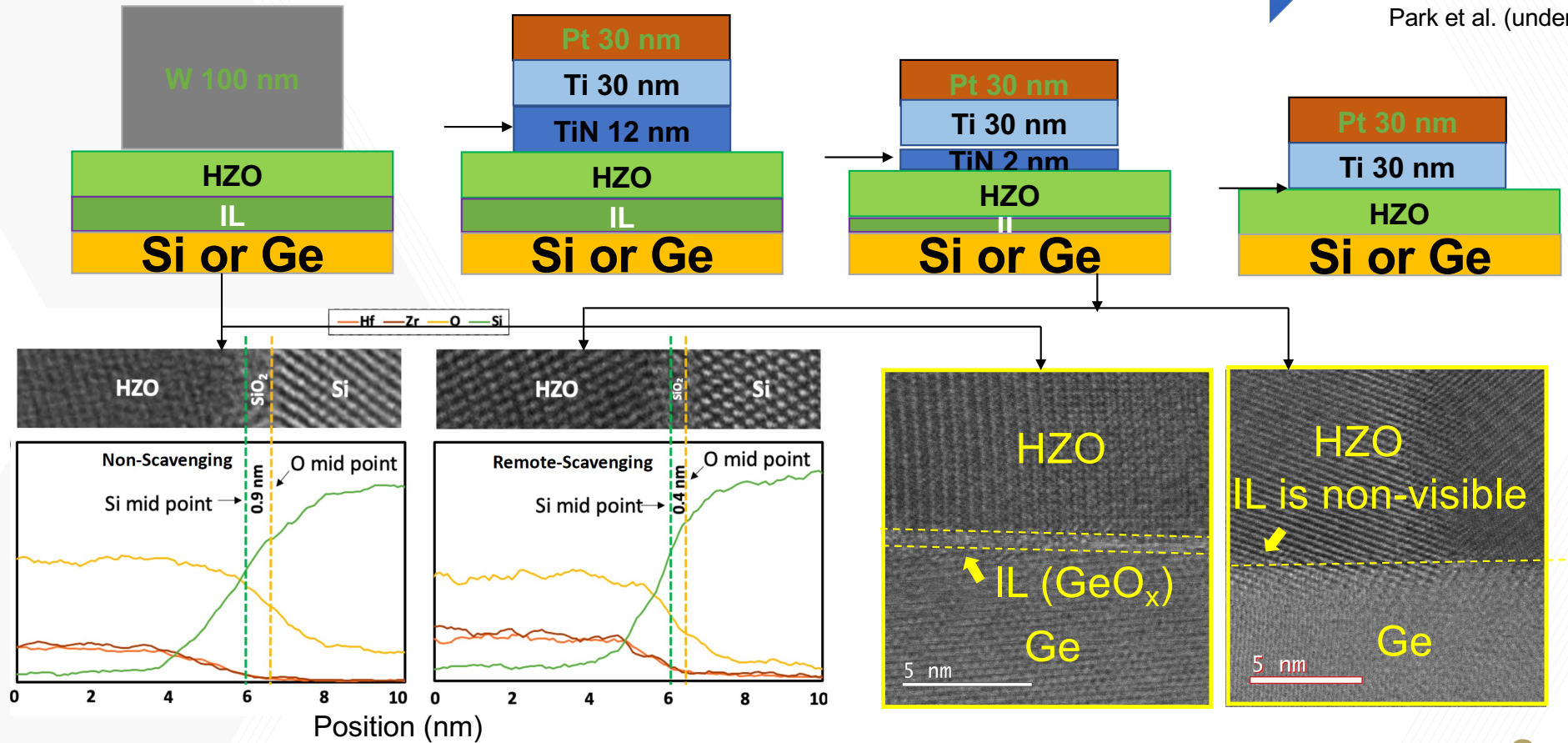
Remote-Scavenging



Tasneem et al. "Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium–Zirconium Oxide-Based Metal–Oxide–Semiconductor Structures", ACS Appl. Mater. Interfaces 2022, 14, 43897–43906

Decrease in IL thickness

Park et al. (under review)



Remote oxygen scavenging can result in controllable IL thickness.

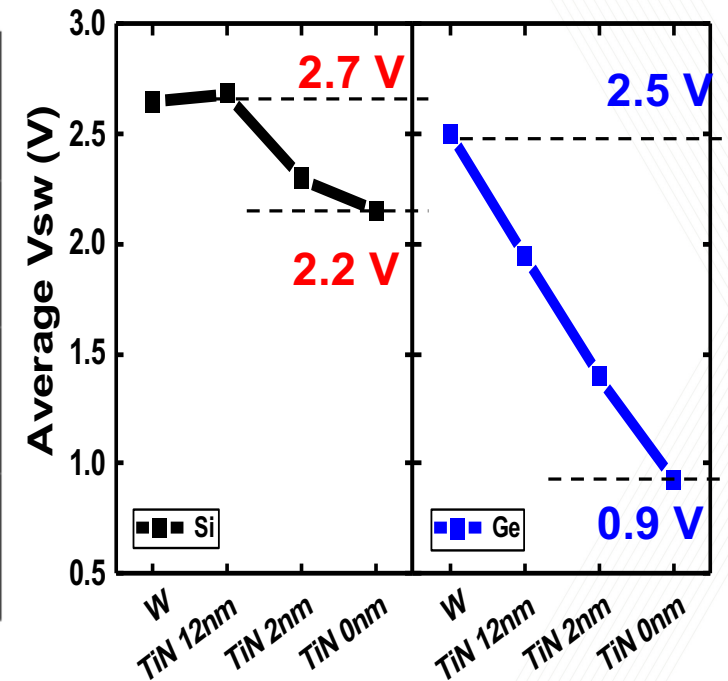
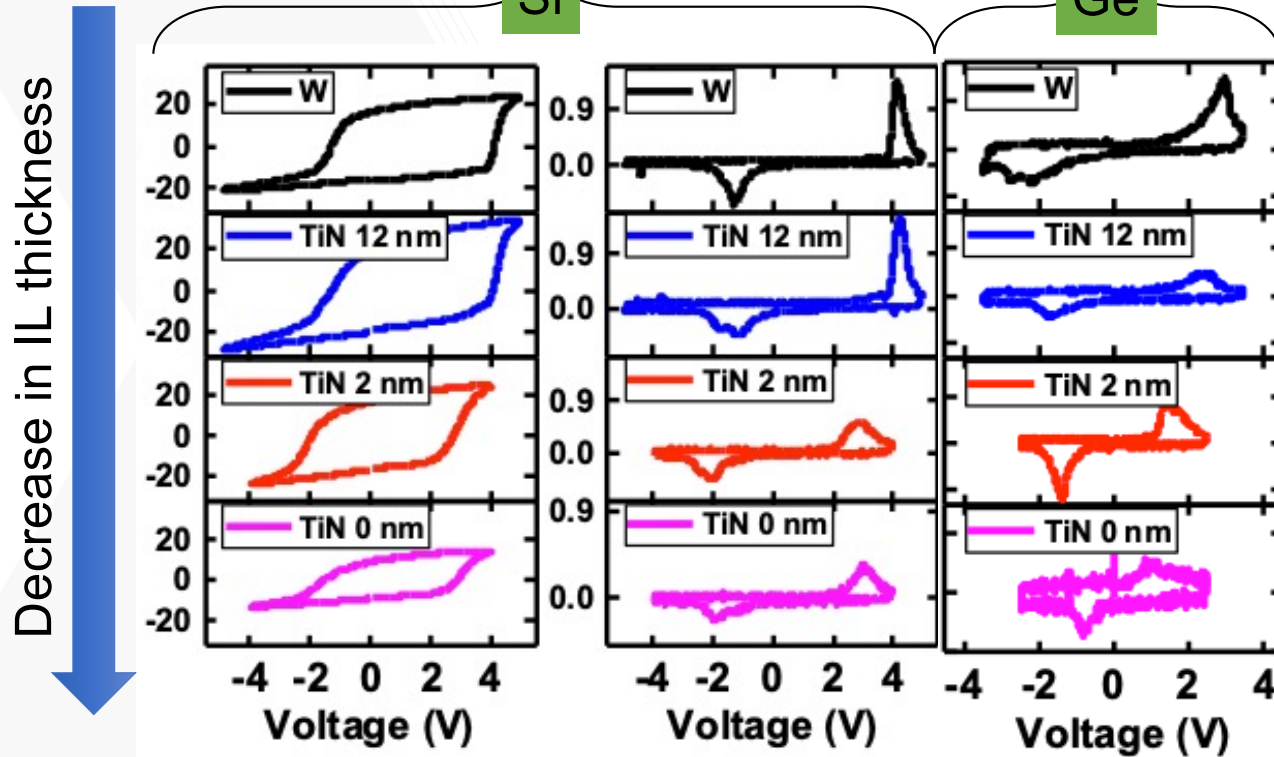
The effect of the IL thickness on Vc



Nujhat
Tasneem

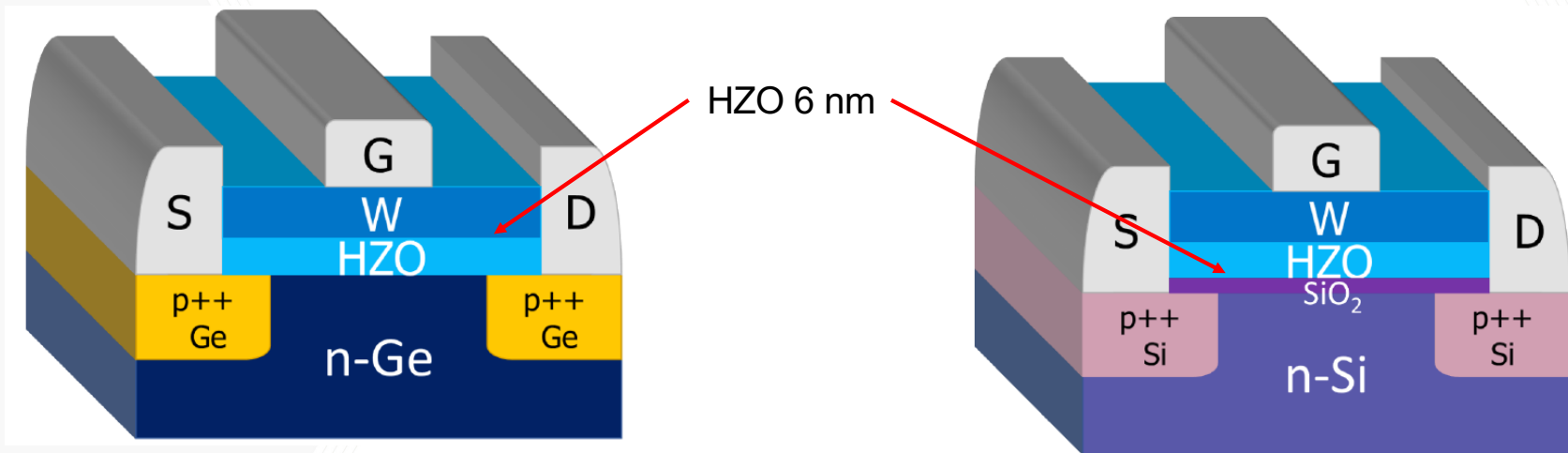


Chinsung
Park



Dramatic reduction in coercive voltage is observed in Ge platform with the change of the gate metal stack.

Ge-channel FEFETs with record-low write voltages



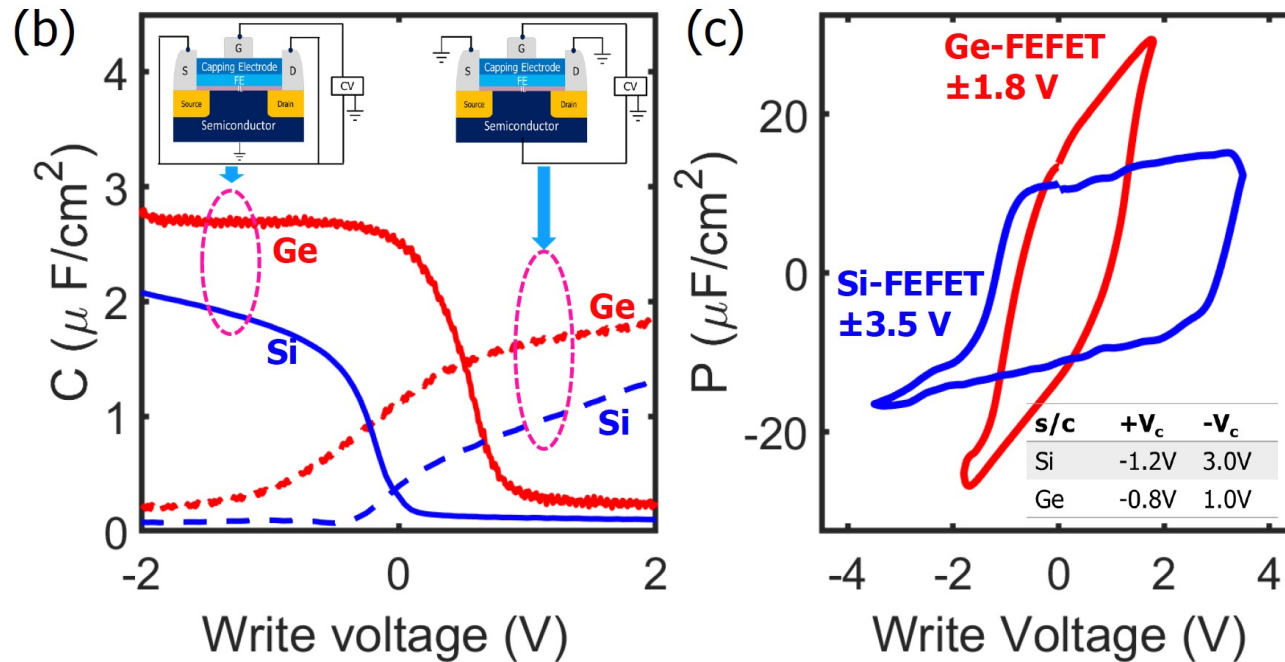
Si and Ge-channel FEFETs fabricated with the same 6 nm HZO layers, under similar process and fabrication conditions.



Dr. Dipjyoti
Das

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

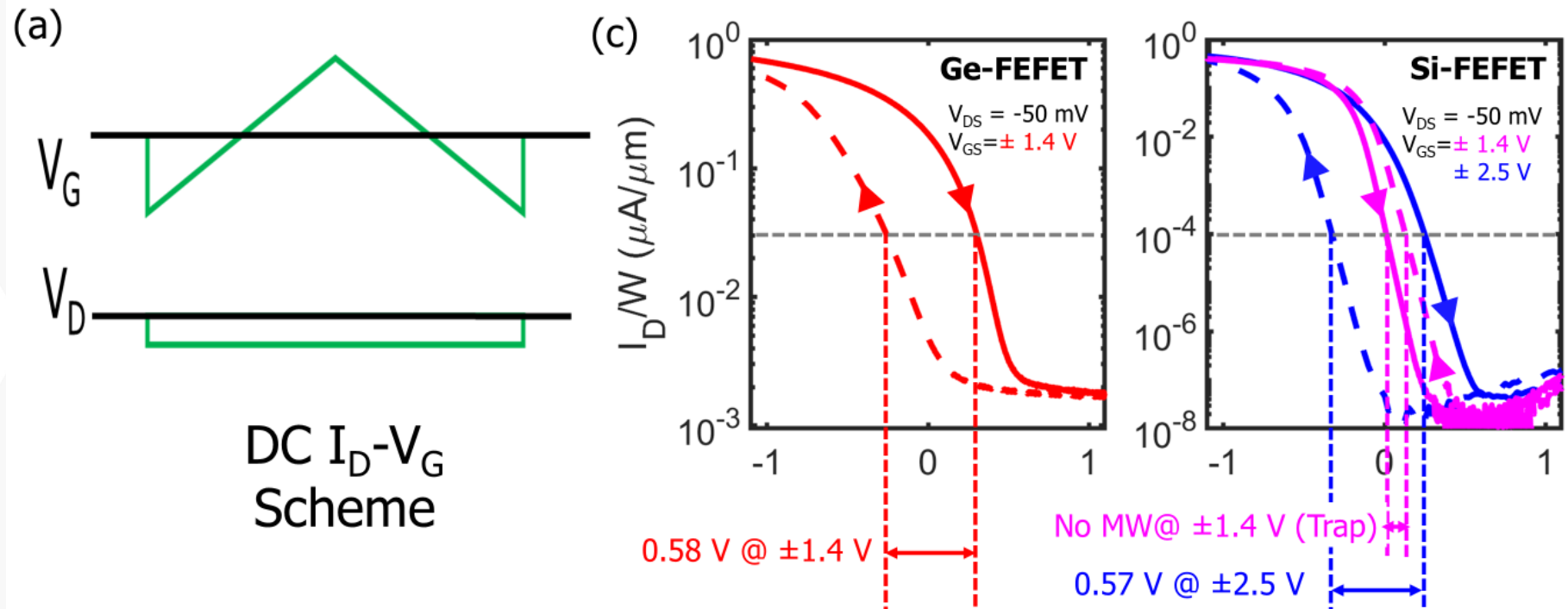
Ge-channel FEFETs with record-low write voltages



Significant increase on the on-capacitance and reduction in coercive voltage in Ge-channel FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

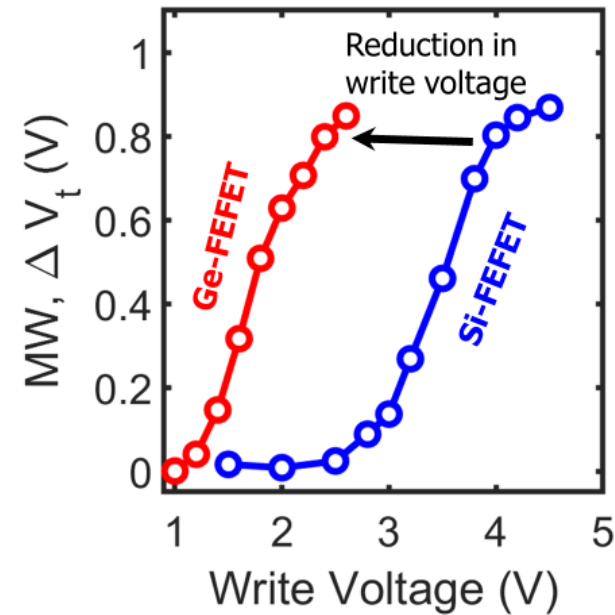
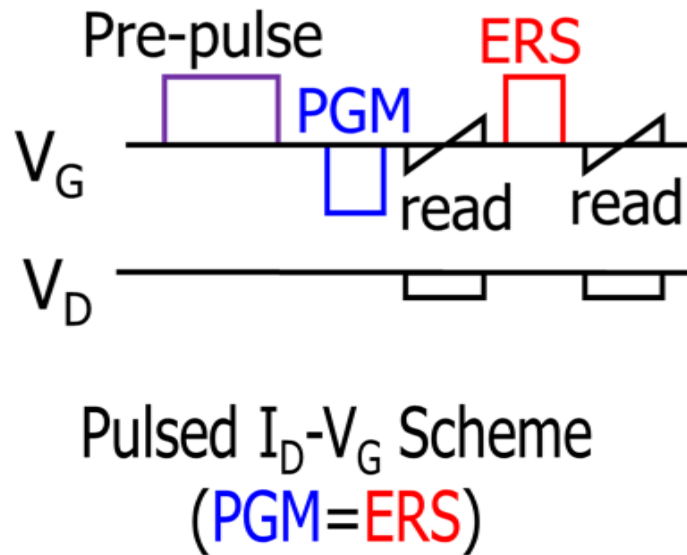
DC I_D - V_G characteristics



Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

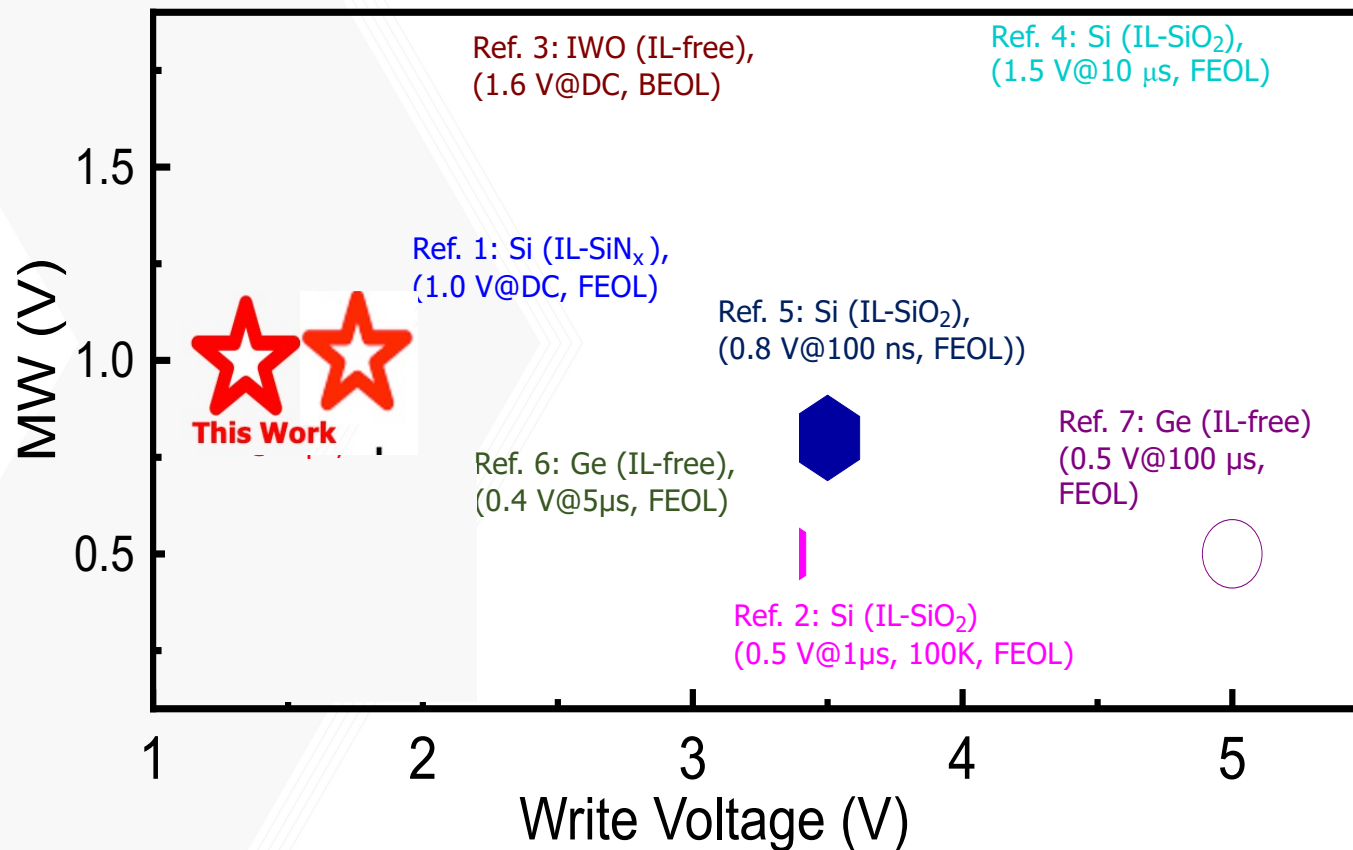
Pulsed I_D - V_G characteristics



Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Benchmarking Memory Window v. Write Voltage Tradeoff



Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

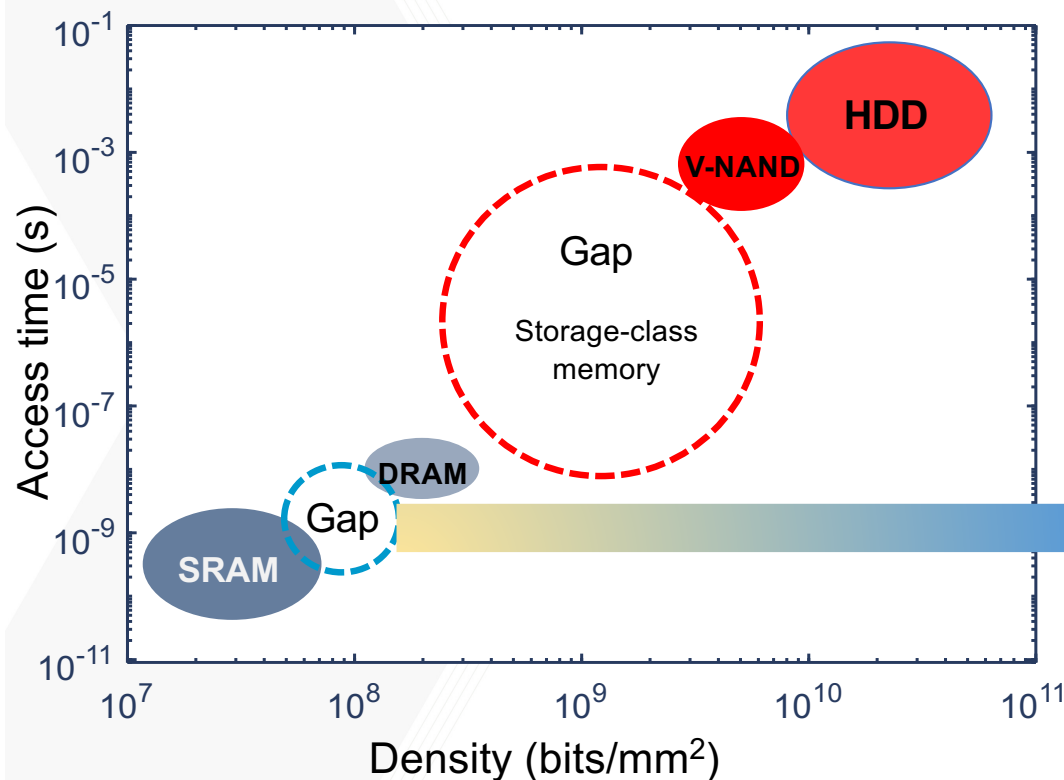
- [1] Tan *et al.*, *IEEE EDL*, 42, 994, (2021).
- [2] Tan *et al.*, *2020 IEEE Symposium on VLSI Technology* (2020).
- [3] Dutta *et al.*, *IEEE EDL*, 43, 382 (2022).
- [4] D unkel *et al.*, *IEDM* (2017).
- [5] Nguyen *et al.*, *IEEE EDL*, 42, 1295, (2021).
- [6] Liu *et al.*, *IEEE EDL*, 40, 1419, (2019).
- [7] Zacharaki *et al.*, *ACS Appl. Electron. Mater.*, 4, (2022).

FEFET as an embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM ⁷⁰	eFlash (FG)	eFlash (SG MONOS) ⁴²	eFlash (SONOS) ⁴¹	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based) ⁶⁷
Cell size	120-150F ²	40F ²	40-60F ²	40-50F ²	50-60F ²	10-30F ²	10-30F ²	30-40F ²	50-60F ²
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5-4 V	~1.5 V	1-3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1-10 pJ	1-10 fJ	1-10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1-10 ns	1-10 ns	1-10 ns	1 μ s
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1-10 ns	1-10 ns	1-25 ns	50-100 ns
Endurance	>10 ¹⁶	>10 ¹⁶	~10 ⁴	~10 ⁵	~10 ⁶	10 ⁵ -10 ⁹	>10 ¹⁰	>10 ¹²	>10 ¹⁴

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

Ferroelectrics for last level cache



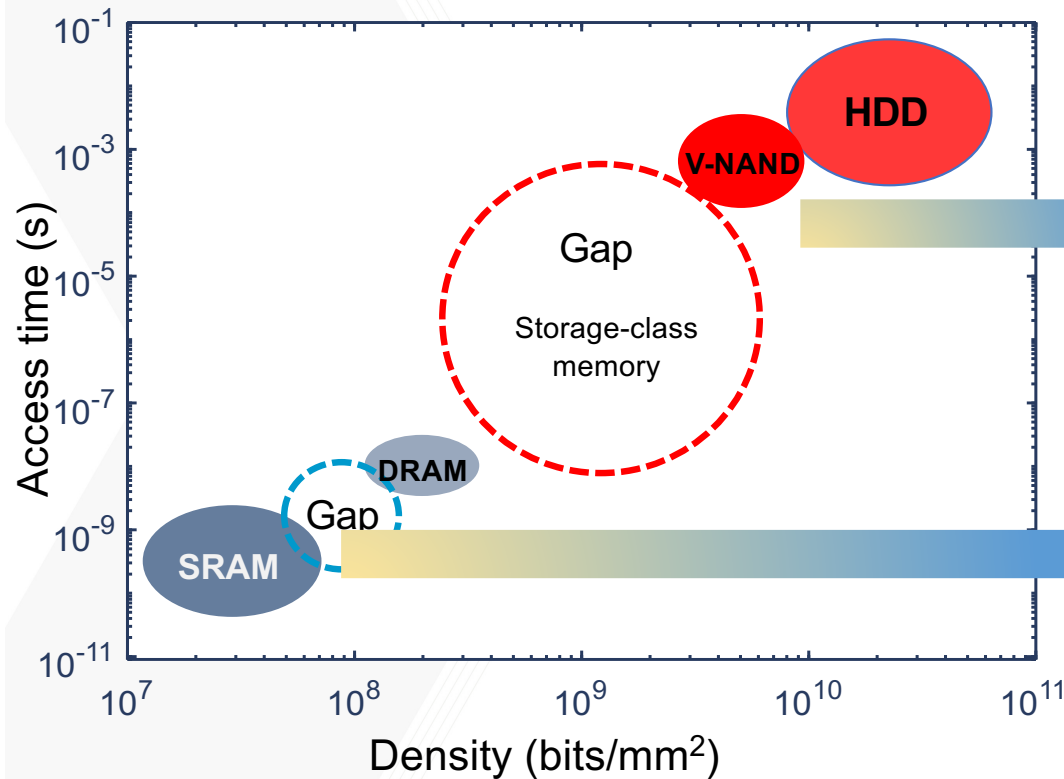
Ferroelectrics for embedded memories/cache

- Density
- BEOL compatibility
- Fast

Cell area | Speed

DRAM:	6-30F² <10 ns
FEFET:	5-10F² 5-10 ns
SRAM:	140-280F² <1 ns

Ferroelectrics for flash

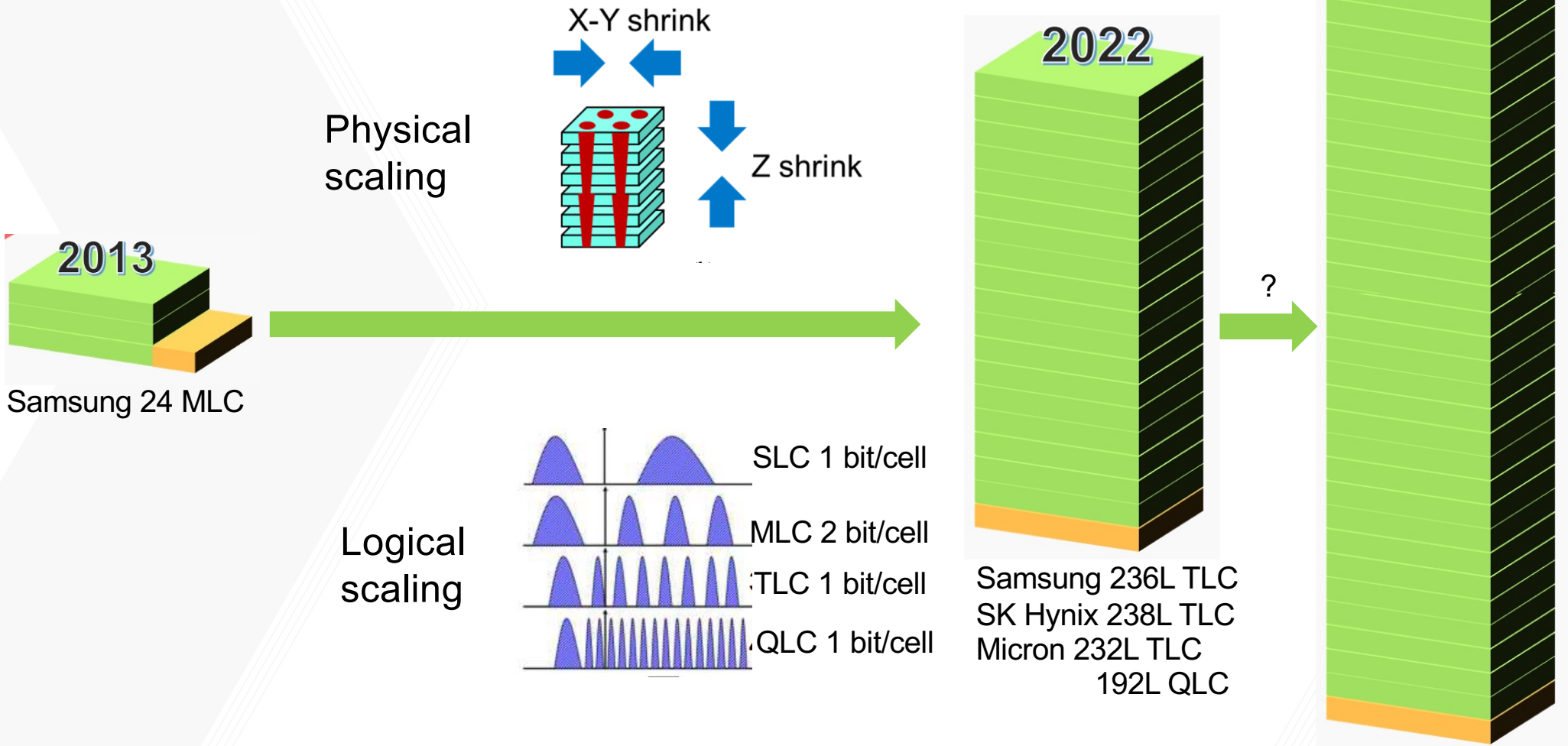


Ferroelectrics for flash?

Ferroelectrics for embedded memories/cache

- Density
- BEOL compatibility
- Fast

Vertical NAND Scaling



Vertical NAND scaling toward 1000 layers

Layer stacking trend

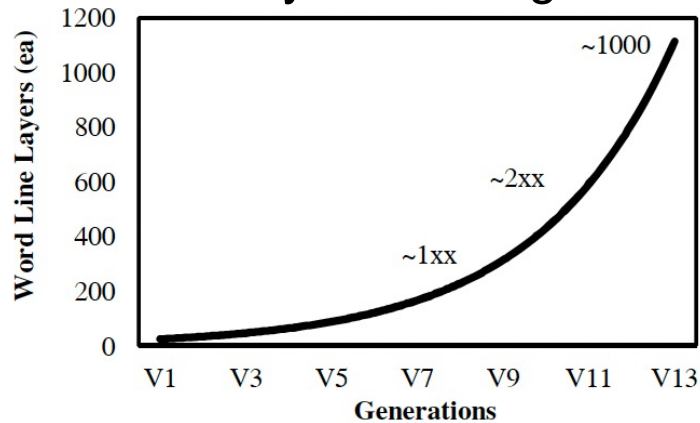


Fig. 1. Number of word line layers by generation

Package thickness limits the NAND chip height.

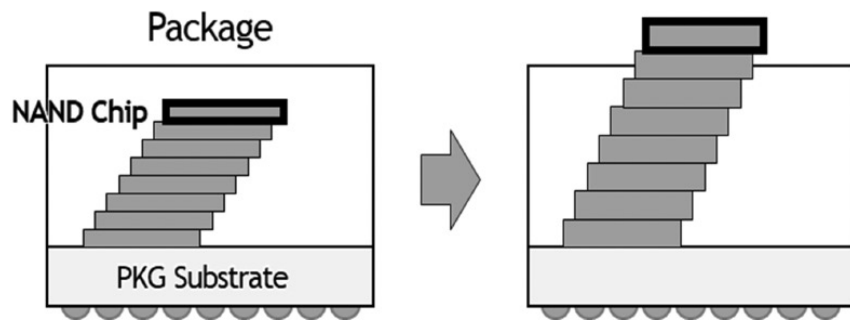
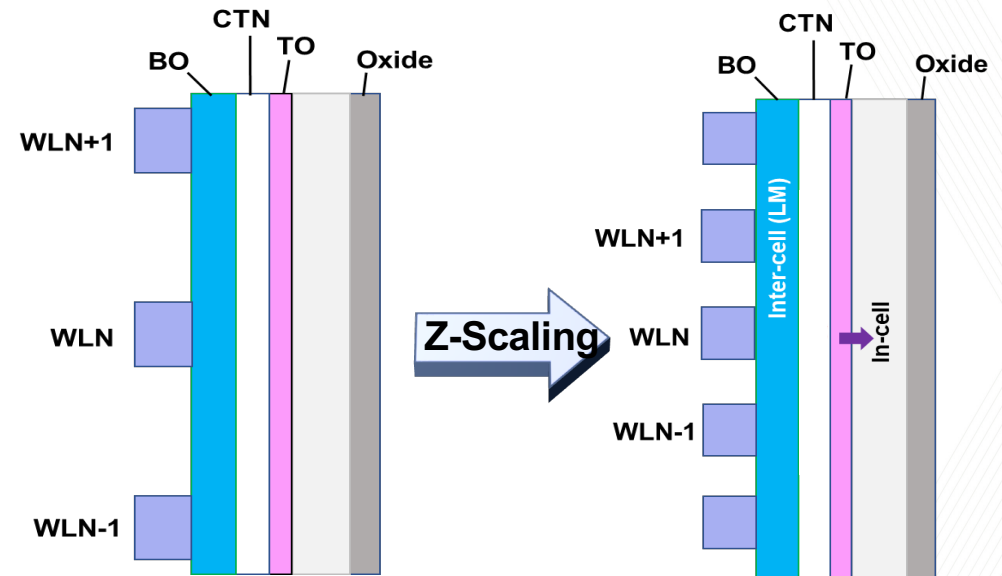


Fig. 4. Package thickness limit with multiple chips

Aggressive Z-scaling is required.

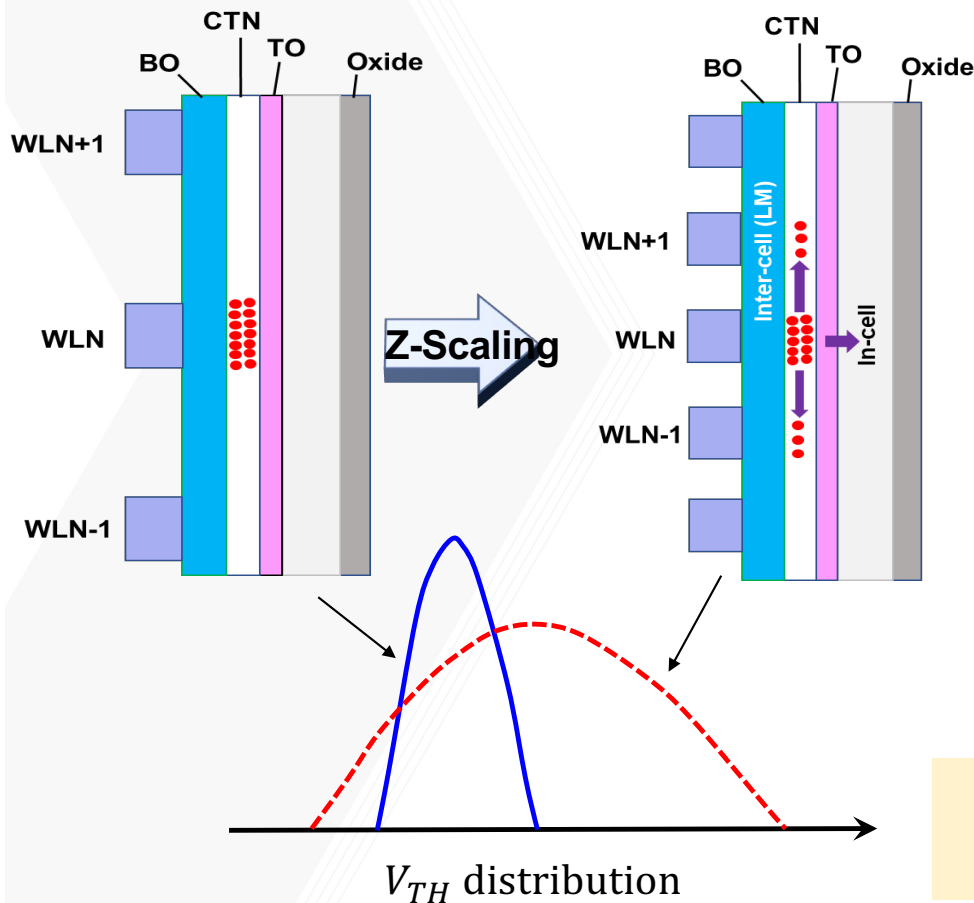


The mold height (cell height) needs to be reduced dramatically.

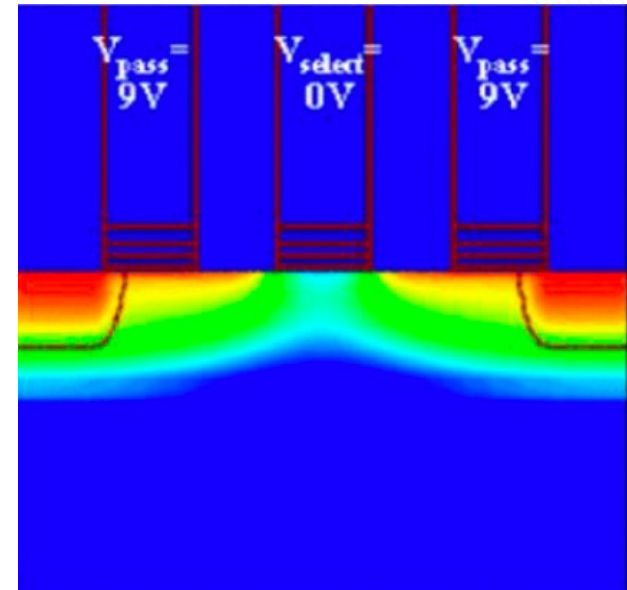
Han et al. Fundamental Issues in VNAND Integration
Toward More Than 1K Layers. IEDM 2023. Paper 35.1

Challenges for 1000+ layer vertical NAND

1 Lateral charge migration



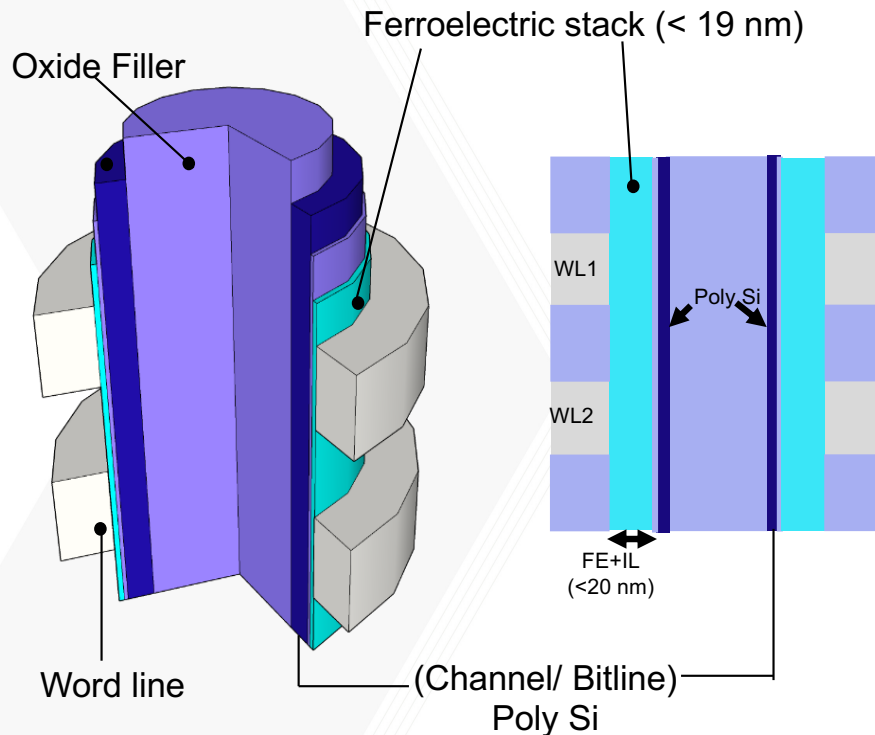
2 High write voltage



Write voltage of state of the art NAND is >20 V.
Large write voltage affects effective threshold voltage,
similar to cell-to-cell interference.

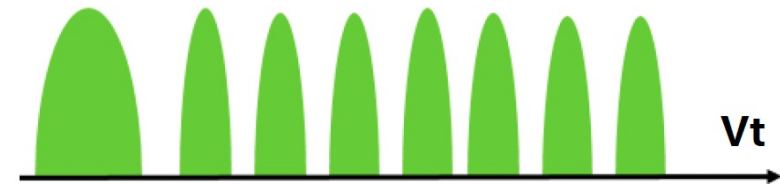
Cell-to-cell interference will significantly
increase with aggressive Z-scaling for 1000L
VNAND.

Ferroelectric as a replacement for Charge Trap Layer

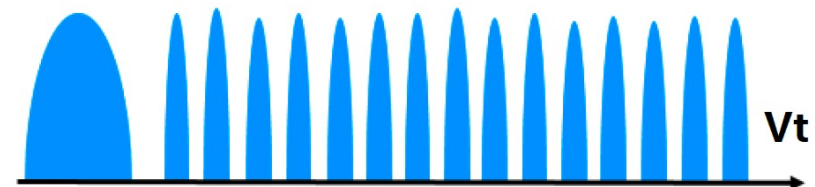


To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm

TLC:3 bits/cell $\rightarrow$ 8 Vt level MW $\approx$ 6V



QLC:4 bits/cell $\rightarrow$ 16 Vt level MW $\approx$ 7.5 V



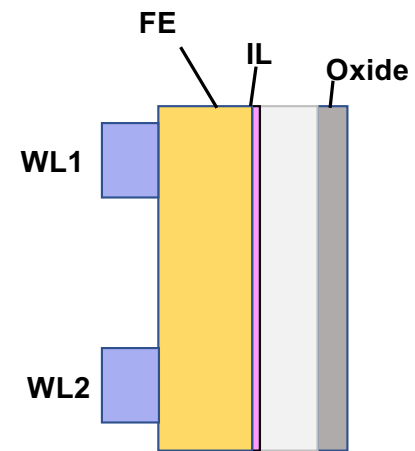
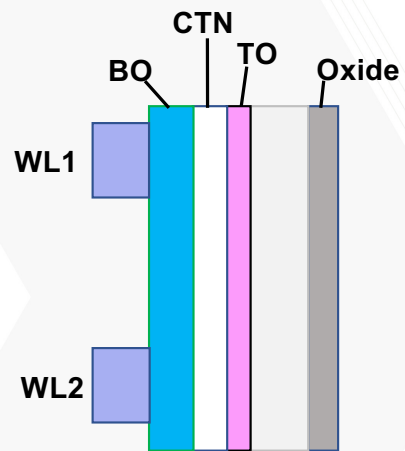
Design constraints

Ferroelectric thickness, $t_{FE} \leq 19$ nm

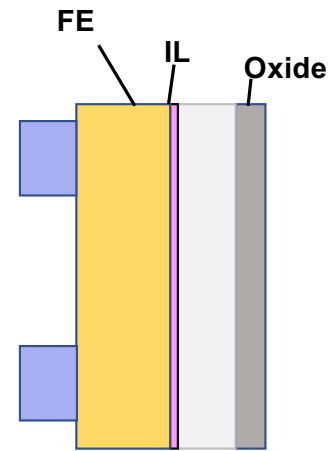
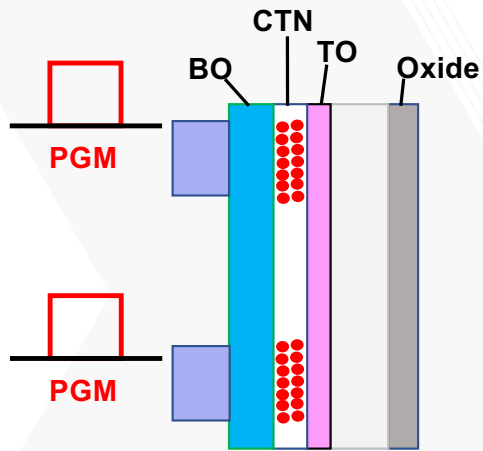
Write voltage ≤ 15 V

Memory window MW > 6.5 V

CTF vs FEFET

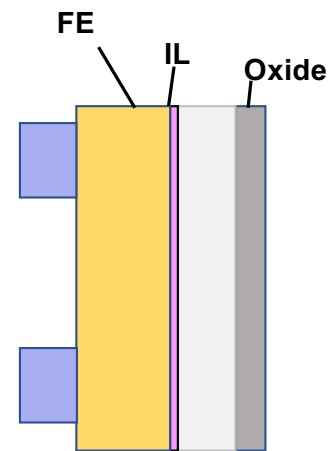
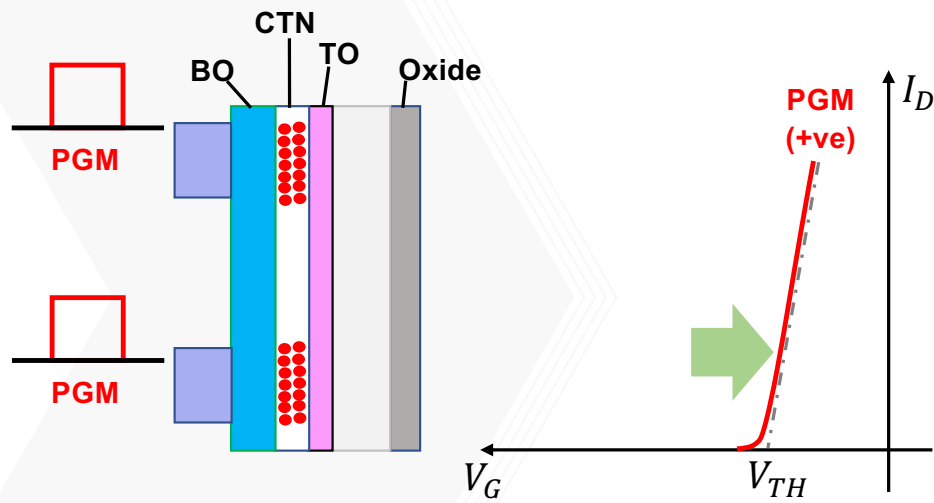


CTF vs FEFET (Program)



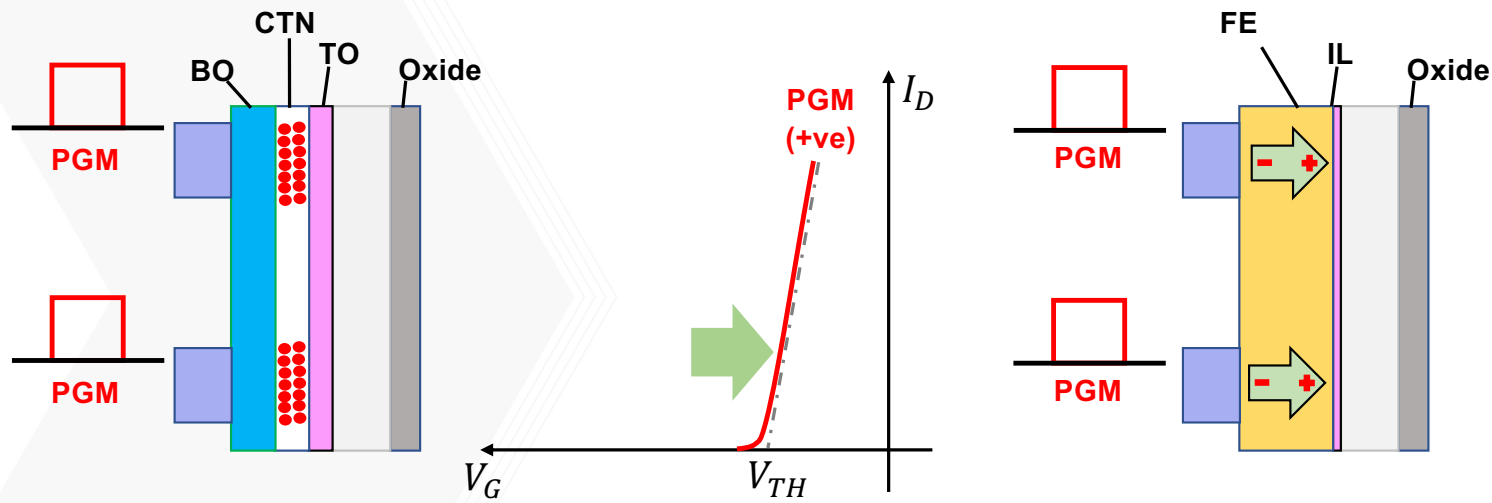
CTF that stores data in the form of charge

CTF vs FEFET (Program)



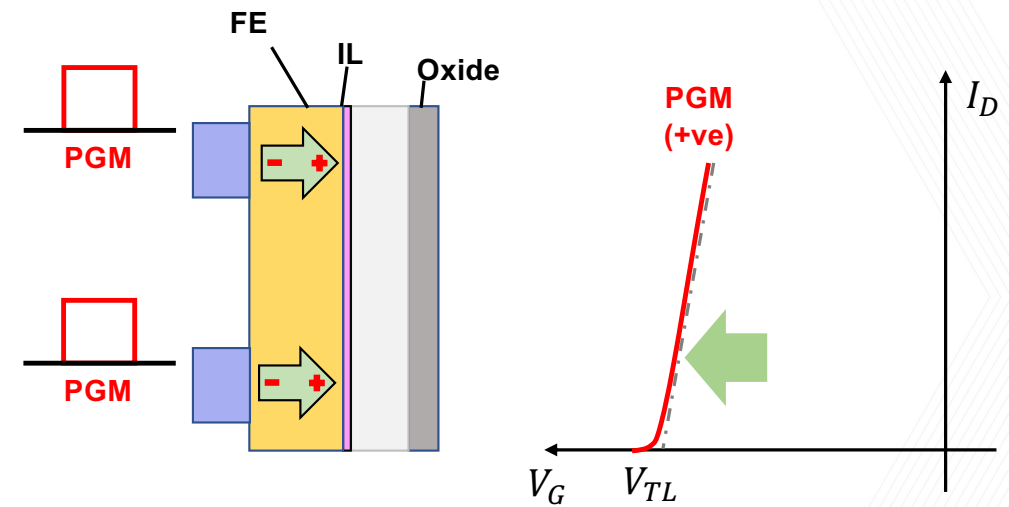
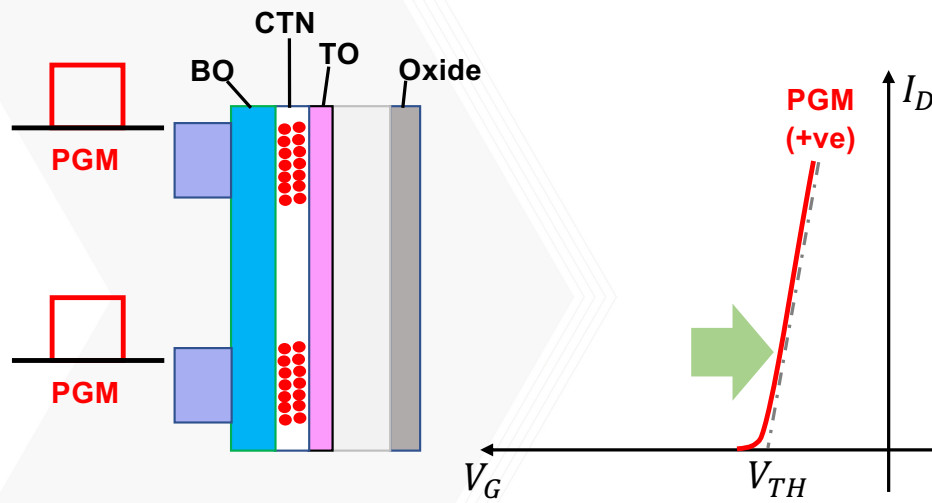
Positive PGM pulse sets the V_t to high V_t state in CTF

CTF vs FEFET (Program)



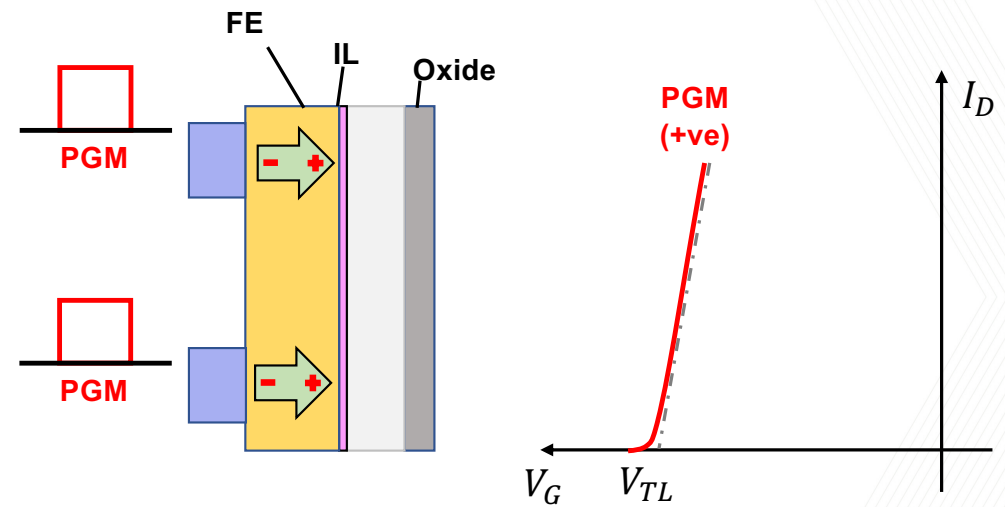
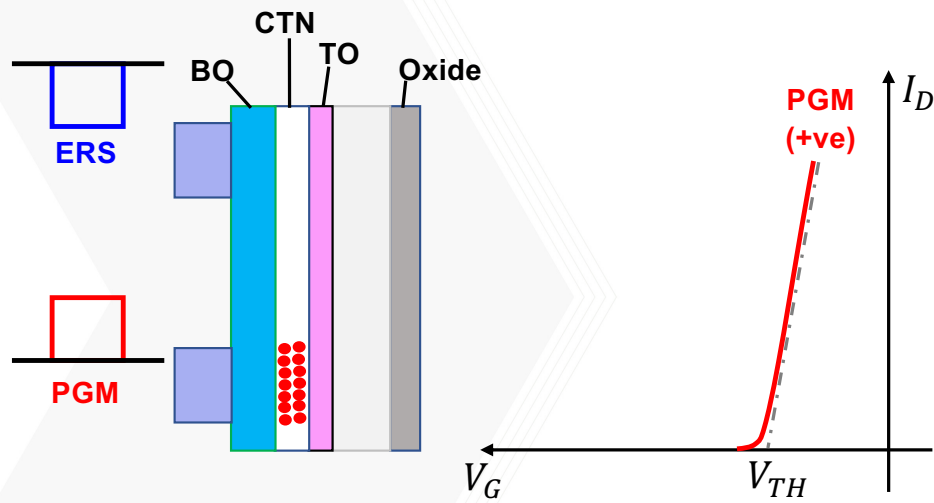
Positive PGM pulse sets the V_t to high V_t state in CTF

CTF vs FEFET (Program)



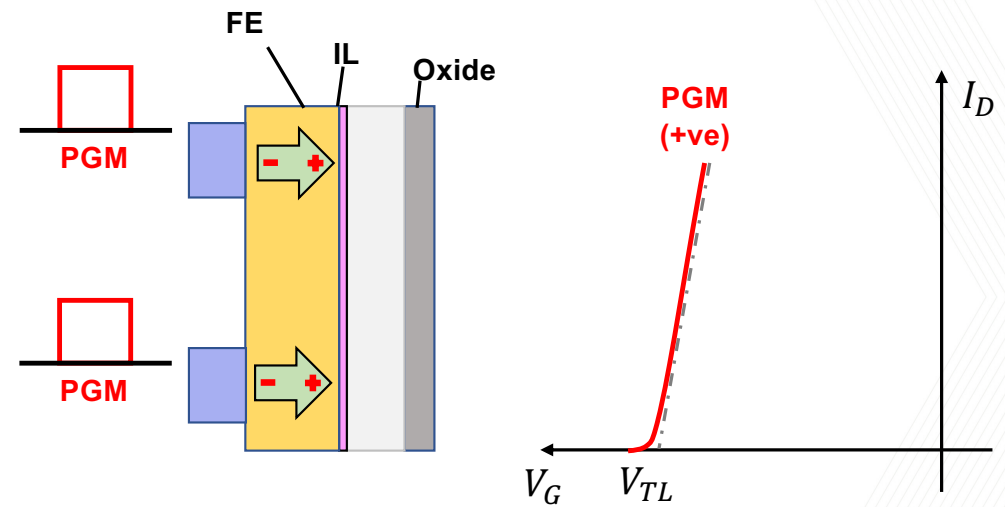
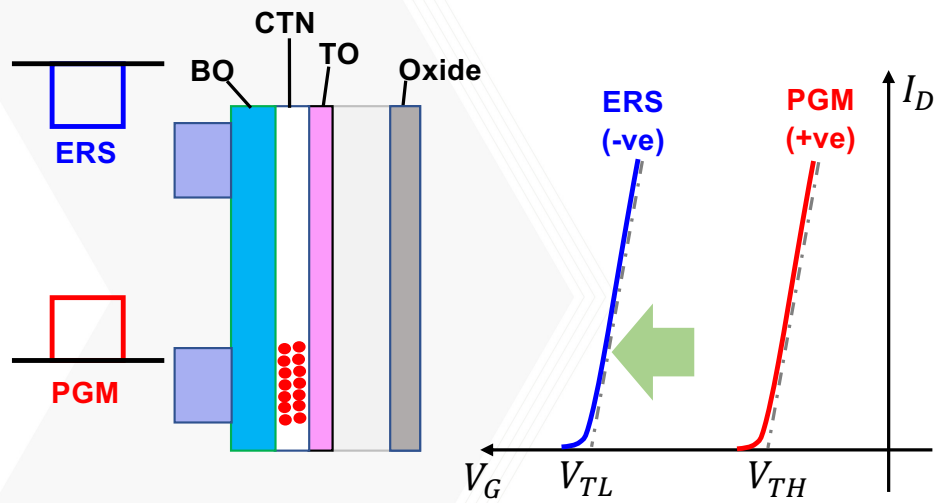
On the contrary, Positive PGM pulse sets the V_t to low V_t state in FEFET

CTF vs FEFET (Erase)



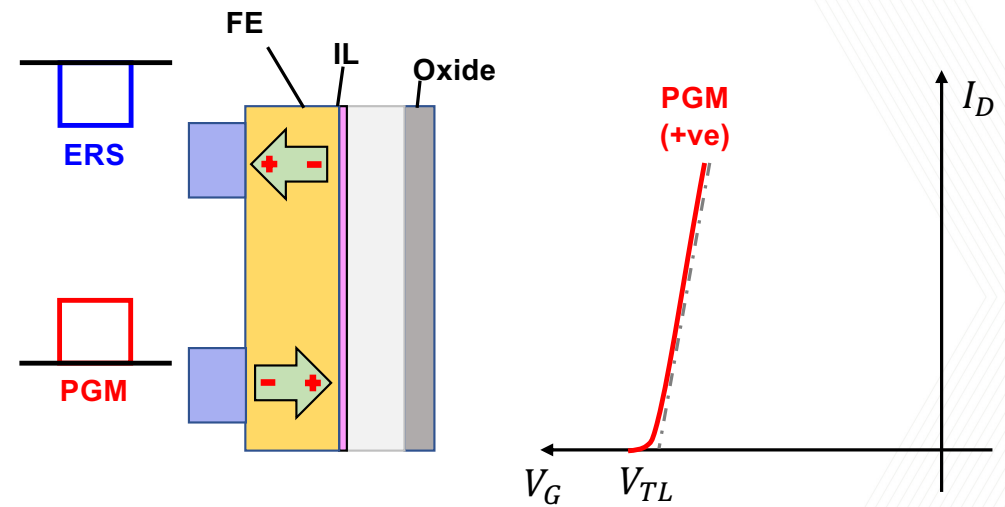
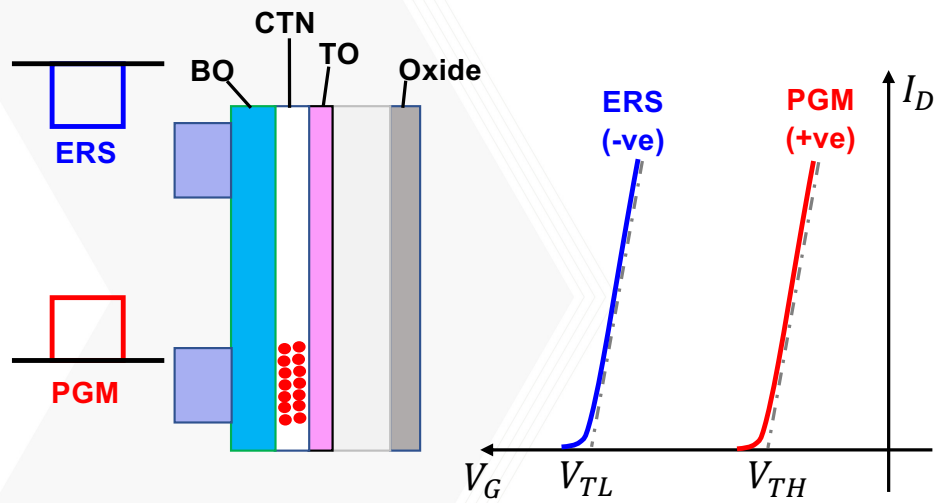
Negative ERS pulse sets the V_t to low V_t state in CTF

CTF vs FEFET (Erase)



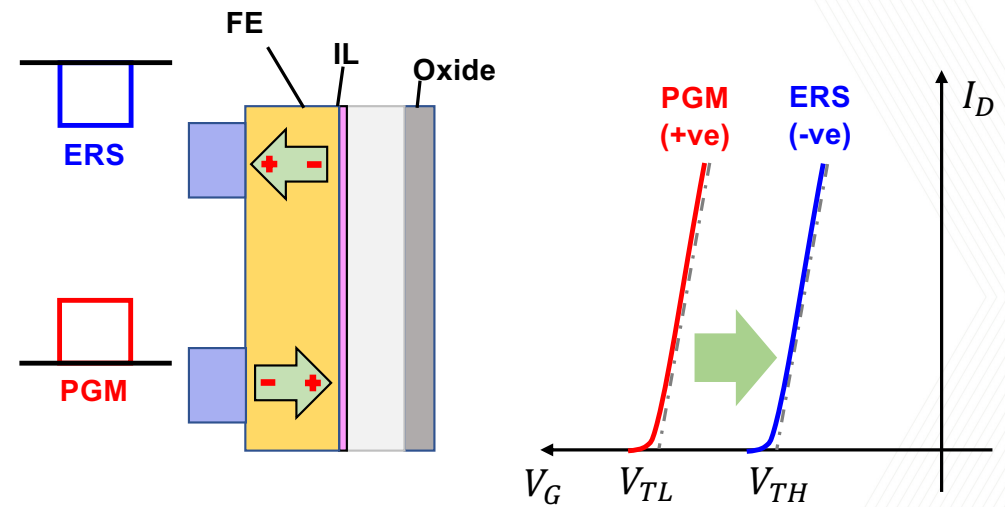
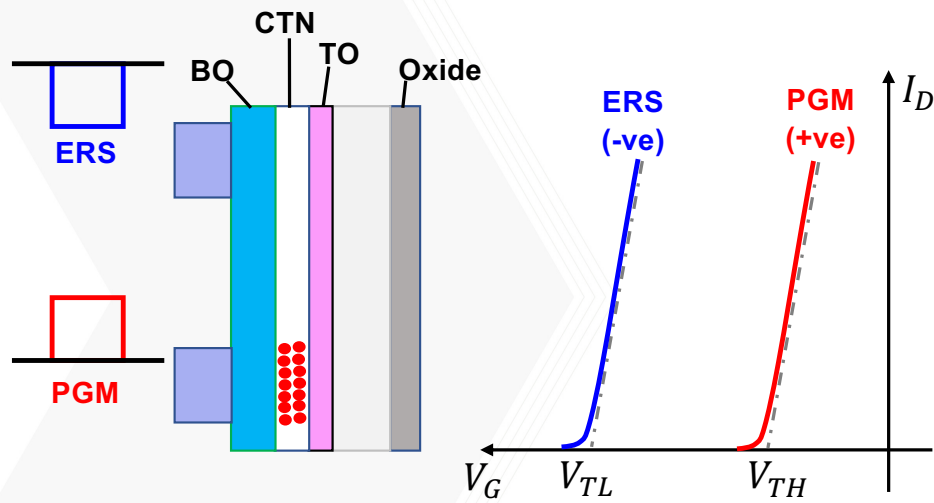
Negative ERS pulse sets the V_t to low V_t state in CTF

CTF vs FEFET (Erase)



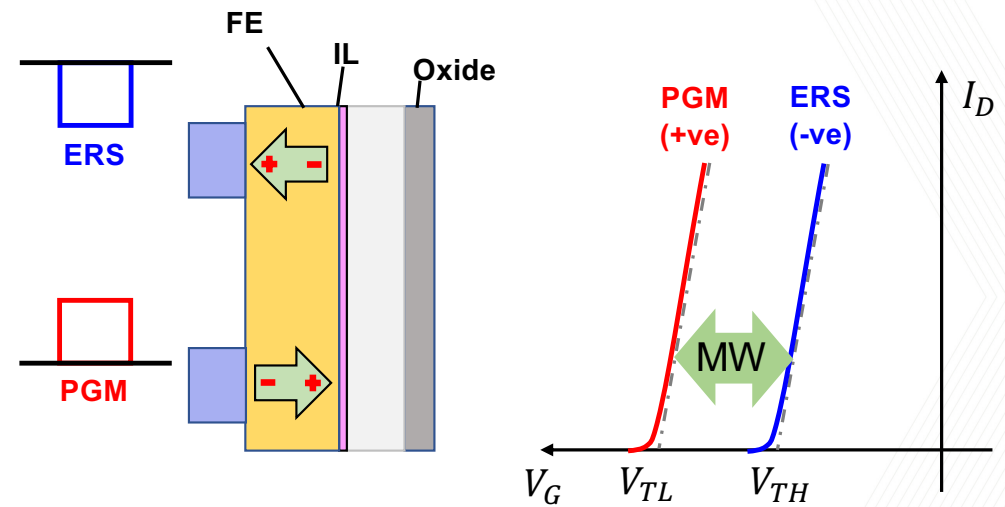
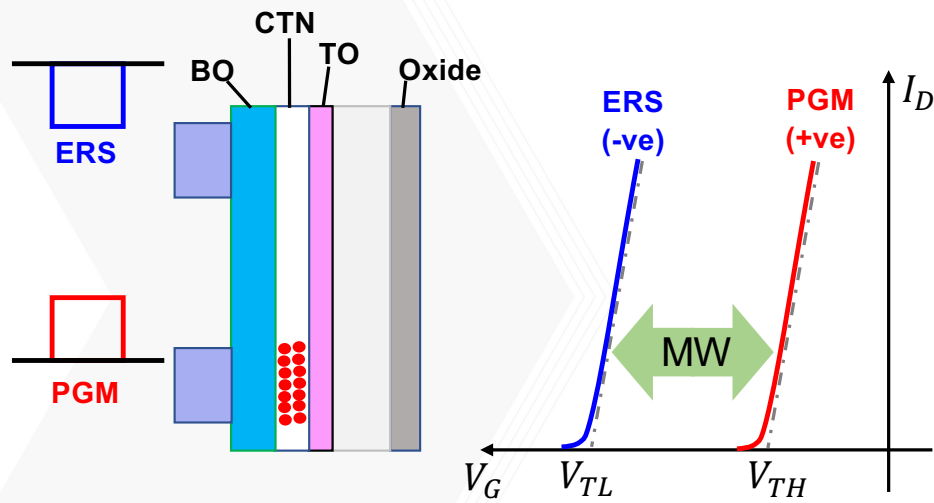
Negative ERS pulse sets the V_t to high V_t state in FEFET

CTF vs FEFET (Erase)



Negative ERS pulse sets the V_t to high V_t state in FEFET

CTF vs FEFET (MW)

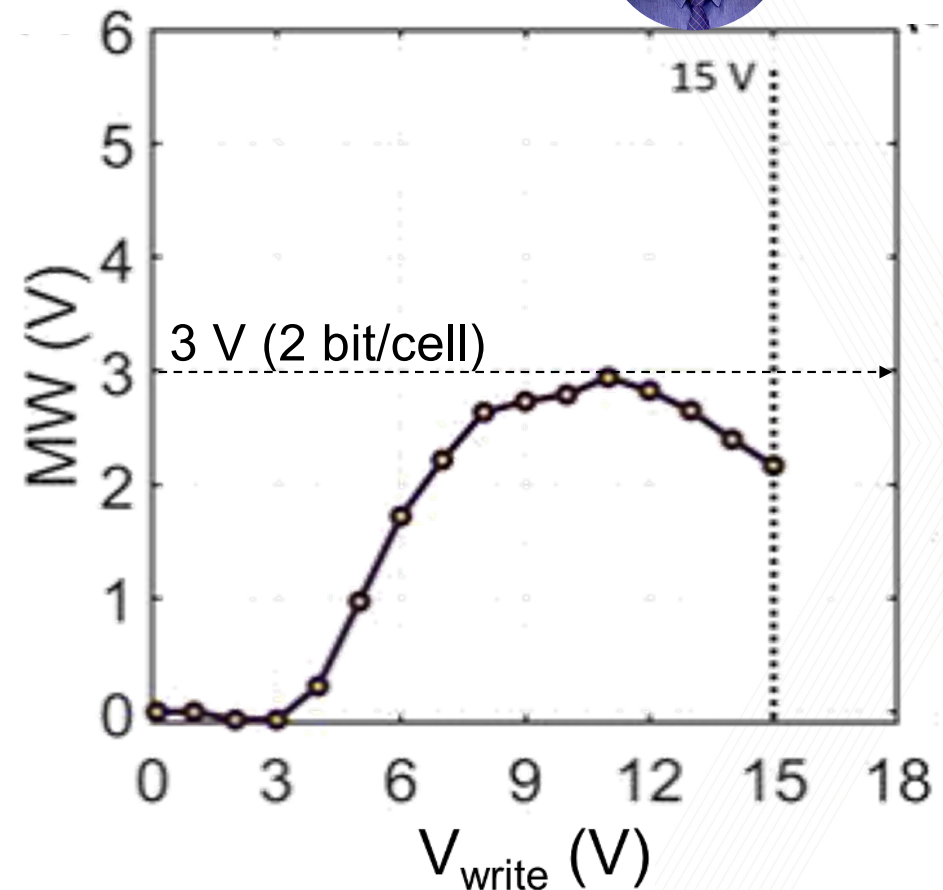
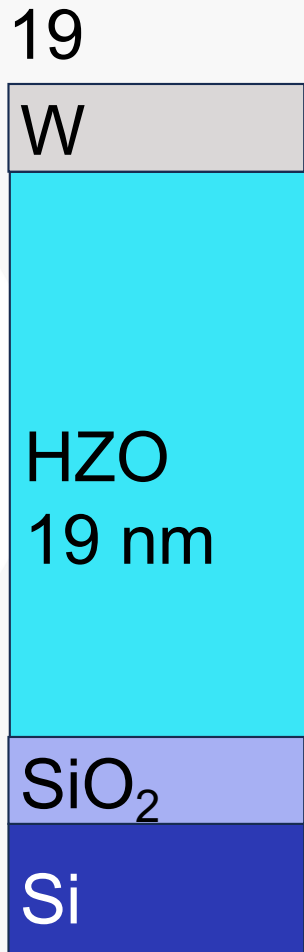


$$MW = V_{TH} - V_{TL}$$

Impact of tunnel dielectric insertion

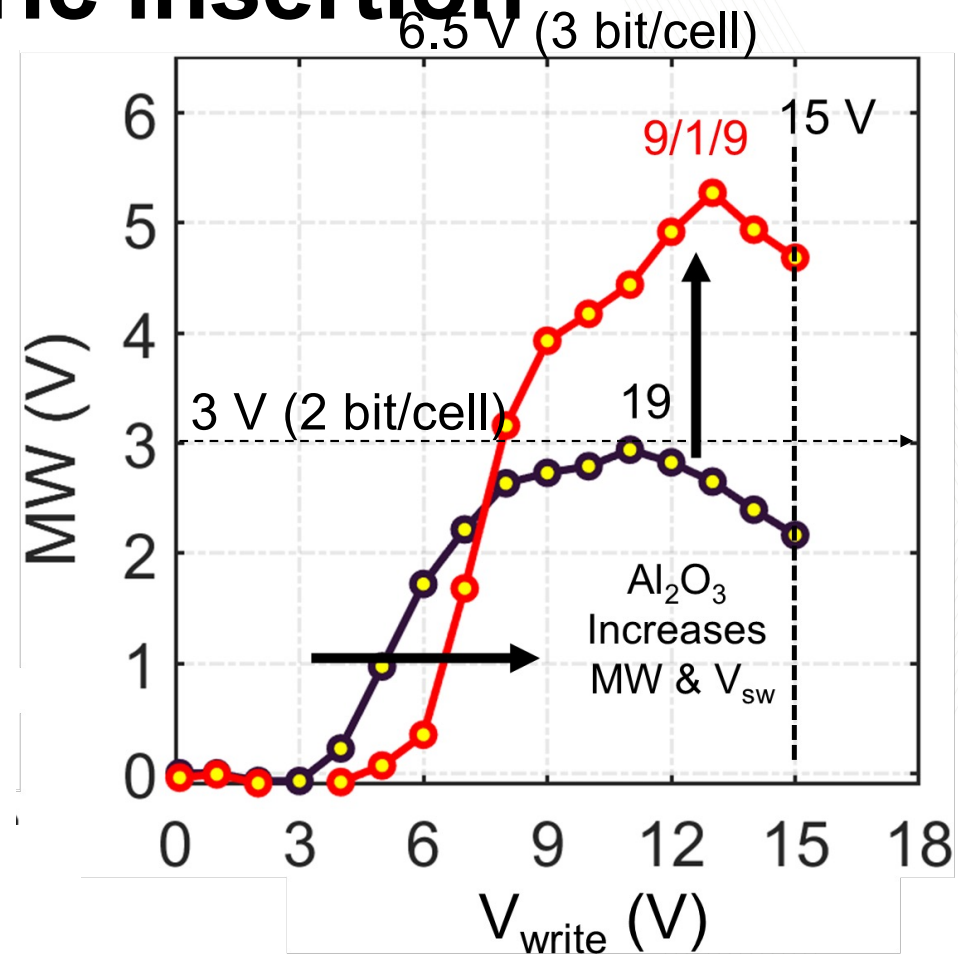
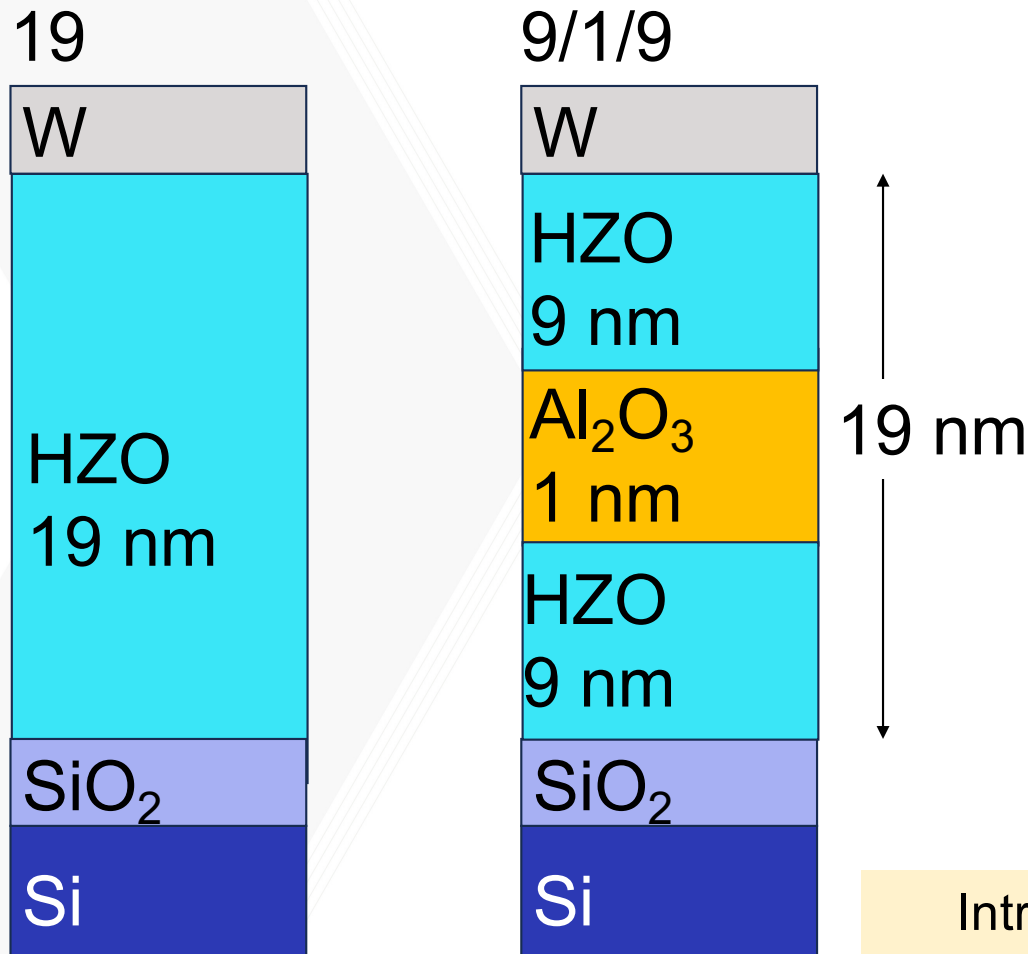


Dr. Dipjyoti Das



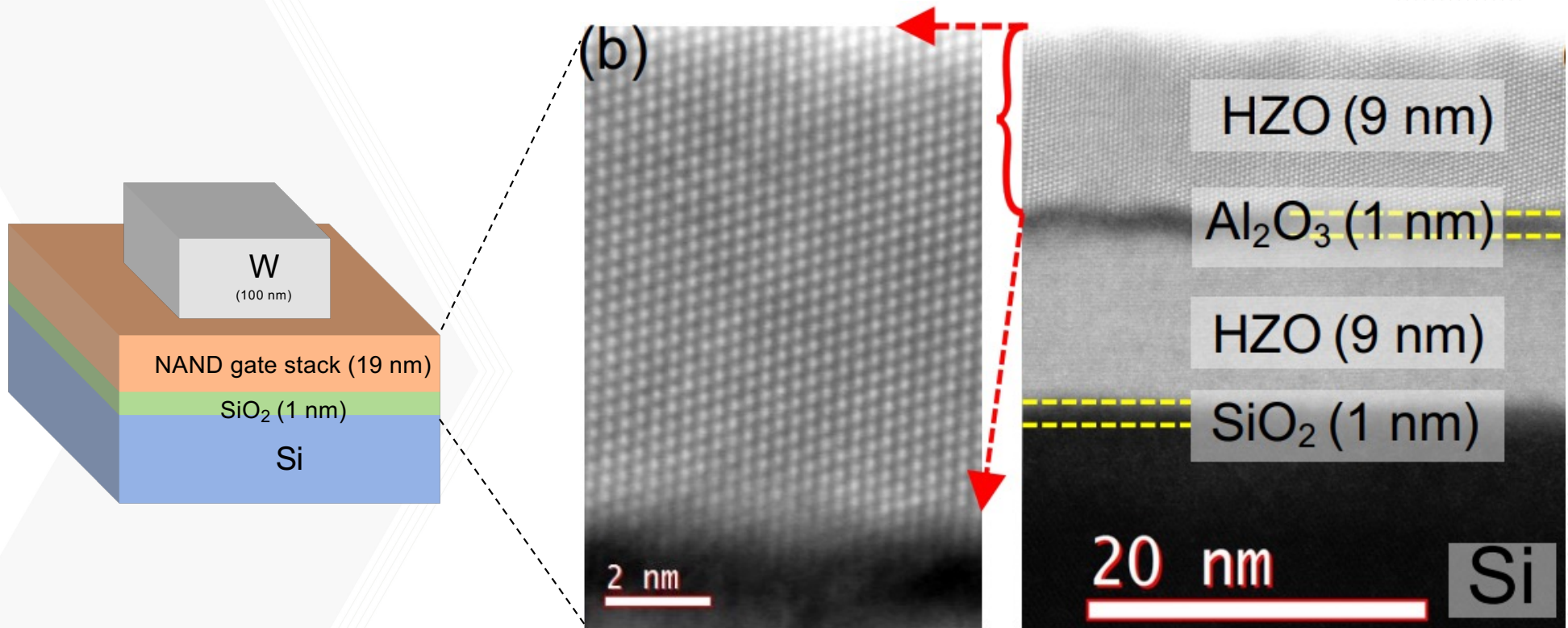
10 nm HZO layer leads to maximum memory window of 2.9 V.

Impact of tunnel dielectric insertion



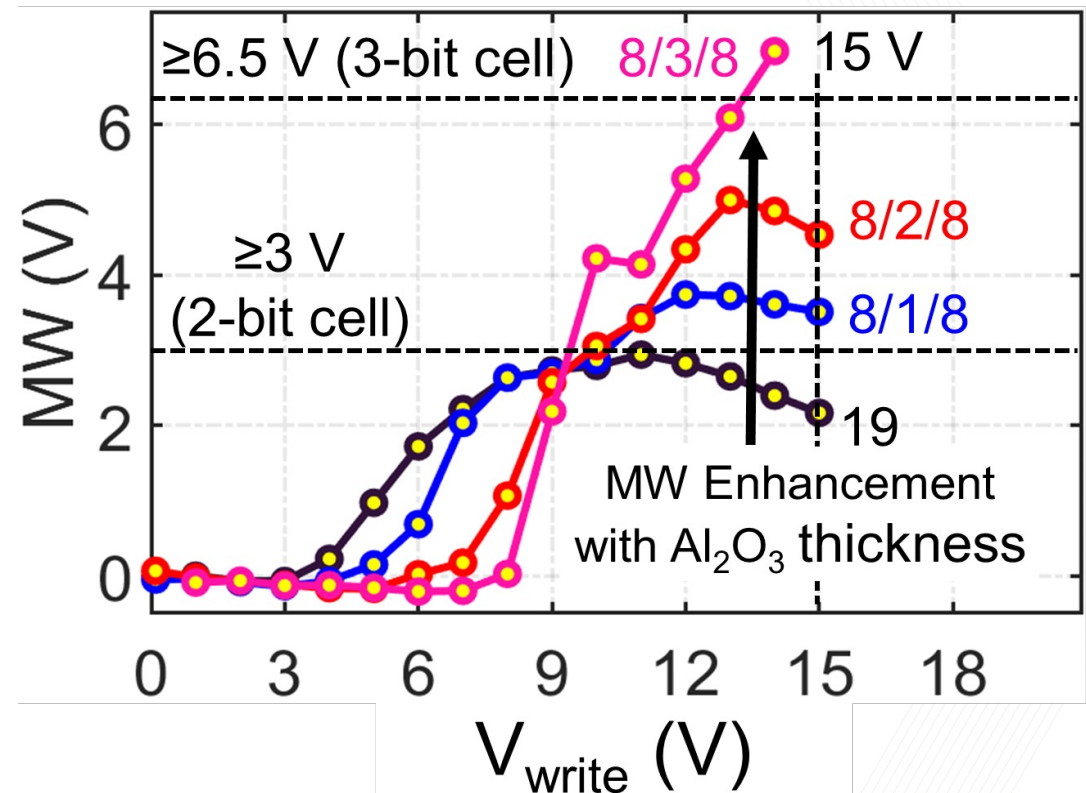
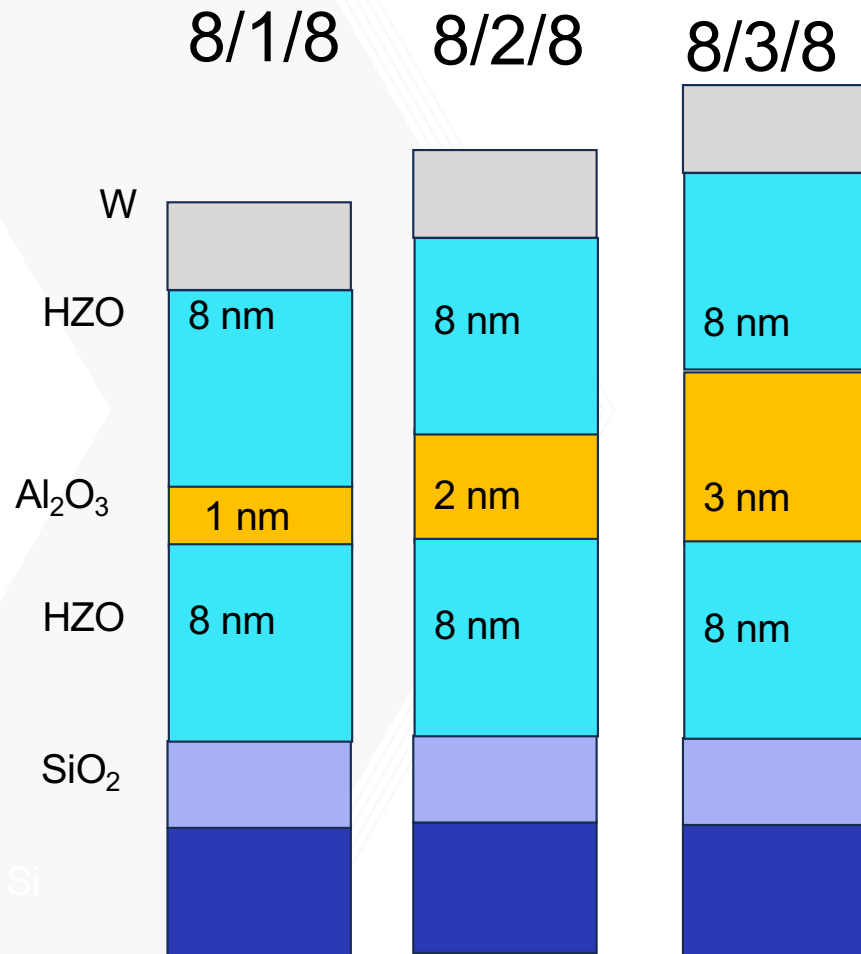
Introducing 1 nm Al₂O₃ intermediate layer dramatically memory window to 5.3 V.

Impact of tunnel dielectric insertion



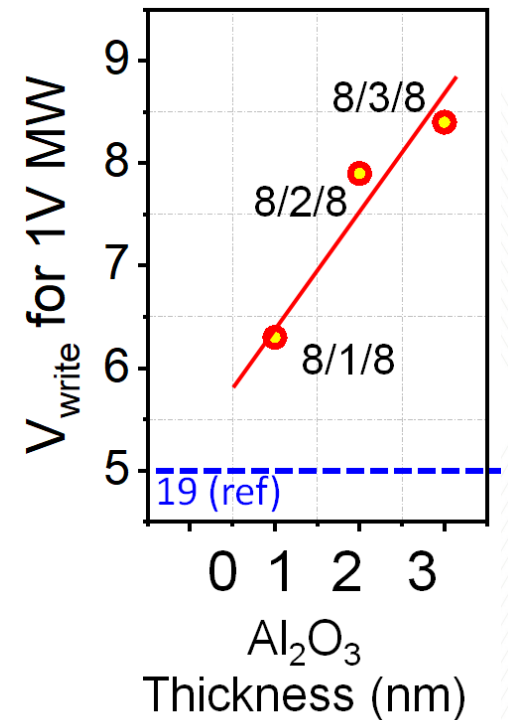
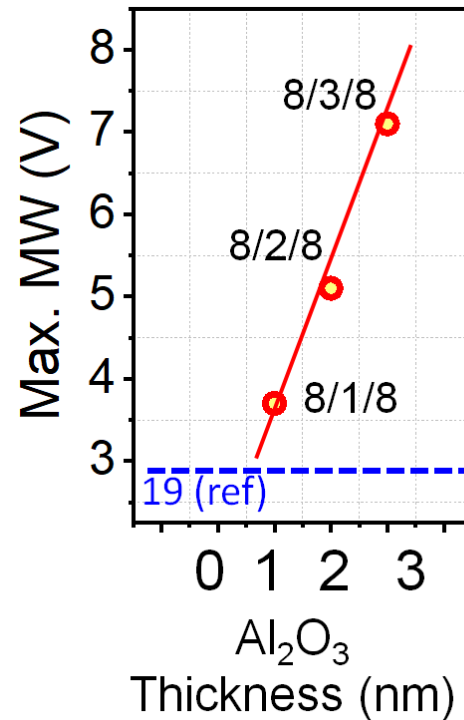
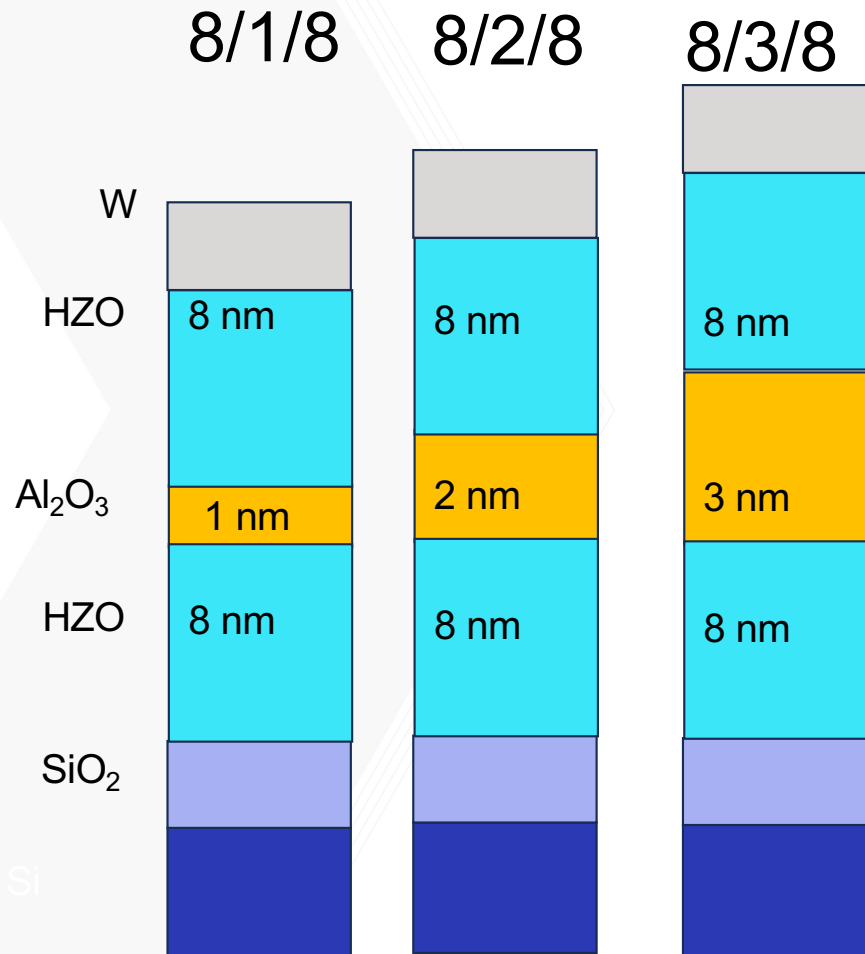
Full coverage of 1 nm Al₂O₃ is observed.

Impact of tunnel dielectric insertion



FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

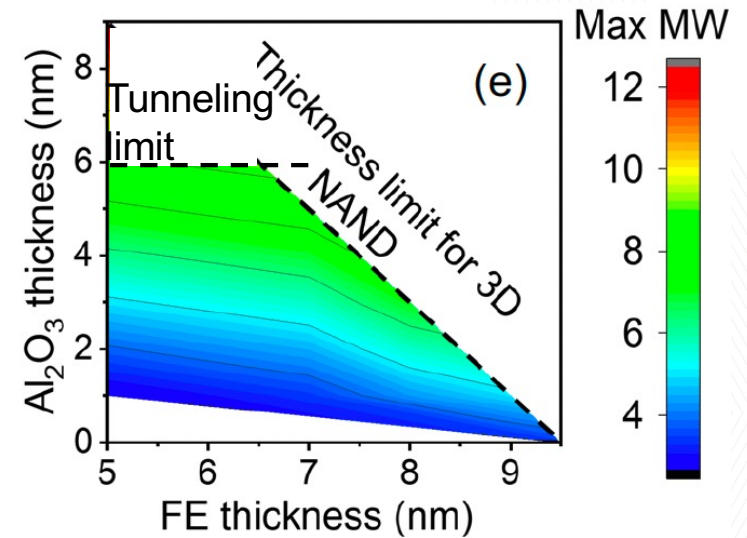
Impact of tunnel dielectric insertion



For a fixed FE layer, increase AIO layer increases the MW while increasing the write voltage <15 V.

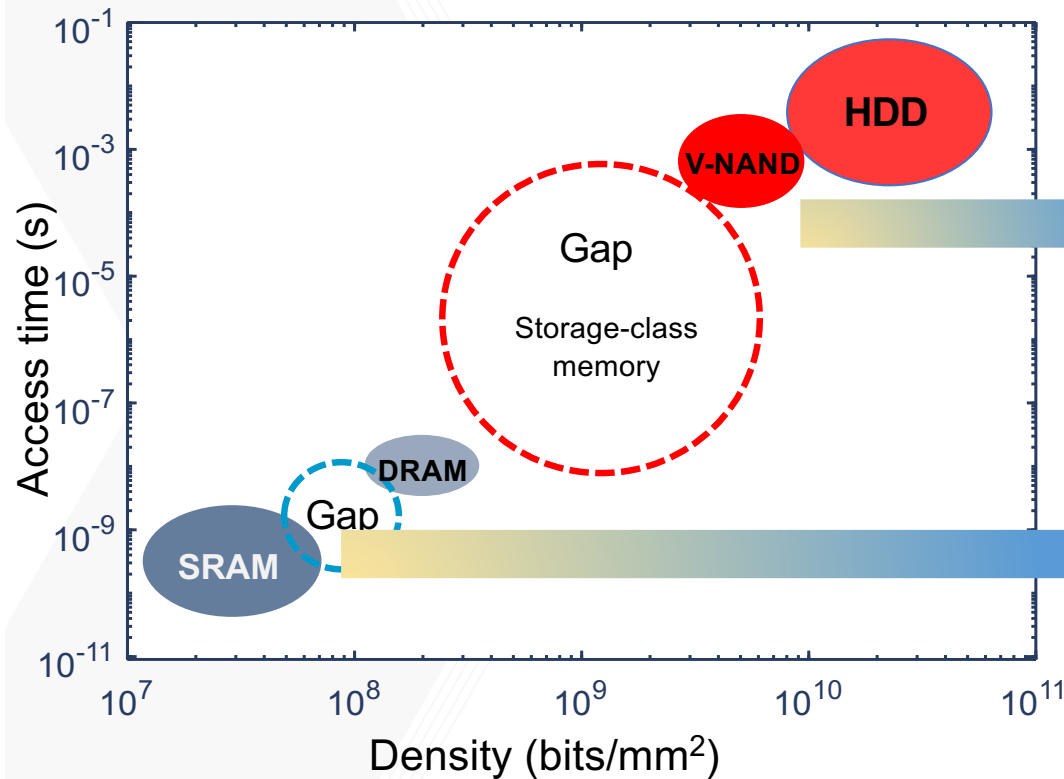
Ferroelectric NAND

- Ferroelectricity presents opportunities for NAND storage technologies.
 - Write voltage reduction and memory window enhancement.
 - Potential for QLC by stack engineering.
 - Vertical scaling towards 1000 layers.
- Further exploration and engineering required for
 - Tunneling mechanism
 - Disturb characteristics and mitigation.



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Ferroelectrics for flash

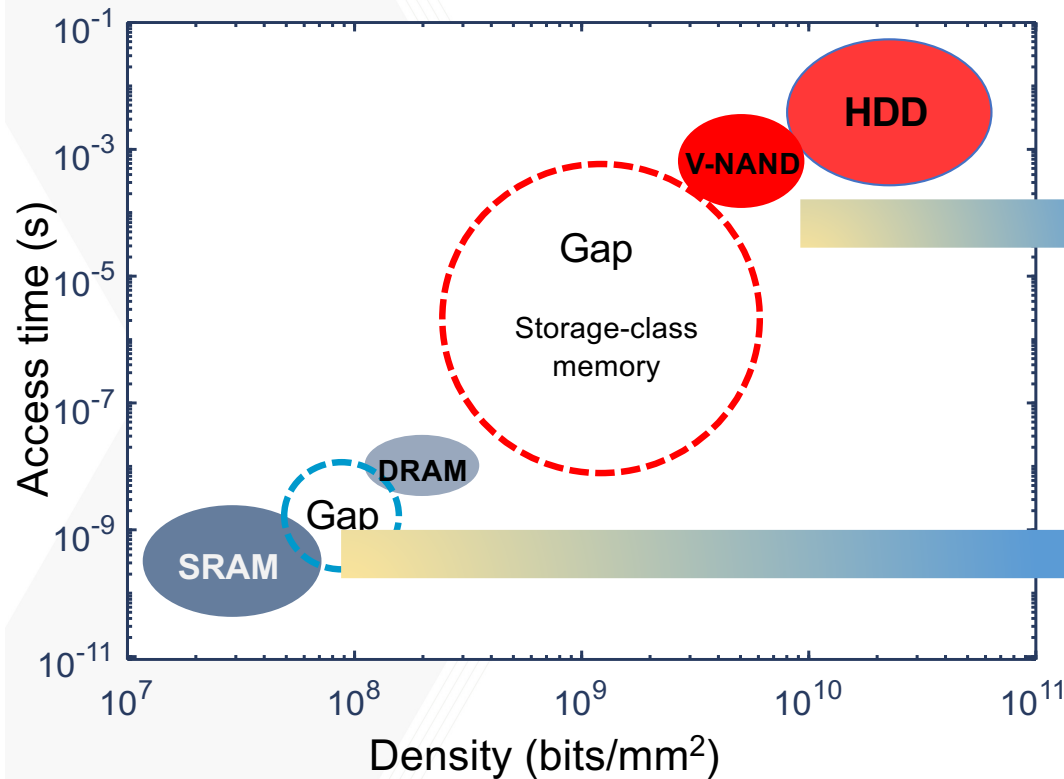


Ferroelectrics for flash?

Ferroelectrics for embedded memories/cache

- Density
- BEOL compatibility
- Fast

Ferroelectrics for flash



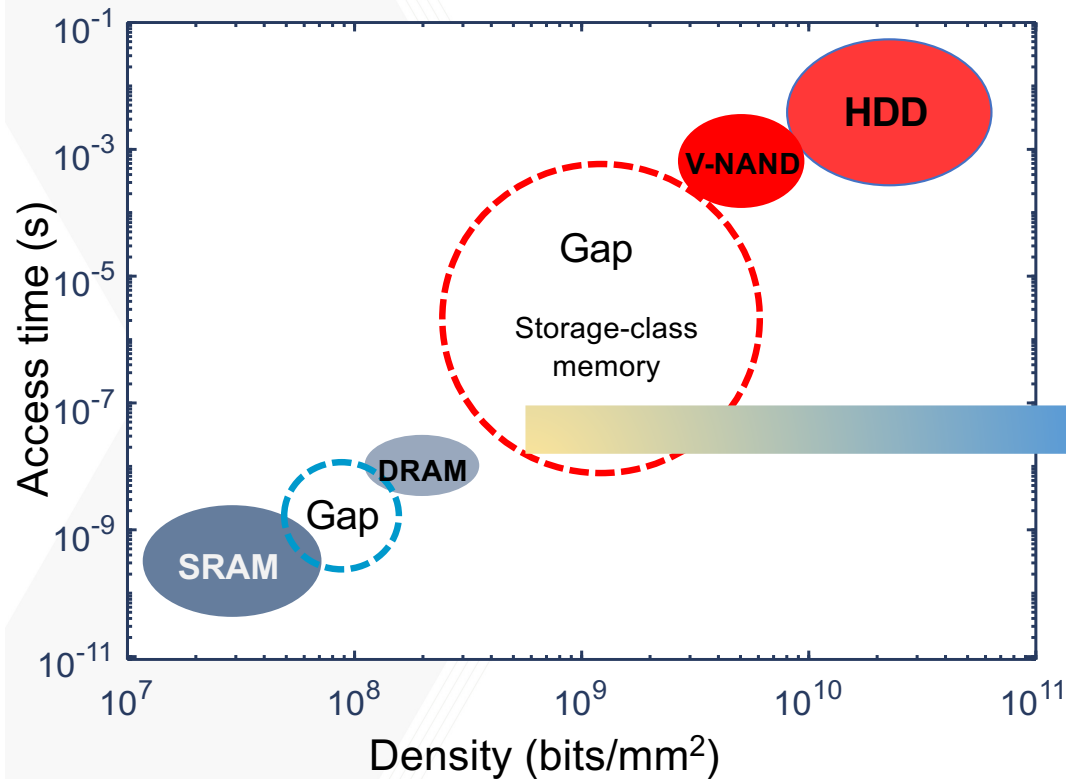
Ferroelectrics for flash

- Voltage scaling below 15 V
- Z-scaling

Ferroelectrics for embedded memories/cache

- Density
- BEOL compatibility
- Fast

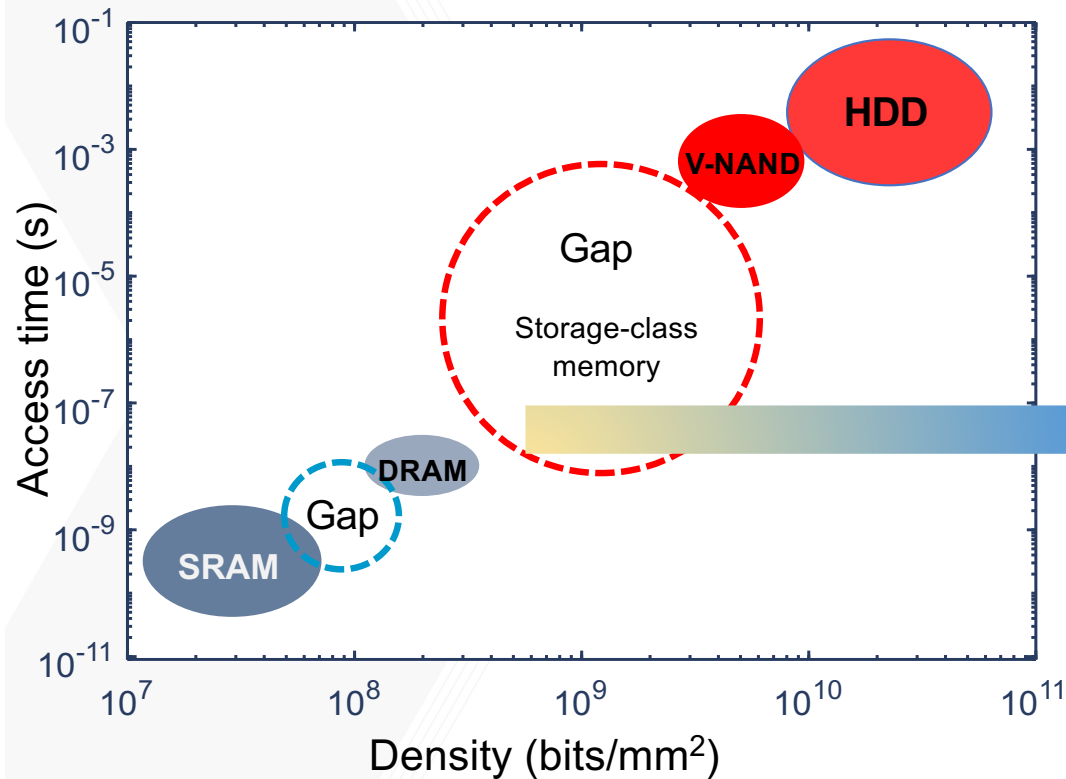
Ferroelectrics for flash



**Ferroelectrics for the
DRAM/Storage class space**

Micron: 32 Gb Dual Layer 3-D stacked FRAM

Ferroelectrics for flash



**Ferroelectrics for the
DRAM/Storage class space?**

2011→2023

APPLIED PHYSICS LETTERS 99, 112904 (2011)

Phase transitions in ferroelectric silicon doped hafnium oxide

T. S. Börske,^{1,2,a,b)} St. Teichert,^{3,b)} D. Bräuhäus,⁴ J. Müller,⁵ U. Schröder,^{2,b)} U. Böttger,⁴ and T. Mikolajick^{2,6}

¹Löberwallgraben 2, 99096 Erfurt, Germany

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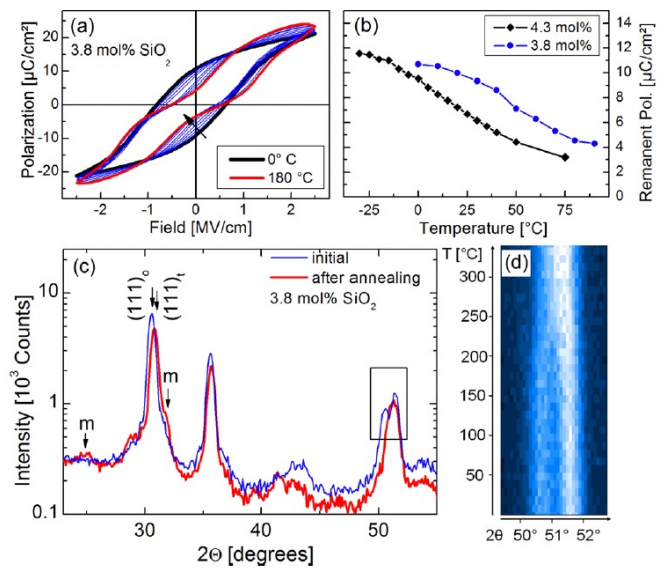
³UAS Jena, Department of SciTec, 07745 Jena, Germany

⁴RWTH Aachen, Institut für Werkstoffe der Elektrotechnik, 52062 Aachen, Germany

⁵Fraunhofer Center Nanoelectronic Technologies (CNT), 01099 Dresden, Germany

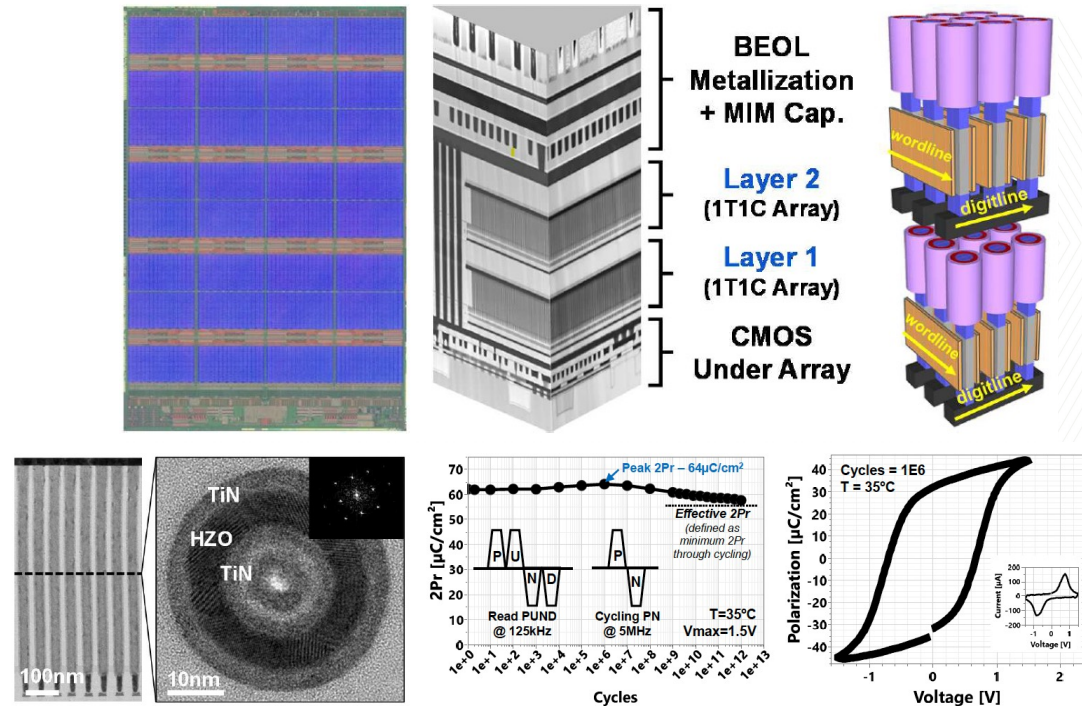
⁶Department of Nanoelectronic Materials, University of Technology Dresden, 01062 Dresden, Germany

(Received 18 July 2011; accepted 19 August 2011; published online 15 September 2011)



NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads

N. Ramaswamy, A. Calderoni, J. Zahurak, G. Servalli, A. Chavan, S. Chhajed, M. Balakrishnan, M. Fischer, M. Hollander, D. P. Ettisserry, A. Liao, K. Karda, M. Jerry, M. Mariani, A. Visconti, B. R. Cook, B. D. Cook, D. Mills, A. Torsi, C. Mouli, E. Byers, M. Helm, S. Pawlowski, S. Shiratake, and N. Chandrasekaran
Micron Technology Inc., Boise, USA, email: dramaswamy@micron.com



Georgia
Tech
CREATING THE NEXT

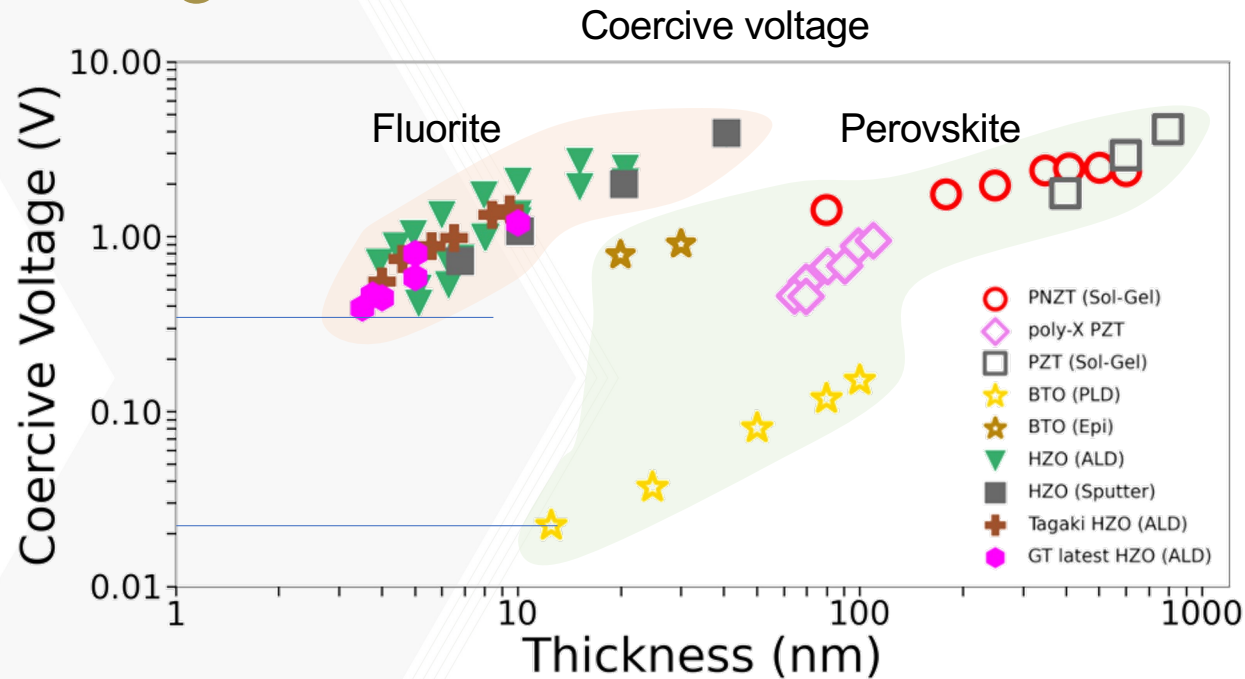
“
We learned that if you think you can do
something,
you may very well be able to do
one thousand times better once you
understand what’s going on.
”

John Mayo
Former President, Bell Labs



What are the fundamental challenges to address?

Challenge #1 - Ferroelectrics require rather too a high voltage and are slower

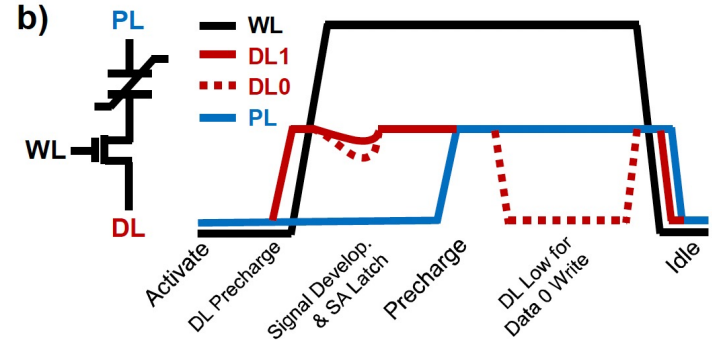


Switching speed

a)

Timing	LPDDR5	NVDRAM
tRC	60ns	185ns
tRCD	18ns	85ns
tWR	34ns	10ns
tRP	18ns	80ns
tAA	22ns	26ns

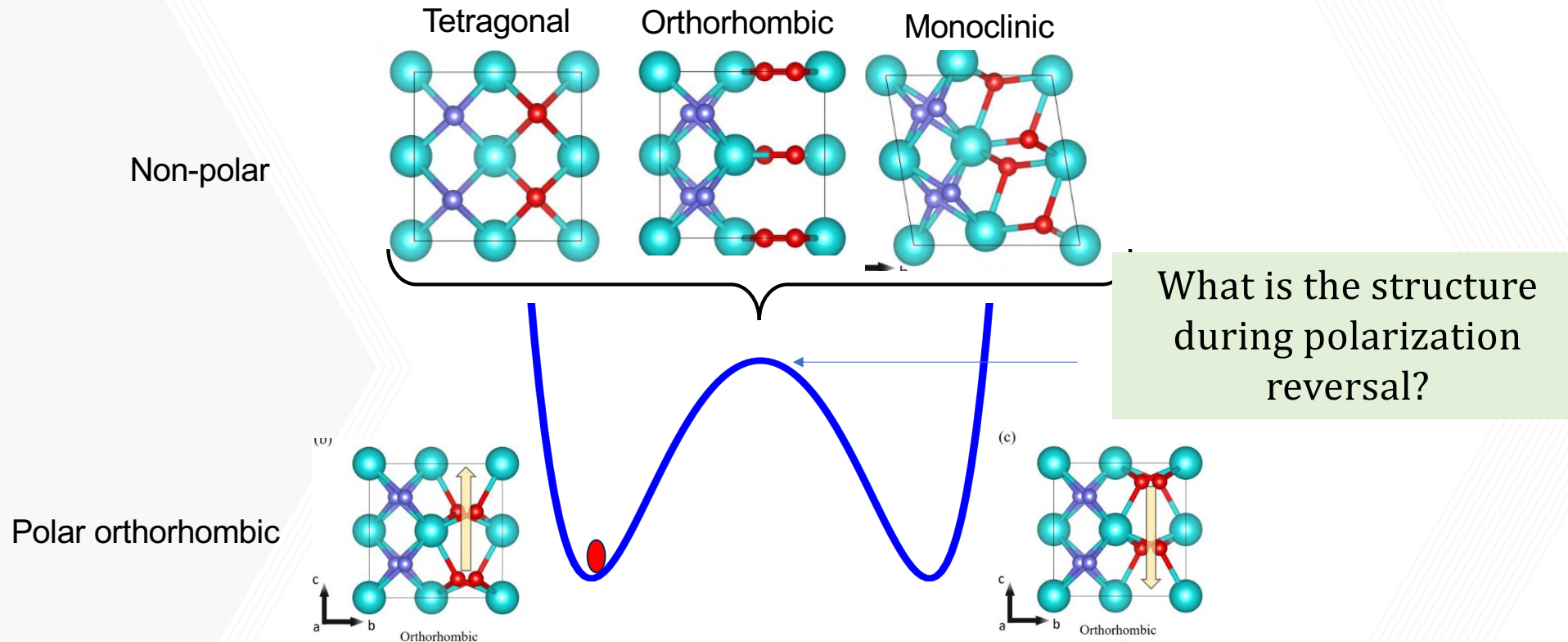
b)



Ramaswamy et al. IEDM 2023

Understanding the switching mechanism may lead to techniques to reduce write voltage and switching delay.

Switching pathway

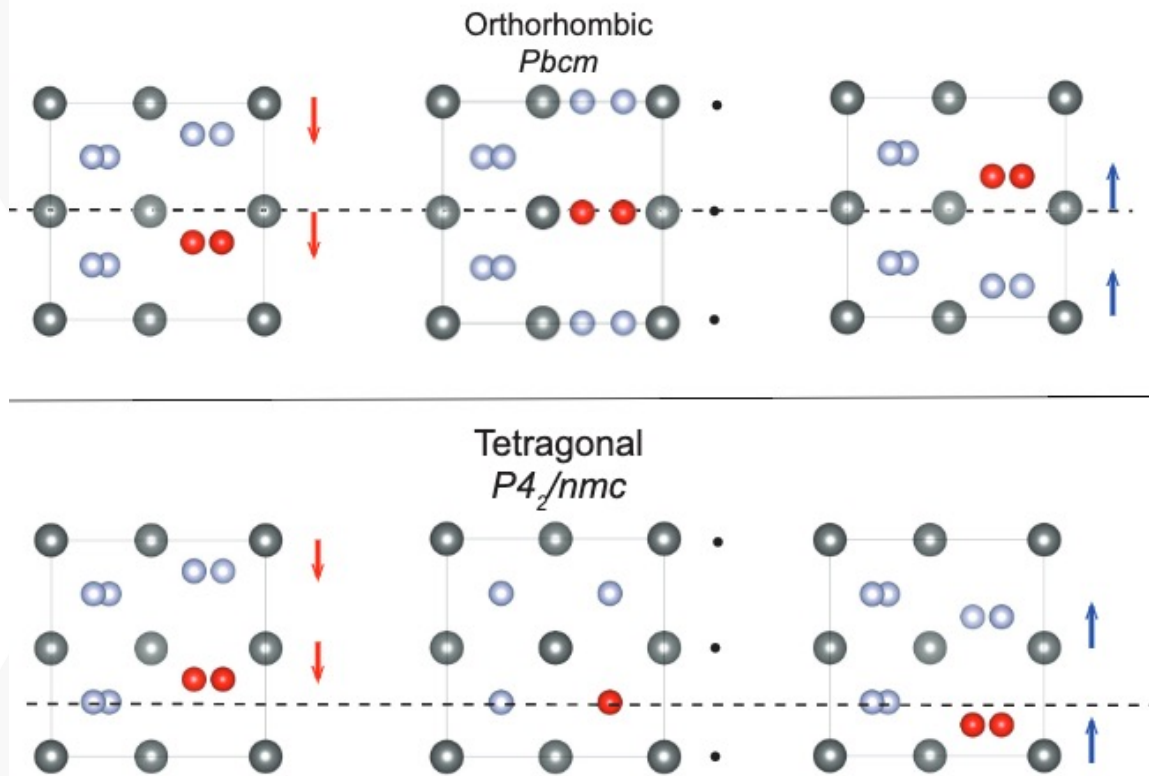


Understanding the switching mechanism may lead to techniques to reduce write voltage and switching delay.

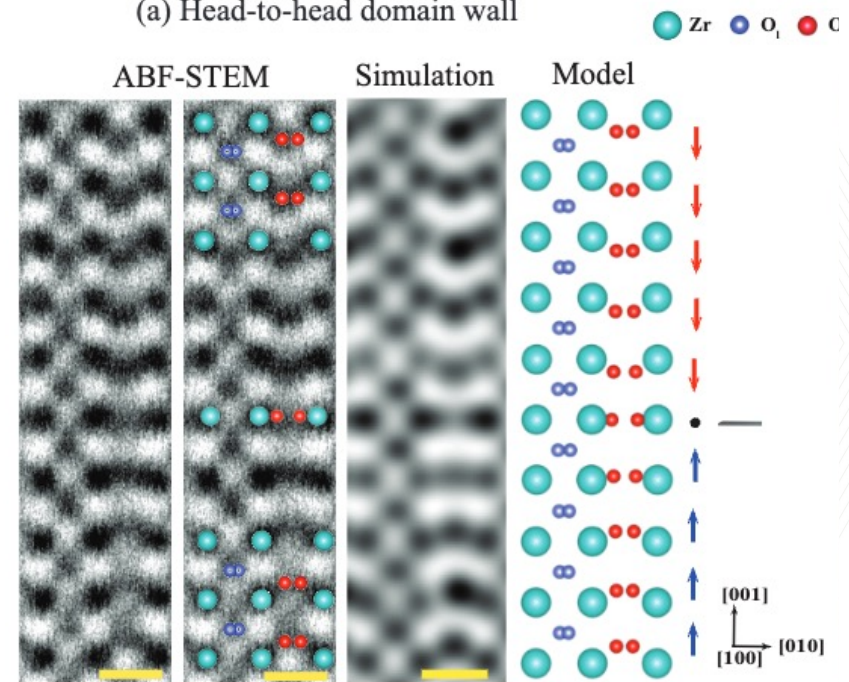
Switching pathway



Nashrah
Afroze

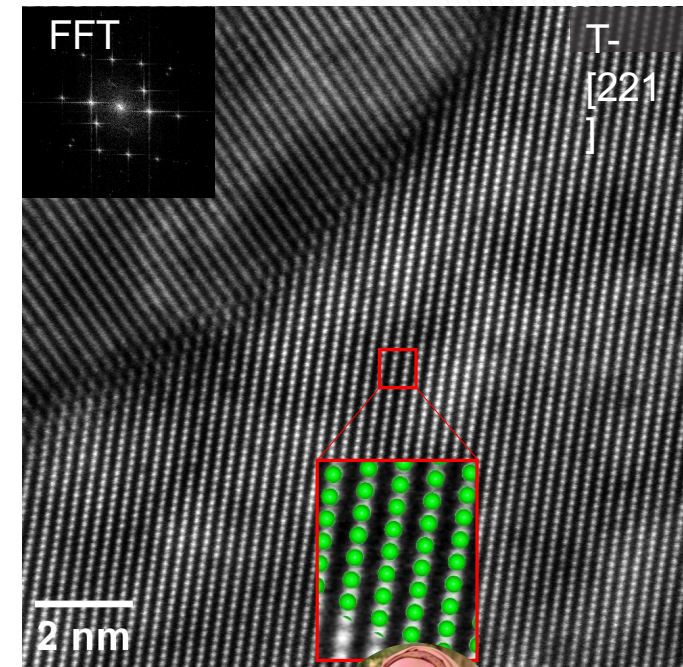
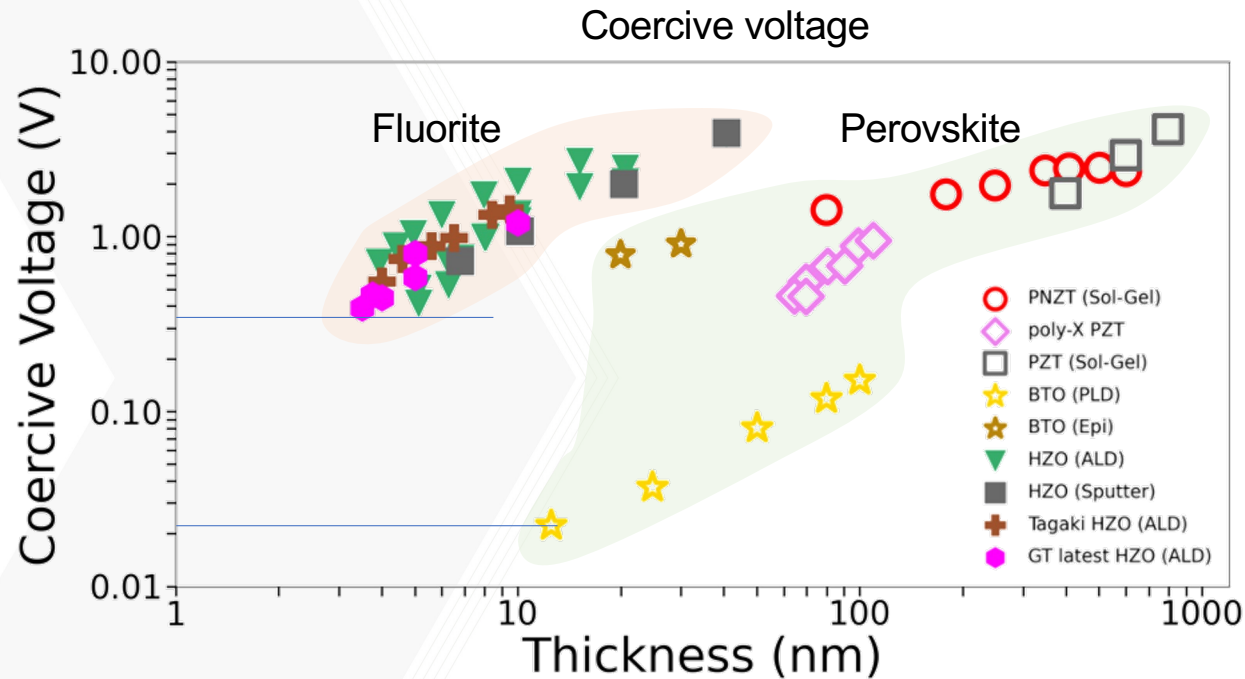


(a) Head-to-head domain wall



What is the structure during polarization reversal?

Challenge #2 - Scaling limit limited by grain boundaries and direct tunneling?

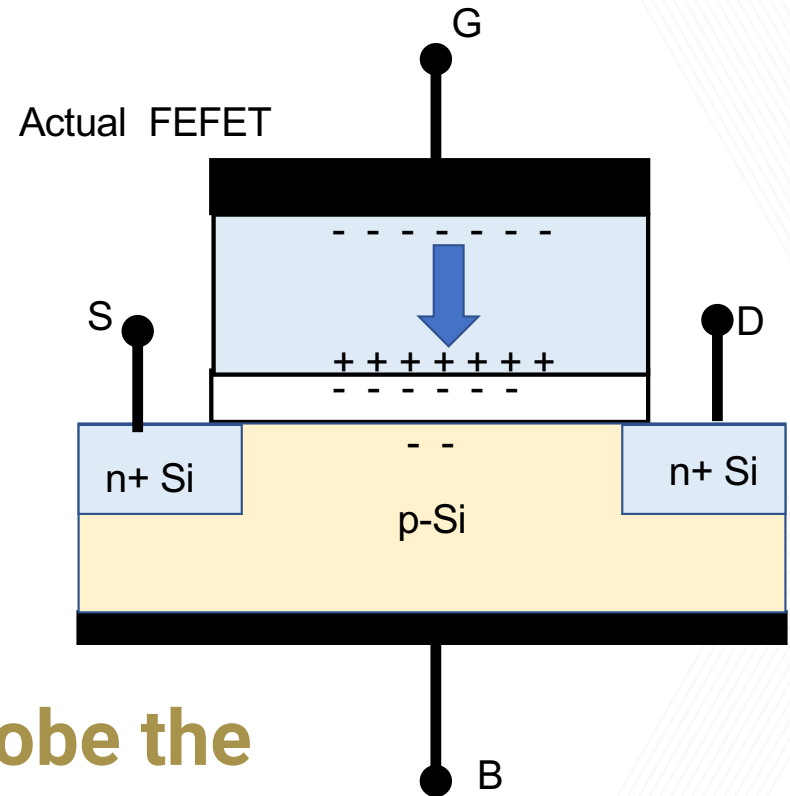
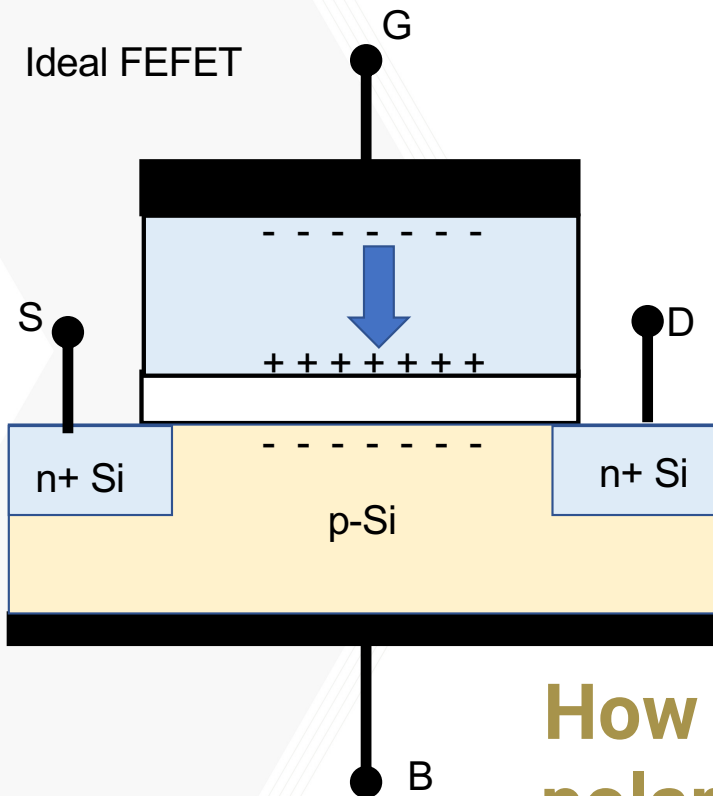


Nashrah
Afroze

78

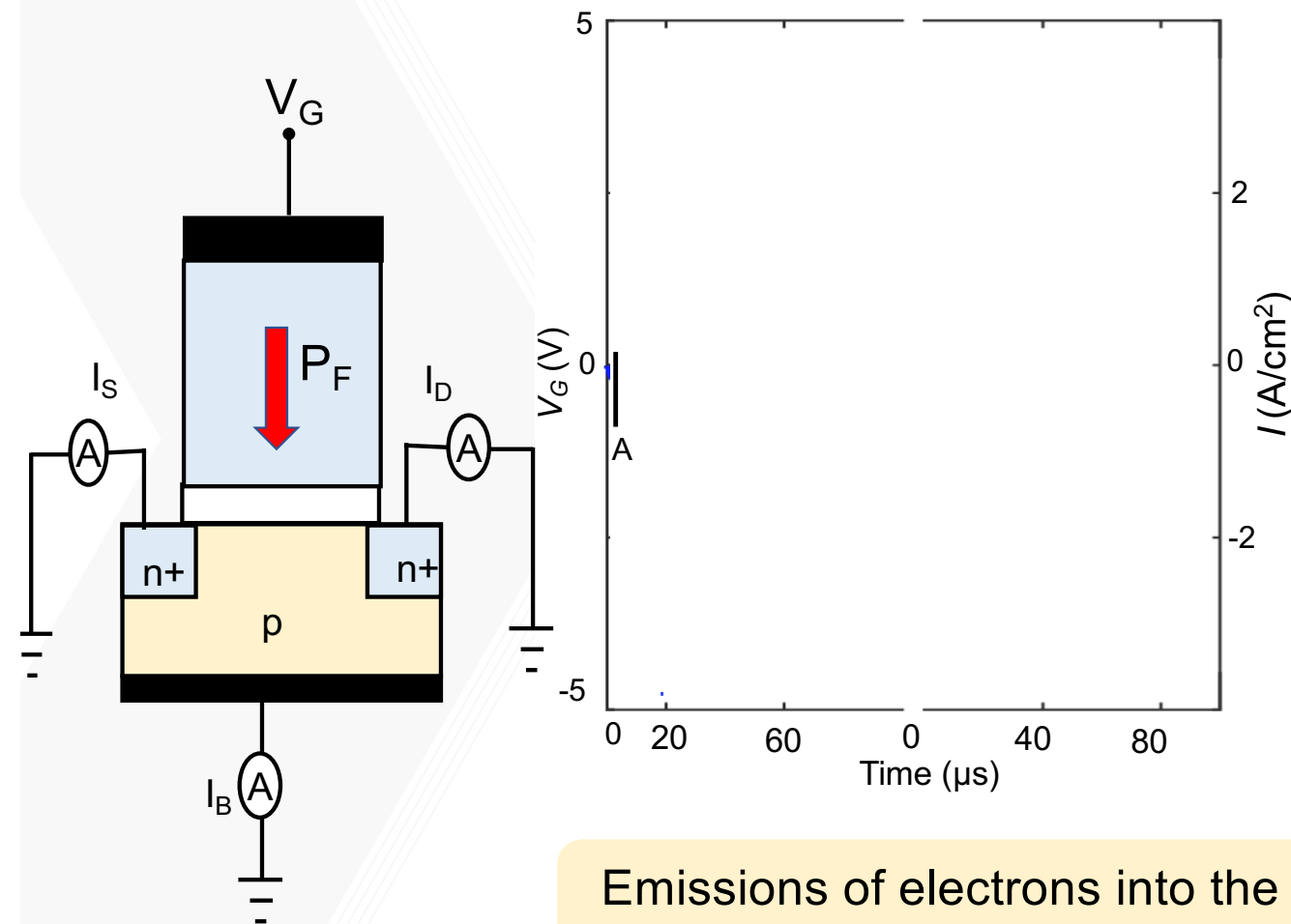
What role do the grain boundaries play in leakage and reliability?

Challenge #3: Interface traps are essential for polarization switching.



How can we probe the polarization screening dynamics?

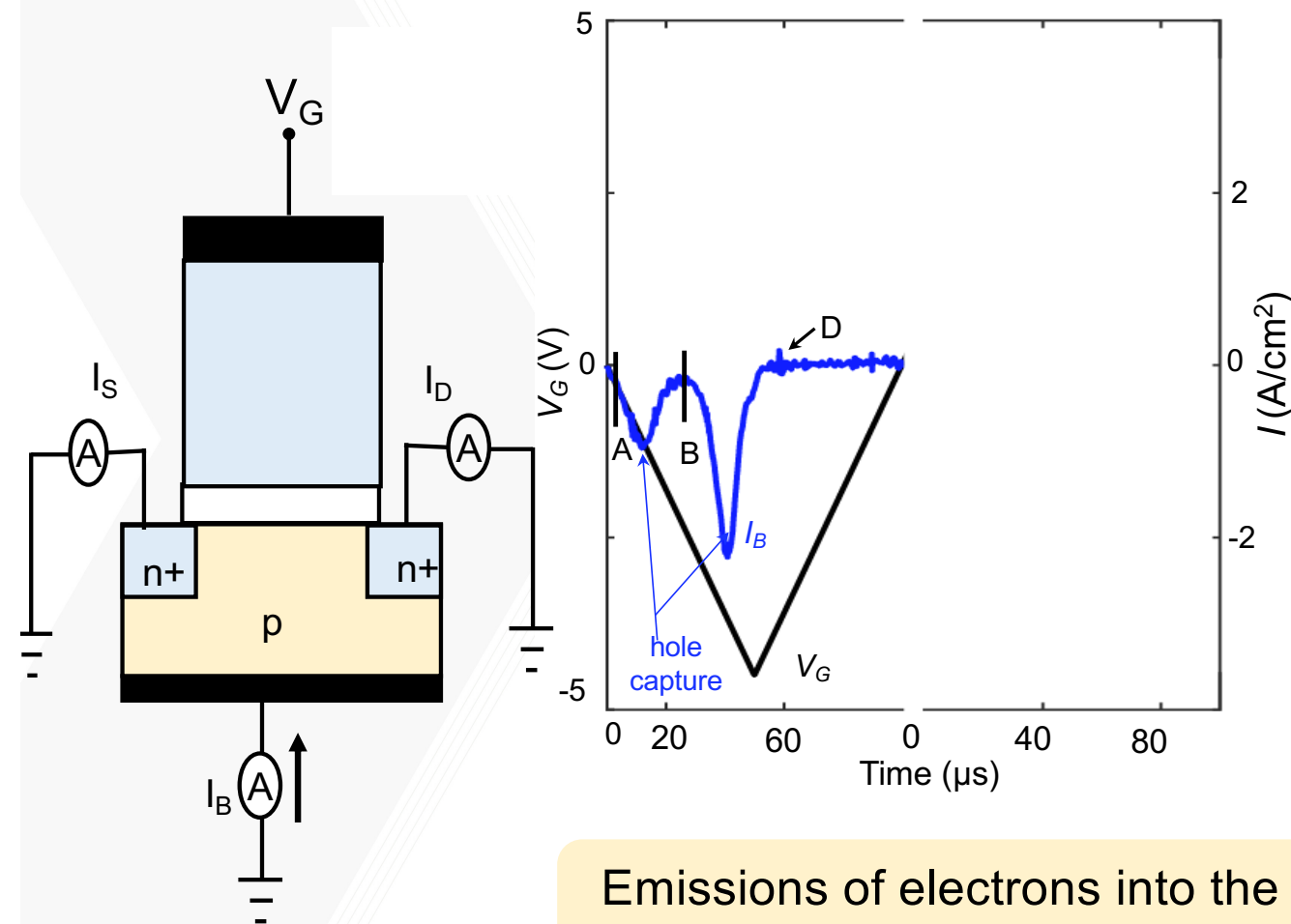
Trap Emission and Capture During Write



Emissions of electrons into the S/D during hole accumulation.

Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2021.

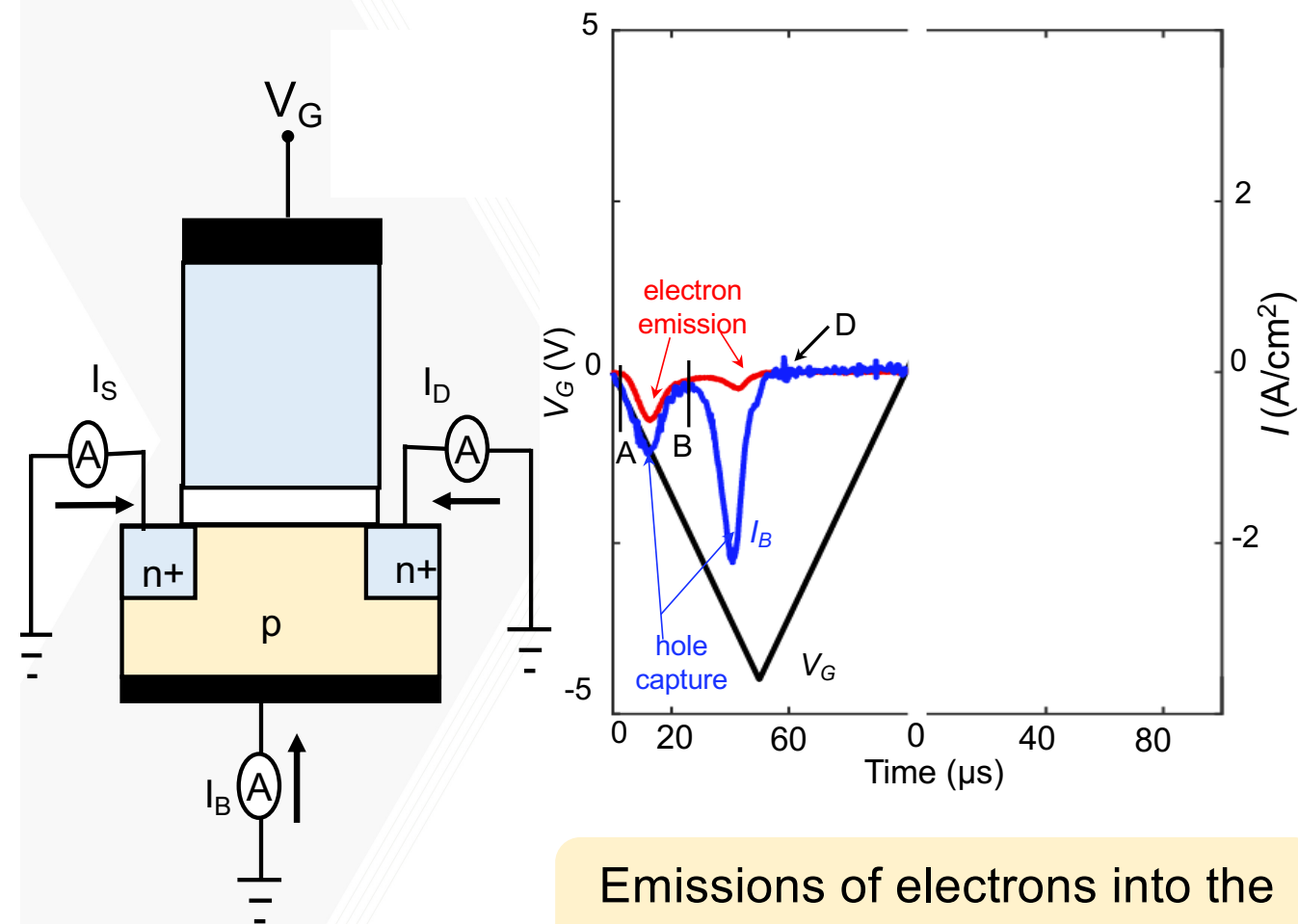
Trap Emission and Capture During Write



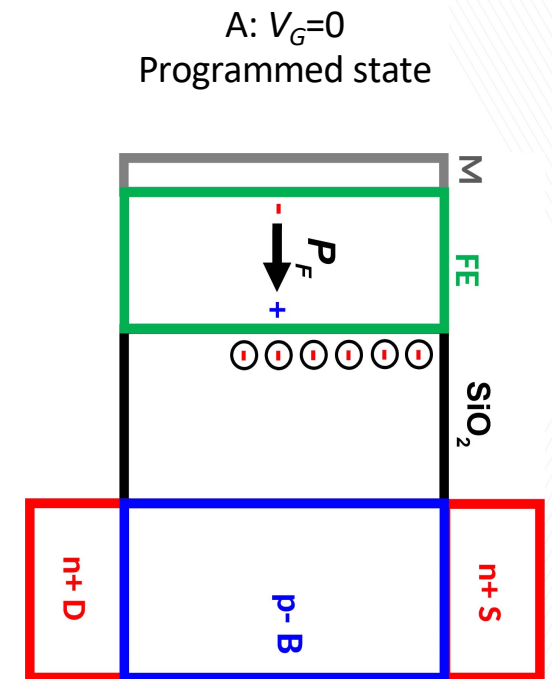
Emissions of electrons into the S/D during hole accumulation.

Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2021.

Trap Emission and Capture During Write

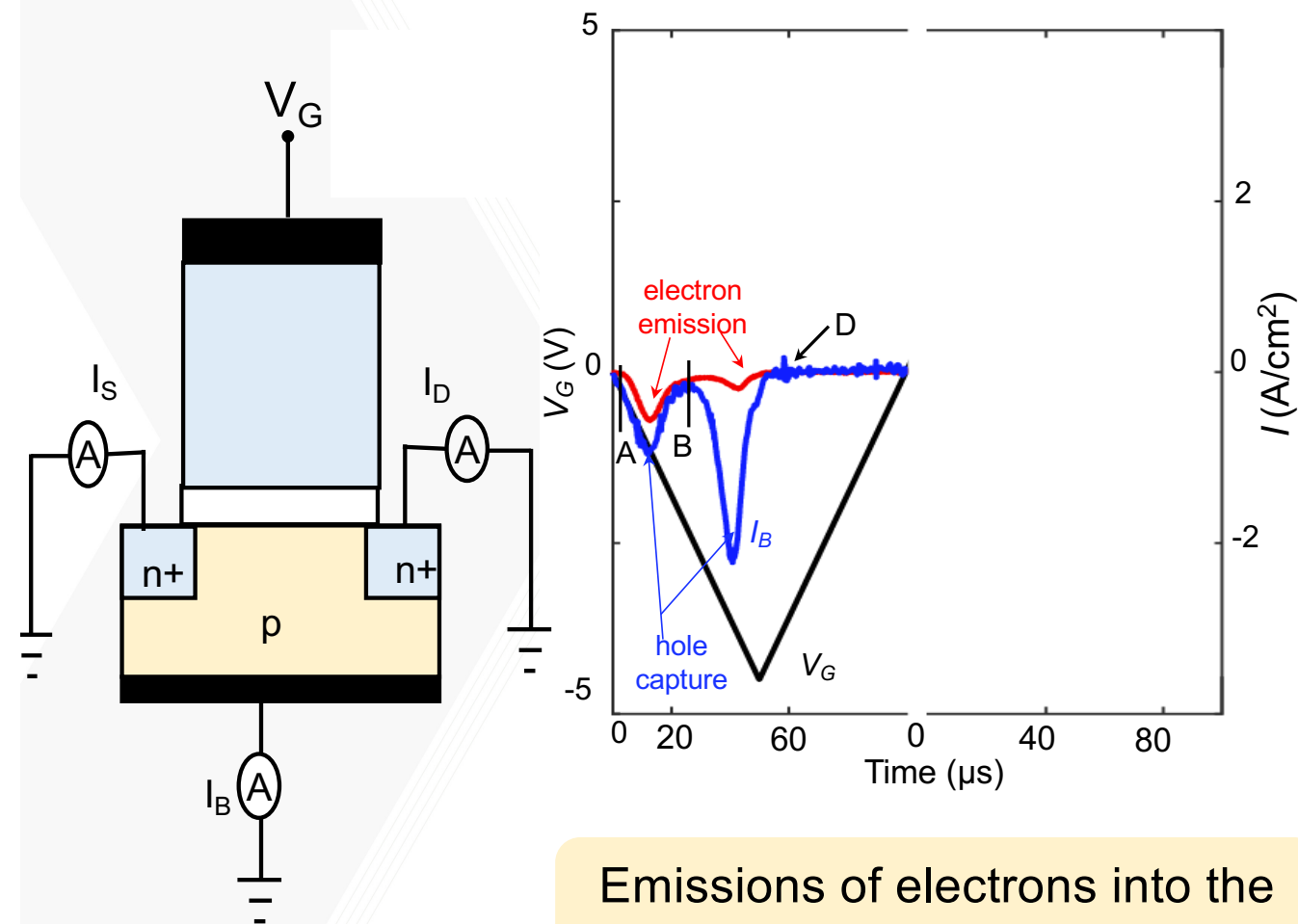


Emissions of electrons into the S/D during hole accumulation.

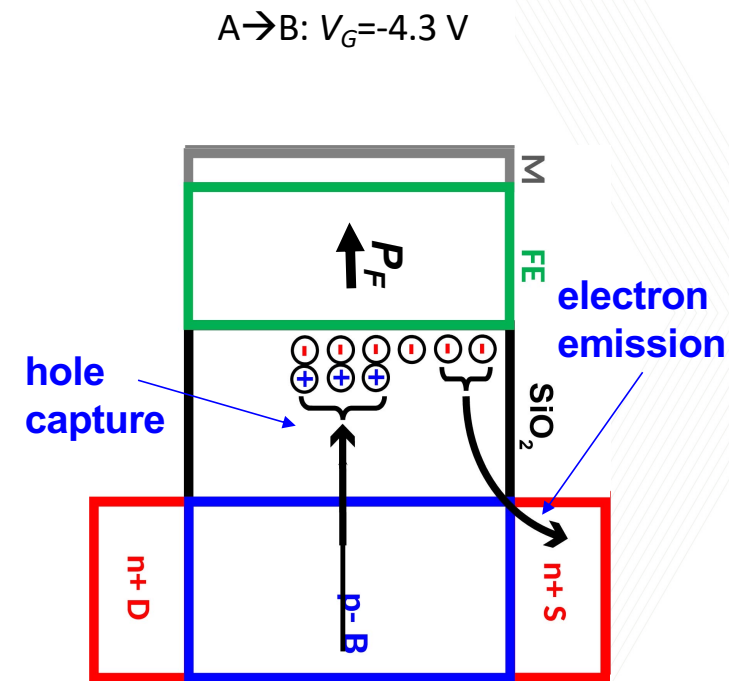


Tasneem et al. IEDM 2021.

Trap Emission and Capture During Write

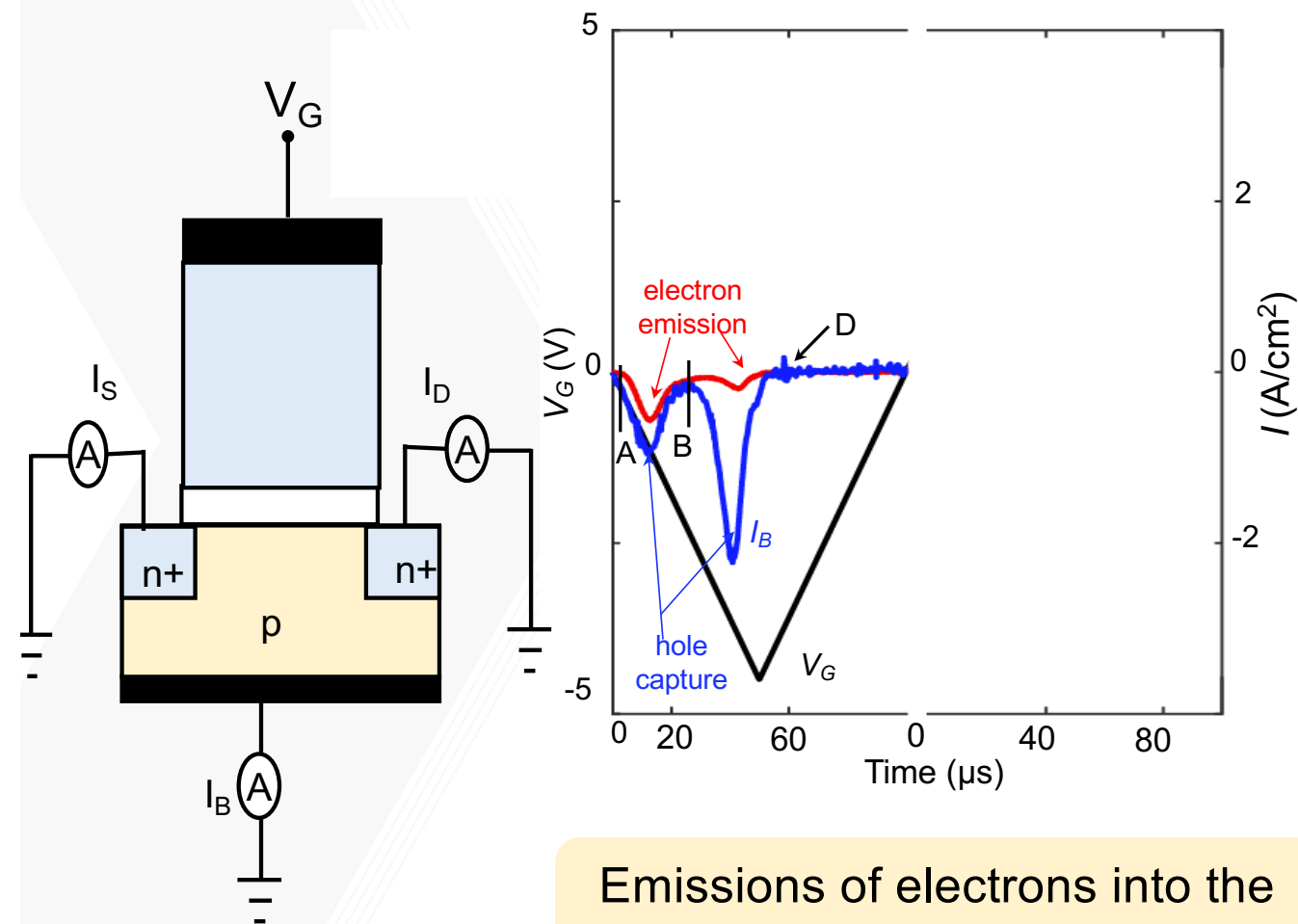


Emissions of electrons into the S/D during hole accumulation.

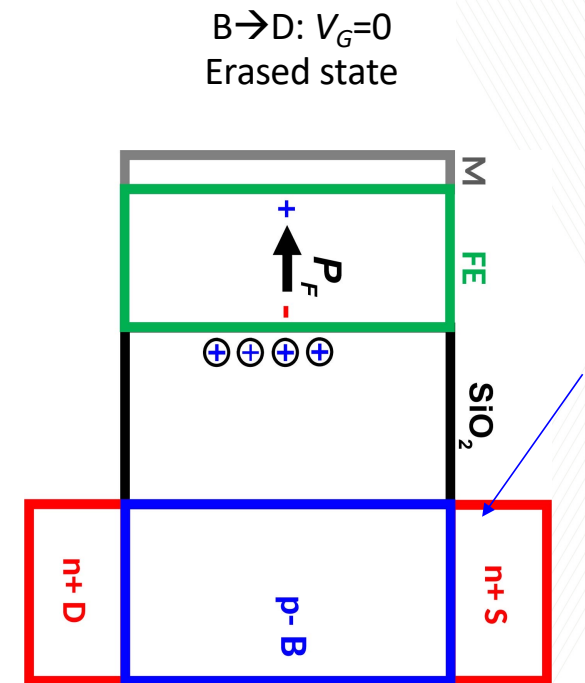


Tasneem et al. IEDM 2021.

Trap Emission and Capture During Write

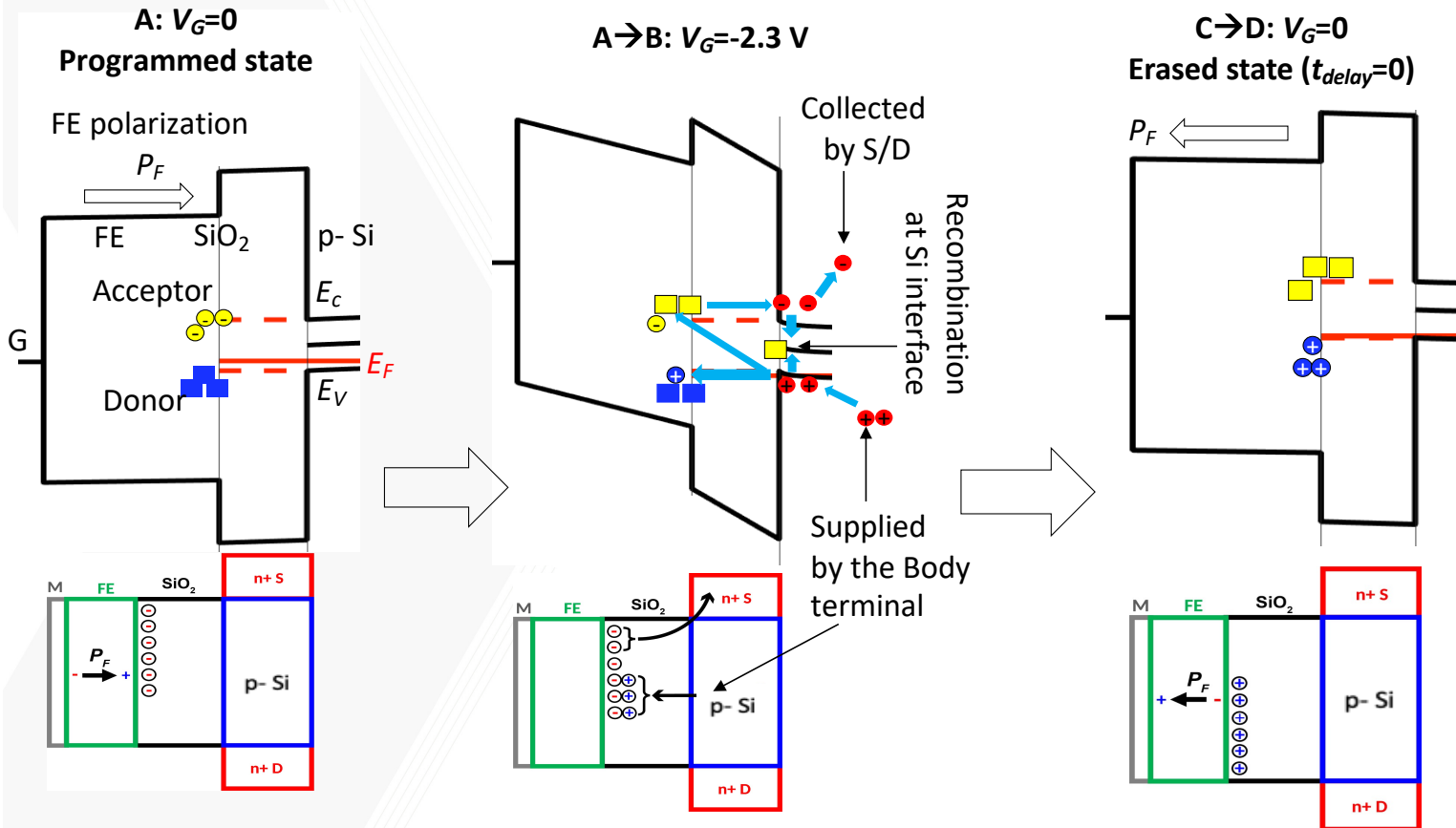


Emissions of electrons into the S/D during hole accumulation.



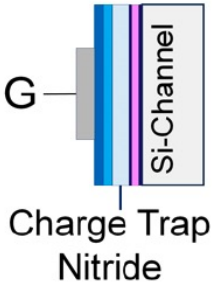
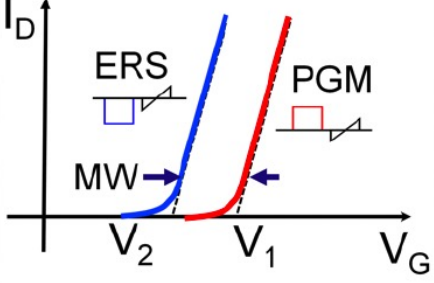
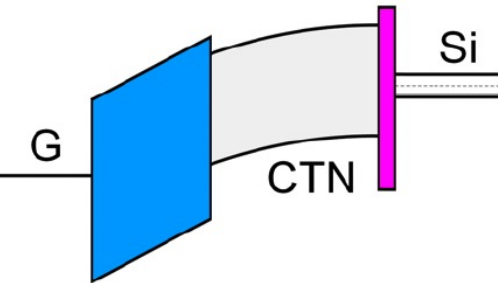
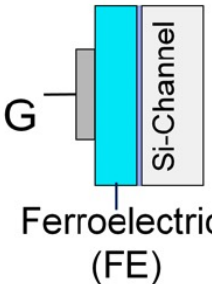
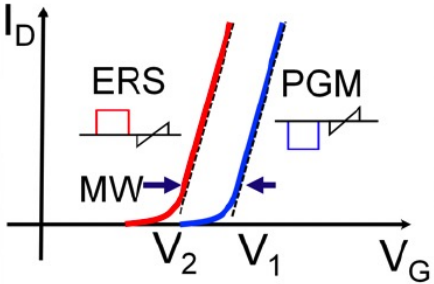
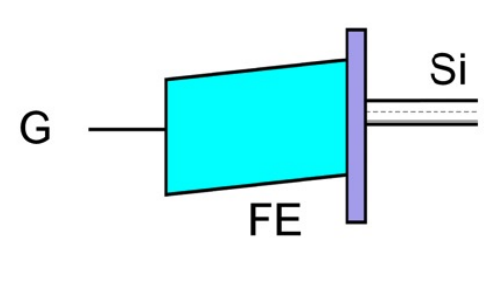
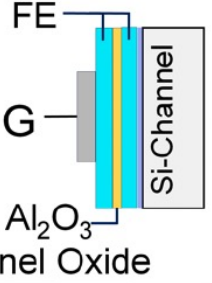
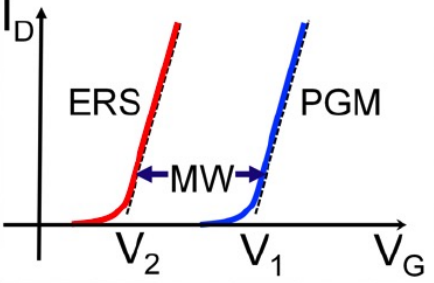
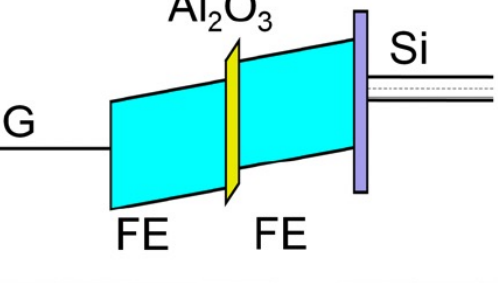
Tasneem et al. IEDM 2021.

Trap Capture and Emission Dynamics



Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2021.

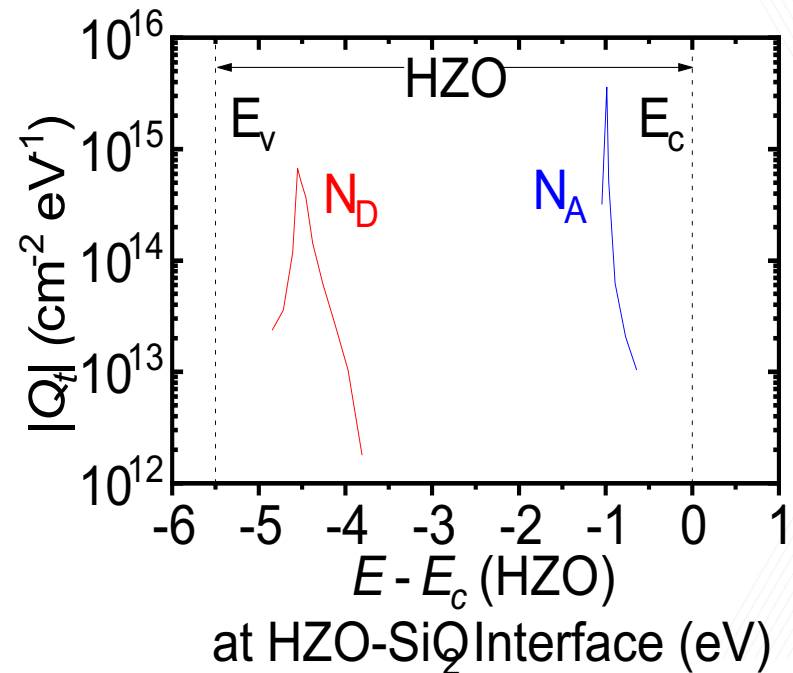
Ferroelectric NAND

	Structure	Characteristics	Band diagram at FB condition	Attributes
Charge Trap Flash Conventional FEFET Proposed FEFET	 Charge Trap Nitride			✓ Large MW × Large Write Voltage Mechanism: Trapping
	 Ferroelectric (FE)			× Low MW ✓ Low Write Voltage Mechanism: Polarization Switching
	 Al₂O₃ tunnel Oxide			✓ Large MW ✓ Moderate Write Voltage Mechanism: Polarization Switching + Trapping + Tunneling

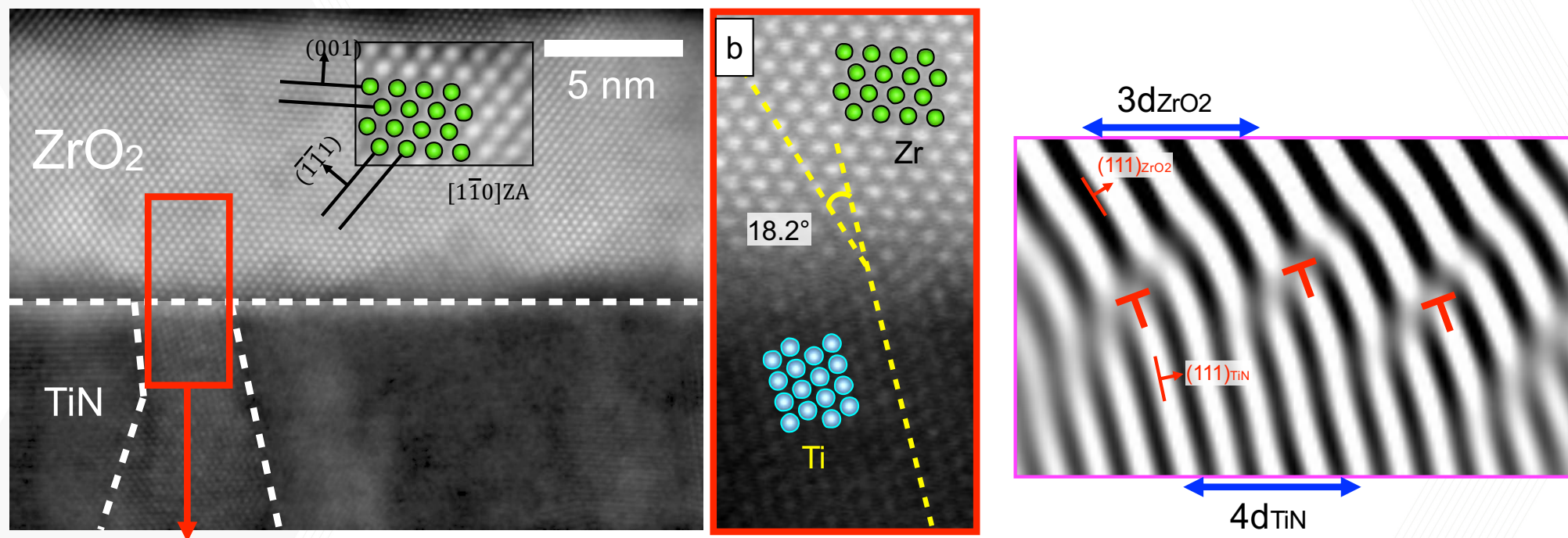
Trap Capture and Emission Dynamics

- Trap levels N_D and N_A are essentially discrete levels
- Donor type trap energy E_D is 0.93 eV above HZO E_v
- Acceptor type trap energy E_A is 0.98 eV below HZO E_c

Passlack, Tasneem et al. IEDM 2022.



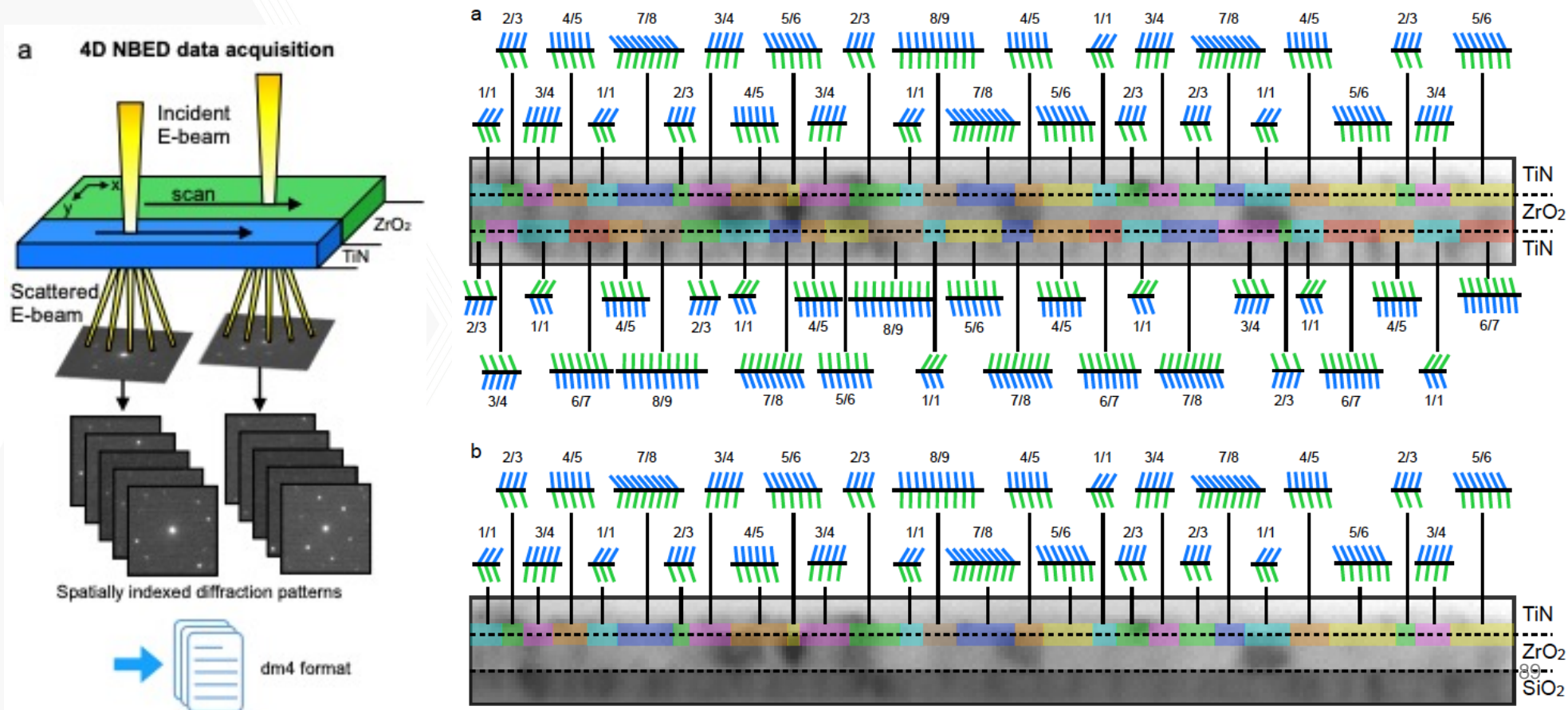
Challenge #4: Polycrystalline microstructure



Orientations in TiN and ZrO₂ are often correlated.

Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO₂. *ACS Applied Materials & Interfaces*, 14(32), 36771-36780.

Epitaxial-like templating: Near coincidence site epitaxy

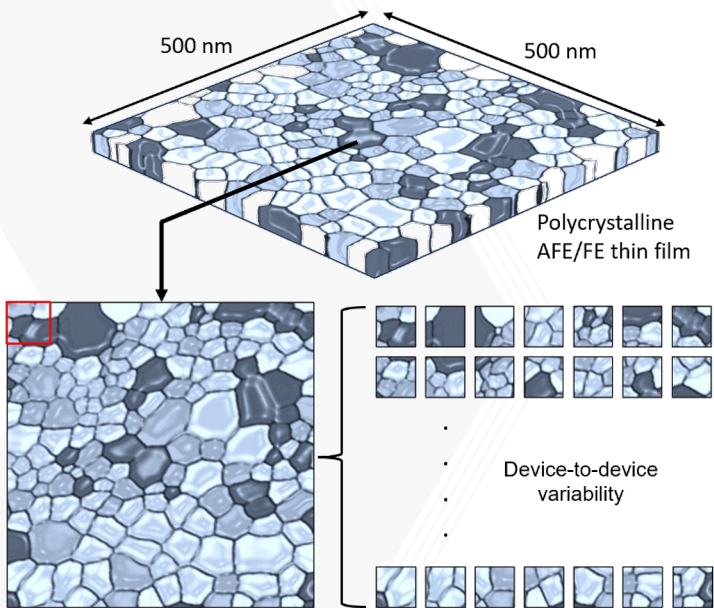


Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO₂. *ACS Applied Materials & Interfaces*, 14(32), 36771-36780.

Connection between microstructure and reliability?



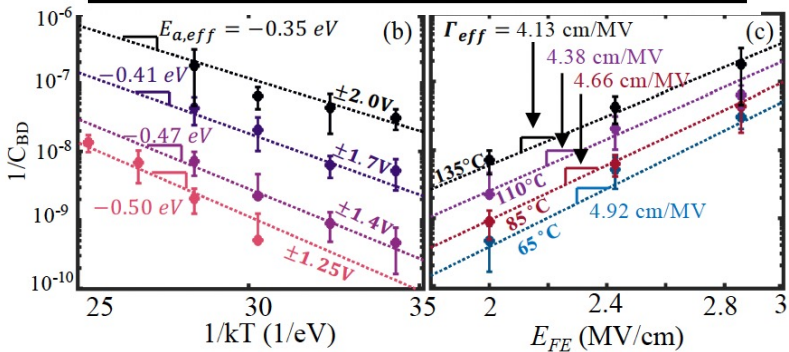
Priyanka
G R



(a) Pre-exponent Field acceleration Bond polarization constant

$$\frac{1}{C_{BD}} = A \exp\left(\frac{-E_a}{kT}\right) \exp\left(\left(\Gamma_o + \frac{\alpha}{kT}\right) E_{FE}\right)$$

Field acceleration factor, $\Gamma_{eff}(T) = \Gamma_o + \frac{\alpha}{kT}$ Effective activation energy, $E_{a,eff}(E_{FE}) = E_{FE}\alpha - E_a$ Activation energy



(f)	Property	Γ_o (cm/MV)	α (eA)	E_a (eV)
HZO	Ferroelectric	0.32	13.39	0.74
SiO ₂ [8]	Dielectric	2.4	1.5	0.6

Ravikumar... Mahapatra, Khan et al. IRPS 2024

Does microstructure have impact on reliability?

Machine Learning Assisted Predictive TCAD Modeling (from Metrology to Device Metrics)

Ferro polarization map (from TKD data from SEM/TEM)

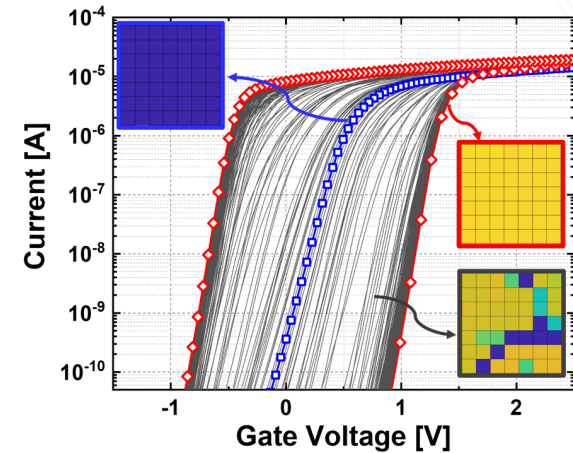
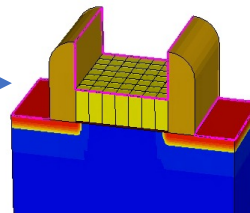
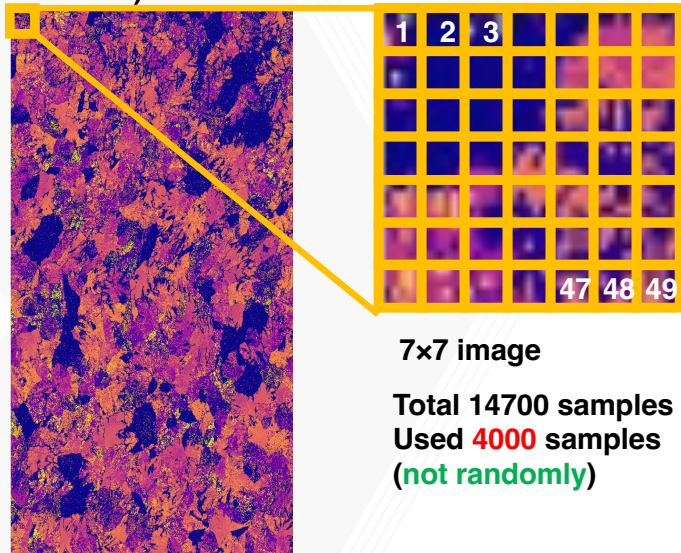
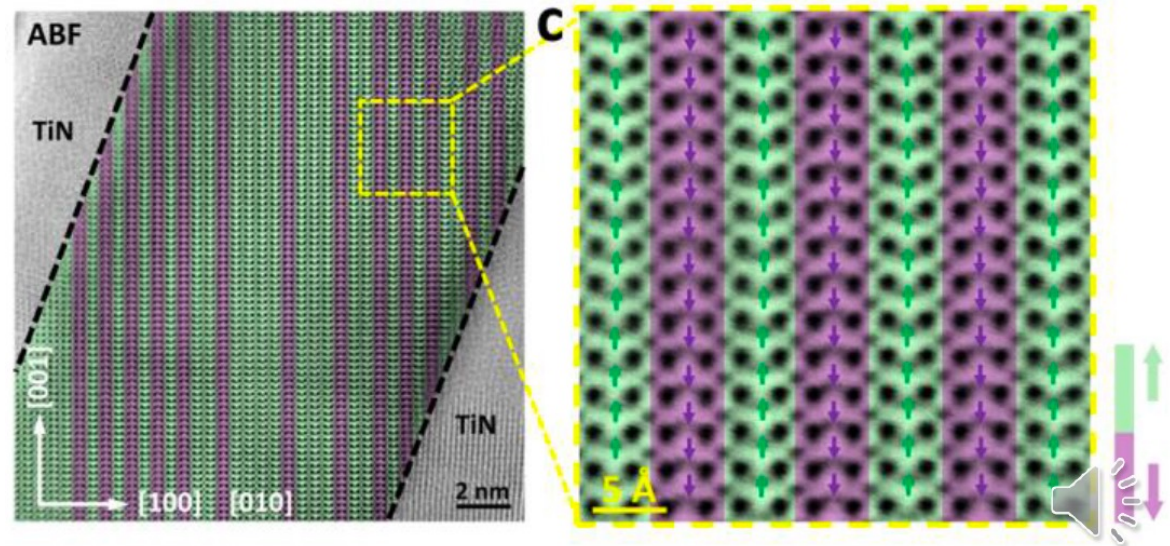
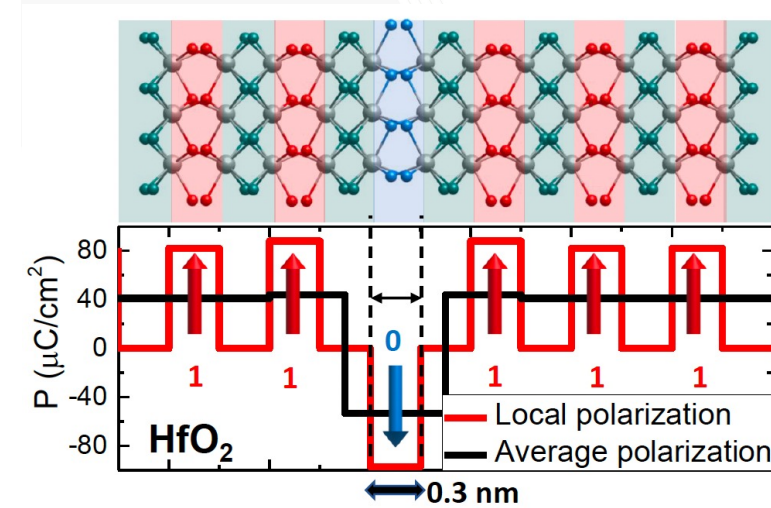


TABLE II. Average, 3-sigma and percentage of prediction error

	TCAD	ML-based prediction		
	μ	μ	3σ	Error
HVT [V]	1.05	1.05	0.08	1.2%
LVT [V]	-0.53	-0.53	0.07	2.0%
I_{on} [μA]	6.68	6.68	1.01	2.1%
SS [mV/dec]	94.52	94.48	9.0	1.6%

G. Choe, P. V. Ravindran, A. Lu, J. Hur, M. Lederer, A. Reck, S. Lombardo, N. Afroze, J. Kacher, A. I. Khan, S. Yu, "Machine learning assisted statistical variation analysis of ferroelectric transistors: from experimental metrology to predictive modeling," IEEE Symposium on VLSI Technology and Circuits (VLSI) 2022.

Challenge #5: Atom scale memories?



Can ferroelectric enable the ultimately scaled memory?
What would be the read scheme?

Lee et al. Science 2020.

The 7 trillion \$ chip industry of the future

Forbes

Artificial General Intelligence (AGI) And The Coming Wave

Randy Bean Contributor

Randy Bean is a noted Author, Speaker, Founder, CEO, & Senior Advisor.

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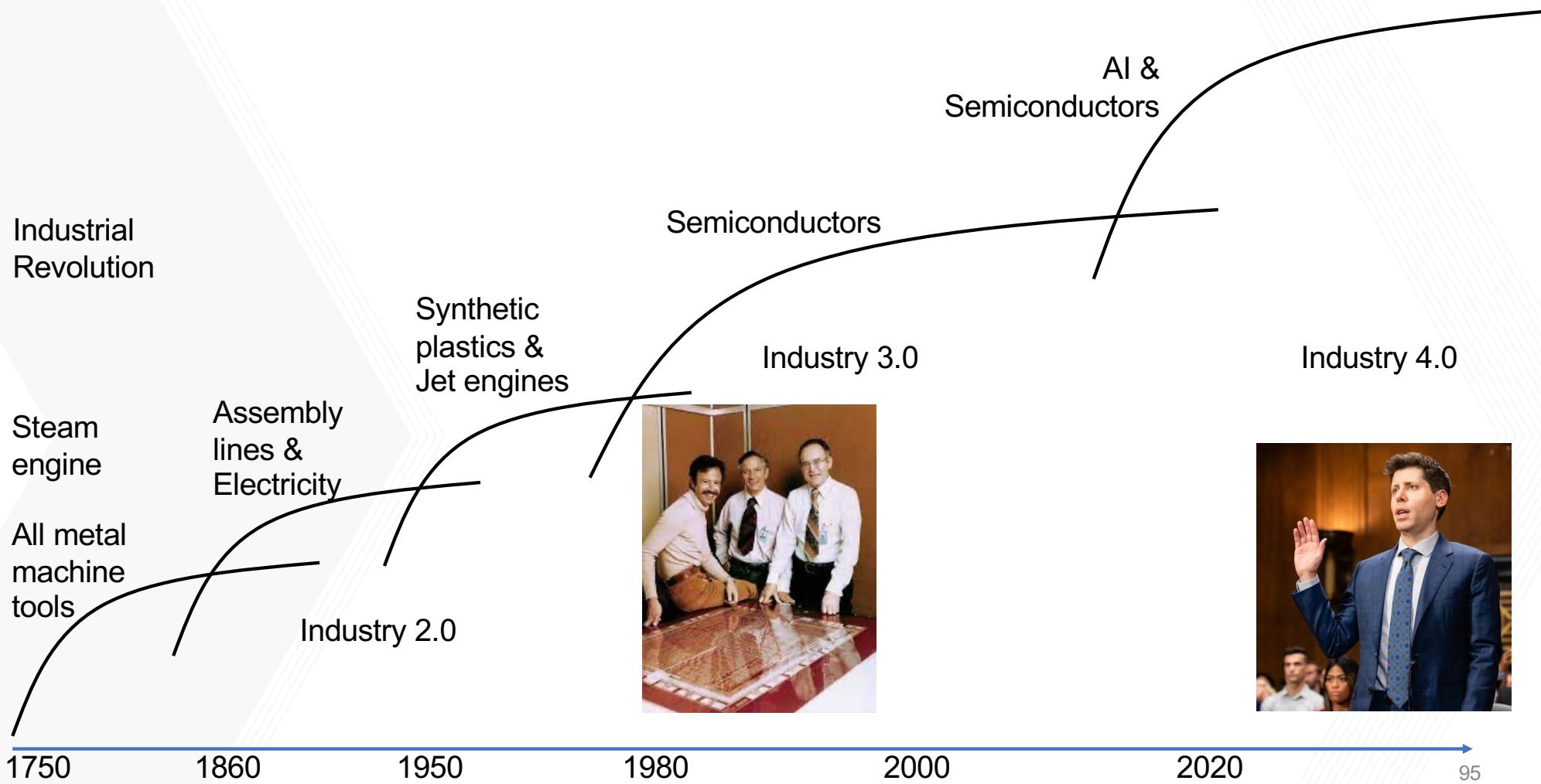
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TECHNOLOGY | ARTIFICIAL INTELLIGENCE

Sam Altman Seeks Trillions of Dollars to Reshape Business of Chips and AI

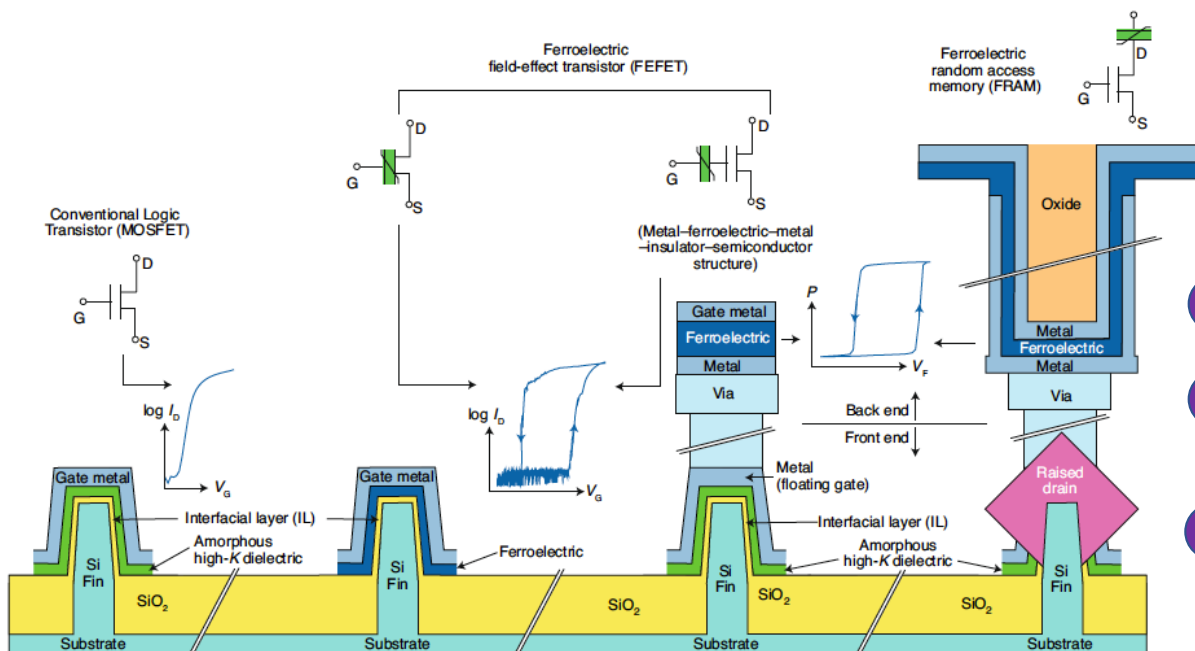
OpenAI chief pursues investors including the U.A.E. for a project possibly requiring up to \$7 trillion





The era of ferroelectronics

The next wave of exponential growth of the semiconductor industry depends on how well the electronic hardware can support the explosion of data-centric computing.



Ferroelectric technology will be a key component because of

- 1 Performance
- 2 Energy and area efficiency
- 3 Logic and memory functionalities

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.



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