Ferroelectronics for memory and storage

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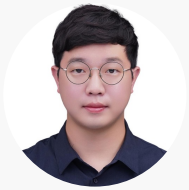
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Examples	Capabilities	Limitations
"Explain quantum computing in simple terms"	Remembers what user said earlier in the conversation	May occasionally generate incorrect information
"Got any creative ideas for a 10 year old's birthday?"	Allows user to provide follow-up corrections	May occasionally produce harmful instructions or biased content
"How do I make an HTTP request in Javascript?"	Trained to decline inappropriate requests	Limited knowledge of world and events after 2021

Try SemiconductorGPT at
https://chat.openai.com/g/g-Wz4h6XhrV-semiconductorgpt

GT ECE 3030 Course Assistant

ChatGPT

You

Consider an n-type MOSFET with N_A=7E18}m^3. The gate length of the MOSFET L=2 um, width W=12 um and the oxide thickness t_ox= 8 nm.
Take N_C=N_V=1E25 m^-3, E_G=1.12 eV, n_i=1.5E{16} m^-3, kT=0.026 eV.

Calculate the numerical values of following quantities.
(1) phi_B=|E_F-E_i|,
(2) the oxide capacitance C_ox,
(3) the maximum depletion width W_max , and
(4) the threshold voltage V_t.

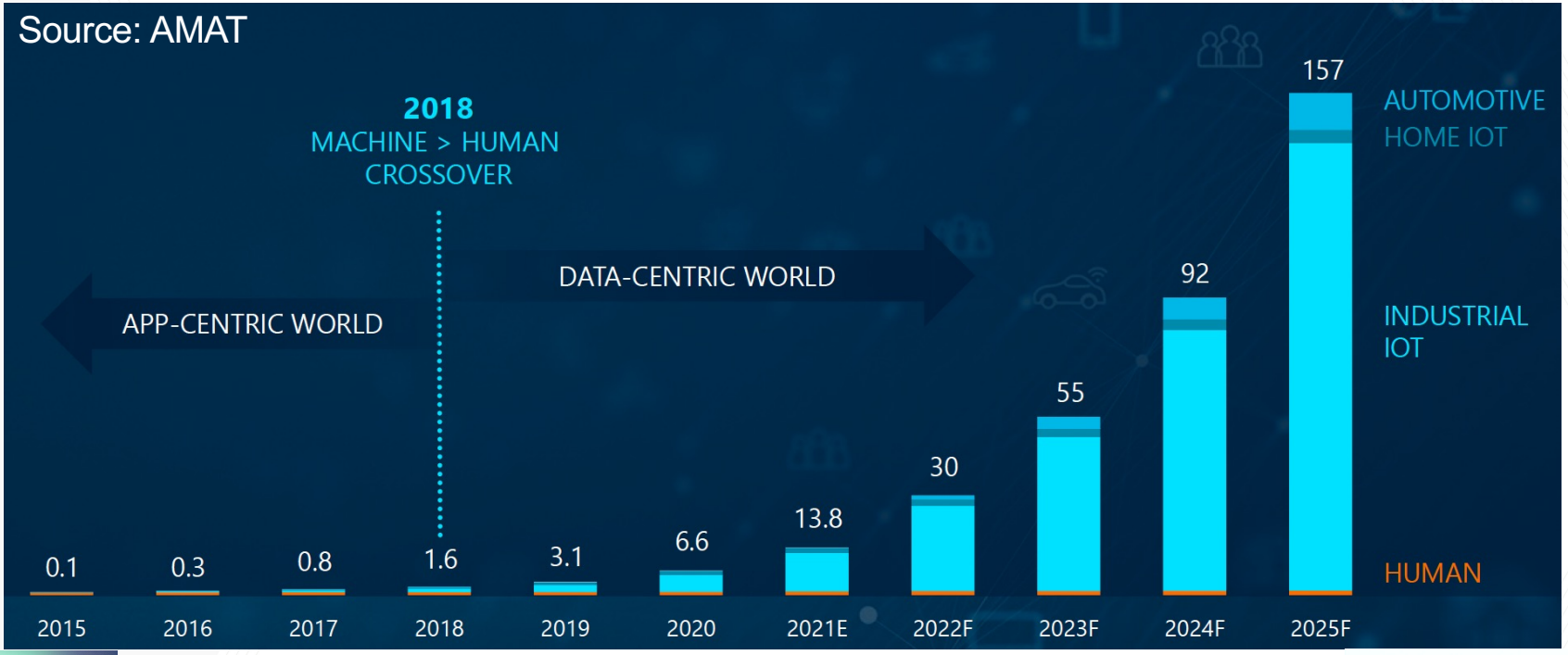
ChatGPT

To calculate the quantities ●

Message ChatGPT...

Inflection and Data centric world

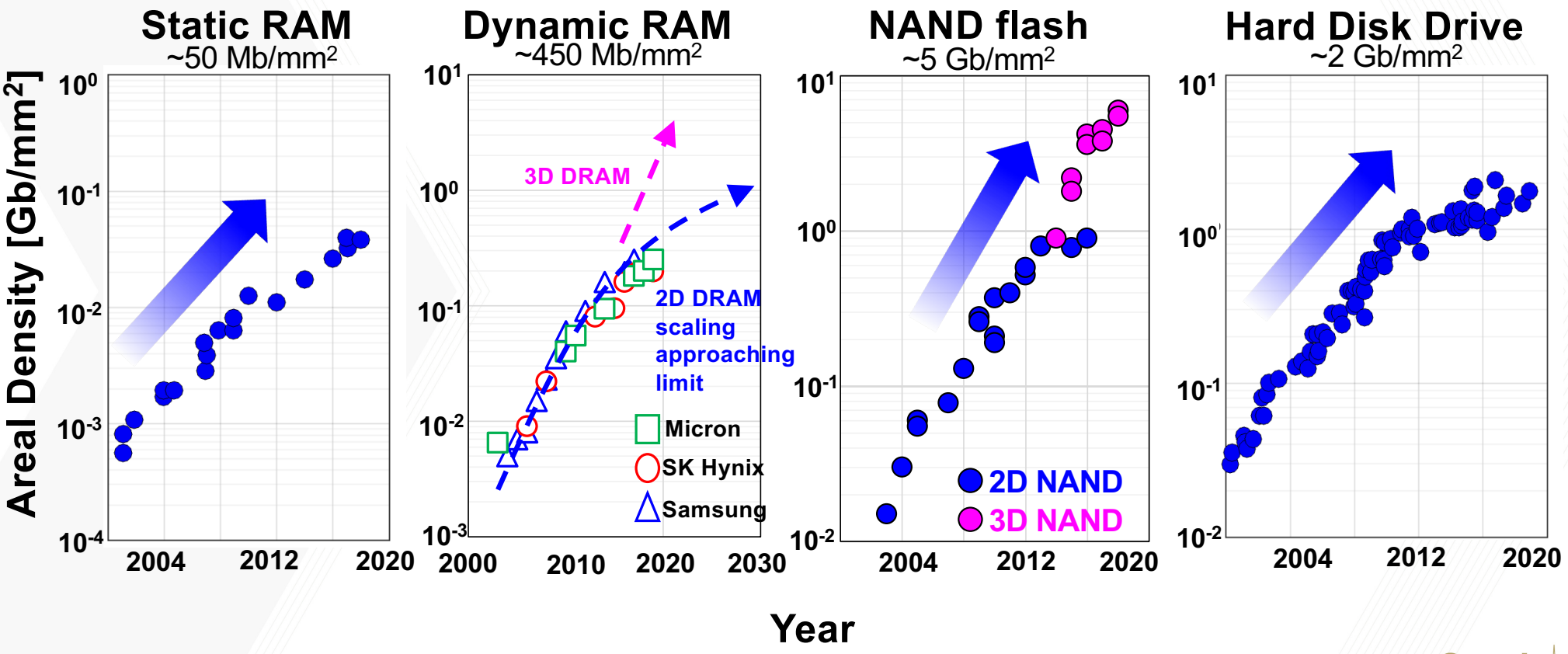
1 ZB=10^{21} B



Human generated data
An individual created an average of **120 MB of data per hour** in 2020.

Machine generated data
A connected car create up to **25 GB of data per hour**.

Innovation at the core – Memory



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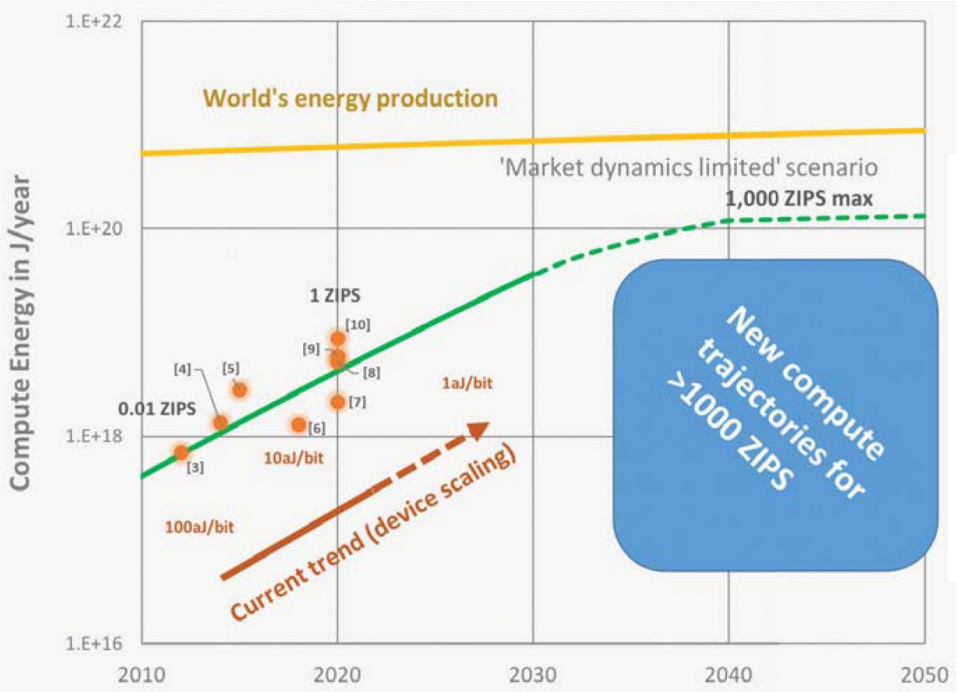
Sustainability of computation

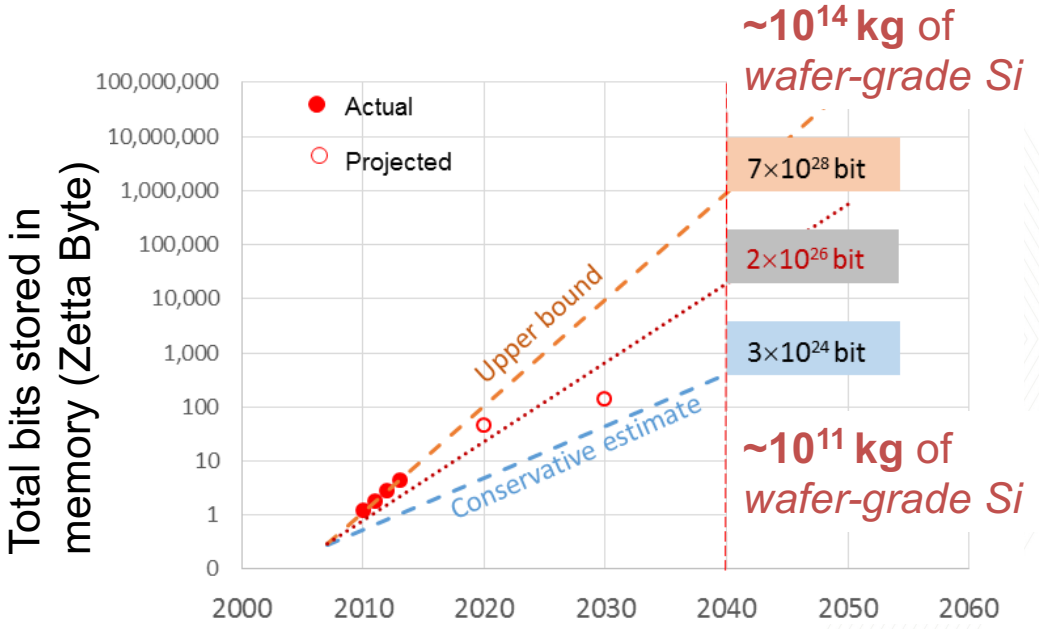
Source: SRC decadal plan

Projected energy cost of computation



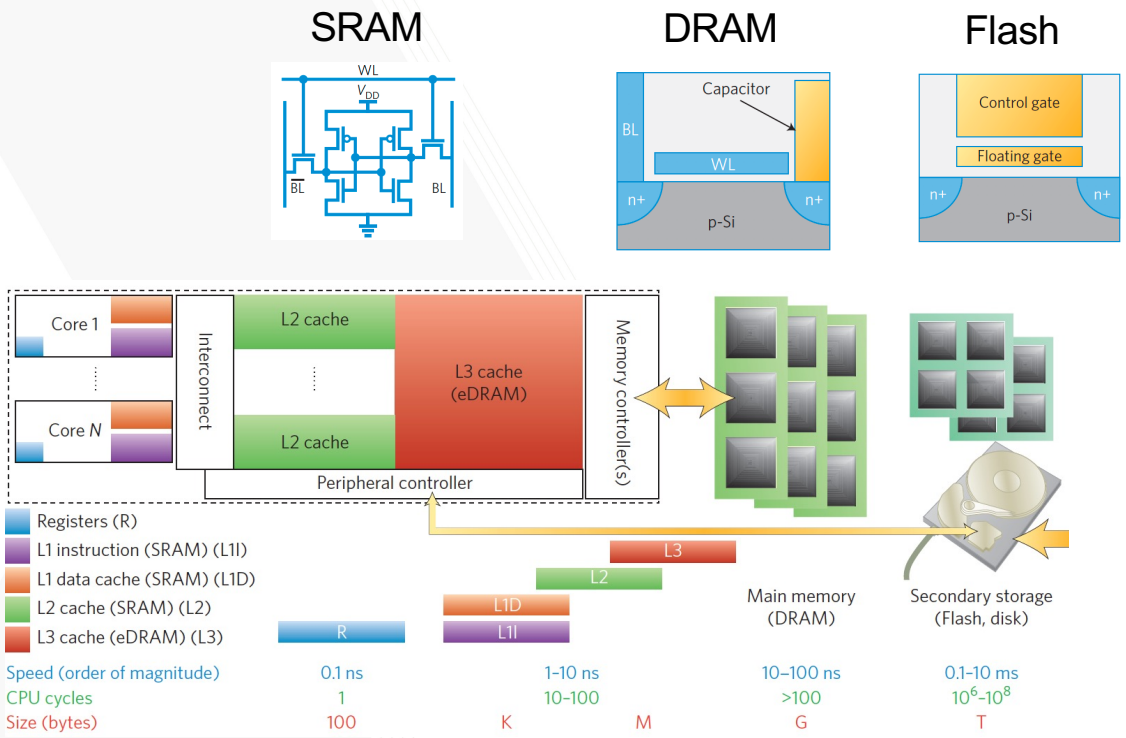
Compute energy rises exponentially, while global energy production grows linearly.

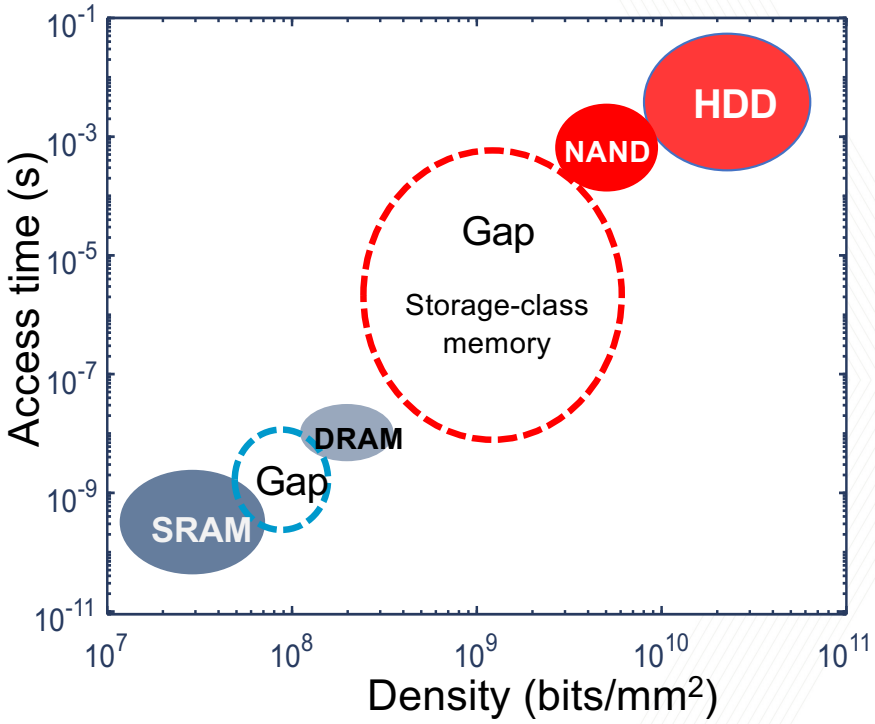
Projected Si supply



Projected annual global supply of Silicon wafers: 10^7 – 10^8 kg in 2040.

Generational challenges in memory





1. Continue scaling.
2. Fill the Gaps.

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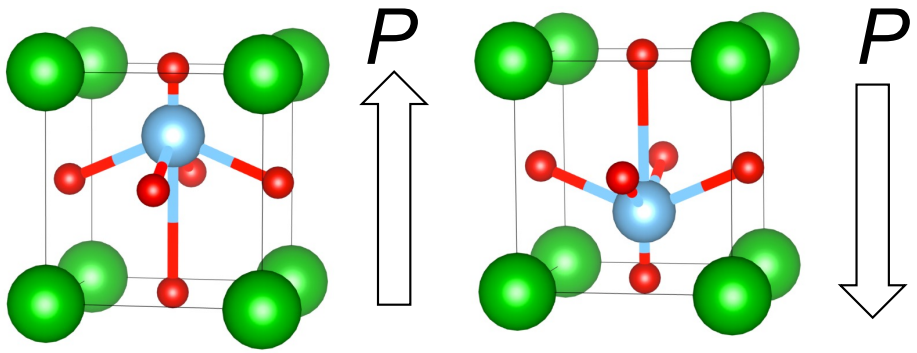
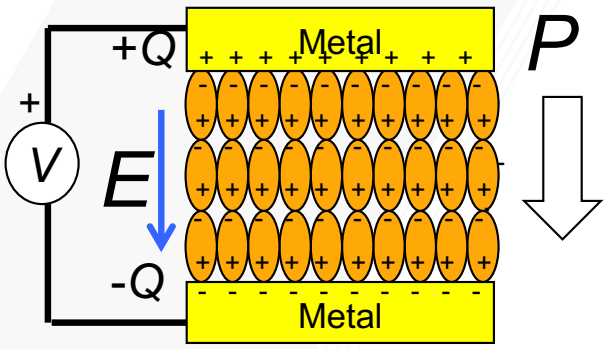
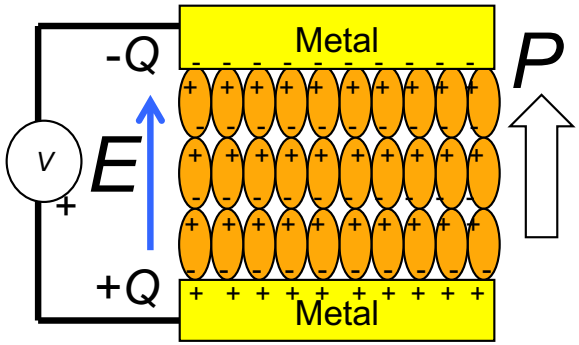
Ferroelectricity

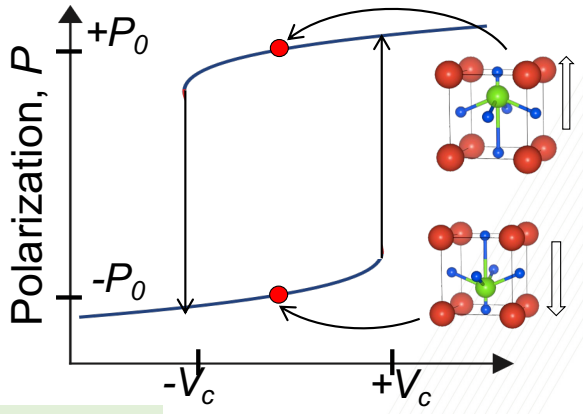
Classical Ferroelectric
$PbTiO_3$, $BaTiO_3$ etc.

Emerging CMOS compatible
Ferroelectrics:
Doped HfO_2









A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

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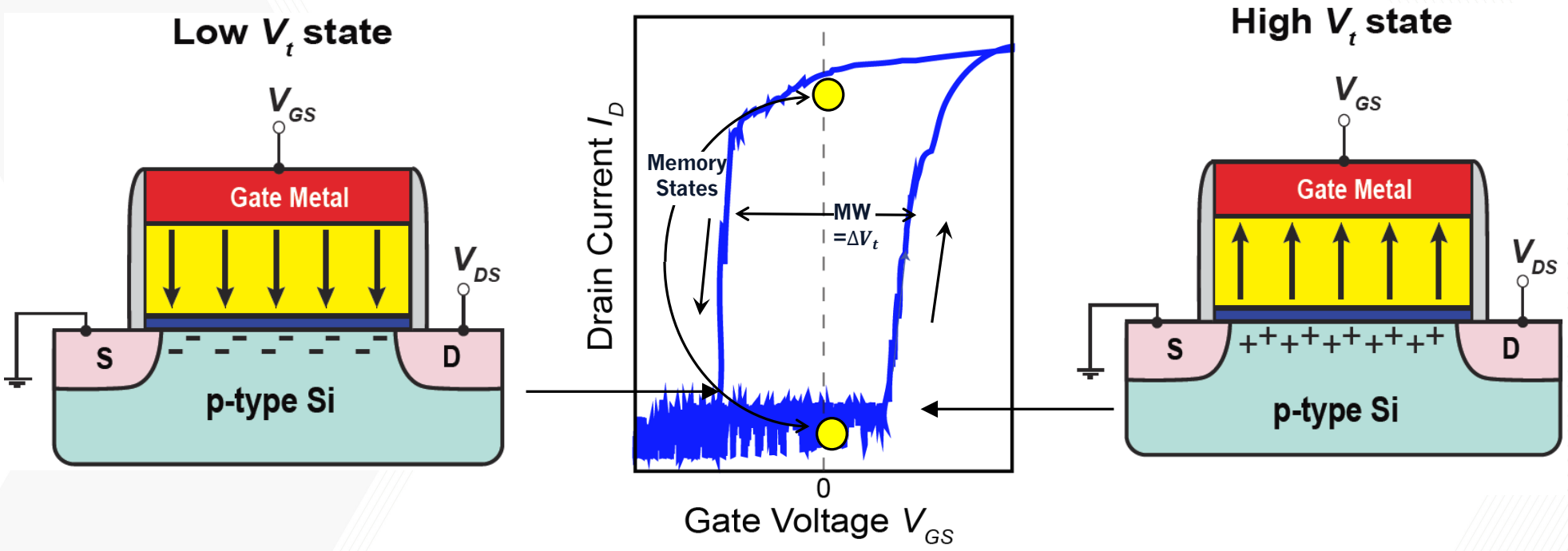
Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the "remnant" polarization.

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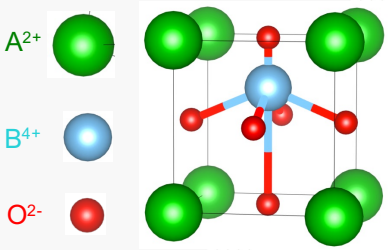
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for for code storage in microcontrollers.

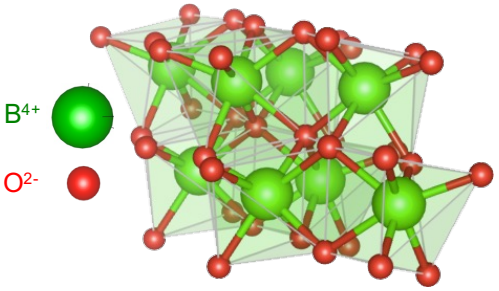
2. Controlled annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al. Appl. Phys. Lett*. 99, 112904 (2011)
- Boscke *et al. 2011 IEEE Int. Electron Devices Meeting.* p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al. Nano Lett.* 12, 4318 (2012)

Perovskite-structure ferroelectric oxide (ABO_3)



Fluorite-structure ferroelectric oxide (BO_2)



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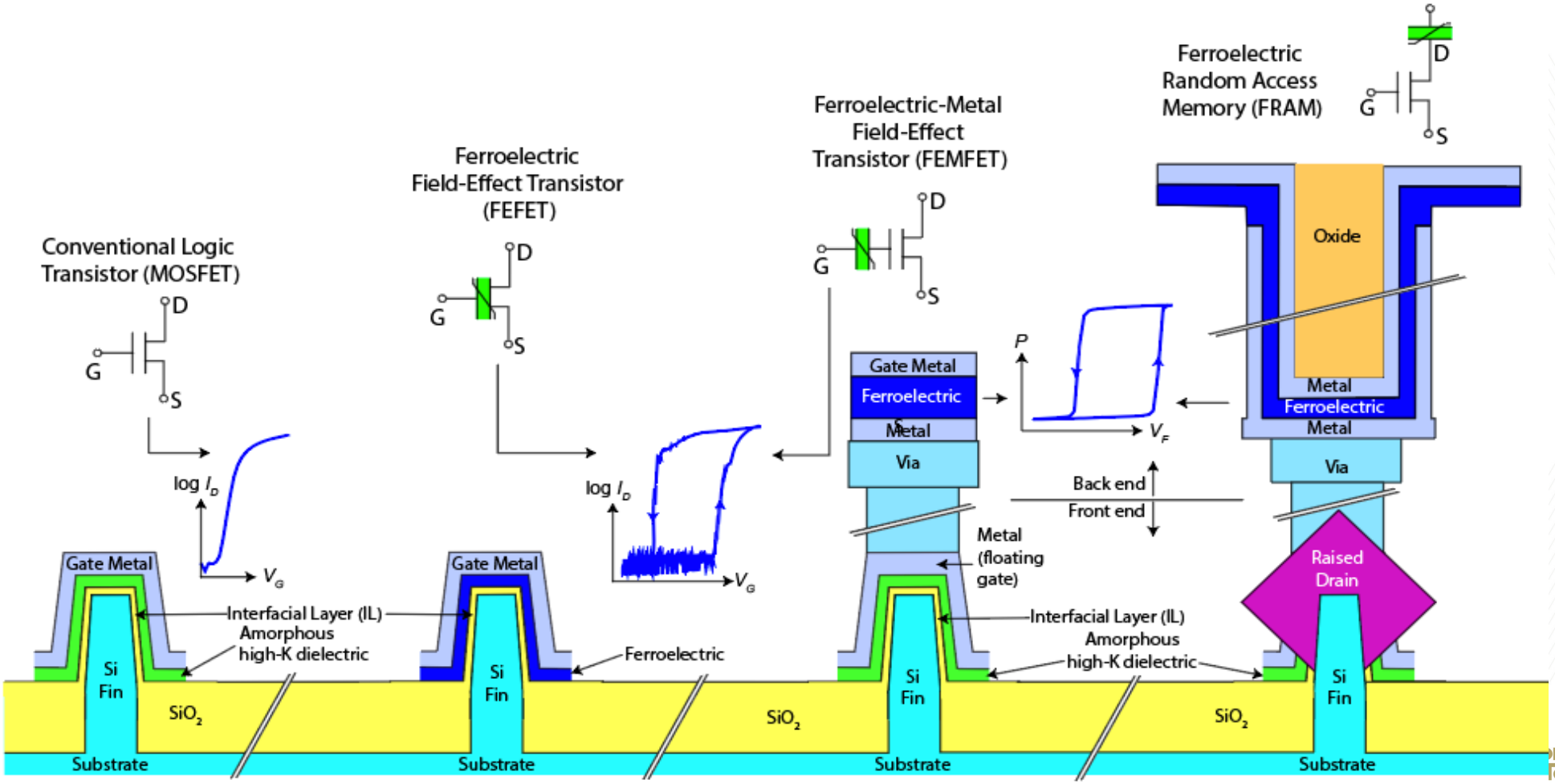
Ferroelectric devices



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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APPLIED PHYSICS LETTERS **99**, 112904 (2011)

Phase transitions in ferroelectric silicon doped hafnium oxide

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[6]*Department of Nanoelectronic Materials, University of Technology Dresden, 01062 Dresden, Germany*

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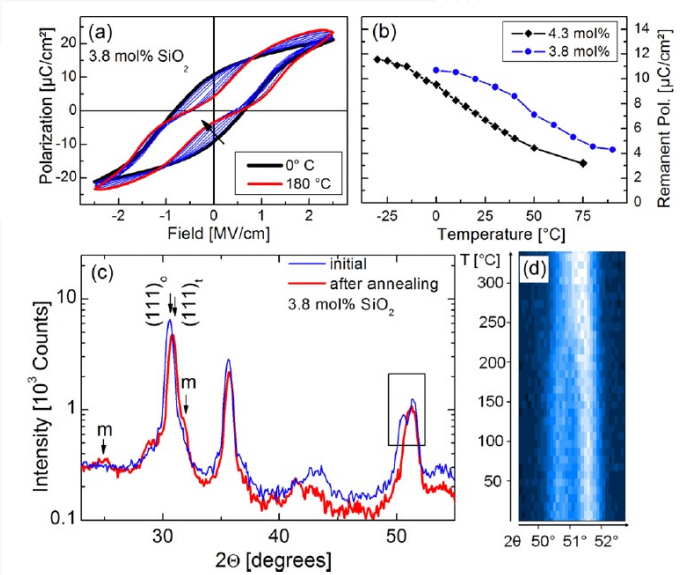

NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads

N. Ramaswamy, A. Calderoni, J. Zahurak, G. Servalli, A. Chavan, S. Chhajed, M. Balakrishnan, M. Fischer, M. Hollander, D. P. Ettisserry, A. Liao, K. Karda, M. Jerry, M. Mariani, A. Visconti, B. R. Cook, B. D. Cook, D. Mills, A. Torsi, C. Mouli, E. Byers, M. Helm, S. Pawlowski, S. Shiratake, and N. Chandrasekaran
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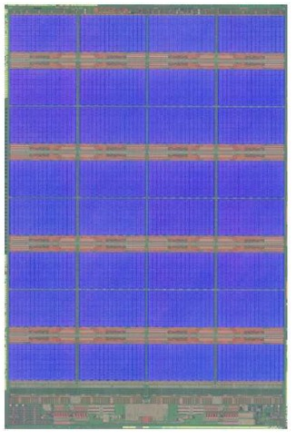

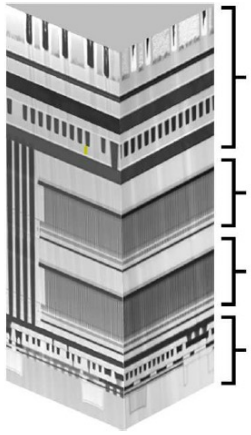

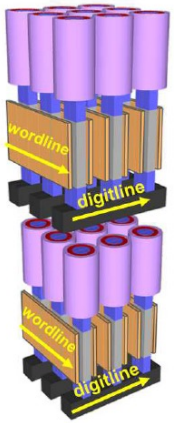

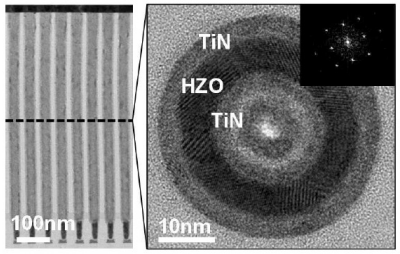

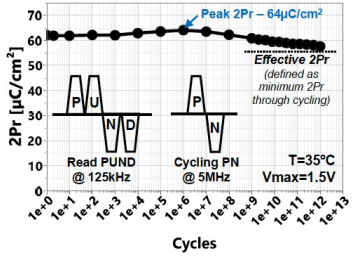

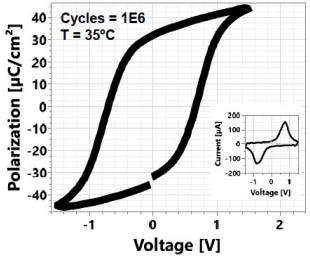

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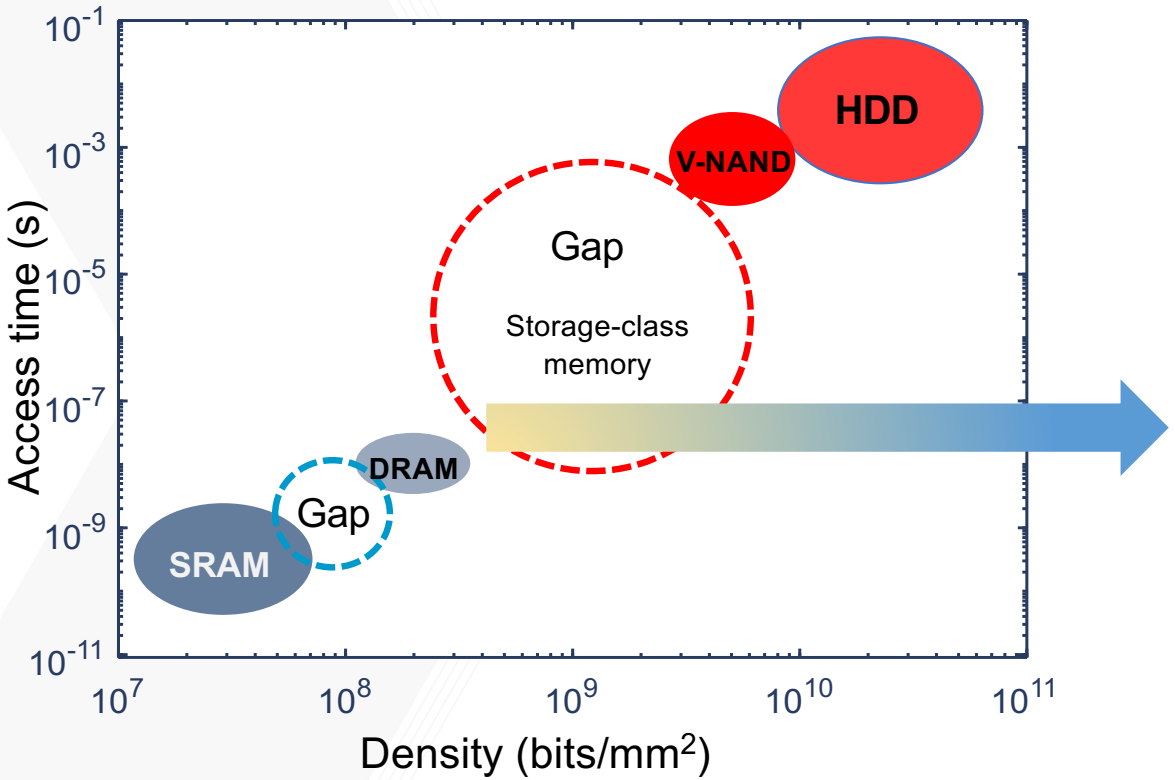
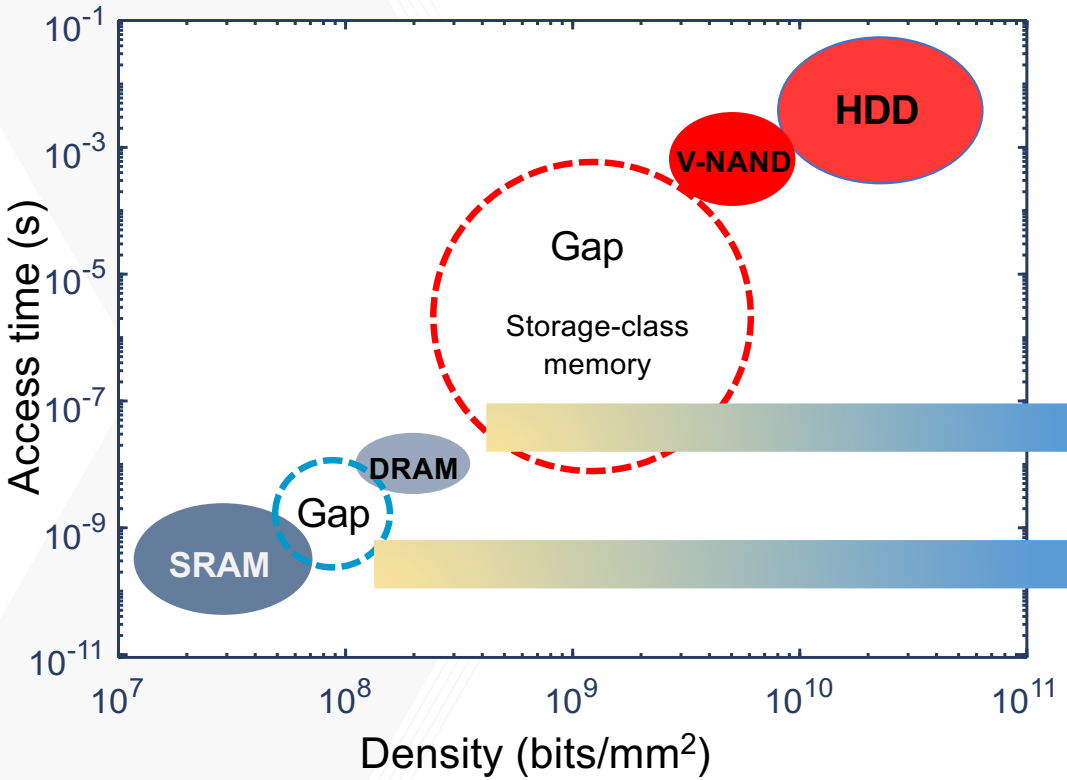
Ferroelectrics for memory and storage



Ferroelectrics for the DRAM/Storage class space

Micron
Dual Layer 3-D stacked FRAM
Capacity – 32 Gb (Sk Hynix DRAM –-8 Gb)
Latency – 180 ns (LPDDR5 – 60 ns)
Density – 450 Mb/mm^2

Ferroelectrics for memory and storage



Ferroelectrics for the DRAM/Storage class space

Ramaswamy et al. Micron, IEDM 2024
Dual Layer 3-D stacked FRAM
Capacity – 32 Gb (Sk Hynix DRAM –-8 Gb)
Latency – 180 ns (LPDDR5 – 60 ns)
Density – 450 Mb/mm^2

Ferroelectrics for embedded memories/cache?

FEFET as an embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM[70]	eFlash (FG)	eFlash (SG MONOS)[42]	eFlash (SONOS)[41]	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based)[67]
Cell size	120–150F^2	40F^2	40–60F^2	40–50F^2	50–60F^2	10–30F^2	10–30F^2	30–40F^2	50–60F^2
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 µs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	>10^{16}	>10^{16}	~10^4	~10^5	~10^6	10^5–10^9	>10^{10}	>10^{12}	>10^{14}

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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Progress in FEFET technology

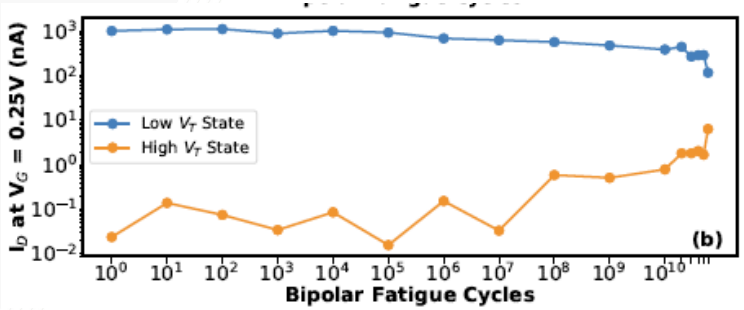
1 Write voltage and Memory Window	2 Read/Write Speed	3 Device-to-device variation	4 Reliability and endurance
Specs			
<1.5 V write voltage >0.5 V memory window	<10 ns write speed <10 ns read-after-write delay	$\Delta V_{t,3\sigma} =$ 20-50 mV (7 nm node)	>10^{12} cycles

Progress in FEFET technology

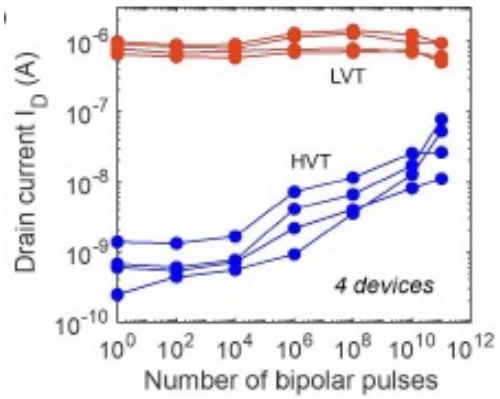
1	2	3	4
Write voltage and Memory Window	Read/Write Speed	Device-to-device variation	Reliability and endurance

Specs

<1.5 V write voltage >0.5 V memory window	<10 ns write speed <10 ns read-after-write delay	$\Delta V_{t,3\sigma}$ = 20-50 mV (7 nm node)	>10^{12} cycles



Tan et al. IEEE EDL 42, 994 (2021).



Dutta et al. IEEE EDL 43, 383 (2022).

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Progress in FEFET technology

1	2	3	4
Write voltage and Memory Window	Read/Write Speed	Device-to-device variation	Reliability and endurance

Specs

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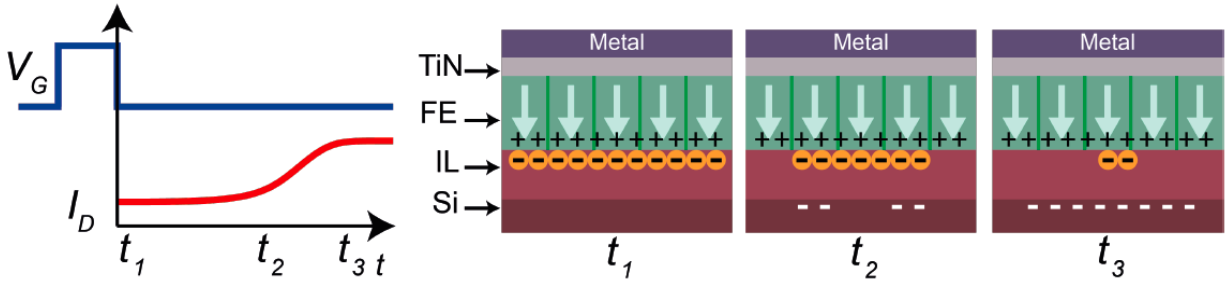

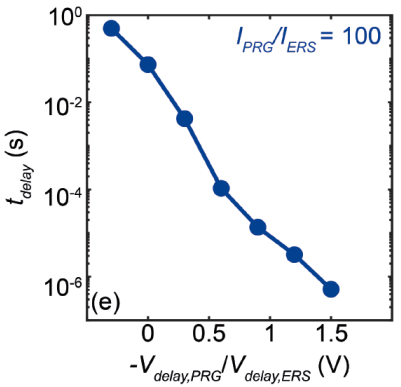

Wang, Z., Tasneem, N., Hur, J., Chen, H., Yu, S., Chern, W., & Khan, A. (2021, December). Standby bias improvement of read after write delay in ferroelectric field effect transistors. In *2021 IEEE International Electron Devices Meeting (IEDM)* (pp. 19-3). IEEE.

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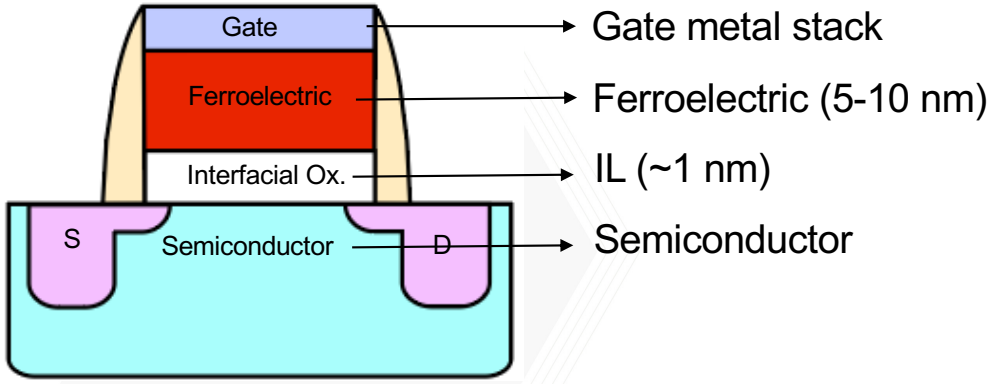
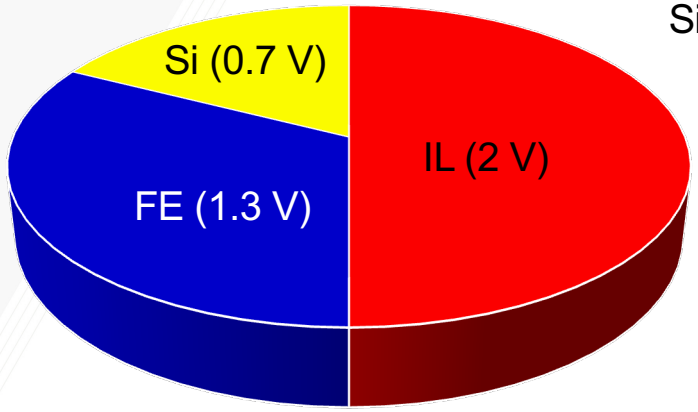
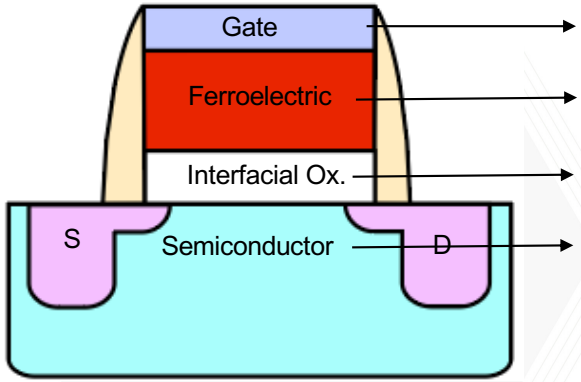
Write voltage vs. memory window trade-off





Write voltage vs. memory window trade-off

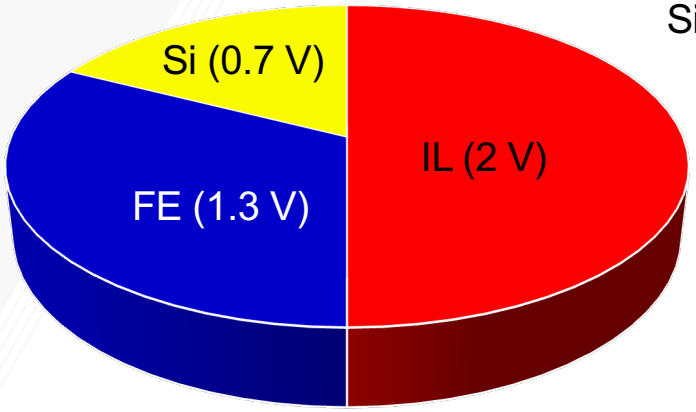


Gate metal stack

Ferroelectric (5-10 nm)

IL (~1 nm)

Semiconductor

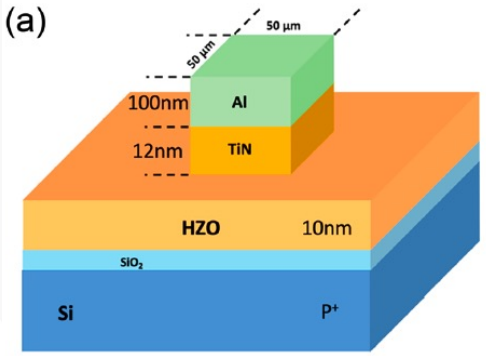


Reducing the thickness of the IL or increasing the K of the IL.

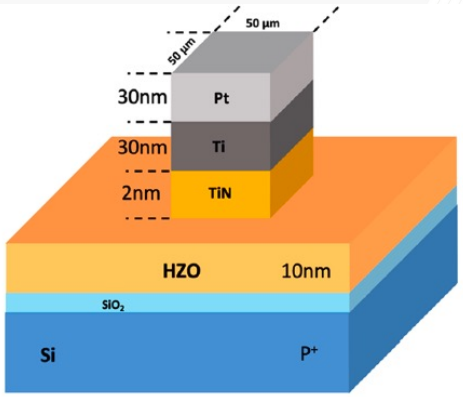
Reducing FE thickness reduces MW. $MW_{max}=2V_C$

Changing the band-gap of the semiconductor By changing the channel material from Si to SiGe or Ge.

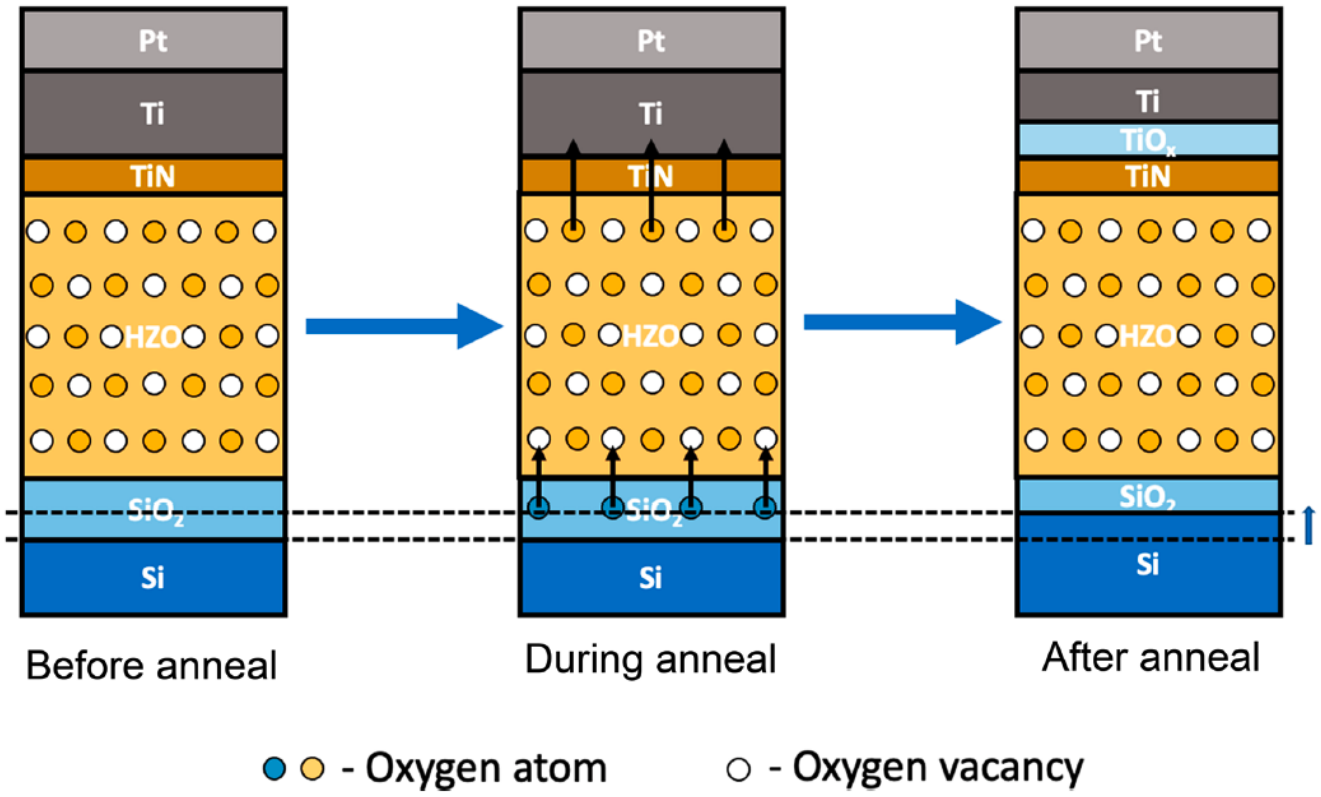
Remote oxygen scavenging to reduce IL thickness



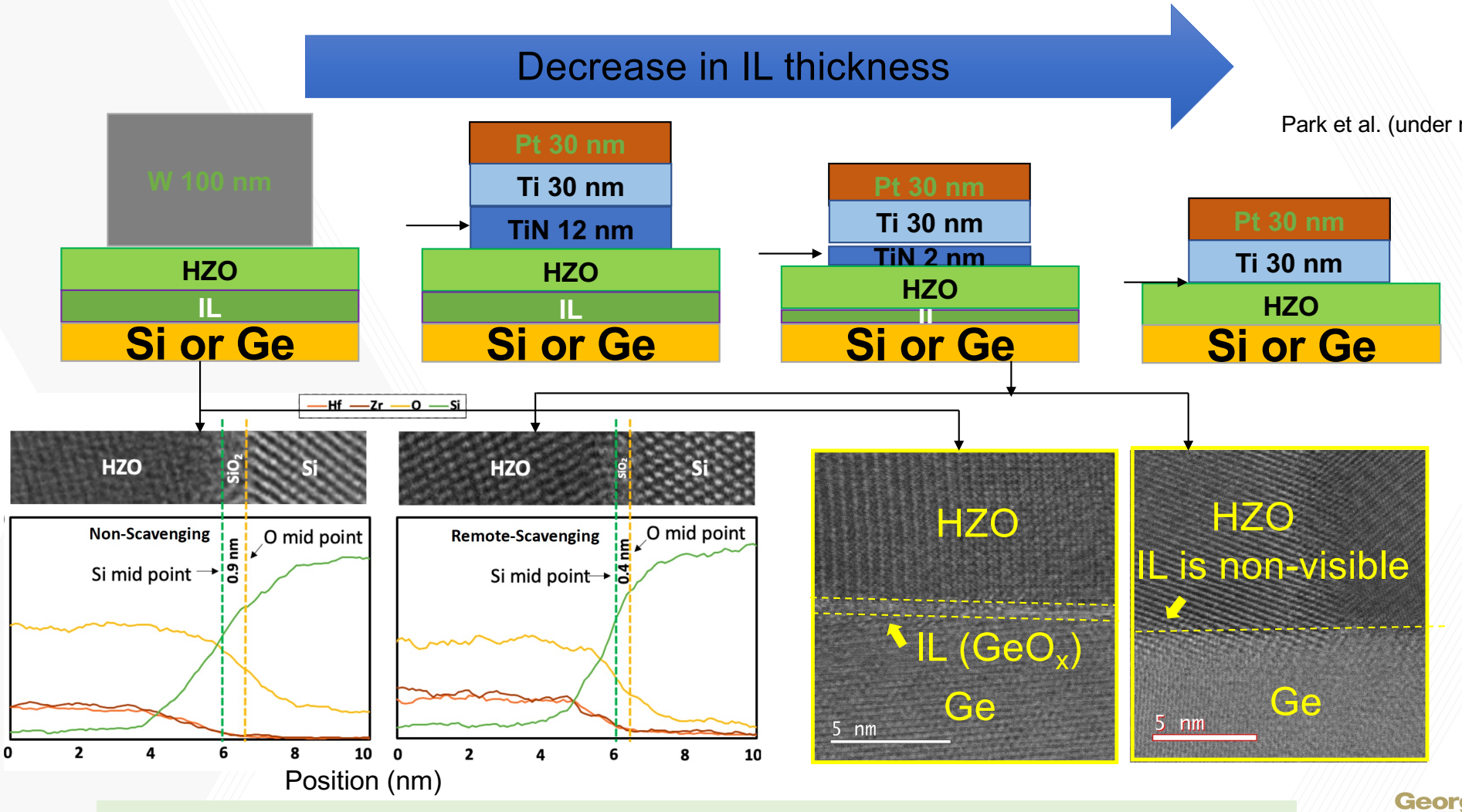
Non-Scavenging



Remote-Scavenging



Tasneem et al. “Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium–Zirconium Oxide-Based Metal–Oxide–Semiconductor Structures”, ACS Appl. Mater. Interfaces 2022, 14, 43897–43906



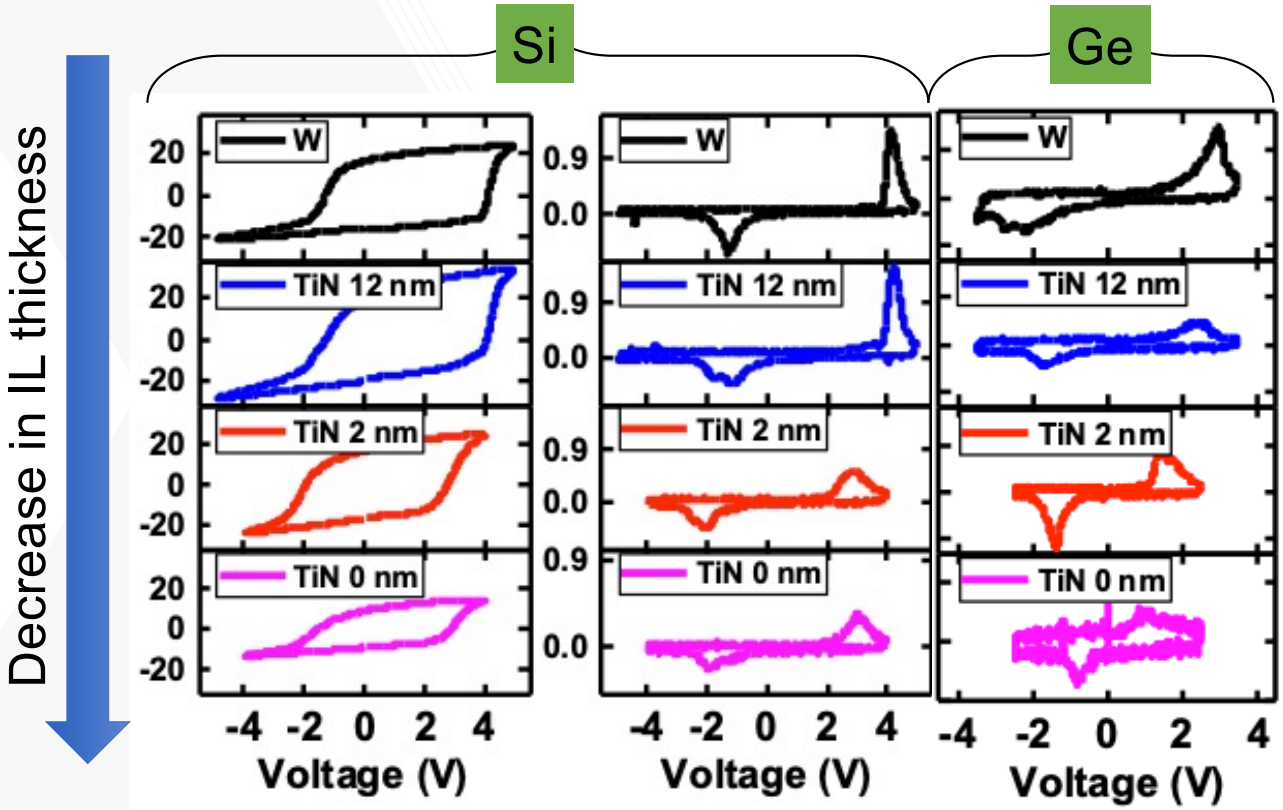
Park et al. (under review)

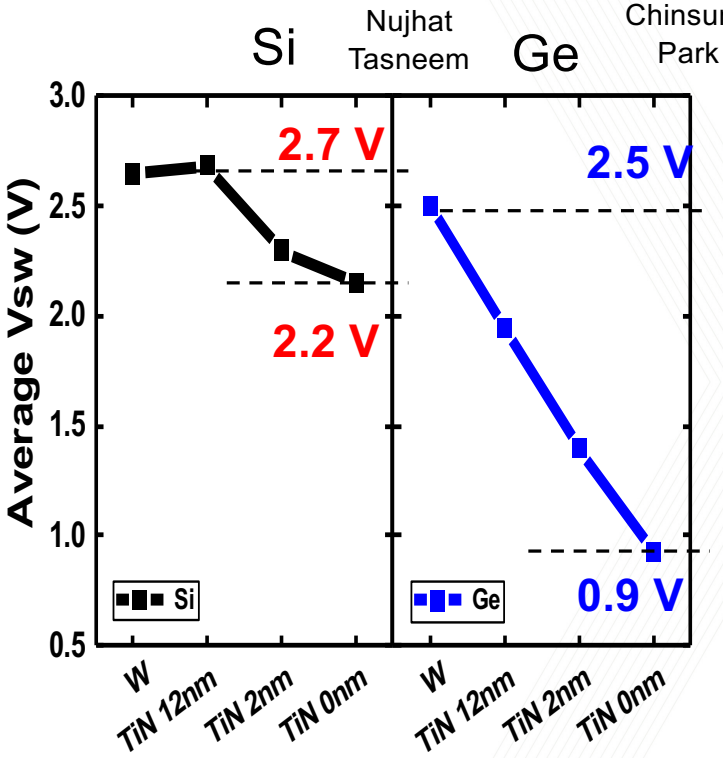
Remote oxygen scavenging can result in controllable IL thickness.

The effect of the IL thickness on Vc

Nujhat Tasneem

Chinsung Park





Dramatic reduction in coercive voltage is observed in Ge platform with the change of the gate metal stack.

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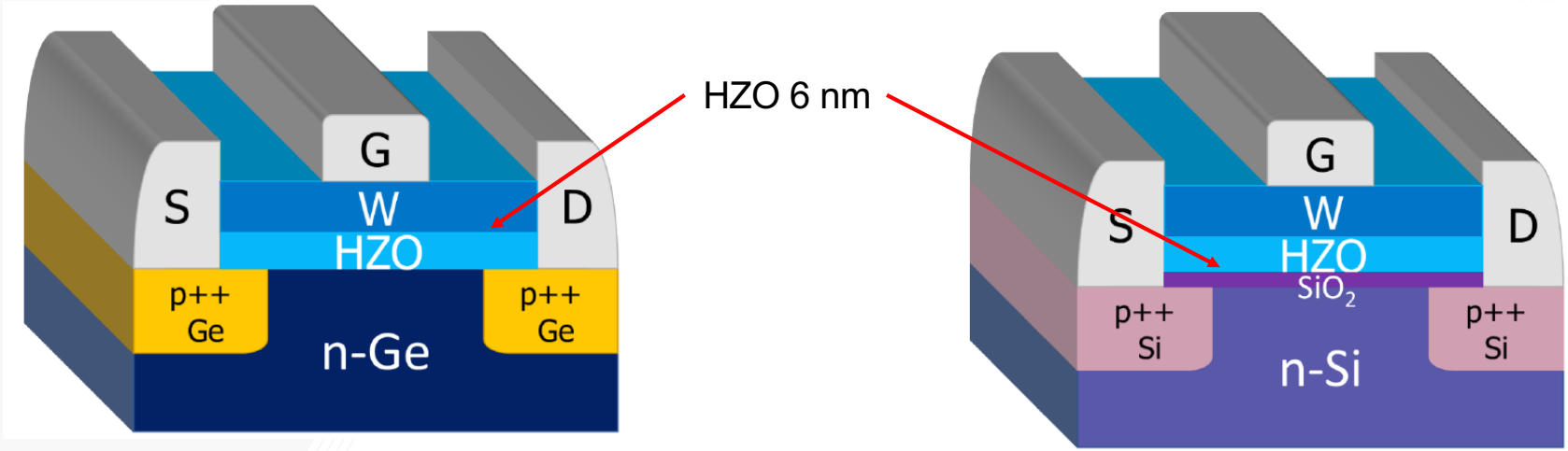
Ge-channel FEFETs with record-low write voltages



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Si and Ge-channel FEFETs fabricated with the same 6 nm HZO layers, under similar process and fabrication conditions.

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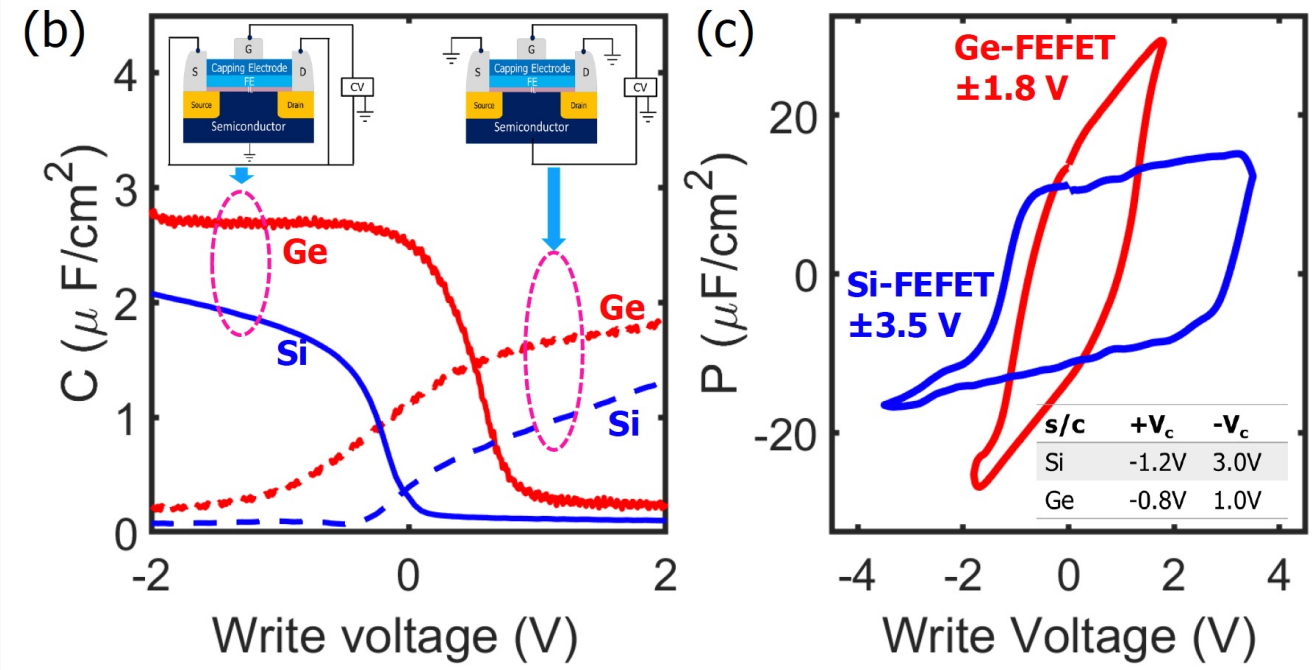
Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

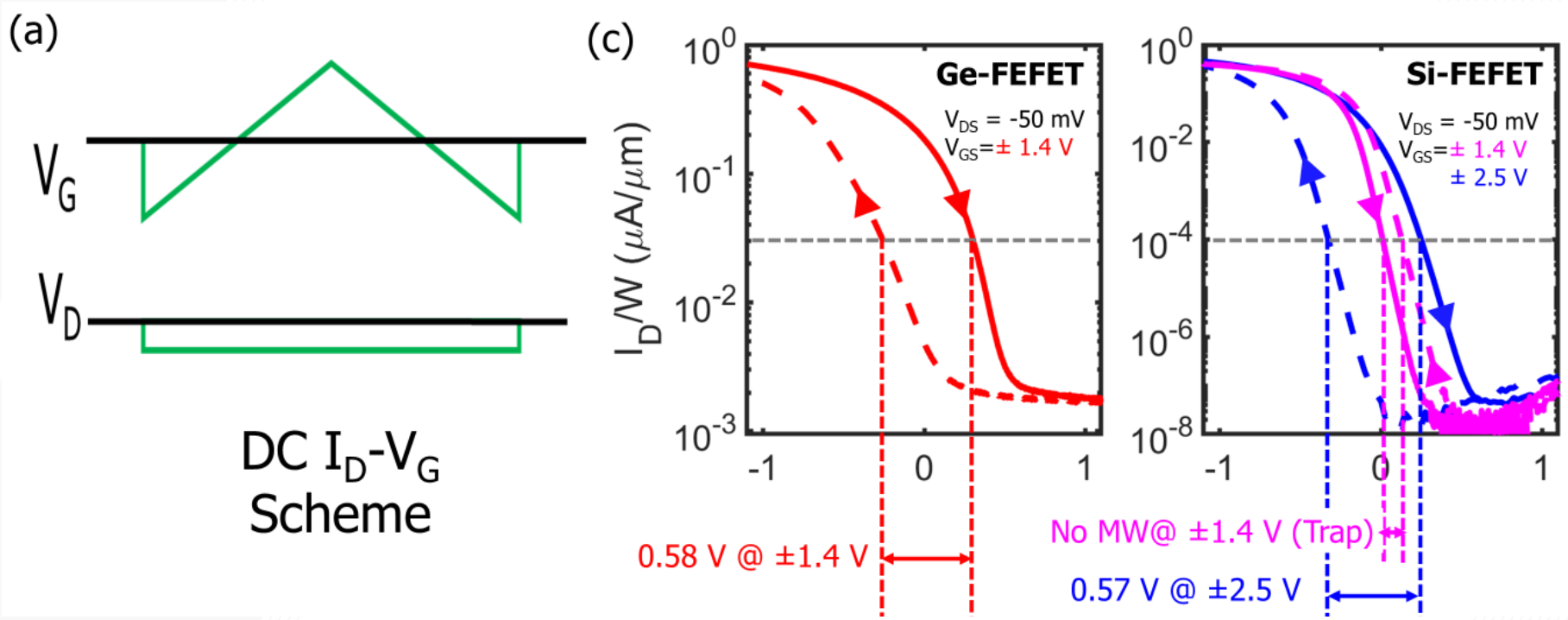
Ge-channel FEFETs with record-low write voltages



Significant increase on the on-capacitance and reduction in coercive voltage in Ge-channel FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

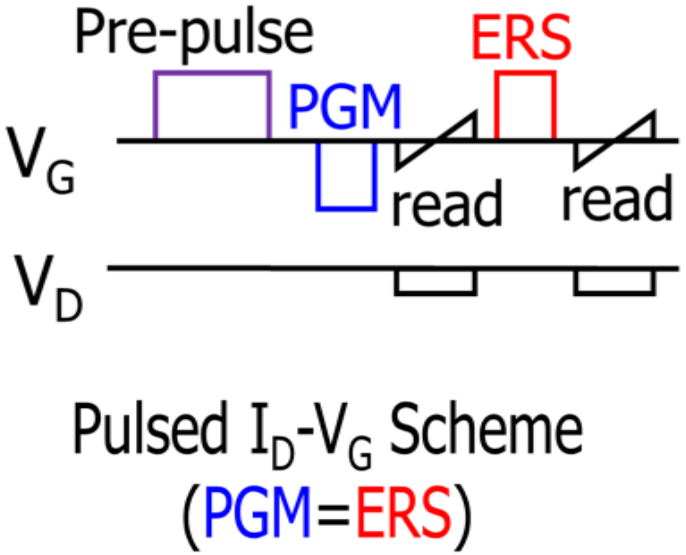
DC I_D-V_G characteristics

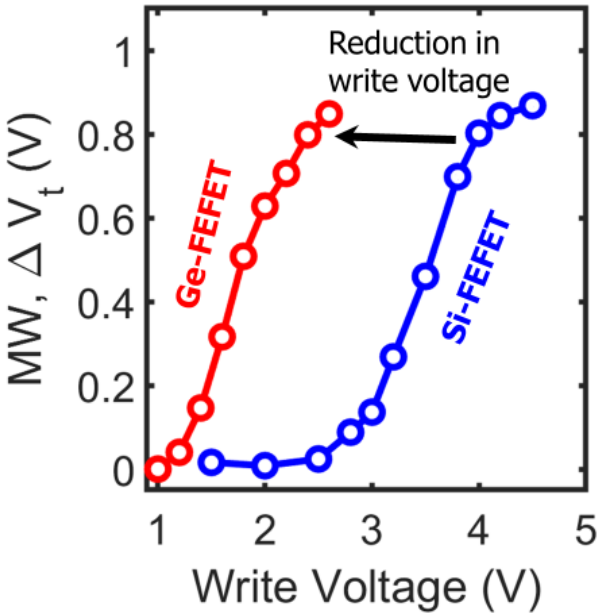


Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Pulsed I_D-V_G characteristics



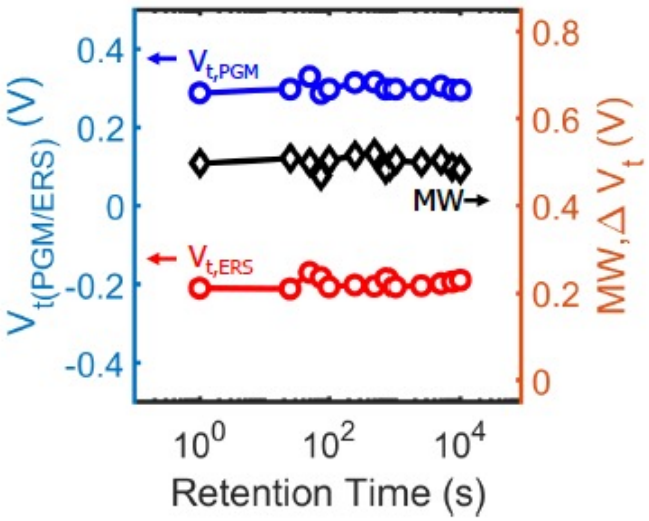


Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

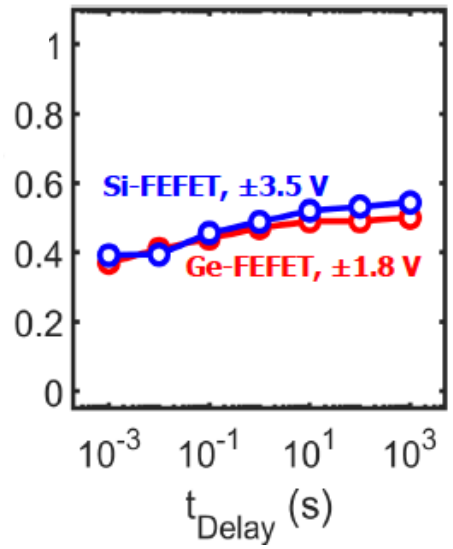
Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Retention, endurance and read-after-write delay

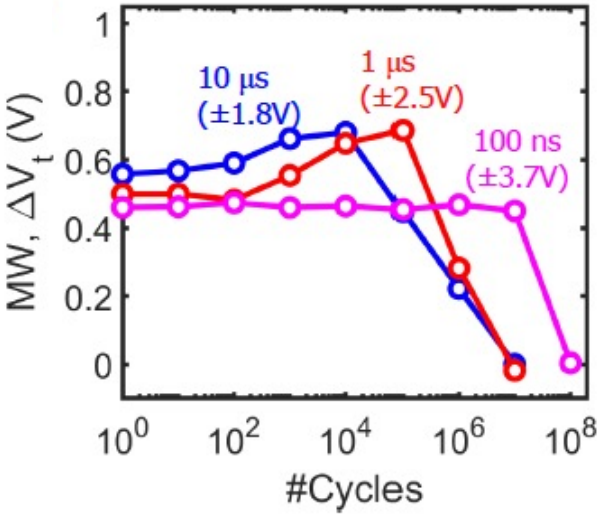
Retention



Read-after-write delay



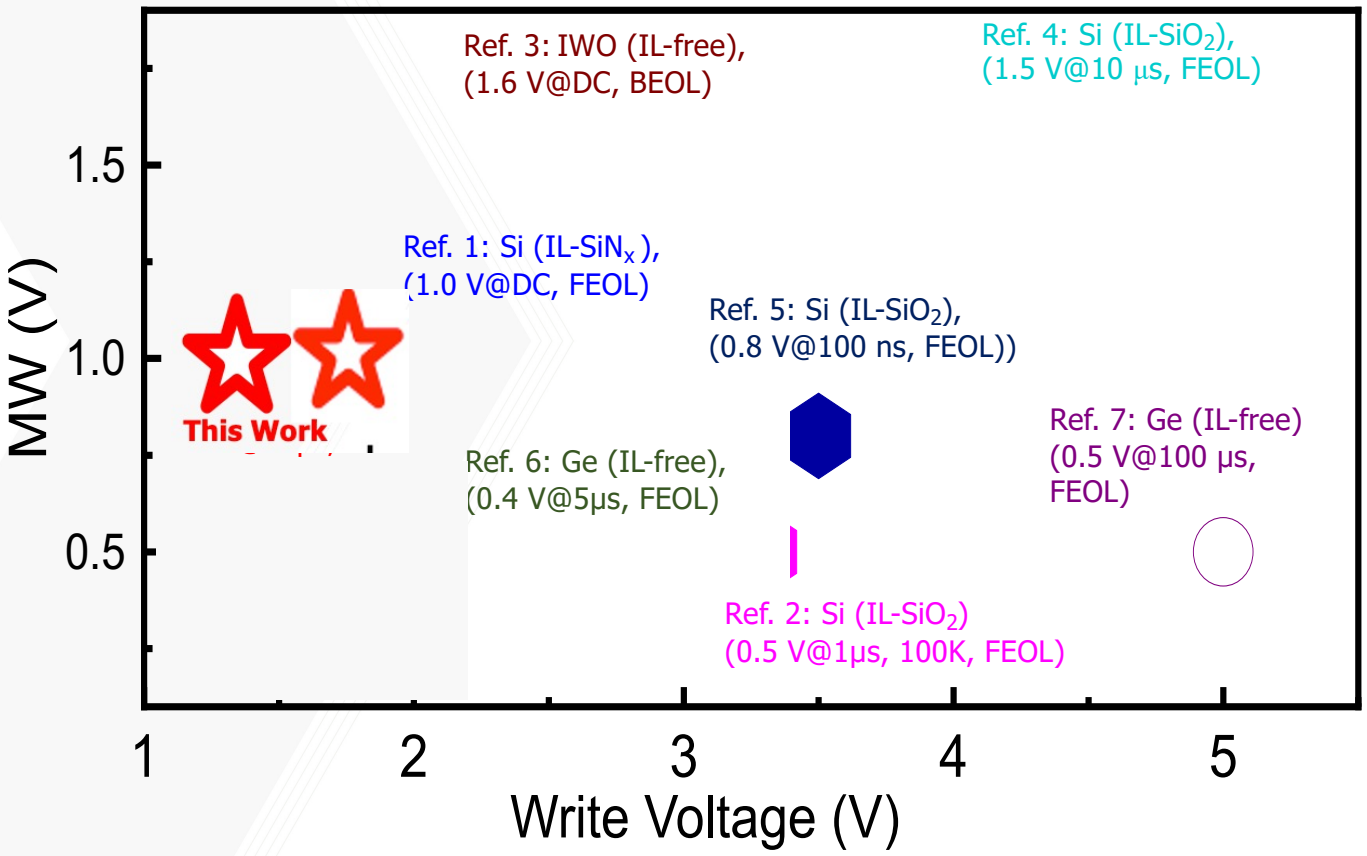
Endurance



The Ge-FEFET show write endurance of 107 cycles, excellent data retention and immediate read-after-write capability.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Benchmarking Memory Window v. Write Voltage Tradeoff



Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

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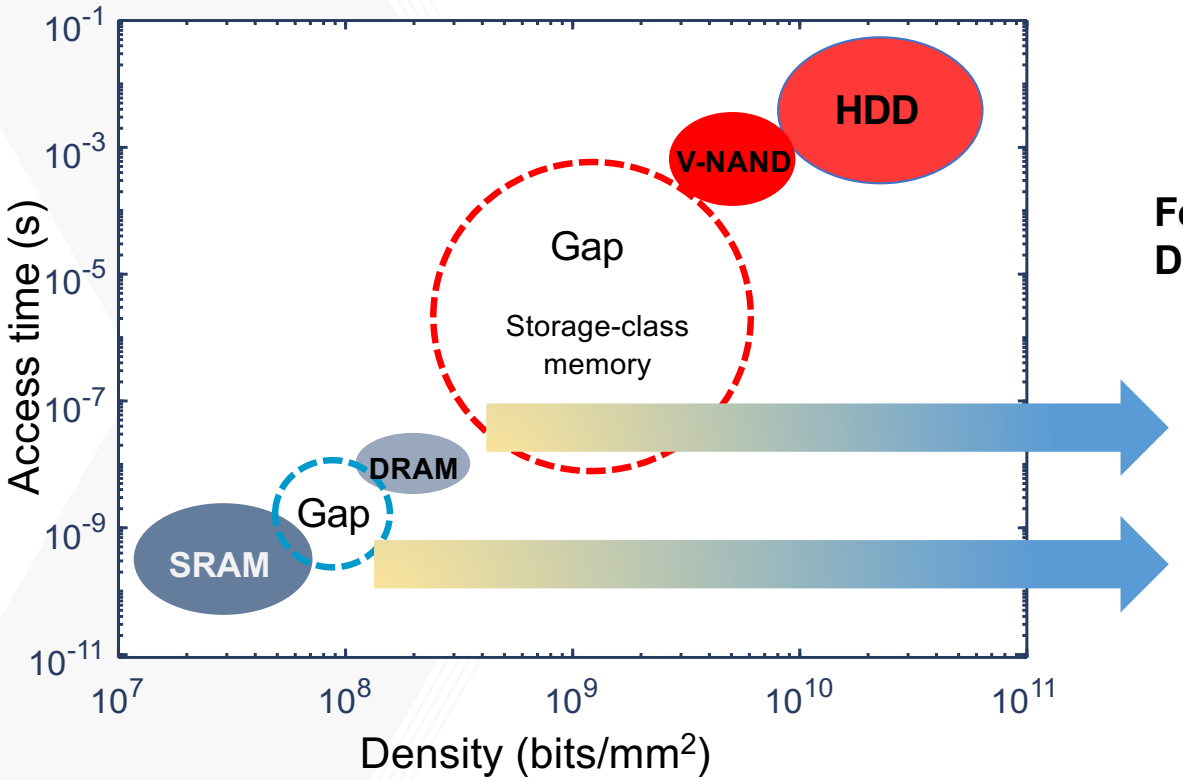
Ferroelectrics for memory and storage

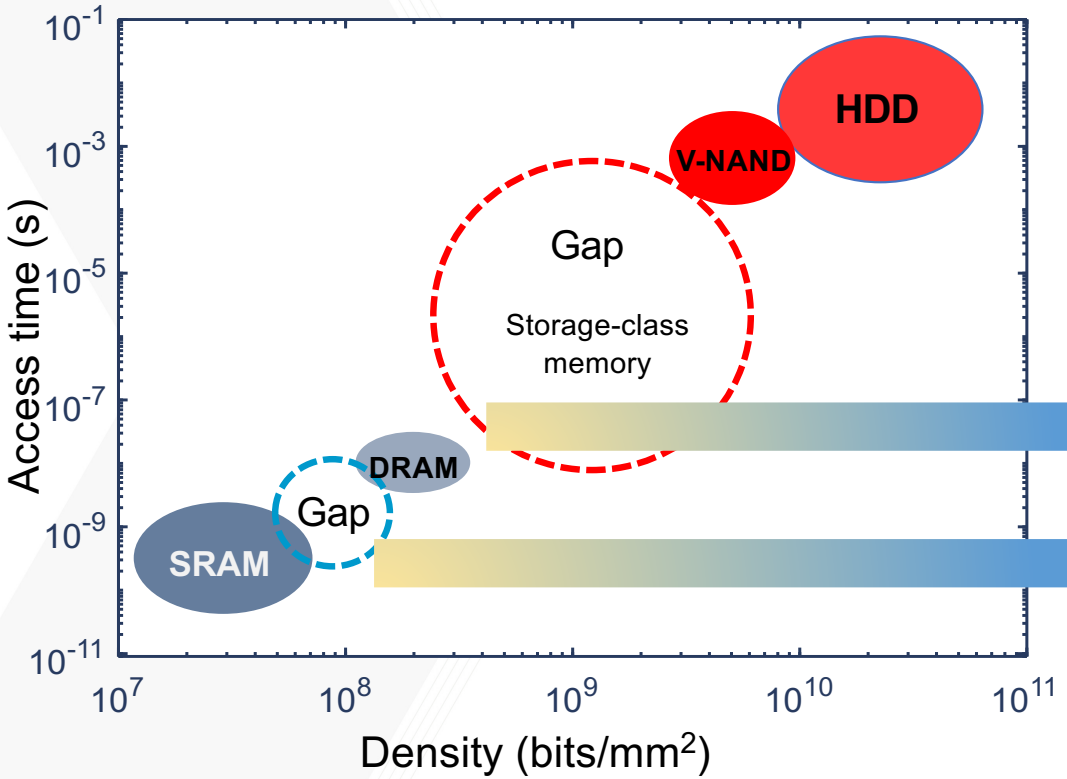


Ferroelectrics for the DRAM/Storage class space

Ramaswamy et al. Micron, IEDM 2024
Dual Layer 3-D stacked FRAM
Capacity – 32 Gb (Sk Hynix DRAM –-8 Gb)
Latency – 180 ns (LPDDR5 – 60 ns)
Density – 450 Mb/mm^2

Ferroelectrics for embedded memories/cache?

Ferroelectrics for memory and storage



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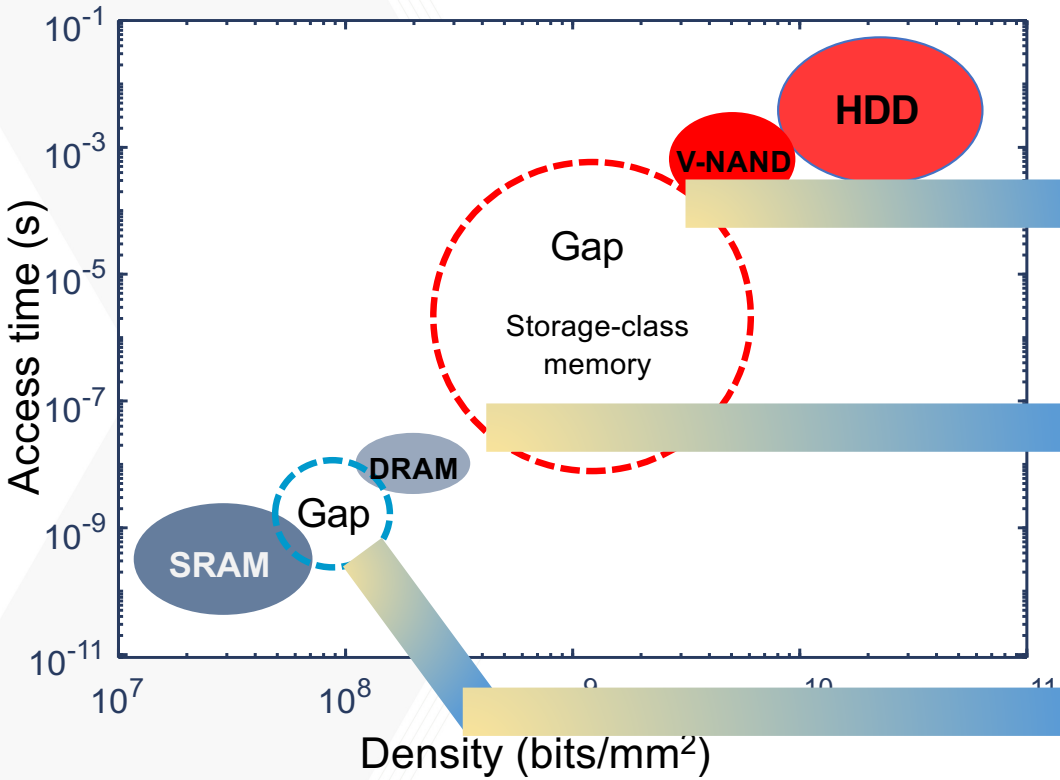
Ferroelectrics for embedded memories/cache

- Density
- BEOL compatibility
- Fast

	Cell area | Speed
DRAM:	6-30F^2 | <10 ns
FEFET:	**5-10F^2 | 5-10 ns**
SRAM:	140-280F^2 | <1 ns

Ferroelectrics for memory and storage



Ferroelectrics for flash?

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Ferroelectrics for embedded memories/cache

- Density
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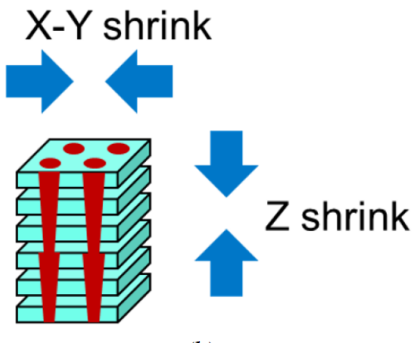
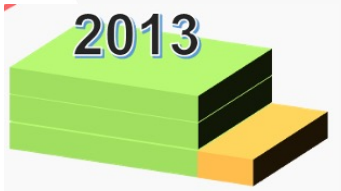
Vertical NAND Scaling

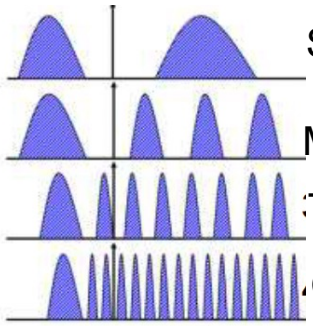
Physical scaling

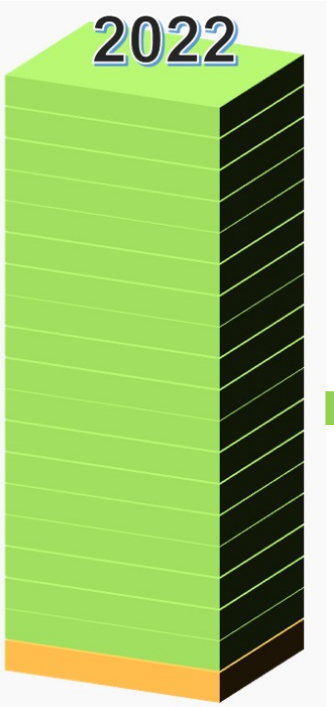




Samsung 24L MLC

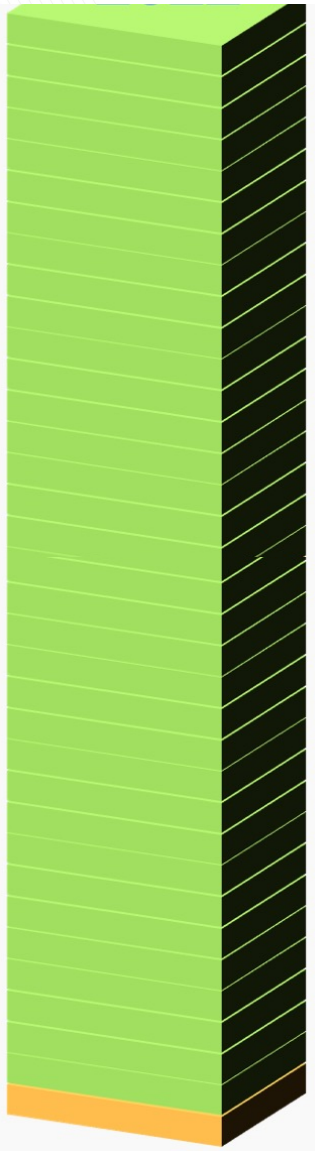
Logical scaling





Samsung 236L TLC
SK Hynix 238L TLC
Micron 232L TLC
192L QLC

?



Vertical NAND scaling toward 1000 layers

Layer stacking trend

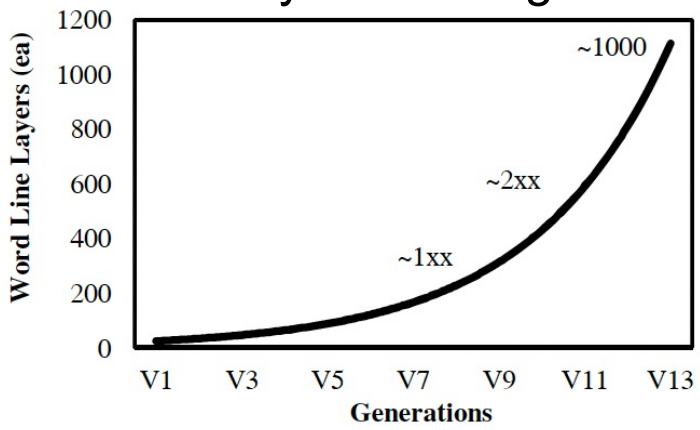


Fig. 1. Number of word line layers by generation

Package thickness limits the NAND chip height.

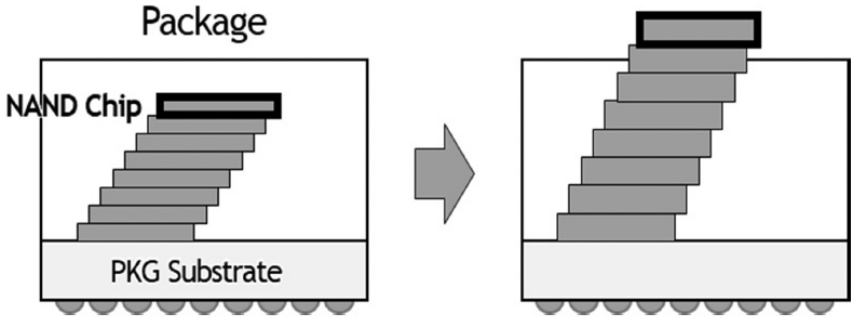
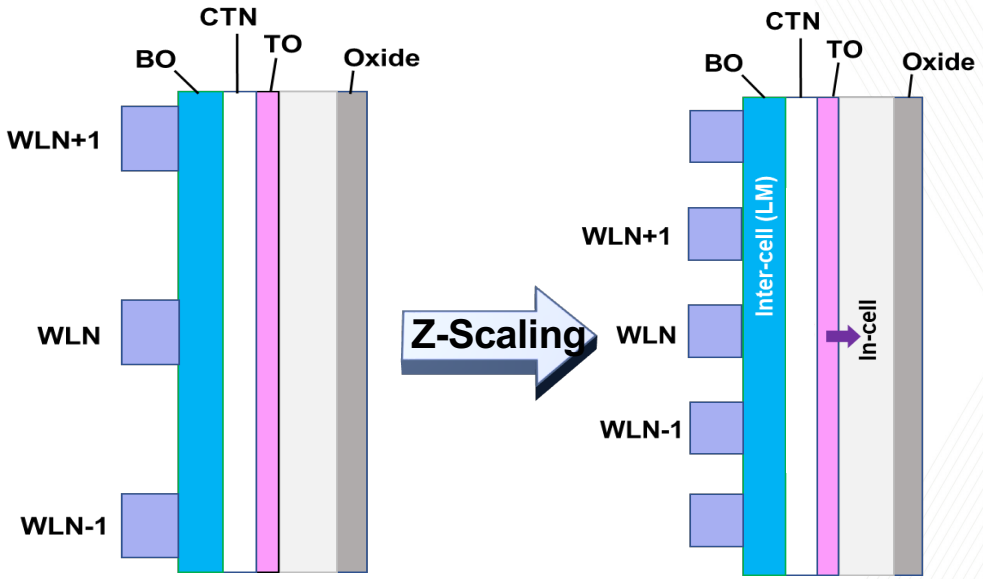


Fig. 4. Package thickness limit with multiple chips

Aggressive Z-scaling is required.

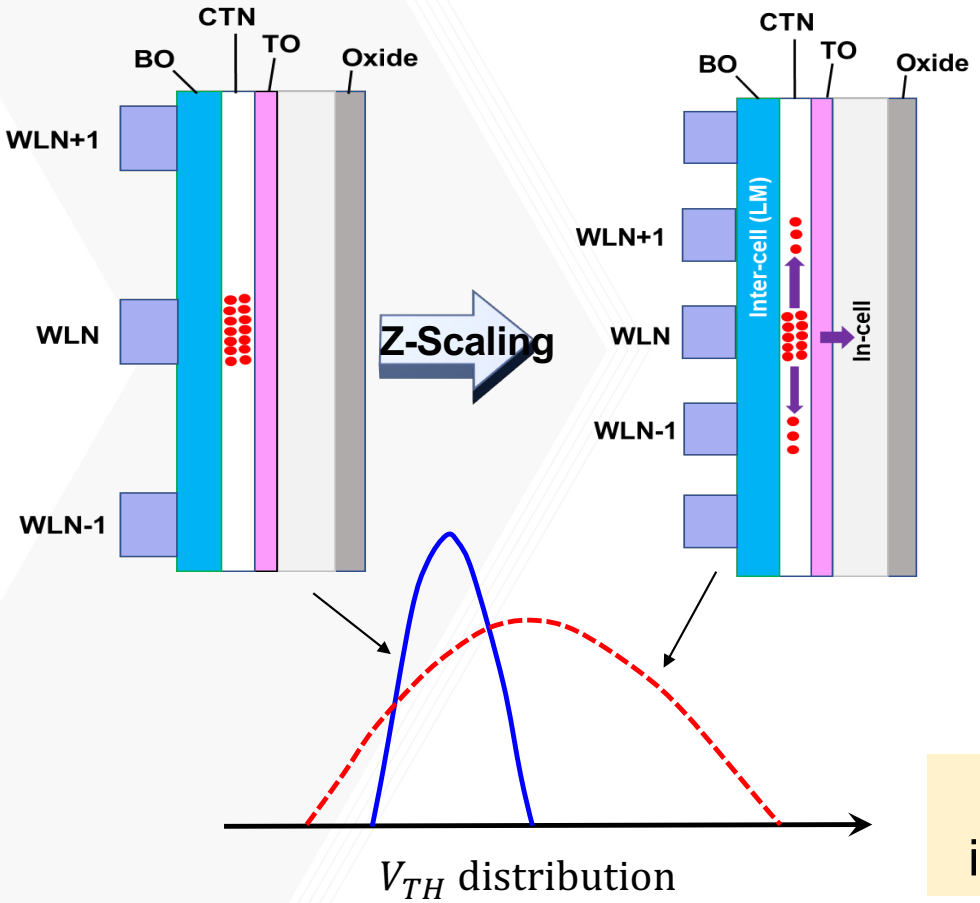


The mold height (cell height) needs to be reduced dramatically.

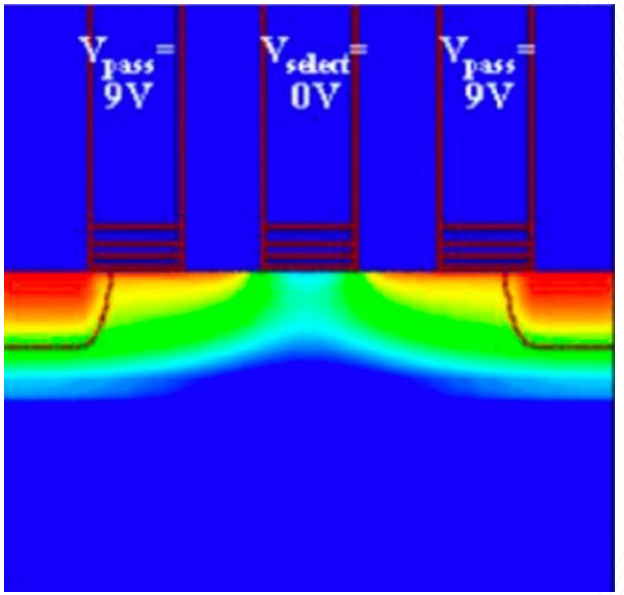
Han et al. Fundamental Issues in VNAND Integration Toward More Than 1K Layers. IEDM 2023. Paper 35.1

Challenges for 1000+ layer vertical NAND

1 Lateral charge migration



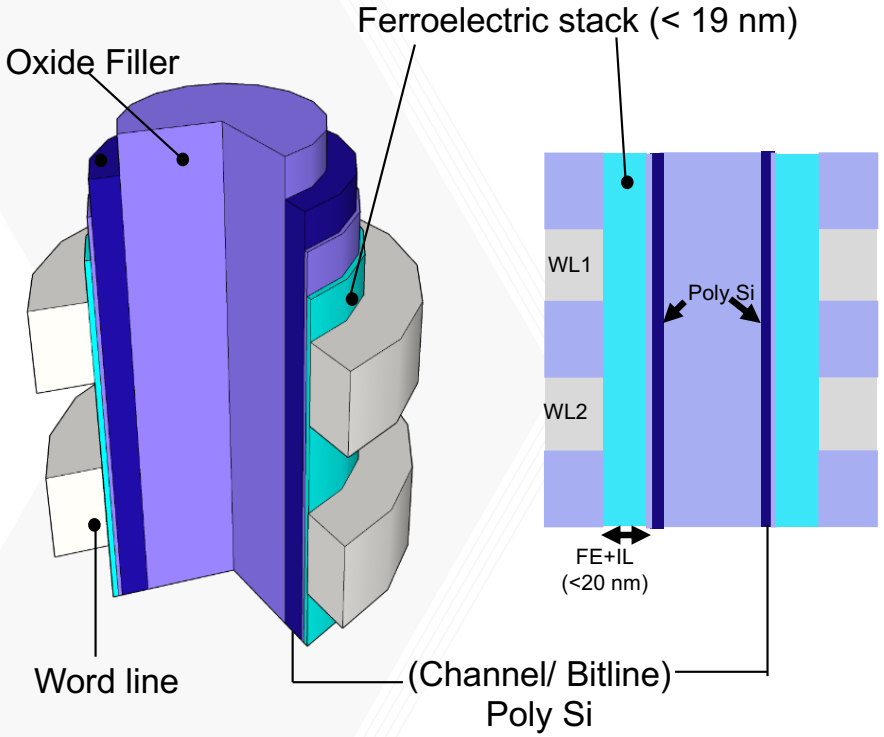
2 High write voltage



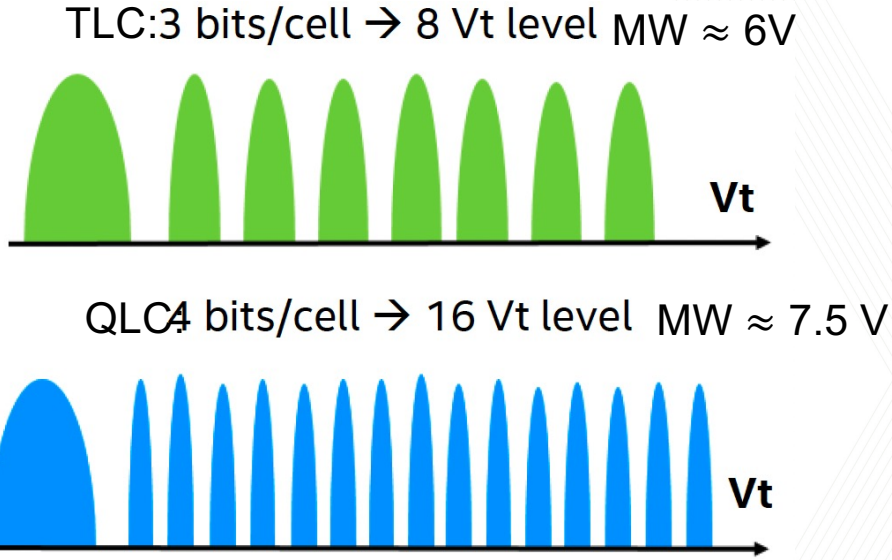
Write voltage of state of the art NAND is >20 V.
Large write voltage affects effective threshold voltage, similar to cell-to-cell interference.

Cell-to-cell interference will significantly increase with aggressive Z-scaling for 1000L VNAND.

Ferroelectric as a replacement for Charge Trap Layer



To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm



Design constraints

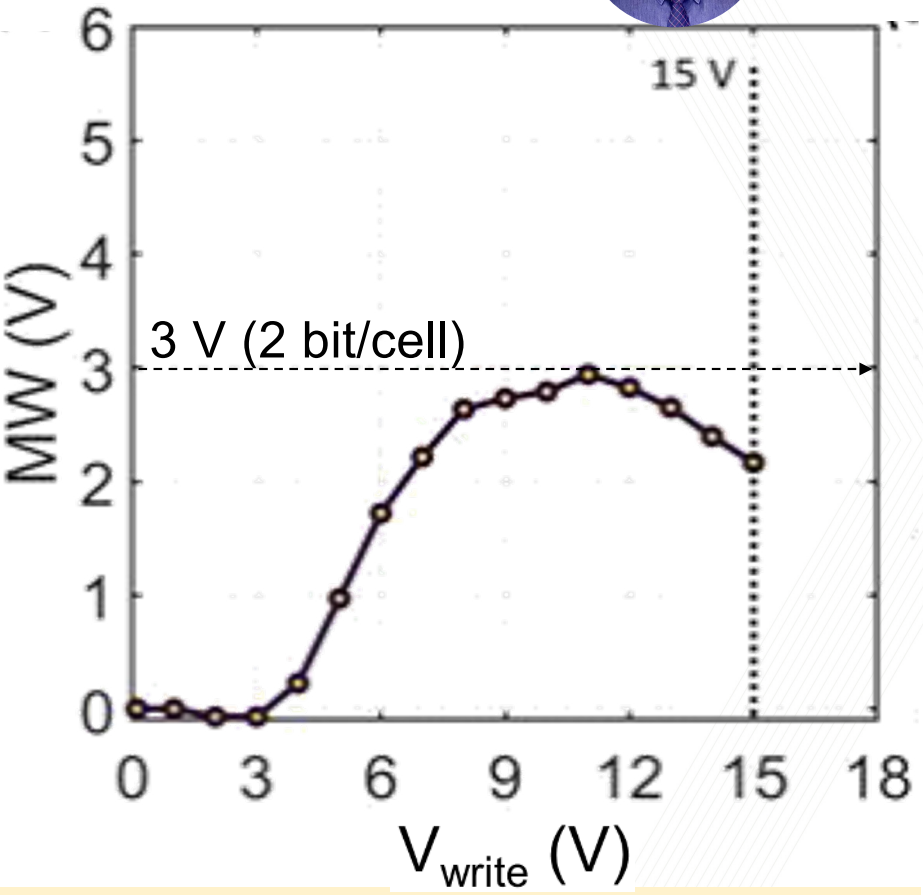
Ferroelectric thickness, $t_{FE} \leq 19$ nm

Write voltage ≤ 15 V

Memory window, MW > 6.5 V

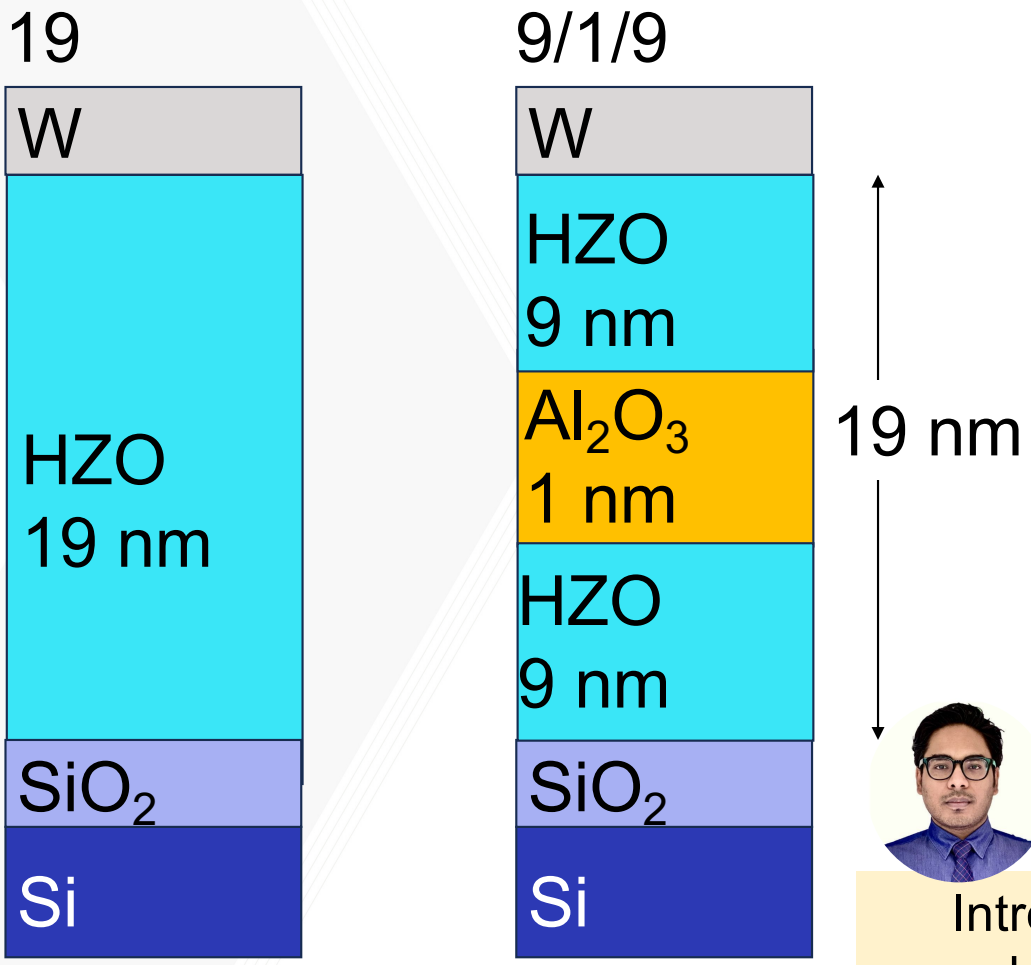
Impact of tunnel dielectric insertion

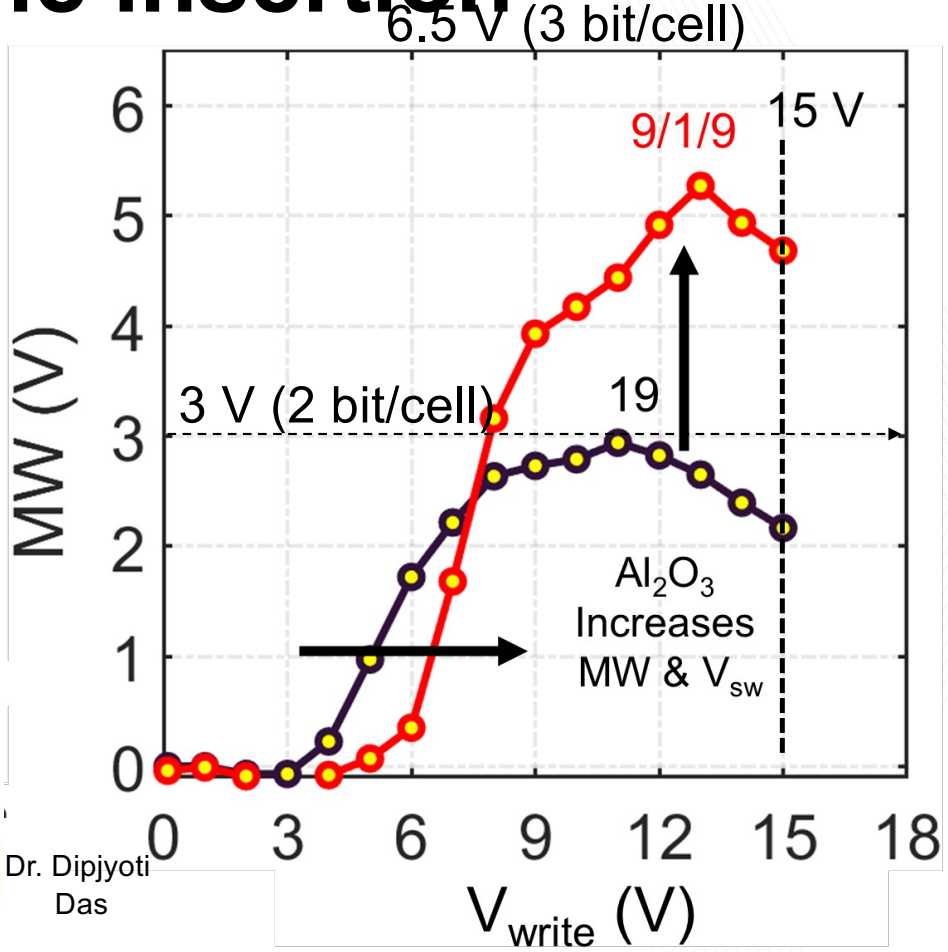
Dr. Dipjyoti Das



10 nm HZO layer leads to maximum memory window of 2.9 V.

Impact of tunnel dielectric insertion

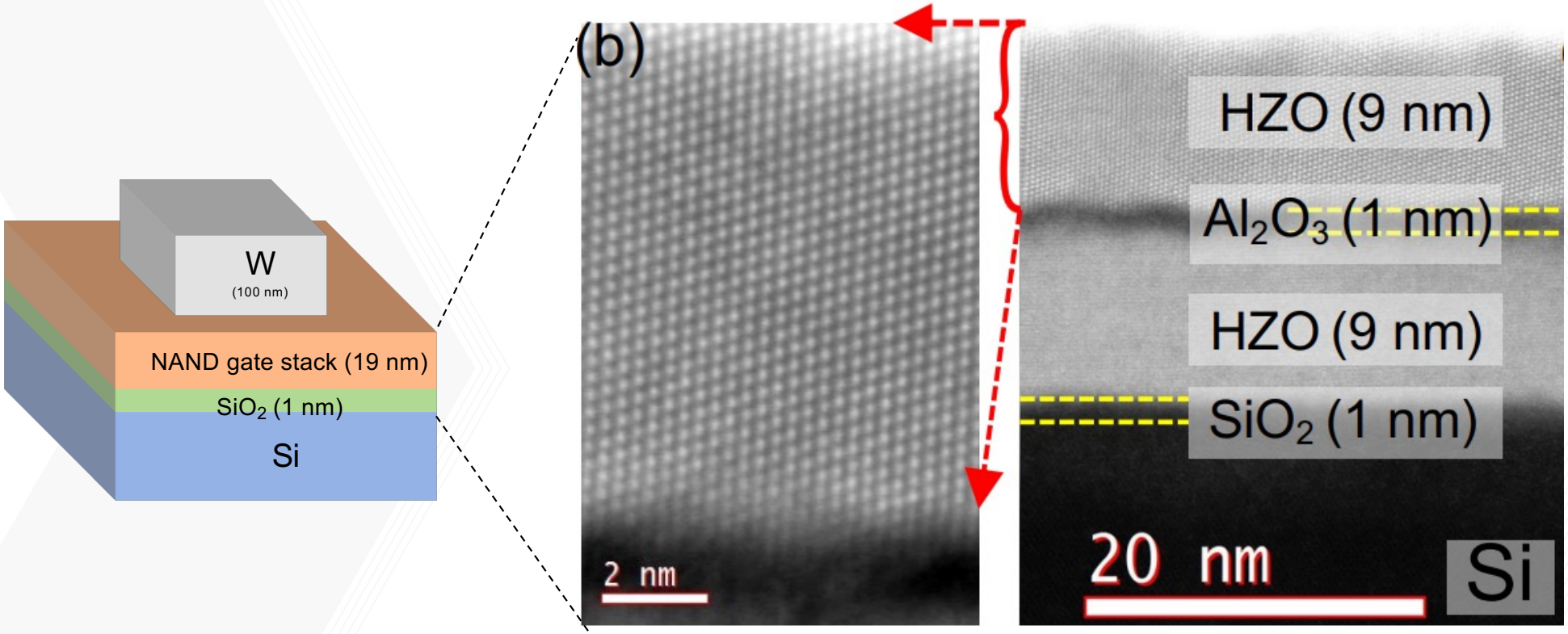




Dr. Dipjyoti Das

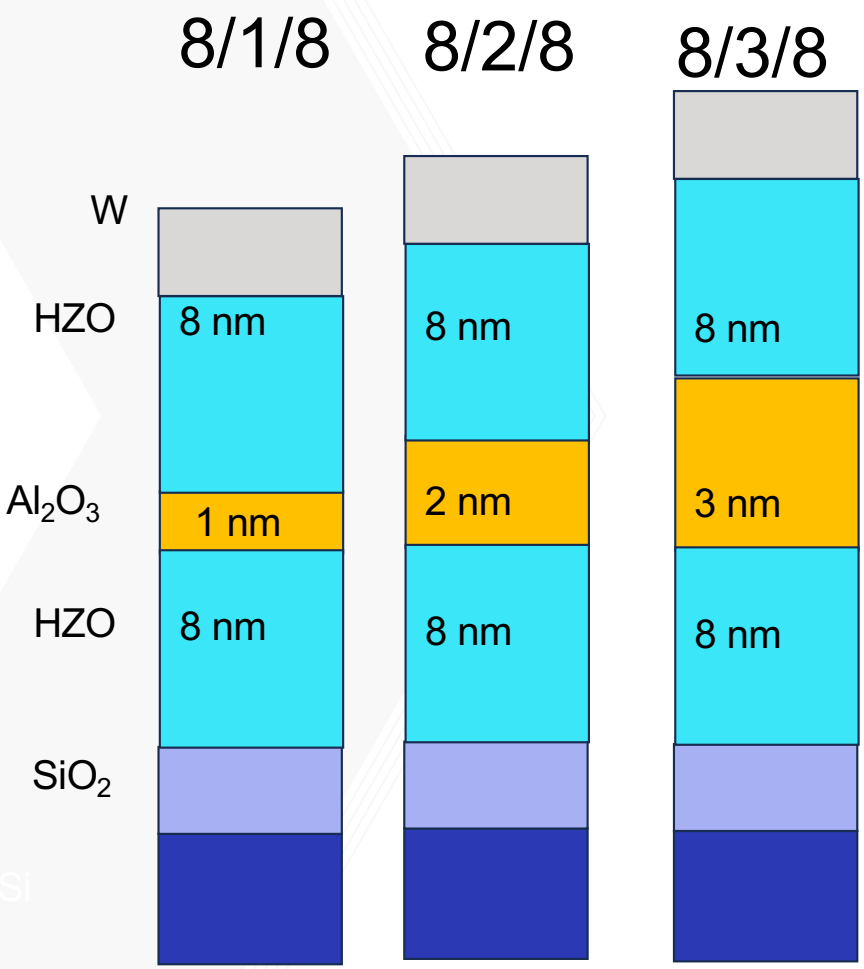
Introducing 1 nm Al_2O_3 intermediate layer dramatically memory window to 5.3 V.

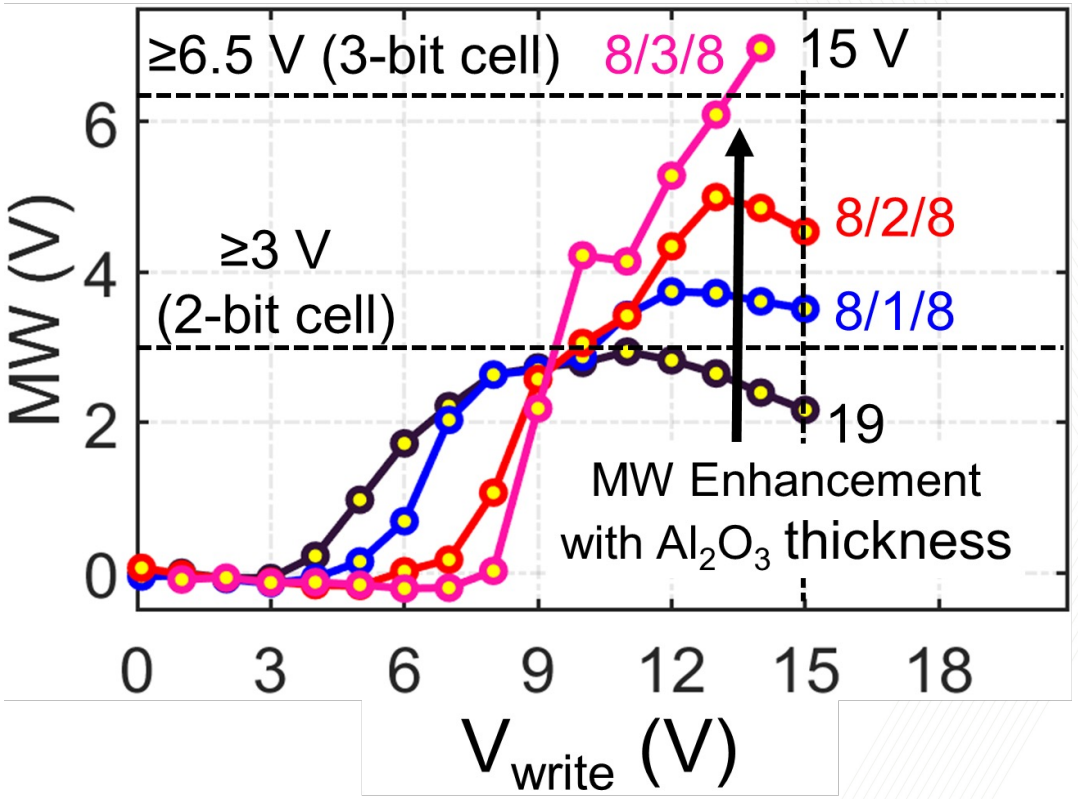
Impact of tunnel dielectric insertion



Full coverage of 1 nm Al_2O_3 is observed.

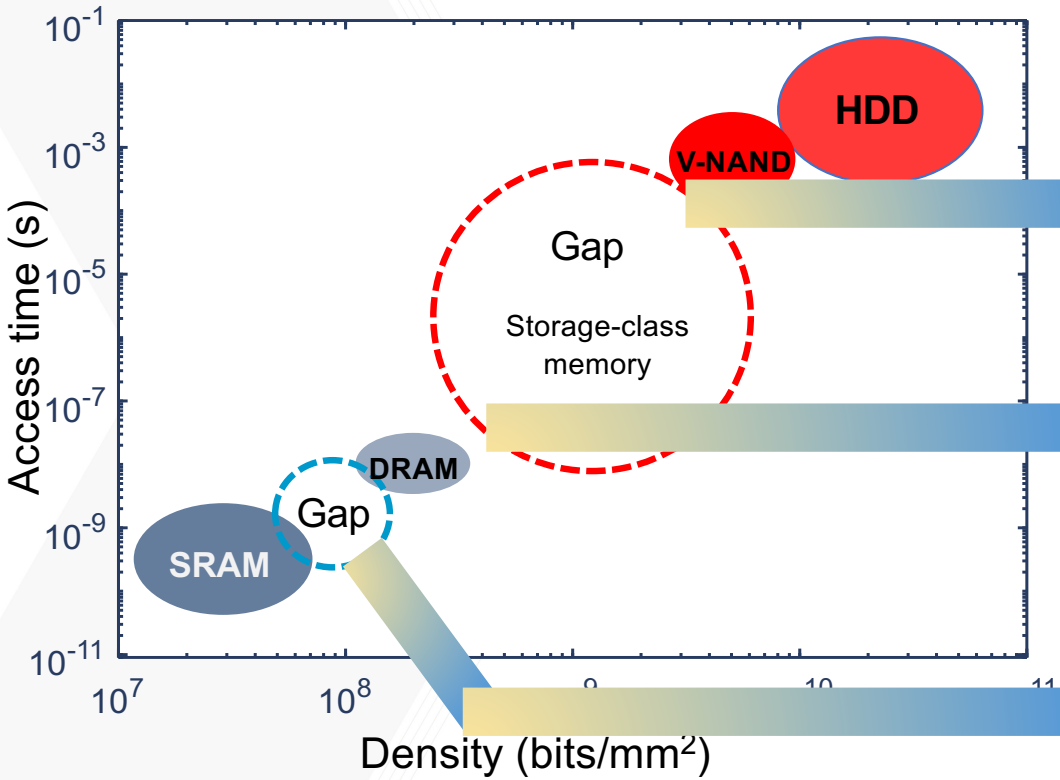
Impact of tunnel dielectric insertion





FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

Ferroelectrics for memory and storage



Ferroelectrics for flash?

Ferroelectrics for the DRAM/Storage class space

Ramaswamy et al. Micron, IEDM 2024
Dual Layer 3-D stacked FRAM
Capacity – 32 Gb (Sk Hynix DRAM –-8 Gb)
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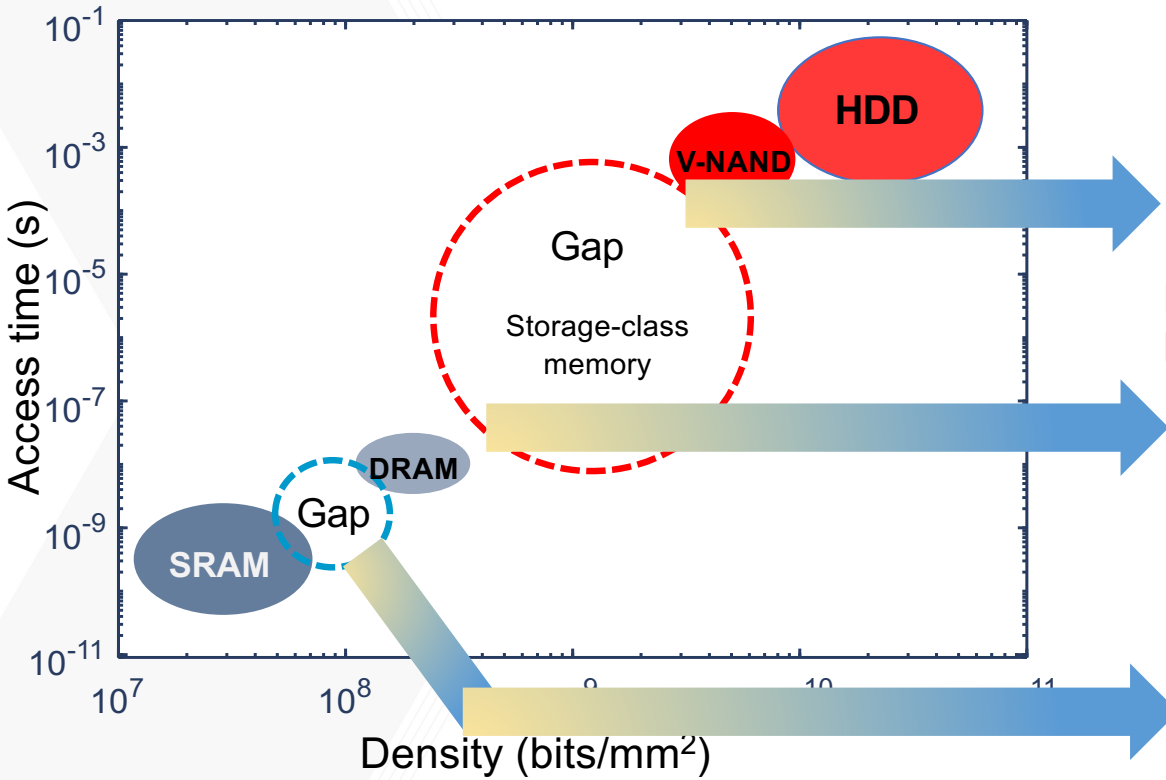
Density – 450 Mb/mm^2

Ferroelectrics for embedded memories/cache

- Density
- BEOL compatibility
- Fast

Ferroelectrics for memory and storage



Ferroelectrics for flash

- Voltage scaling below 15 V
- Z-scaling

Ferroelectrics for the DRAM/Storage class space

Ramaswamy et al. Micron, IEDM 2024

- Dual Layer 3-D stacked FRAM
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Ferroelectrics for embedded memories/cache

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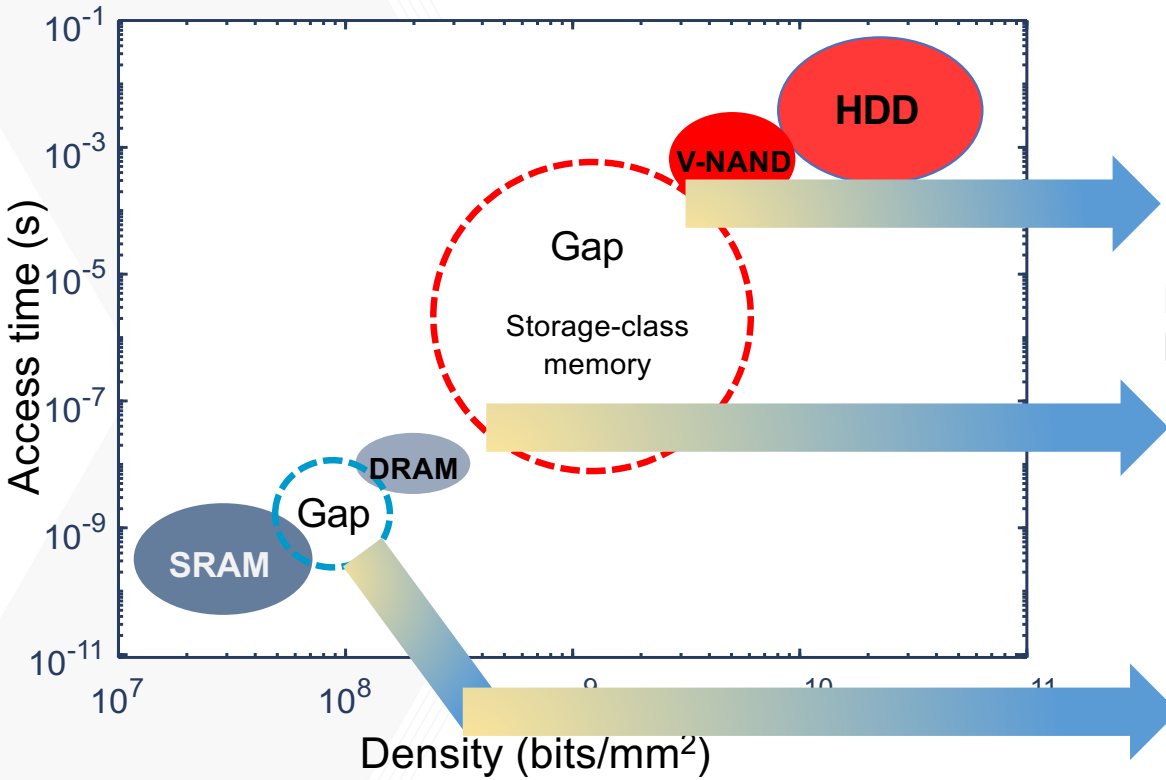
Ferroelectrics for memory and storage – Challenges



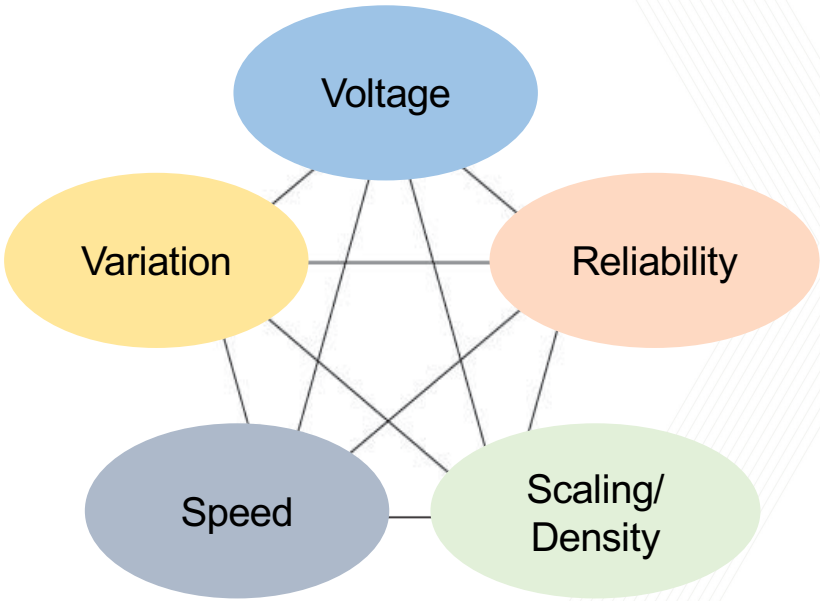
Ferroelectrics for flash
- Disturb

Ferroelectrics for the DRAM/Storage class space
- Voltage and speed

Ferroelectrics for embedded memories/cache
- Voltage and speed

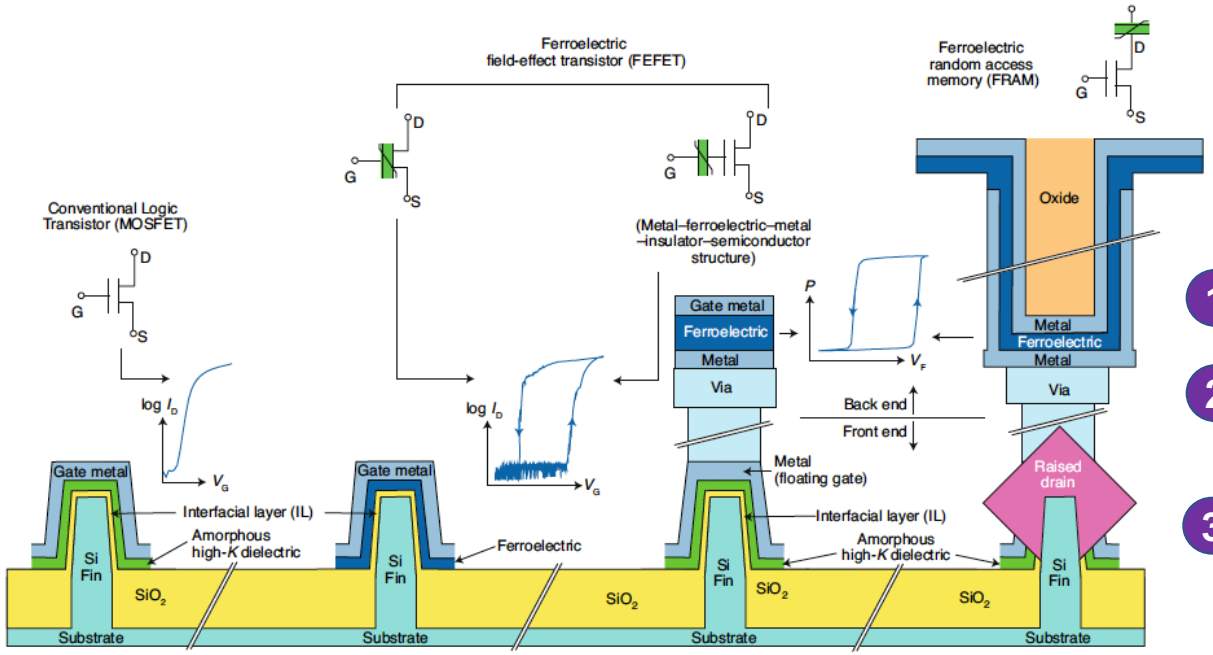
Fundamental questions according to Asif Khan

1. What is(are) the switching paths?
2. What is the nature of the grain boundaries?
3. What controls the microstructure in poly-X heterostructures?
4. What is the nature of interfaces in poly-X heterostructures?



The era of ferroelectronics

The next wave of exponential growth of the semiconductor industry depends on how well the electronic hardware can support the explosion of data-centric computing.



Ferroelectric technology will be a key component because of

1. Performance
2. Energy and area efficiency
3. Logic and memory functionalities

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

Forbes

Artificial General Intelligence (AGI) And The Coming Wave

Randy Bean Contributor

Randy Bean is a noted Author, Speaker, Founder, CEO, & Senior Advisor.

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