

Outlook and Prospects of Ferroelectric Memories

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Our team



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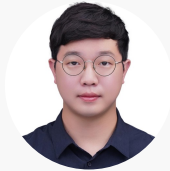
Priyanka
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Gaskell (TSMC)

Our sponsors



ChatGPT



Examples

"Explain quantum computing in simple terms"

"Got any creative ideas for a 10 year old's birthday?"

"How do I make an HTTP request in Javascript?"



Capabilities

Remembers what user said earlier in the conversation

Allows user to provide follow-up corrections

Trained to decline inappropriate requests



Limitations

May occasionally generate incorrect information

May occasionally produce harmful instructions or biased content

Limited knowledge of world and events after 2021

ChatGPT ▾

 You

Consider an n-type MOSFET with $N_A=7E18\text{ m}^{-3}$. The gate length of the MOSFET $L=2\text{ }\mu\text{m}$, width $W=12\text{ }\mu\text{m}$ and the oxide thickness $t_{ox}=8\text{ nm}$. Take $N_C=N_V=1E25\text{ m}^{-3}$, $E_G=1.12\text{ eV}$, $n_i=1.5E(16)\text{ m}^{-3}$, $kT=0.026\text{ eV}$.

Calculate the numerical values of following quantities.

- (1) $\phi_B=|E_F-E_{il}|$,
- (2) the oxide capacitance C_{ox} ,
- (3) the maximum depletion width W_{max} , and
- (4) the threshold voltage V_t .

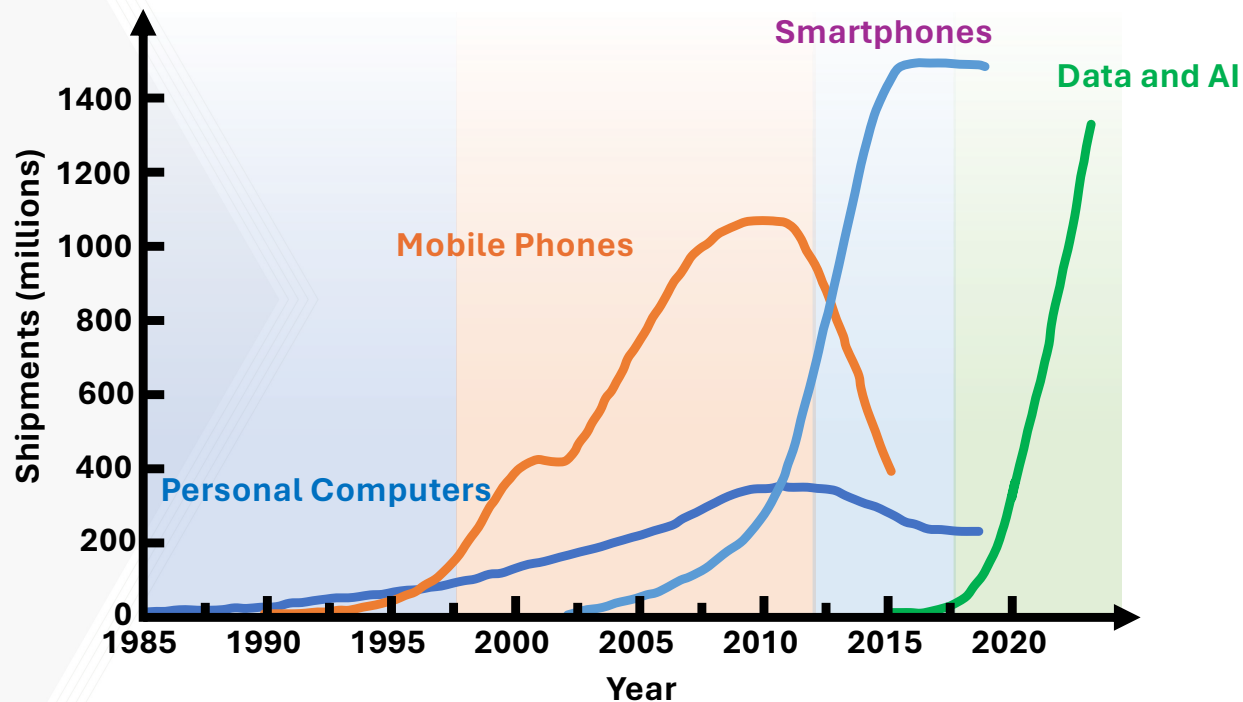
 ChatGPT

To calculate the quantities ●

Message ChatGPT...

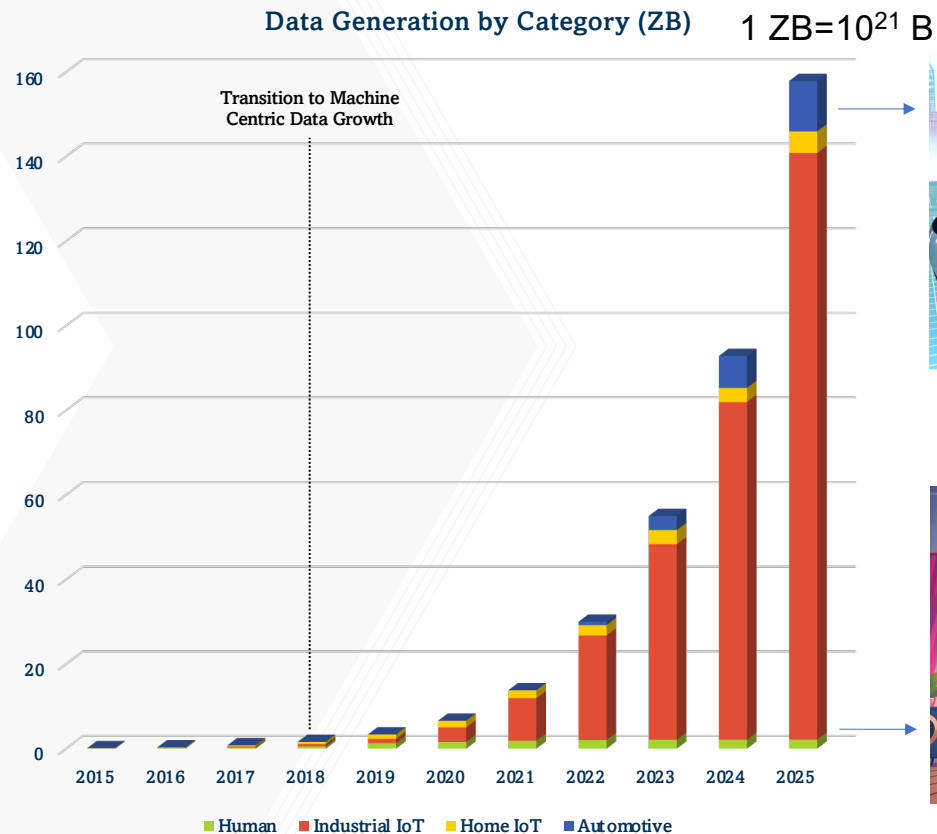


How the computing paradigms have evolved



<https://www.economist.com/briefing/2015/02/26/the-truly-personal-computer>
<https://www.statista.com/chart/12798/global-smartphone-shipments/>

The inflection of data



A connected car create up to 25 gigabytes of data per hour. That's the equivalent of nearly 30 hours of HD video playback and more than a month's worth of 24-hour music streaming.



In the year 2020, an astonishing **1.7 megabytes of data** was generated by every individual in just one second.

Projecting the future

- An overwhelming **97.2% of organizations** invest in big data and artificial intelligence.

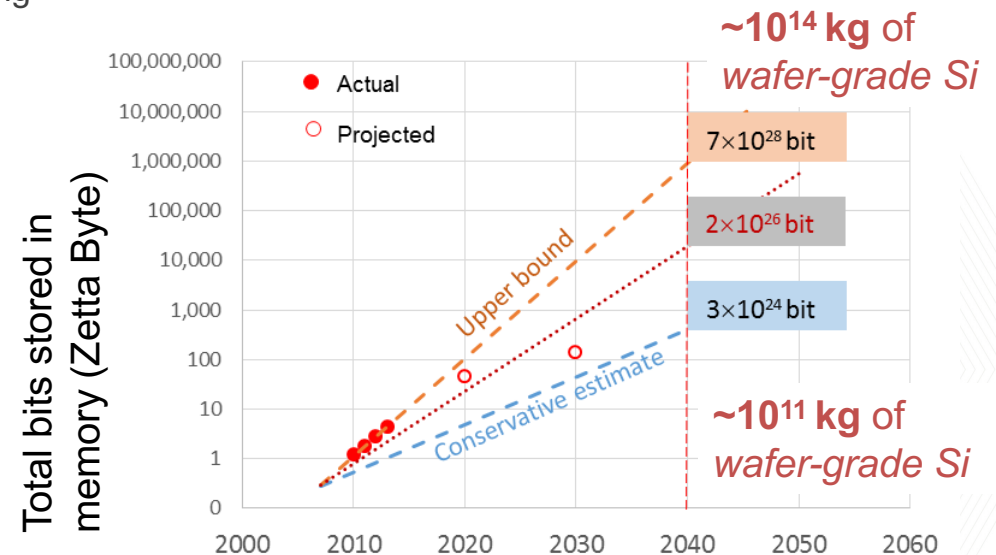
Using big data, Netflix successfully **saves \$1 billion annually** through customer retention strategies.

- Currently, the average share of IT infrastructure costs is about 3-4% of the total budget of U.S. companies, and data storage systems can account for up to 30% of total IT costs.

What if the volume of data storage goes up 100x?

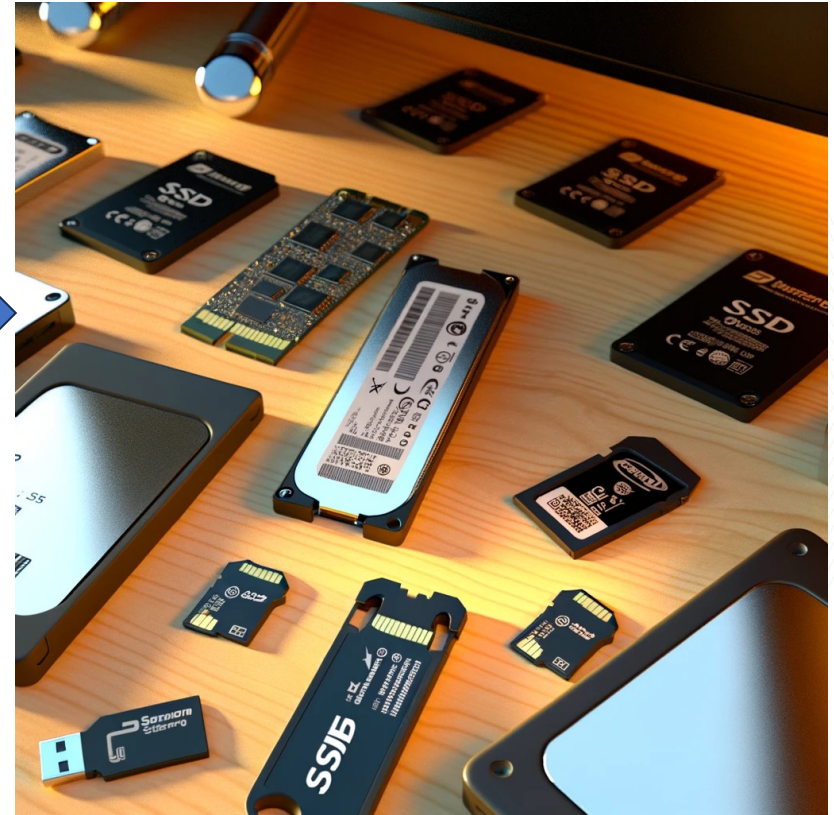
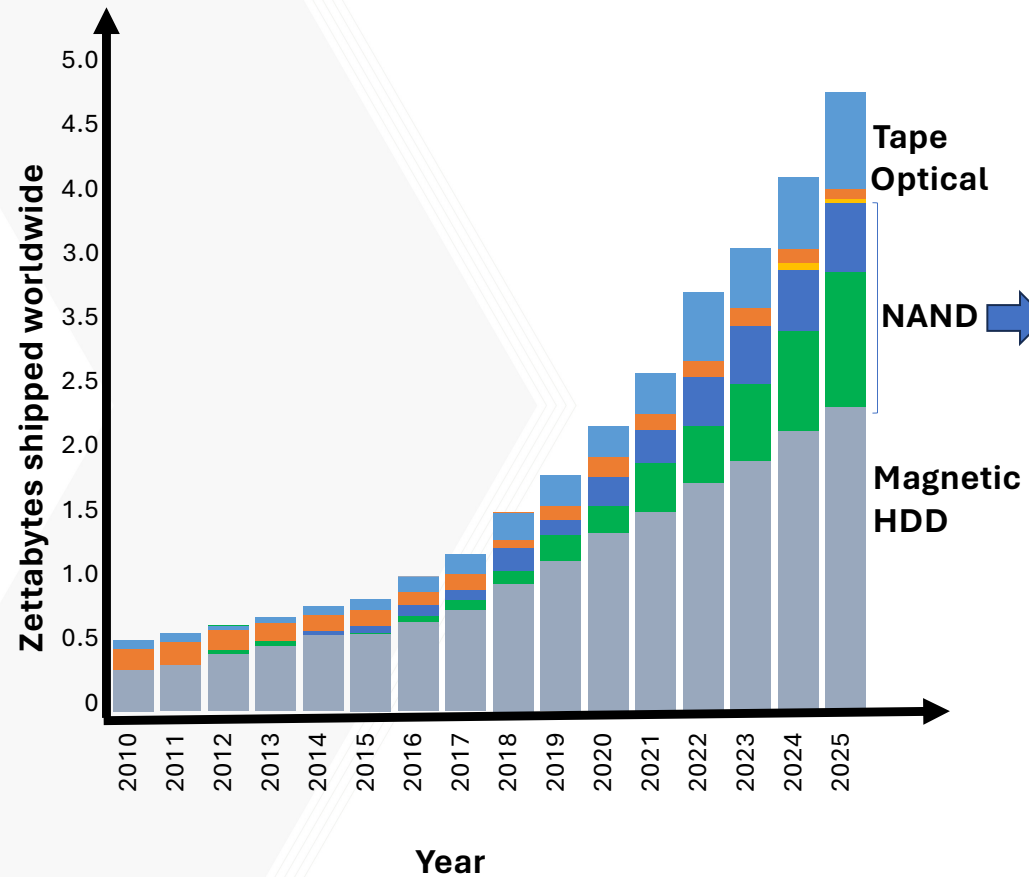
- The United States economy incurs an annual **cost of up to \$3.1 trillion** due to poor data quality.
- 80-90% of the data generated** in the modern era is unstructured.

Unstructured data repositories **hold a treasure trove** of helpful information capable of informing business decisions.

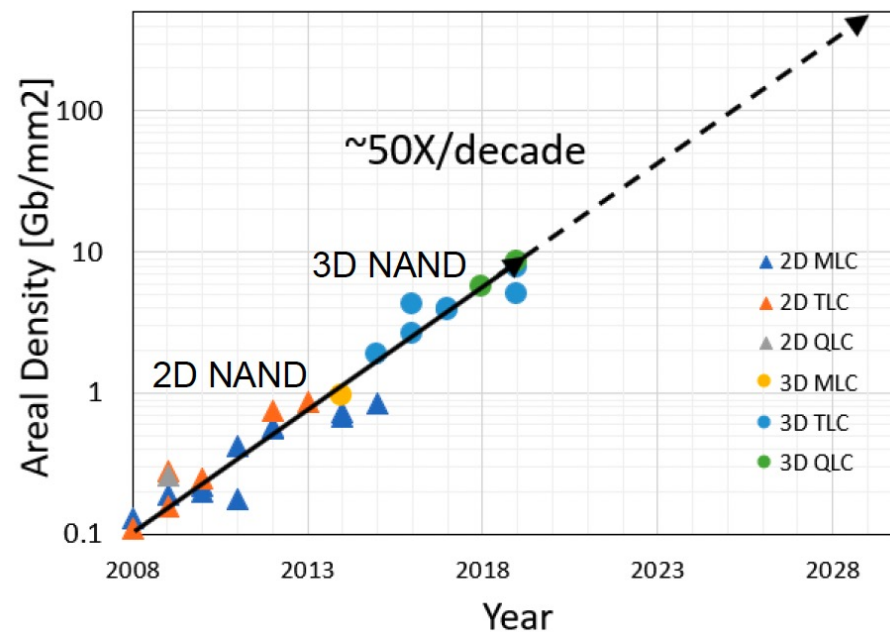
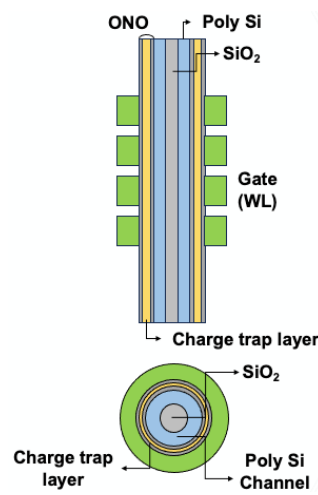
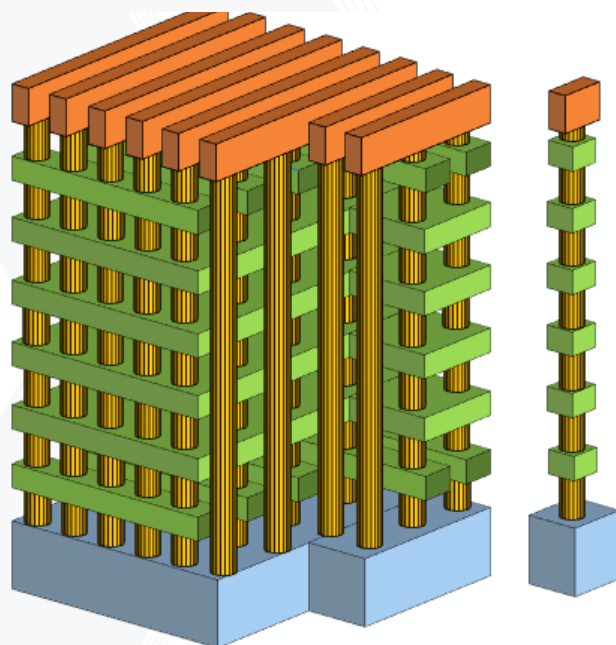


Projected annual global supply of Silicon wafers: $10^7 - 10^8$ kg in 2040

Storage Technologies



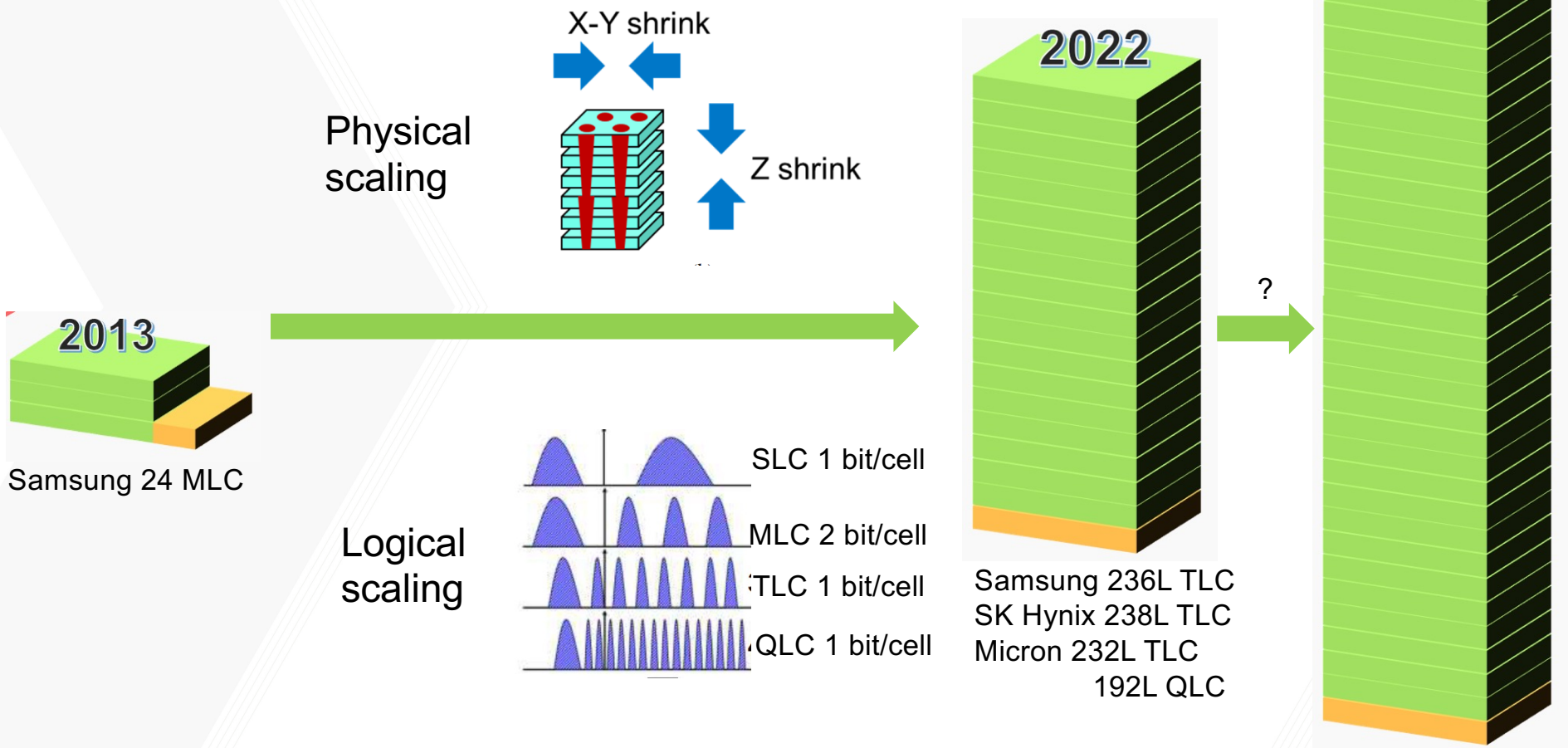
Vertical NAND Scaling



A. Goda, IEEE, TED 2020

Relentless innovations have led to a 50x improvement in bit areal density per decade.

Vertical NAND Scaling



Vertical NAND Scaling

Layer stacking trend

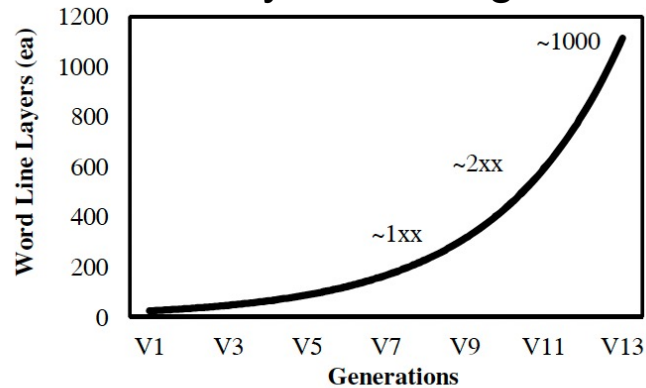


Fig. 1. Number of word line layers by generation

Package thickness limits the NAND chip height.

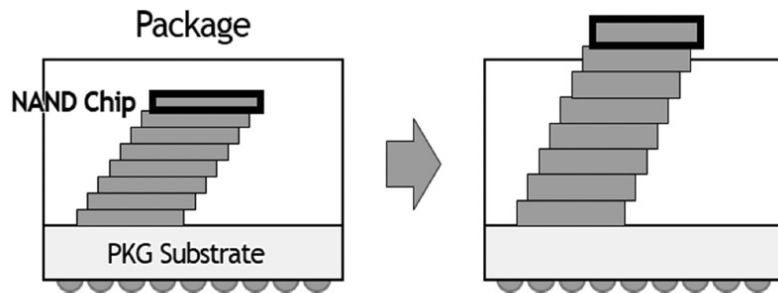
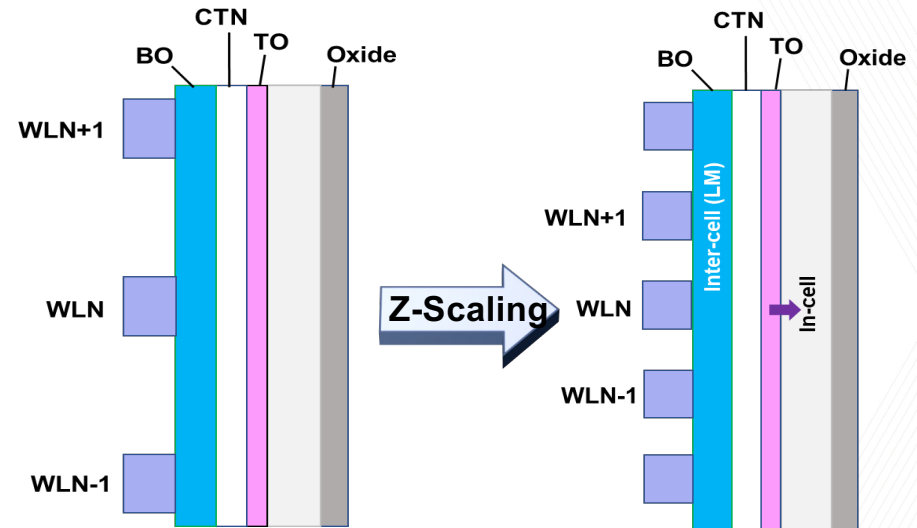


Fig. 4. Package thickness limit with multiple chips

Aggressive Z-scaling is required.

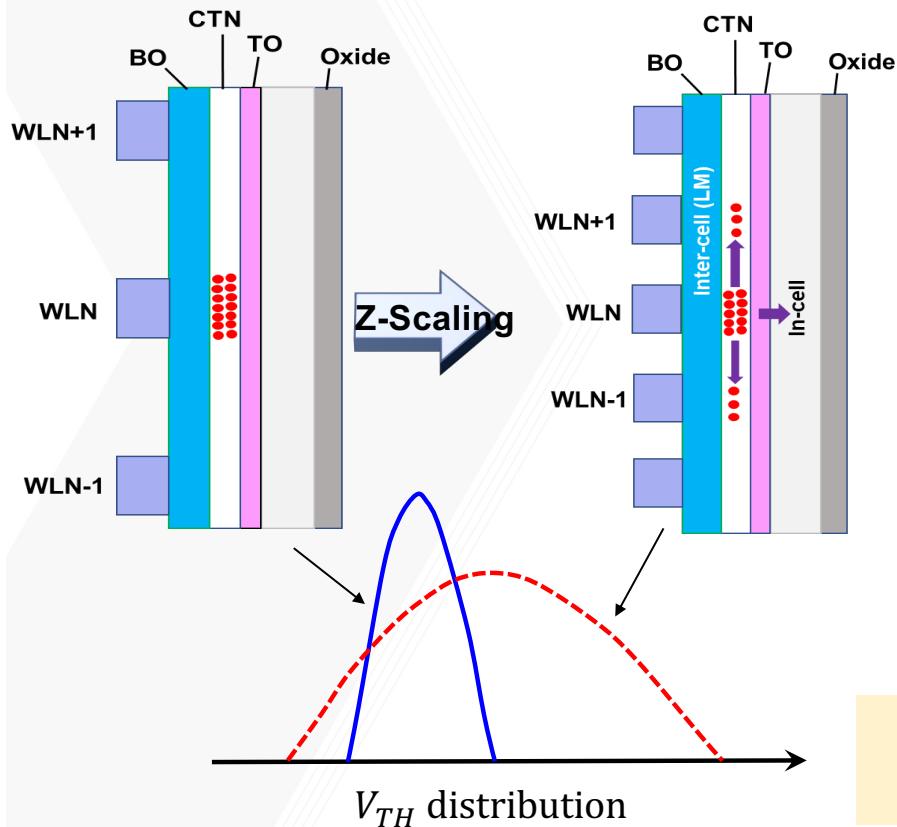


The mold height (cell height) needs to be reduced dramatically.

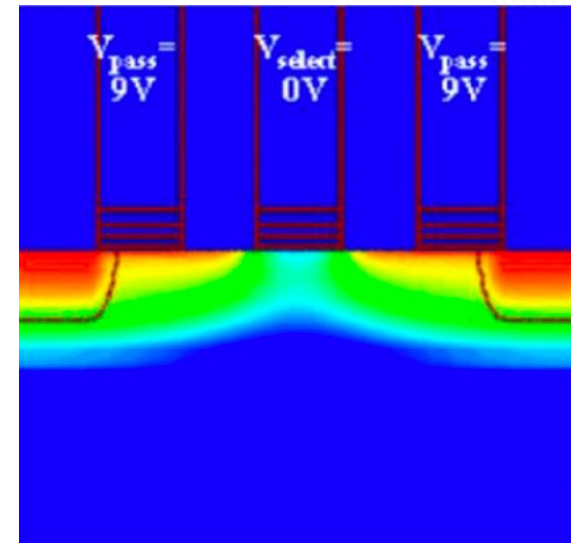
Han et al. Fundamental Issues in VNAND Integration
Toward More Than 1K Layers. IEDM 2023. Paper 35.1

Challenges for 1000+ layer vertical NAND

1 Lateral charge migration



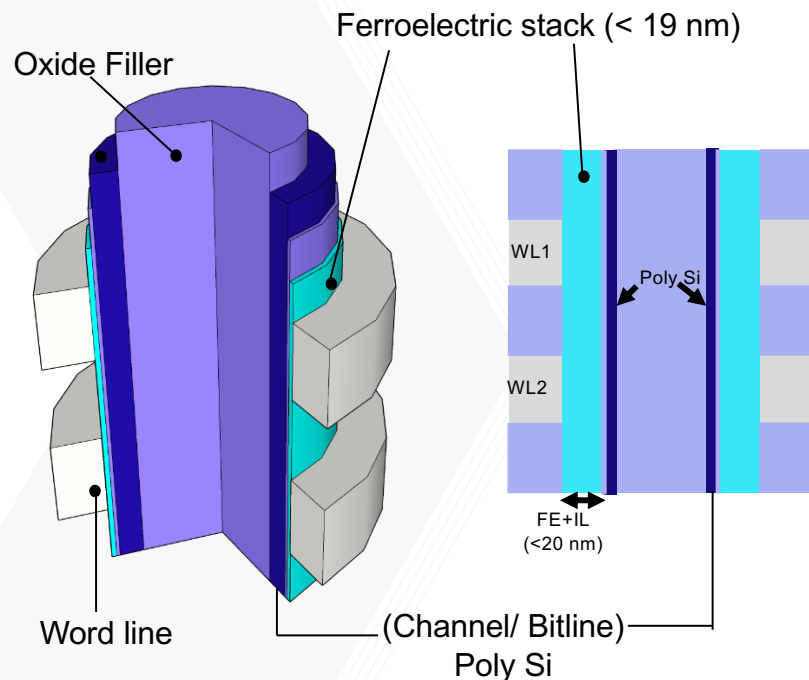
2 High write voltage



Write voltage of state of the art NAND is $>20V$. Large write voltage affects effective threshold voltage, similar to cell-to-cell interference.

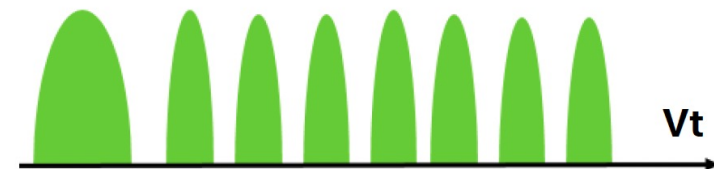
Cell-to-cell interference will significantly increase with aggressive Z-scaling for 1000L VNAND

Ferroelectric as a replacement for Charge Trap Layer

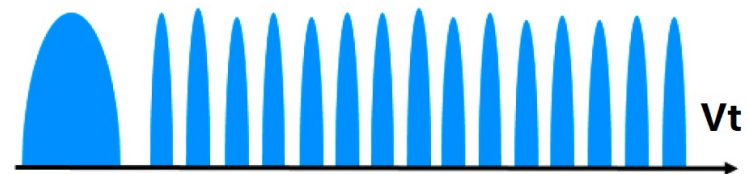


To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm

TLC:3 bits/cell $\rightarrow$ 8 Vt level MW $\approx$ 6V



QLC:4 bits/cell $\rightarrow$ 16 Vt level MW $\approx$ 7.5 V



Design constraints

Ferroelectric thickness, $t_{FE} \leq 19$ nm

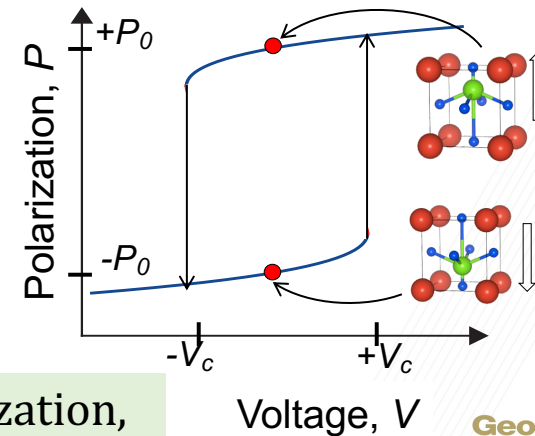
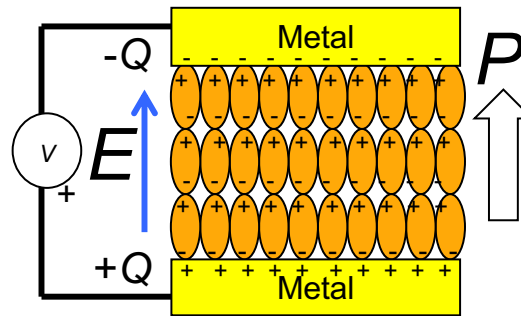
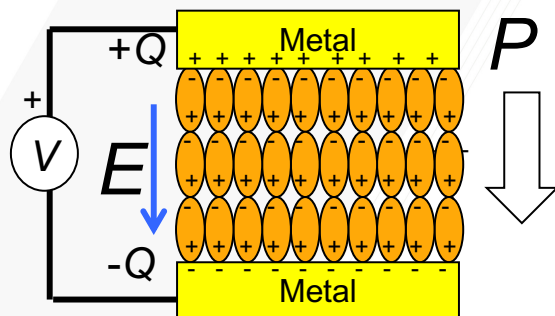
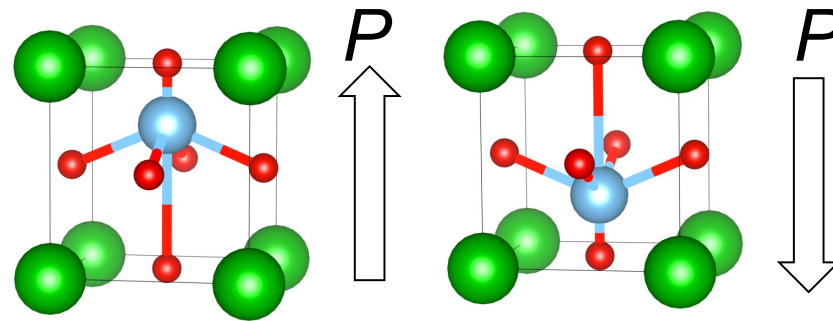
Write voltage ≤ 15 V

Memory window, MW ≥ 6.5 V

Ferroelectricity

Classical Ferroelectric
 PbTiO_3 , BaTiO_3 etc.

Emerging CMOS compatible
Ferroelectrics:
Doped HfO_2



A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

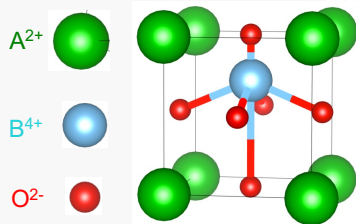
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for code storage in microcontrollers.

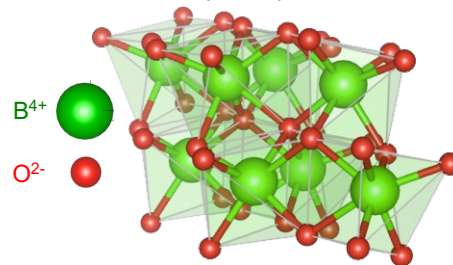
2. Controlled annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al.* *Appl. Phys. Lett.* 99, 112904 (2011)
- Boscke *et al.* *2011 IEEE Int. Electron Devices Meeting*. p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al.* *Nano Lett.* 12, 4318 (2012)

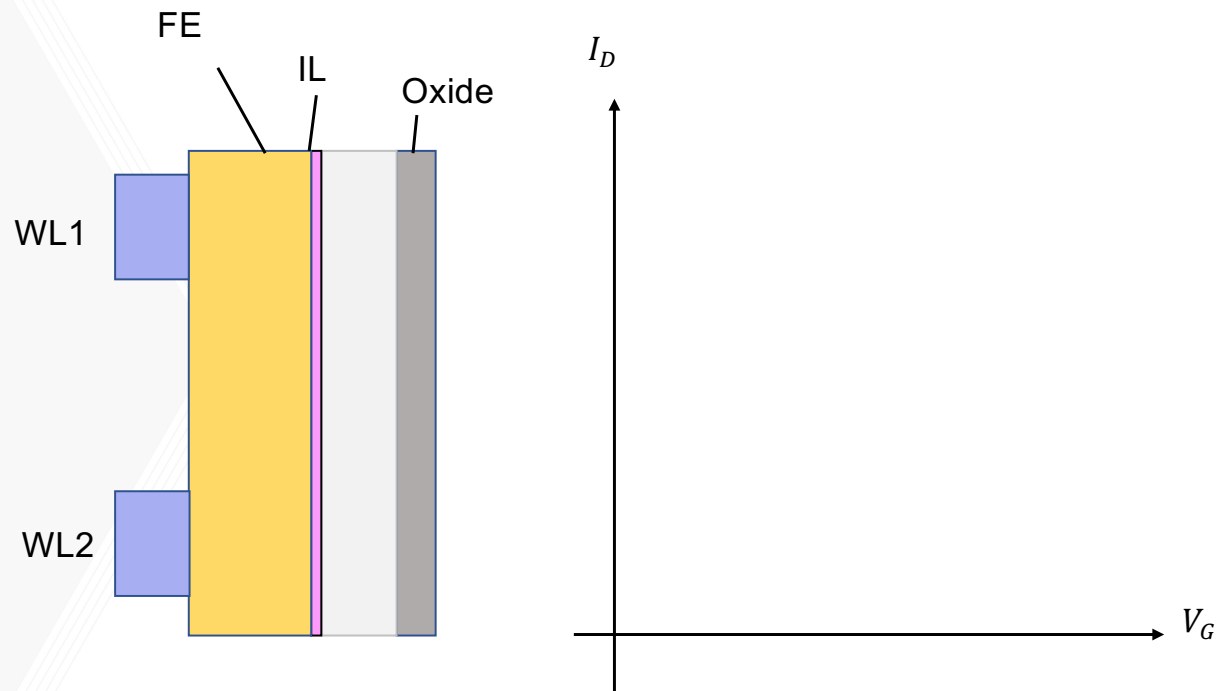
Perovskite-structure
ferroelectric oxide
(ABO_3)



Fluorite-structure
ferroelectric oxide
(BO_2)

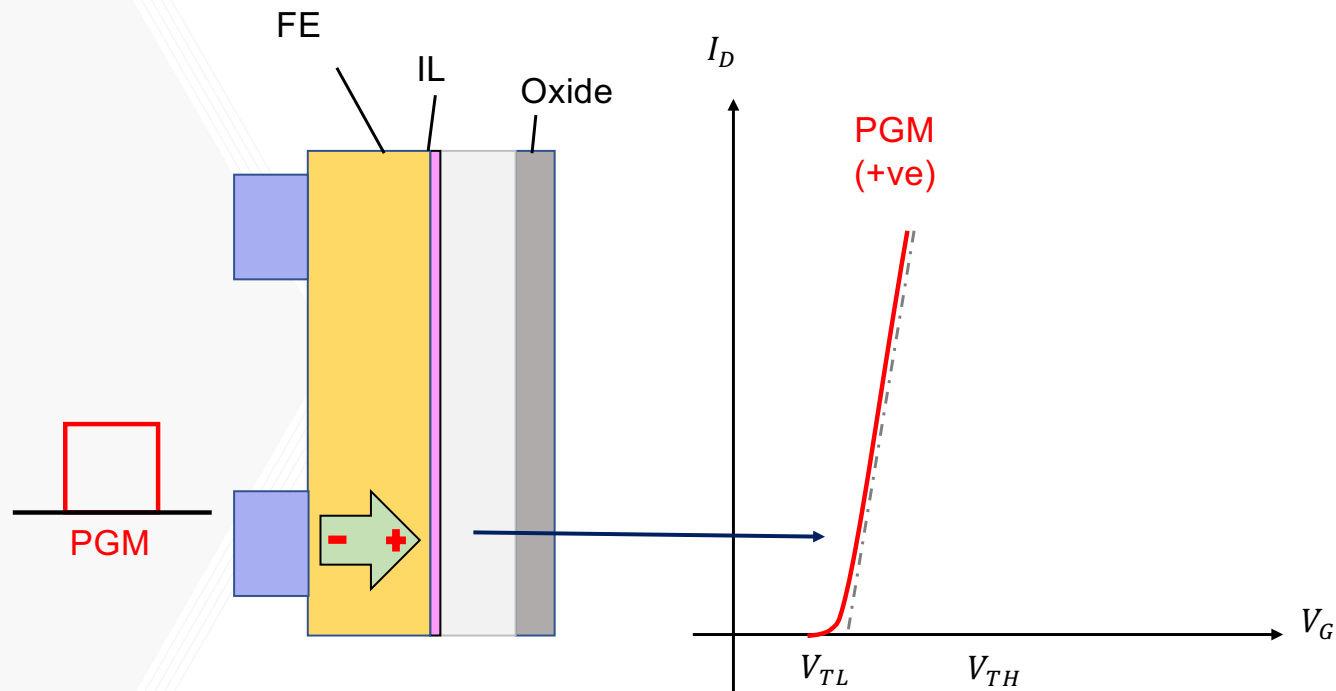


Ferroelectric field-effect transistor



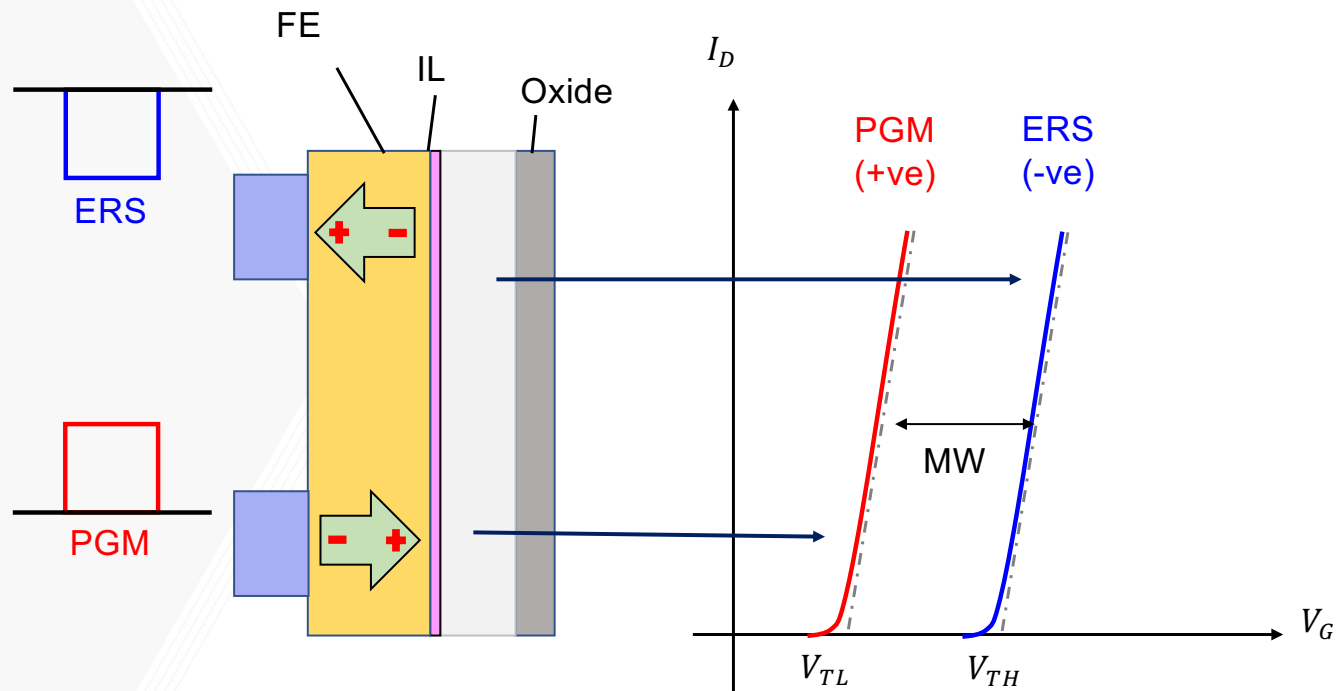
FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the “remnant” polarization.

Ferroelectric field-effect transistor



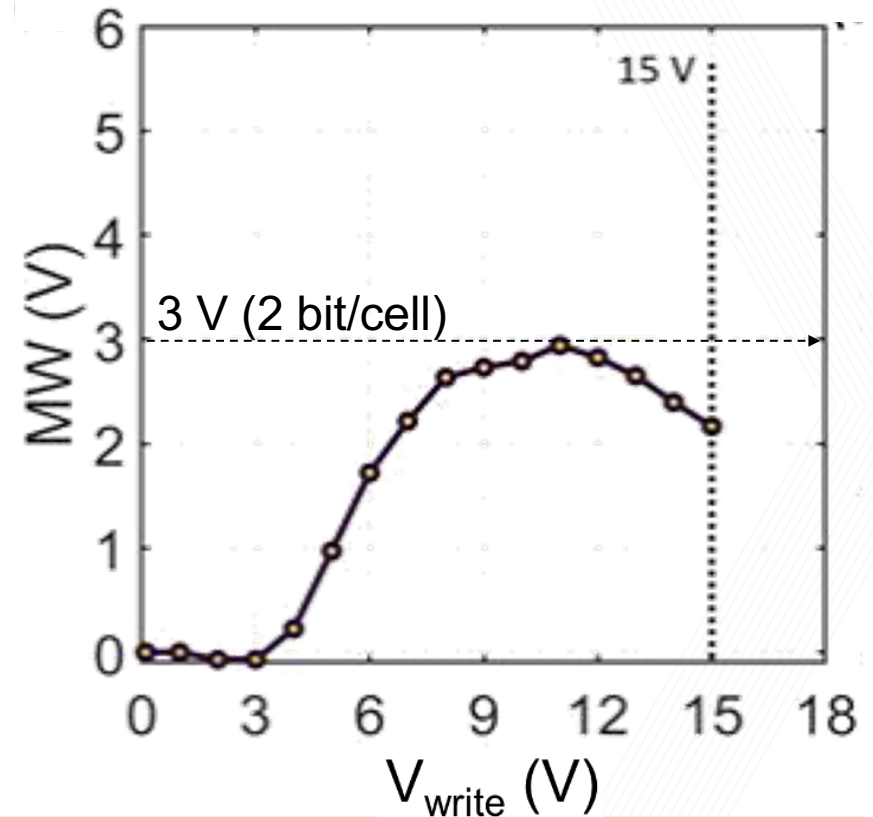
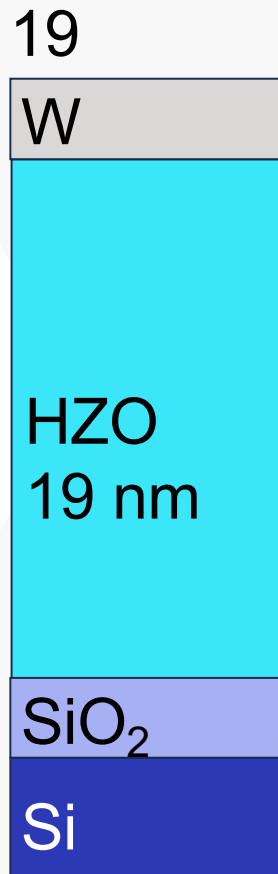
PGM (positive voltage) pulse sets the V_t to high V_t state in FEFET

Ferroelectric field-effect transistor



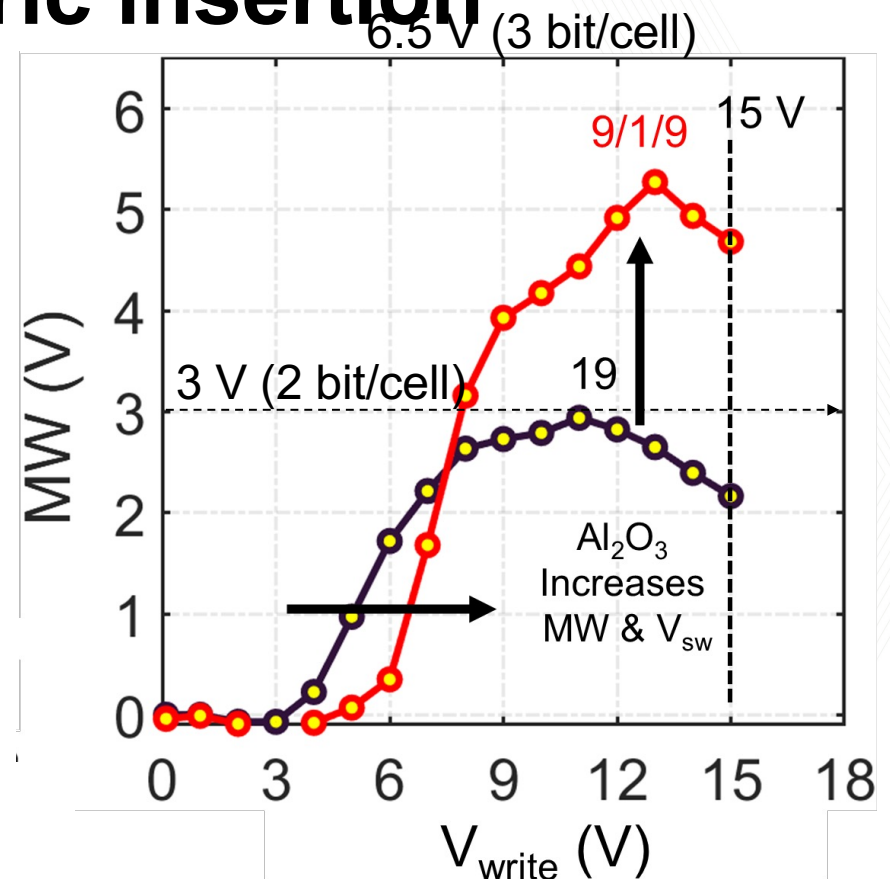
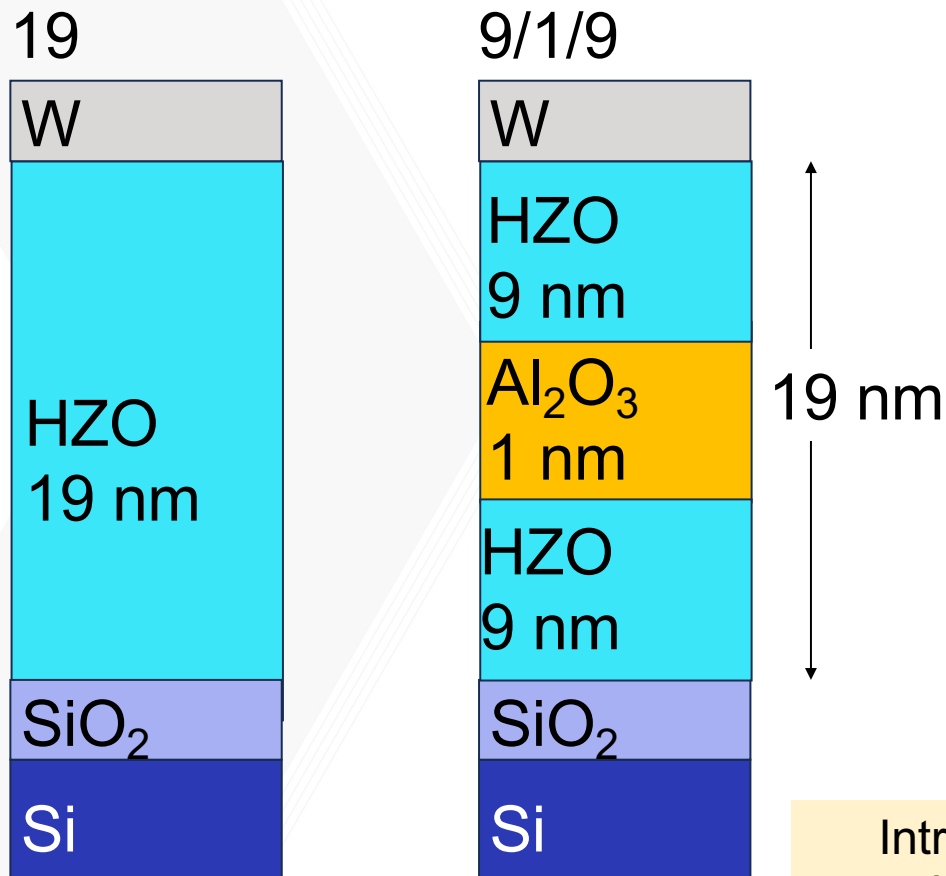
ERS (negative voltage) pulse sets the V_t to high V_t state in FEFET

Impact of tunnel dielectric insertion



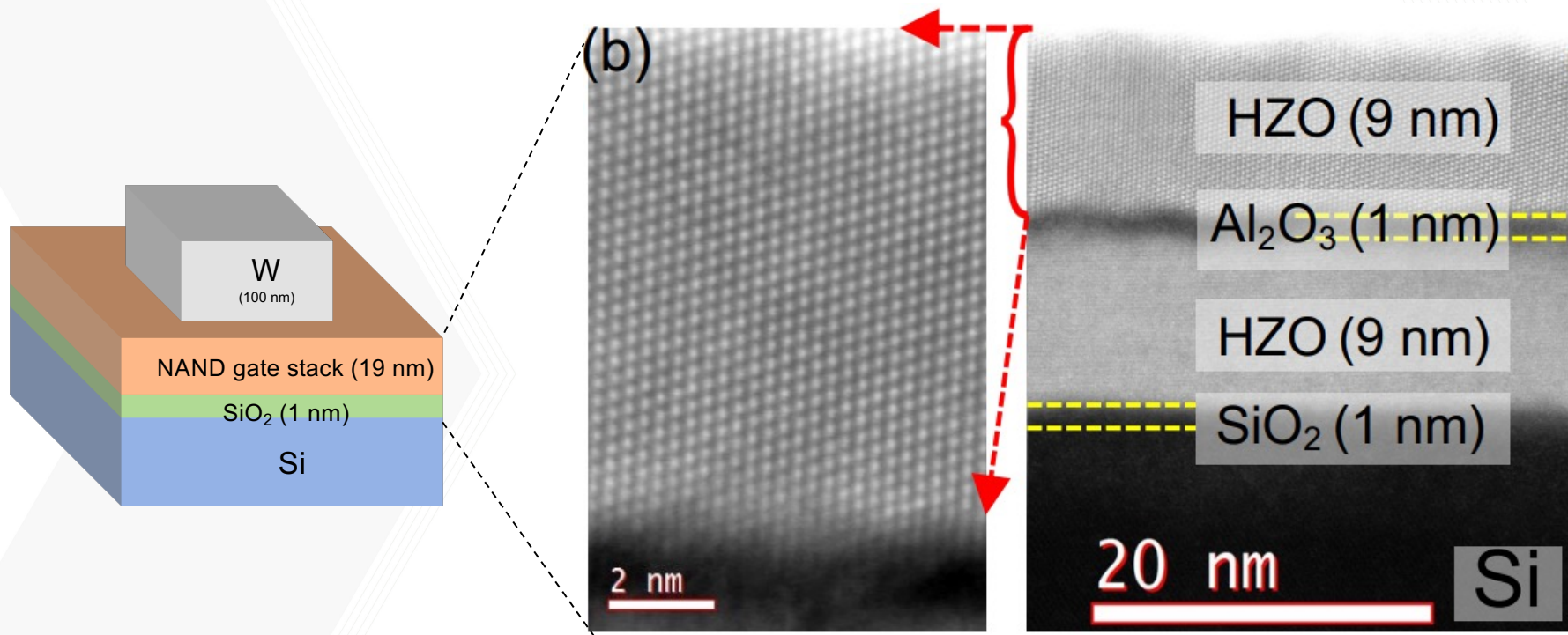
10 nm HZO layer leads to maximum memory window of 2.9 V.

Impact of tunnel dielectric insertion



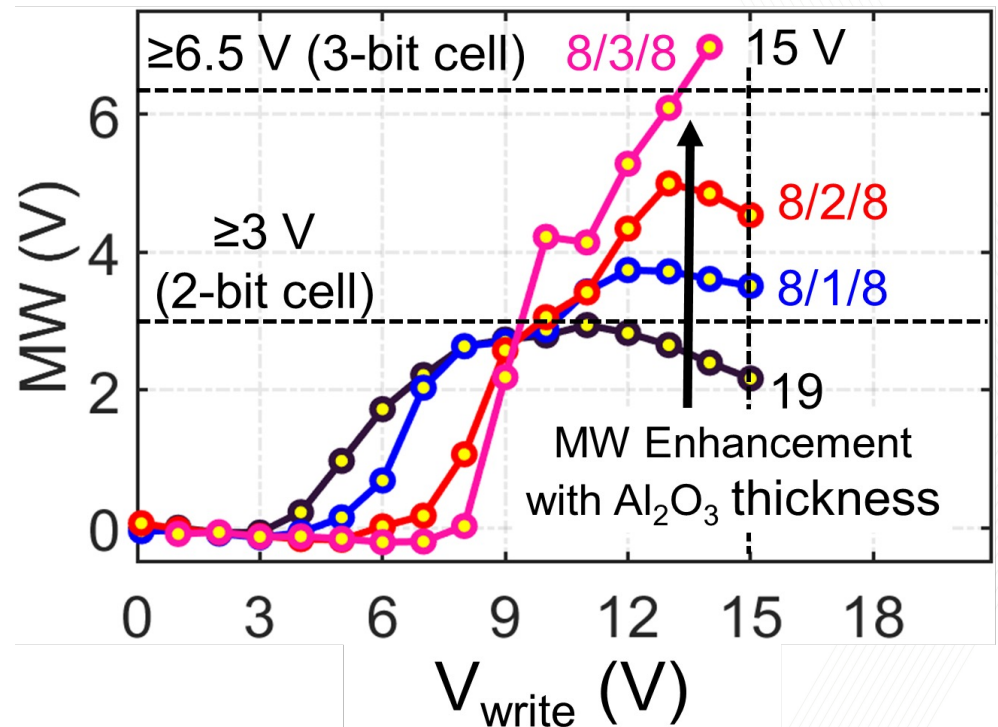
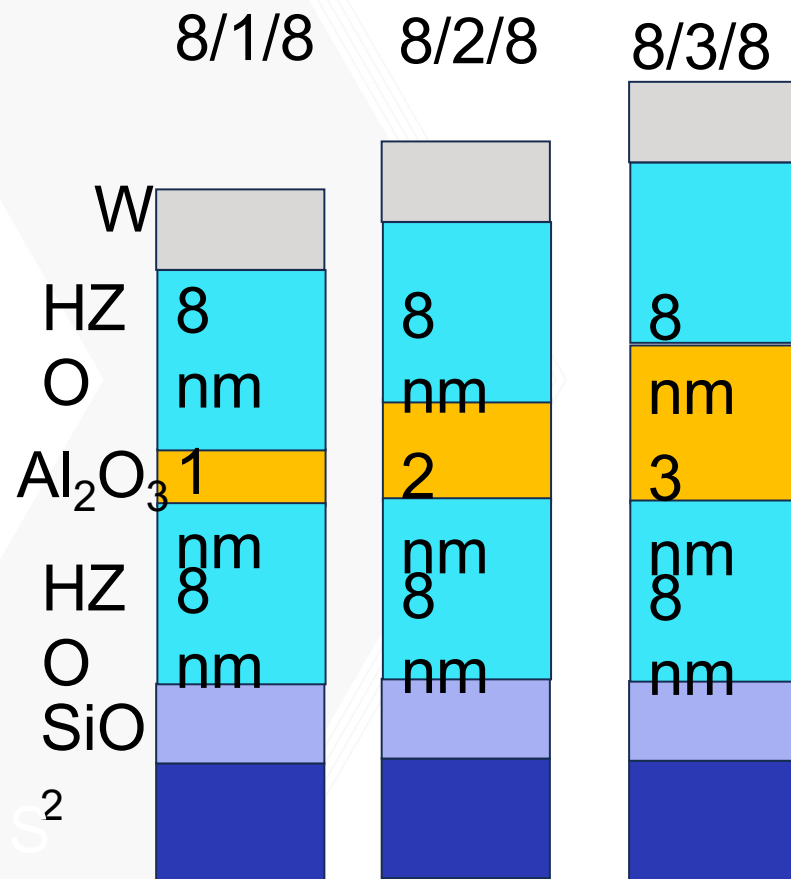
Introducing 1 nm Al₂O₃ intermediate layer dramatically memory window to 5.3 V.

Impact of tunnel dielectric insertion



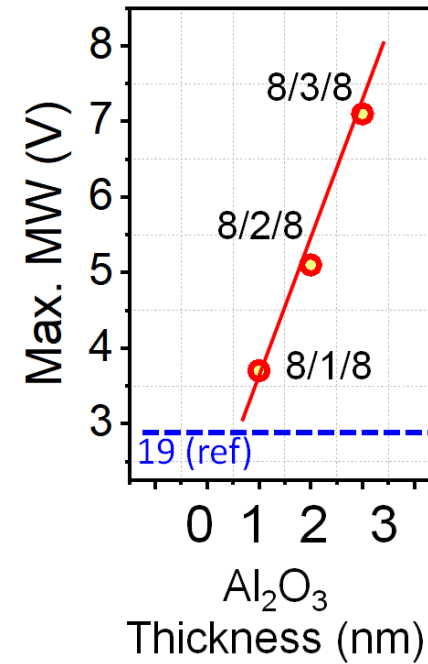
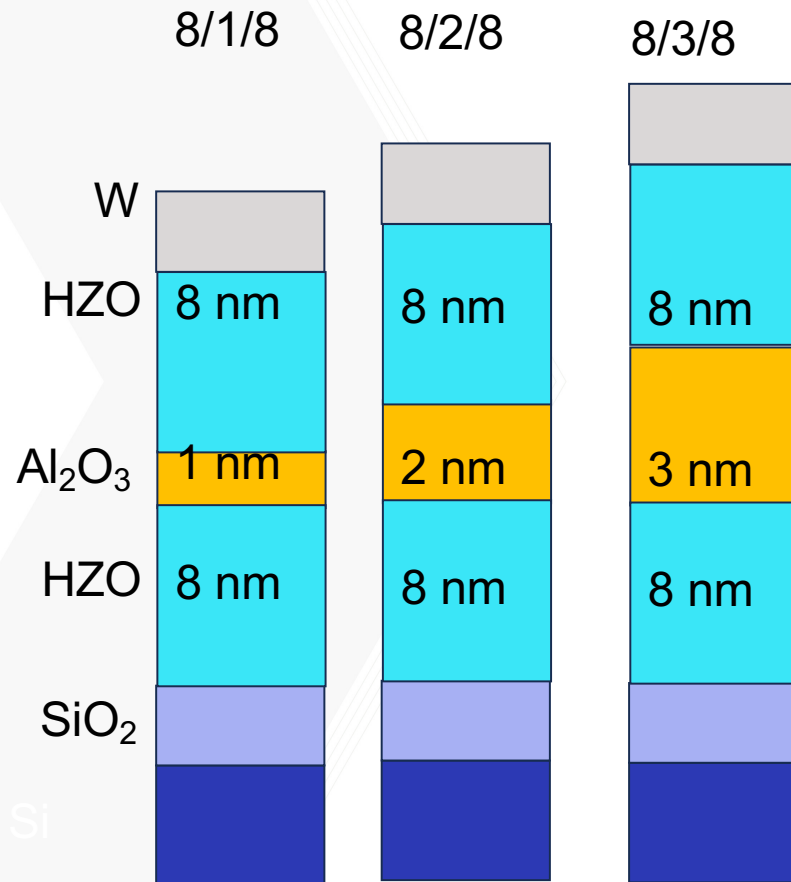
Full coverage of 1 nm Al₂O₃ is observed.

Impact of tunnel dielectric insertion



FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

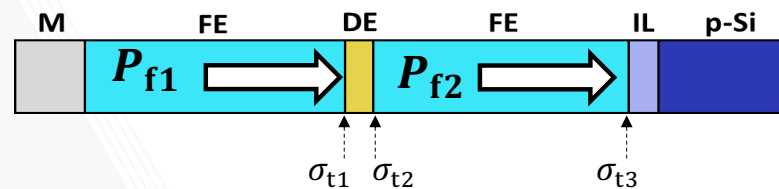
Impact of tunnel dielectric insertion



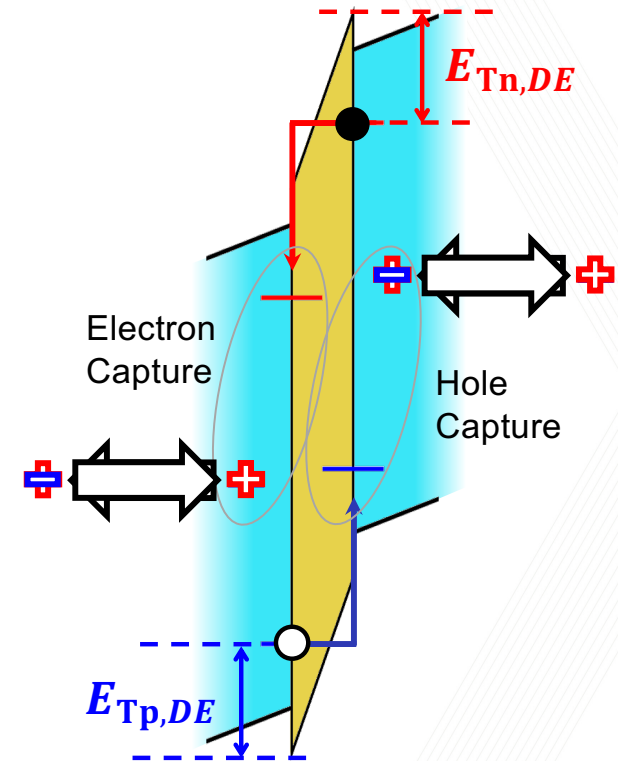
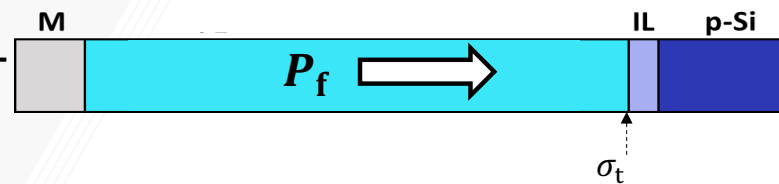
For a fixed FE layer, increase AlO layer increases the MW while increasing the write voltage <15 V.

Why do we call it a tunnel dielectric?

Band Engineered FEFET

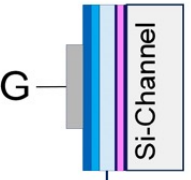
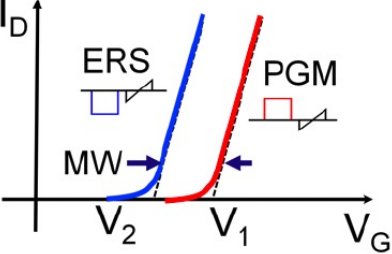
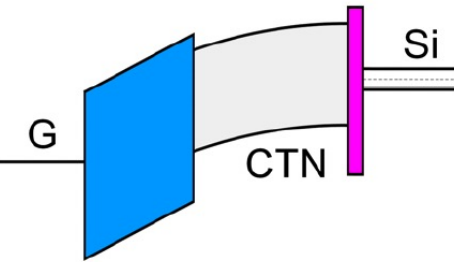
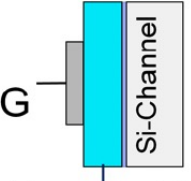
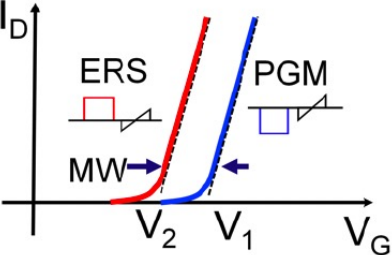
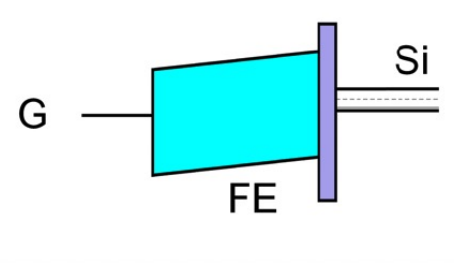
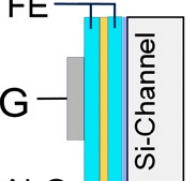
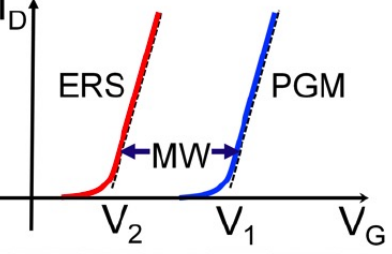
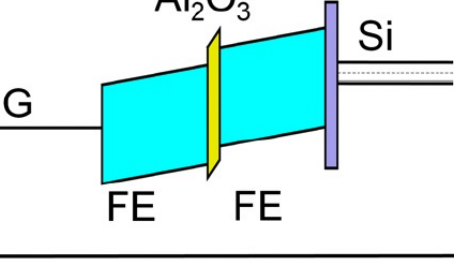


Standard FEFET



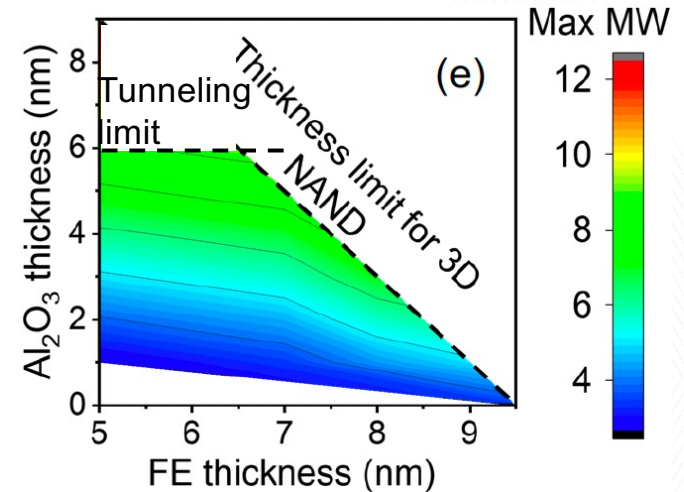
The interface trapped charges is hypothesized to interchange position via tunneling!

Ferroelectric NAND

	Structure	Characteristics	Band diagram at FB condition	Attributes
Charge Trap Flash	 Charge Trap Nitride			✓ Large MW × Large Write Voltage Mechanism: Trapping
Conventional FEFET	 Ferroelectric (FE)			× Low MW ✓ Low Write Voltage Mechanism: Polarization Switching
Band Engineered FEFET	 Al₂O₃ tunnel Oxide			✓ Large MW ✓ Moderate Write Voltage Mechanism: Polarization Switching + Trapping + Tunneling

Ferroelectric NAND

- Ferroelectricity presents opportunities for NAND storage technologies.
 - Write voltage reduction and memory window enhancement.
 - Potential for QLC by stack engineering.
 - Vertical scaling towards 1000 layers.
- Further exploration and engineering required for
 - Tunneling mechanism
 - Disturb characteristics and mitigation.
- Alternative structures can also lead to MW enhancement via gate side injection through blocking layer.
 - See: Lim et al. Comprehensive Design Guidelines of Gate Stack for QLC and Highly Reliable Ferroelectric VNAND. IEDM 2023 paper 35.4.



What can ferroelectric FETs go is beyond V-NAND storage?

“Ideally one would desire an indefinitely large memory capacity such that any particular ... word would be immediately available ...

It does not seem possible physically to achieve such a capacity. We are therefore forced to recognize the possibility of constructing a hierarchy of memories, each of which has greater capacity than the preceding, but which is less quickly accessible.”



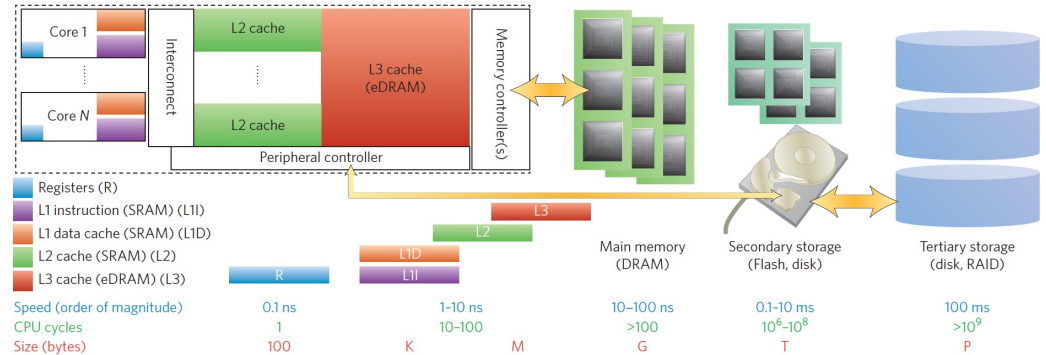
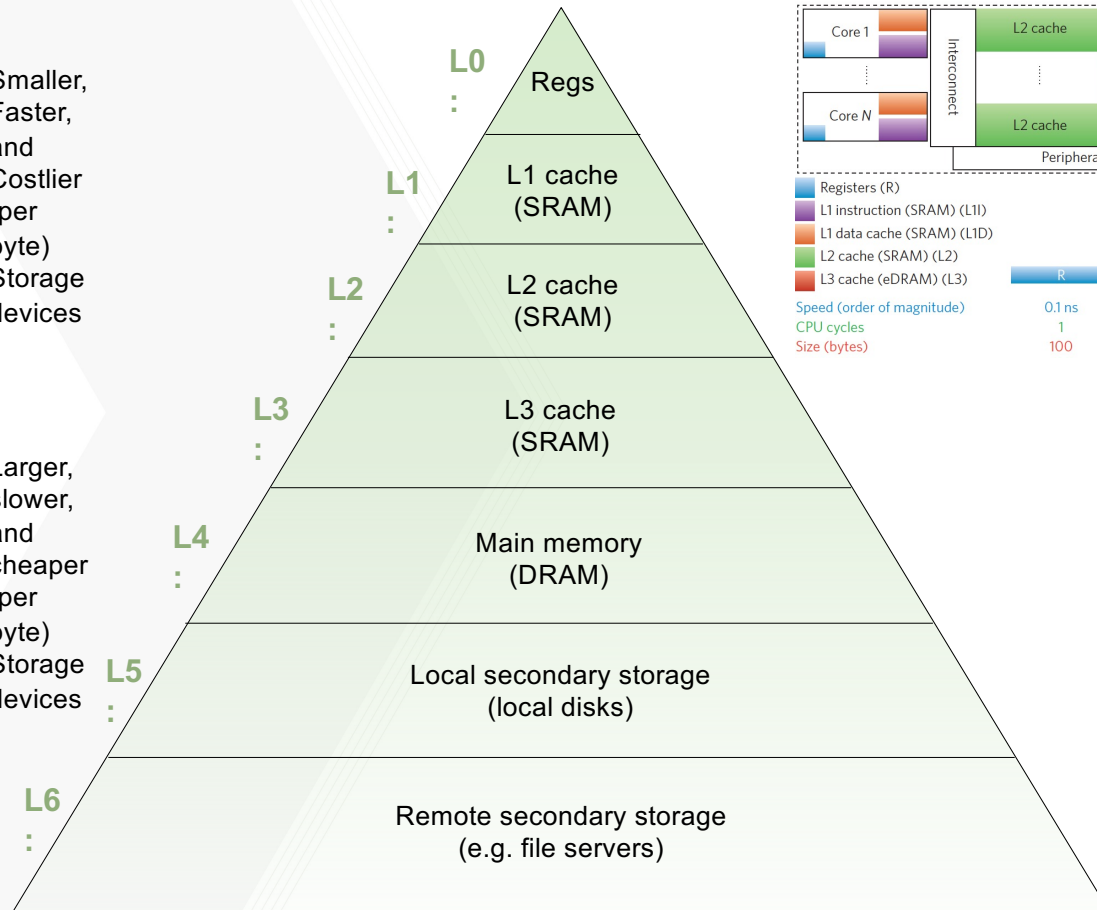
-von Neumann et al., 1947

**Preliminary Discussion of the Logical
Design of an Electronic Computing
Instrument**

The Memory Hierarchy

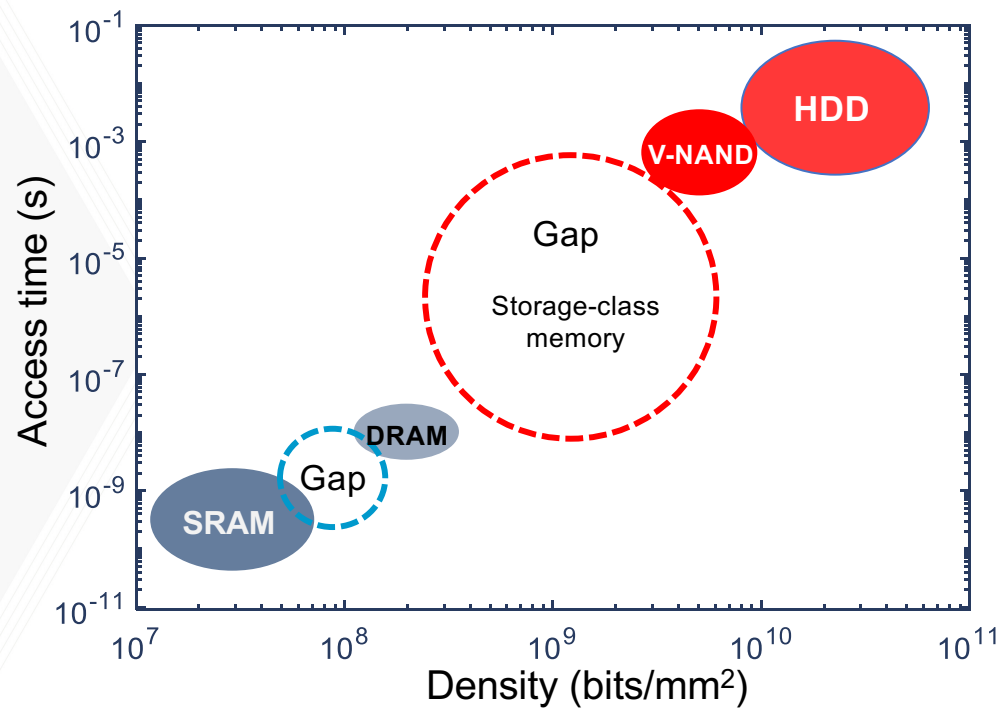
Smaller,
Faster,
and
Costlier
(per
byte)
Storage
devices

Larger,
slower,
and
cheaper
(per
byte)
Storage
devices



<http://www.nature.com/nnano/journal/v10/n3/full/nnano.2015.29.html>

The Memory Hierarchy



FEFET as an embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM ⁷⁰	eFlash (FG)	eFlash (SG MONOS) ⁴²	eFlash (SONOS) ⁴¹	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based) ⁶⁷
Cell size	120-150F ²	40F ²	40-60F ²	40-50F ²	50-60F ²	10-30F ²	10-30F ²	30-40F ²	50-60F ²
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	-12 V	-12 V	-5 V	1.5-4 V	-1.5 V	1-3 V	1.5 V
Write energy	-1 fJ	-1 pJ	-100 pJ	-100 pJ	1-10 pJ	1-10 fJ	1-10 fJ	-100 fJ	-1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	-100 ns	<100 ns	-100 ns	1-10 ns	1-10 ns	1-10 ns	1 μs
Read speed	<1 ns	>10 ns	-10 ns	<10 ns	-10 ns	1-10 ns	1-10 ns	1-25 ns	50-100 ns
Endurance	>10 ¹⁶	>10 ¹⁶	-10 ⁴	-10 ⁵	-10 ⁶	10 ⁵ -10 ⁹	>10 ¹⁰	>10 ¹²	>10 ¹⁴

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

Progress in FEFET technology

1

Write voltage
and Memory Window

<1.5 V write voltage
>0.5 V memory window

2

Read/Write
Speed

<10 ns write speed
<10 ns read-after-write delay

3

Device-to-device
variation

$\Delta V_{t,3\sigma} = 20\text{-}50 \text{ mV}$
(7 nm node)

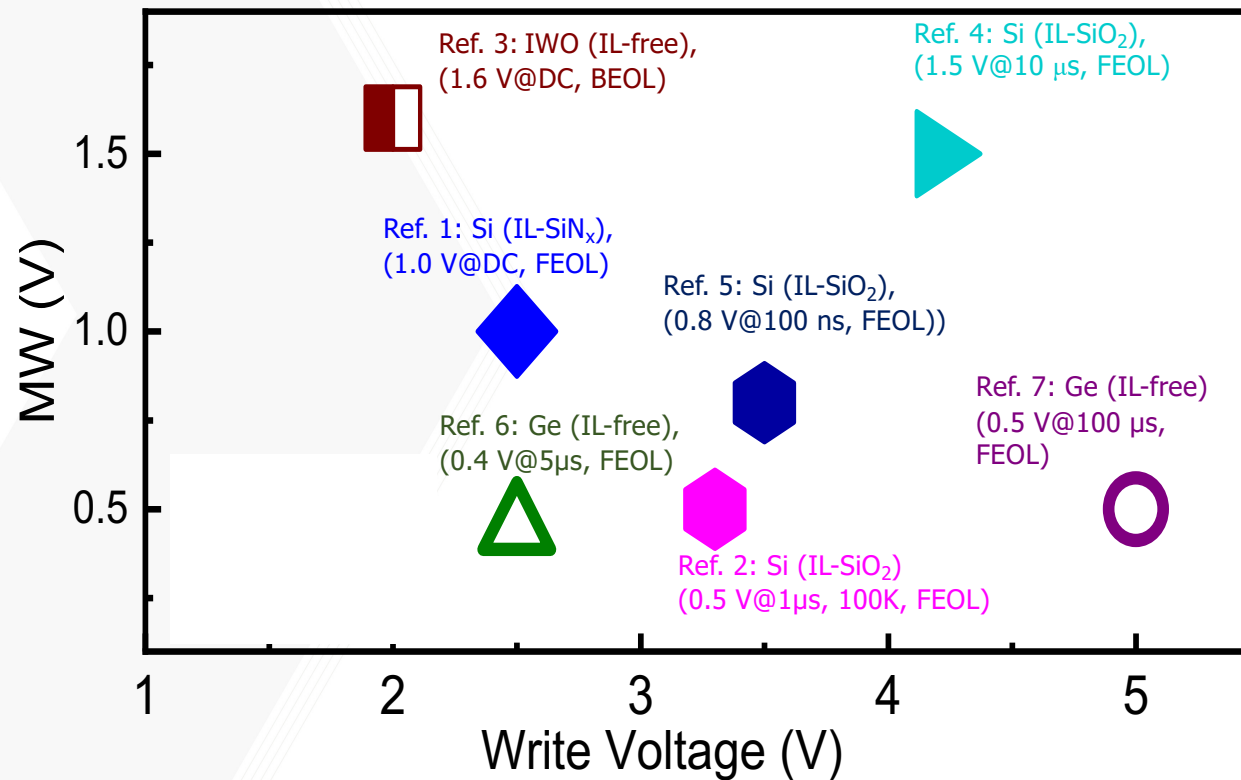
4

Reliability and endurance

>10¹² cycles

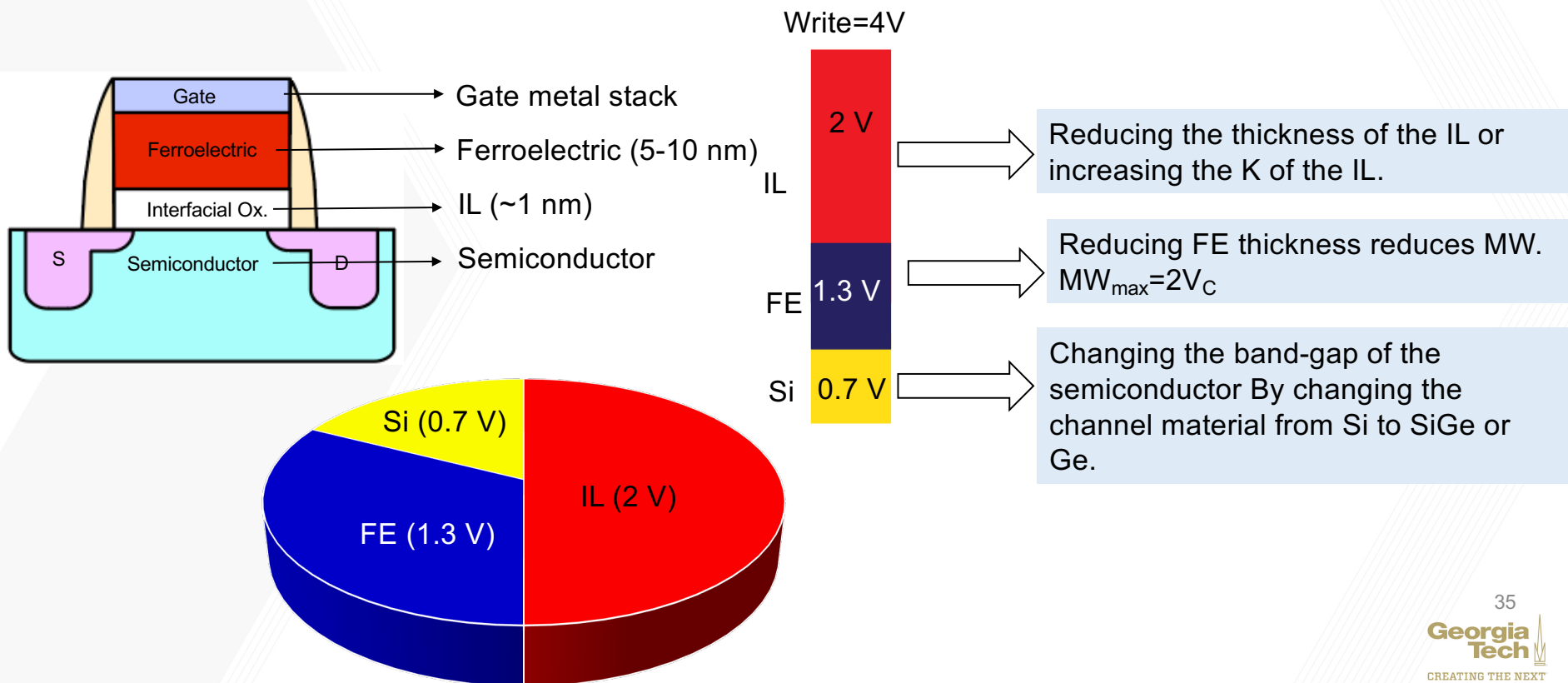
33

Benchmarking Memory Window v. Write Voltage Tradeoff

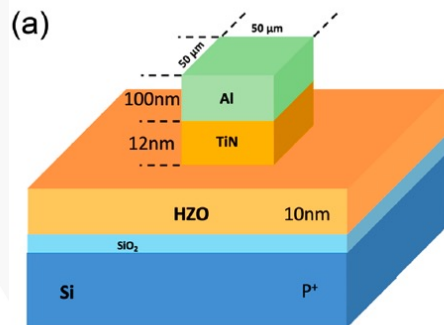


- [1] Tan *et al.*, *IEEE EDL*, 42, 994, (2021).
- [2] Tan *et al.*, *2020 IEEE Symposium on VLSI Technology* (2020).
- [3] Dutta *et al.*, *IEEE EDL*, 43, 382 (2022).
- [4] Dünkel *et al.*, *IEDM* (2017).
- [5] Nguyen *et al.*, *IEEE EDL*, 42, 1295, (2021).
- [6] Liu *et al.*, *IEEE EDL*, 40, 1419, (2019).
- [7] Zacharaki *et al.*, *ACS Appl. Electron. Mater.*, 4, (2022).

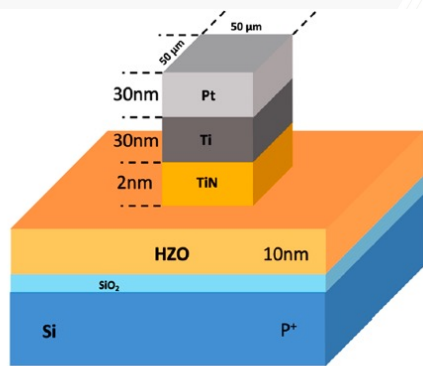
Write voltage vs. memory window trade-off



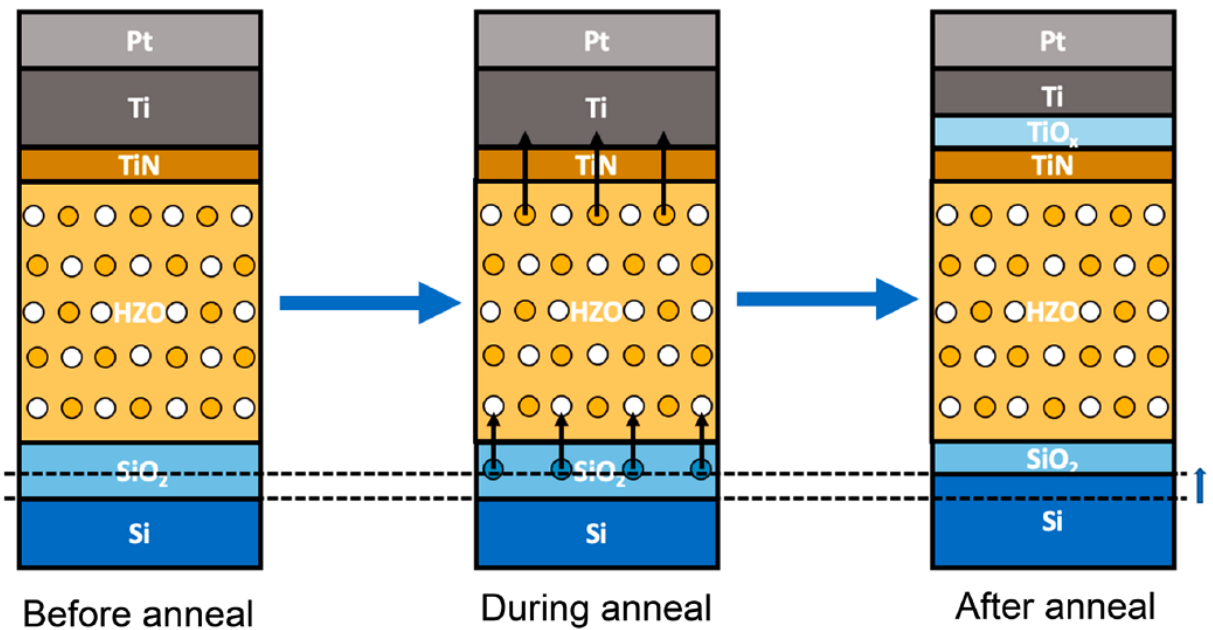
Remote oxygen scavenging to reduce IL thickness



Non-Scavenging



Remote-Scavenging

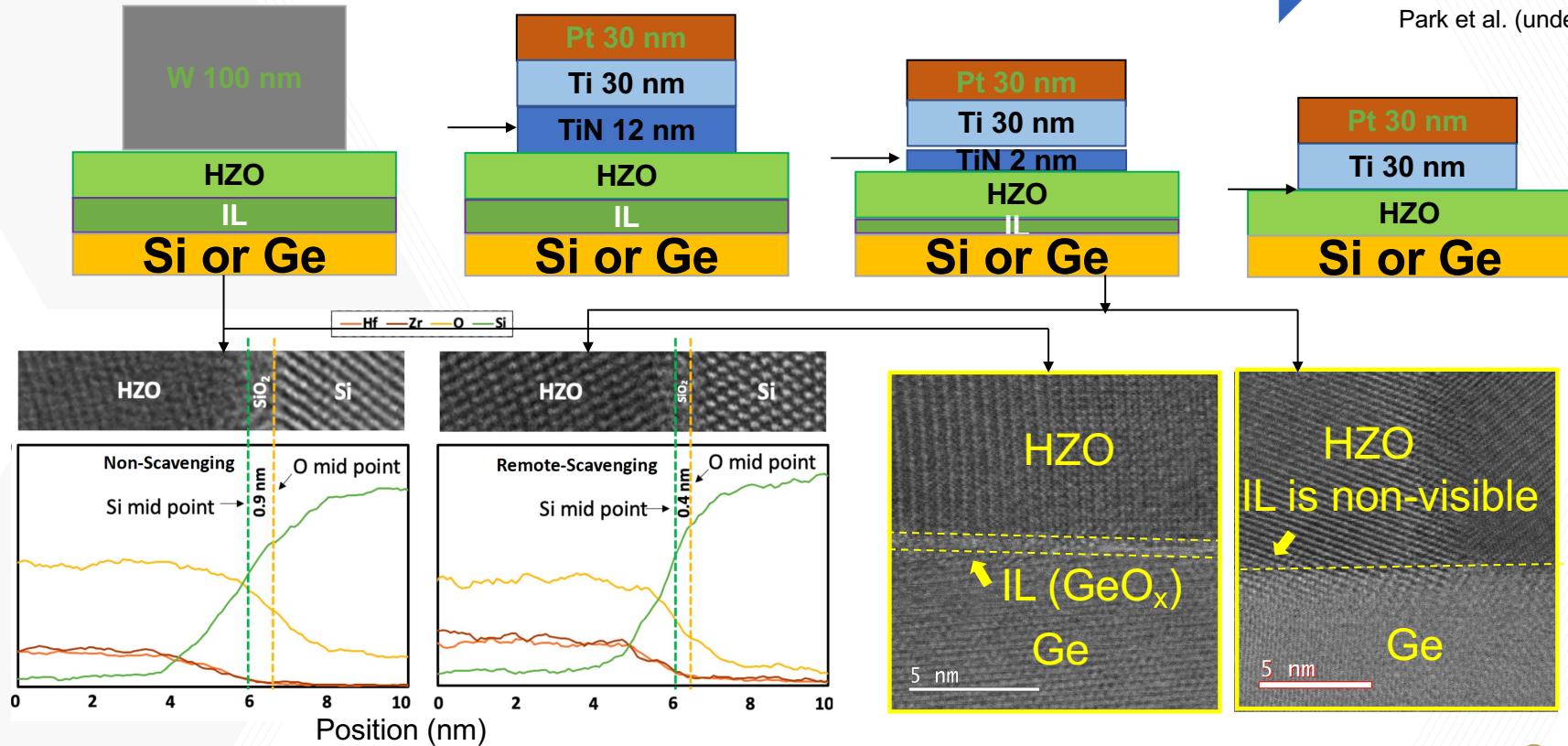


● - Oxygen atom ○ - Oxygen vacancy

Tasneem et al. "Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium–Zirconium Oxide-Based Metal–Oxide–Semiconductor Structures", ACS Appl. Mater. Interfaces 2022, 14, 43897–43906

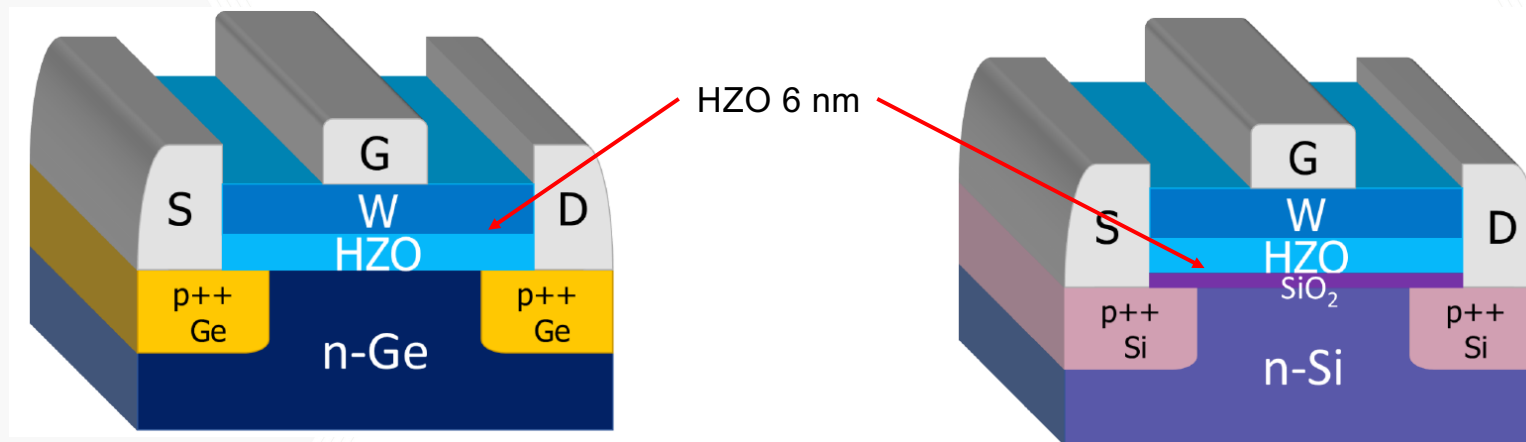
Decrease in IL thickness

Park et al. (under review)



Remote oxygen scavenging can result in controllable IL thickness.

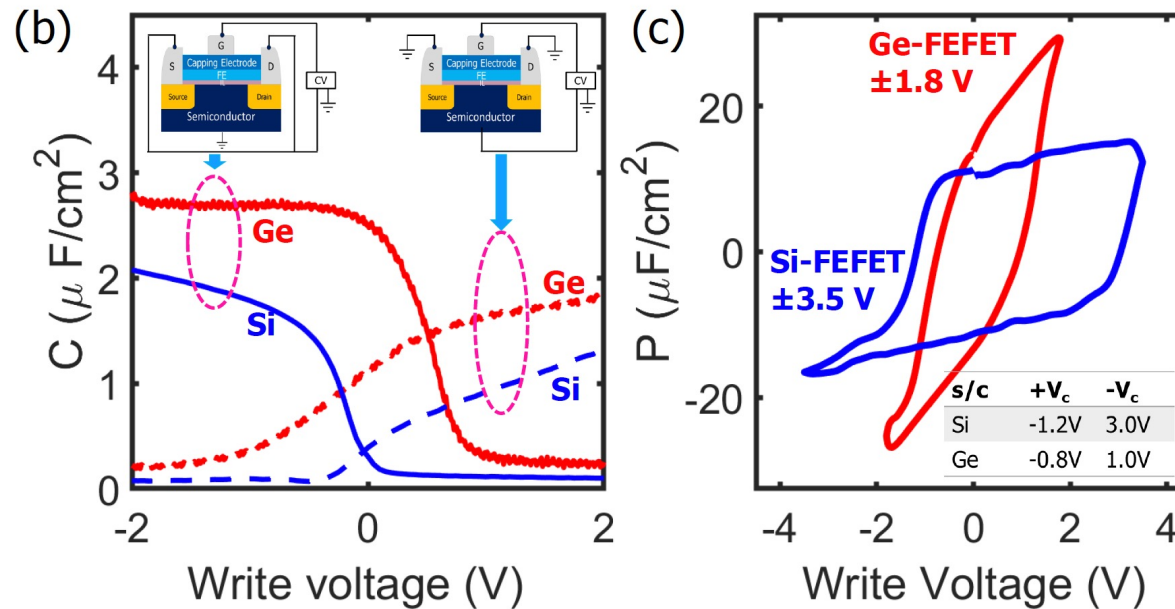
Ge-channel FEFETs with record-low write voltages



Si and Ge-channel FEFETs fabricated with the same 6 nm HZO layers, under similar process and fabrication conditions.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

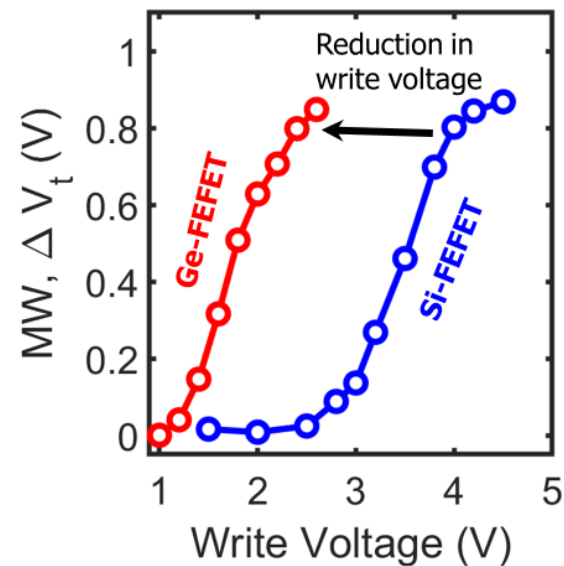
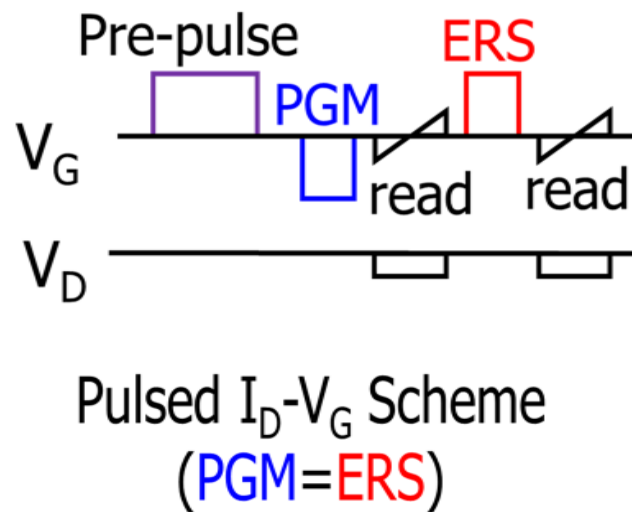
Ge-channel FEFETs with record-low write voltages



Significant increase on the on-capacitance and reduction in coercive voltage in Ge-channel FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

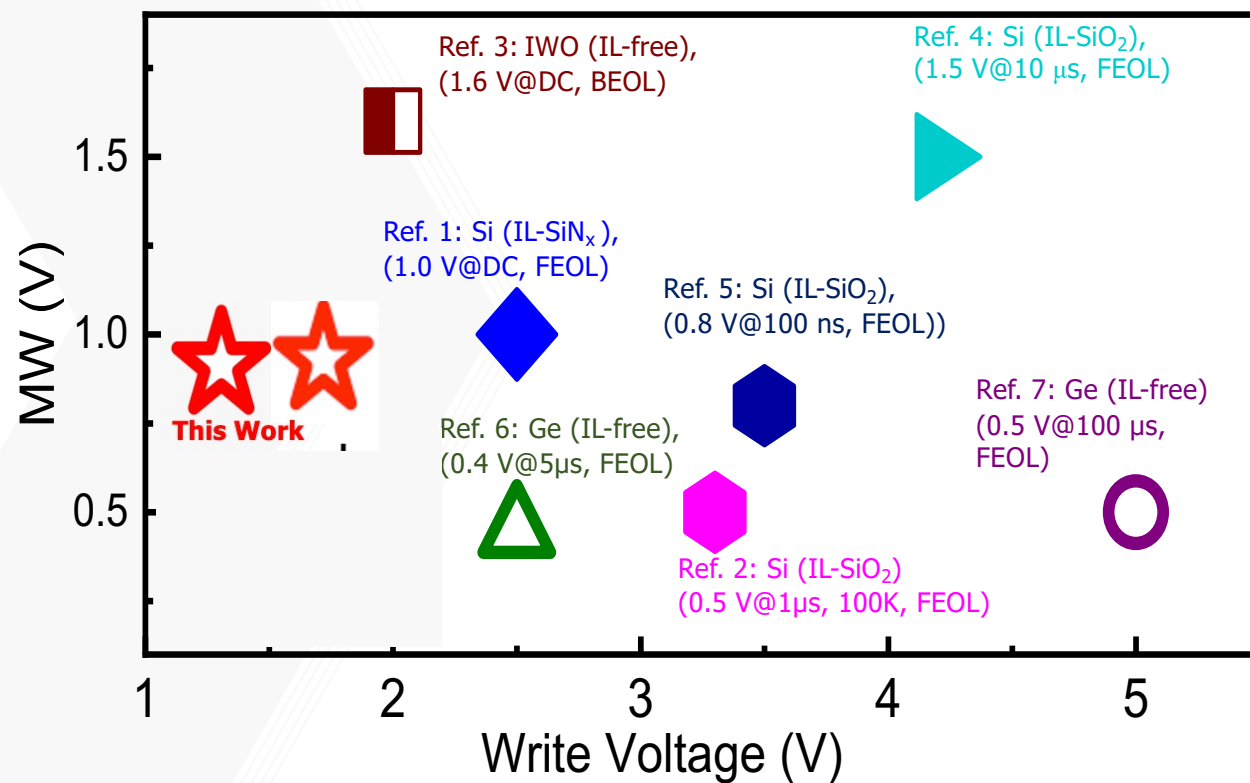
Pulsed I_D - V_G characteristics



Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

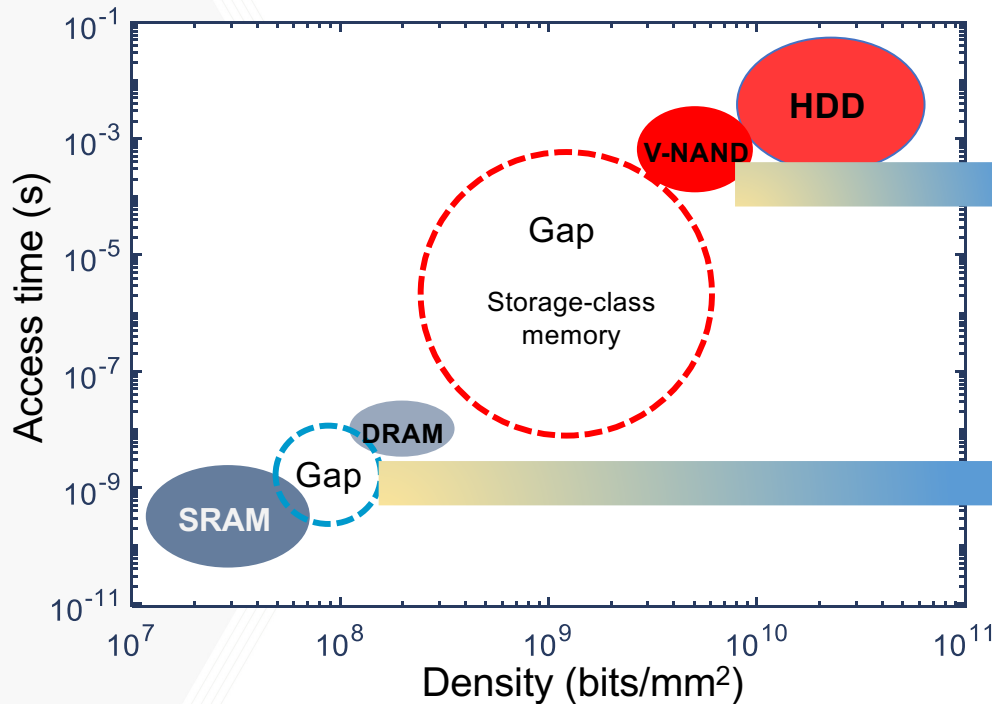
Benchmarking Memory Window v. Write Voltage Tradeoff



Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

- [1] Tan *et al.*, *IEEE EDL*, 42, 994, (2021).
- [2] Tan *et al.*, *2020 IEEE Symposium on VLSI Technology* (2020).
- [3] Dutta *et al.*, *IEEE EDL*, 43, 382 (2022).
- [4] Dünkler *et al.*, *IEDM* (2017).
- [5] Nguyen *et al.*, *IEEE EDL*, 42, 1295, (2021).
- [6] Liu *et al.*, *IEEE EDL*, 40, 1419, (2019).
- [7] Zacharaki *et al.*, *ACS Appl. Electron. Mater.*, 4, (2022).

FEFETs in the Memory Hierarchy



NAND FLASH

- Limited scaling (oxide > 20 nm)
- High write voltage (~20 V)
- Slow write (1-10 ms)
- Limited endurance (10³ for MLC)

V-FeNAND

- Scalable oxide (< 5 nm)
- Smaller write voltage (~10 V)
- Fast write (< 1 μs)

Cell area | Speed

DRAM:	6-30F ² <10 ns
FeFET:	5-10F ² 5-10 ns
SRAM:	140-280F ² <1 ns

What are the key fundamental questions to address for ferroelectrics?

2011→2023

APPLIED PHYSICS LETTERS 99, 112904 (2011)

Phase transitions in ferroelectric silicon doped hafnium oxide

T. S. Böske,^{1,2,a,b)} St. Teichert,^{3,b)} D. Bräuhäus,⁴ J. Müller,⁵ U. Schröder,^{2,b)} U. Böttger,⁴ and T. Mikolajick^{2,6}

¹Löberwallgraben 2, 99096 Erfurt, Germany

²NamLab gGmbH, 01187 Dresden, Germany

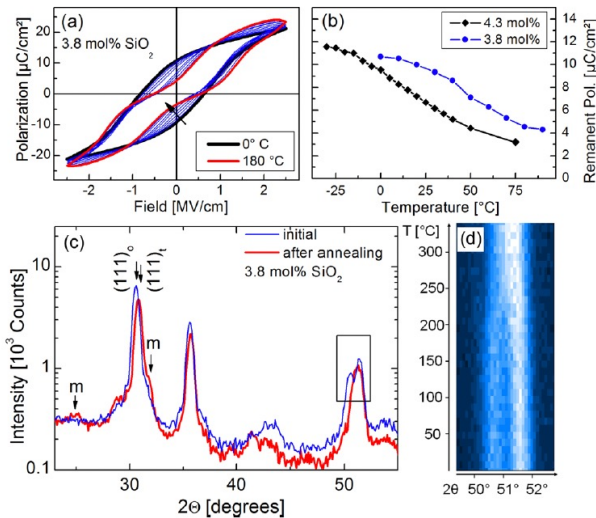
³UAS Jena, Department of SciTec, 07745 Jena, Germany

⁴RWTH Aachen, Institut für Werkstoffe der Elektrotechnik, 52062 Aachen, Germany

⁵Fraunhofer Center Nanoelectronic Technologies (CNT), 01099 Dresden, Germany

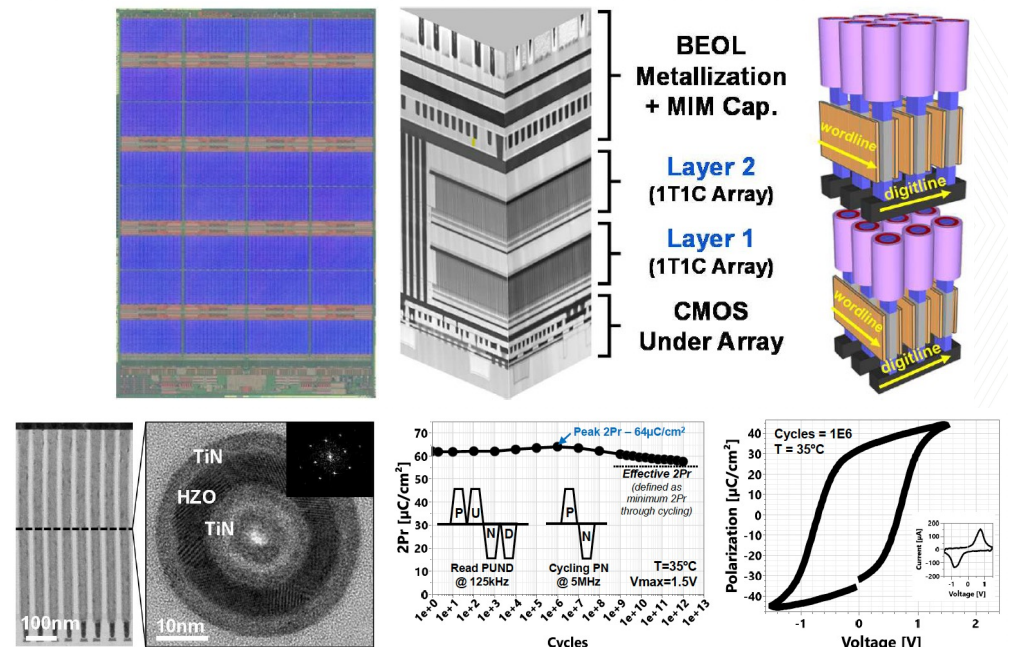
⁶Department of Nanoelectronic Materials, University of Technology Dresden, 01062 Dresden, Germany

(Received 18 July 2011; accepted 19 August 2011; published online 15 September 2011)



NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads

N. Ramaswamy, A. Calderoni, J. Zahurak, G. Servalli, A. Chavan, S. Chhajed, M. Balakrishnan, M. Fischer, M. Hollander, D. P. Ettisseray, A. Liao, K. Karda, M. Jerry, M. Mariani, A. Visconti, B. R. Cook, B. D. Cook, D. Mills, A. Torsi, C. Mouli, E. Byers, M. Helm, S. Pawlowski, S. Shiratake, and N. Chandrasekaran
Micron Technology Inc., Boise, USA, email: dramaswamy@micron.com



Georgia
Tech
CREATING THE NEXT

“

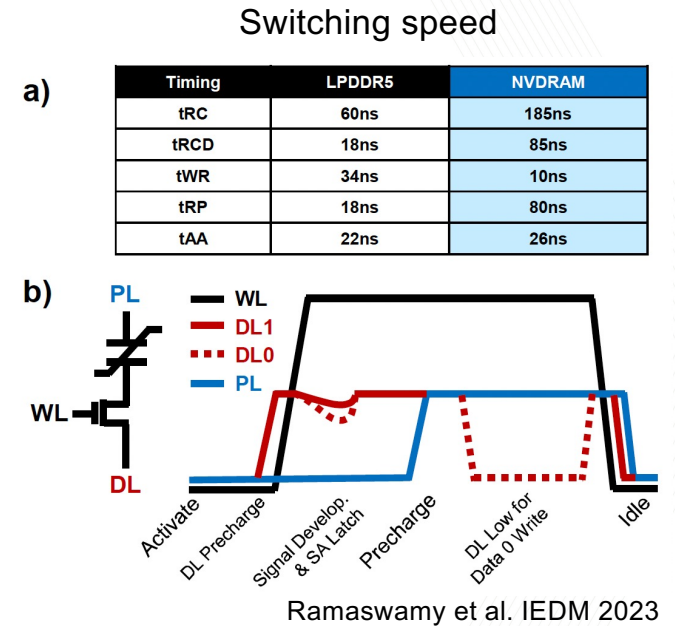
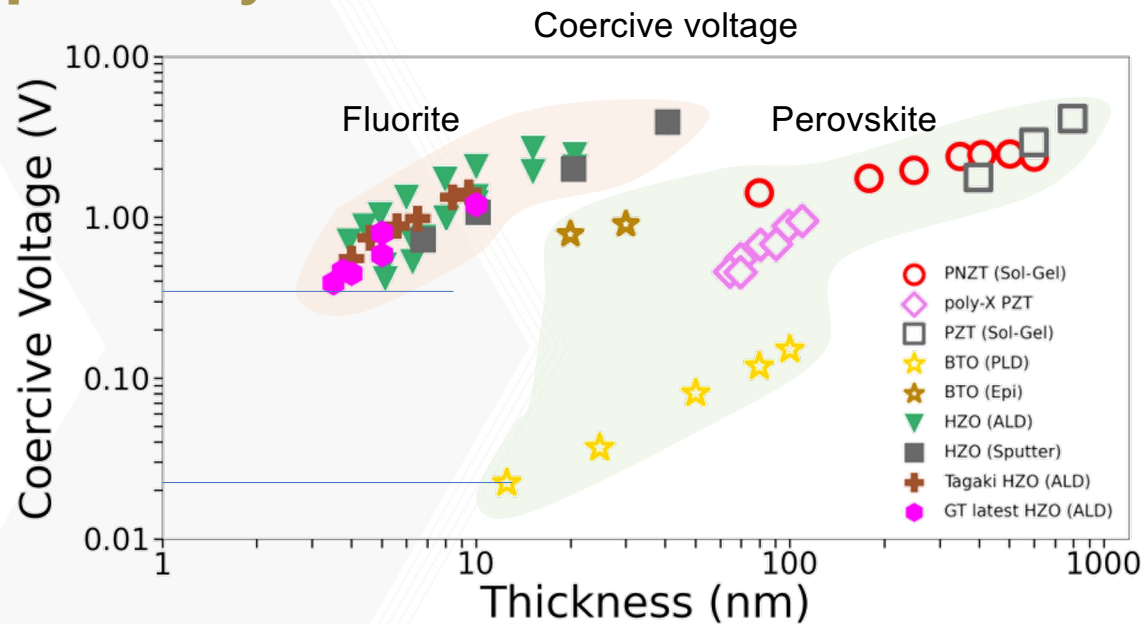
We learned that if you think you can do something,
you may very well be able to do one thousand times better once you understand what's going on.

”

John Mayo
Former President, Bell Labs

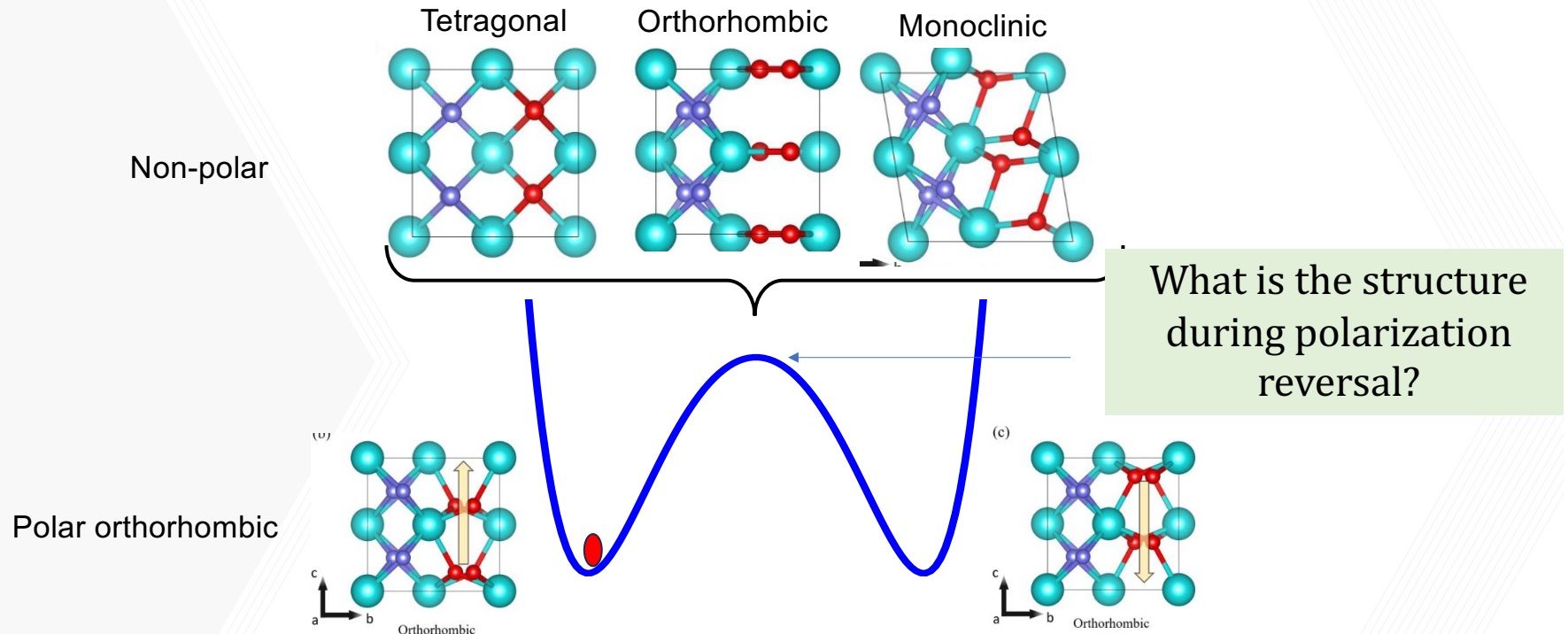


Write voltage, switching speed and microscopic switching pathway



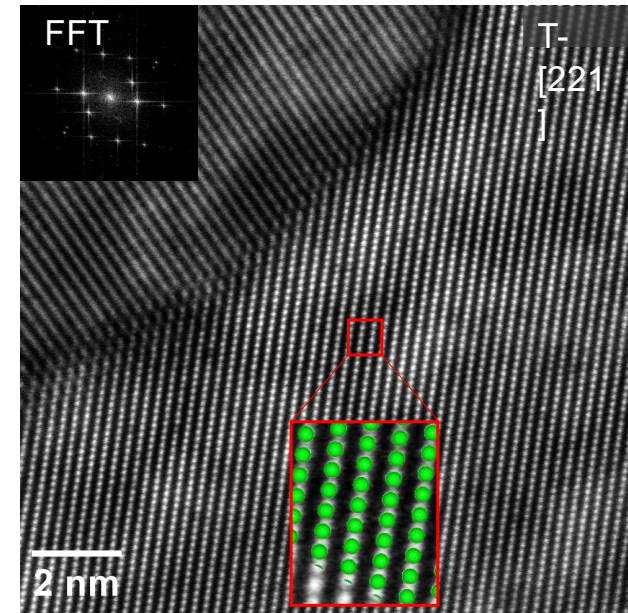
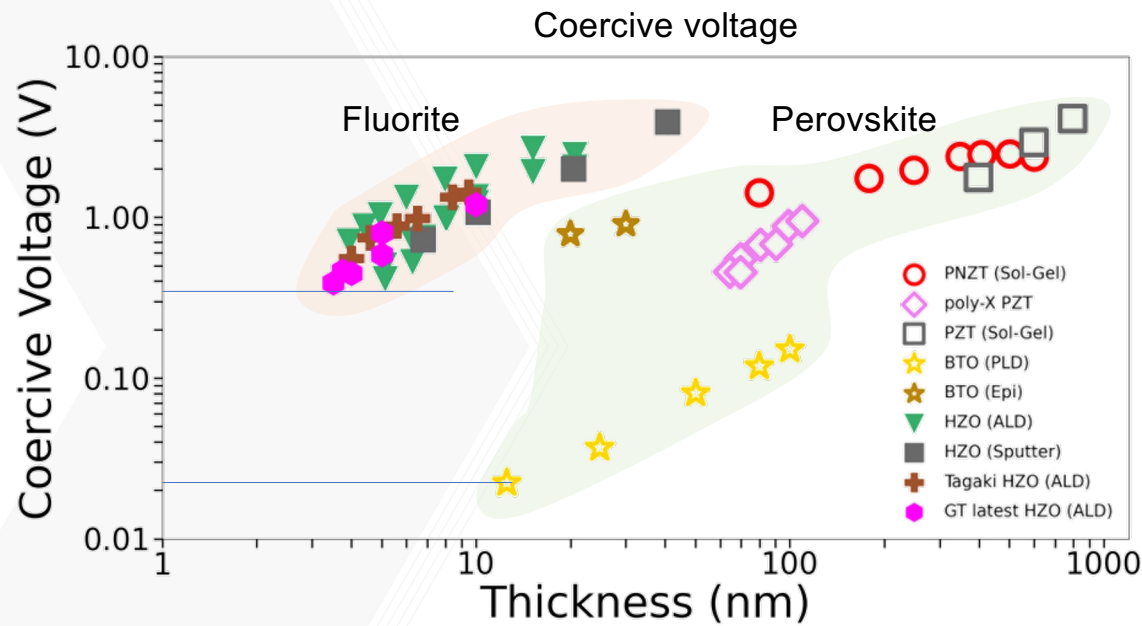
Understanding the switching mechanism may lead to techniques to reduce write voltage and switching delay.

Switching pathway



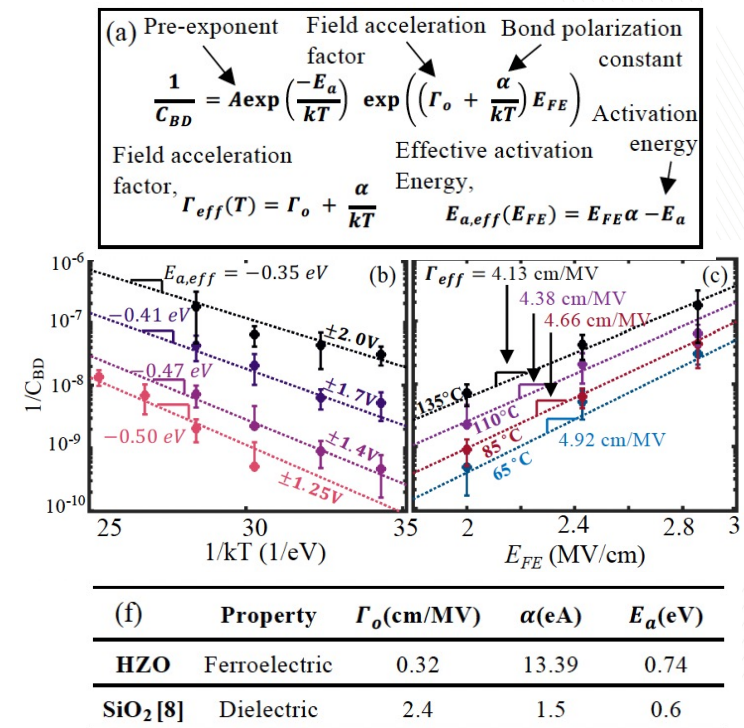
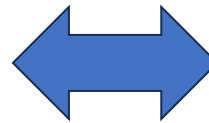
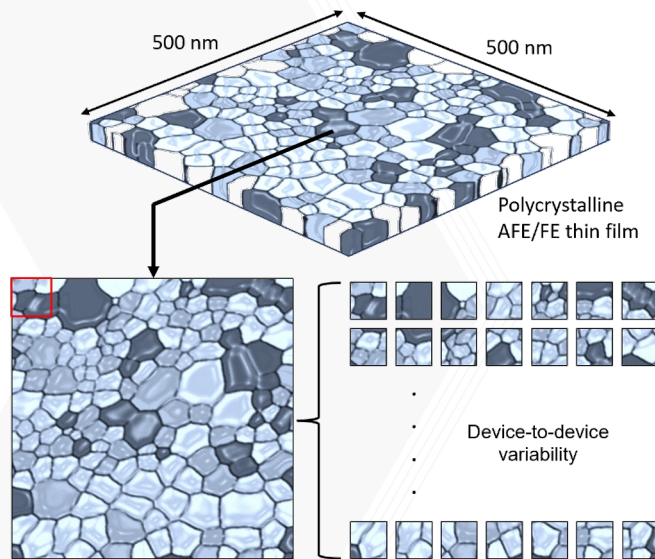
Understanding the switching mechanism may lead to techniques to reduce write voltage and switching delay.

Scaling limit limited by grain boundaries and direct tunneling?



What role do the grain boundaries play in leakage and reliability?

Connection between reliability and microstructure?



Does microstructure have impact on reliability?

Machine Learning Assisted Predictive TCAD Modeling (from Metrology to Device Metrics)

Ferro polarization map (from TKD data from SEM/TEM)

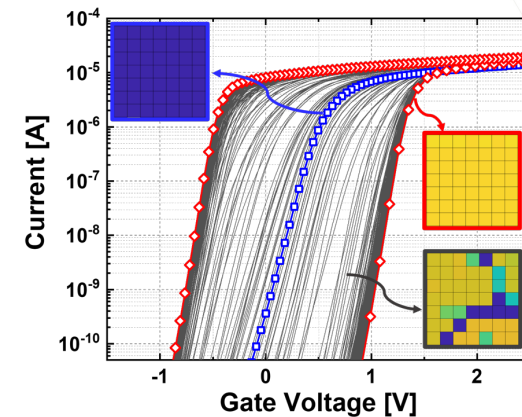
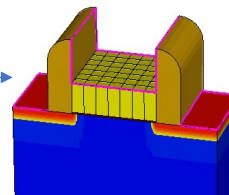
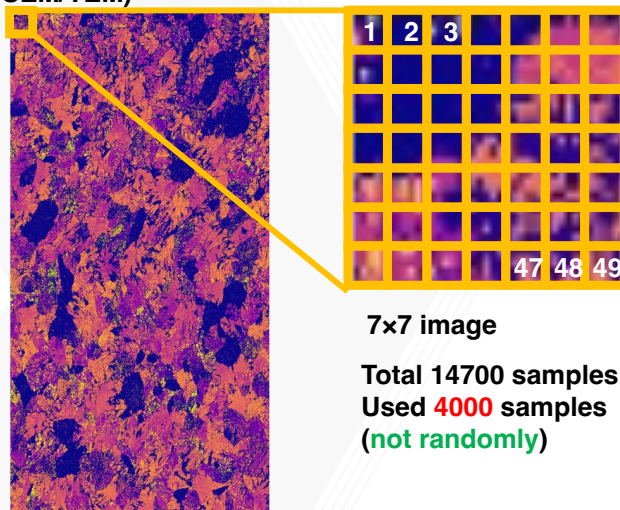


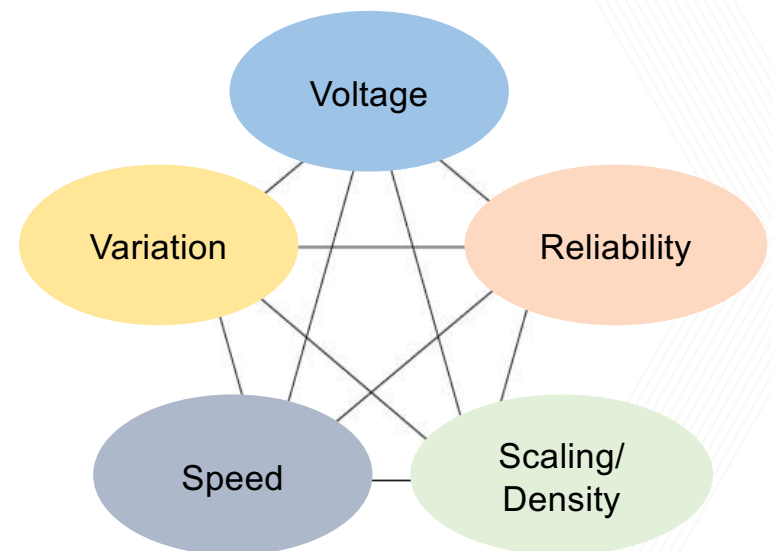
TABLE II. Average, 3-sigma and percentage of prediction error

	TCAD	ML-based prediction		
	μ	μ	3σ	Error
HVT [V]	1.05	1.05	0.08	1.2%
LVT [V]	-0.53	-0.53	0.07	2.0%
I_{on} [μA]	6.68	6.68	1.01	2.1%
SS [mV/dec]	94.52	94.48	9.0	1.6%

G. Choe, P. V. Ravindran, A. Lu, J. Hur, M. Lederer, A. Reck, S. Lombardo, N. Afroze, J. Kacher, A. I. Khan, S. Yu, "Machine learning assisted statistical variation analysis of ferroelectric transistors: from experimental metrology to predictive modeling," IEEE Symposium on VLSI Technology and Circuits (VLSI) 2022.

Fundamental questions

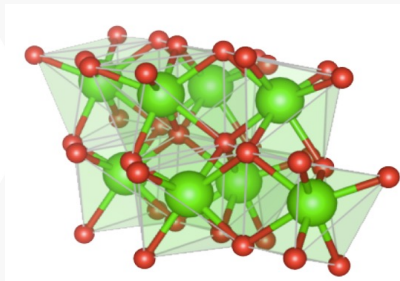
- 1 What is(are) the switching paths?
- 2 What is the nature of the grain boundaries?
- 3 What controls the microstructure in poly-X heterostructures?
- 4 What is the nature of interfaces in poly-X heterostructures?



What is the future of ferroelectric field-effect transistors?

Ferroelectric field-effect transistors (FEFETs)

Ferroelectric Oxide



Properties of
Ferroelectric oxides

Non-volatility and
hysteresis

Plasticity,
Meta-plasticity and
Anti-plasticity

Negative dielectric
permittivity/negative
capacitance

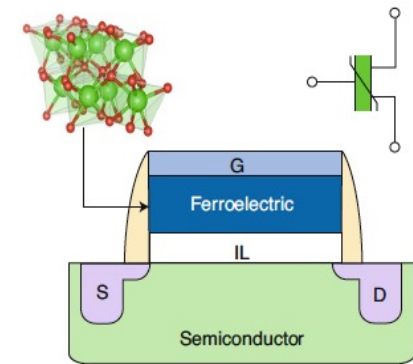
Stochasticity

Transistor
physics

Transconductance
gain

Circuit-level design

Ferroelectric field-effect transistor

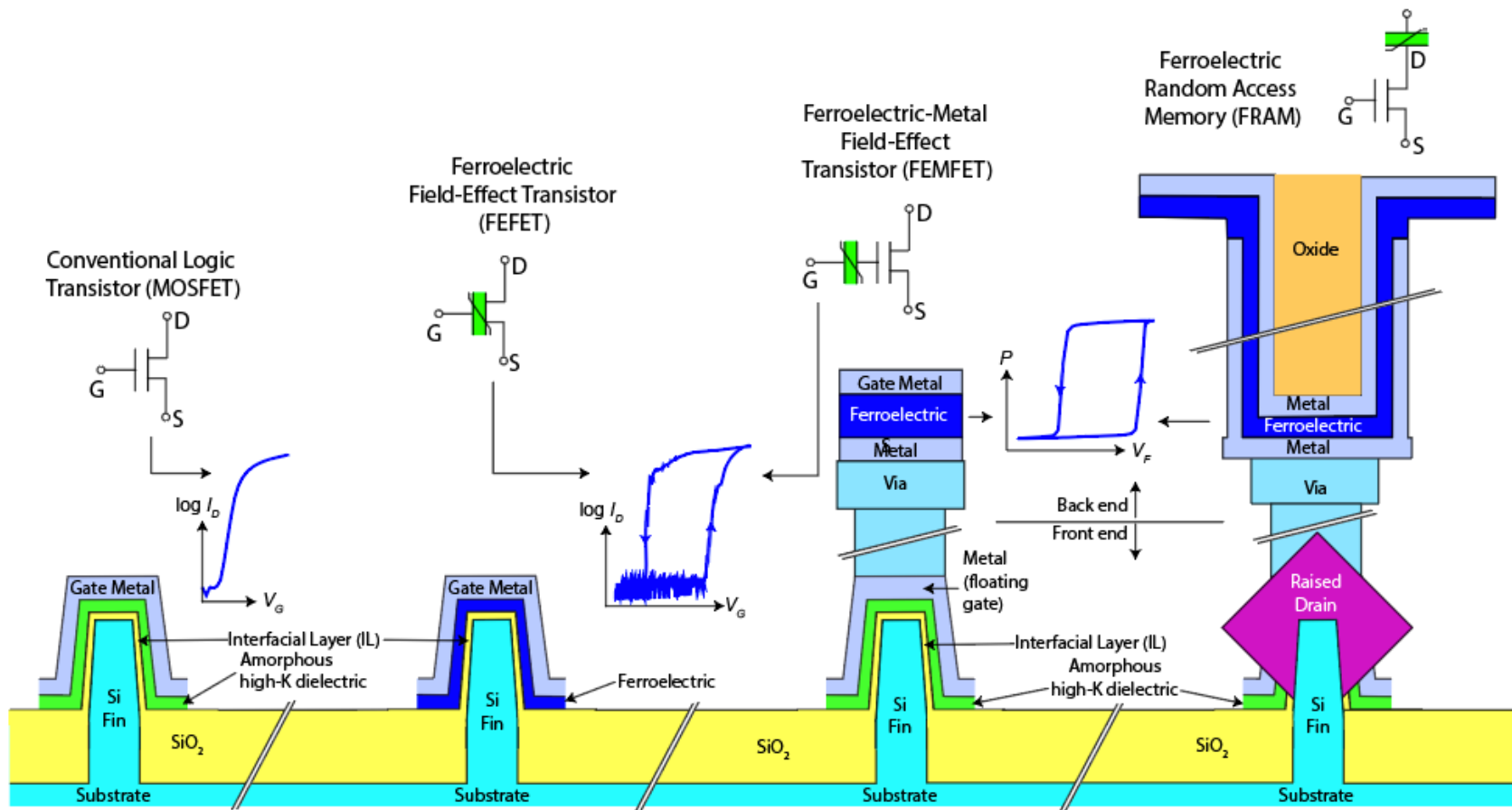


Properties enabled by
a transistor structure

Ferroelectric FET is one of most versatile transistor technologies – ever conceived.

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

Ferroelectric devices (1 of 2)

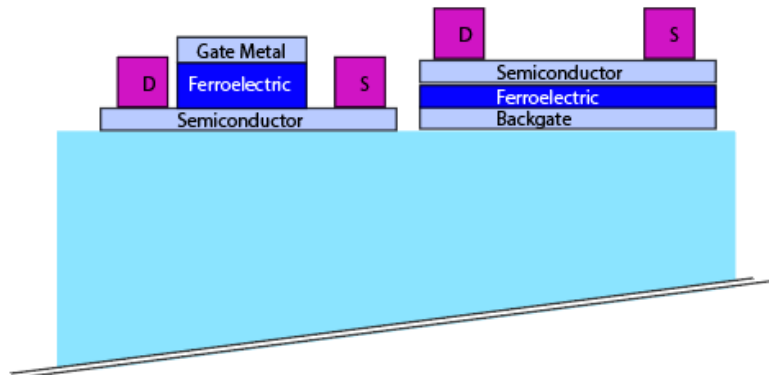


Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

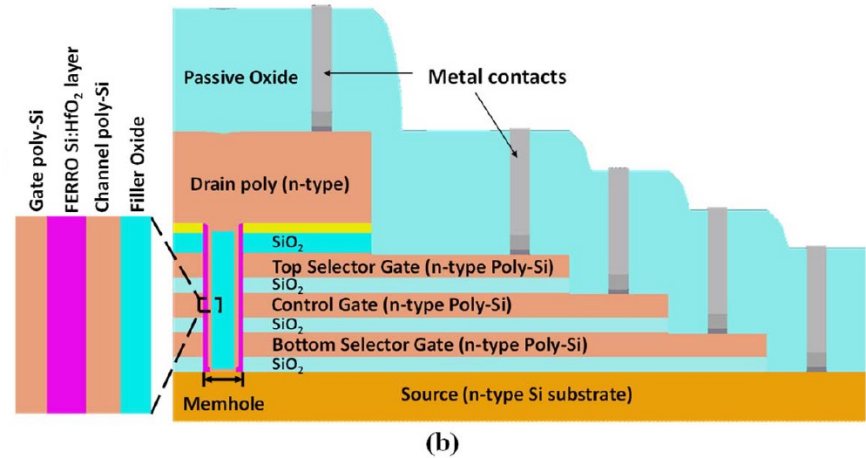
Ferroelectric devices (2 of 2)

BEOL FEFET

Ferroelectric
Field-Effect Transistor
(FEFET)



Vertical FEFET for NAND Storage



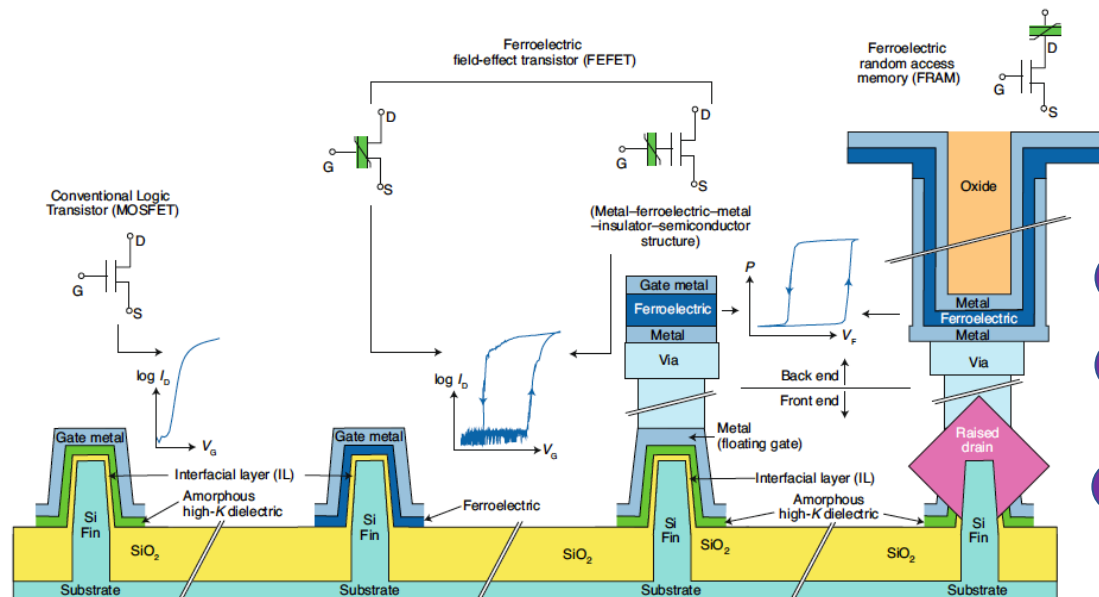
Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

The era of ferroelectronics

The next wave of exponential growth of the semiconductor industry depends on how well the electronic hardware can support the explosion of data-centric computing.

Ferroelectric technology will be a key component because of

- 1 Performance
- 2 Energy and area efficiency
- 3 Logic and memory functionalities



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

Our team



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Ravindran



Chinsung
Park



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Afroze



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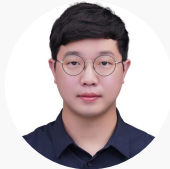
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Dr. Mengkun
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