Ferroelectronics for next generation memory and NAND storage technology

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IEEE Electron Devices Society–Santa Clara Valley/San Francisco Chapter
1/19/2024

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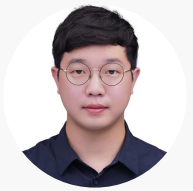
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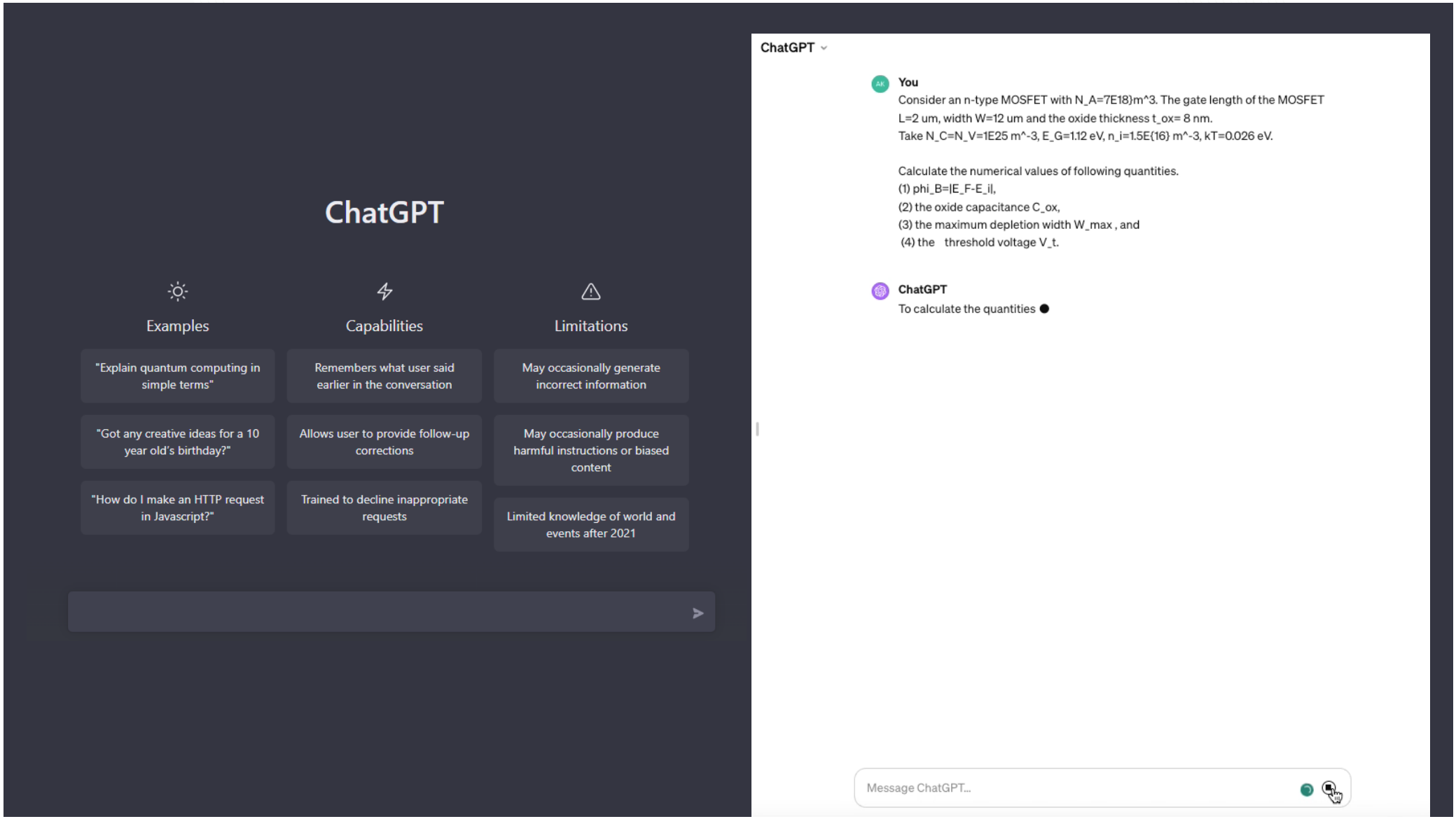
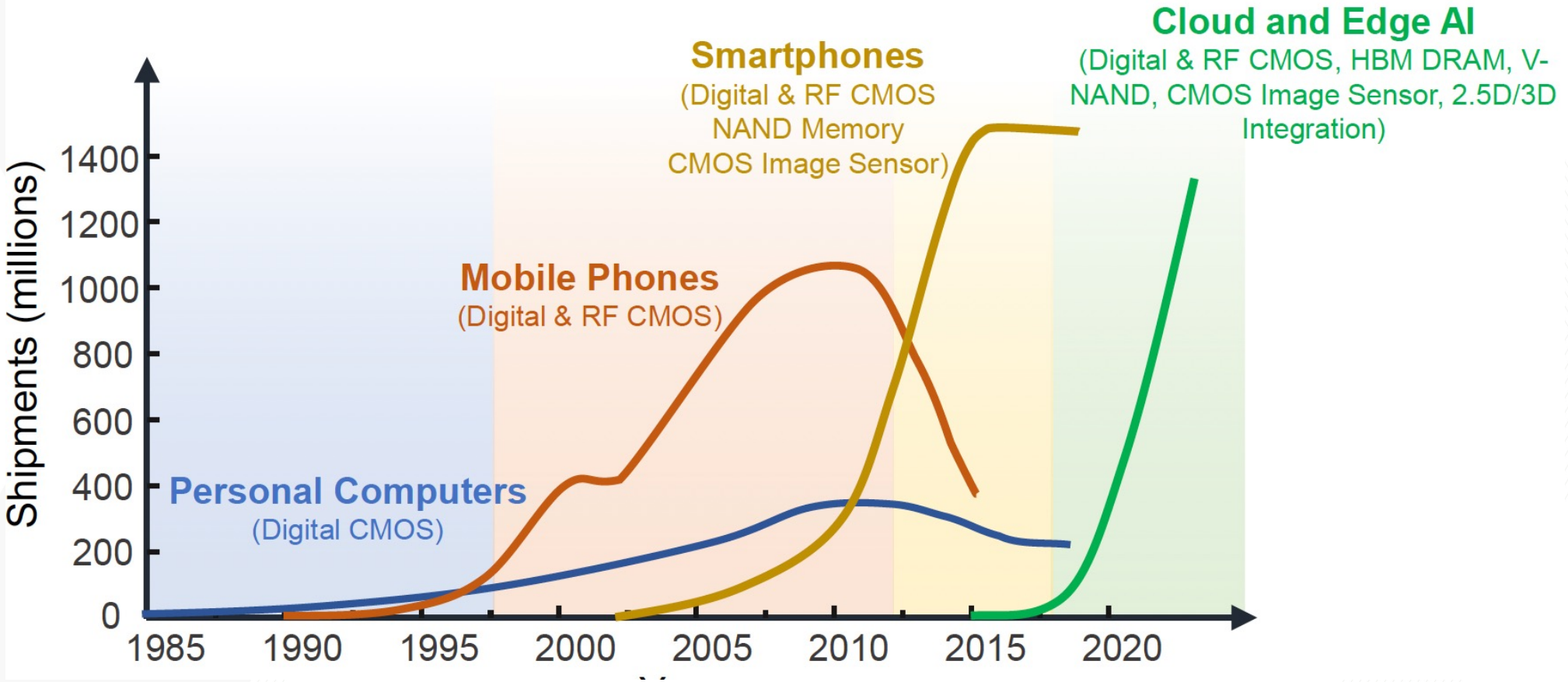

ChatGPT
Examples
"Explain quantum computing in simple terms"
"Got any creative ideas for a 10 year old's birthday?"
"How do I make an HTTP request in Javascript?"
Capabilities
Remembers what user said earlier in the conversation
Allows user to provide follow-up corrections
Trained to decline inappropriate requests
Limitations
May occasionally generate incorrect information
May occasionally produce harmful instructions or biased content
Limited knowledge of world and events after 2021
ChatGPT
You
Consider an n-type MOSFET with N_A=7E18}m^3. The gate length of the MOSFET L=2 um, width W=12 um and the oxide thickness t_ox= 8 nm.
Take N_C=N_V=1E25 m^-3, E_G=1.12 eV, n_i=1.5E{16} m^-3, kT=0.026 eV.
Calculate the numerical values of following quantities.
(1) phi_B=|E_F-E_i|,
(2) the oxide capacitance C_ox,
(3) the maximum depletion width W_max , and
(4) the threshold voltage V_t.
ChatGPT
To calculate the quantities
Message ChatGPT...

How the computing paradigms have evolved



Adapted from: Datta, EDTM 2023
https://www.economist.com/briefing/2015/02/26/the-truly-personal-computer
https://www.statista.com/chart/12798/global-smartphone-shipments/

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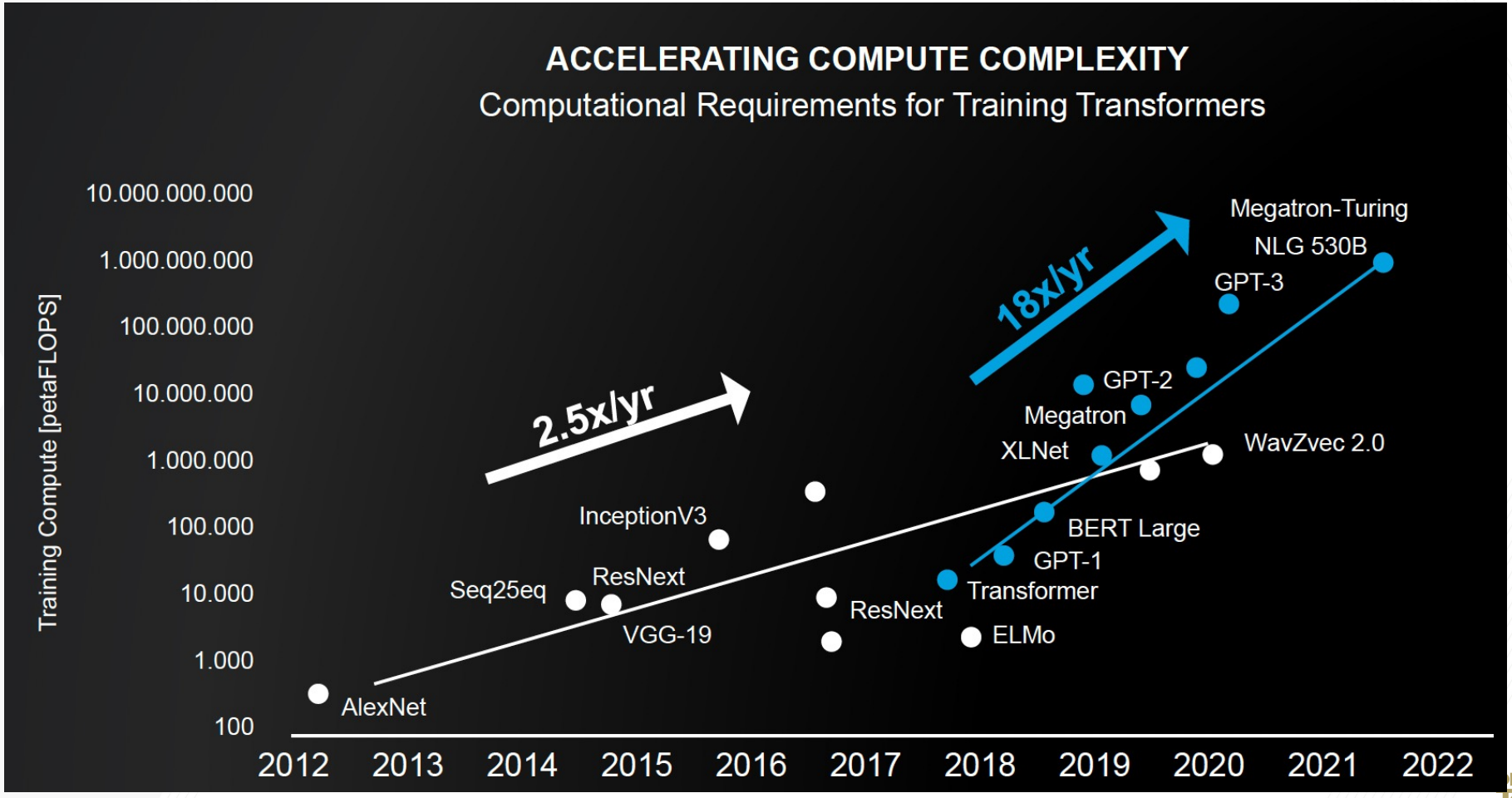
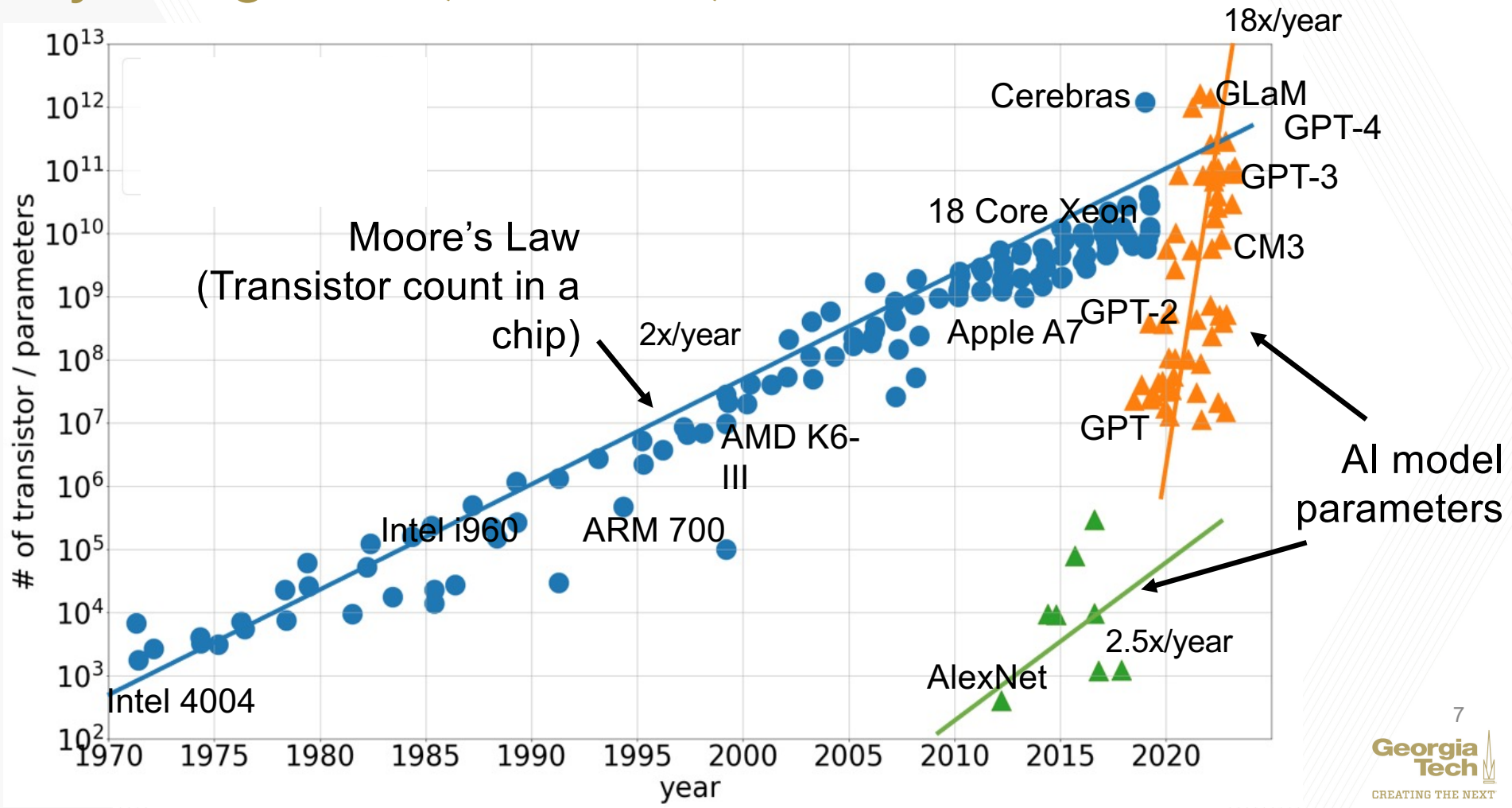
Evolution of AI model parameter count



Source: NVIDIA

A story of algorithm, software, and hardware



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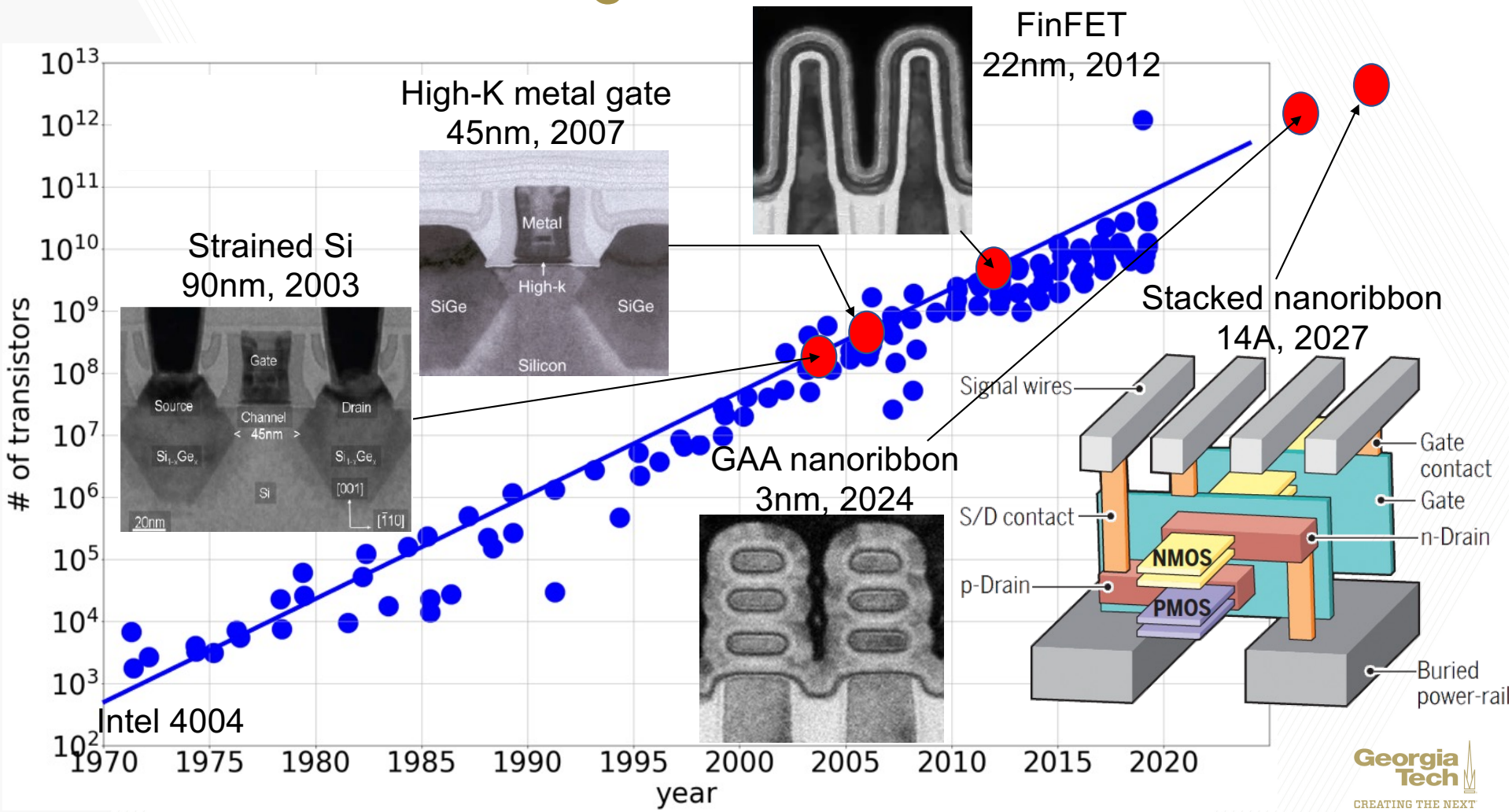
Innovation at the core - Logic



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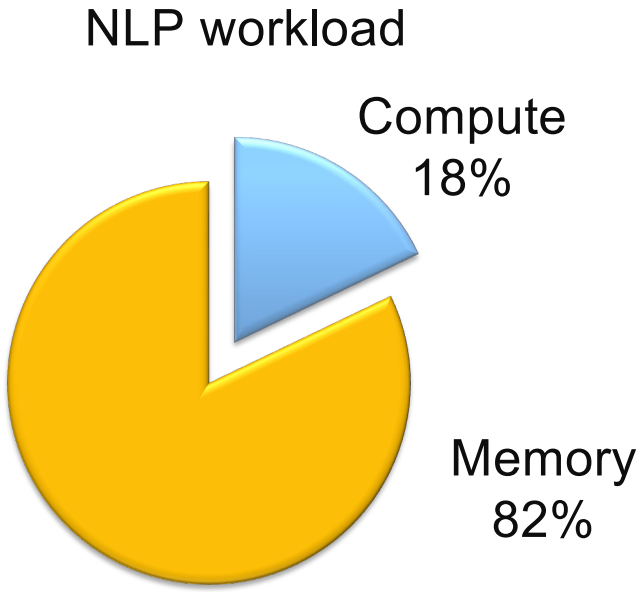
Innovation at the core – Memory / Cache

The primary bottleneck for performance, energy efficiency, and sustainability in AI computing is memory – Cache, main memory, storage



We want memory systems to be of low latency, high bandwidth, high capacity, and high energy efficiency.

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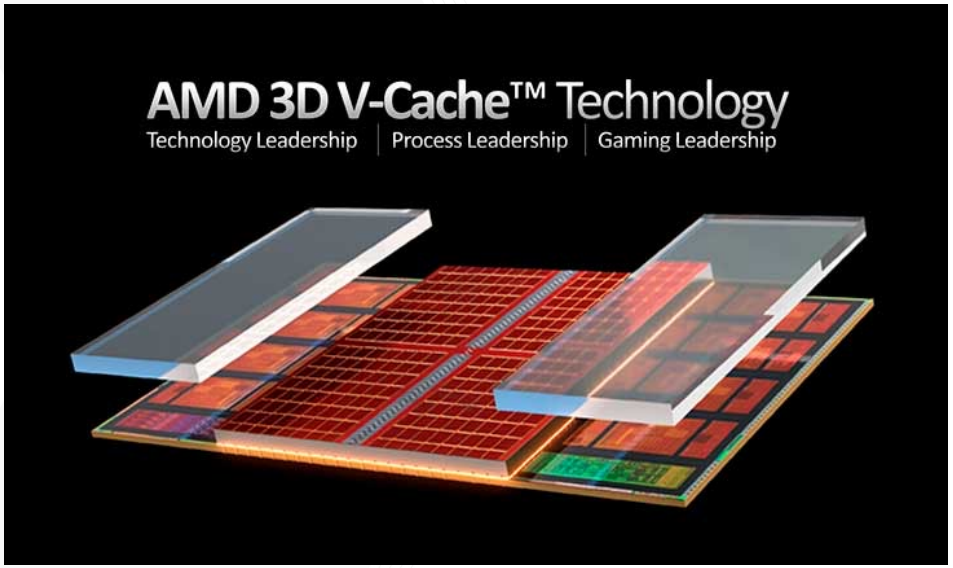
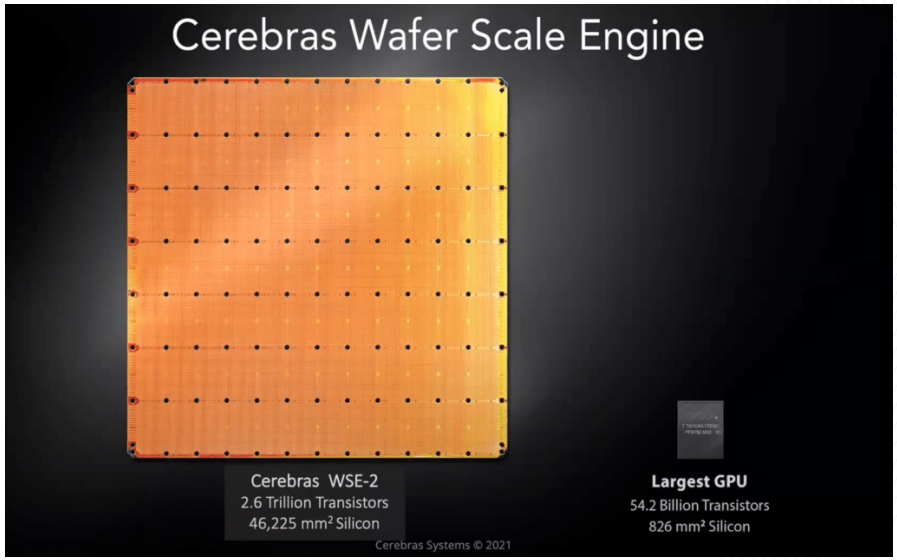
Innovation at the core – Memory / Cache

The primary bottleneck for performance, energy efficiency, and sustainability in AI computing is memory – Cache, main memory, storage



Ryzen - 64 MB L3 Cache extension
EPYC GENOAX 1GB L3 Cache

https://www.techpowerup.com/review/amd-ryzen-7-5800x3d/2.html
https://www.avadirect.com/blog/amd-3d-v-cache-technology/
https://www.anandtech.com/show/18914/amd-epyc-genoax-cpus-with-11gb-of-l3-cache-shipping-now



WSE2 - 60 GB on chip memory

https://www.semianalysis.com/p/cerebras-wafer-scale-hardware-crushes

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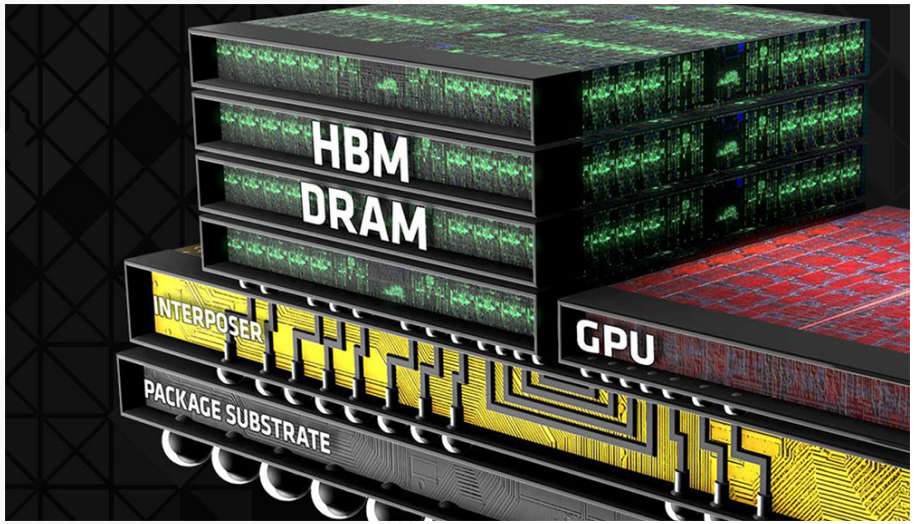
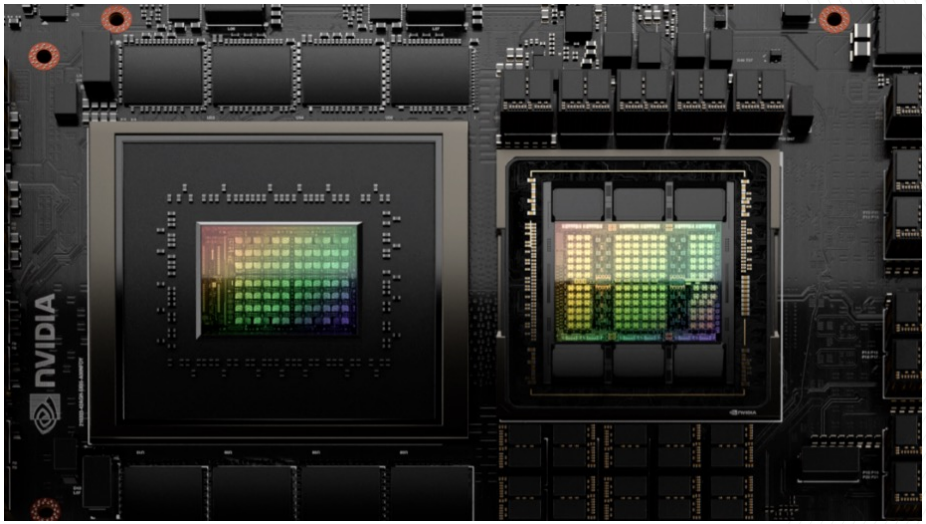
Innovation at the core – Memory / Main memory

The primary bottleneck for performance, energy efficiency, and sustainability in AI computing is memory – Cache, main memory, storage



AMD Fiji GPU architecture - Radeon R9 Fury X graphics, introduced in 2015.

https://pcper.com/2015/05/high-bandwidth-memory-hbm-architecture-amd-plans-for-the-future-of-gpus/



GH200 Grace Hopper Superchip –HBM3e

https://www.hpcwire.com/2023/08/09/nvidia-adds-faster-hbm3e-memory-to-the-gh200-grace-hopper-platform/

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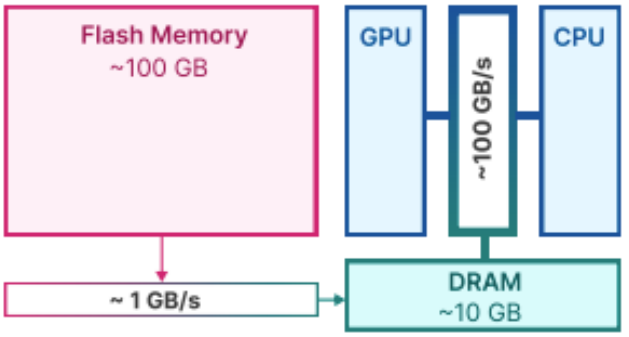
Innovation at the core – Memory / Storage

The primary bottleneck for performance, energy efficiency, and sustainability in AI computing is memory – Cache, main memory, storage

LLM *in a flash*:
Efficient Large Language Model Inference with Limited Memory

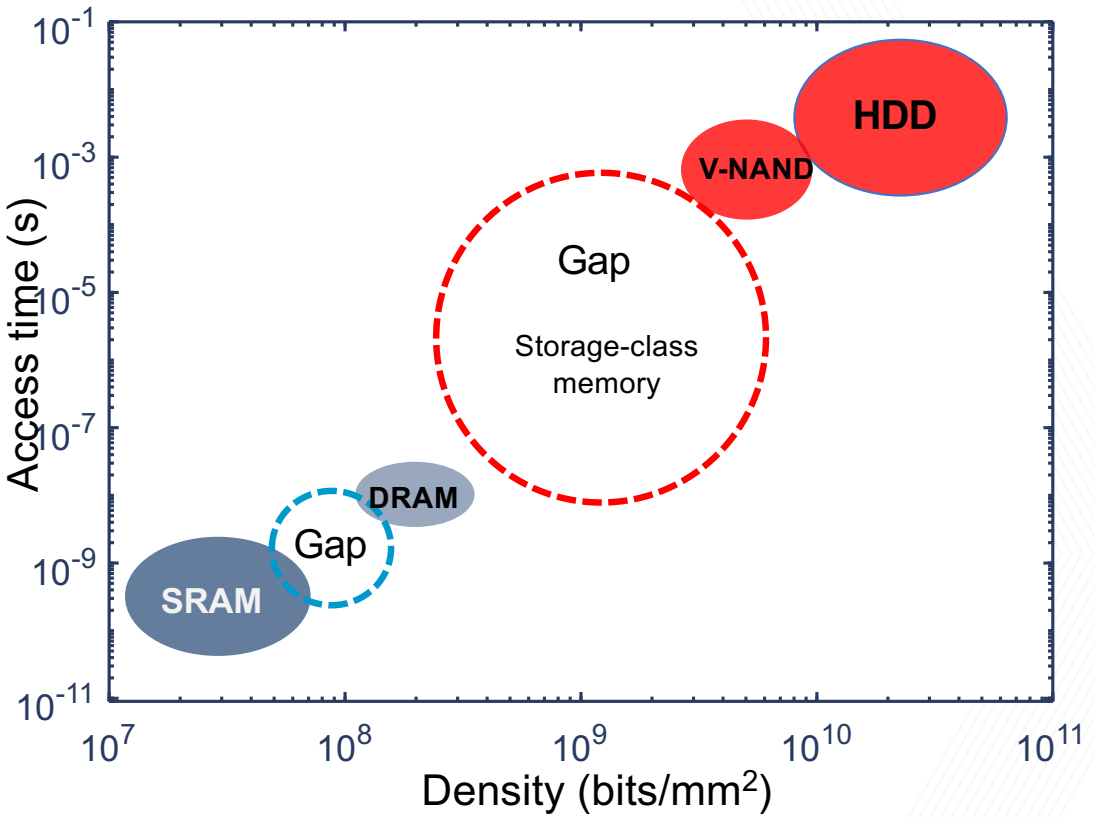
Keivan Alizadeh, Iman Mirzadeh*, Dmitry Belenko*, S. Karen Khatamifard, Minsik Cho, Carlo C Del Mundo, Mohammad Rastegari, Mehrdad Farajtabar
Apple †



(a) Bandwidth in a unified memory architecture

https://arxiv.org/pdf/2312.11514.pdf

Memory Landscape

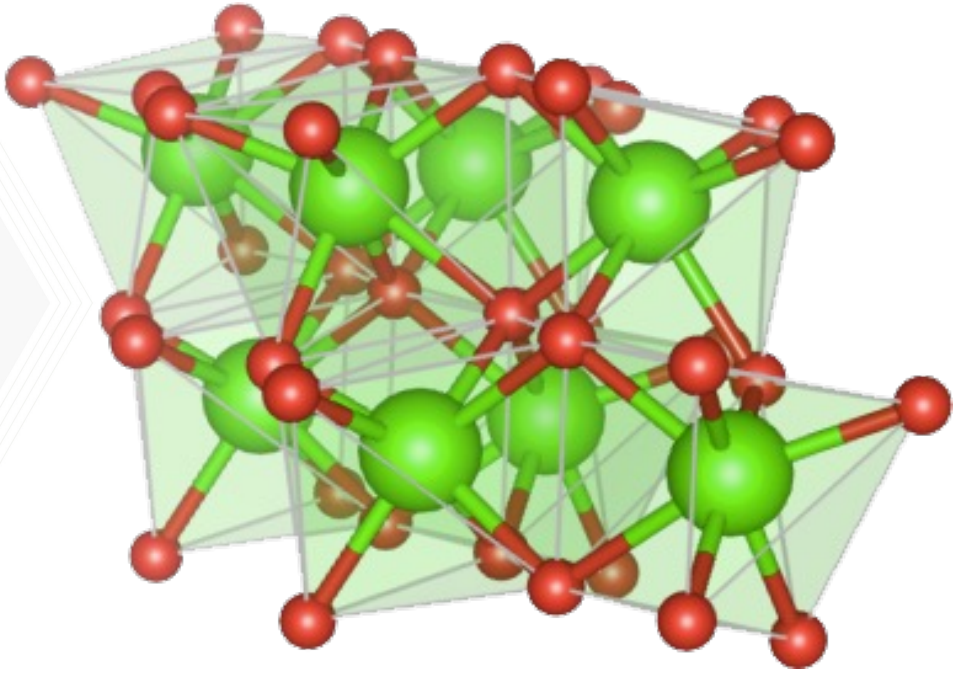


Overarching goal:

- Go to the bottom left corner!
  - Mind the gaps!

100 Tb/s
33k I/O

Let’s dive down to devices and materials



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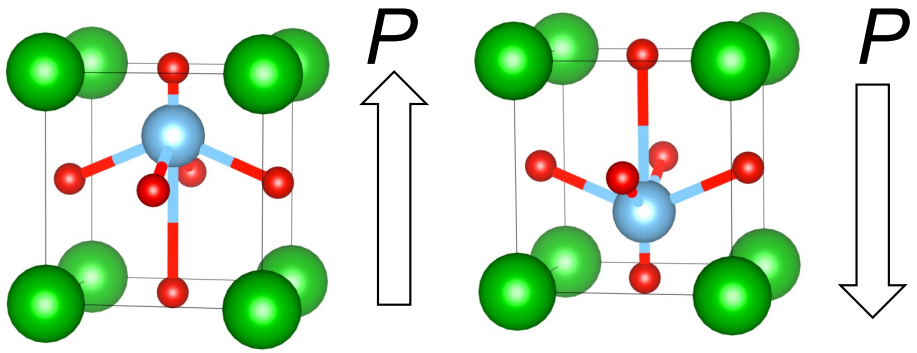
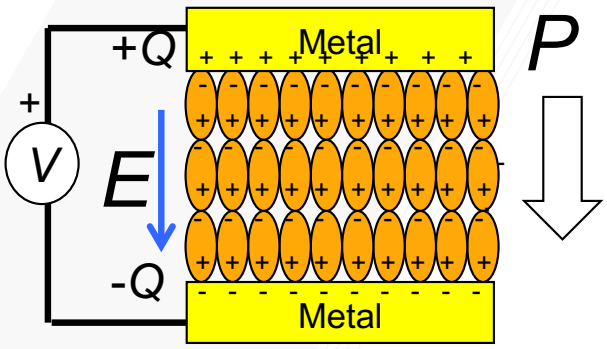
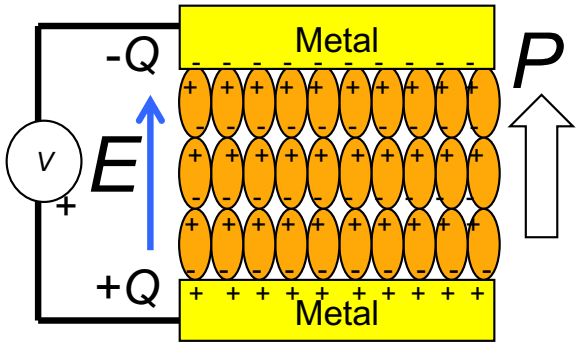
Ferroelectricity

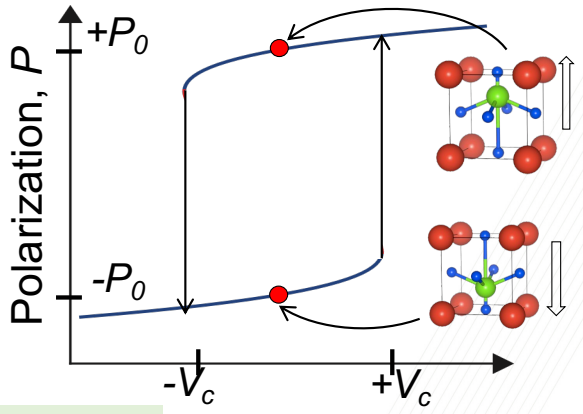
Classical Ferroelectric
$PbTiO_3$, $BaTiO_3$ etc.

Emerging CMOS compatible
Ferroelectrics:
Doped HfO_2









A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

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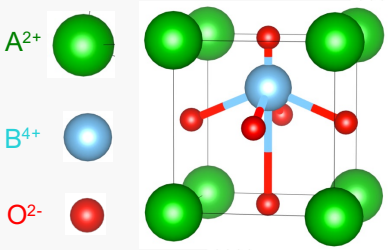
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for for code storage in microcontrollers.

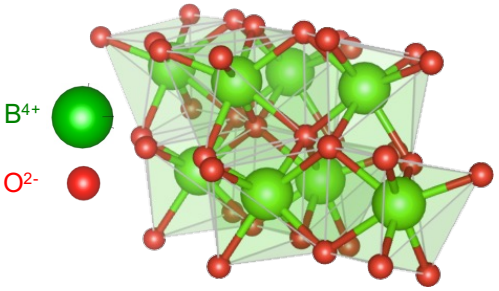
2. Controlled annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al. Appl. Phys. Lett*. 99, 112904 (2011)
- Boscke *et al. 2011 IEEE Int. Electron Devices Meeting.* p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al. Nano Lett.* 12, 4318 (2012)

Perovskite-structure ferroelectric oxide (ABO_3)



Fluorite-structure ferroelectric oxide (BO_2)



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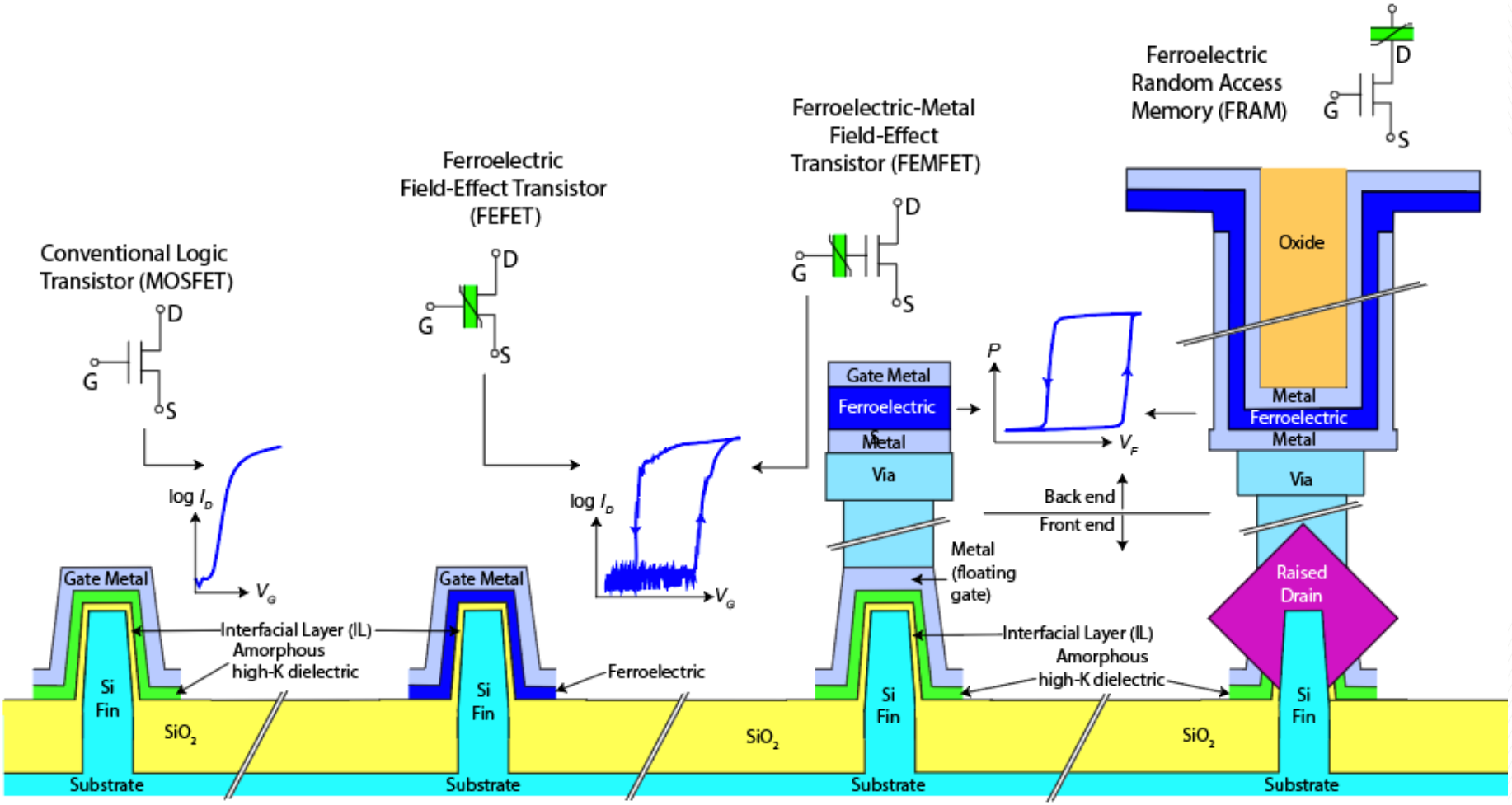
Ferroelectric devices (1 of 2)



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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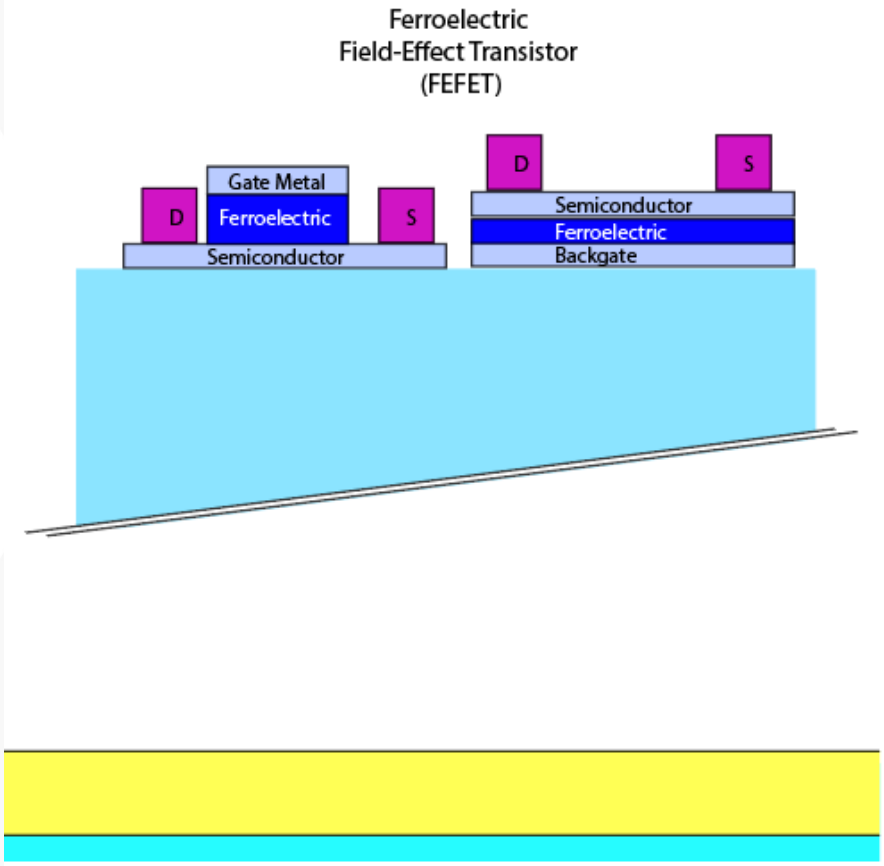
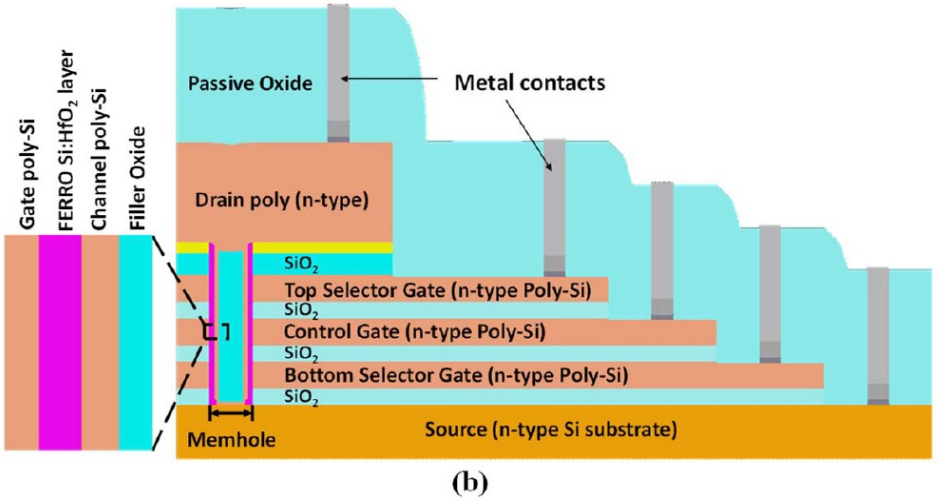
Ferroelectric devices (2 of 2)

BEOL FEFET



Vertical FEFET for NAND Storage



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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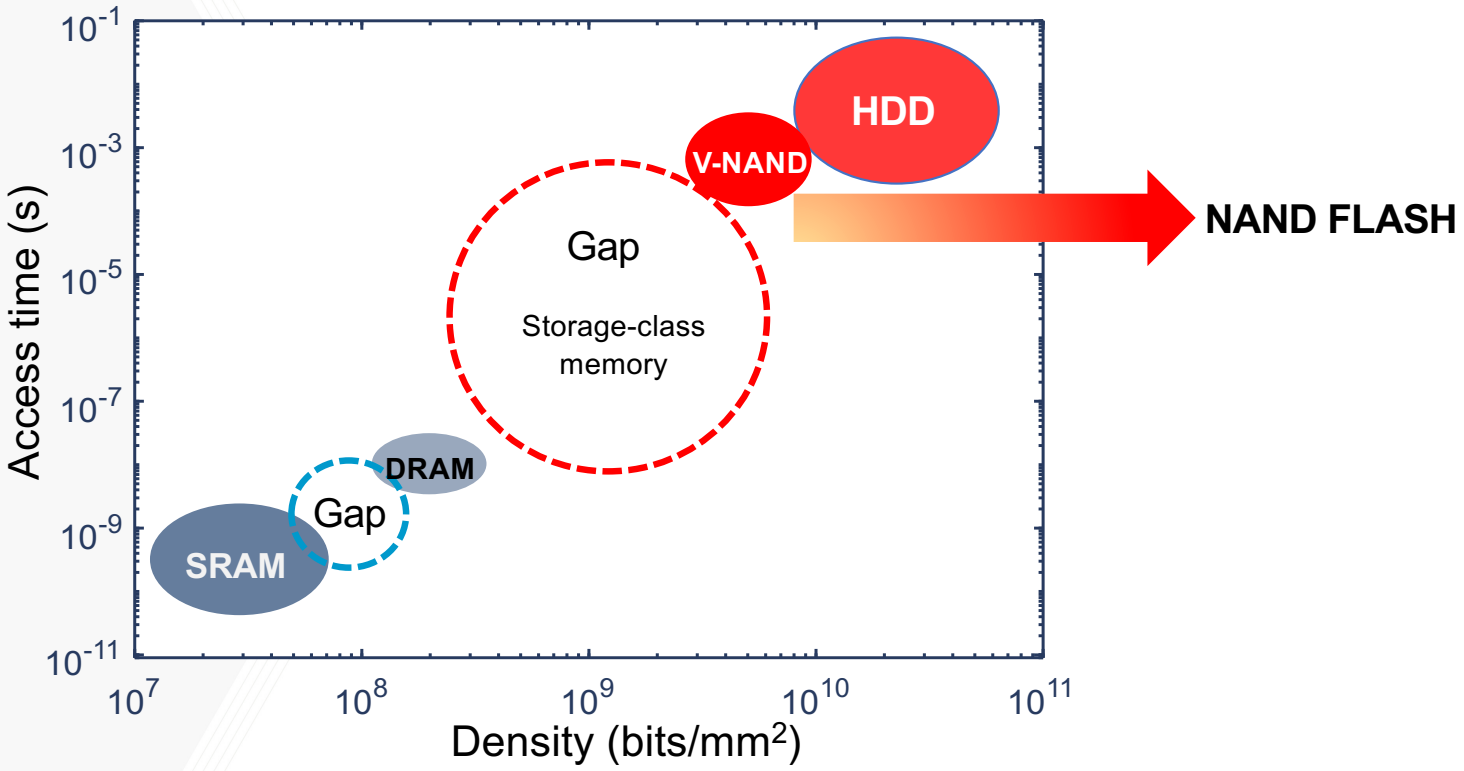
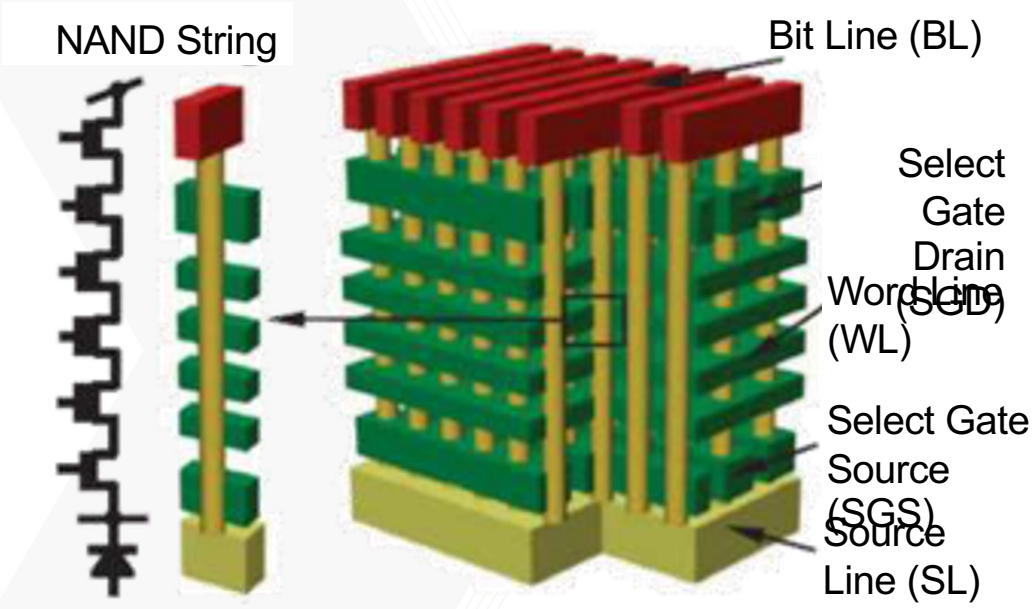
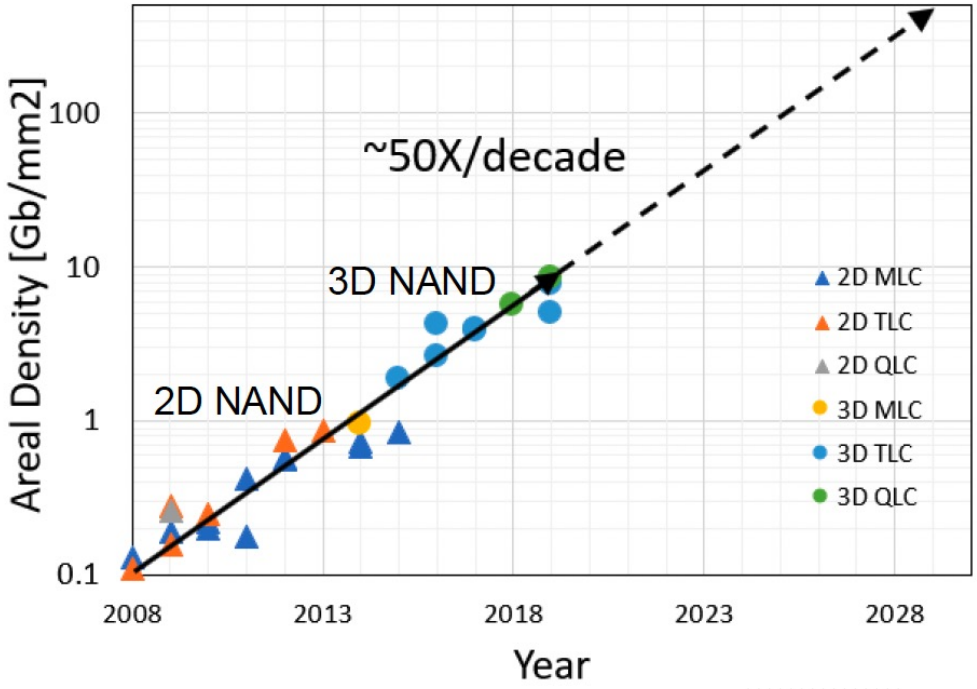
Opportunity for NAND



Vertical NAND Scaling



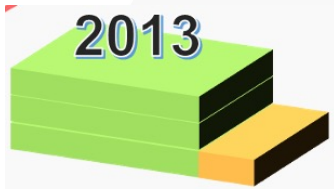
Tanaka et al., 2007 VLSI Tech.



A. Goda, IEEE, TED 2020

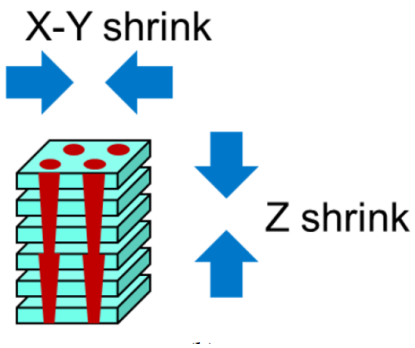
Relentless innovations have led to a 50x improvement in bit arial density per decade.

Vertical NAND Scaling

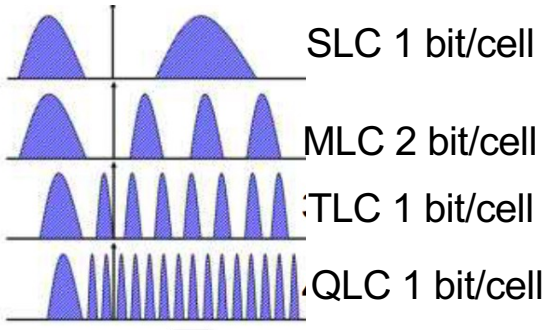


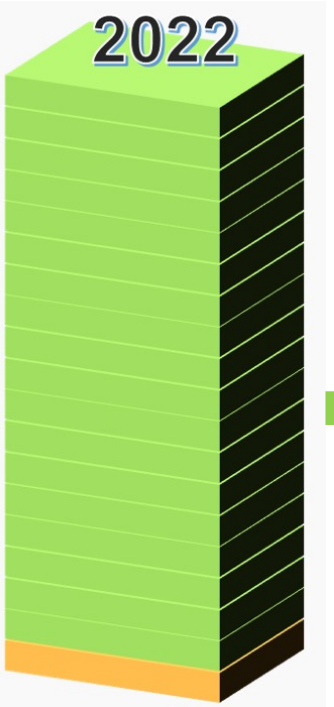
Samsung 24 MLC

Physical scaling



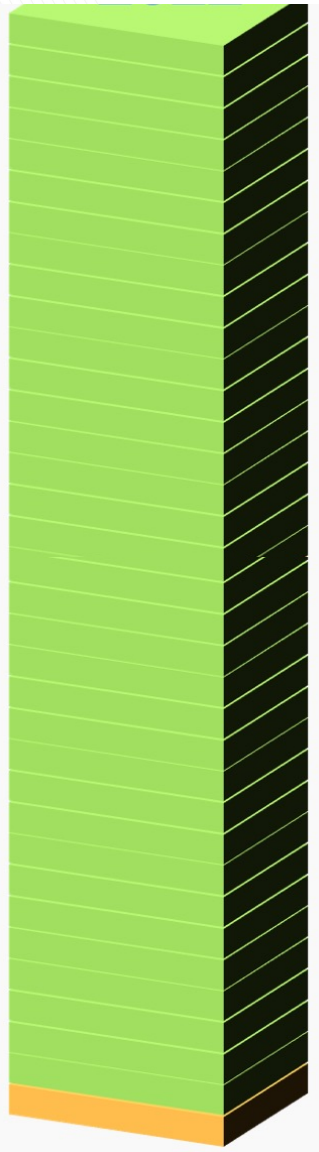
Logical scaling





Samsung 236L TLC
SK Hynix 238L TLC
Micron 232L TLC
192L QLC

?



Vertical NAND scaling toward 1000 layers

Layer stacking trend

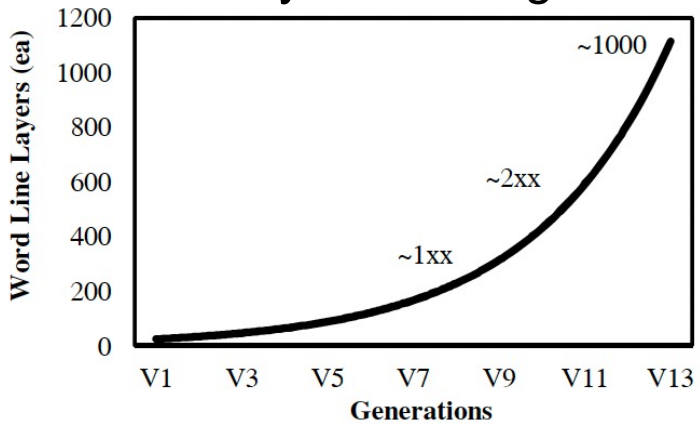


Fig. 1. Number of word line layers by generation

Package thickness limits the NAND chip height.

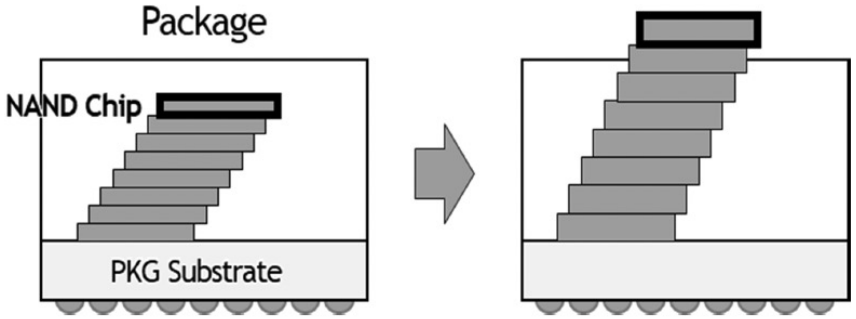
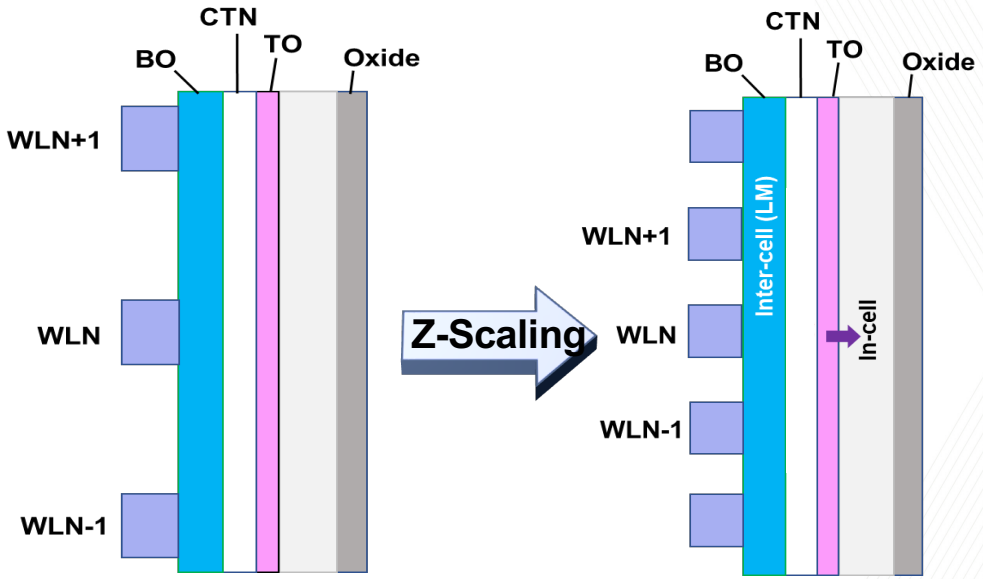


Fig. 4. Package thickness limit with multiple chips

Aggressive Z-scaling is required.

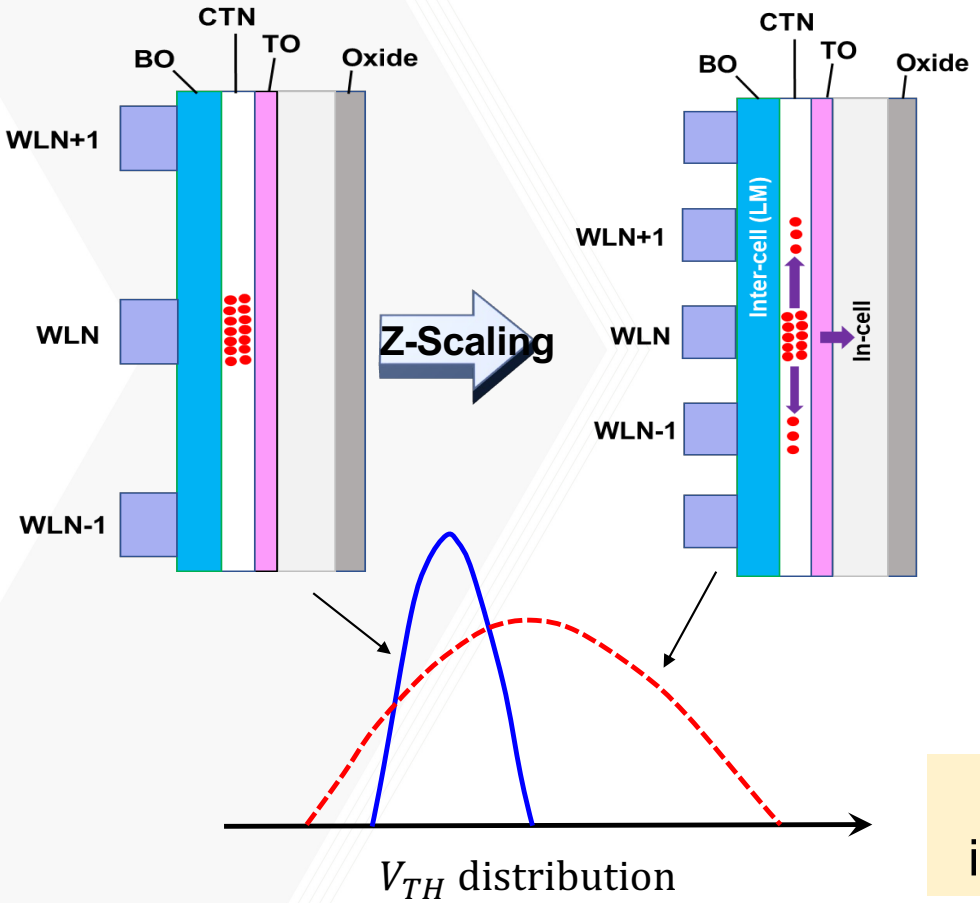


The mold height (cell height) needs to be reduced dramatically.

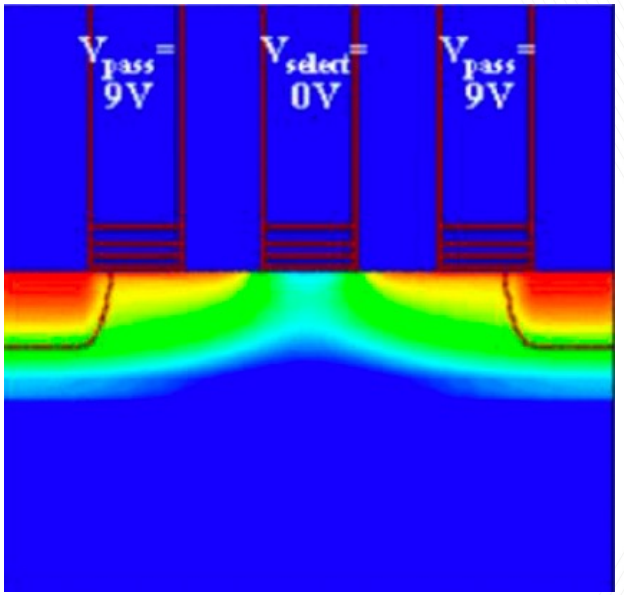
Han et al. Fundamental Issues in VNAND Integration Toward More Than 1K Layers. IEDM 2023. Paper 35.1

Challenges for 1000+ layer vertical NAND

1 Lateral charge migration



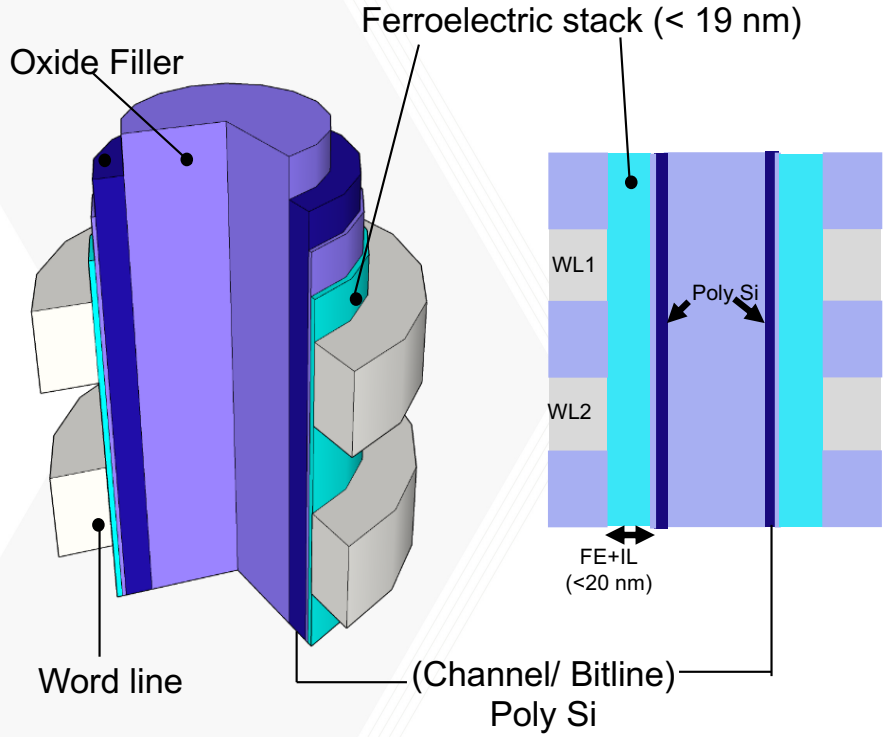
2 High write voltage



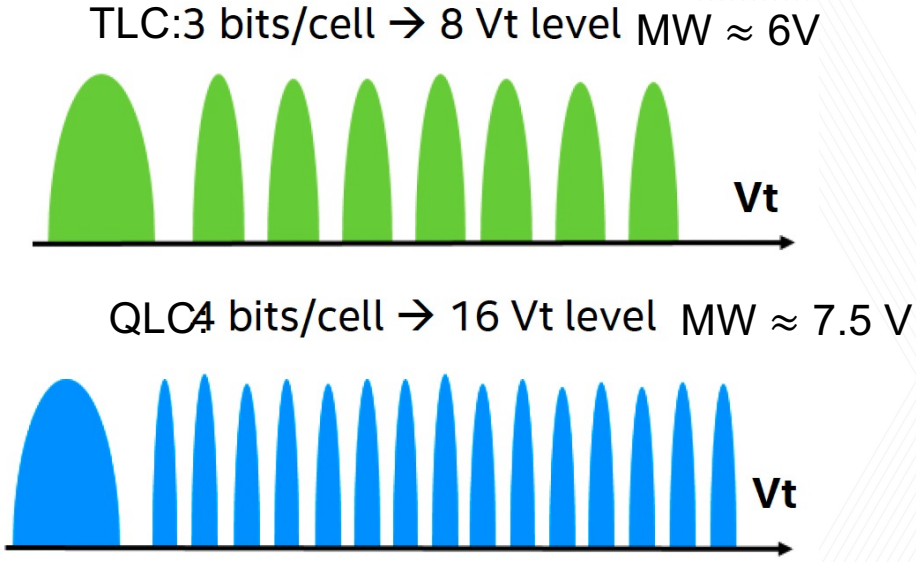
Write voltage of state of the art NAND is >20 V.
Large write voltage affects effective threshold voltage, similar to cell-to-cell interference.

Cell-to-cell interference will significantly increase with aggressive Z-scaling for 1000L VNAND.

Ferroelectric as a replacement for Charge Trap Layer



To accommodate the core-shell structure within the hole diameter of 100 nm of the vertical NAND string, the thickness of the gate stack is limited to ~20 nm



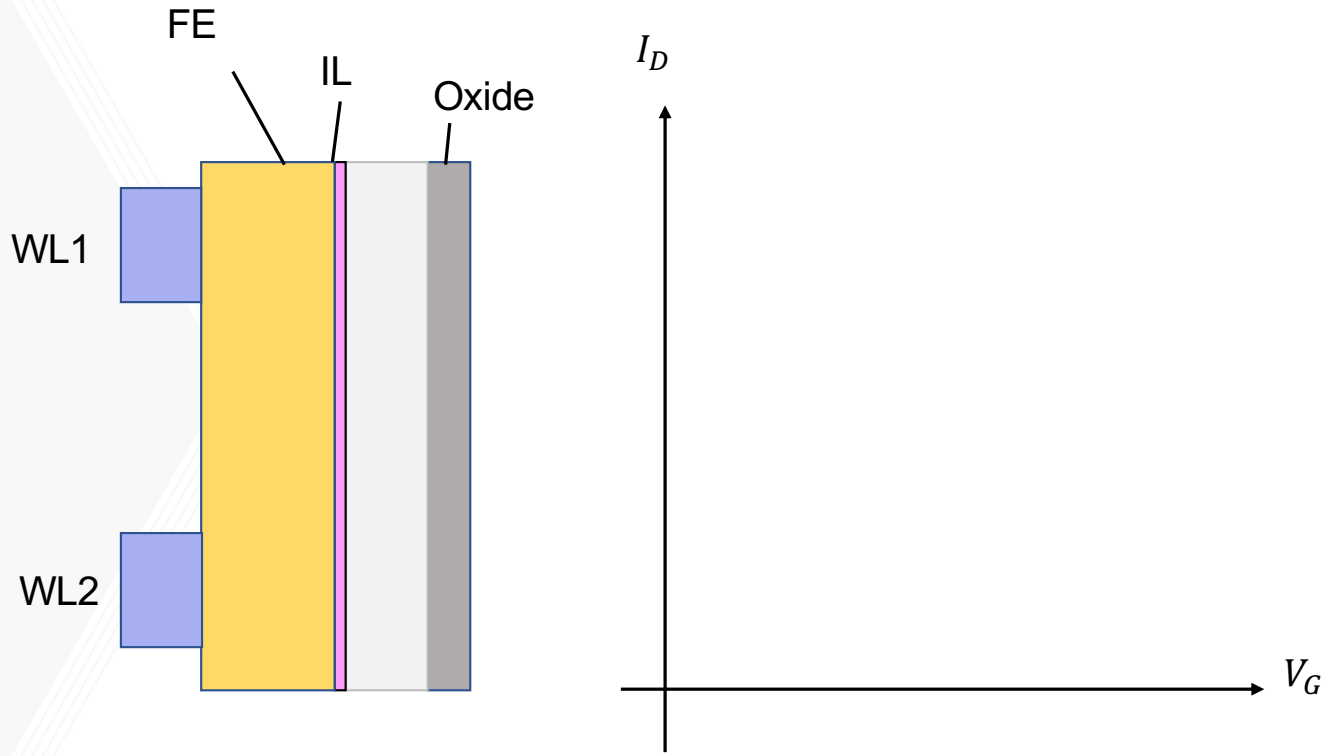
Design constraints

Ferroelectric thickness, $t_{FE} \leq 19$ nm

Write voltage ≤ 15 V

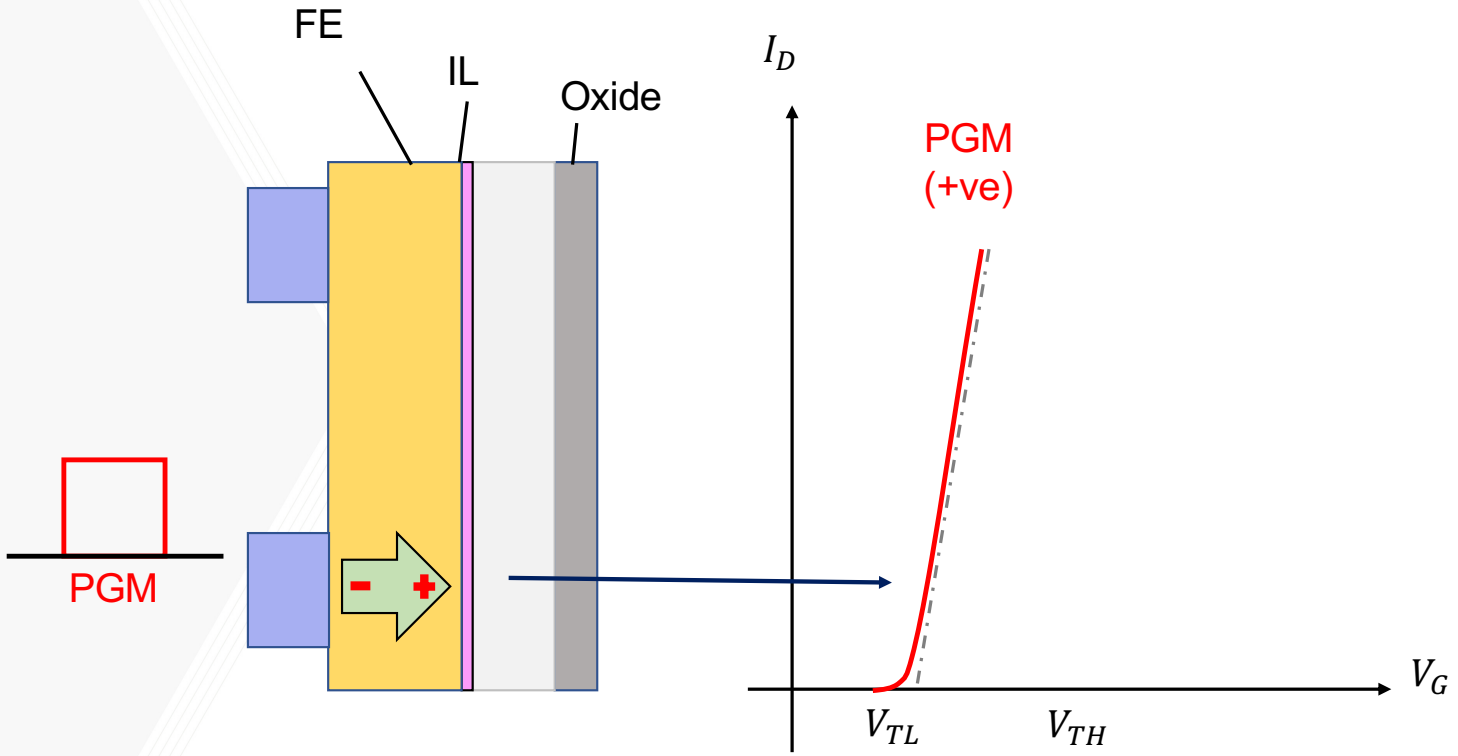
Memory window, MW > 6.5 V

Ferroelectric field-effect transistor



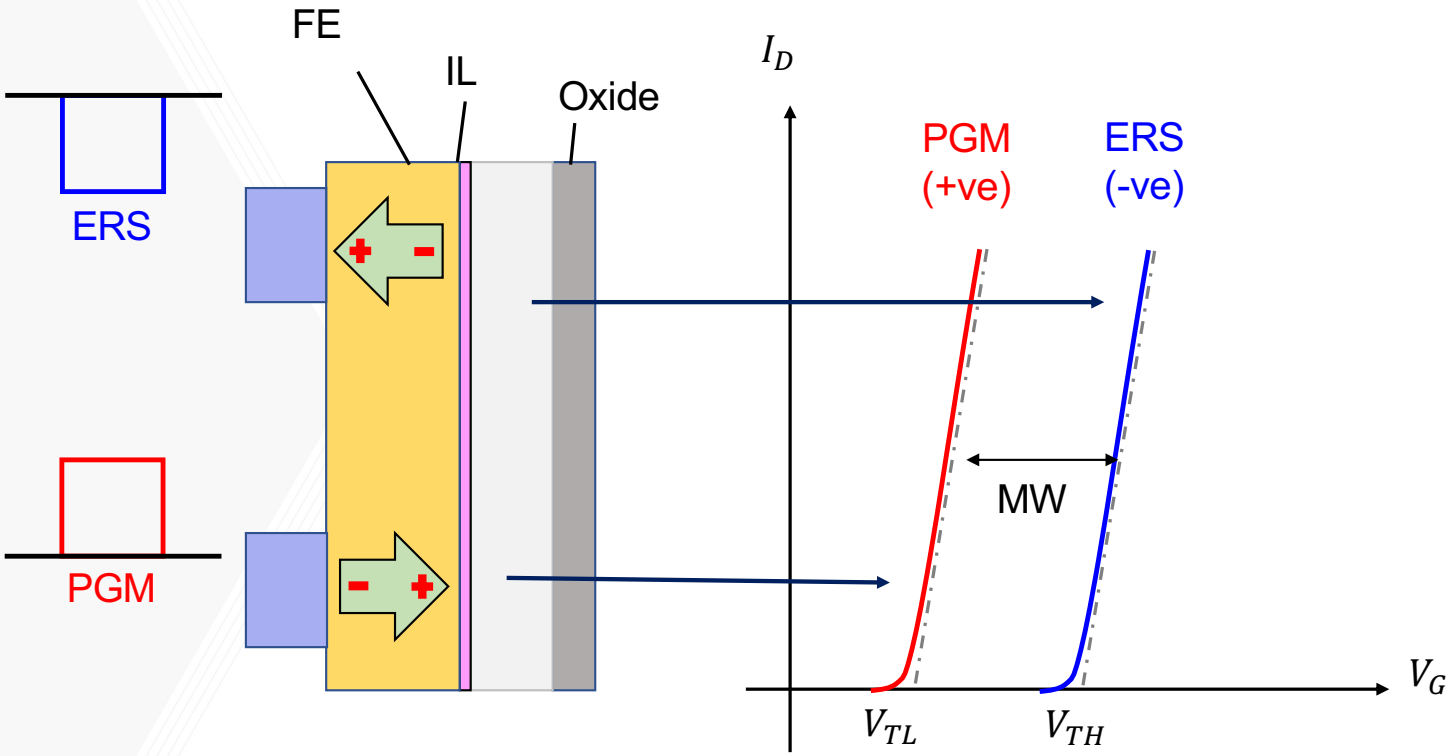
FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the “remnant” polarization.

Ferroelectric field-effect transistor



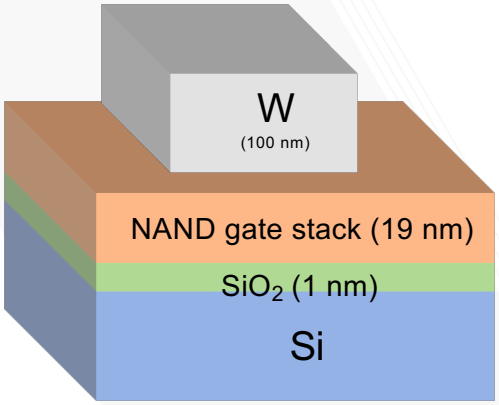
PGM (positive voltage) pulse sets the Vt to high Vt state in FEFET

Ferroelectric field-effect transistor

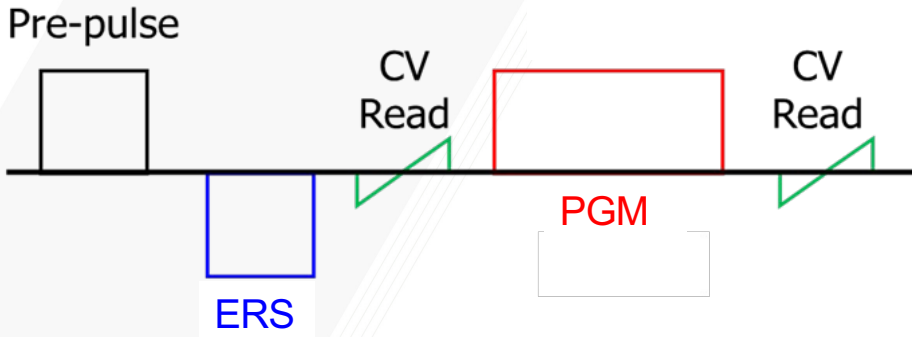


ERS (negative voltage) pulse sets the Vt to high Vt state in FEFET

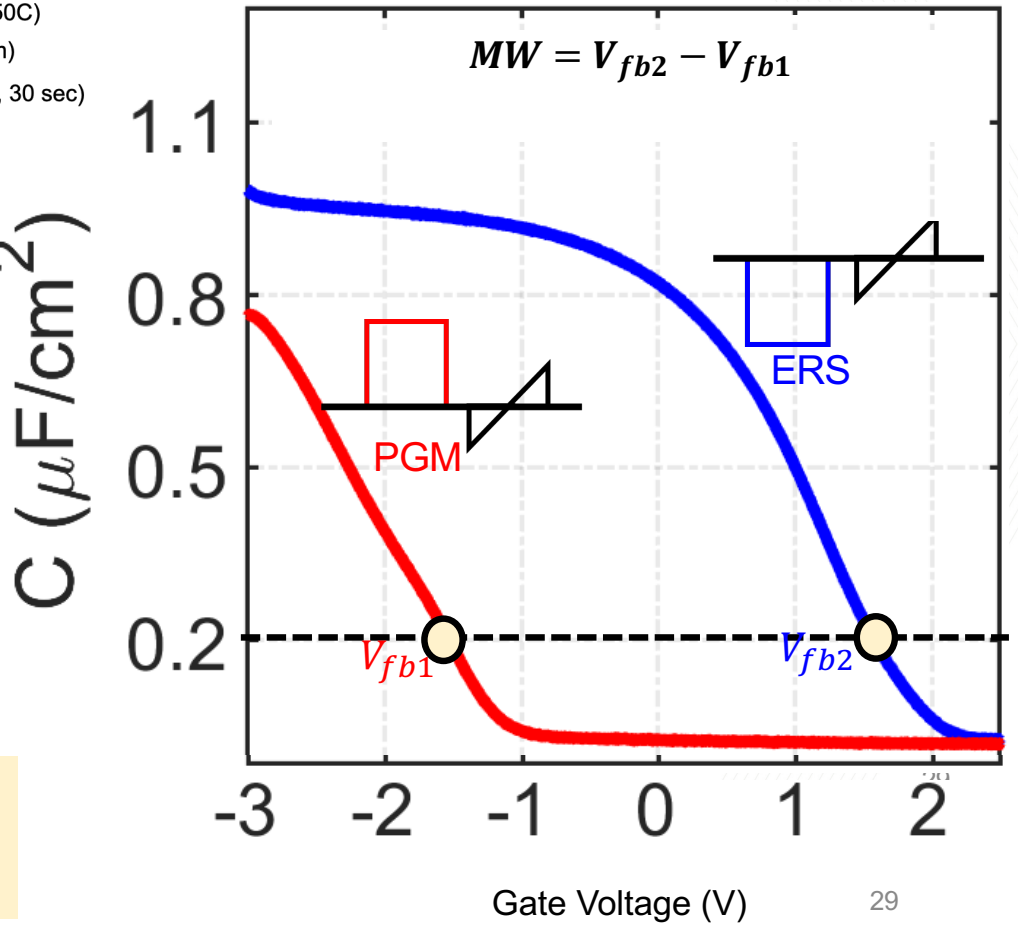
Fabrication and MW measurement



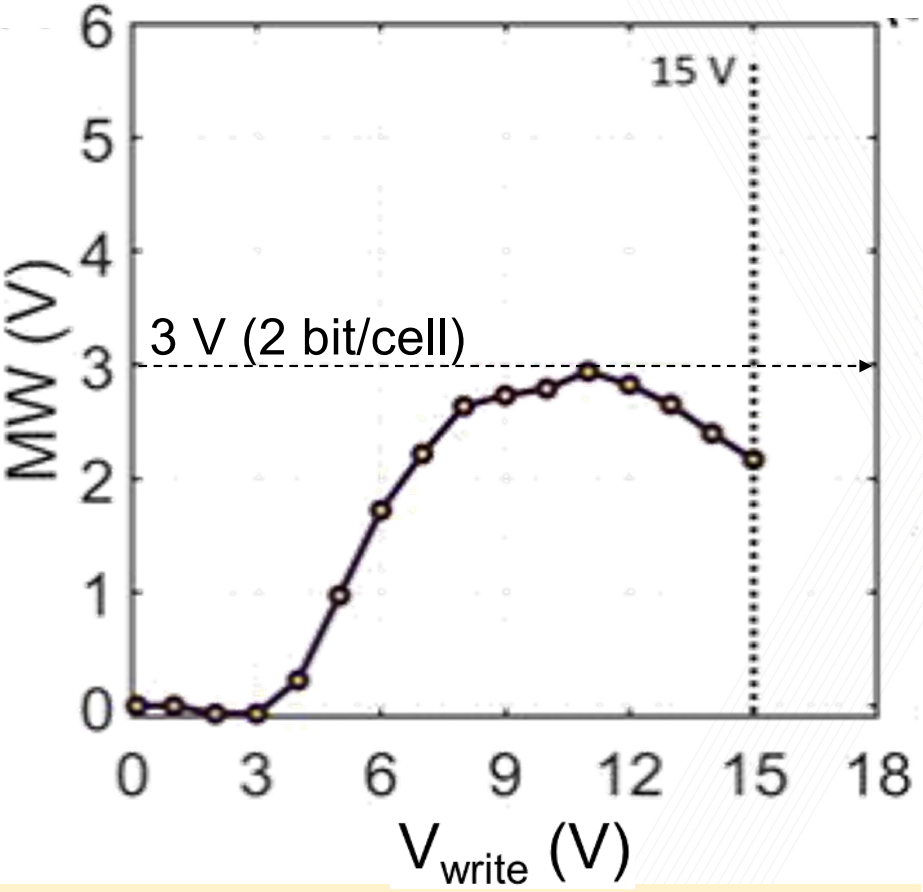
- **Substrate preparation** (RCA clean)
- **Native Oxide** (SC1 for 10 min)
- **NAND gate stack deposition** (Veeco ALD @250C)
- **W top electrode deposition** (sputtered, 100 nm)
- **HZO crystallization annealing** (RTA, N_2, 500C, 30 sec)
- **W Patterning**
- **W Etch** (SF_6:O_2)
- **FGA** (400 C, 30 min)



The MW of the gate stacks were measured from the capacitance-voltage (C-V) curve using constant capacitance

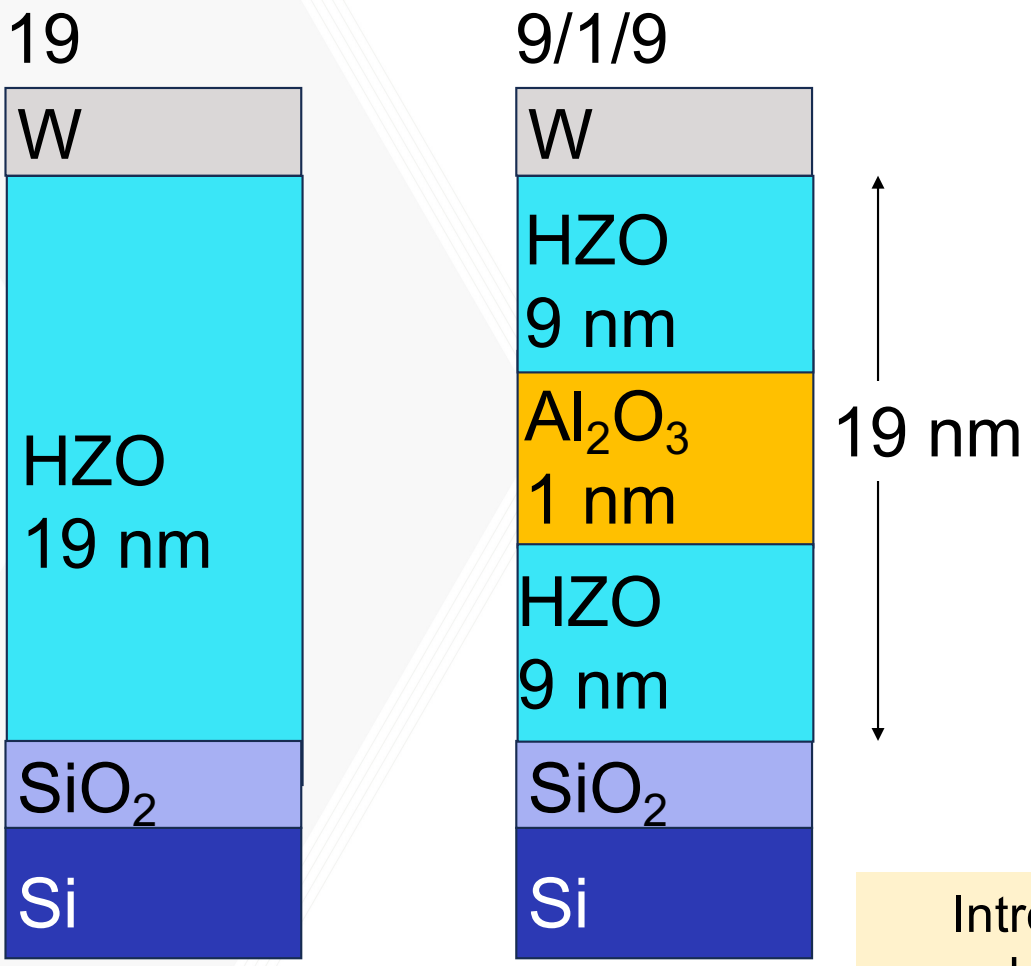


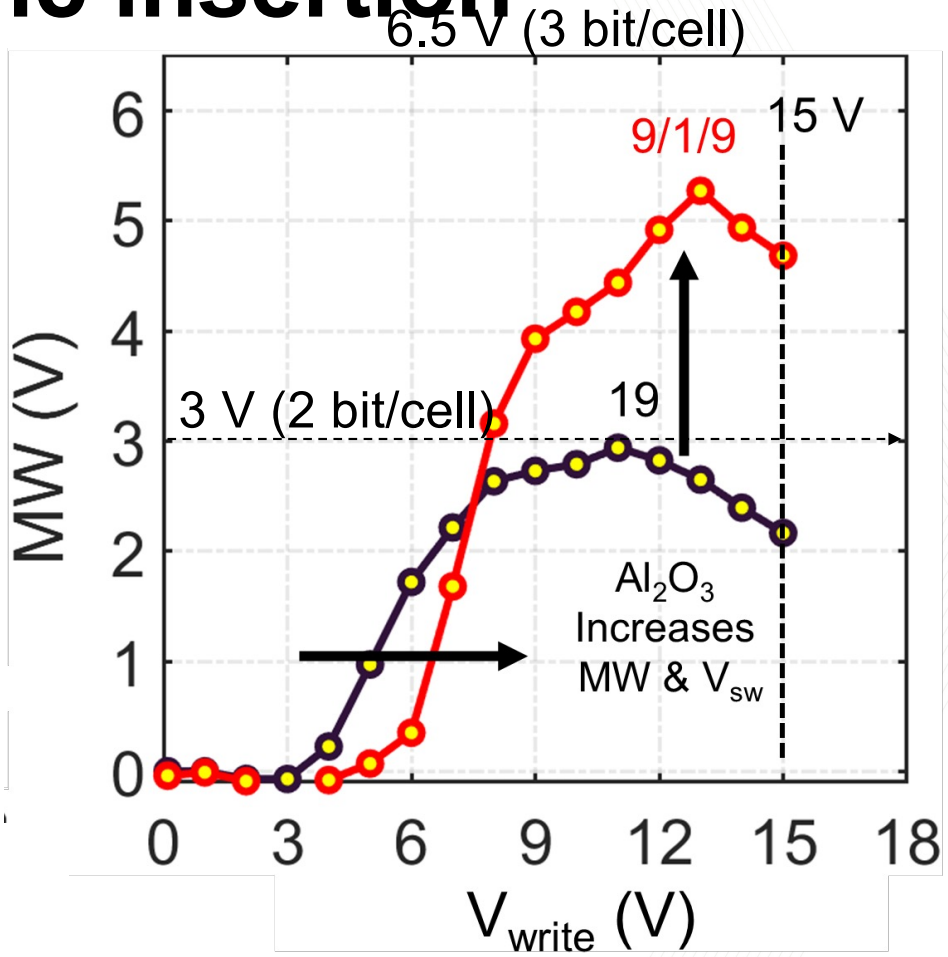
Impact of tunnel dielectric insertion



10 nm HZO layer leads to maximum memory window of 2.9 V.

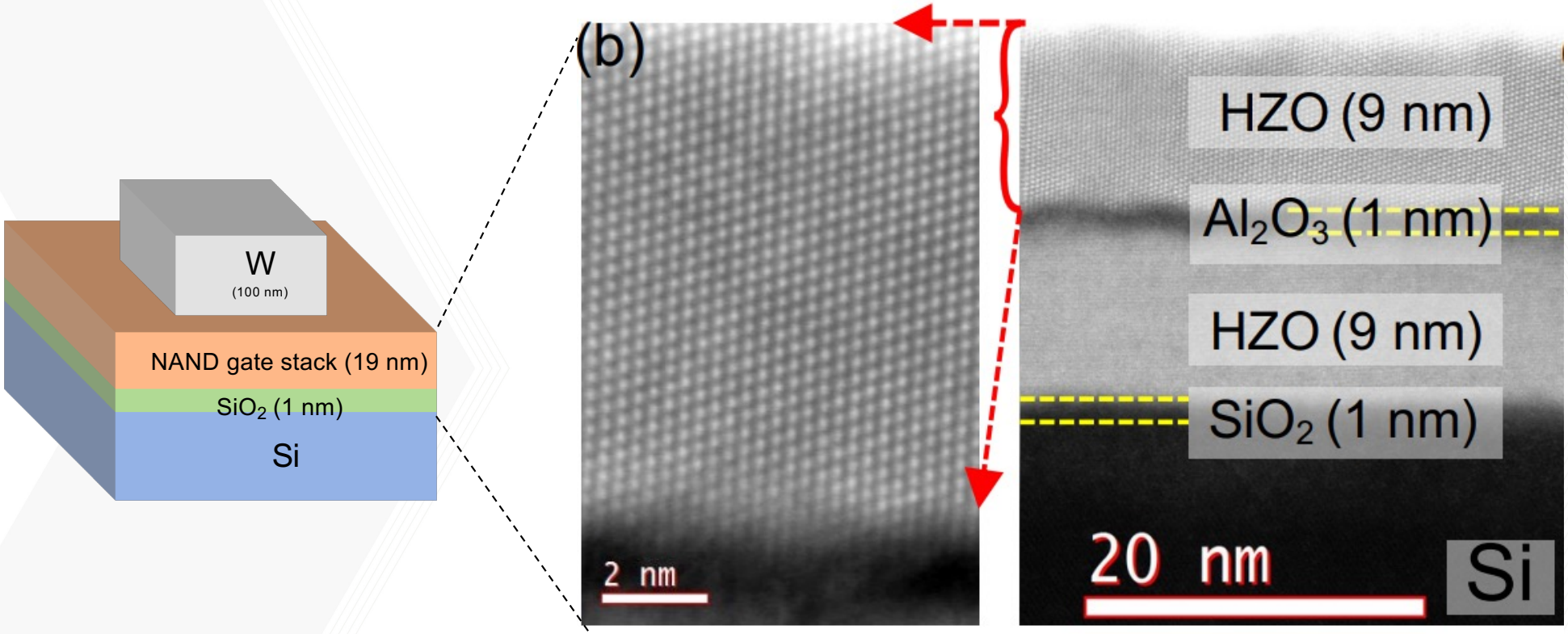
Impact of tunnel dielectric insertion





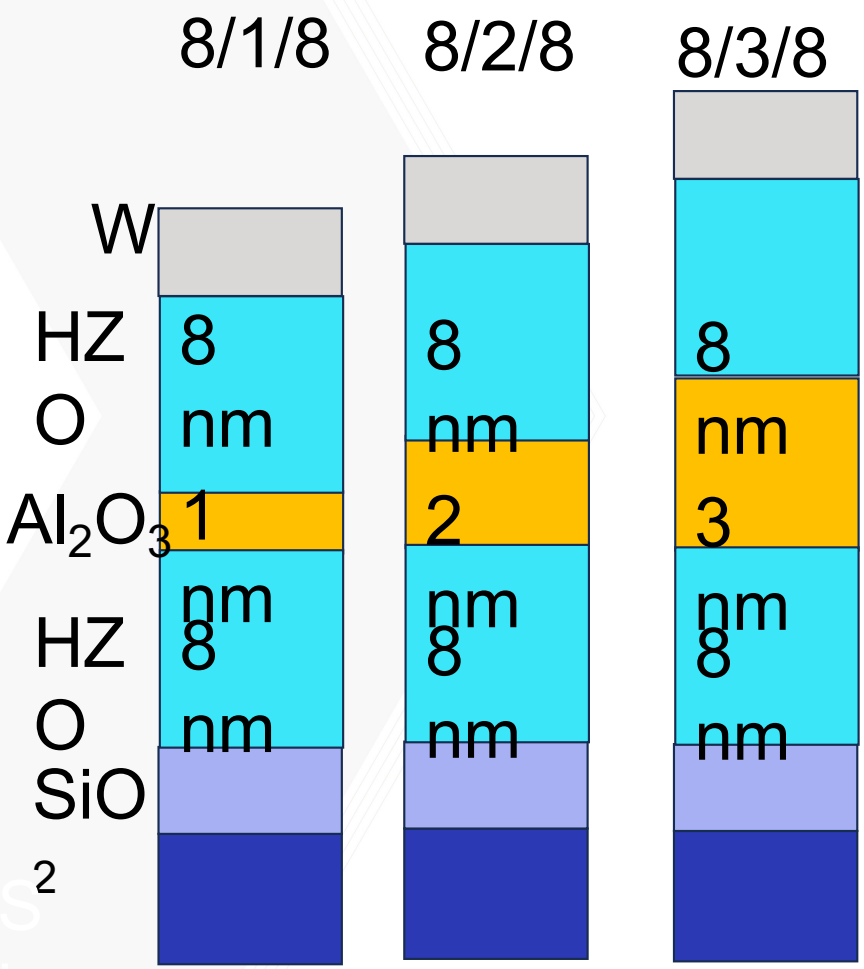
Introducing 1 nm Al_2O_3 intermediate layer dramatically memory window to 5.3 V.

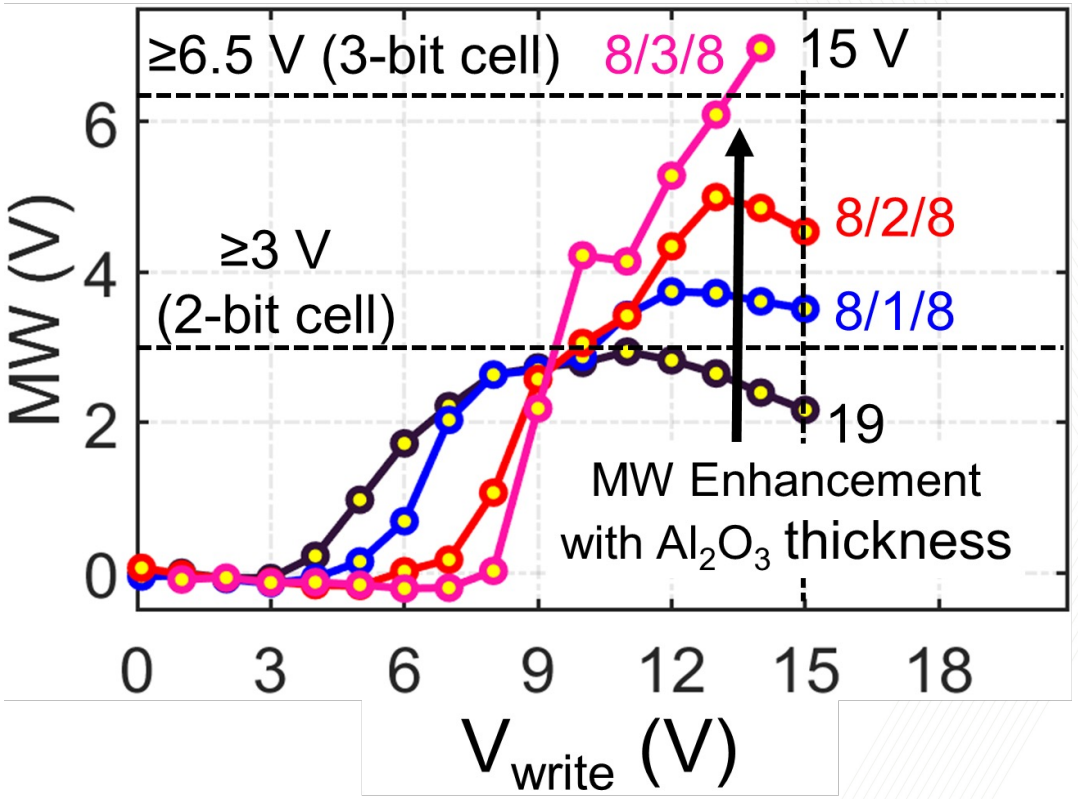
Impact of tunnel dielectric insertion



Full coverage of 1 nm Al_2O_3 is observed.

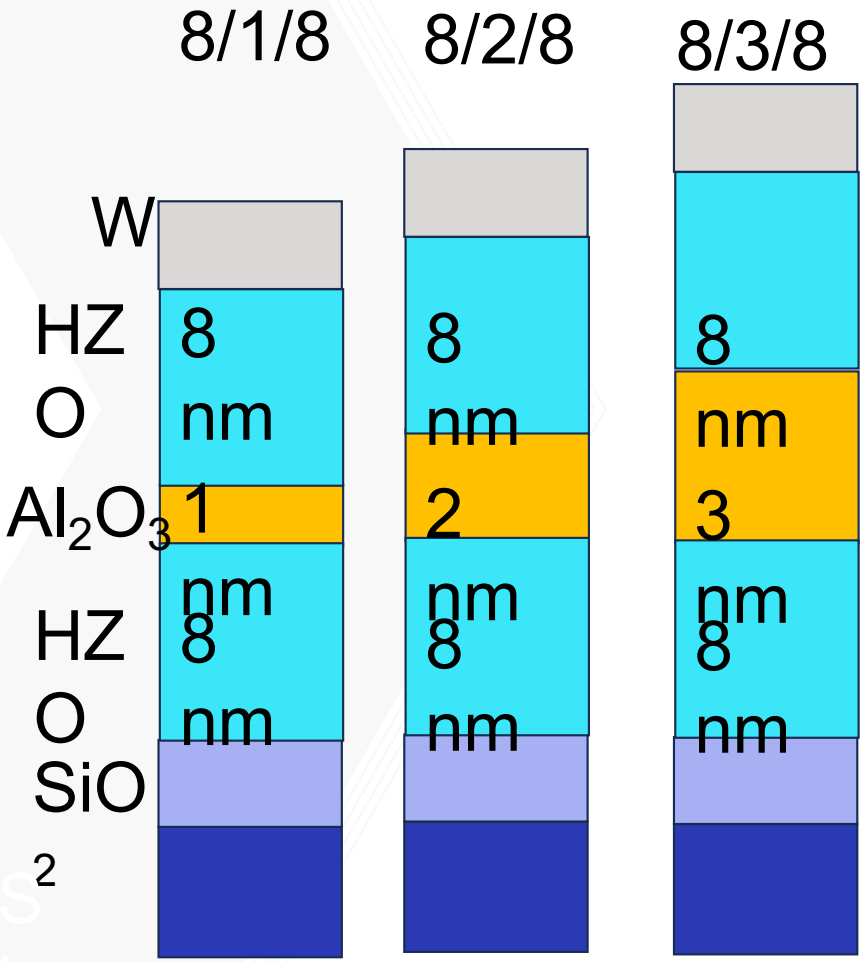
Impact of tunnel dielectric insertion

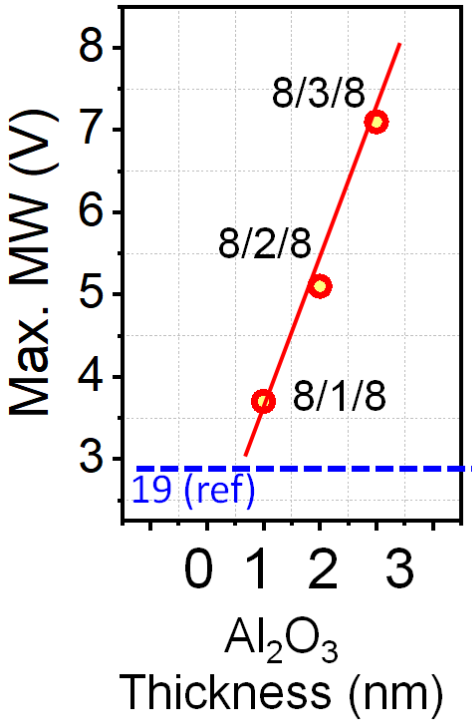


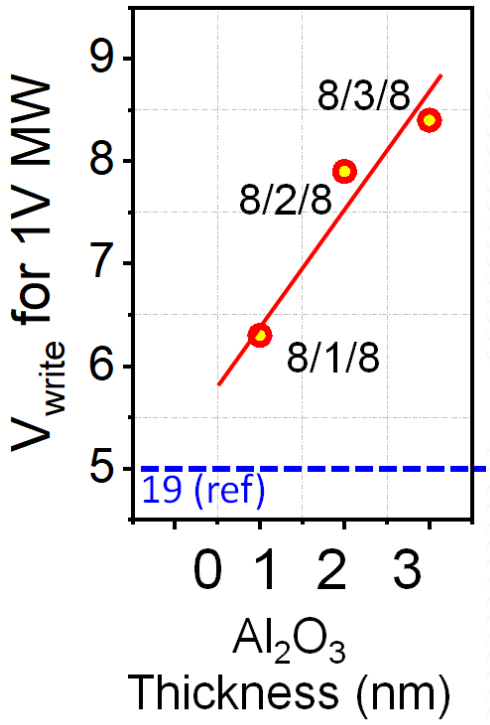


FE 8 nm – AlO 3 nm – FE 8 nm leads to a 7.3 V maximum MW for a 14 V write voltage.

Impact of tunnel dielectric insertion

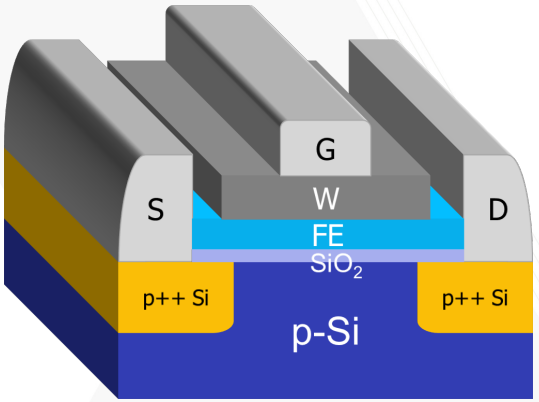




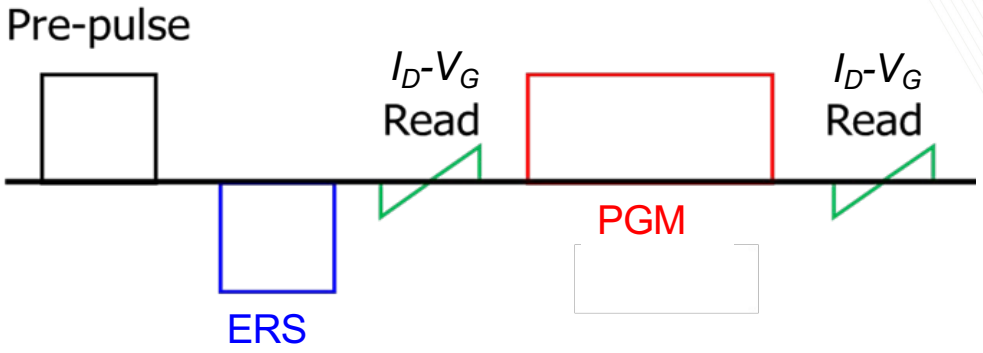


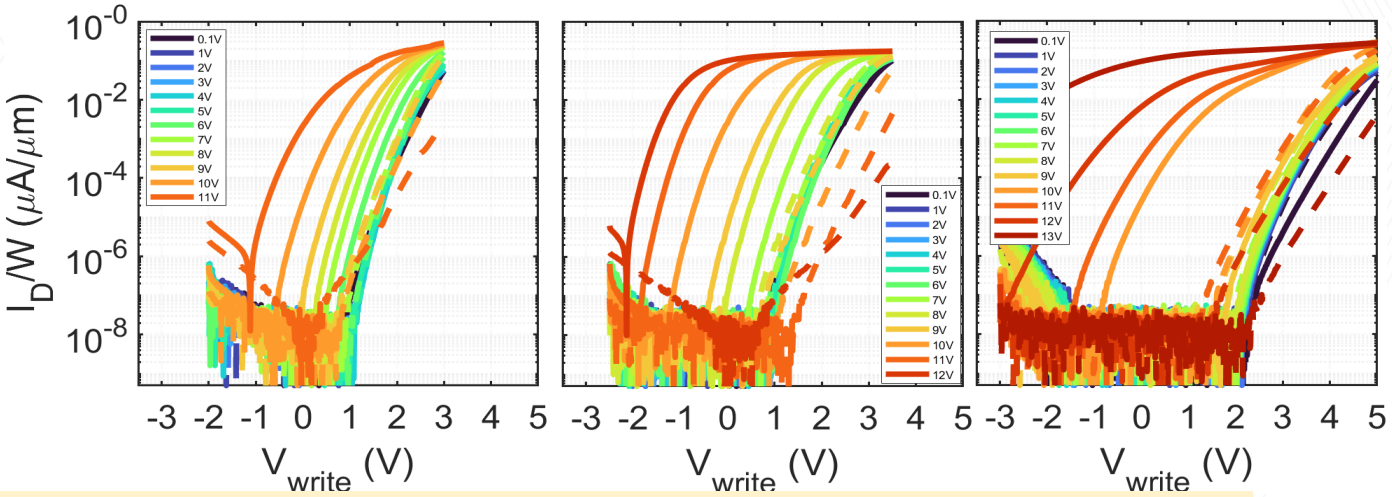
For a fixed FE layer, increase AlO layer increases the MW while increasing the write voltage <15 V

Validation on FEFET structures



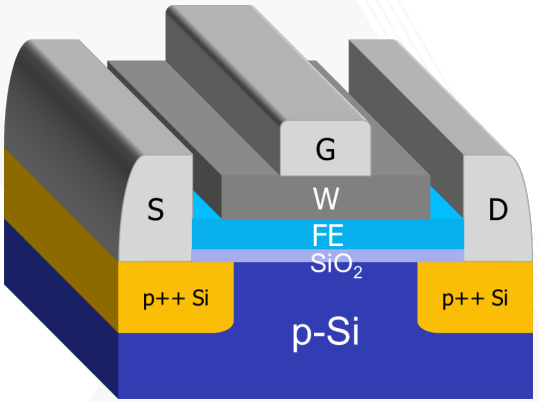
- S/D Implantation
- Screening oxide etch
- ALD of gate stack
- 500 °C, 30 sec anneal
- HZO Dry etch
- Standard ILD
- Al Metallization
- FGA (400 °C, 30 min)





Memory window measured in FEFETs matches quantitatively with those measured on MOS capacitor structures with equivalent gate

Validation on FEFET structures



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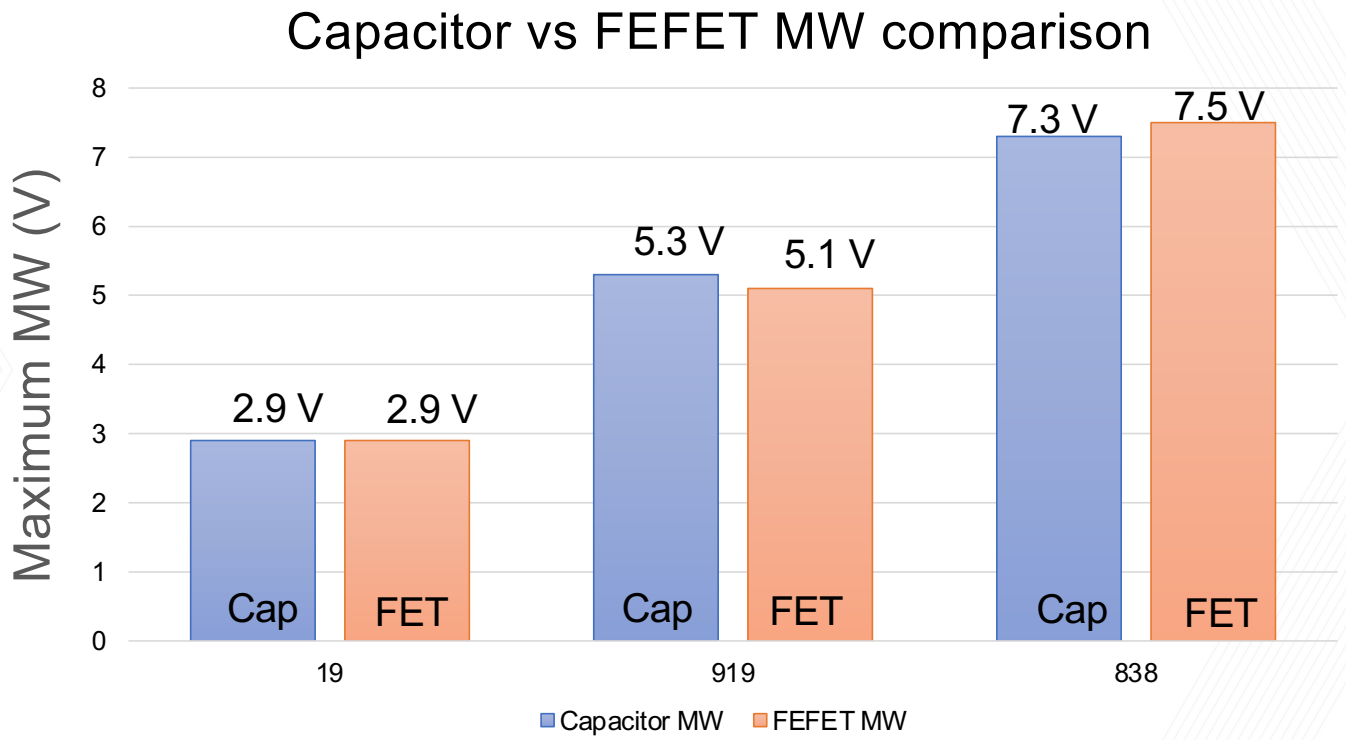
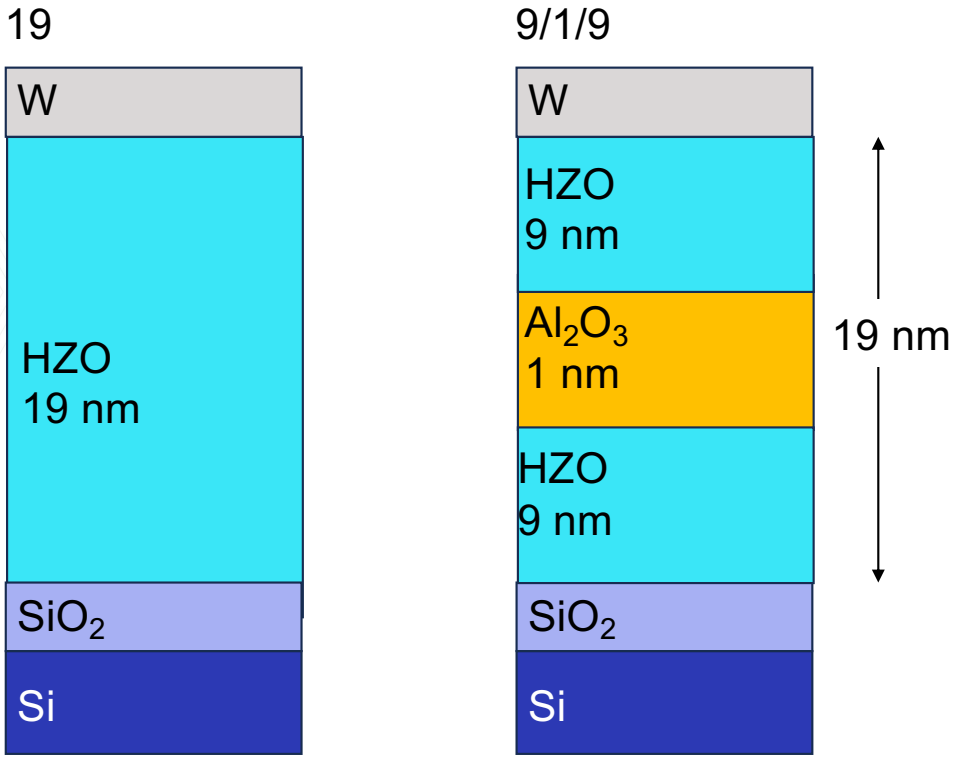


Memory window measured in FEFETs matches quantitatively with those measured on MOS capacitor structures with equivalent gate

Where is the MW enhancement coming from?



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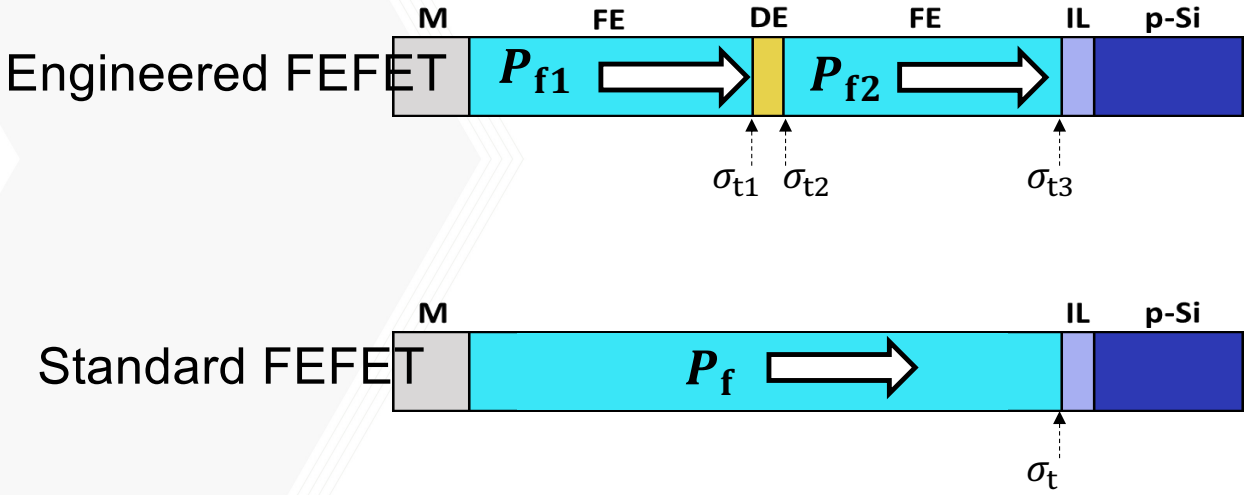
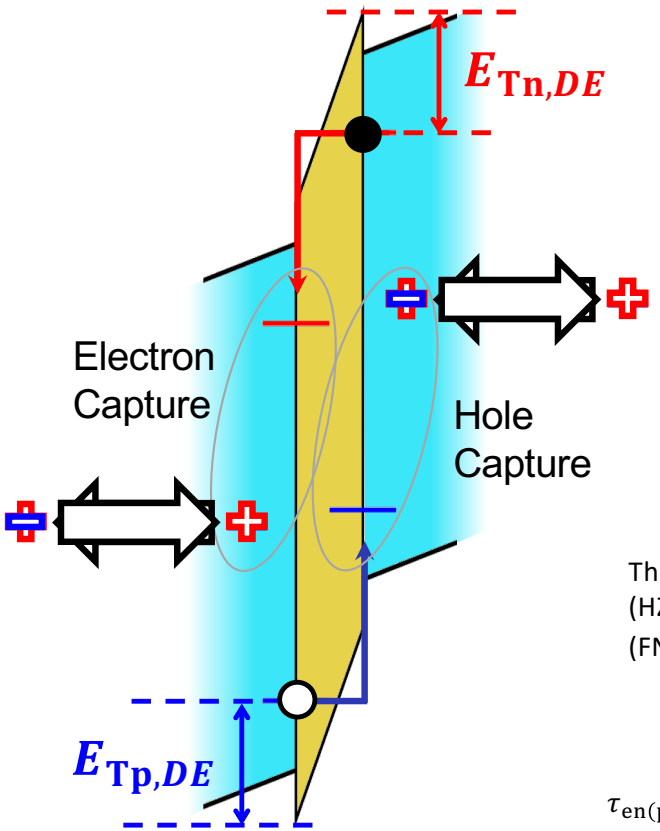


Trapped charges are the key differentiator.

Why do we call it a tunnel dielectric?

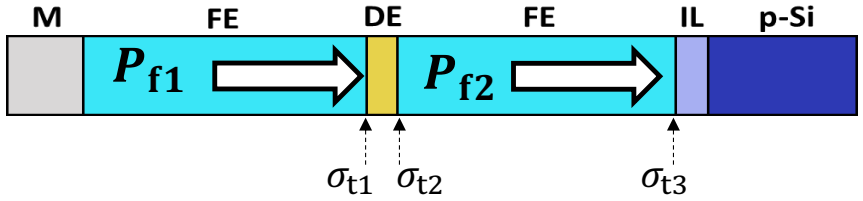


The emission mechanism of the trapped charges at Al_2O_3/HZO (HZO/Al_2O_3) interfaces are assumed to be Fowler-Nordheim (FN) tunneling → **Al_2O_3 as "Tunnel Dielectric Layer"**

$$\tau_{\mathrm{en(p)},i=2(1)} = \tau_{\mathrm{cn(p)},i=1(2)} = \tau_0 \exp\left(-\frac{4\sqrt{2m_{AO}\Phi^3_{\mathrm{Tn(p)},AO}}}{3q\hbar E_{AO}}\right)$$

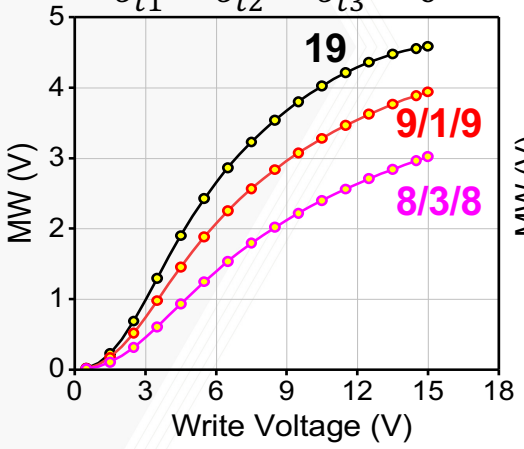
The interface trapped charges is hypothesized to interchange position via tunneling!

Decoupling the impacts of different trapping mechanisms



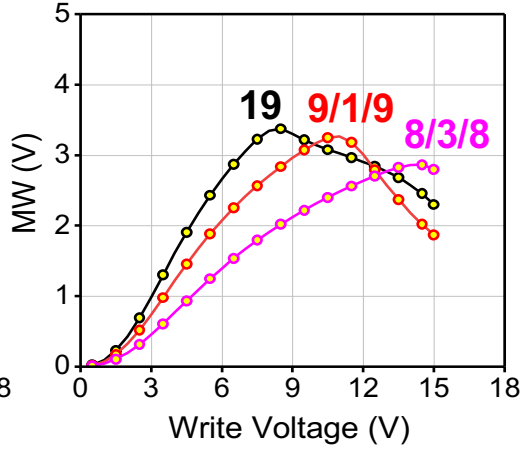
Absence of screening trap charges

$\sigma_{t1} = \sigma_{t2} = \sigma_{t3} = 0$



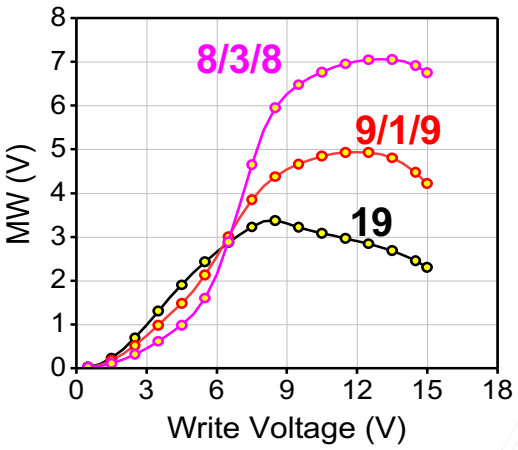
HZO/SiO_2 Traps only

$\sigma_{t1} = \sigma_{t2} = 0;\ \sigma_{t3} \neq 0$



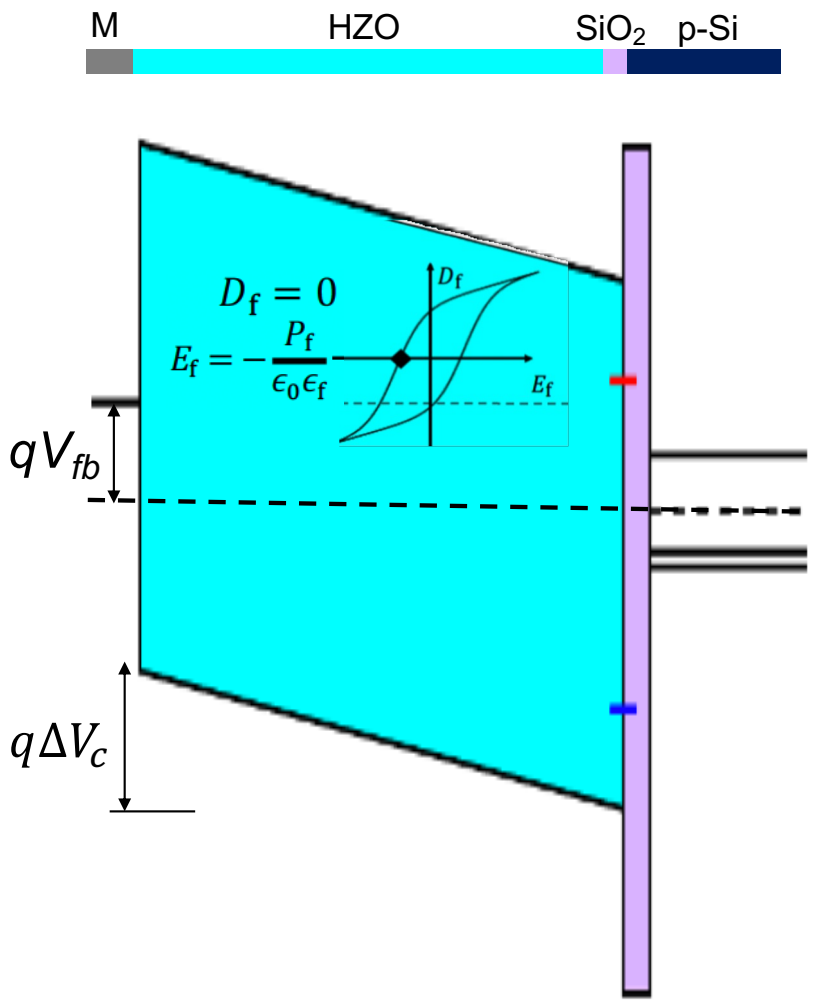
Al_2O_3/HZO + HZO/SiO_2 Traps

$\sigma_{t1} \neq 0;\ \sigma_{t2} \neq 0;\ \sigma_{t3} \neq 0$

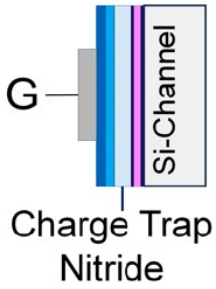
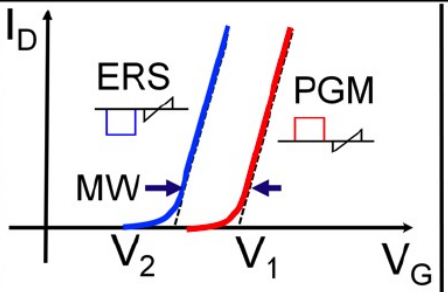
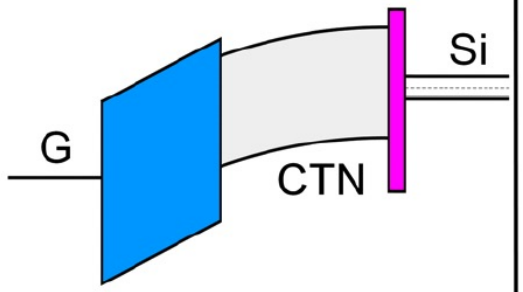
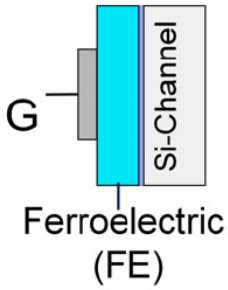
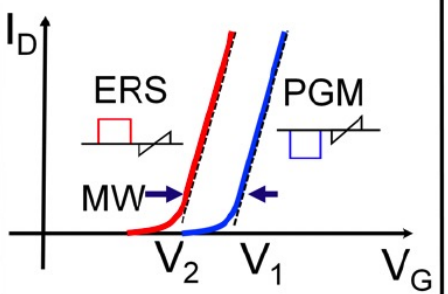
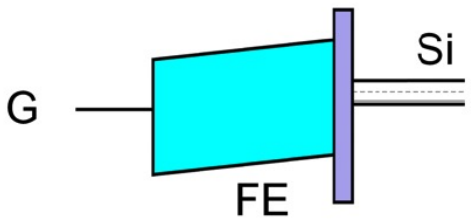
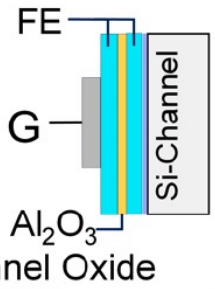
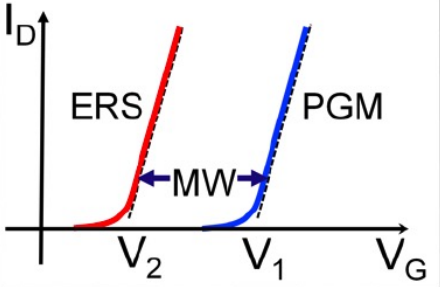
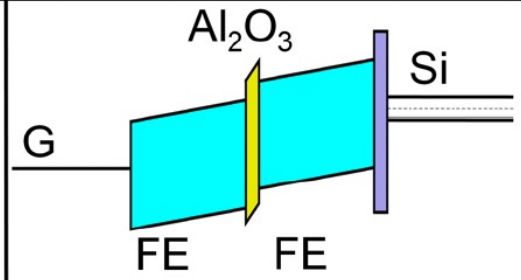


Trap effects are responsible for the observed MW trend (MW: 8/3/8 >9/1/9>19)

MW enhancement mechanism with band diagrams

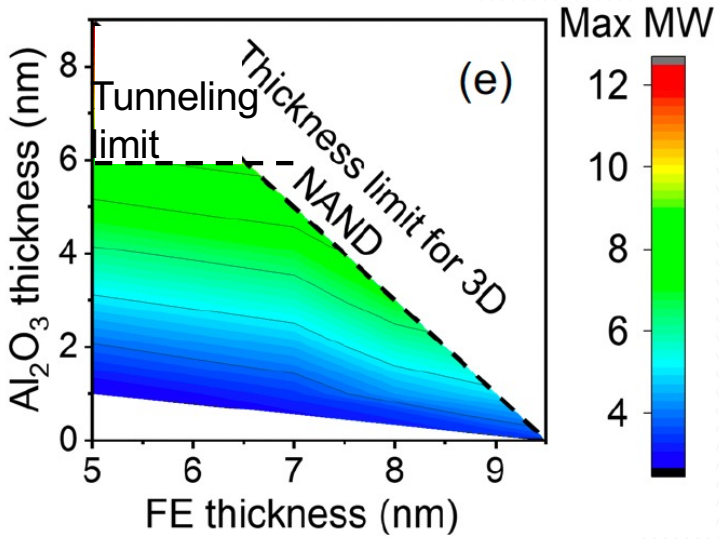


Ferroelectric NAND

	Structure	Characteristics	Band diagram at FB condition	Attributes
Charge Trap Flash				✓ Large MW × Large Write Voltage Mechanism: Trapping
Conventional FEFET				× Low MW ✓ Low Write Voltage Mechanism: Polarization Switching
Proposed FEFET				✓ Large MW ✓ Moderate Write Voltage Mechanism: Polarization Switching + Trapping + Tunneling

Ferroelectric NAND

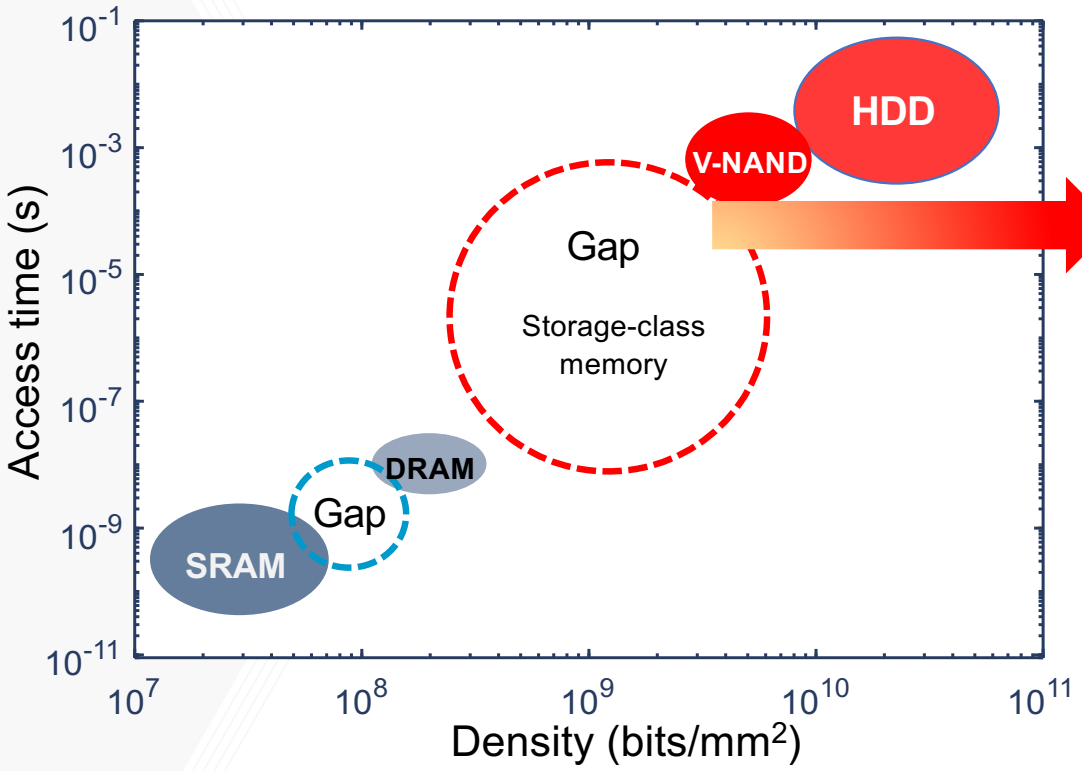
- Ferroelectricity presents opportunities for NAND storage technologies.
  - Write voltage reduction and memory window enhancement.
  - Potential for QLC by stack engineering.
  - Vertical scaling towards 1000 layers.



- Further exploration and engineering required for
  - Tunneling mechanism
  - Disturb characteristics and mitigation.

- Alternative structures can also lead to MW enhancement via gate side injection through blocking layer.
  - See: Lim et al. Comprehensive Design Guidelines of Gate Stack for QLC and Highly Reliable Ferroelectric VNAND. IEDM 2023 paper 35.4.

Opportunity for V-FeNAND



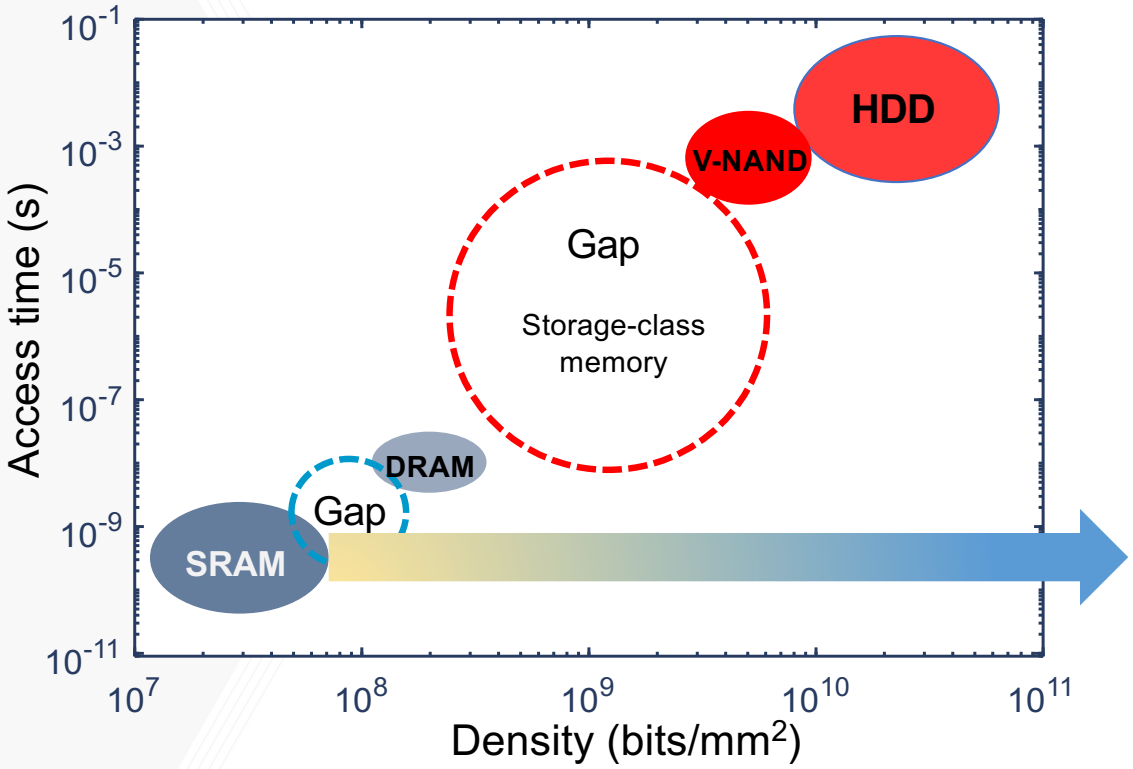
NAND FLASH

- Limited scaling (oxide>20 nm)
- High write voltage (~20 V)
- Slow write (1-10 ms)
- Limited endurance (10^3 for MLC)

V-FeNAND

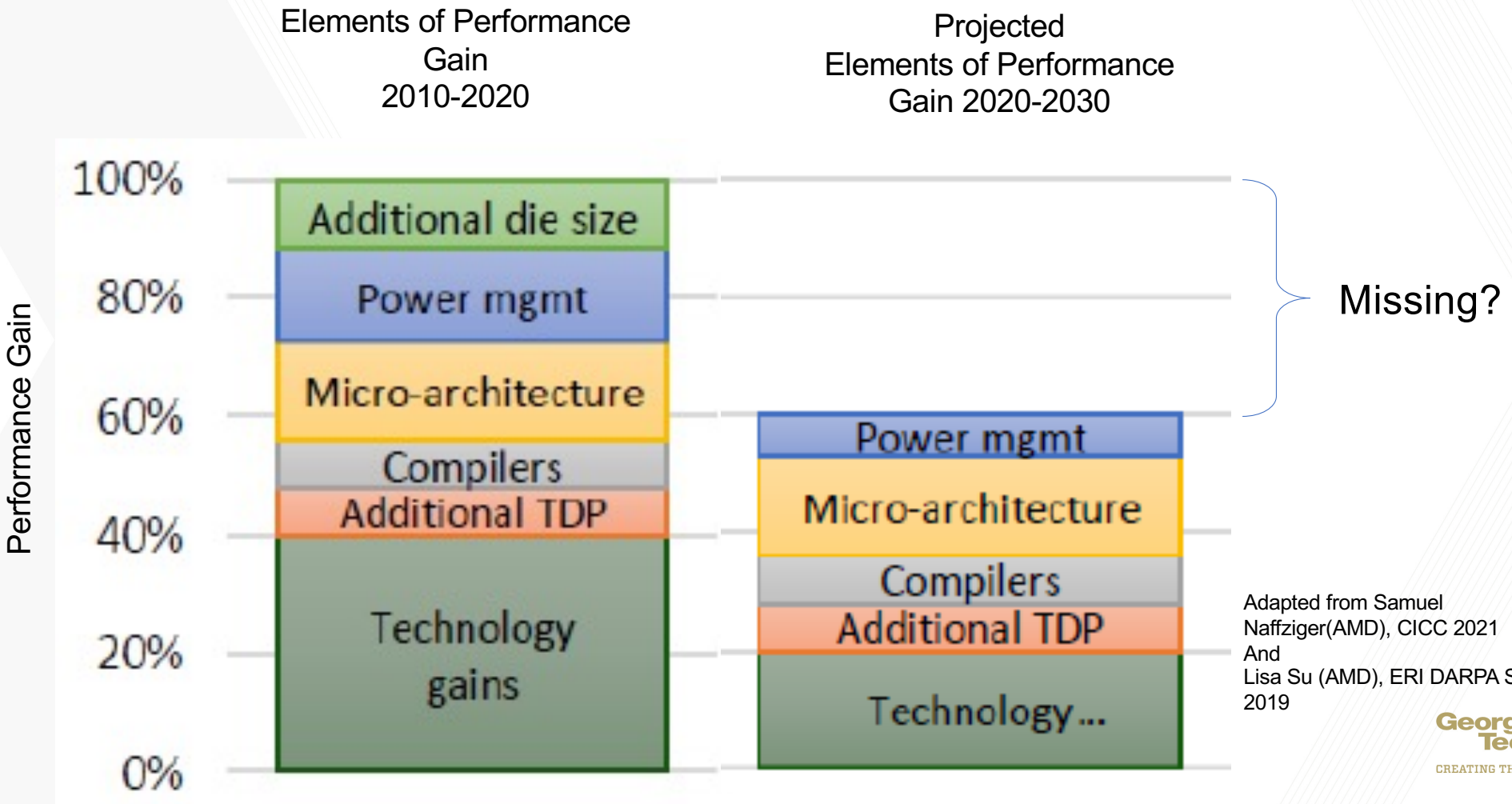
- Scalable oxide (<5 nm)
- Smaller write voltage (~10 V)
- Fast write (<1 μs)

Opportunity for Cache



	Cell area | Speed
DRAM:	6-30F^2 | <10 ns
SRAM:	140-280F^2 | <1 ns

Materials are central to *Future* Electronics



Adapted from Samuel Naffziger(AMD), CICC 2021
And
Lisa Su (AMD), ERI DARPA Summit, 2019

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FEFET as an embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM[70]	eFlash (FG)	eFlash (SG MONOS)[42]	eFlash (SONOS)[41]	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based)[67]
Cell size	120–150F^2	40F^2	40–60F^2	40–50F^2	50–60F^2	10–30F^2	10–30F^2	30–40F^2	50–60F^2
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 µs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	>10^{16}	>10^{16}	~10^4	~10^5	~10^6	10^5–10^9	>10^{10}	>10^{12}	>10^{14}

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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Progress in FEFET technology

1 Write voltage and Memory Window	2 Read/Write Speed	3 Device-to-device variation	4 Reliability and endurance
Specs			
<1.5 V write voltage >0.5 V memory window	<10 ns write speed <10 ns read-after-write delay	$\Delta V_{t,3\sigma} =$ 20-50 mV (7 nm node)	>10^{12} cycles

Progress in FEFET technology

1	2	3	4
Write voltage and Memory Window	Read/Write Speed	Device-to-device variation	Reliability and endurance

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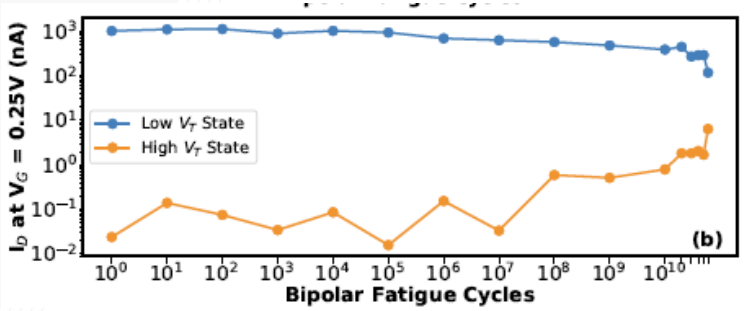
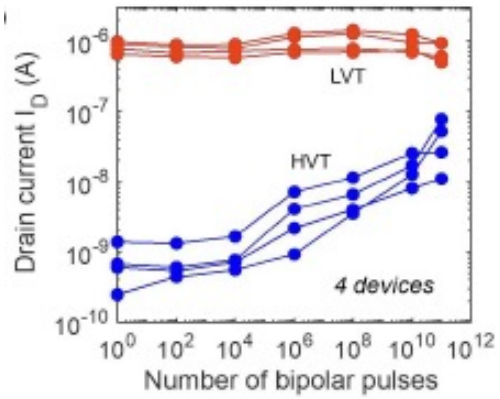


Tan et al. IEEE EDL 42, 994 (2021).



Dutta et al. IEEE EDL 43, 383 (2022).

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Write voltage and Memory Window	Read/Write Speed	Device-to-device variation	Reliability and endurance

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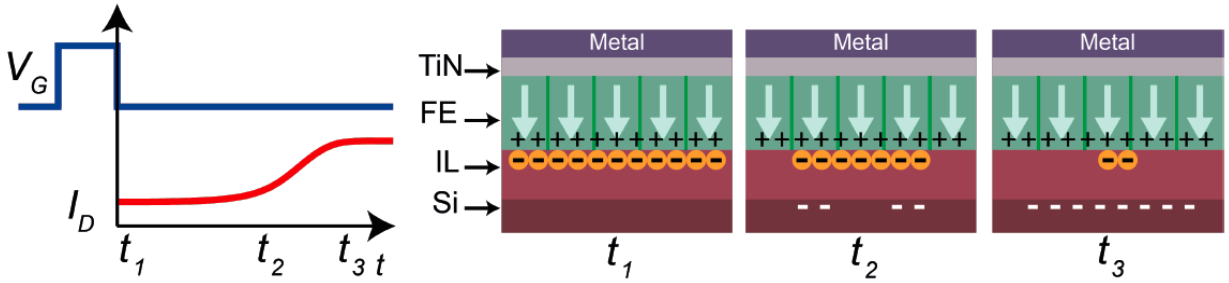

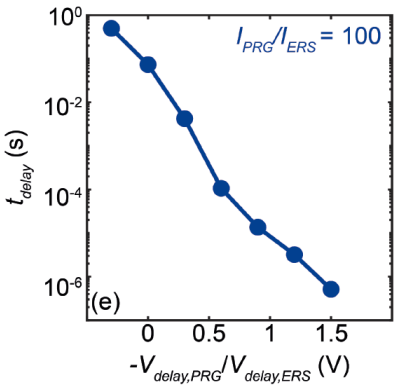

Wang, Z., Tasneem, N., Hur, J., Chen, H., Yu, S., Chern, W., & Khan, A. (2021, December). Standby bias improvement of read after write delay in ferroelectric field effect transistors. In *2021 IEEE International Electron Devices Meeting (IEDM)* (pp. 19-3). IEEE.

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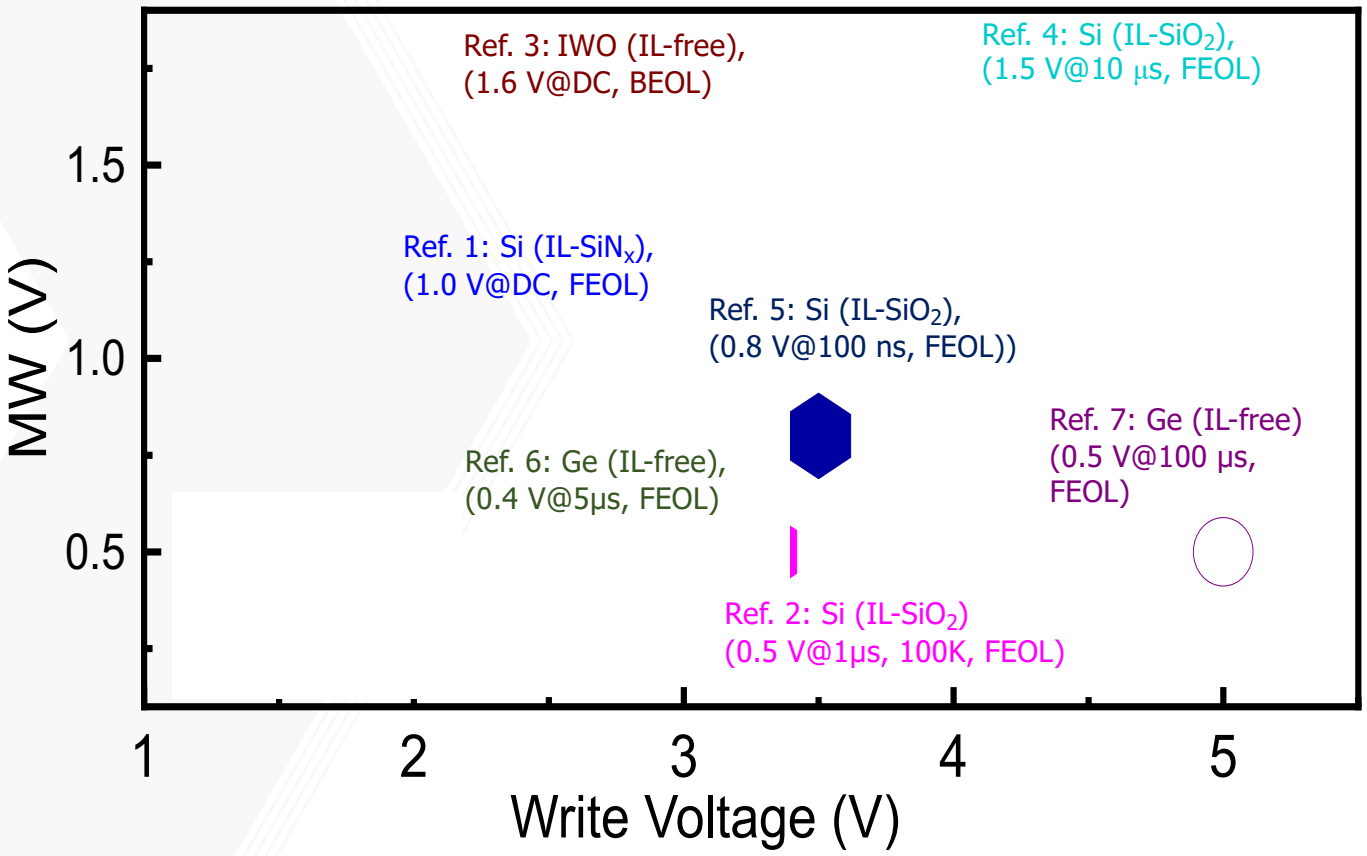
Benchmarking Memory Window v. Write Voltage Tradeoff



[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

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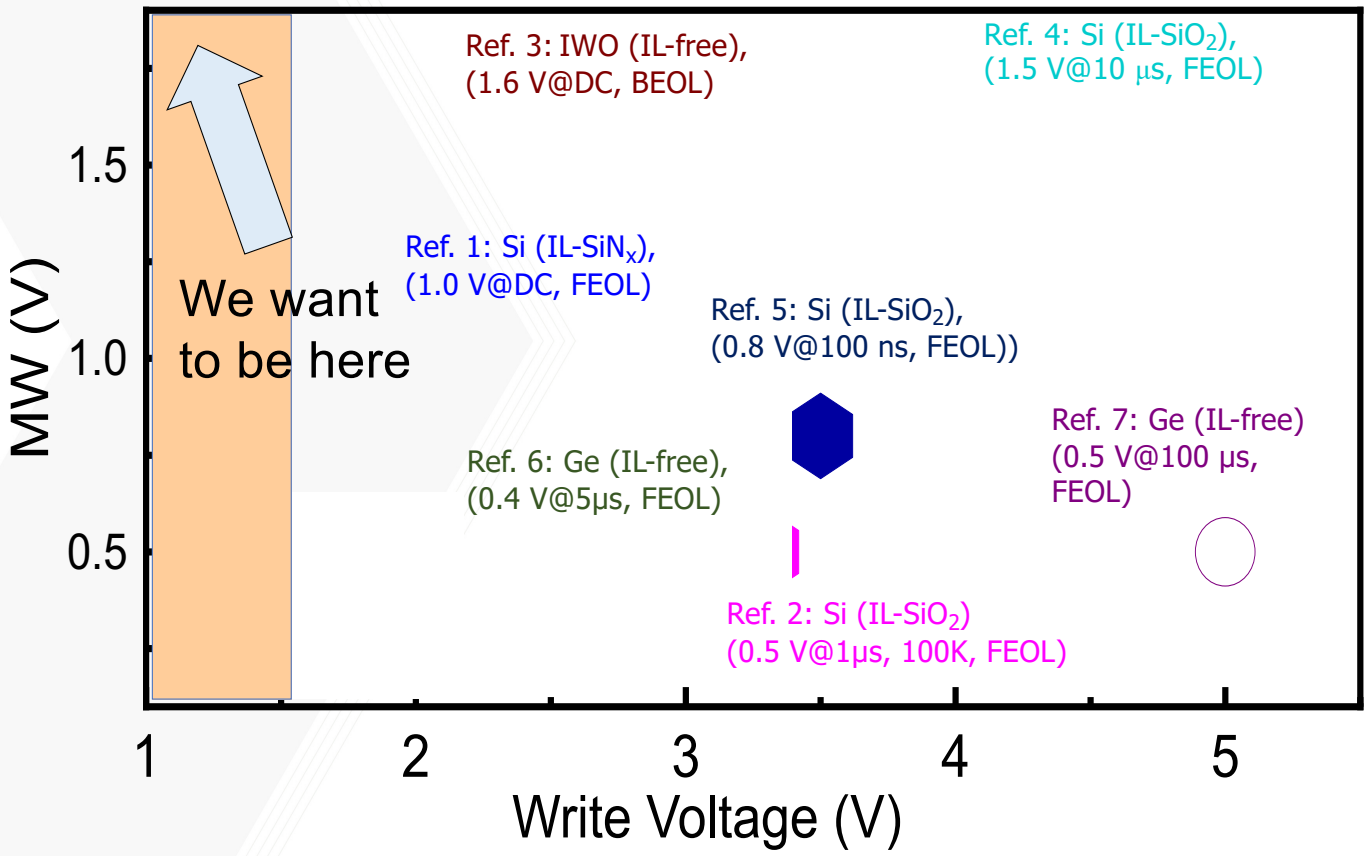
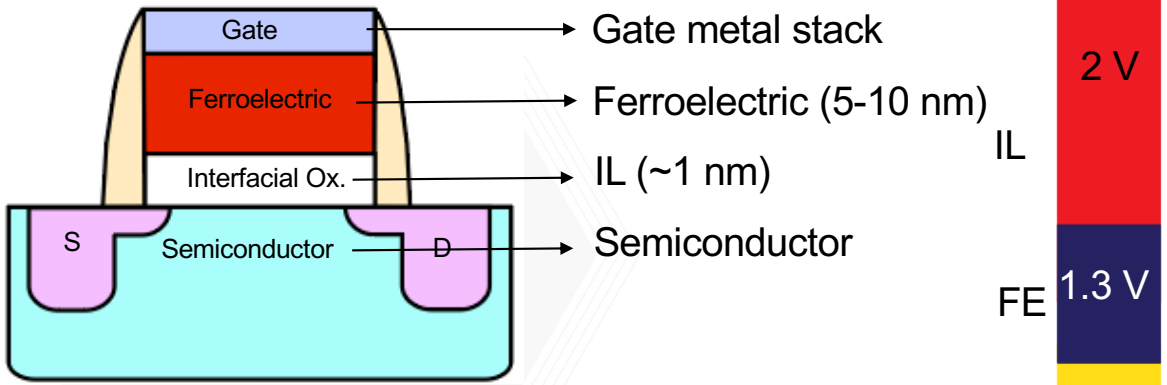
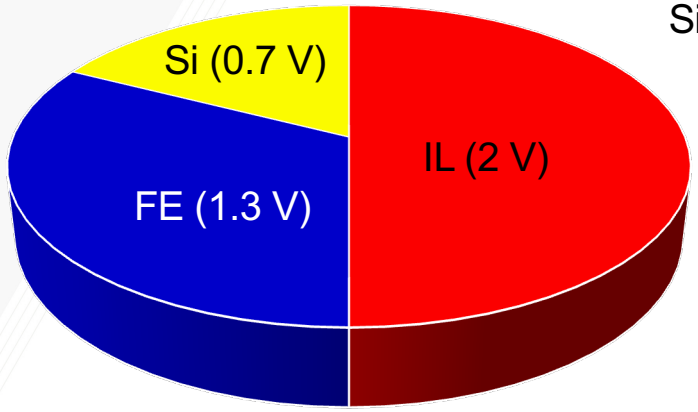


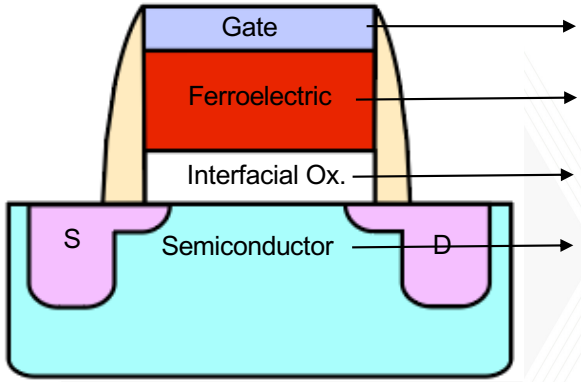
[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

Write voltage vs. memory window trade-off





Write voltage vs. memory window trade-off

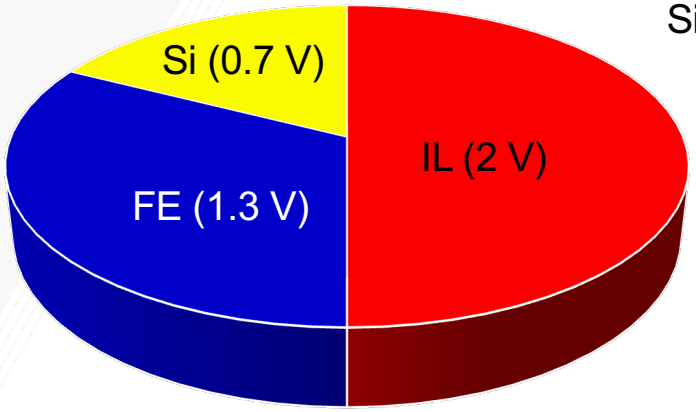


Gate metal stack

Ferroelectric (5-10 nm)

IL (~1 nm)

Semiconductor

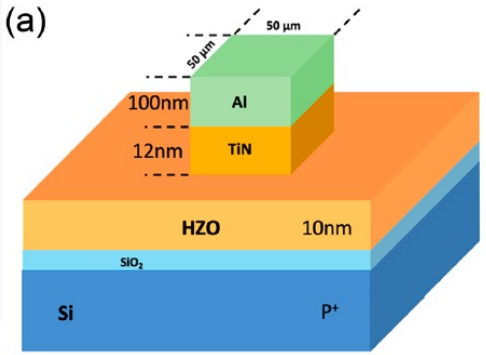


Reducing the thickness of the IL or increasing the K of the IL.

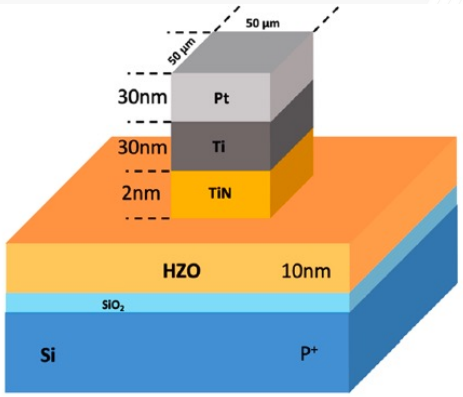
Reducing FE thickness reduces MW. $MW_{max}=2V_C$

Changing the band-gap of the semiconductor By changing the channel material from Si to SiGe or Ge.

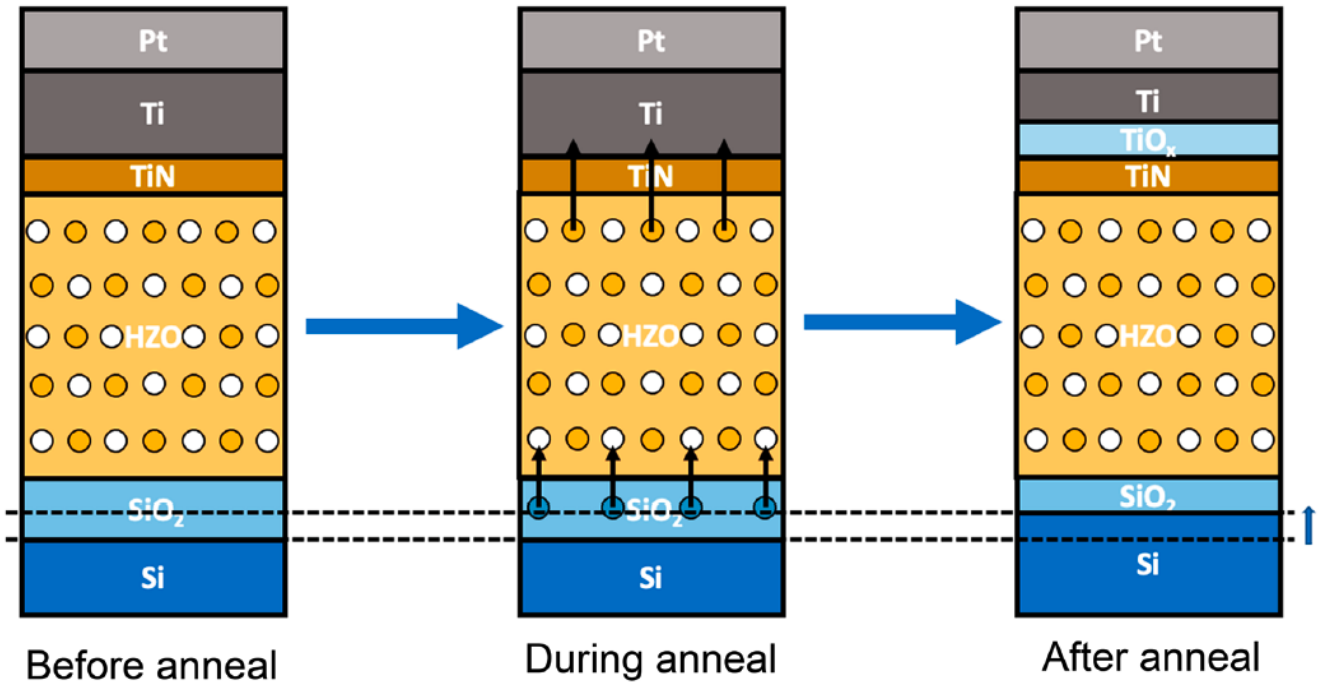
Remote oxygen scavenging to reduce IL thickness



Non-Scavenging



Remote-Scavenging



Tasneem et al. “Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium–Zirconium Oxide-Based Metal–Oxide–Semiconductor Structures”, ACS Appl. Mater. Interfaces 2022, 14, 43897–43906

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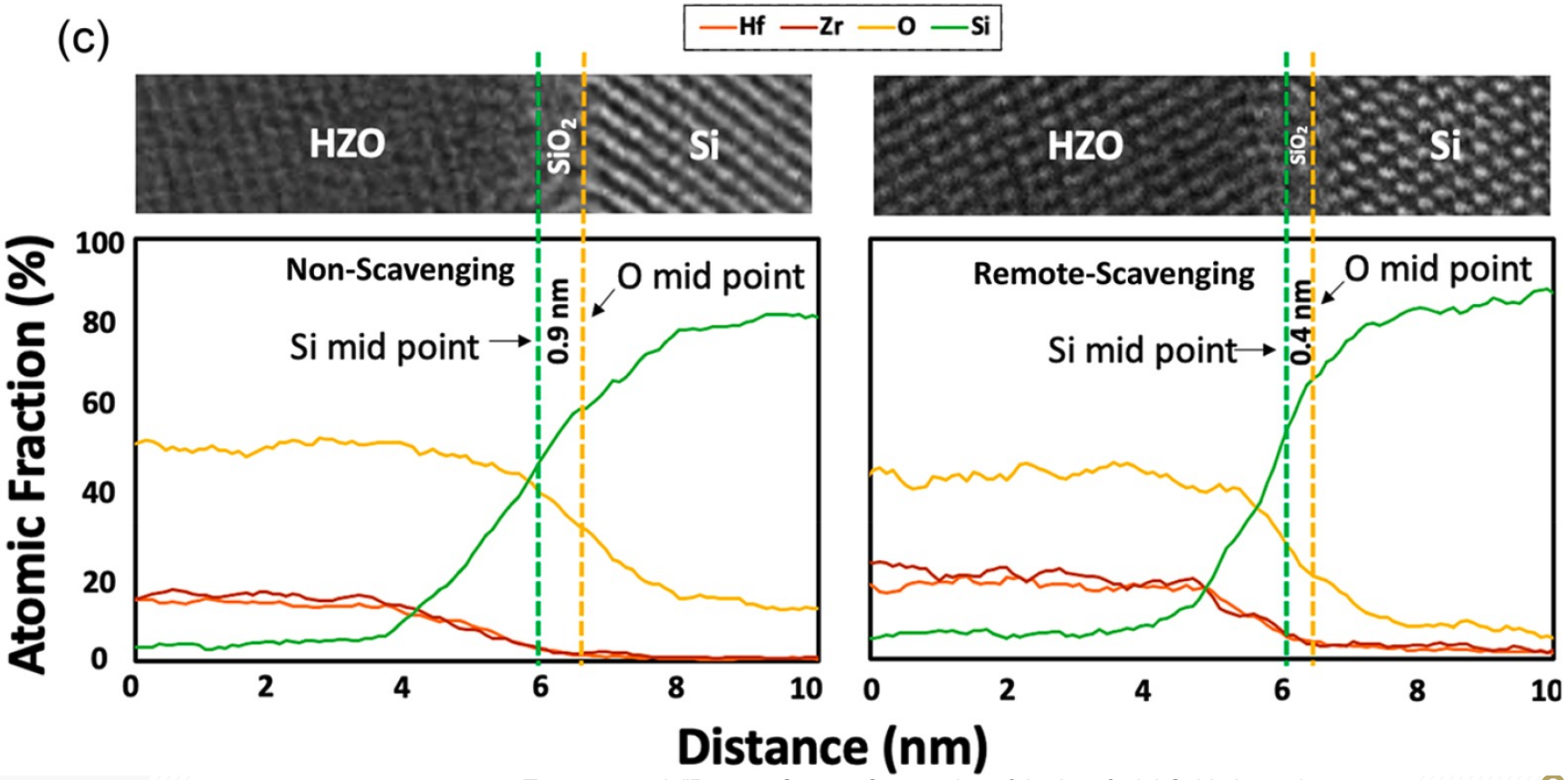
Remote oxygen scavenging to reduce IL thickness



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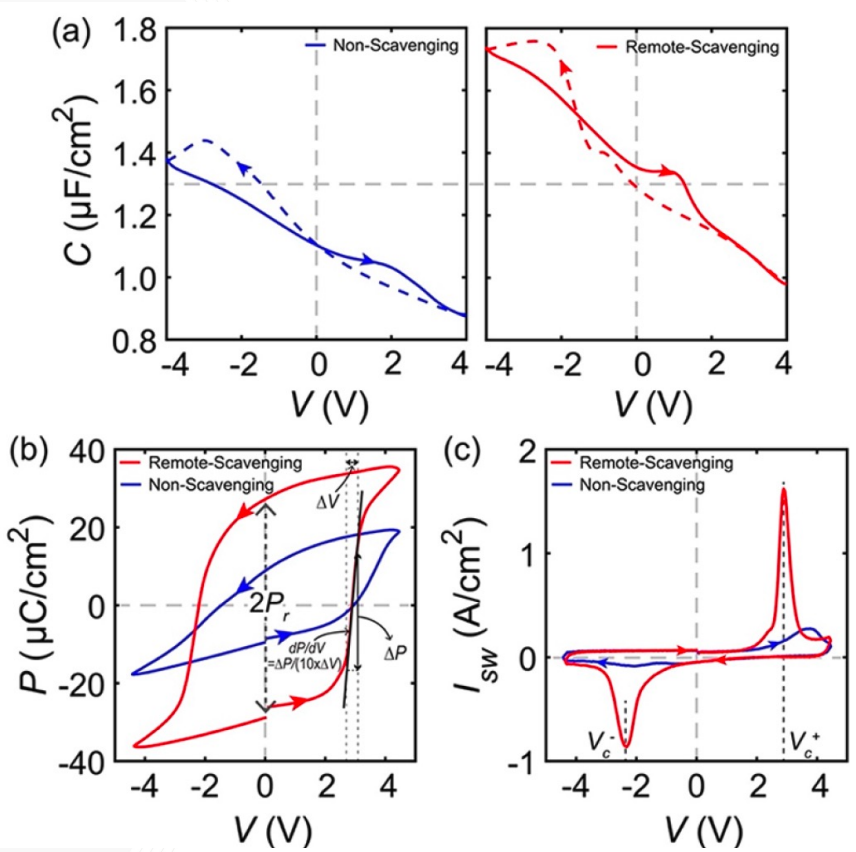
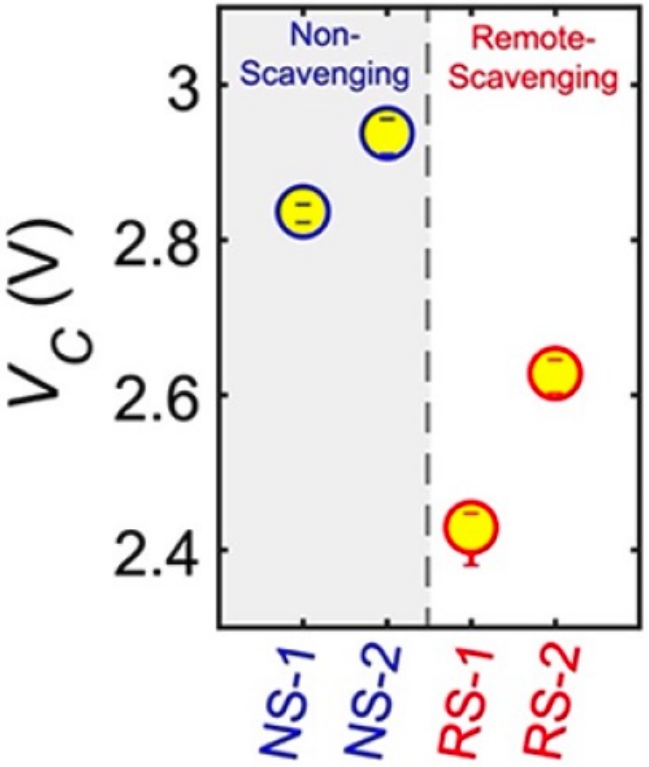
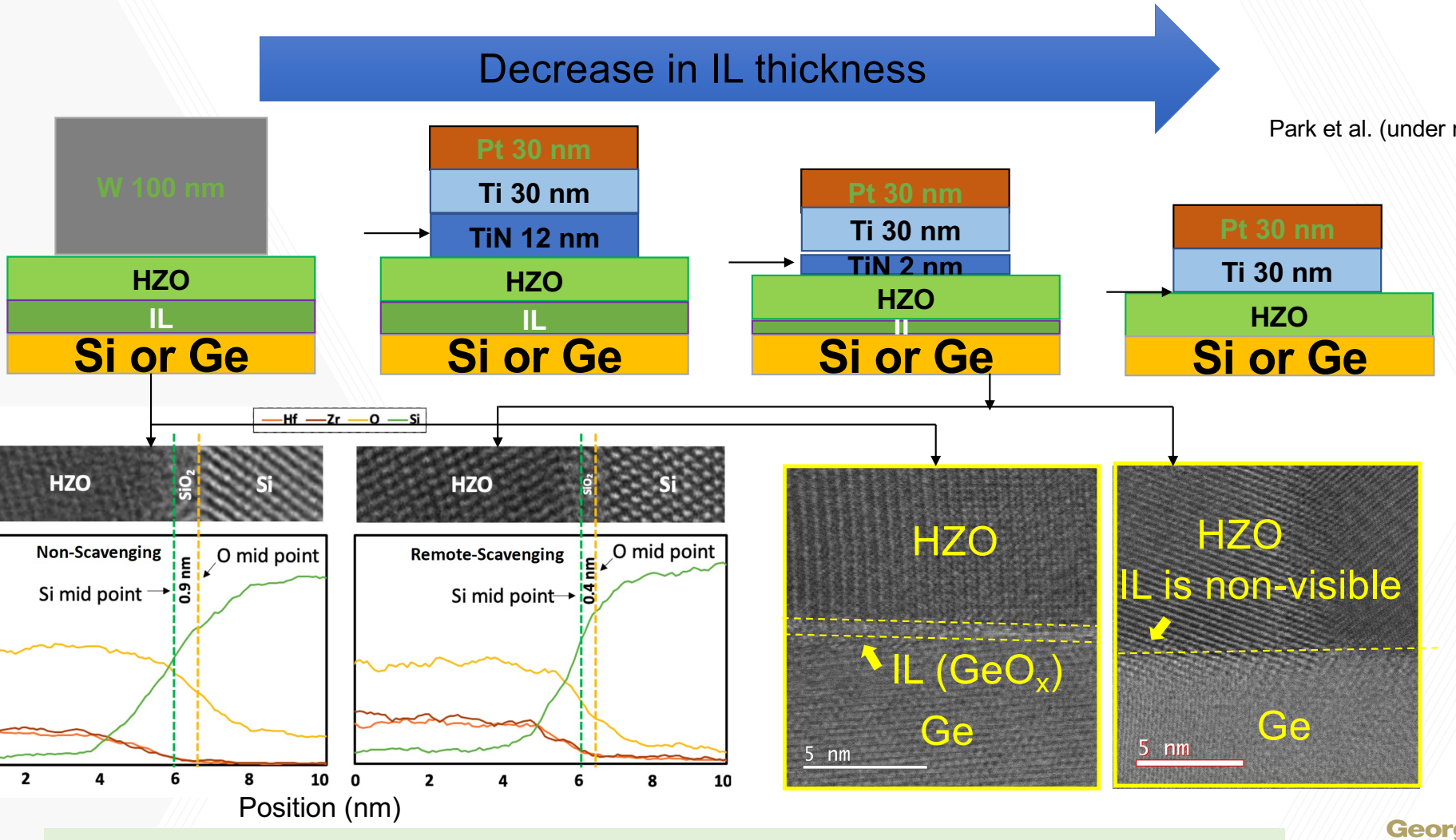
Remote oxygen scavenging to reduce IL thickness





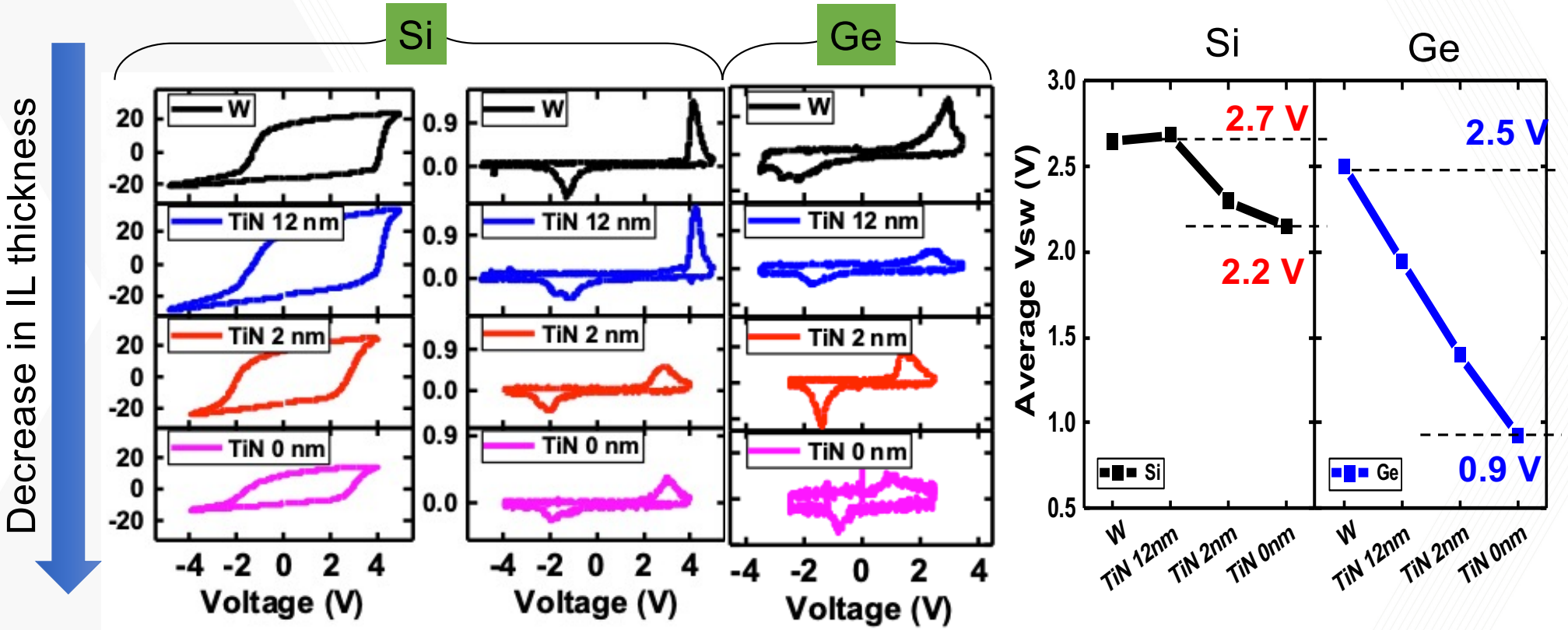
Tasneem et al. "Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium−Zirconium Oxide-Based Metal−Oxide−Semiconductor Structures", ACS Appl. Mater. Interfaces 2022, 14, 43897–43906



Park et al. (under review)

Remote oxygen scavenging can result in controllable IL thickness.

The effect of the IL thickness on Vc



Dramatic reduction in coercive voltage is observed in Ge platform with the change of the gate metal stack.

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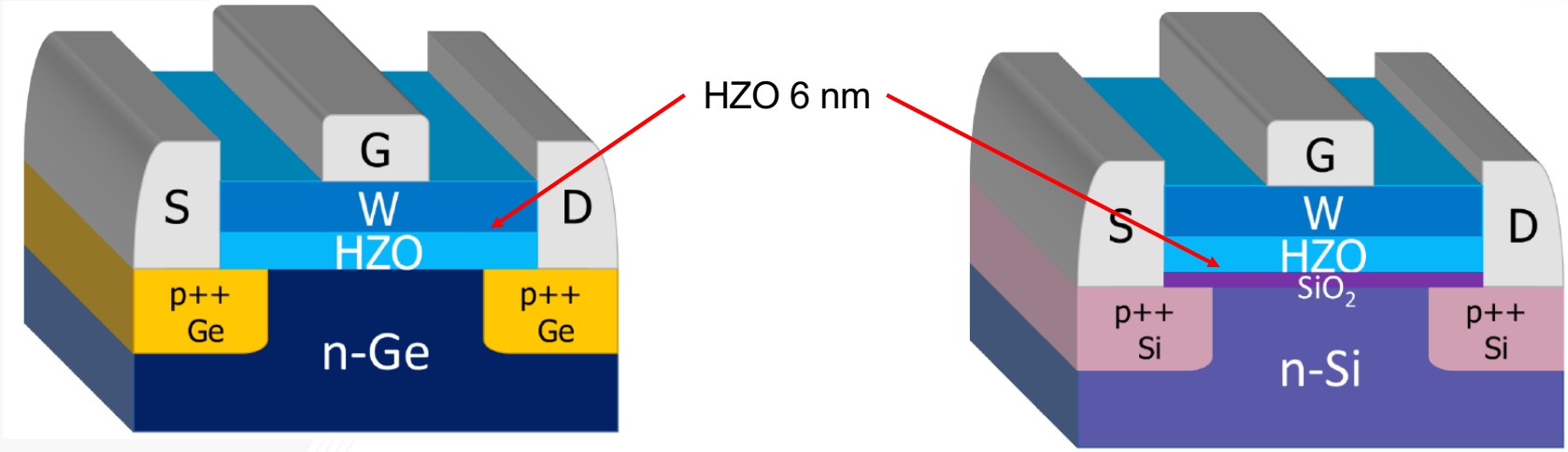
Ge-channel FEFETs with record-low write voltages



Si and Ge-channel FEFETs fabricated with the same 6 nm HZO layers, under similar process and fabrication conditions.

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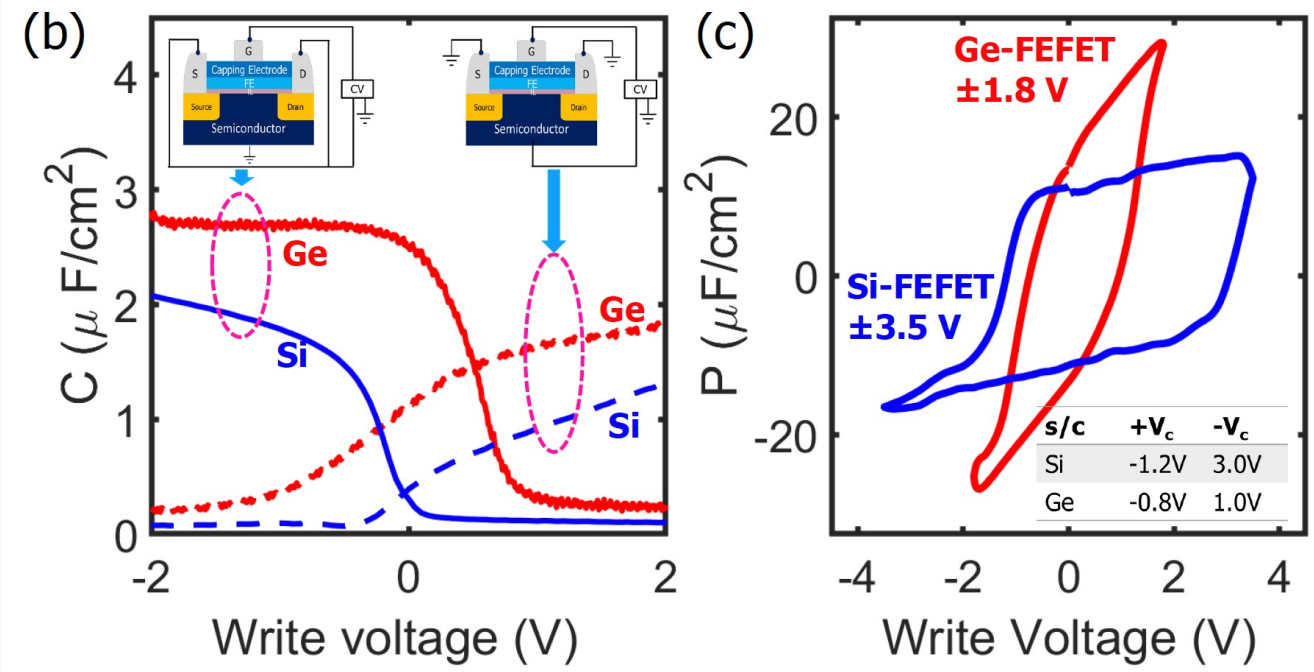
Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

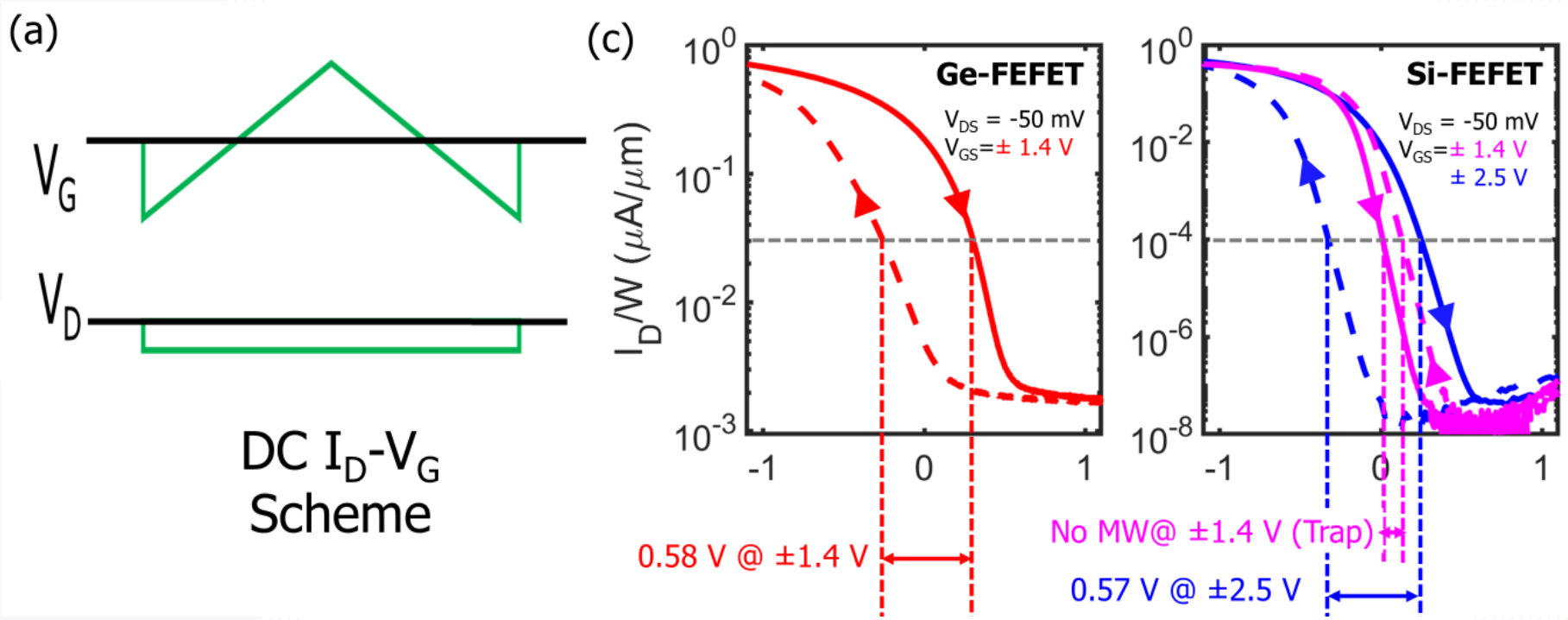
Ge-channel FEFETs with record-low write voltages



Significant increase on the on-capacitance and reduction in coercive voltage in Ge-channel FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

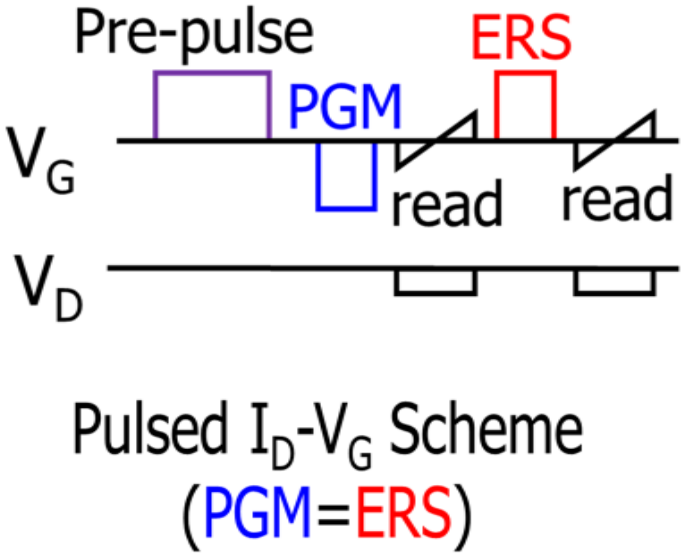
DC I_D-V_G characteristics

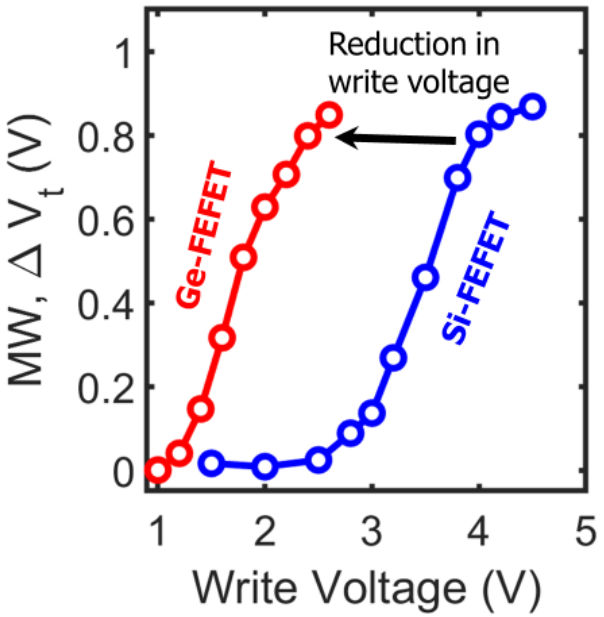


Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Pulsed I_D-V_G characteristics



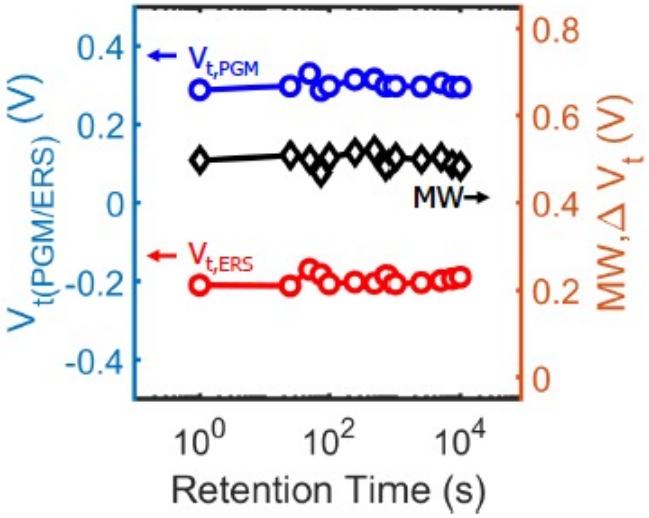


Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

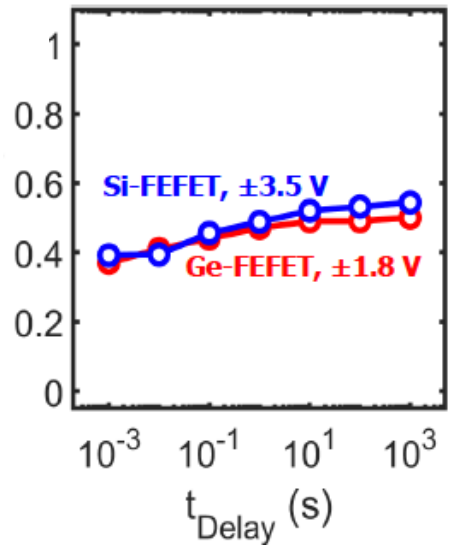
Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Retention, endurance and read-after-write delay

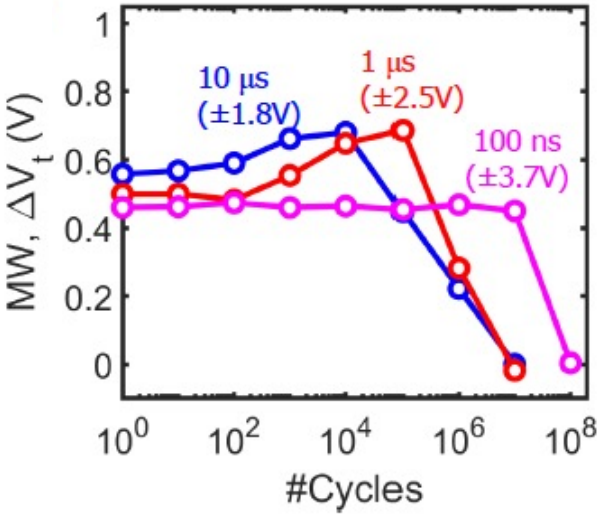
Retention



Read-after-write delay



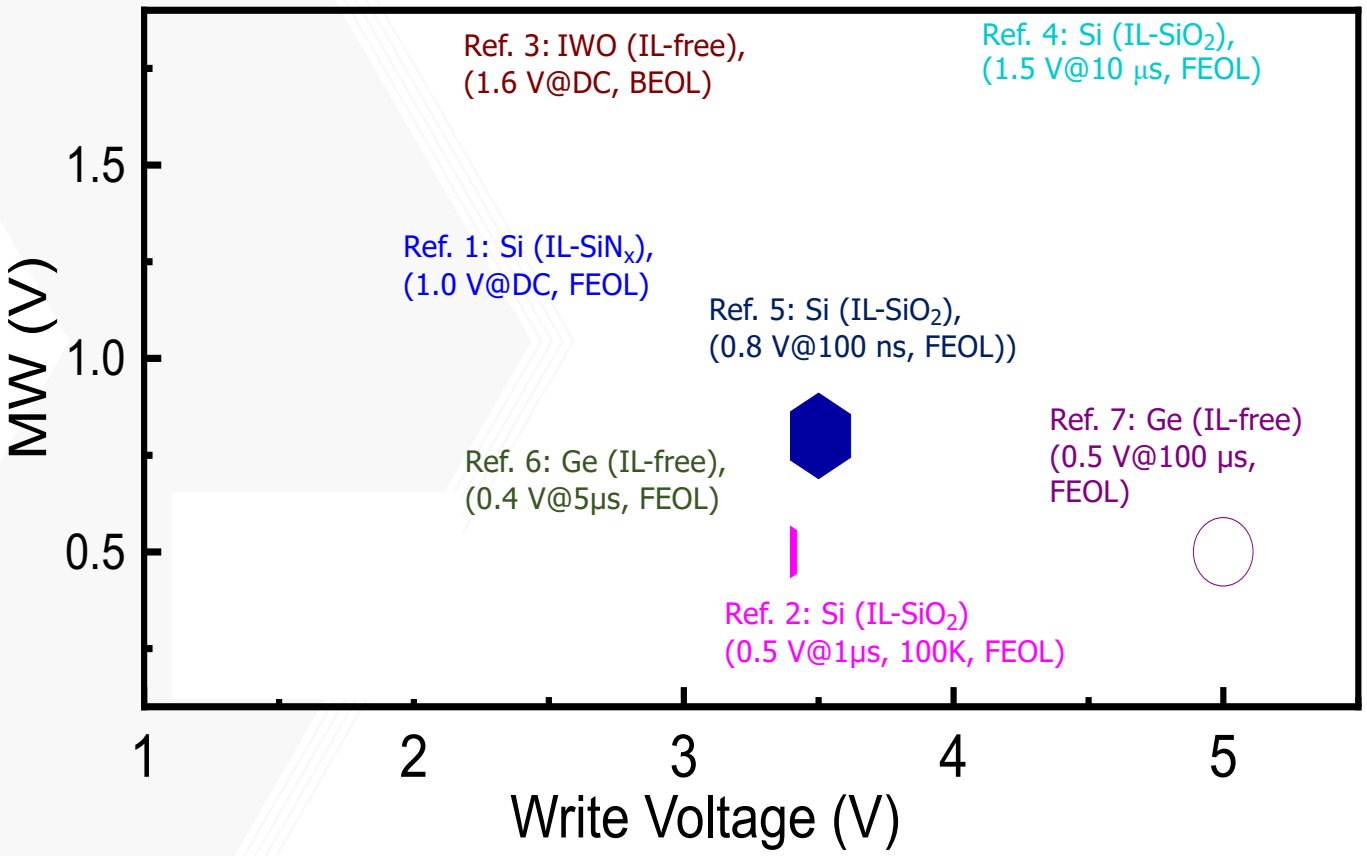
Endurance



The Ge-FEFET show write endurance of 107 cycles, excellent data retention and immediate read-after-write capability.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Benchmarking Memory Window v. Write Voltage Tradeoff



[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
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[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
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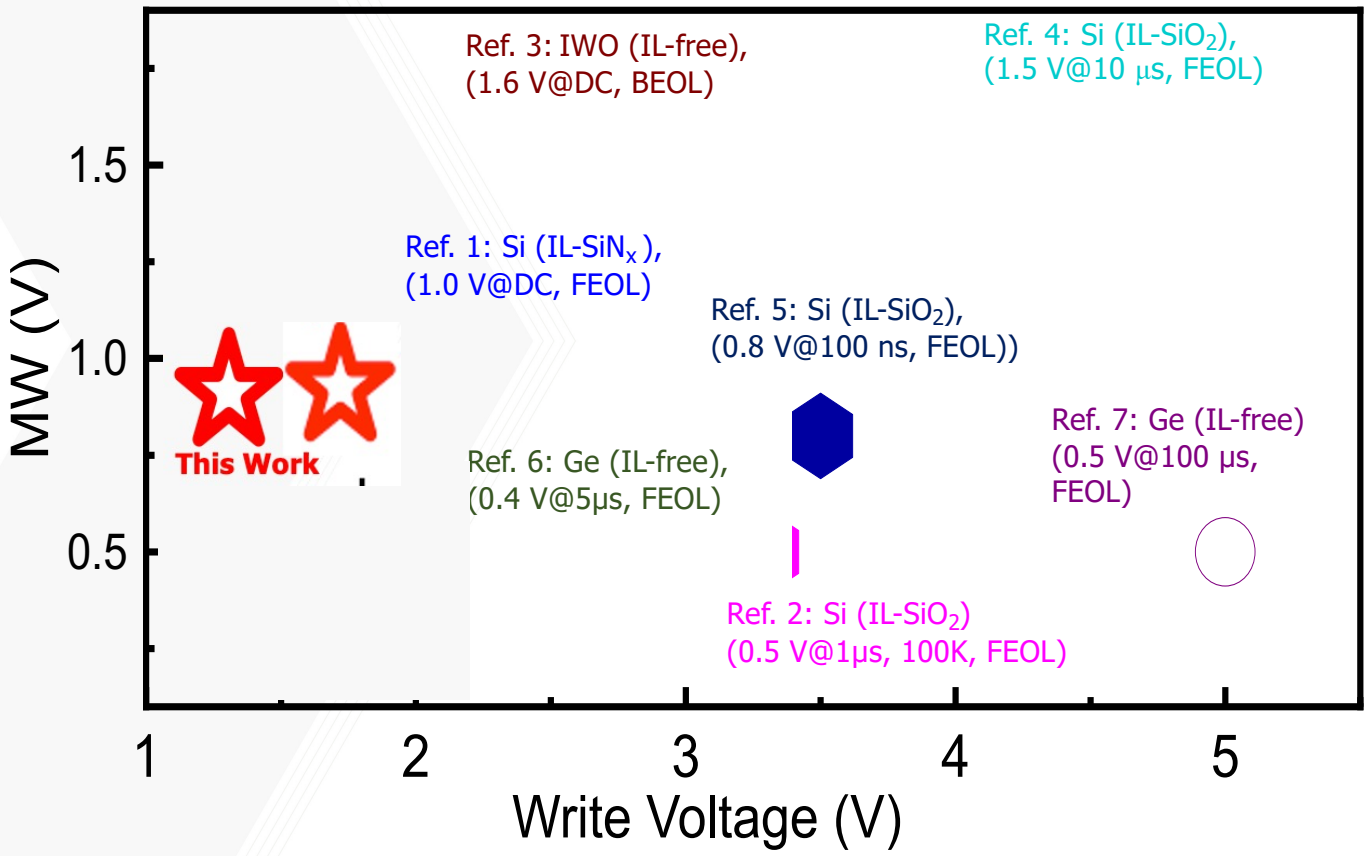
Benchmarking Memory Window v. Write Voltage Tradeoff



Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

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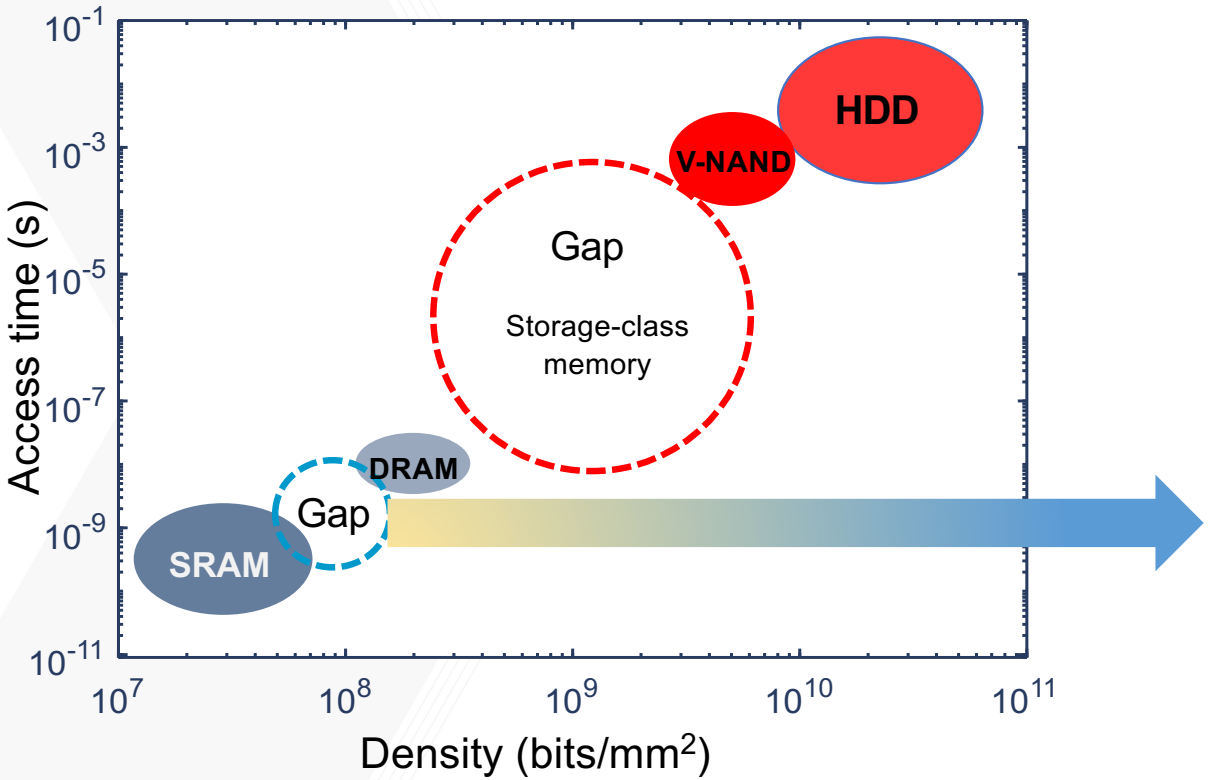
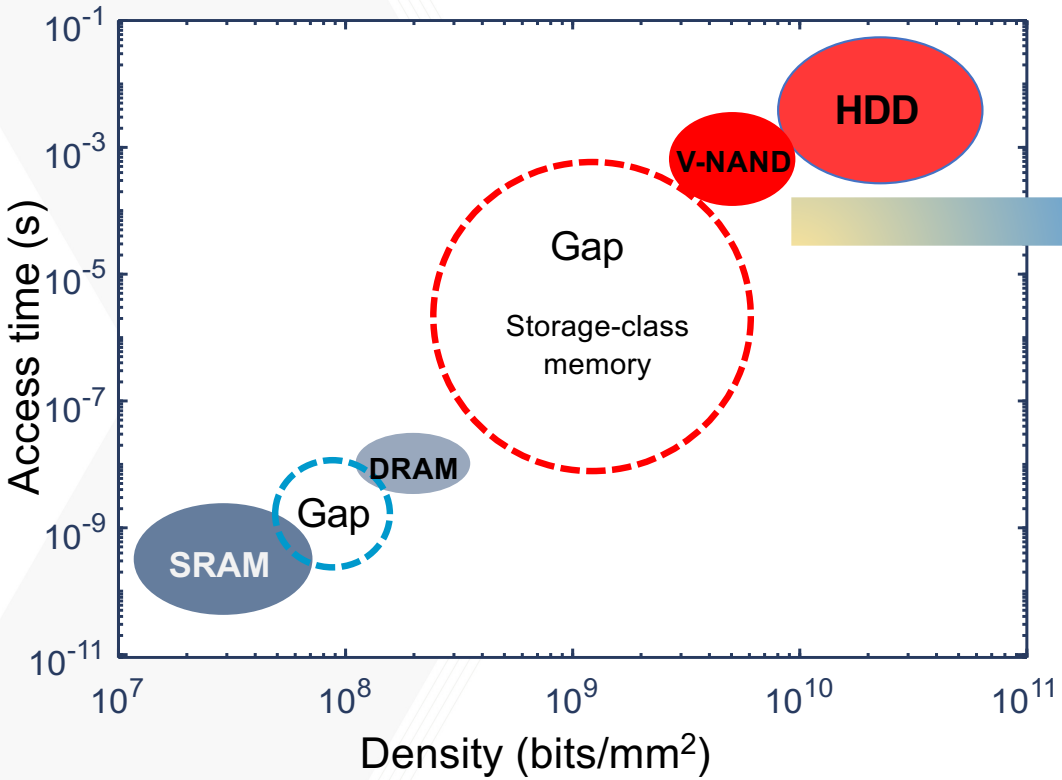
Opportunities for Ferroelectric devices



	Cell area | Speed
DRAM:	6-30F² | <10 ns
FEFET:	5-10F² | 5-10 ns
SRAM:	140-280F² | <1 ns

Opportunities for Ferroelectric devices

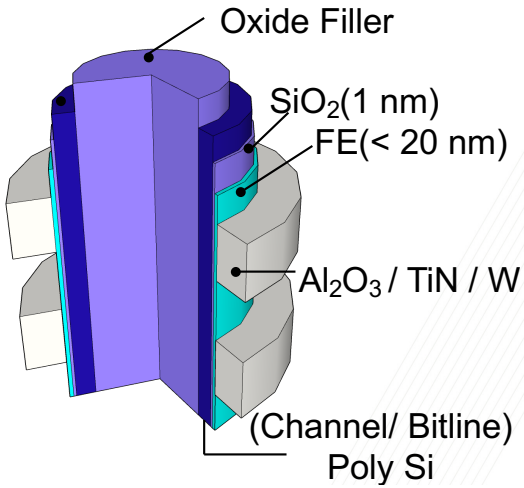


V-NAND FLASH

- Limited scaling (oxide>20 nm)
- High write voltage (~20 V)
- Slow write (1-10 ms)
- Limited endurance (10^3 for MLC)

Ferroelectric V-NAND

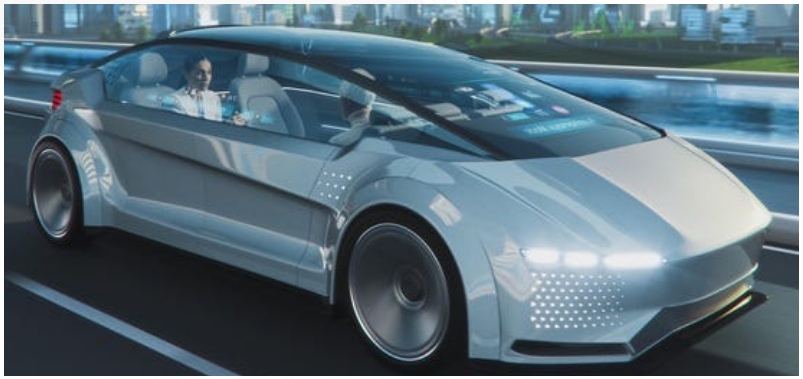
- Scalable oxide (<5 nm)
- Smaller write voltage (~10 V)
- Fast write (<1 μs)

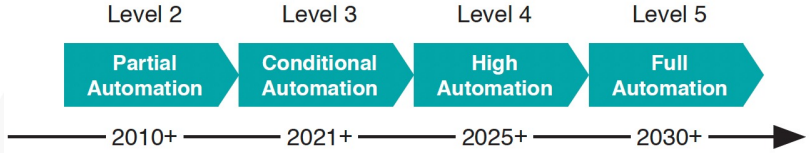


Limits to the possibilities

1

Level 5 autonomous drive



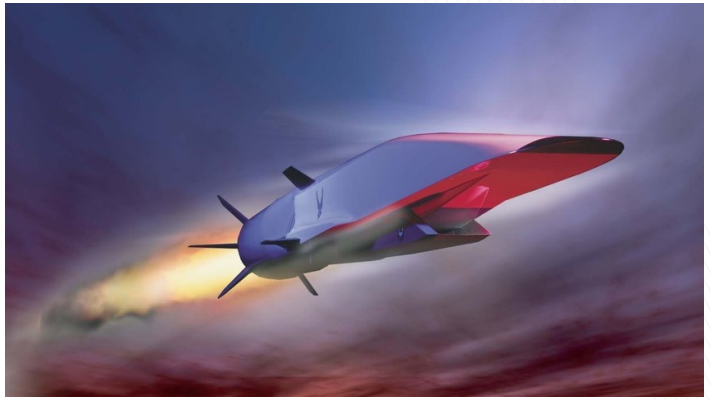


L2 to L5 autonomy will require 10x increase in memory and 100x increase in compute!

Source: SRC Decadal plan

2

Zettascale computing (10^{21} FLOP/s)

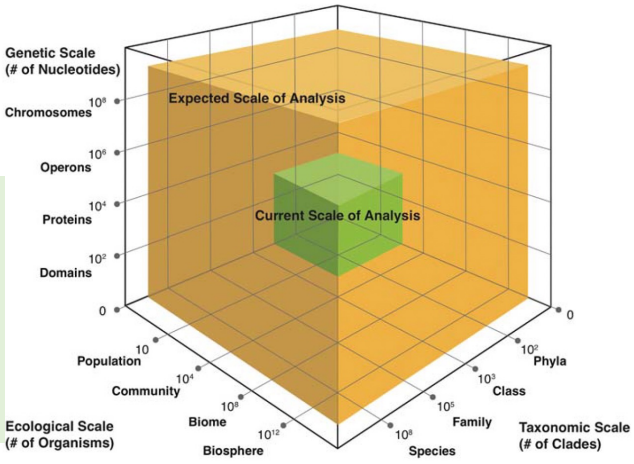


Simulation of a X-51A recoverable hypersonic vehicle over a one-hour flight path is intractable.

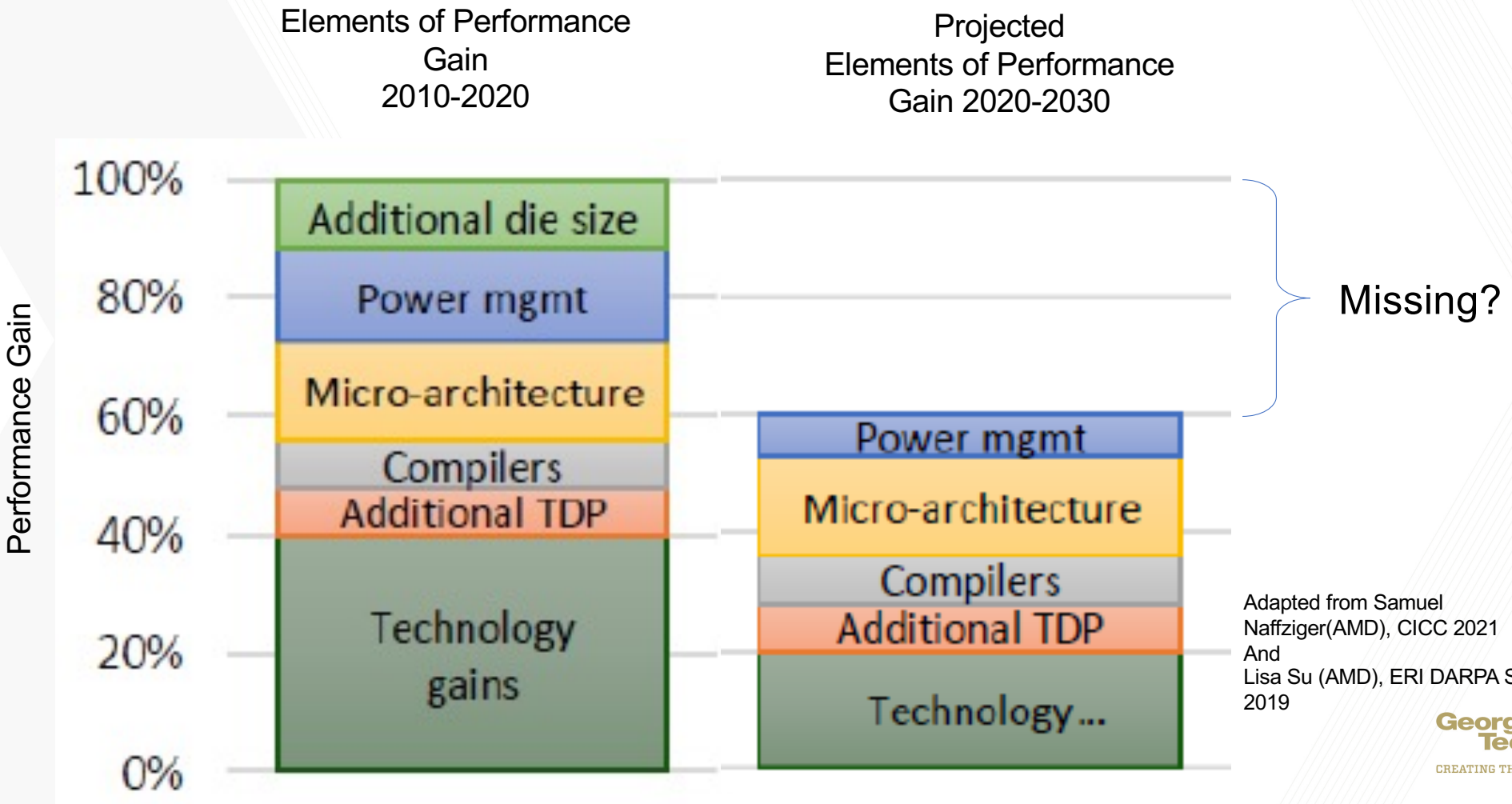
3

Omics data analytics

Advances in sequencing and omics technologies have far outpaced data infrastructure.



Materials are central to *Future* Electronics



Adapted from Samuel Naffziger(AMD), CICC 2021
And
Lisa Su (AMD), ERI DARPA Summit, 2019

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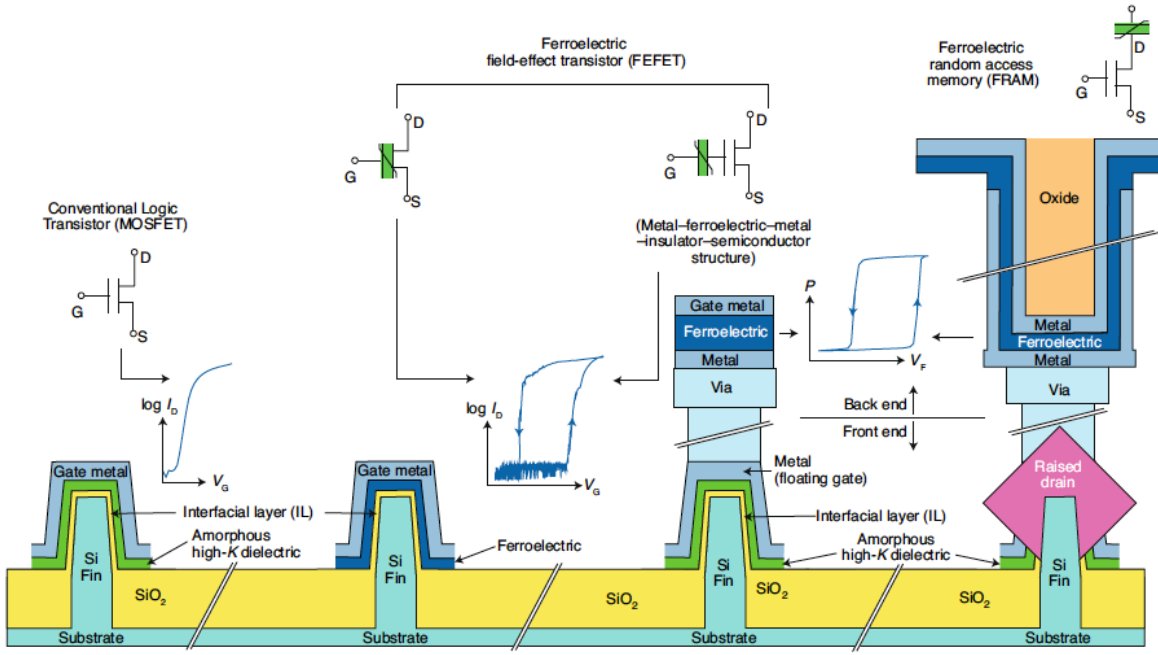
The era of ferroelectronics

The next wave of exponential growth of the semiconductor industry depends on how well the electronic hardware can support the explosion of data-centric computing.

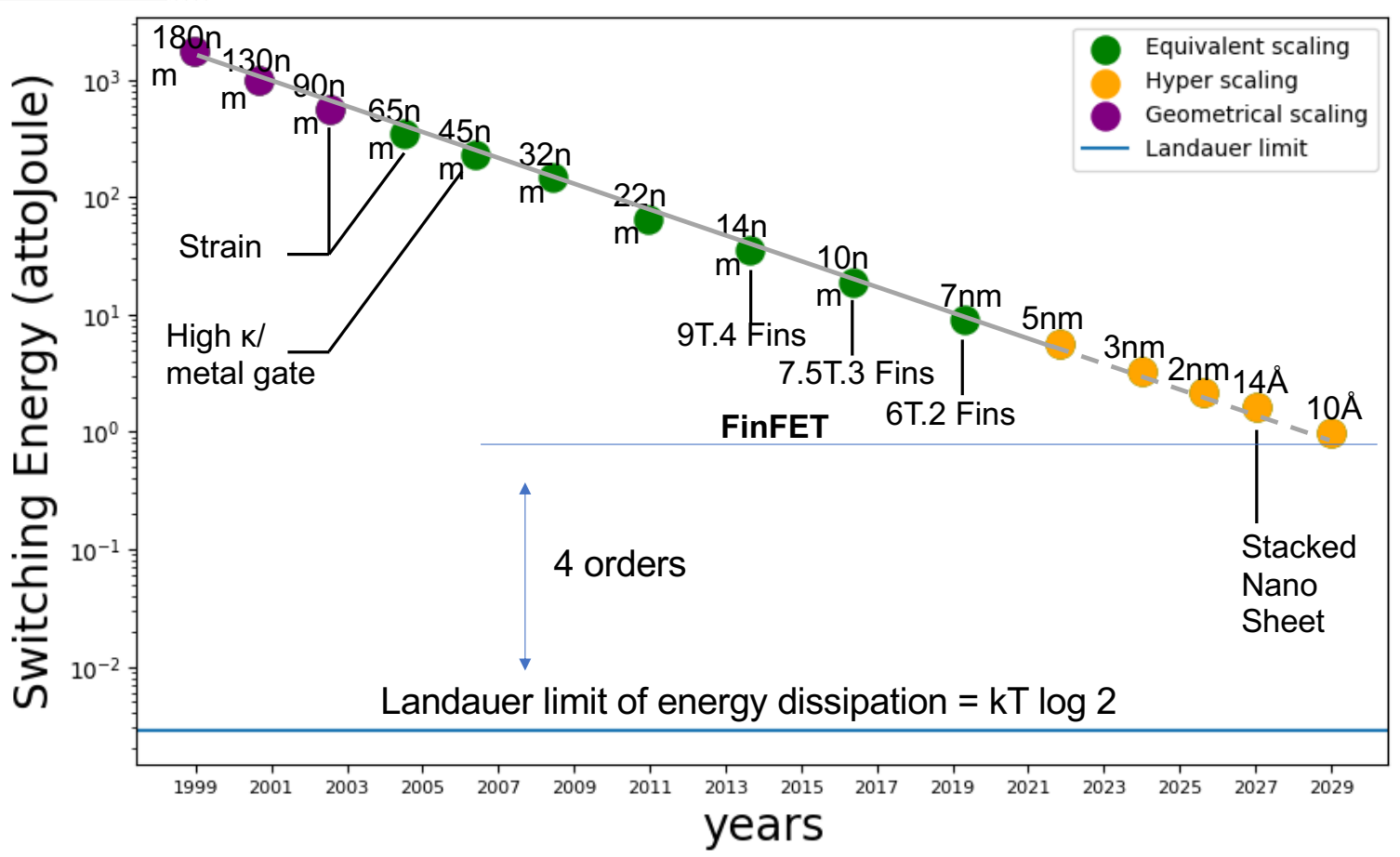


Ferroelectric technology will be a key component because of

1. Performance
2. Energy and area efficiency
3. Logic and memory functionalities

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

Plenty of Room at the Top and Bottom



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Dr. Sarah Lombardo (TEL)


Dr. Nujhat Tasneem (Intel)


Anthony Gaskell (TSMC)

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Thank you


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