Ferroelectric memories

Asif Khan

Associate Professor
School of Electrical and Computer Engineering
School of Materials Science and Engineering
Georgia Institute of Technology
akhan40@gatech.edu

Solid-State Circuits Directions (SSCD) Workshop: Non-Traditional Computing Paradigms with Emerging Technologies for Energy Efficiency Workshop – 11/09/2023

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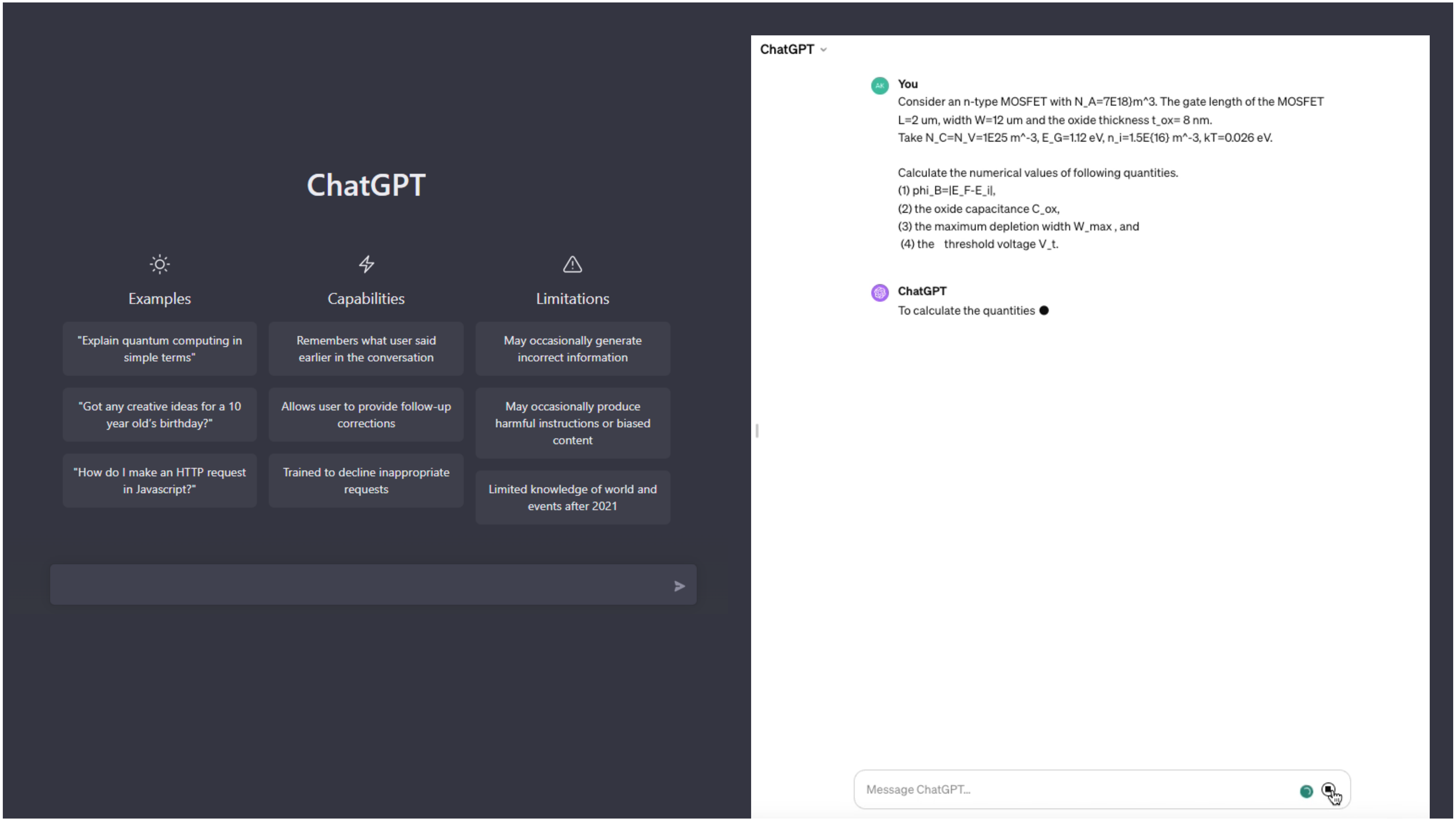
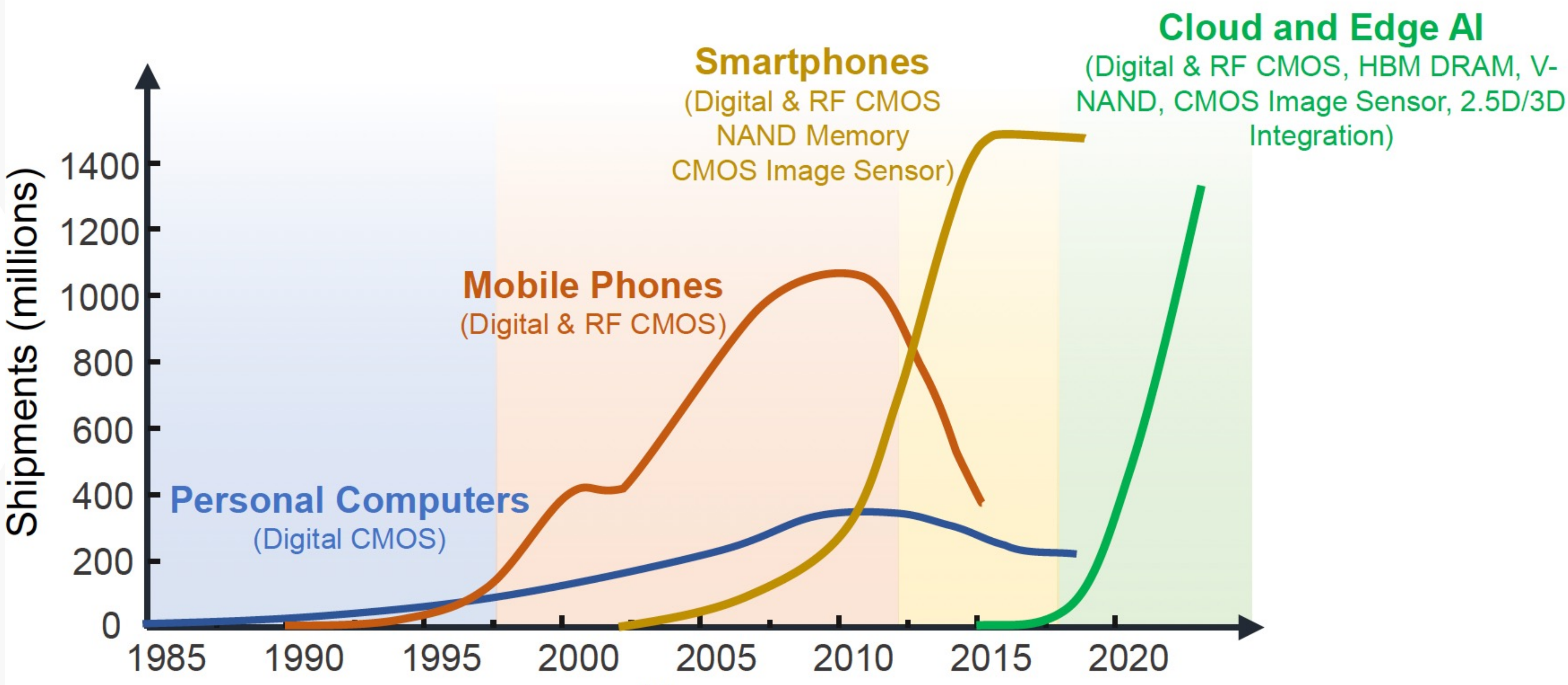
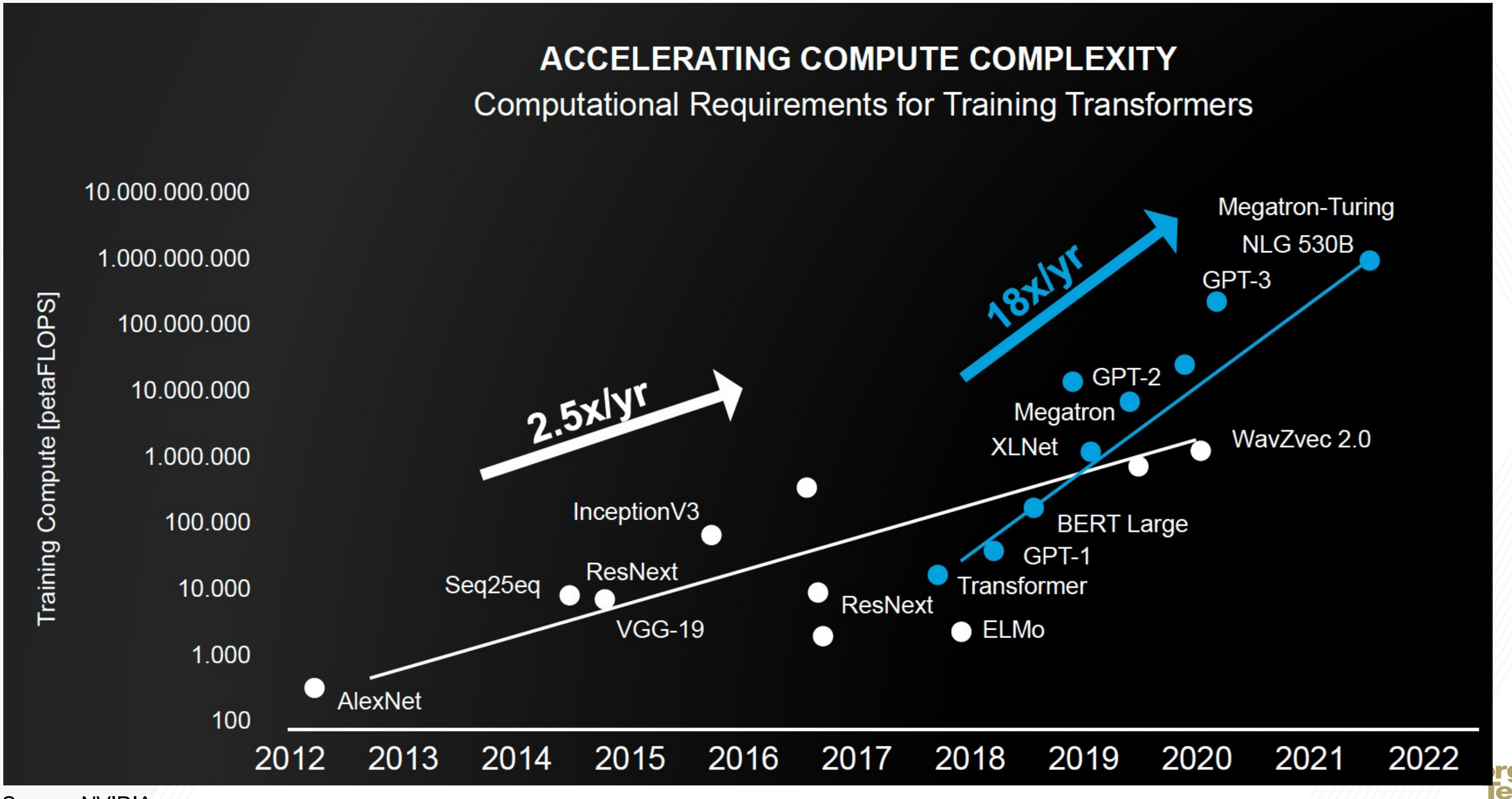

ChatGPT
Examples
Capabilities
Limitations
"Explain quantum computing in simple terms"
Remembers what user said earlier in the conversation
May occasionally generate incorrect information
"Got any creative ideas for a 10 year old's birthday?"
Allows user to provide follow-up corrections
May occasionally produce harmful instructions or biased content
"How do I make an HTTP request in Javascript?"
Trained to decline inappropriate requests
Limited knowledge of world and events after 2021
ChatGPT
You
Consider an n-type MOSFET with N_A=7E18}m^3. The gate length of the MOSFET
L=2 um, width W=12 um and the oxide thickness t_ox= 8 nm.
Take N_C=N_V=1E25 m^-3, E_G=1.12 eV, n_i=1.5E{16} m^-3, kT=0.026 eV.
Calculate the numerical values of following quantities.
(1) phi_B=|E_F-E_i|,
(2) the oxide capacitance C_ox,
(3) the maximum depletion width W_max , and
(4) the threshold voltage V_t.
ChatGPT
To calculate the quantities
Message ChatGPT...

How the computing paradigms have evolved



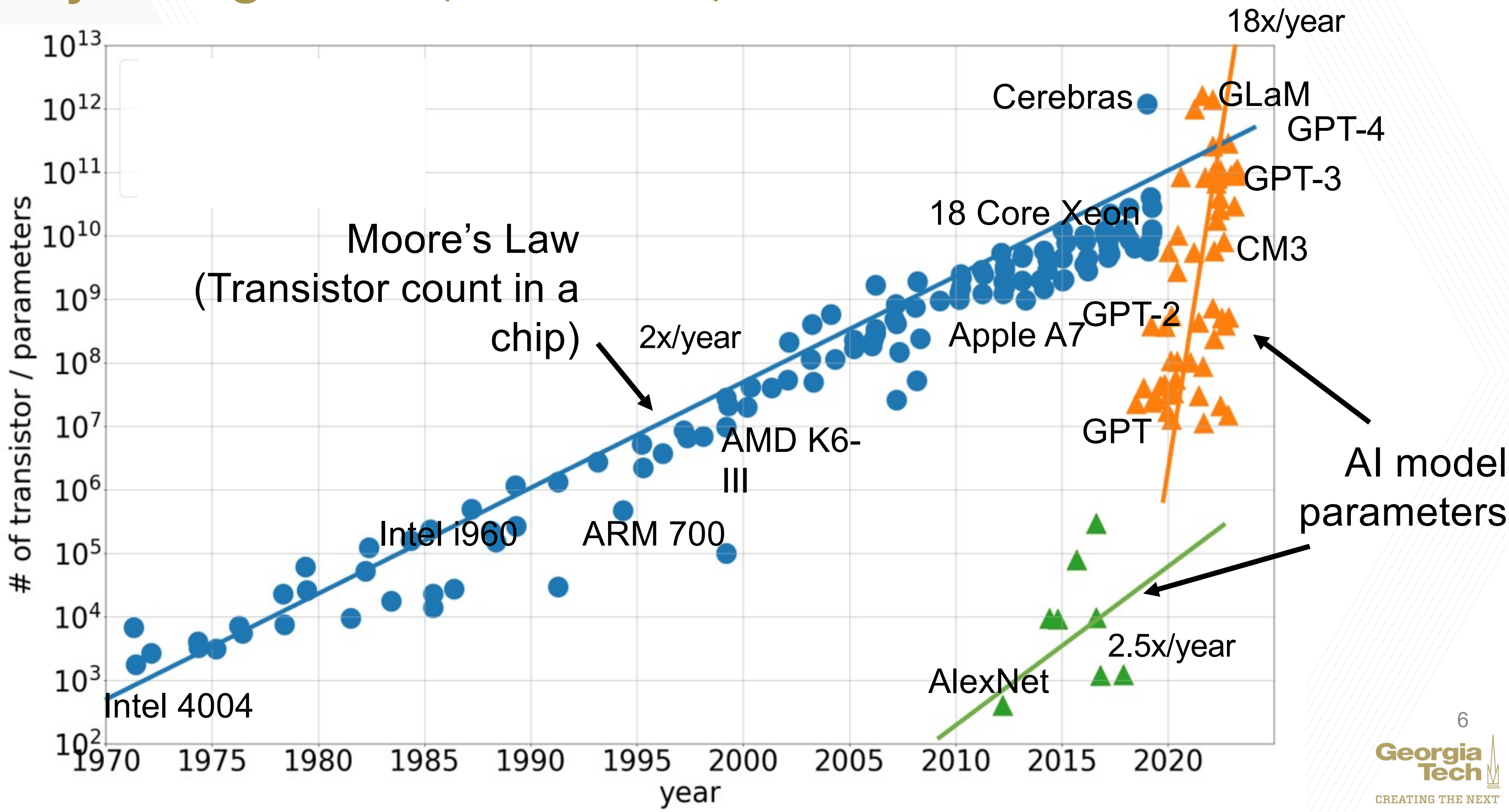
Adapted from: Datta, EDTM 2023
https://www.economist.com/briefing/2015/02/26/the-truly-personal-computer
https://www.statista.com/chart/12798/global-smartphone-shipments/

Evolution of AI model parameter count



Source: NVIDIA

A story of algorithm, software, and hardware



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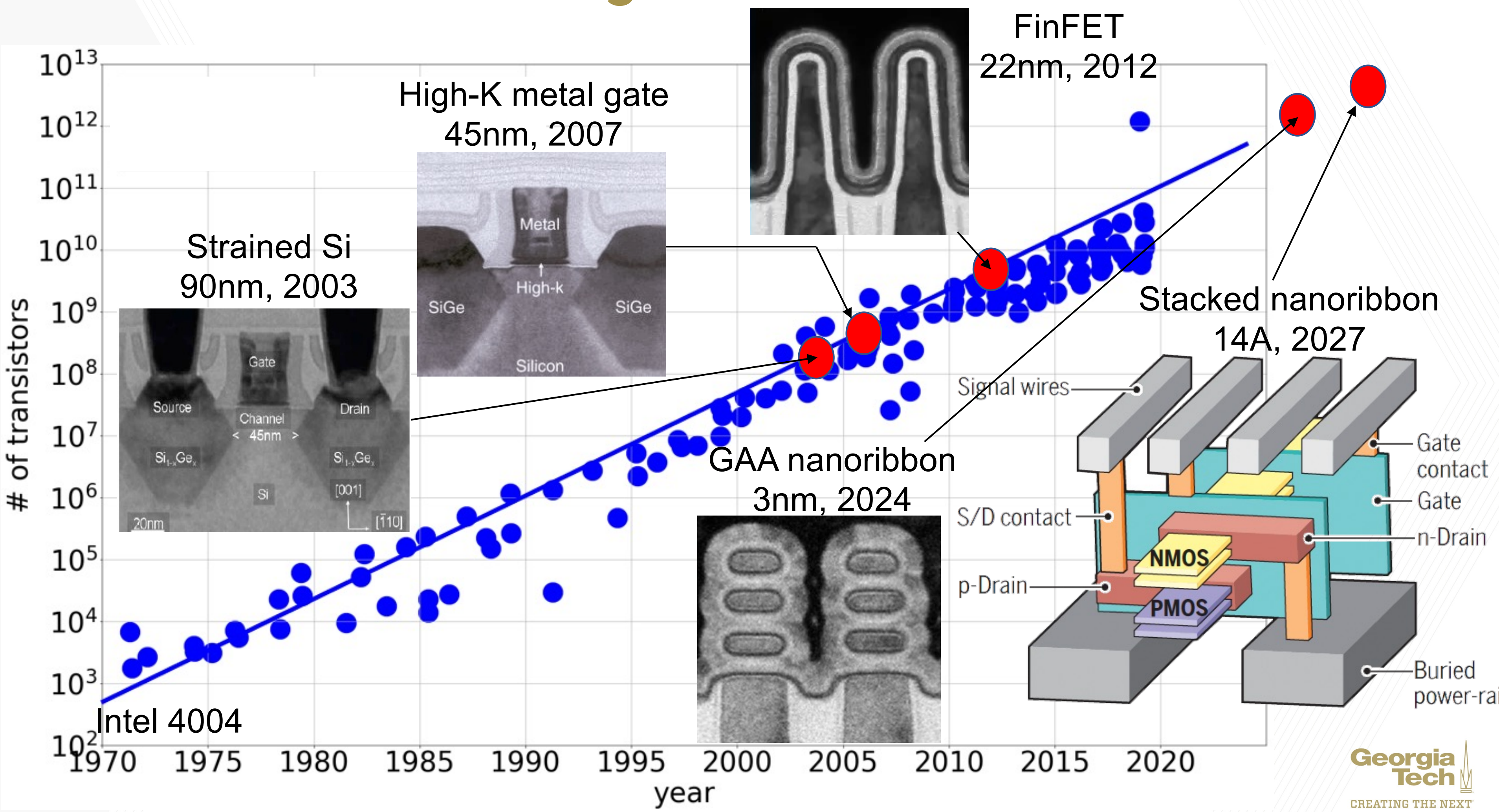
Innovation at the core – Logic transistor



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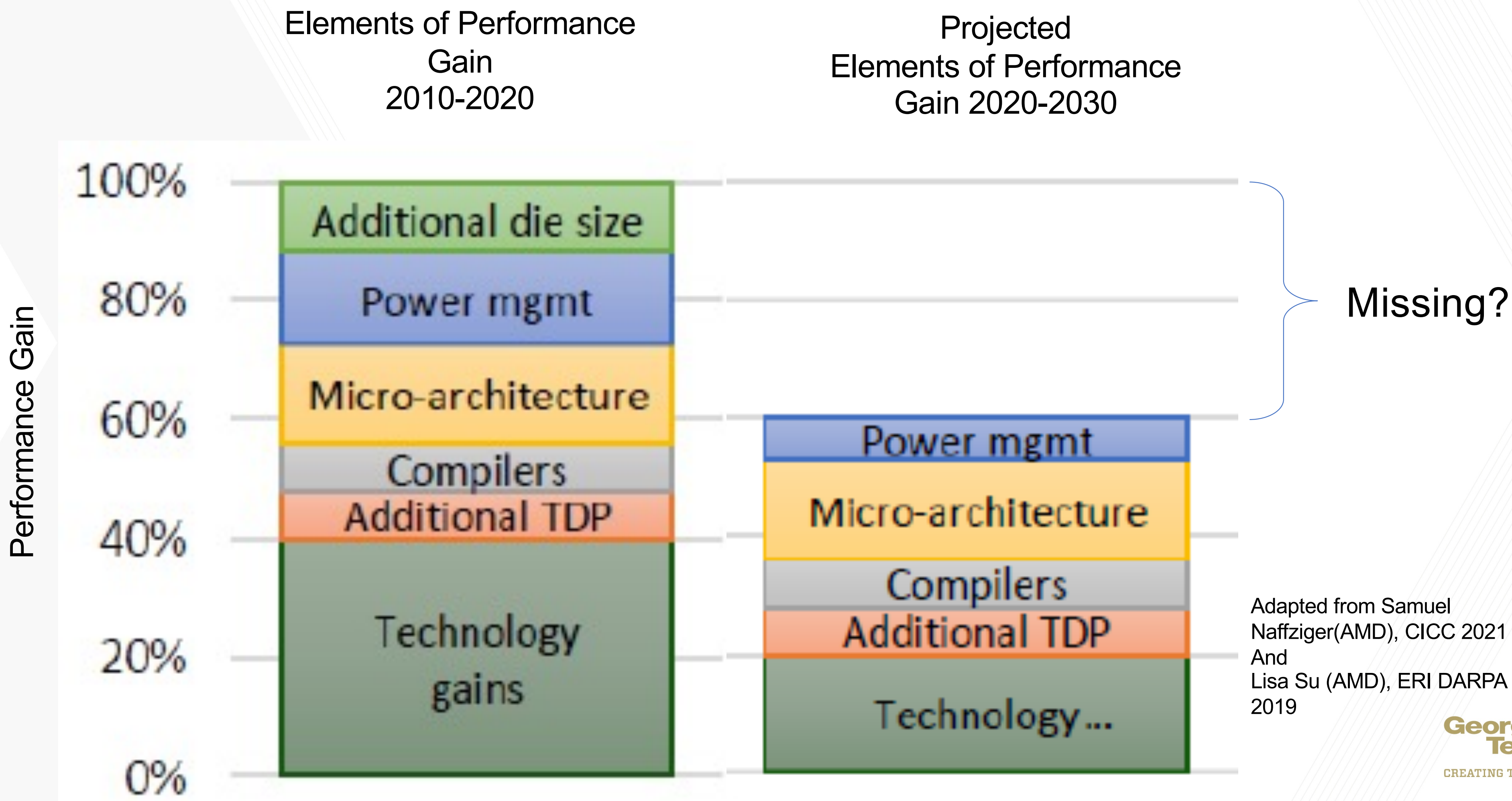
Materials are central to *Future* Electronics



Adapted from Samuel Naffziger(AMD), CICC 2021
And
Lisa Su (AMD), ERI DARPA Summit, 2019

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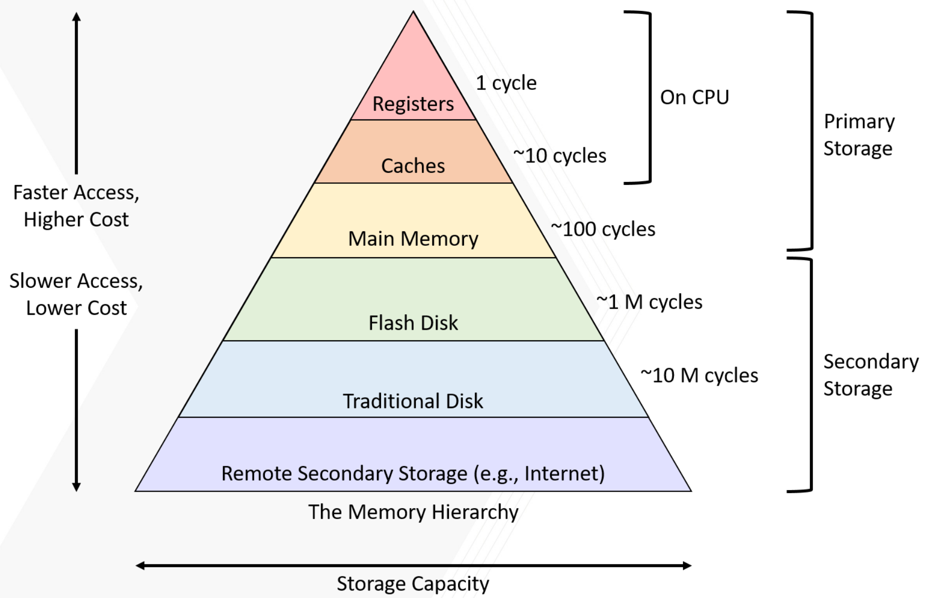
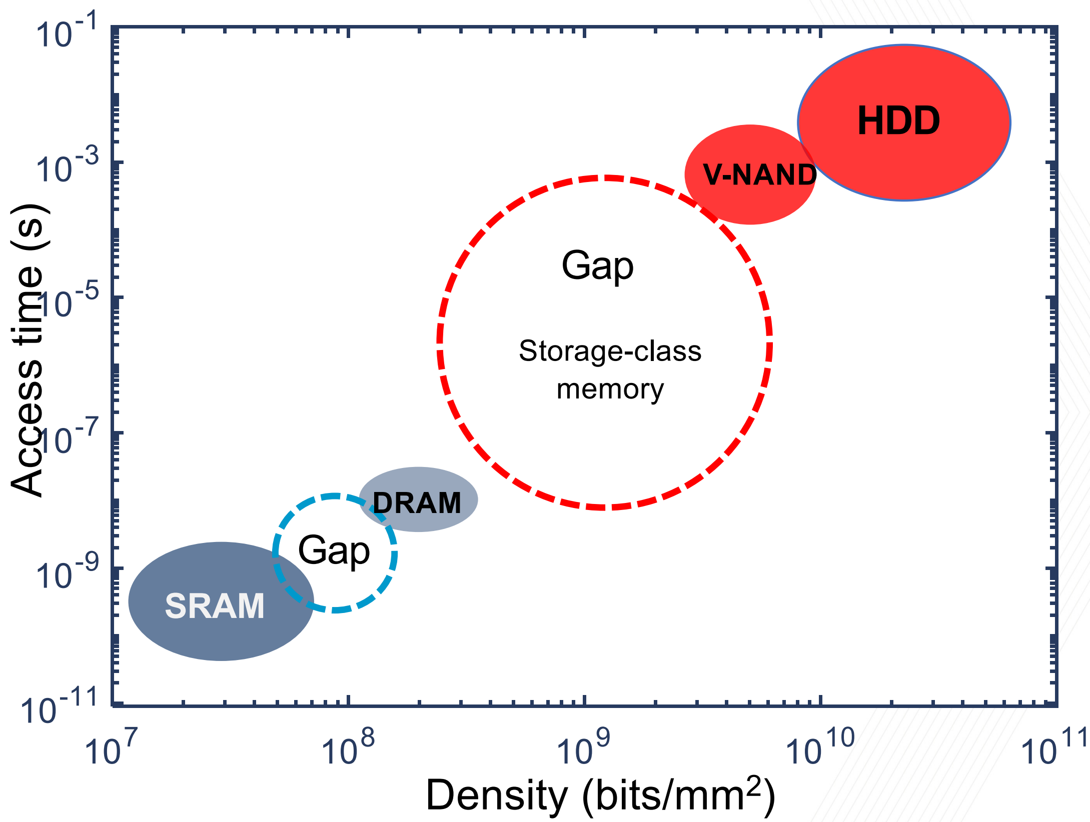
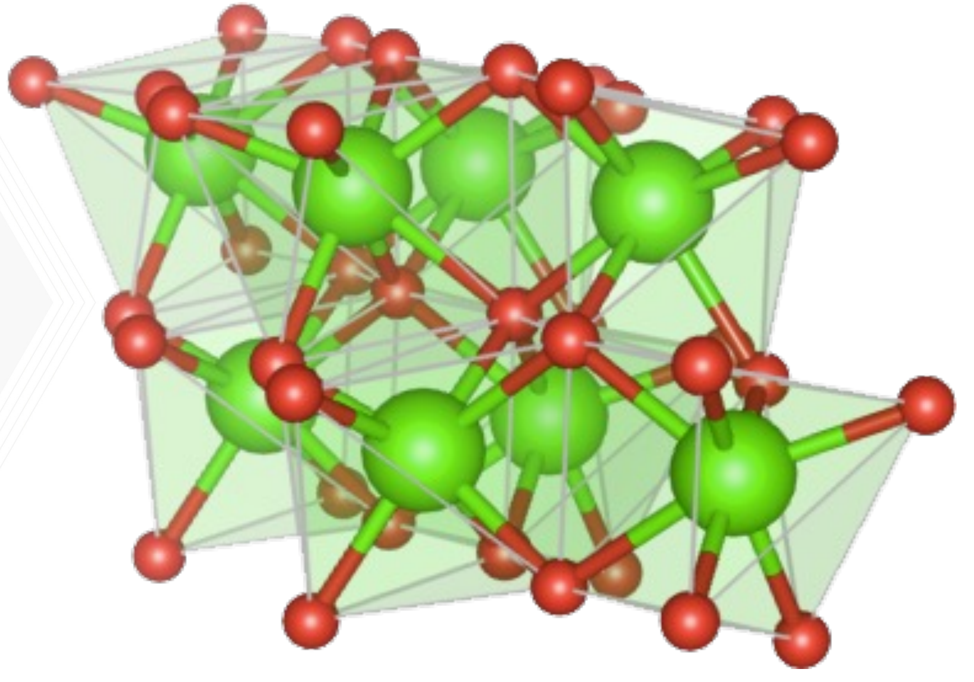
Memory Landscape





Let’s dive down to devices and materials



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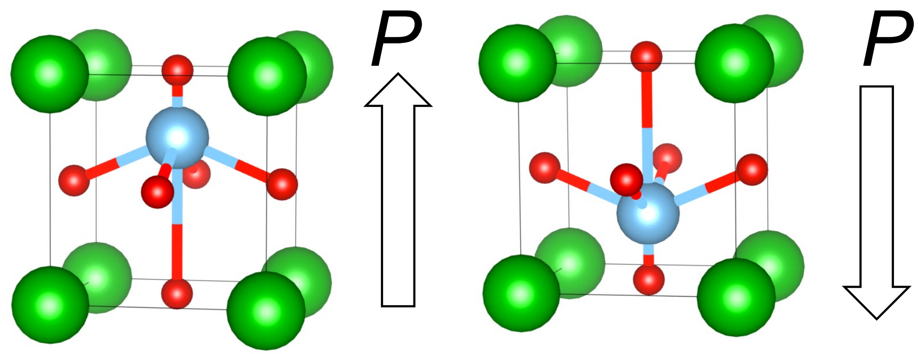
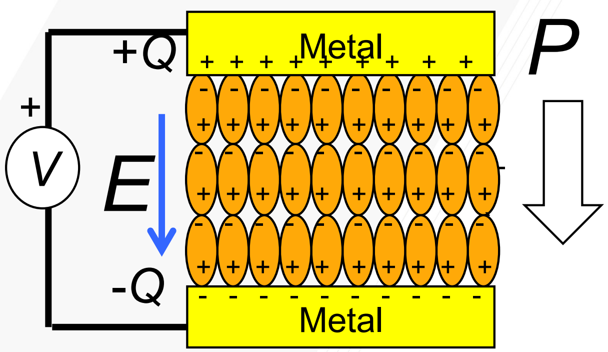
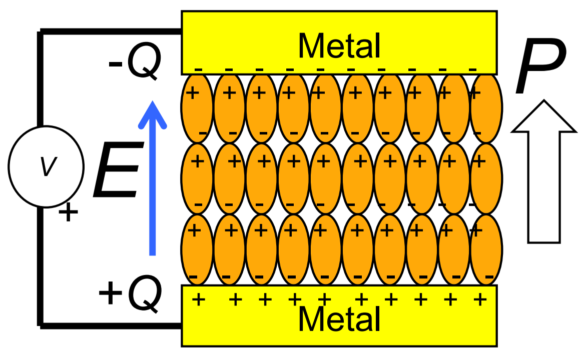
Ferroelectricity

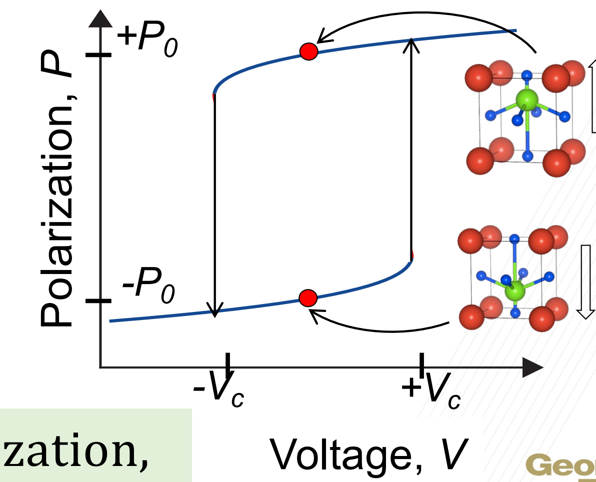
Classical Ferroelectric
$PbTiO_3$, $BaTiO_3$ etc.

Emerging CMOS compatible Ferroelectrics:
Doped HfO_2









A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

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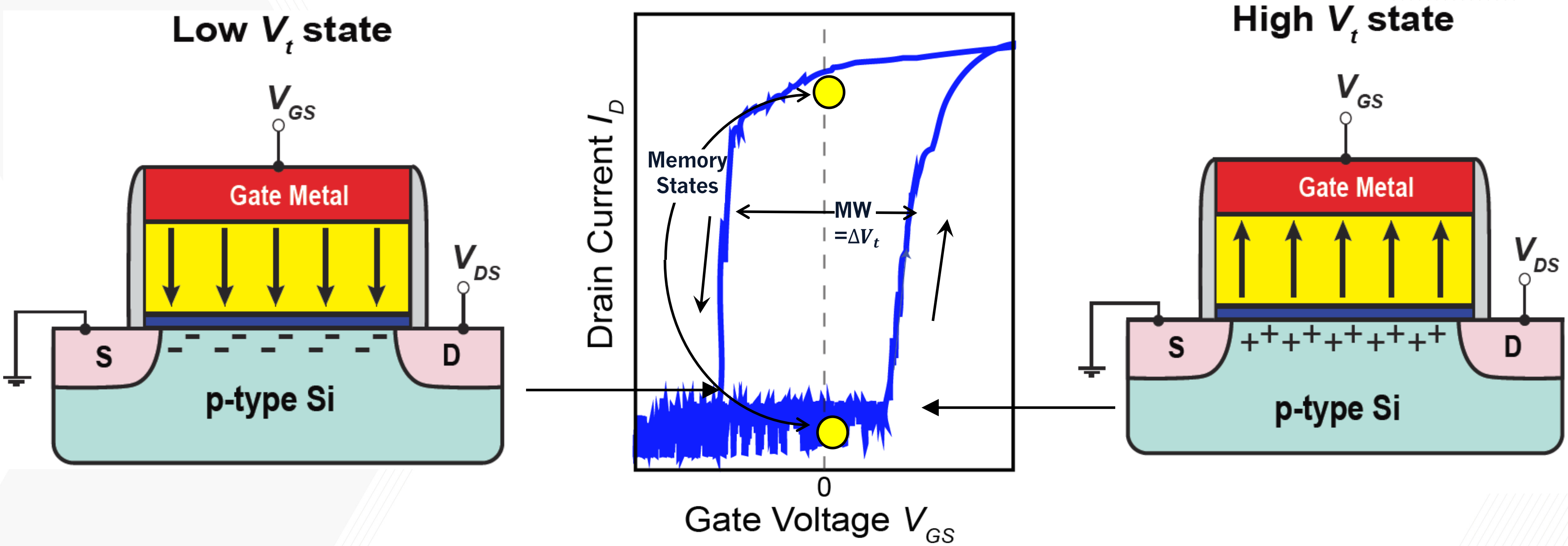
Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the “remnant” polarization.

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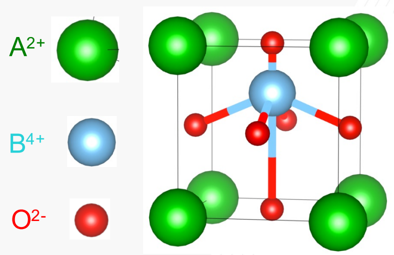
Ferroelectrics in microelectronics: Why now?

1. Ramtron (acquired by Cypress Semiconductor), Texas Instruments, and Fujitsu marketed FRAM products for niche, low-volume applications such as smart cards, energy meters, airplane black boxes, radio frequency tags and wearable medical devices, as well as for for code storage in microcontrollers.

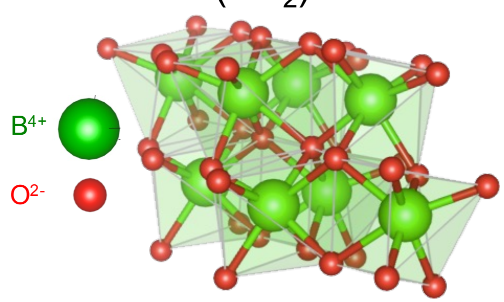
2. Controlled annealing in fluorite structure oxides (such as those based on HfO_2 and ZrO_2 and their alloyed variants) leads to ferroelectricity.

- Boscke *et al. Appl. Phys. Lett*. 99, 112904 (2011)
- Boscke *et al. 2011 IEEE Int. Electron Devices Meeting.* p. 24.5.1–24.5.4 (IEEE, 2011).
- Muller *et al. Nano Lett.* 12, 4318 (2012)

Perovskite-structure ferroelectric oxide (ABO_3)



Fluorite-structure ferroelectric oxide (BO_2)



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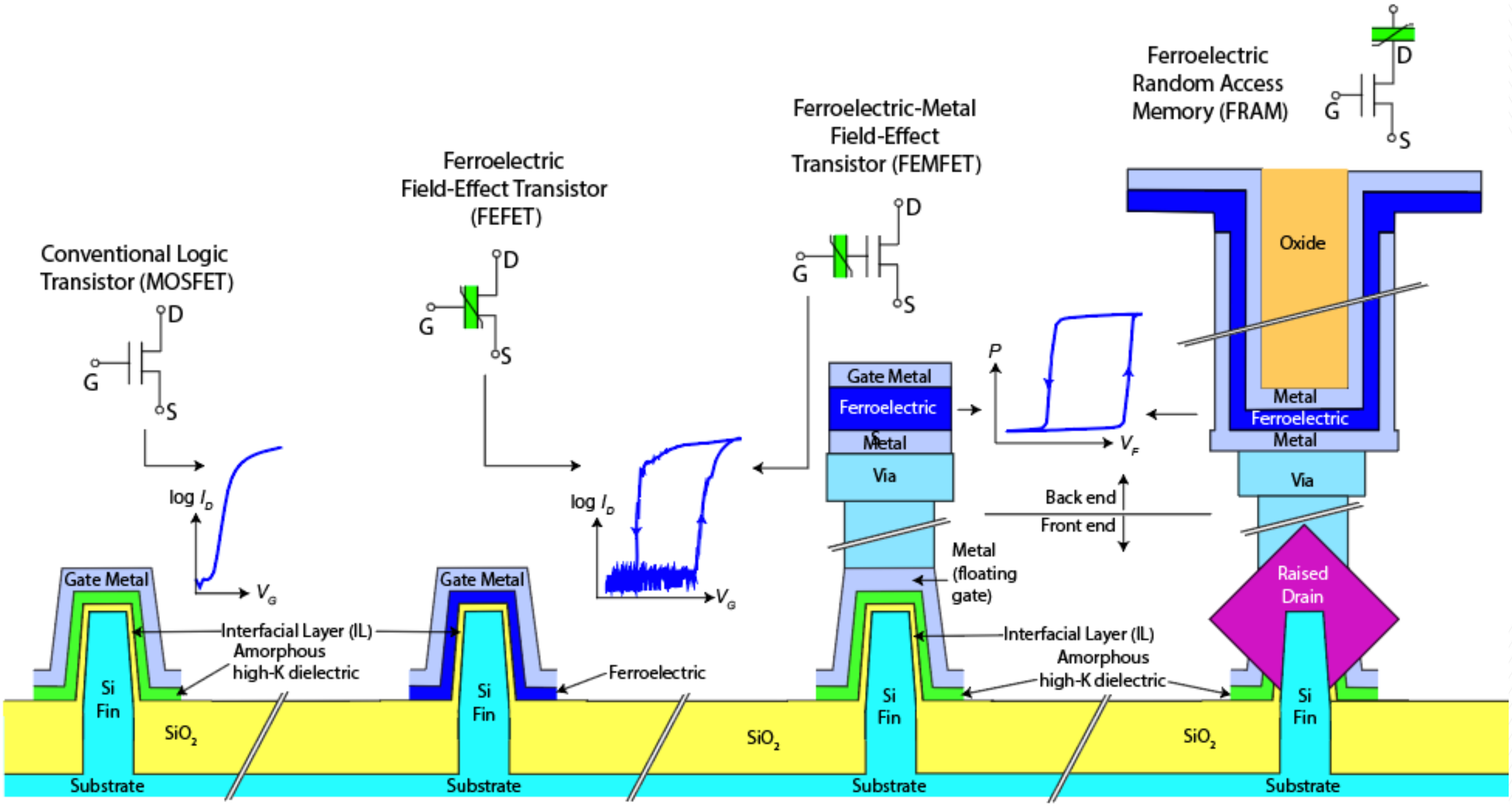
Ferroelectric devices (1 of 2)



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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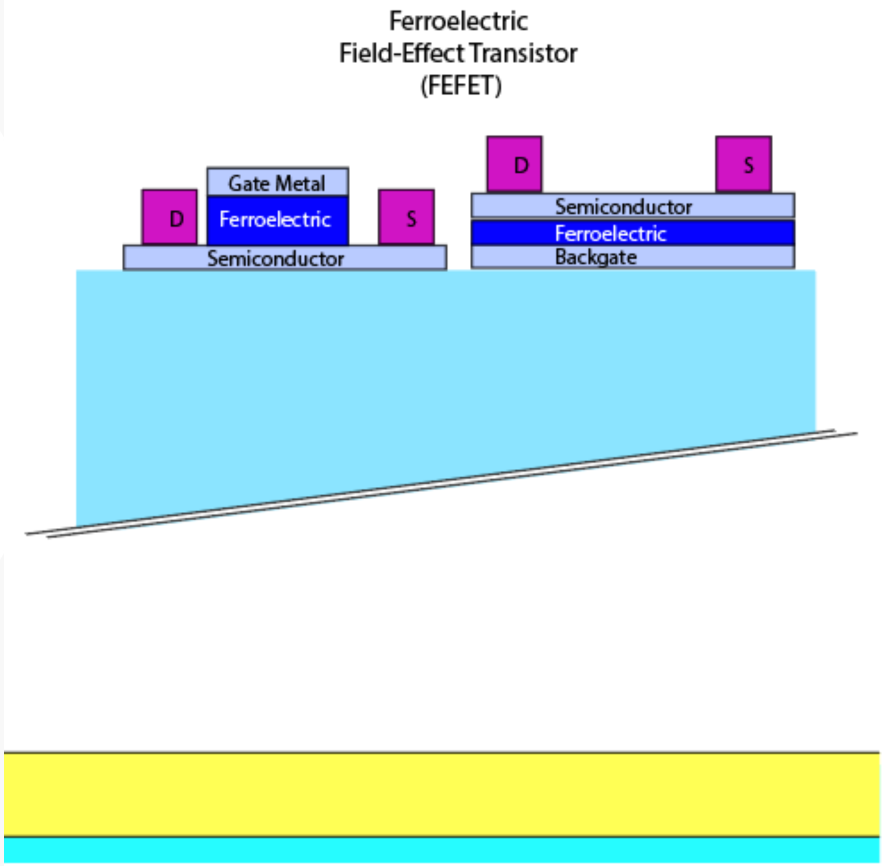
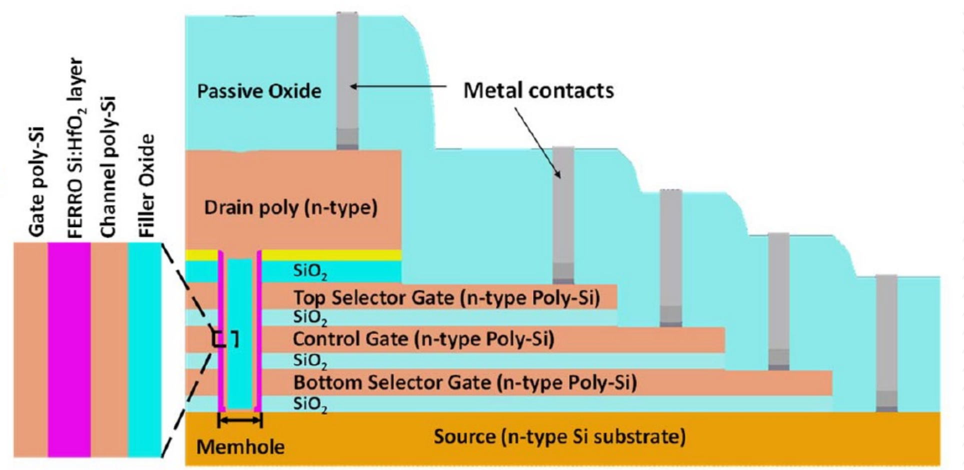
Ferroelectric devices (2 of 2)

BEOL FEFET



Vertical FEFET for NAND Storage



(b)

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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FEFET as an embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM[70]	eFlash (FG)	eFlash (SG MONOS)[42]	eFlash (SONOS)[41]	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based)[67]
Cell size	120–150F^2	40F^2	40–60F^2	40–50F^2	50–60F^2	10–30F^2	10–30F^2	30–40F^2	50–60F^2
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 µs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	$>10^{16}$	$>10^{16}$	$\sim10^4$	$\sim10^5$	$\sim10^6$	10^5–10^9	$>10^{10}$	$>10^{12}$	$>10^{14}$

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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Progress in FEFET technology

1 Write voltage and Memory Window	2 Read/Write Speed	3 Device-to-device variation	4 Reliability and endurance
Specs			
<1.5 V write voltage >0.5 V memory window	<10 ns write speed <10 ns read-after-write delay	$\Delta V_{t,3\sigma}$ = 20-50 mV (7 nm node)	>10^{12} cycles

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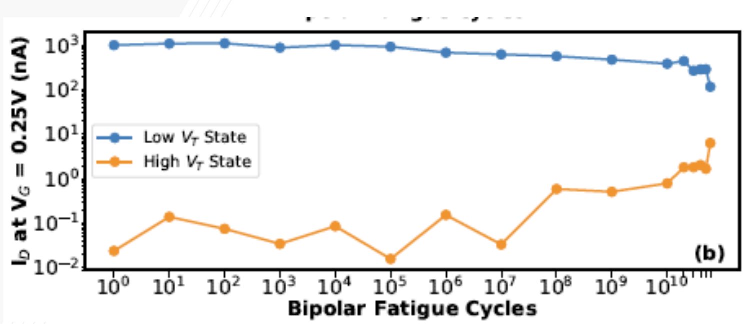
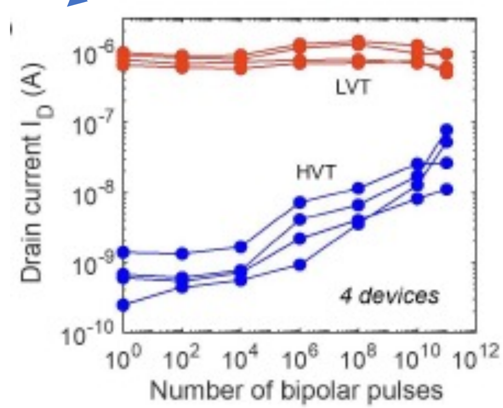


Tan et al. IEEE EDL 42, 994 (2021).



Dutta et al. IEEE EDL 43, 383 (2022).

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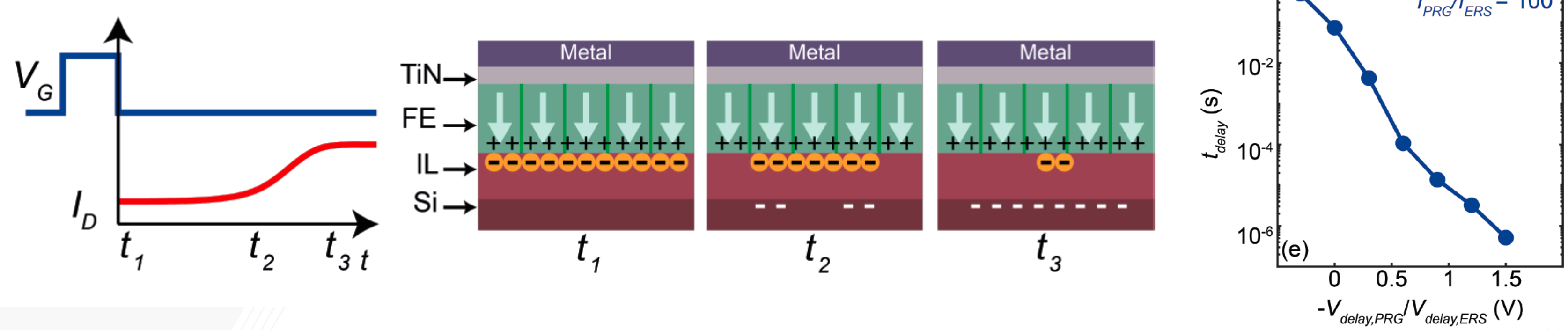

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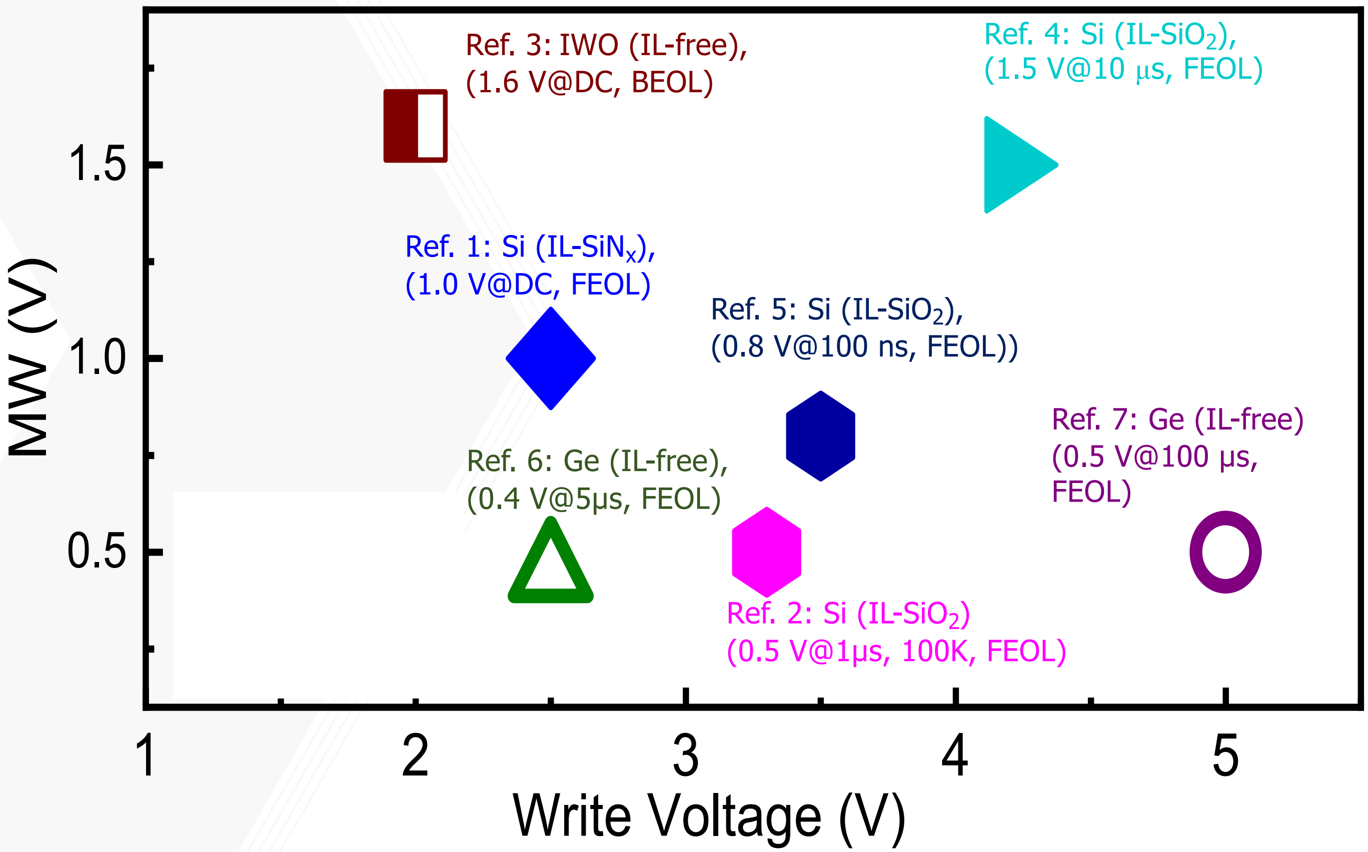
Wang, Z., Tasneem, N., Hur, J., Chen, H., Yu, S., Chern, W., & Khan, A. (2021, December). Standby bias improvement of read after write delay in ferroelectric field effect transistors. In *2021 IEEE International Electron Devices Meeting (IEDM)* (pp. 19-3). IEEE.

Benchmarking Memory Window v. Write Voltage Tradeoff



[1] Tan *et al., IEEE EDL*, 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

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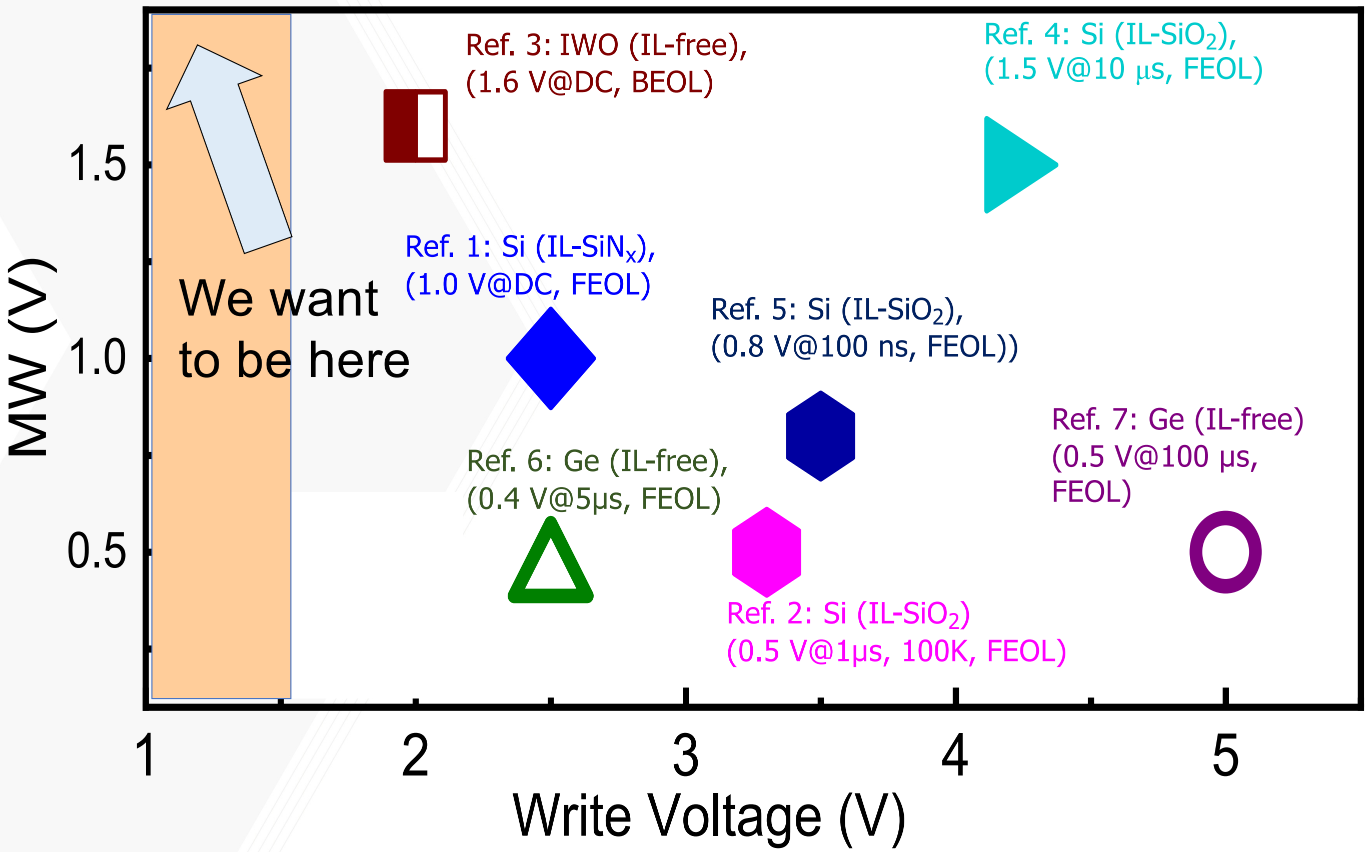
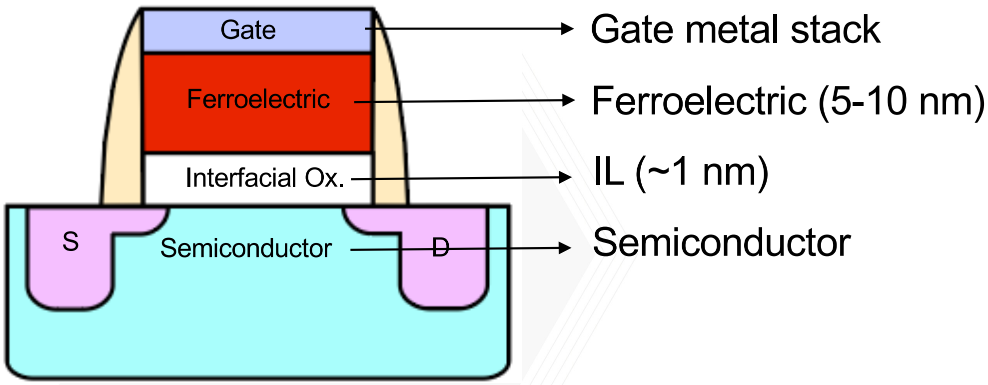
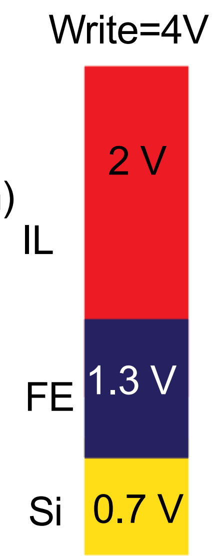
Benchmarking Memory Window v. Write Voltage Tradeoff

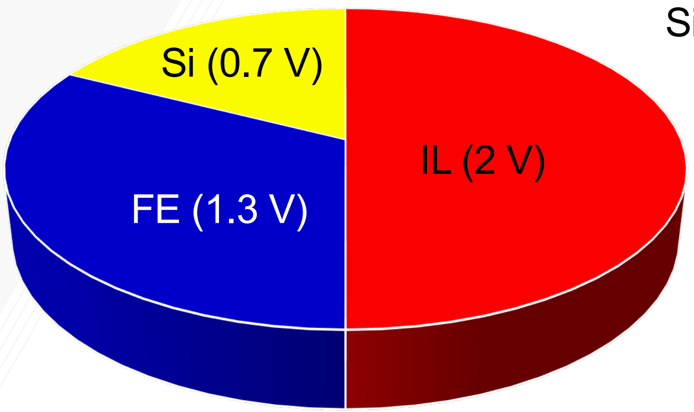


[1] Tan *et al.*, *IEEE EDL*, 42, 994, (2021).
[2] Tan *et al.*, *2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al.*, *IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al.*, *IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al.*, *IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

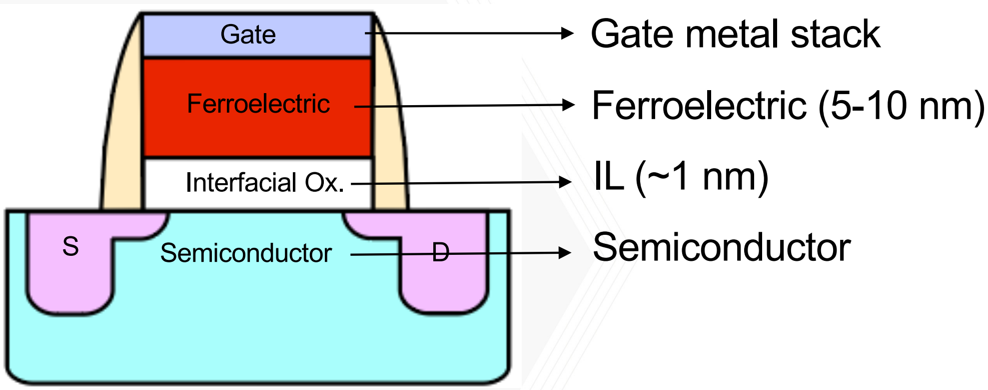
Write voltage vs. memory window trade-off

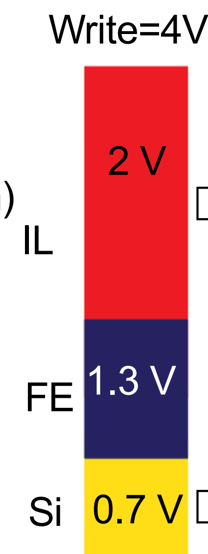






Write voltage vs. memory window trade-off

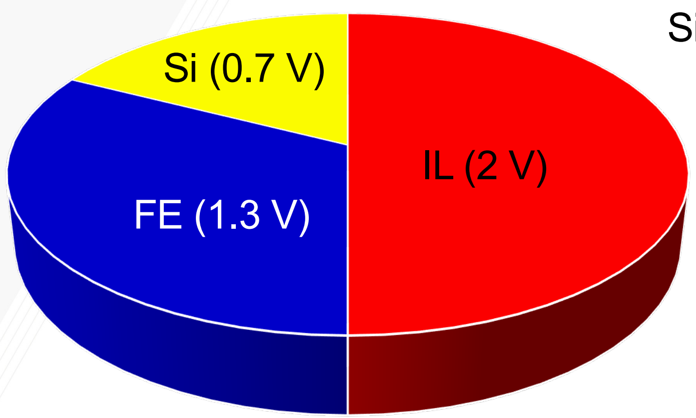




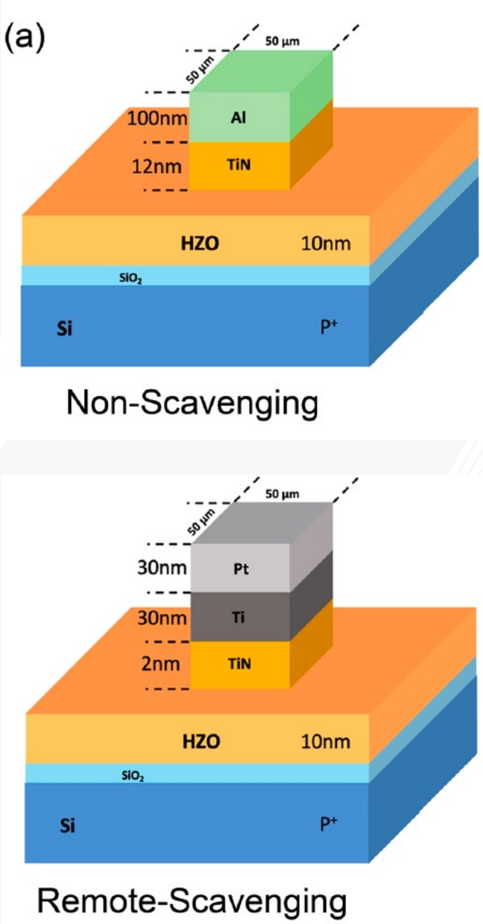
Reducing the thickness of the IL or increasing the K of the IL.

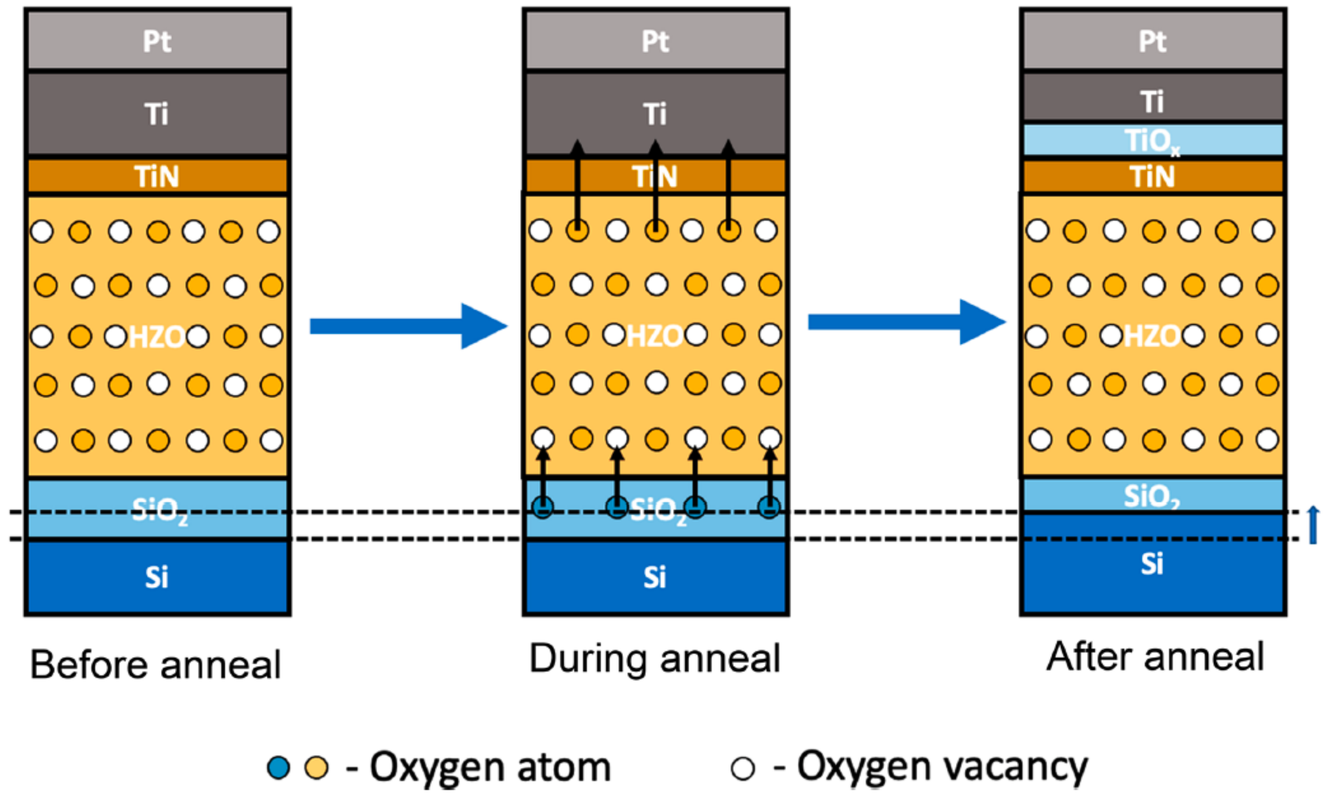
Reducing FE thickness reduces MW. $MW_{max}=2V_C$

Changing the band-gap of the semiconductor By changing the channel material from Si to SiGe or Ge.



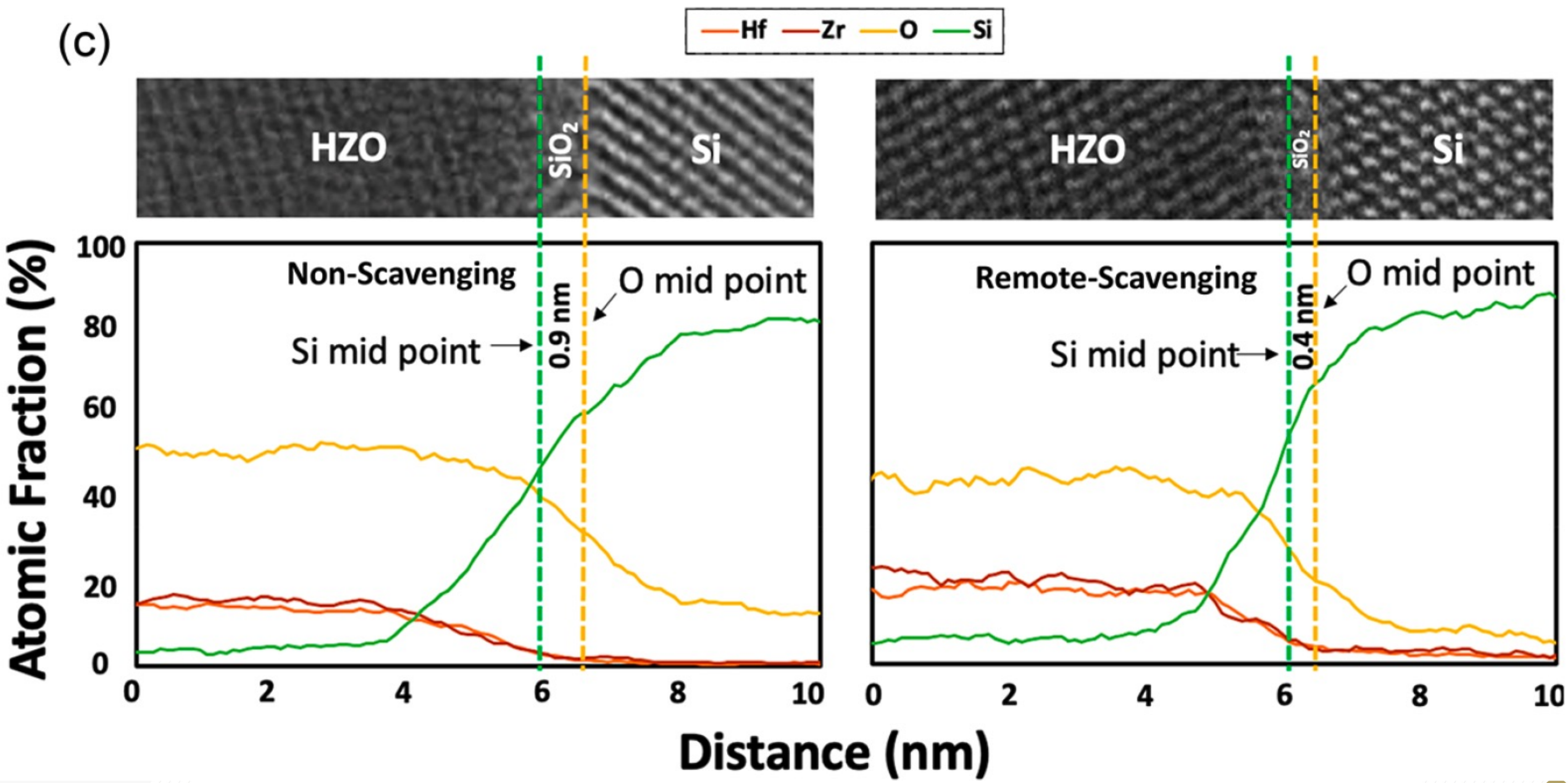
Remote oxygen scavenging to reduce IL thickness





Tasneem et al. "Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium−Zirconium Oxide-Based Metal−Oxide−Semiconductor Structures", ACS Appl. Mater. Interfaces 2022, 14, 43897−43906

Remote oxygen scavenging to reduce IL thickness



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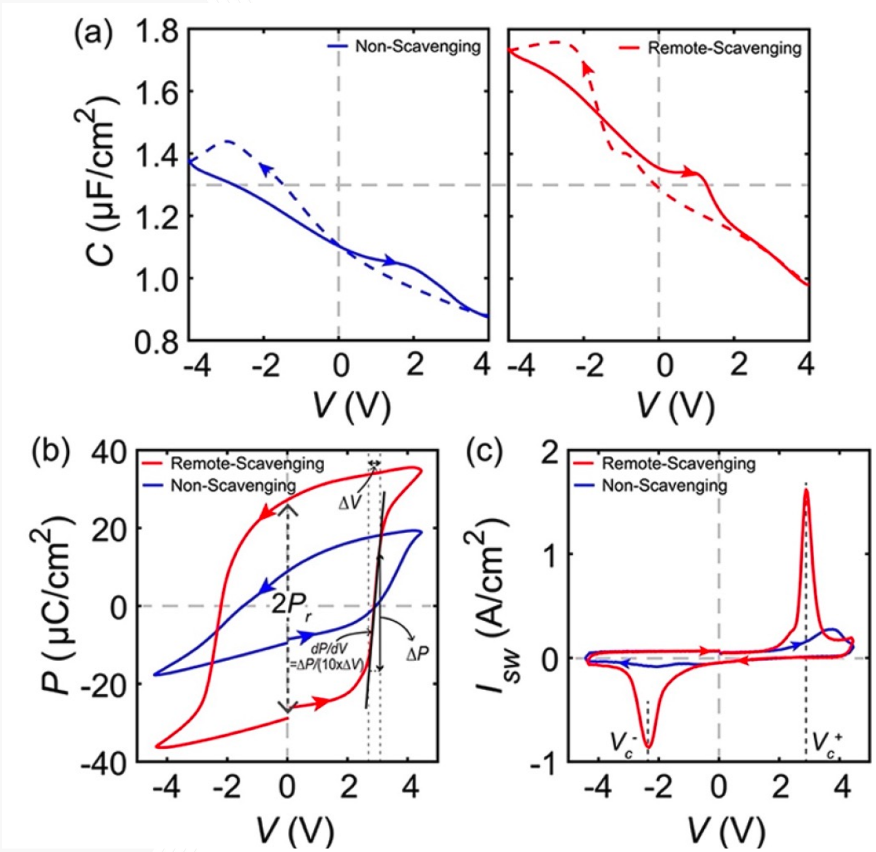

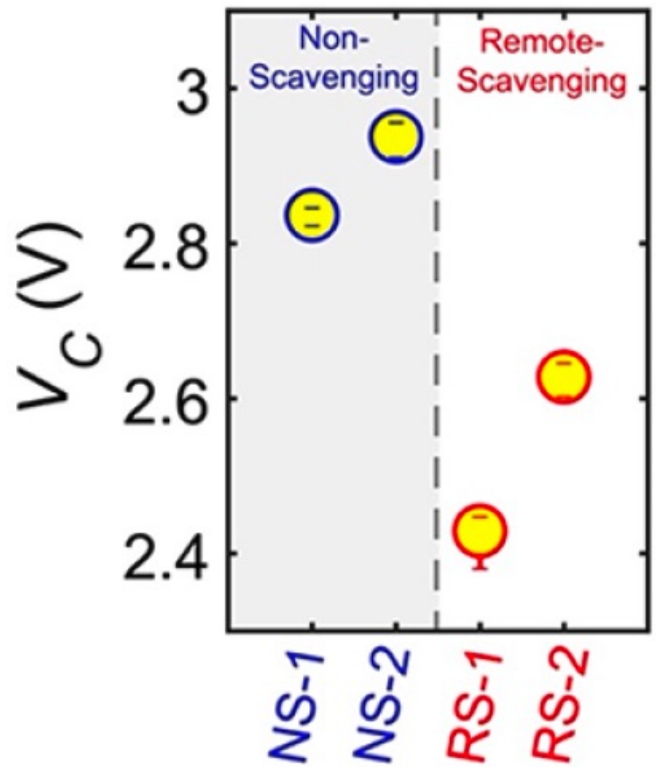

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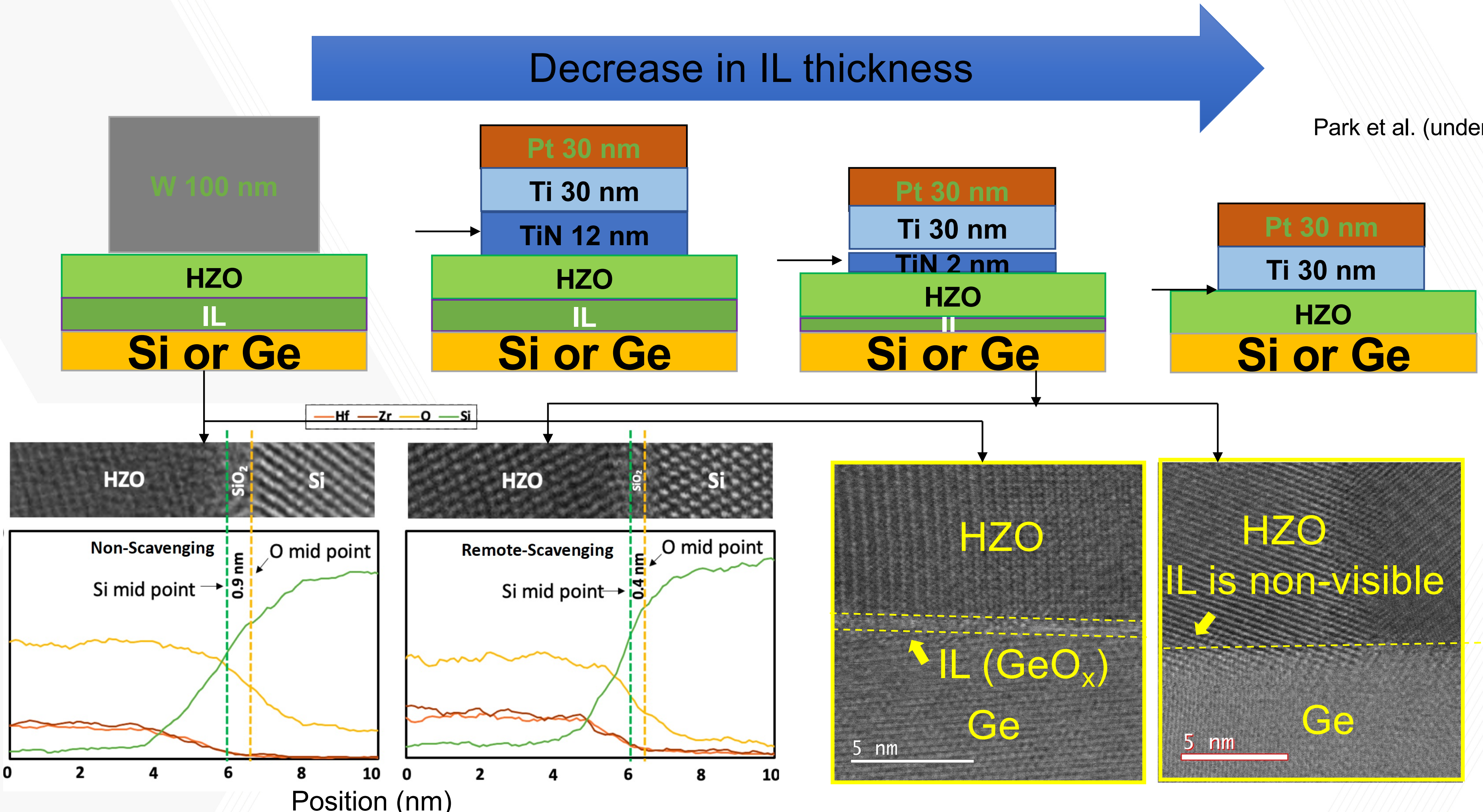
Tasneem et al. “Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium−Zirconium Oxide-Based Metal−Oxide−Semiconductor Structures”, ACS Appl. Mater. Interfaces 2022, 14, 43897–43906

Park et al. (under review)



Remote oxygen scavenging can result in controllable IL thickness.

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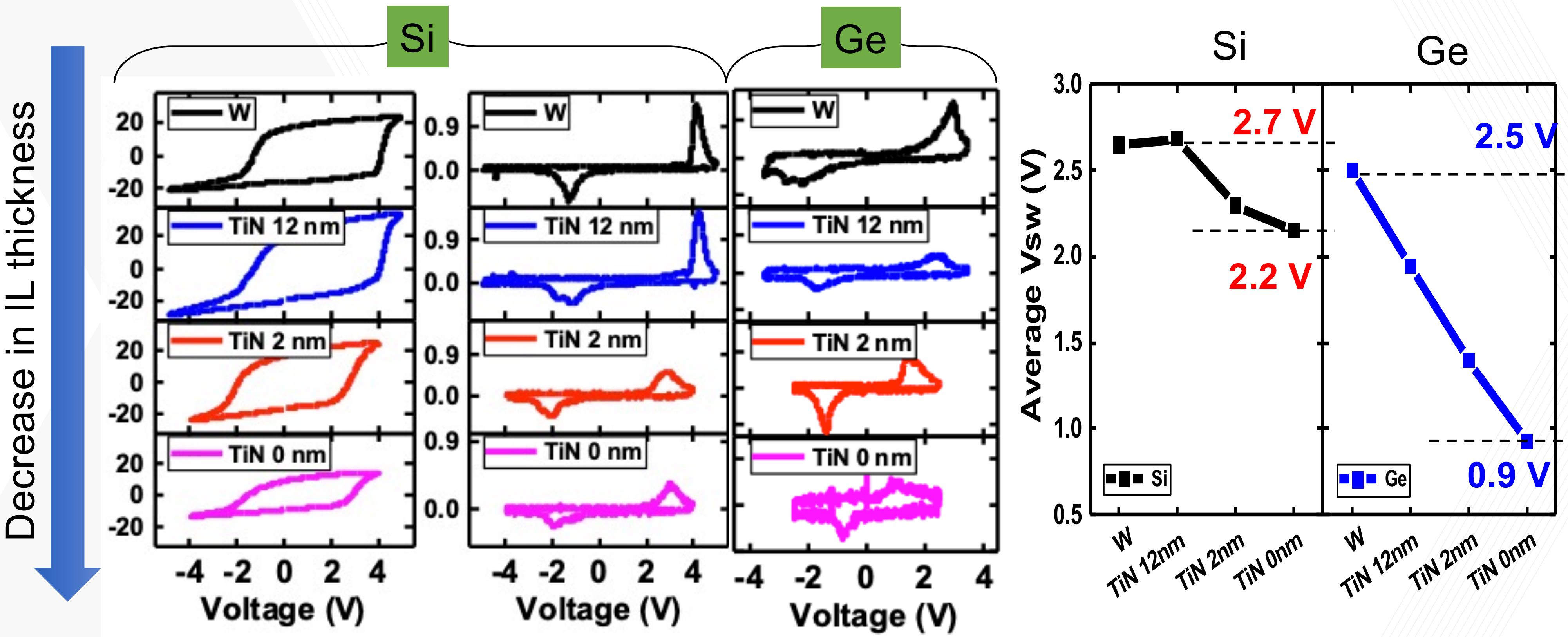
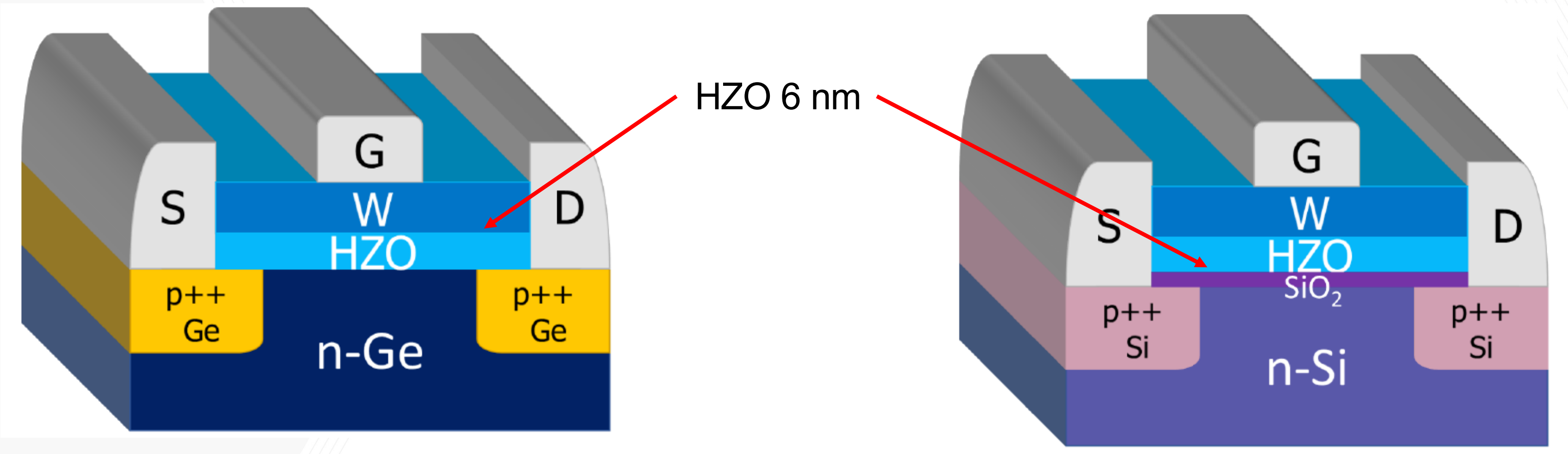
The effect of the IL thickness on Vc



Dramatic reduction in coercive voltage is observed in Ge platform with the change of the gate metal stack.

Ge-channel FEFETs with record-low write voltages



Si and Ge-channel FEFETs fabricated with the same 6 nm HZO layers, under similar process and fabrication conditions.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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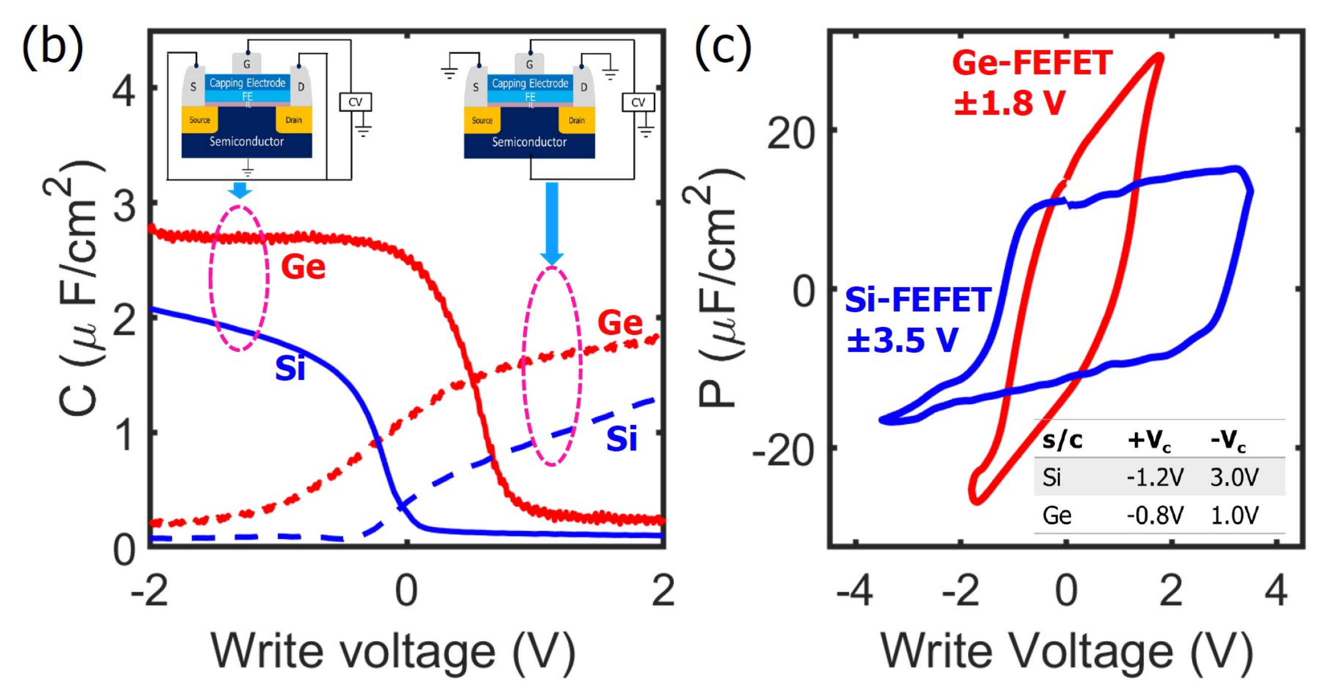
Ge-channel FEFETs with record-low write voltages



s/c	$+V_c$	$-V_c$
Si	-1.2V	3.0V
Ge	-0.8V	1.0V

Significant increase on the on-capacitance and reduction in coercive voltage in Ge-channel FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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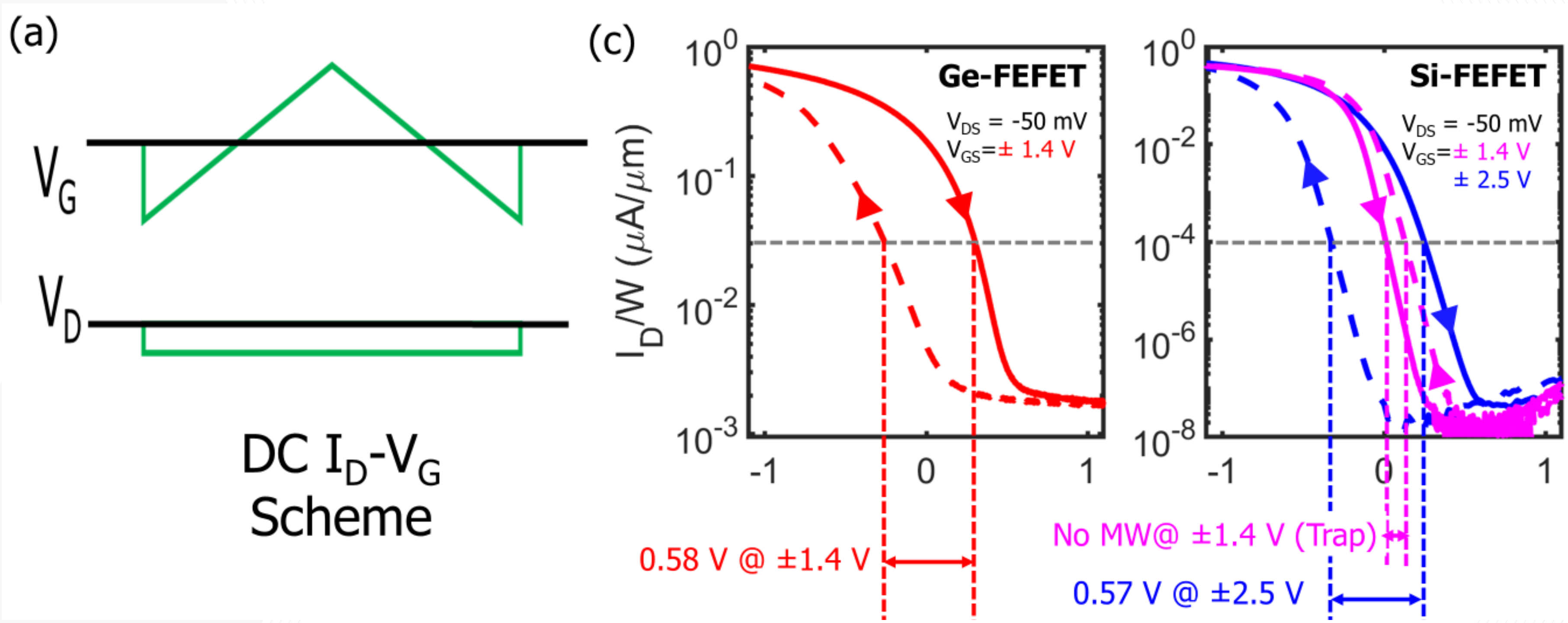
DC I_D-V_G characteristics



Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

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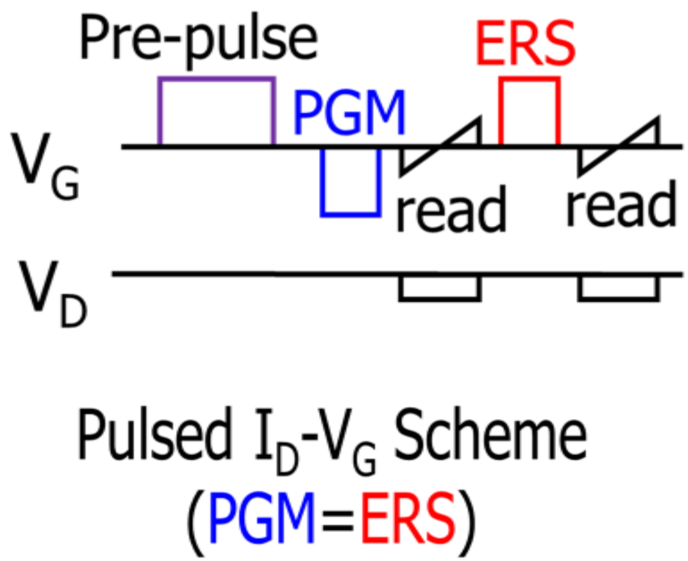
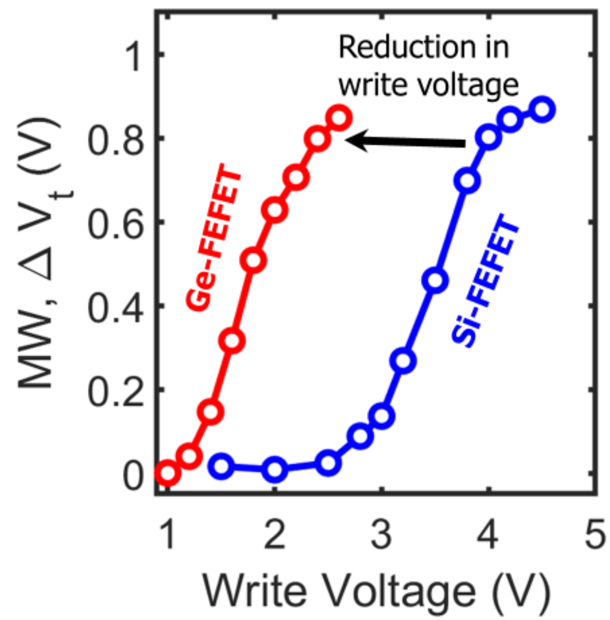
Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Pulsed I_D-V_G characteristics





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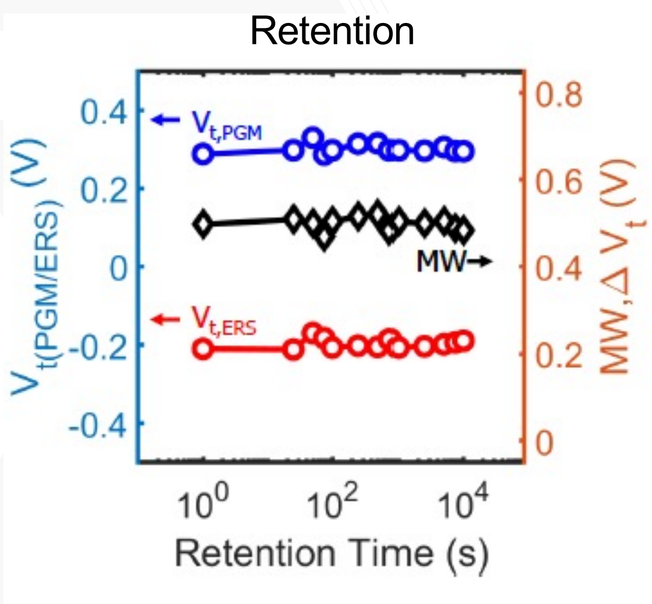
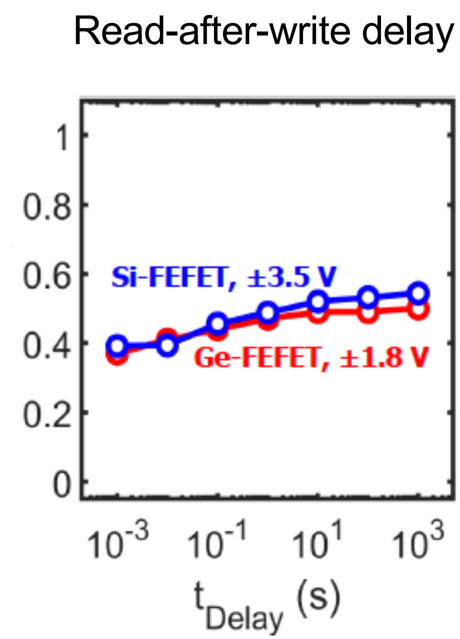
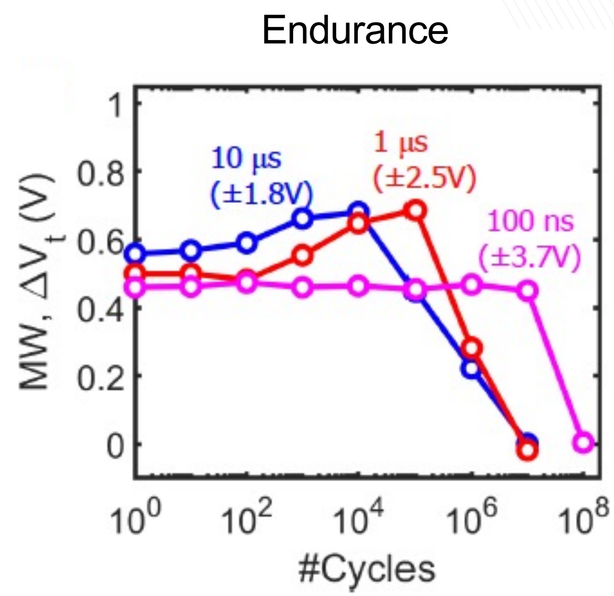
Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Retention, endurance and read-after-write delay



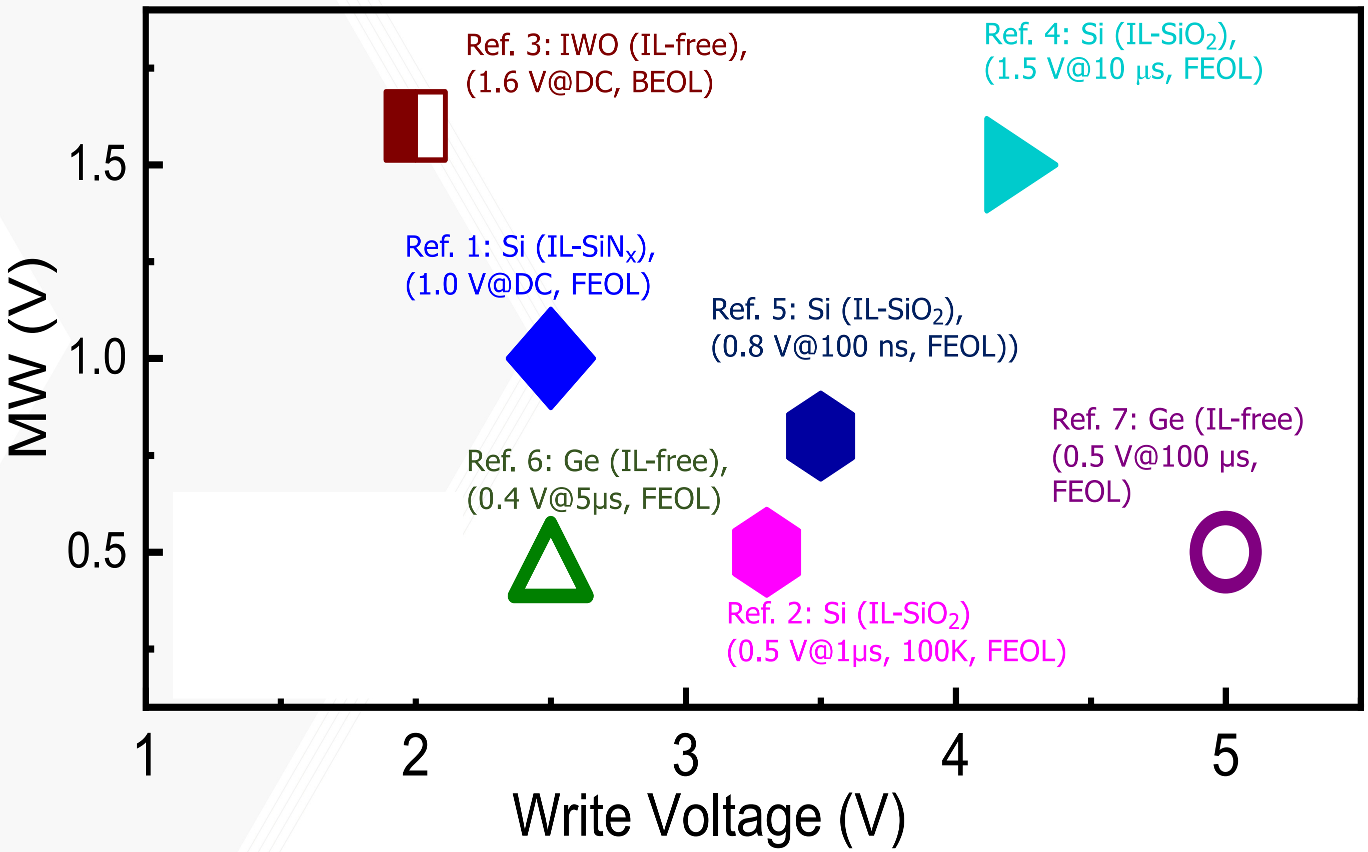




The Ge-FEFET show write endurance of 107 cycles, excellent data retention and immediate read-after-write capability.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Benchmarking Memory Window v. Write Voltage Tradeoff



[1] Tan *et al., IEEE EDL*, 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

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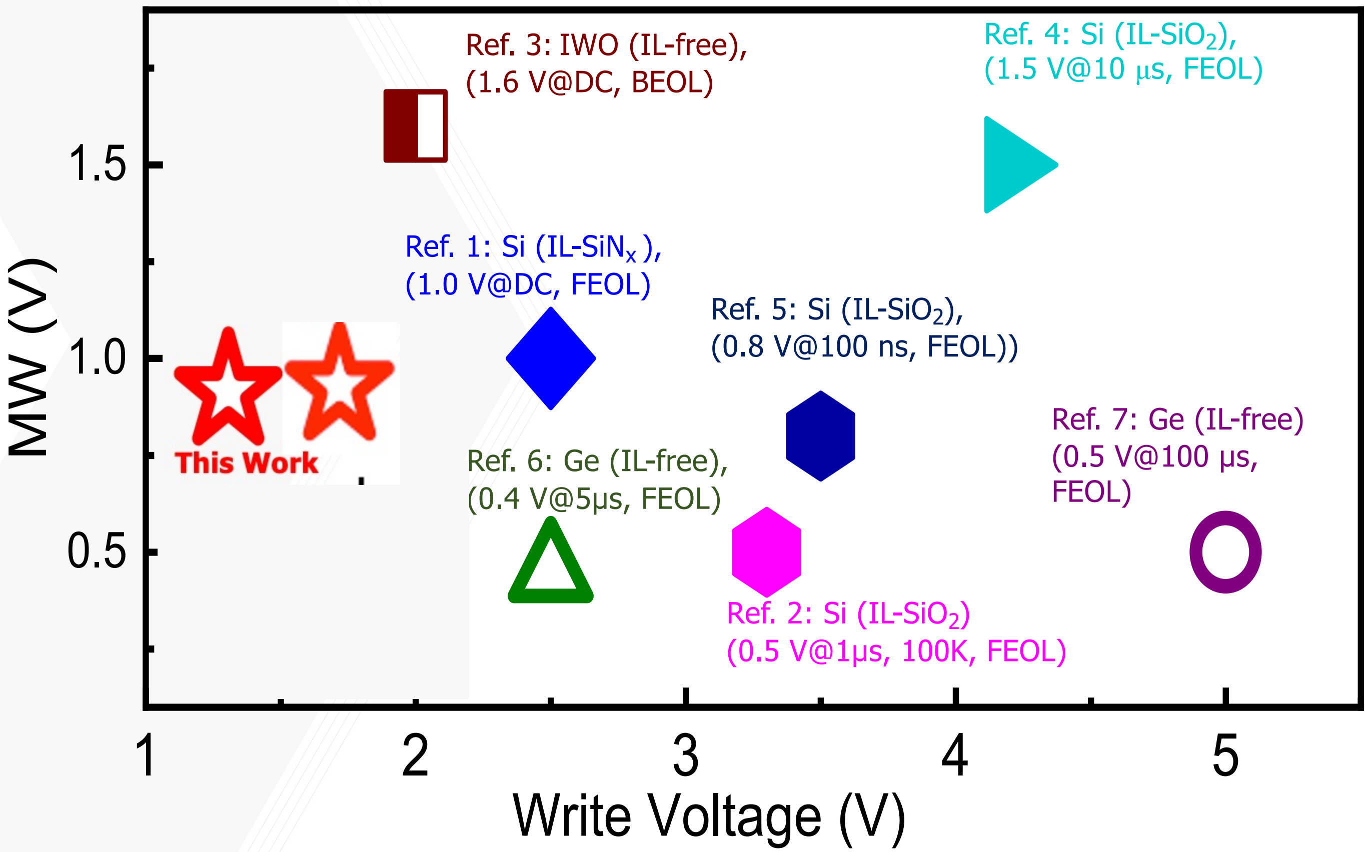
Benchmarking Memory Window v. Write Voltage Tradeoff



Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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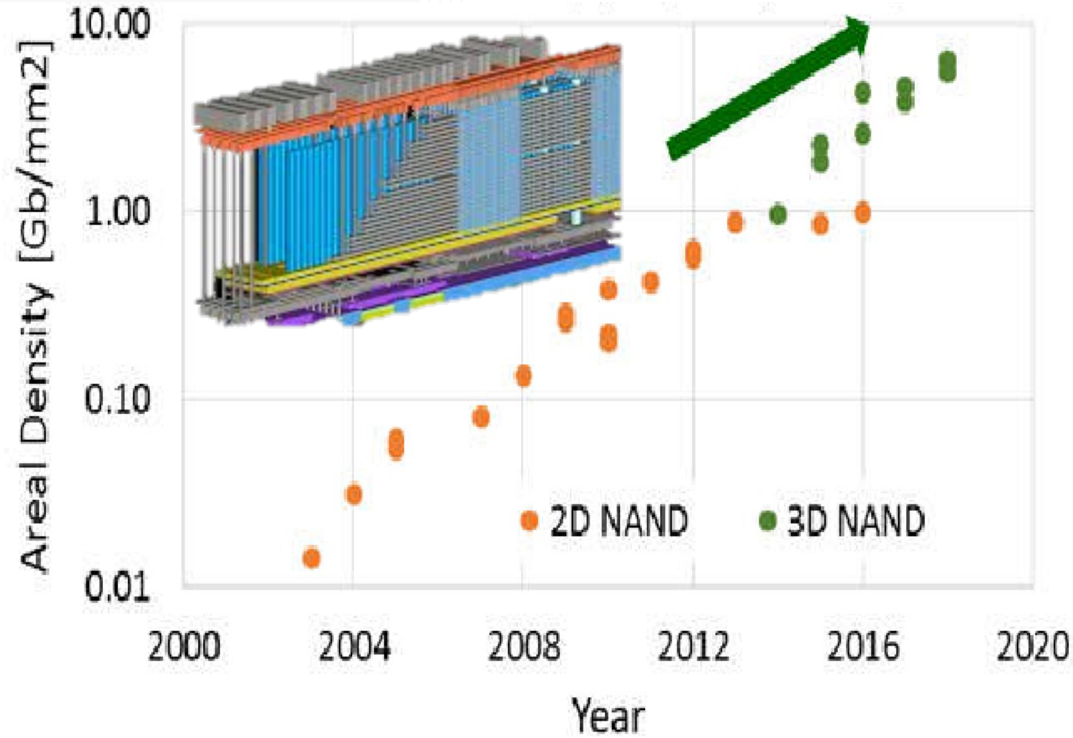
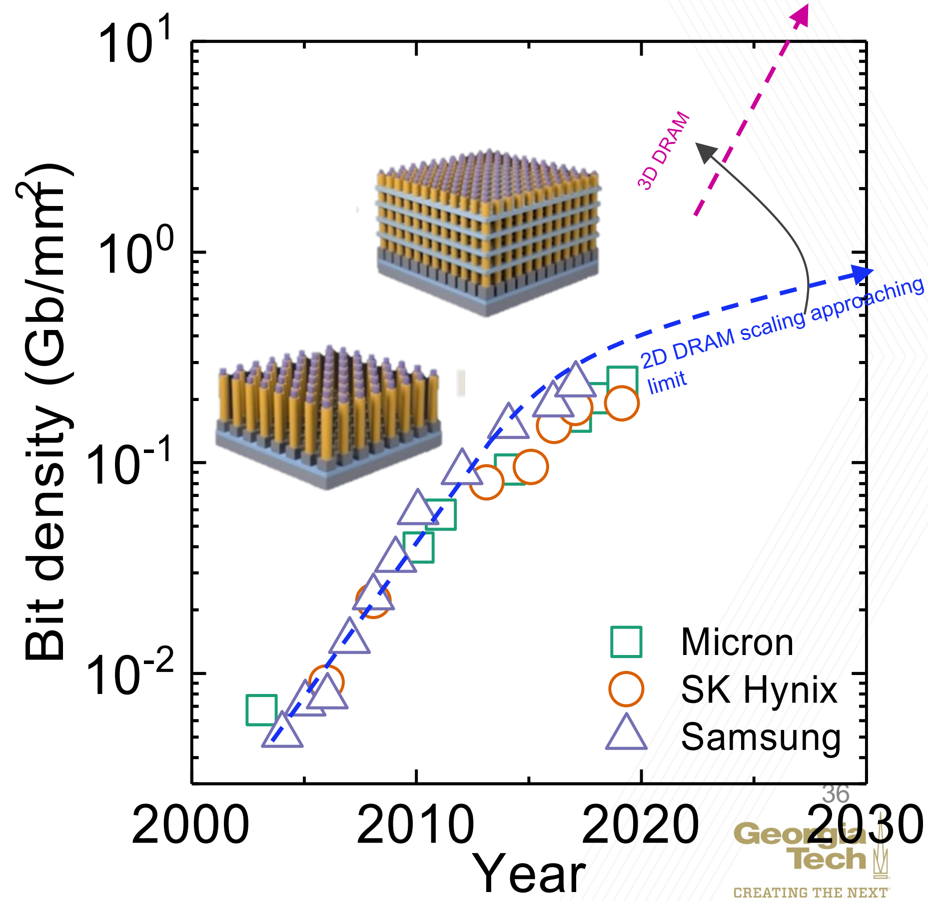
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

Innovation at the core – Memory

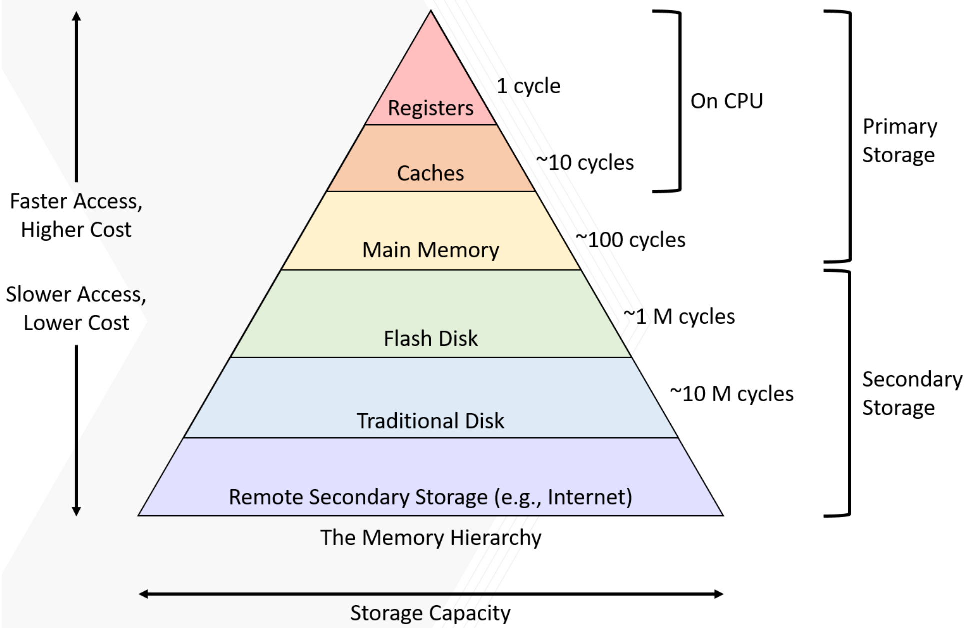
NAND Flash Technology



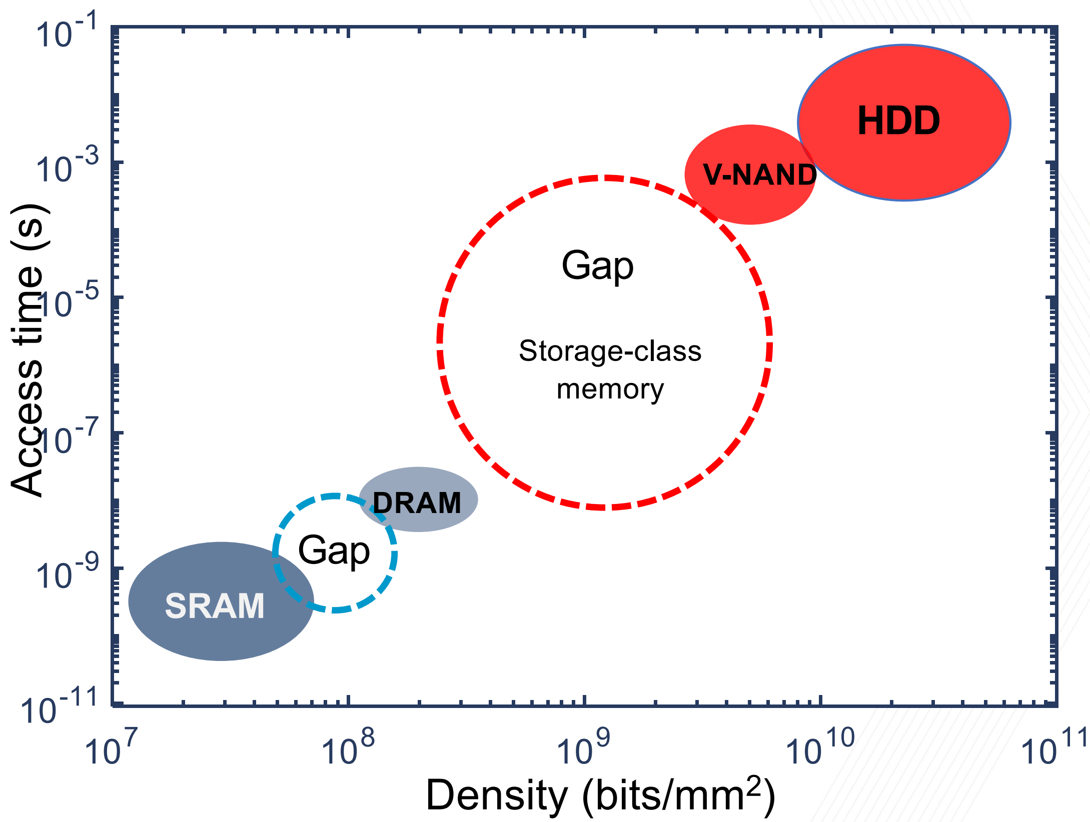
Dynamic Random Access Memories (DRAM)



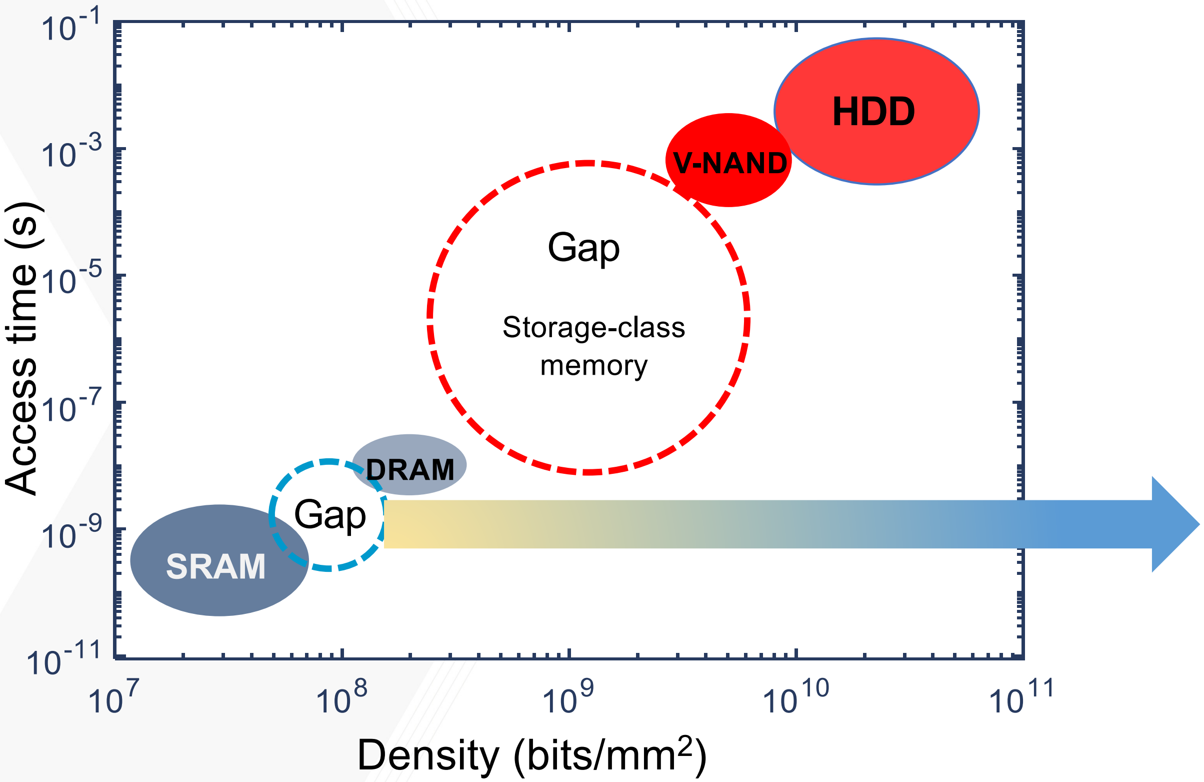
Memory Landscape



The Memory Hierarchy

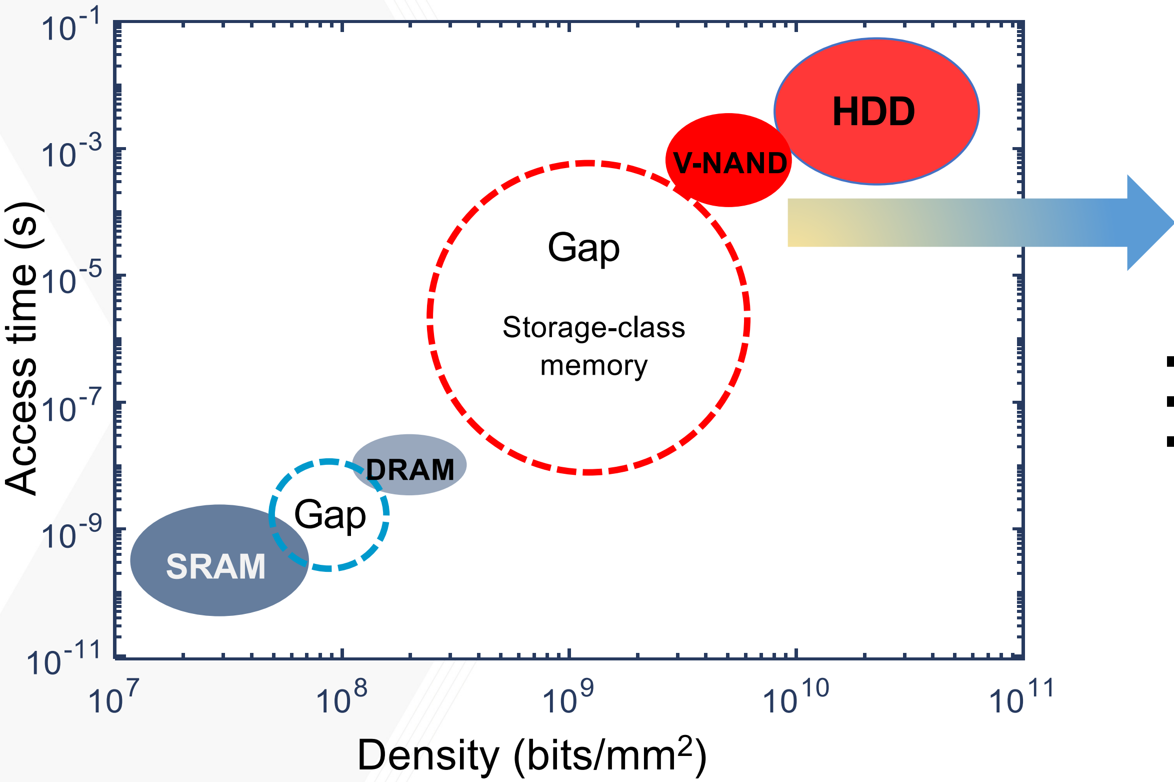


Opportunities for Ferroelectric devices



	Cell area | Speed
DRAM:	6-30F^2 | <10 ns
FEFET:	5-10F^2 | 5-10 ns
SRAM:	140-280F^2 | <1 ns

Opportunities for Ferroelectric devices

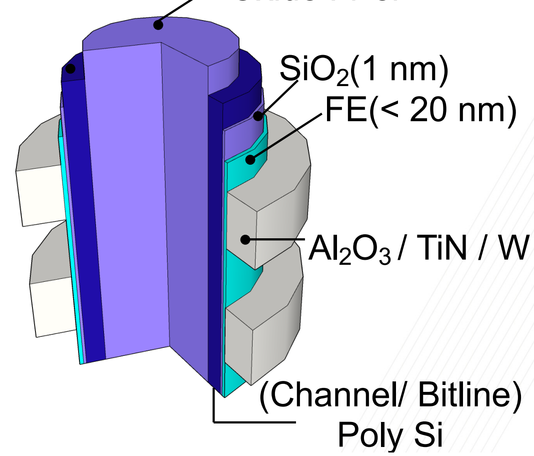


V-NAND FLASH

- Limited scaling (oxide>20 nm)
- High write voltage (~20 V)
- Slow write (1-10 ms)
- Limited endurance (10^3 for MLC)

Ferroelectric V-NAND

- Scalable oxide (<5 nm)
- Smaller write voltage (~10 V)
- Fast write (<1 μs)



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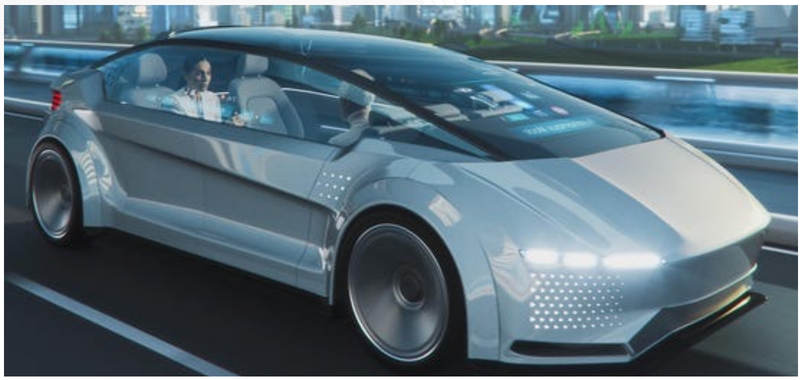
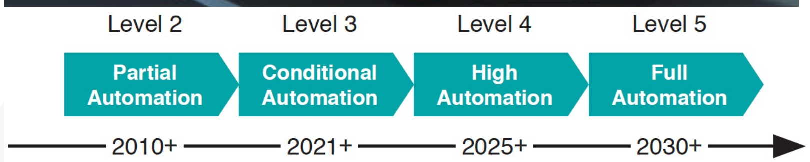
Limits to the possibilities

1

Level 5 autonomous drive



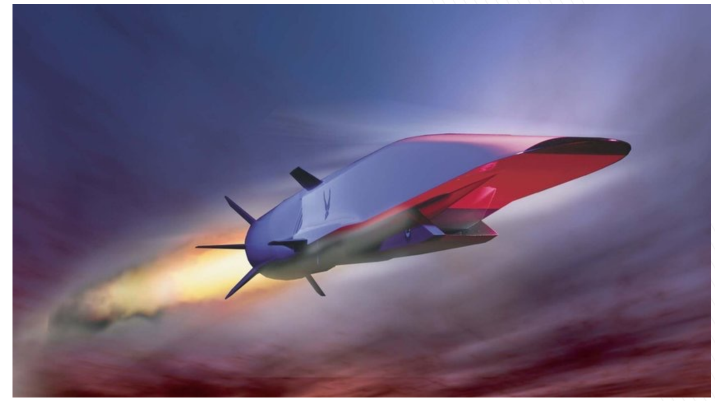


L2 to L5 autonomy will require 10x increase in memory and 100x increase in compute!

Source: SRC Decadal plan

2

Zettascale computing (10^{21} FLOP/s)

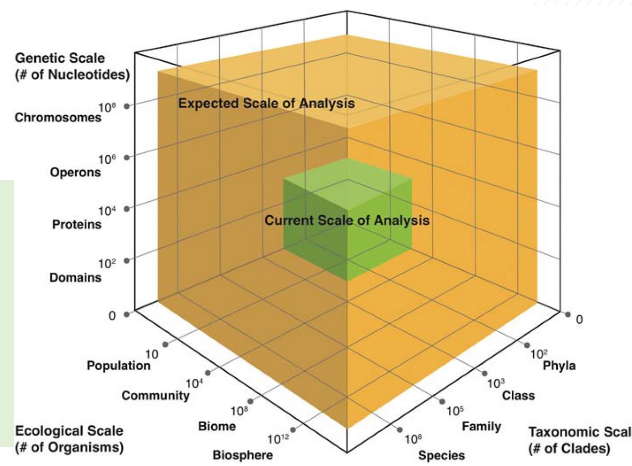


Simulation of a X-51A recoverable hypersonic vehicle over a one-hour flight path is intractable.

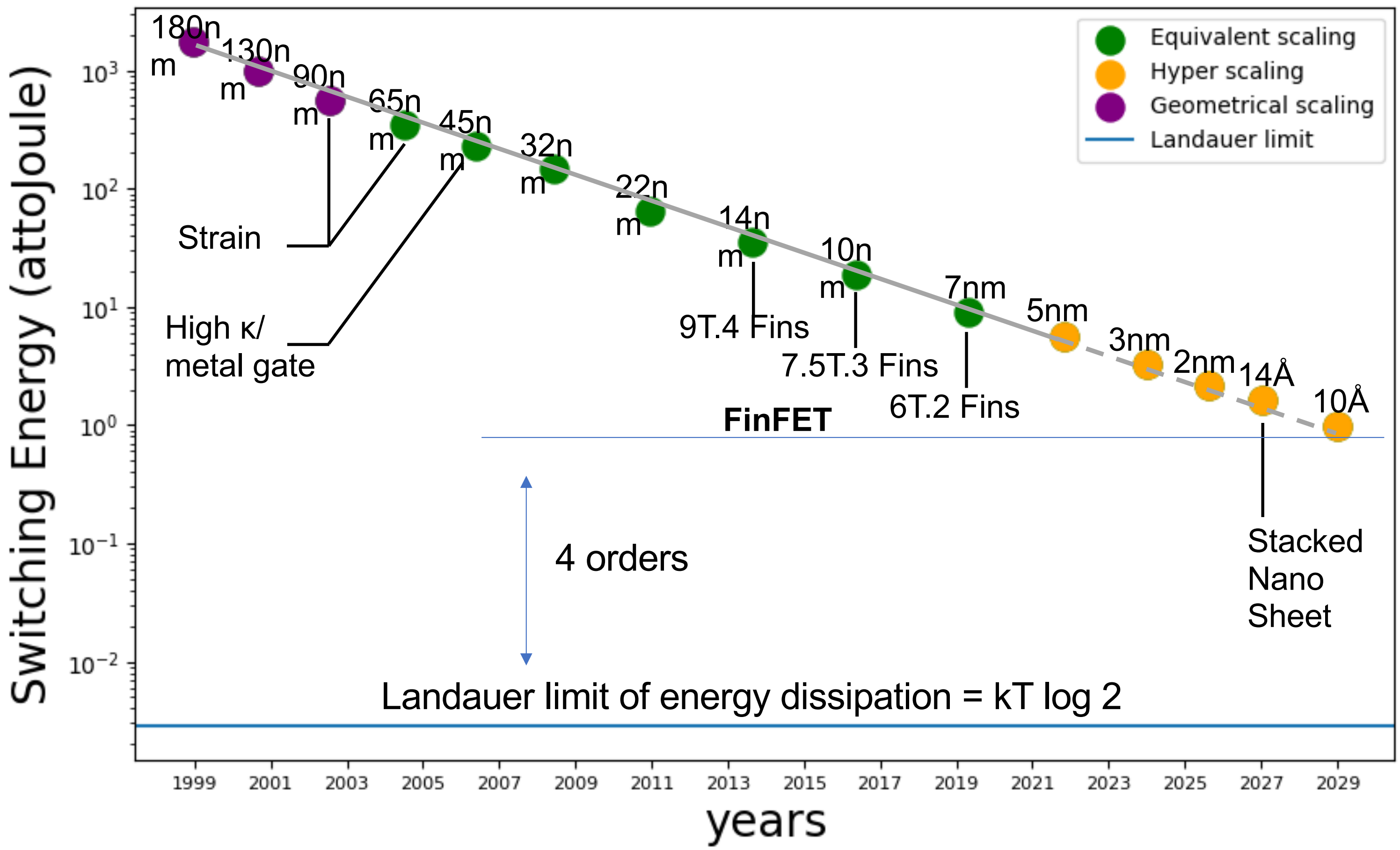
3

Omics data analytics

Advances in sequencing and omics technologies have far outpaced data infrastructure.



Plenty of Room at the Top and Bottom

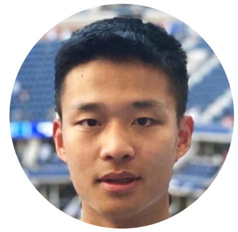


Our team


Prasanna Ravindran


Chinsung Park

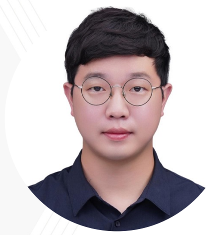

Nashrah Afroze


Jiayi Chen


Priyankka G R


Zekai Wang


Lance Fernandes


Jaewon Shin


Yu Hsin Kuo


Taeyoung Song


Eknath Sarkar


Dr. Dipjyoti Das


Dr. Hang Chen


Dr. Mengkun Tian


Dr. Zheng Wang (Micron)


Dr. Sarah Lombardo (TEL)


Dr. Nujhat Tasneem (Intel)


Anthony Gaskell (TSMC)

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Thank you


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midtown
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