Defects and Trapping Effects in Ferroelectric Field-Effect Transistors

Asif Khan

School of Electrical and Computer Engineering

School of Materials Science and Engineering

Georgia Institute of Technology

akhan40@gatech.edu

MRS Spring Meeting 2023, Tutorial EL21—Research Approaches for Energy Efficient Computing

Monday, April 10, 2023, Moscone West, Level 3, Room 3011

Our team

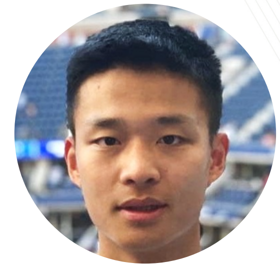
Current

Nujhat Tasneem
Graduate Student

Prasanna Ravindran
Graduate Student

Nashrah Afroze
Graduate Student

Chinsung Park
Graduate Student



Jiayi Chen
Graduate Student

Dr. Hang Chen
Staff member

Priyankka G R
Graduate Student

Henna Mian
Graduate Student

Zekai Wang
Undergraduate student

Dr. Dipjyoti Das
Post-doctoral scholar

Dr. Mengkun Tian
Staff member

Graduated

Dr. Sarah Lombardo
TEL

Dr. Zheng Wang
Micron

Anthony Gaskell
TSMC

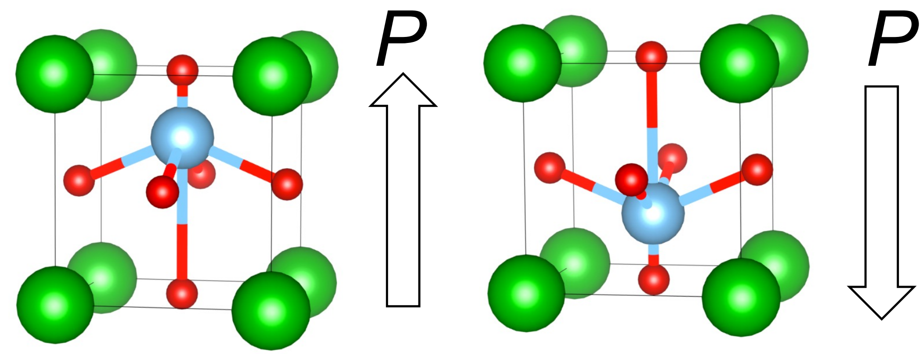
Georgia Tech
CREATING THE NEXT

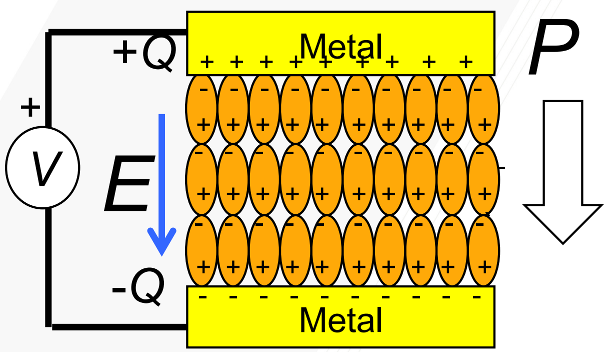

Georgia Tech
midtown
ATLANTA

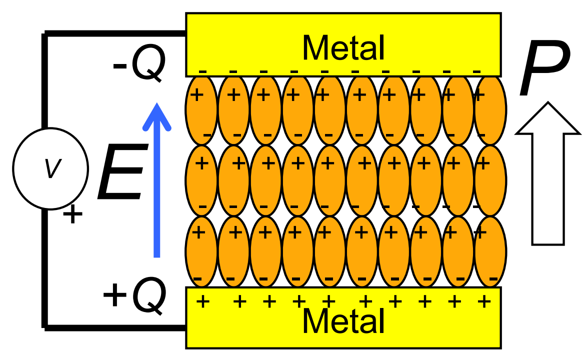
Ferroelectricity

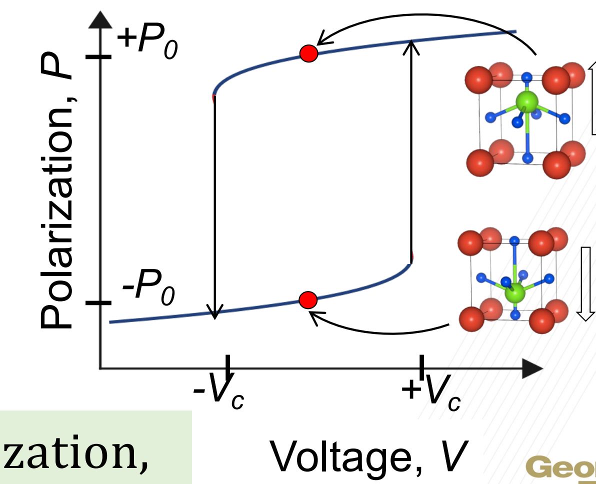
Classical Ferroelectric
$PbTiO_3$, $BaTiO_3$ etc.

Emerging CMOS compatible Ferroelectrics:
Doped HfO_2



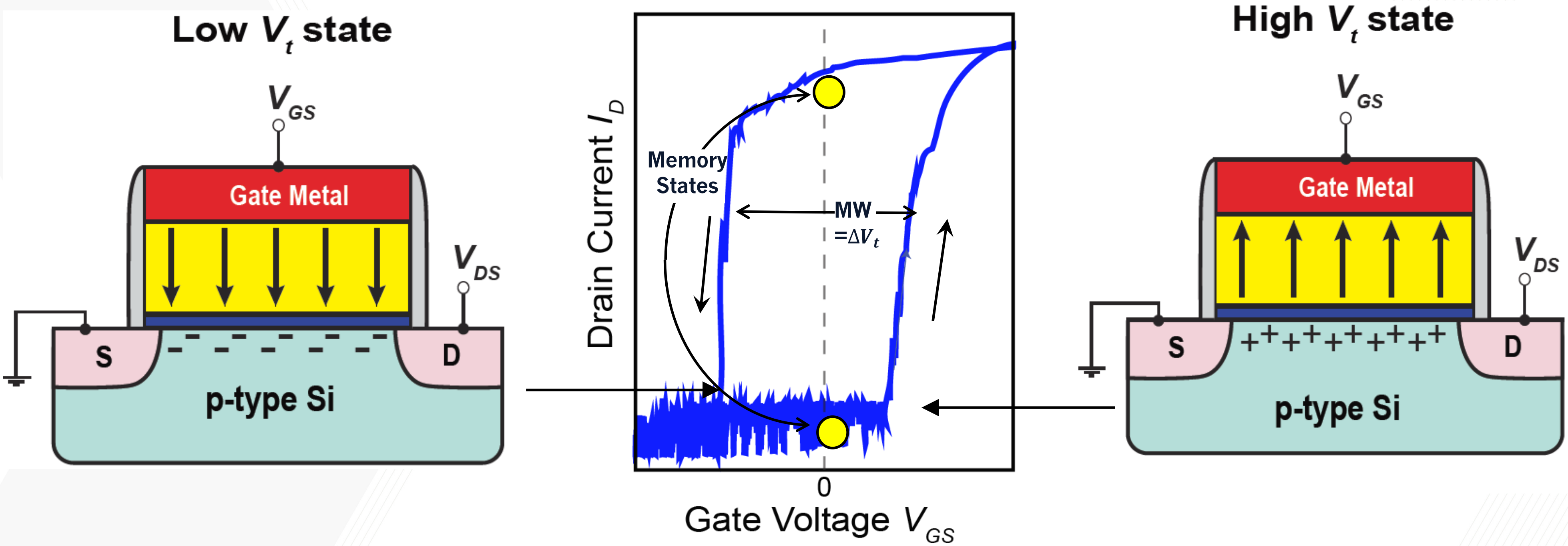






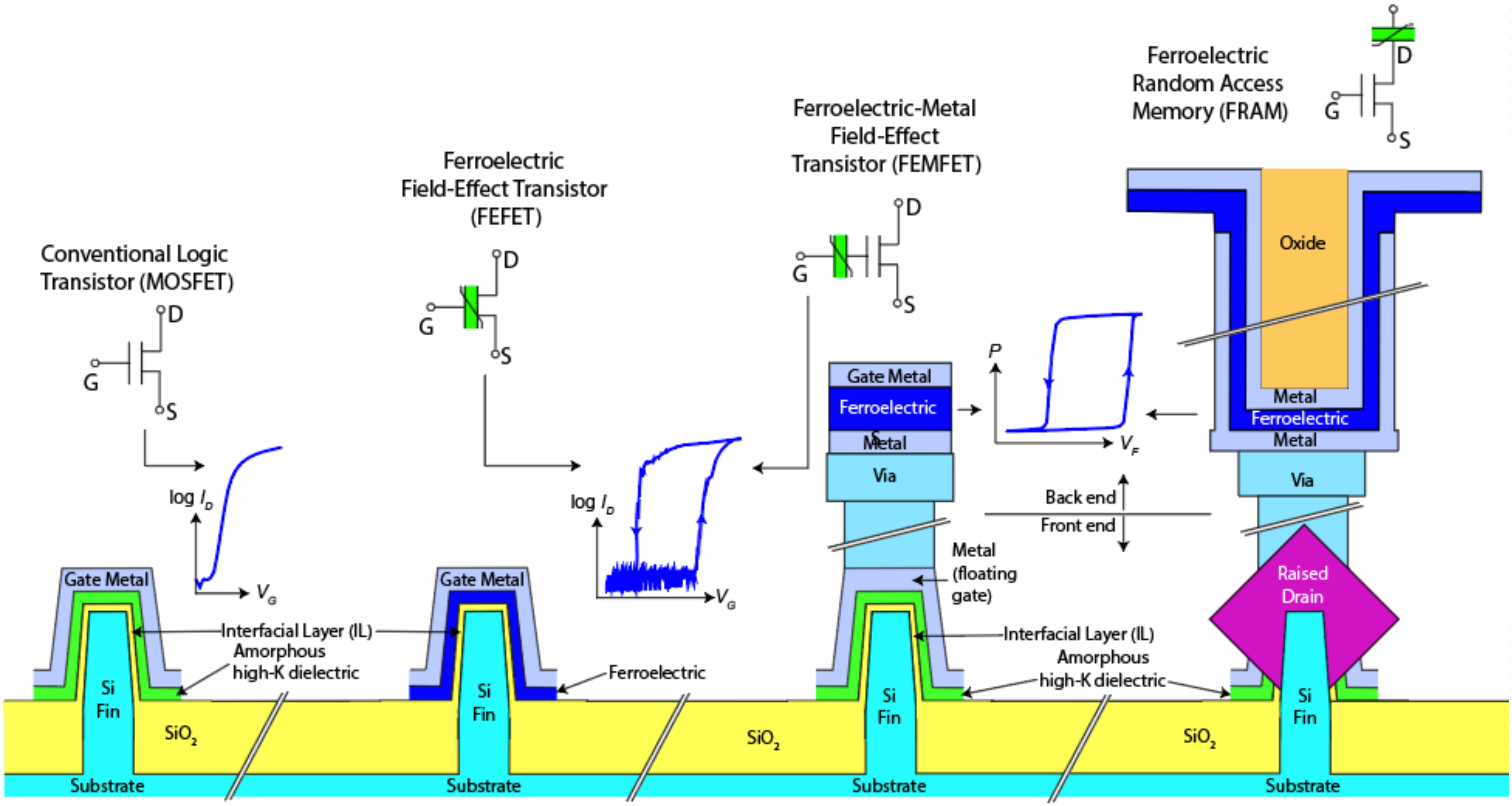
A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET with the threshold voltage shifted by the remnant polarization.

Ferroelectric devices (1 of 2)

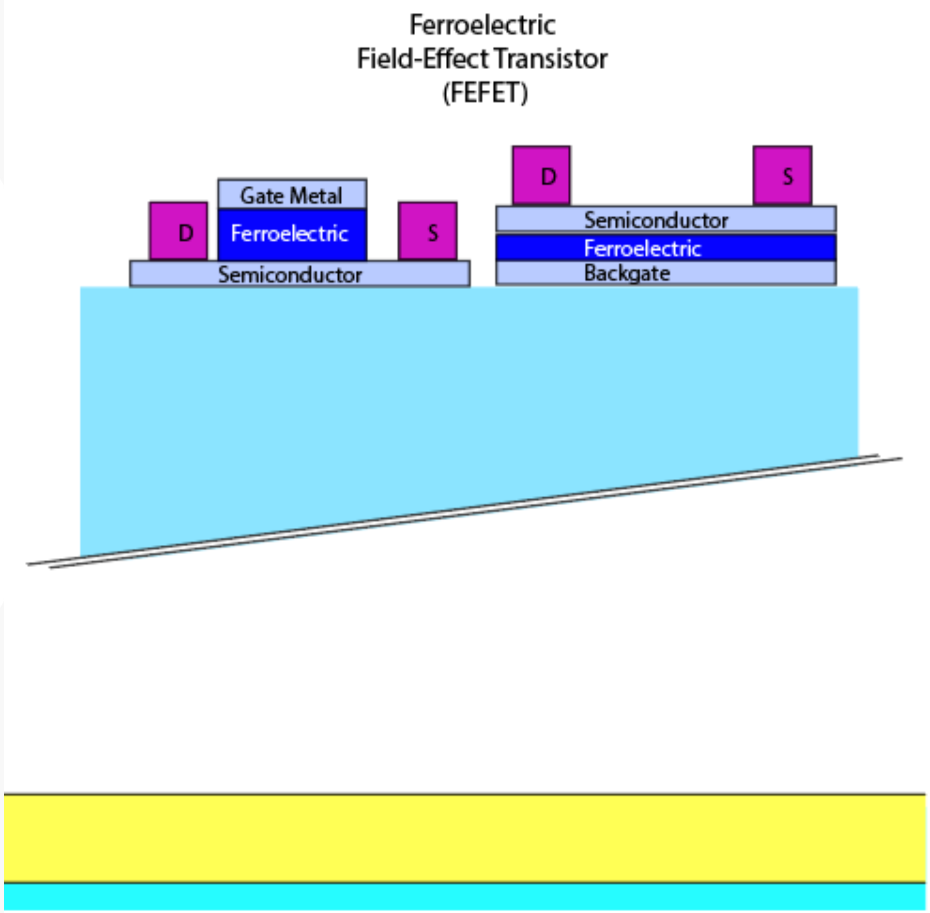


Khan, Keshavarzi, Datta, "The future of ferroelectric field-effect transistor technology", Nature Electronics 2020

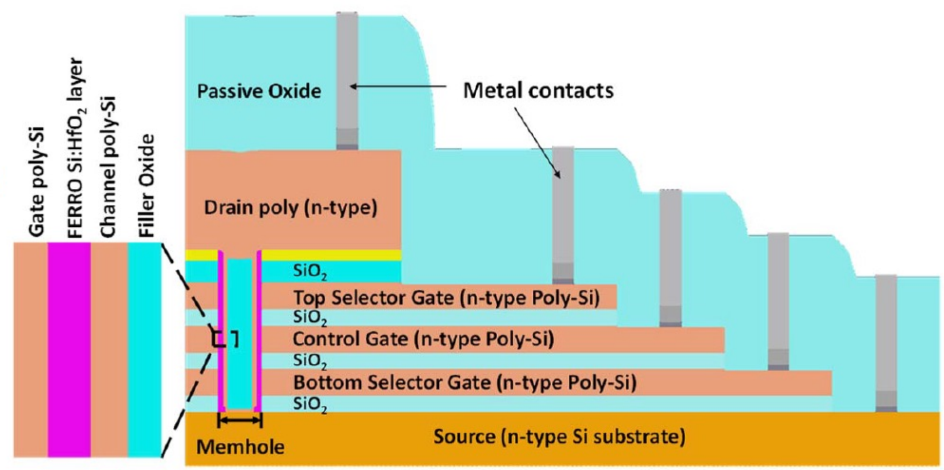
Georgia Tech
CREATING THE NEXT

Ferroelectric devices (2 of 2)

BEOL FEFET



Vertical FEFET for NAND Storage



(b)

Khan, Keshavarzi, Datta, "The future of ferroelectric field-effect transistor technology", Nature Electronics 2020

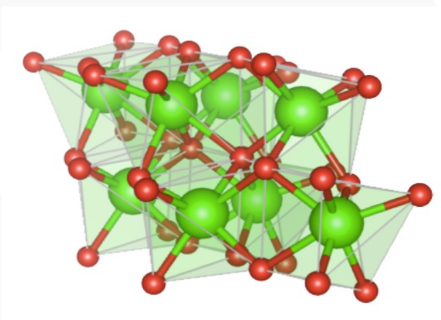
FEFET as an embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	**eDRAM[70]**	**eFlash (FG)**	**eFlash (SG MONOS)[42]**	**eFlash (SONOS)[41]**	**FEFET (hafnia based, MFIS structure)**	**FEFET (hafnia based, MFMIS structure)**	**FRAM (hafnia based)**	**FRAM (perovskite based)[67]**
Cell size	120–150F^2	40F^2	40–60F^2	40–50F^2	50–60F^2	10–30F^2	10–30F^2	30–40F^2	50–60F^2
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 µs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	$>10^{16}$	$>10^{16}$	$\sim10^4$	$\sim10^5$	$\sim10^6$	10^5–10^9	$>10^{10}$	$>10^{12}$	$>10^{14}$

Khan, Keshavarzi, Datta, "The future of ferroelectric field-effect transistor technology", Nature Electronics 2020

Ferroelectric field-effect transistor

Ferroelectric Oxide



Properties of Ferroelectric oxides

- Non-volatility and hysteresis
- Plasticity, Meta-plasticity and Anti-plasticity
- Negative dielectric permittivity/negative capacitance
- Stochasticity

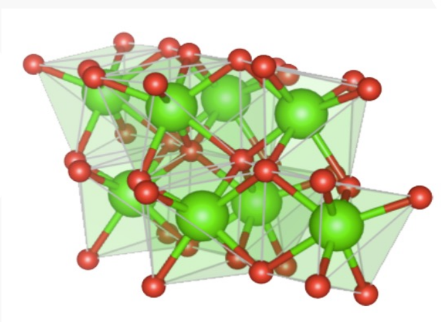
Ferroelectric FET is one of most versatile transistor technologies – ever conceived.

Georgia Tech
CREATING THE NEXT

Khan, Keshavarzi, Datta. “The future of ferroelectric field-effect transistors.” *Nature Electronics* 3, 588 (2020).

Ferroelectric field-effect transistor

Ferroelectric Oxide



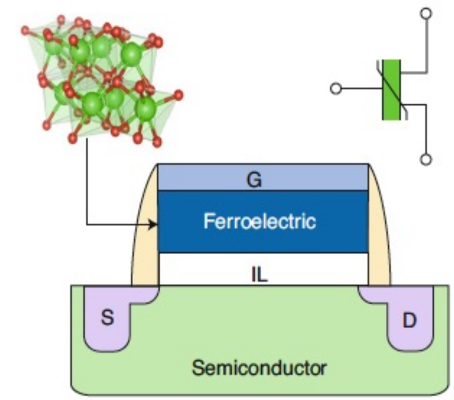
Properties of Ferroelectric oxides

- Non-volatility and hysteresis
- Plasticity, Meta-plasticity and Anti-plasticity
- Negative dielectric permittivity/negative capacitance
- Stochasticity

Properties enabled by a transistor structure

- Transistor physics
- Transconductance gain
- Circuit-level design

Ferroelectric field-effect transistor

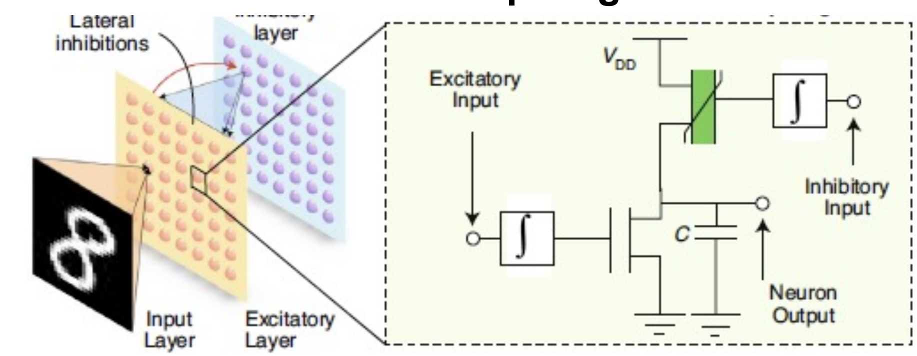


Ferroelectric FET is one of most versatile transistor technologies – ever conceived.

Khan, Keshavarzi, Datta. “The future of ferroelectric field-effect transistors.” *Nature Electronics* 3, 588 (2020).

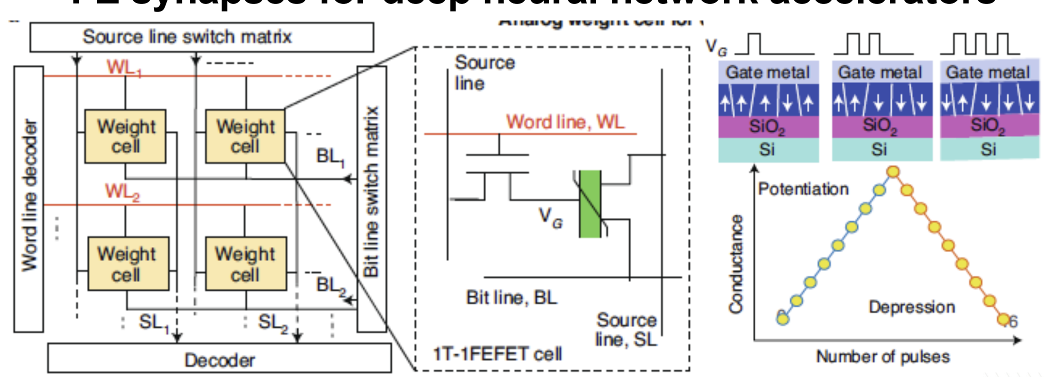
Ferroelectric FET Applications

Ferroelectric neurons for spiking neural networks



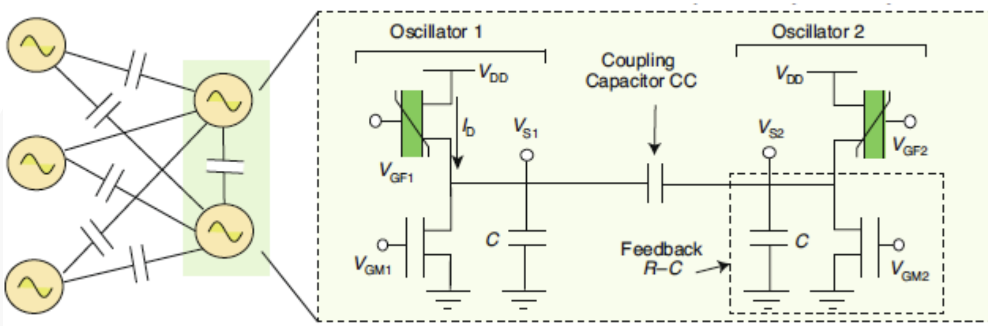
Wang et al. Int. Electron Dev. Meeting (IEDM) 2018.

FE synapses for deep neural network accelerators



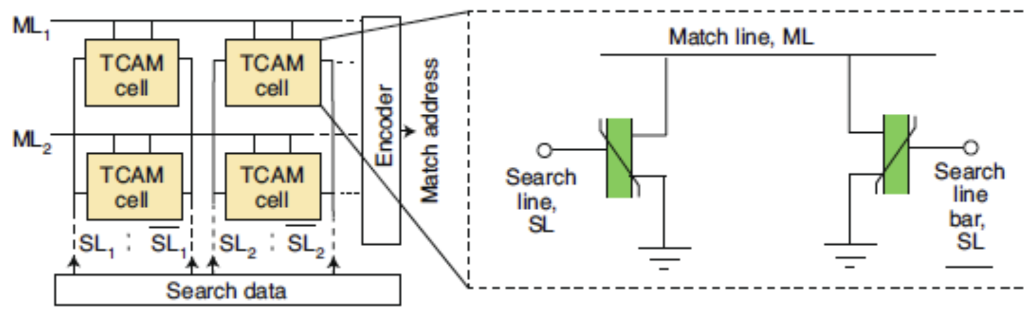
Aabrar et al. VLSI Symp. 2022.

Ferroelectric oscillators for time dynamical systems



Z. Wang et al. EDL 2017

Ferroelectric content addressable memory (CAM)

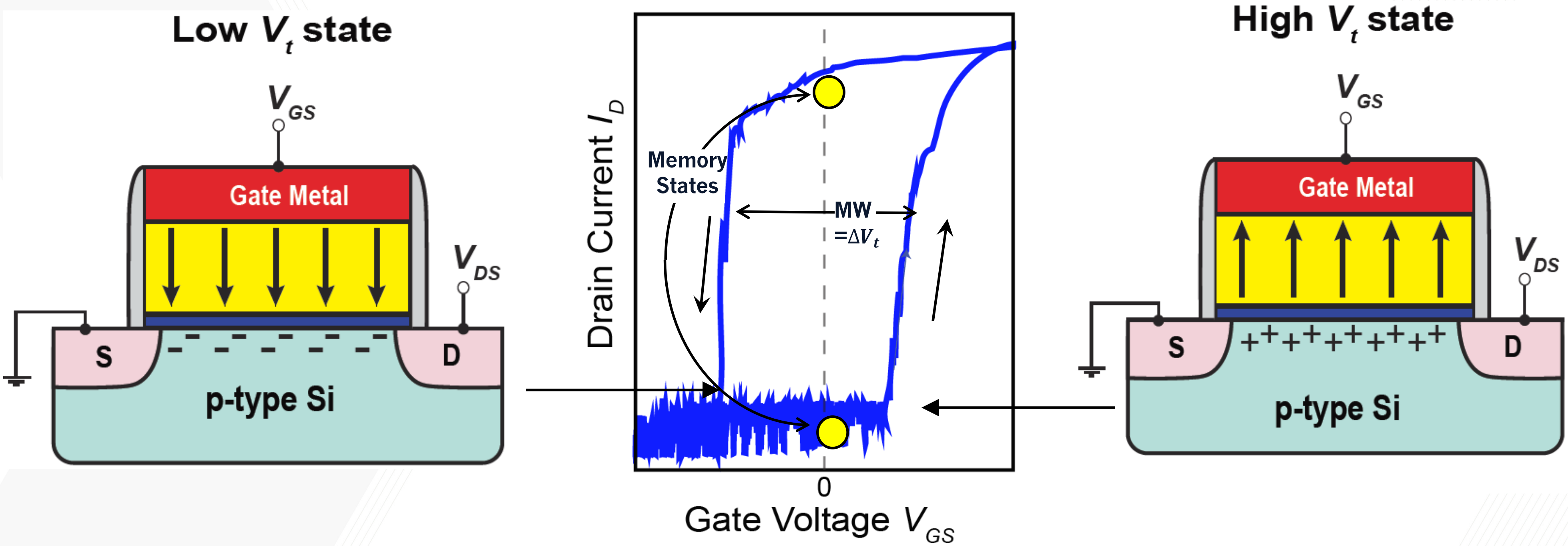


Take-away #1

Ferroelectric Field-Effect Transistors are versatile!

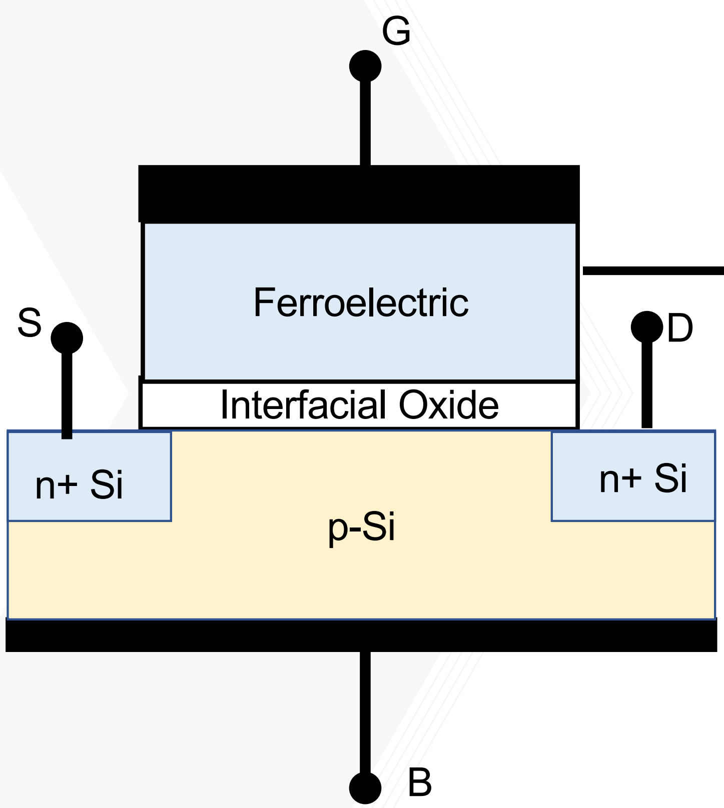
Georgia Tech
CREATING THE NEXT

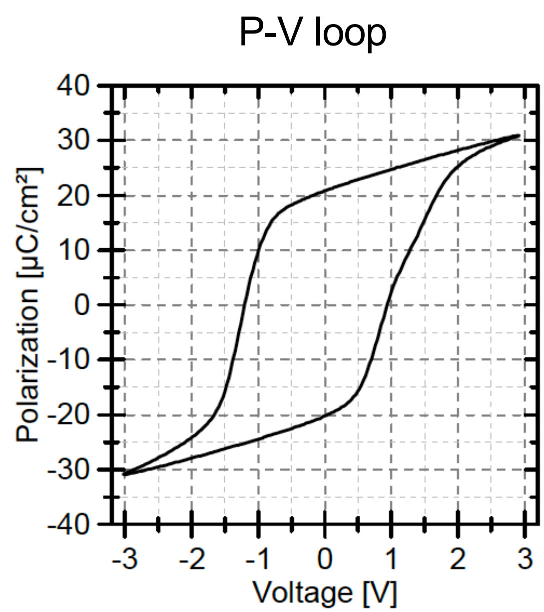
Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET with the threshold voltage shifted by the remnant polarization.

How does electrostatics work out in FEFETs?

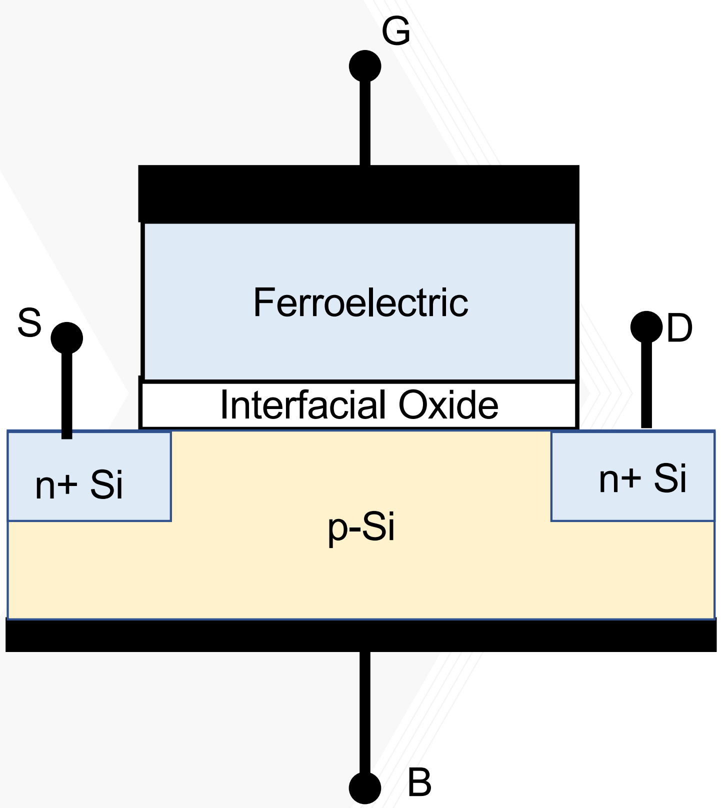




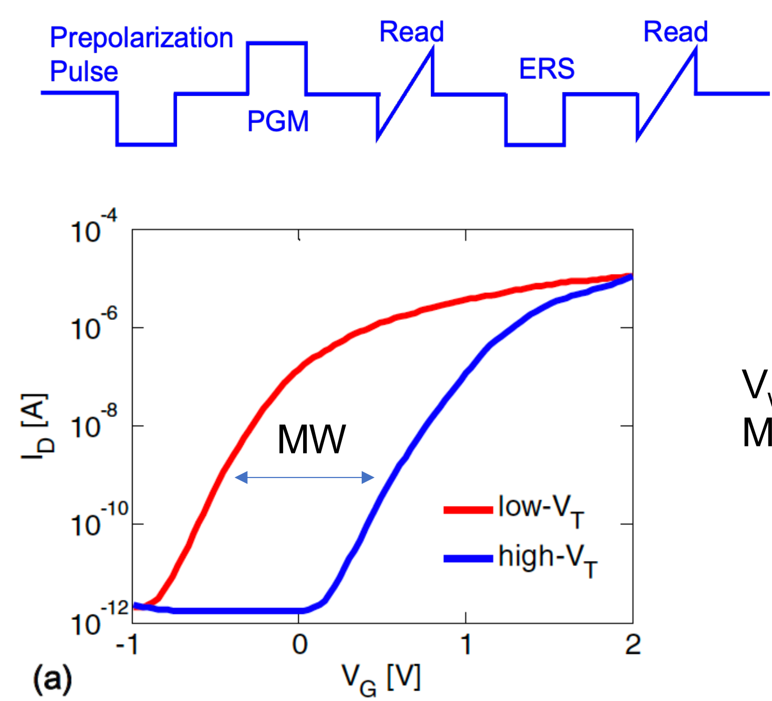
P_r=20 μC/cm^2
V_{max}=2 V

Trentzsch et al. IEDM 2016

How does electrostatics work out in FEFETs?



Memory Window

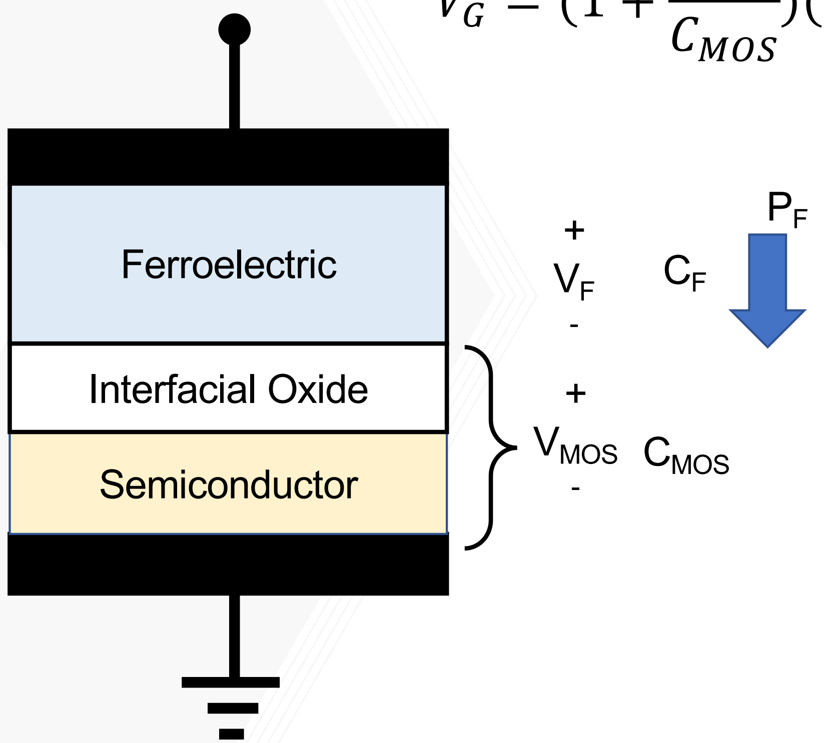


$V_{write}=\pm 4$ V
MW=~1 V

Trentzsch et al. IEDM 2016

How does electrostatics work out in FEFETs?

$$V_G = \left(1 + \frac{C_f}{C_{MOS}}\right)\left(V_f + \frac{P_f}{C_f + C_{MOS}}\right)$$



$$V_F = \frac{C_{MOS}}{C_f + C_{MOS}} V_G + \frac{P_f}{C_f + C_{MOS}}$$

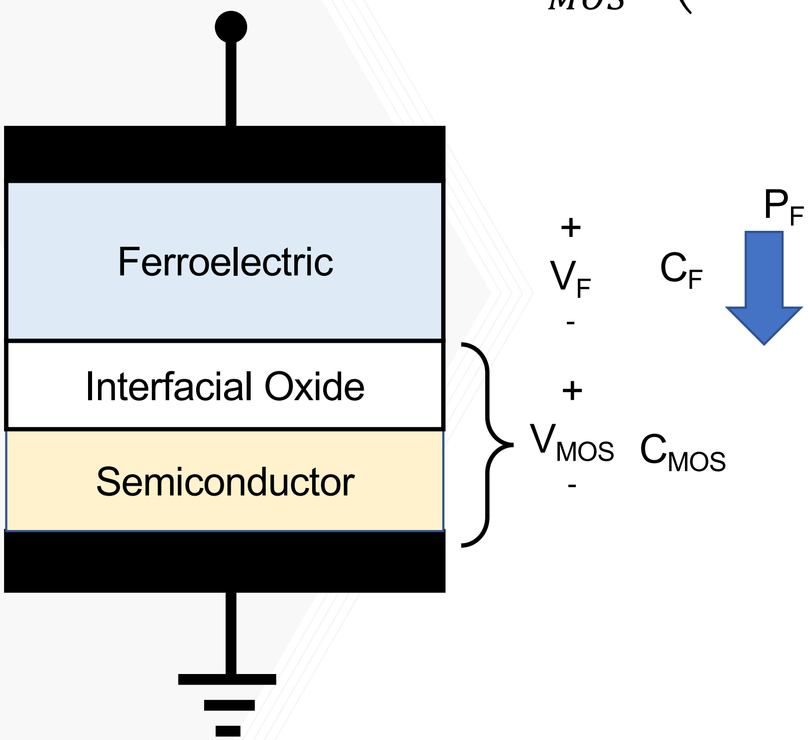
$$V_D = \frac{C_F}{C_F + C_{MOS}} V_G + \frac{-P_f}{C_f + C_{MOS}}$$

Standard Electrostatics

Contribution from Polarization

How does electrostatics work out in FEFETs?

$$V_G = \left(1 + \frac{C_f}{C_{MOS}}\right)\left(V_f + \frac{P_f}{C_f + C_{MOS}}\right) = \left(1 + \frac{4.2}{2.95}\right)\left(2 + \frac{20}{4.2 + 2.95}\right) = 12\ V$$



ε_F=24
t_F=5 nm
P_r=20 μC/cm^2
V_f=2 V

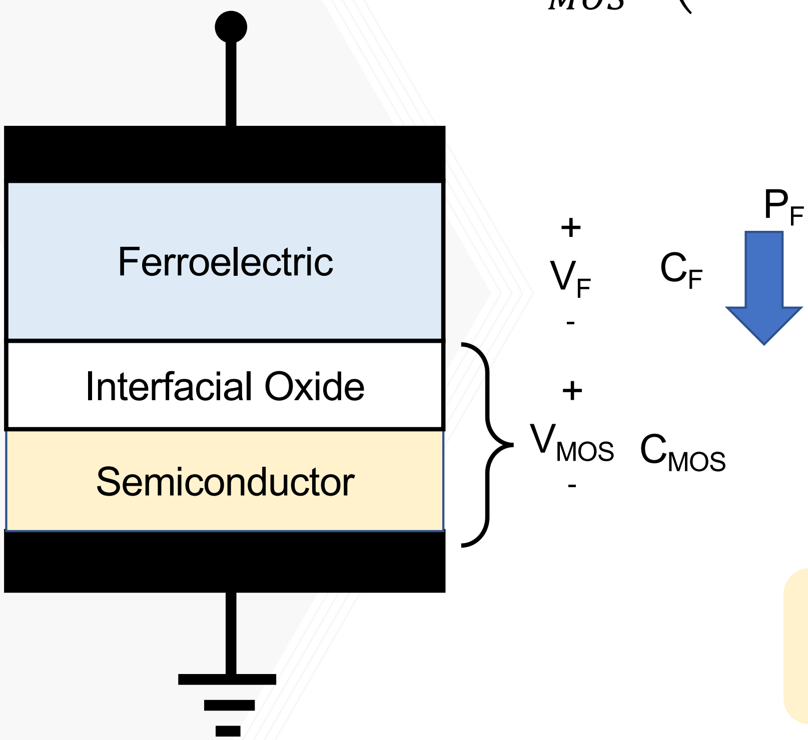
$EOT = \frac{4\times5}{24}$=0.83 nm
C_F=4.2 μF/cm^2

CET=1.2 nm
C_{MOS}=2.95 μF/cm^2

A standard FEFET will need 12 V to switch!

How does electrostatics work out in FEFETs?

$$V_G = \left(1+\frac{C_f}{C_{MOS}}\right)\left(V_f+\frac{P_f}{C_f+C_{MOS}}\right) = \left(1+\frac{4.2}{2.95}\right)\left(2+\frac{20}{4.2+2.95}\right) = 12\ V$$



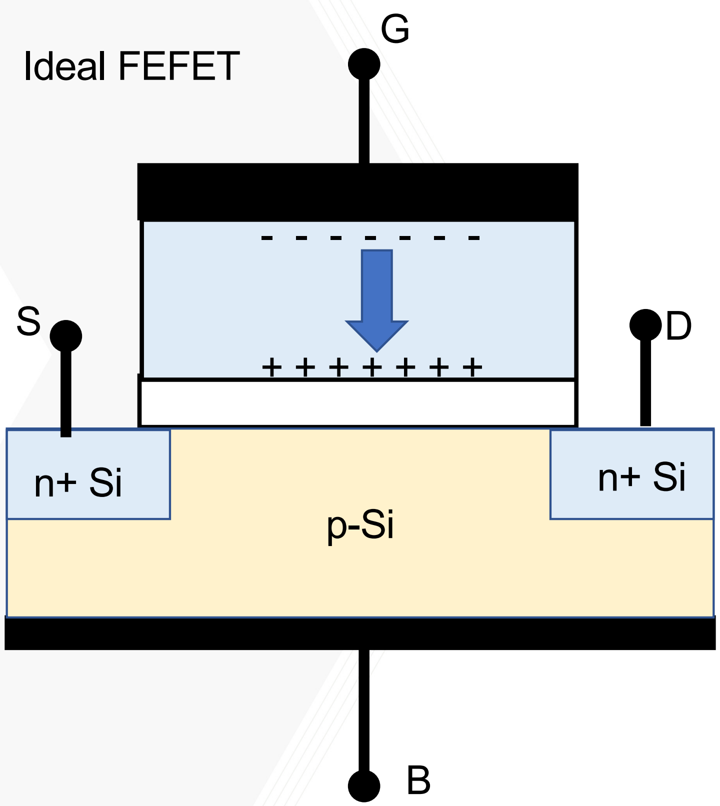
$$V_{MOS} = \frac{P_f}{C_{MOS}+C_F} + \frac{C_f}{C_{MOS}+C_F} V_G$$
$$= \left(\frac{20}{4.2+2.95} + \frac{4.2}{4.2+2.95} V_G\right) = 10\ \text{V}$$

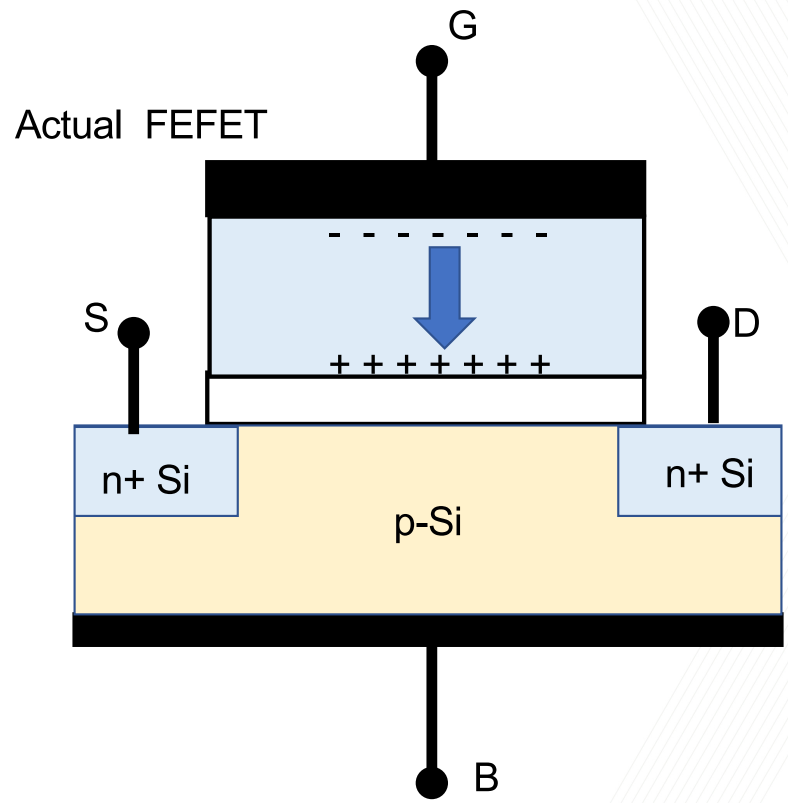
$$E_{ox} = \frac{1}{t_f}\left(\frac{P_f}{C_{MOS}+C_F} + \frac{C_f}{C_{MOS}+C_F} V_G\right) = 20\ \text{MV/cm}$$

The electric field across the interfacial oxide layer will be ~20 MV/cm.

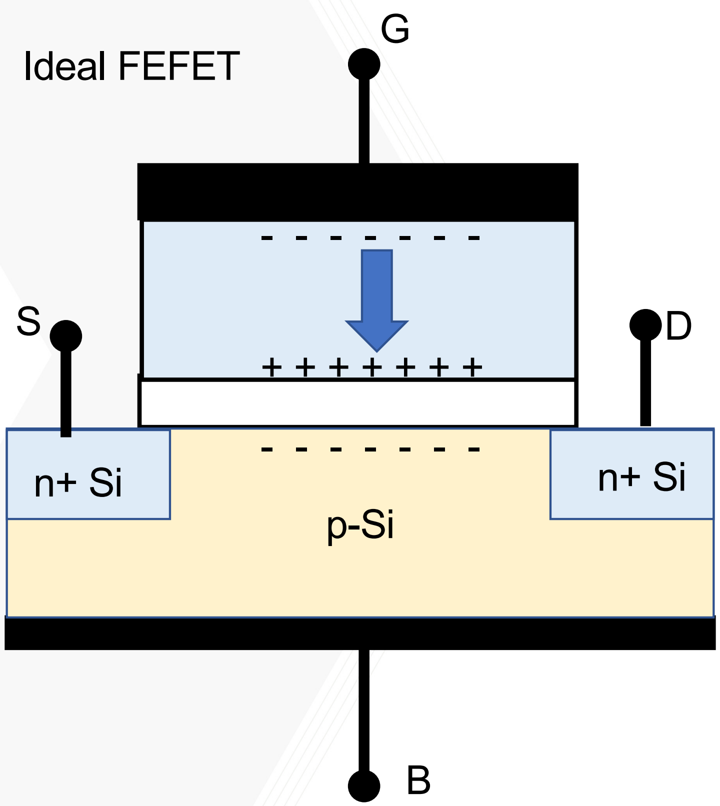
Georgia Tech
CREATING THE NEXT

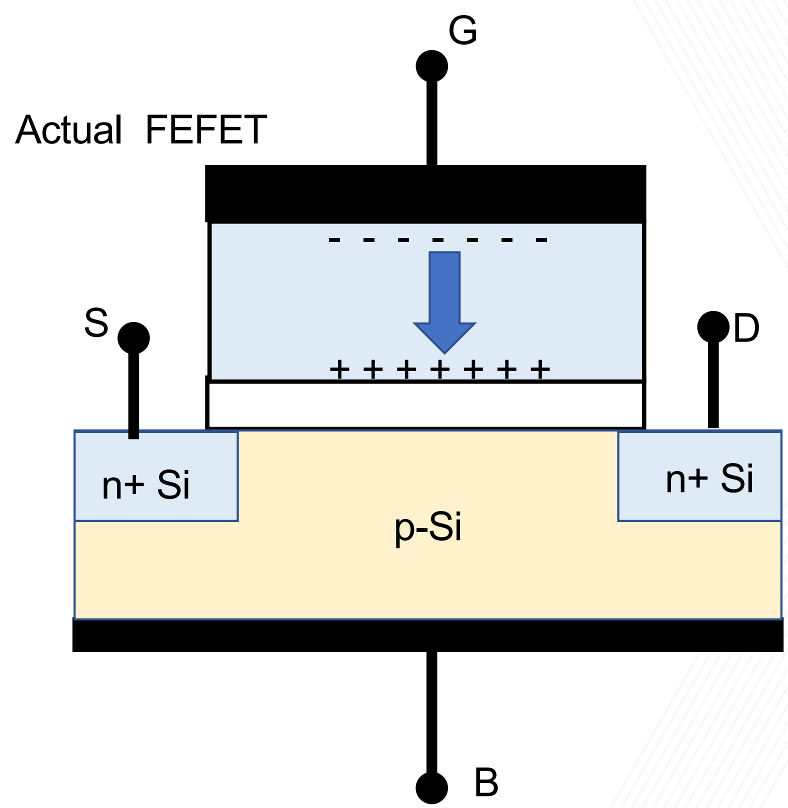
How does electrostatics work out in FEFETs?





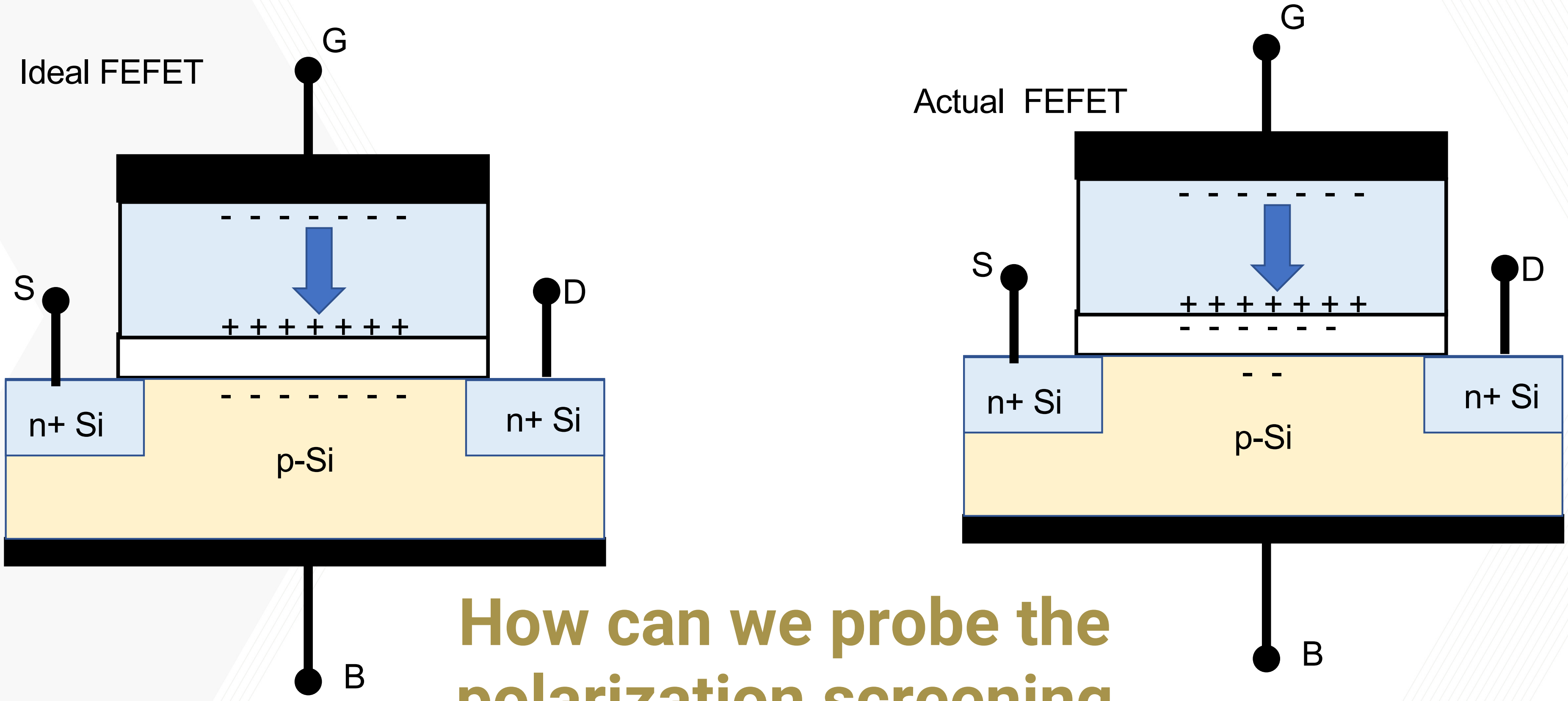
How does electrostatics work out in FEFETs?





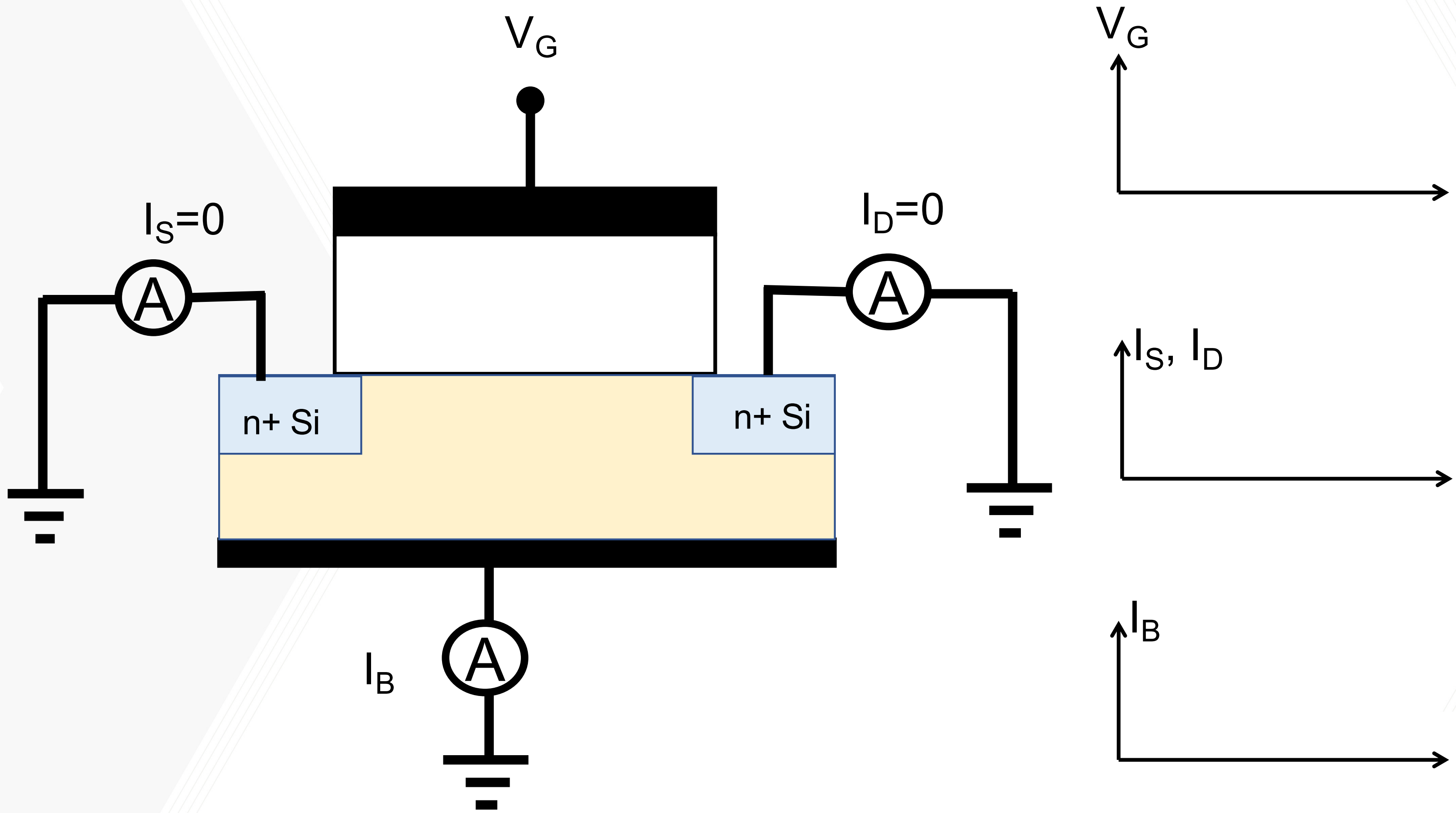
Georgia Tech
CREATING THE NEXT

How does electrostatics work out in FEFETs?

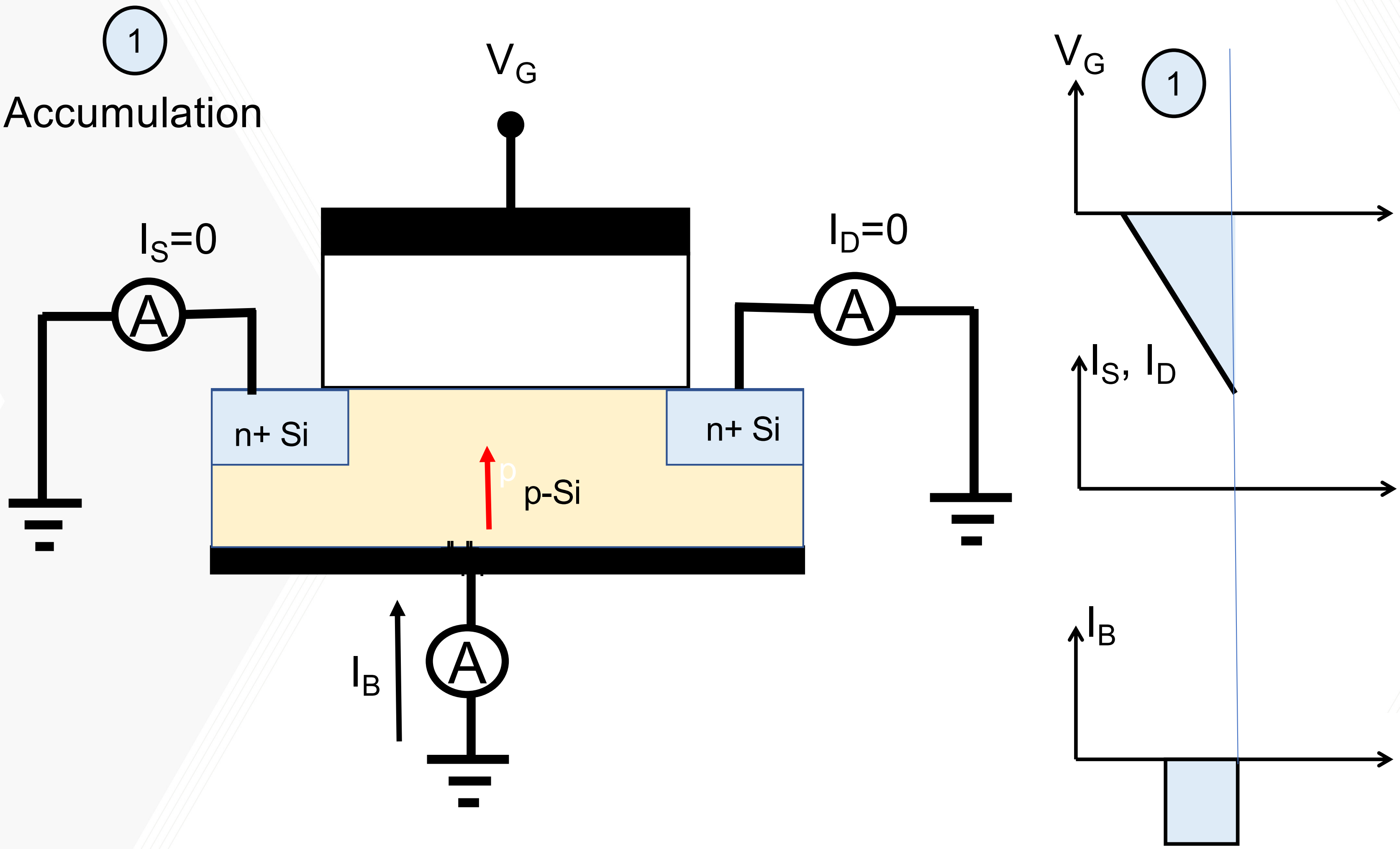


How can we probe the polarization screening dynamics?

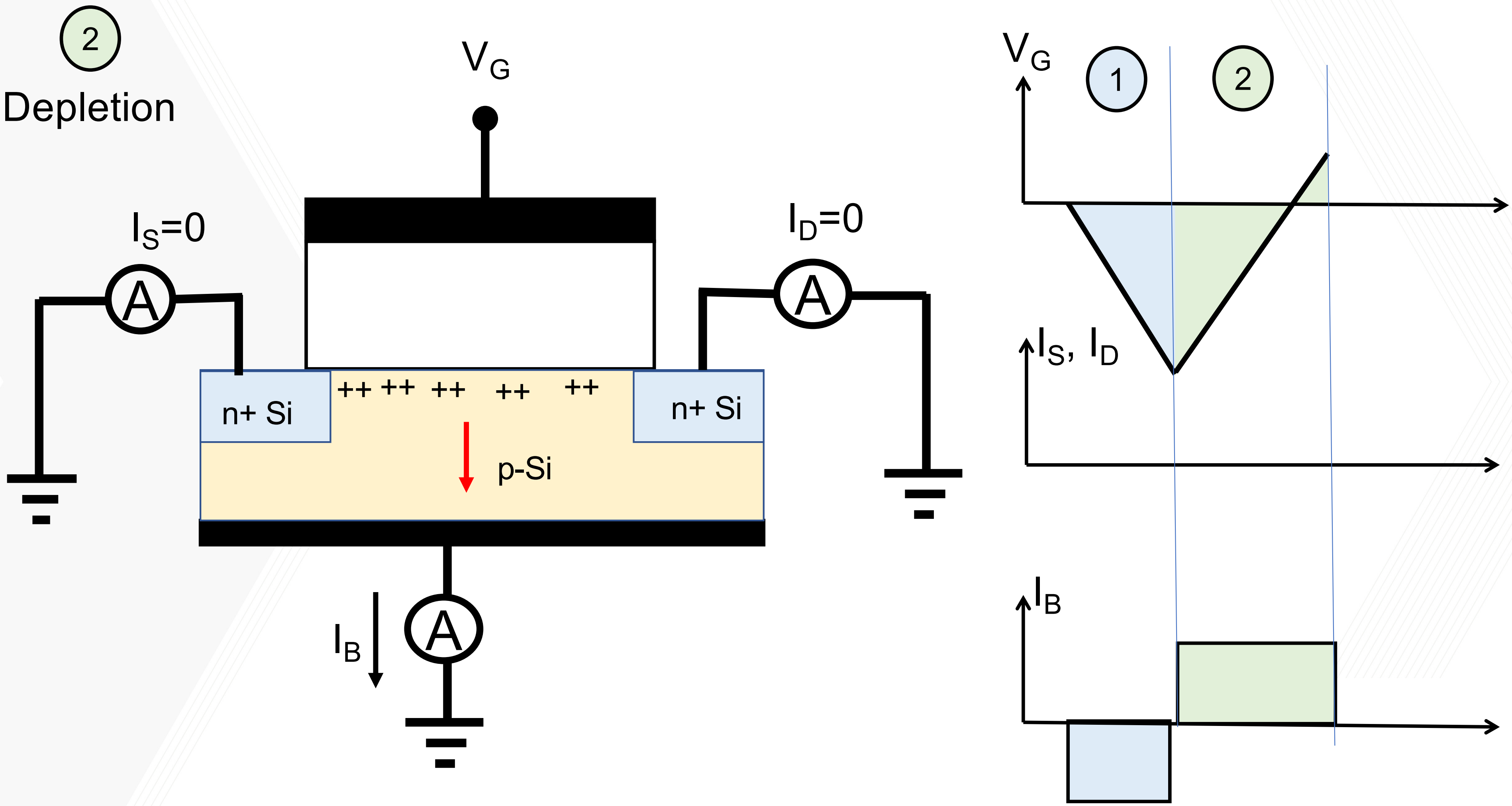
Carrier dynamics in a conventional MOSFET



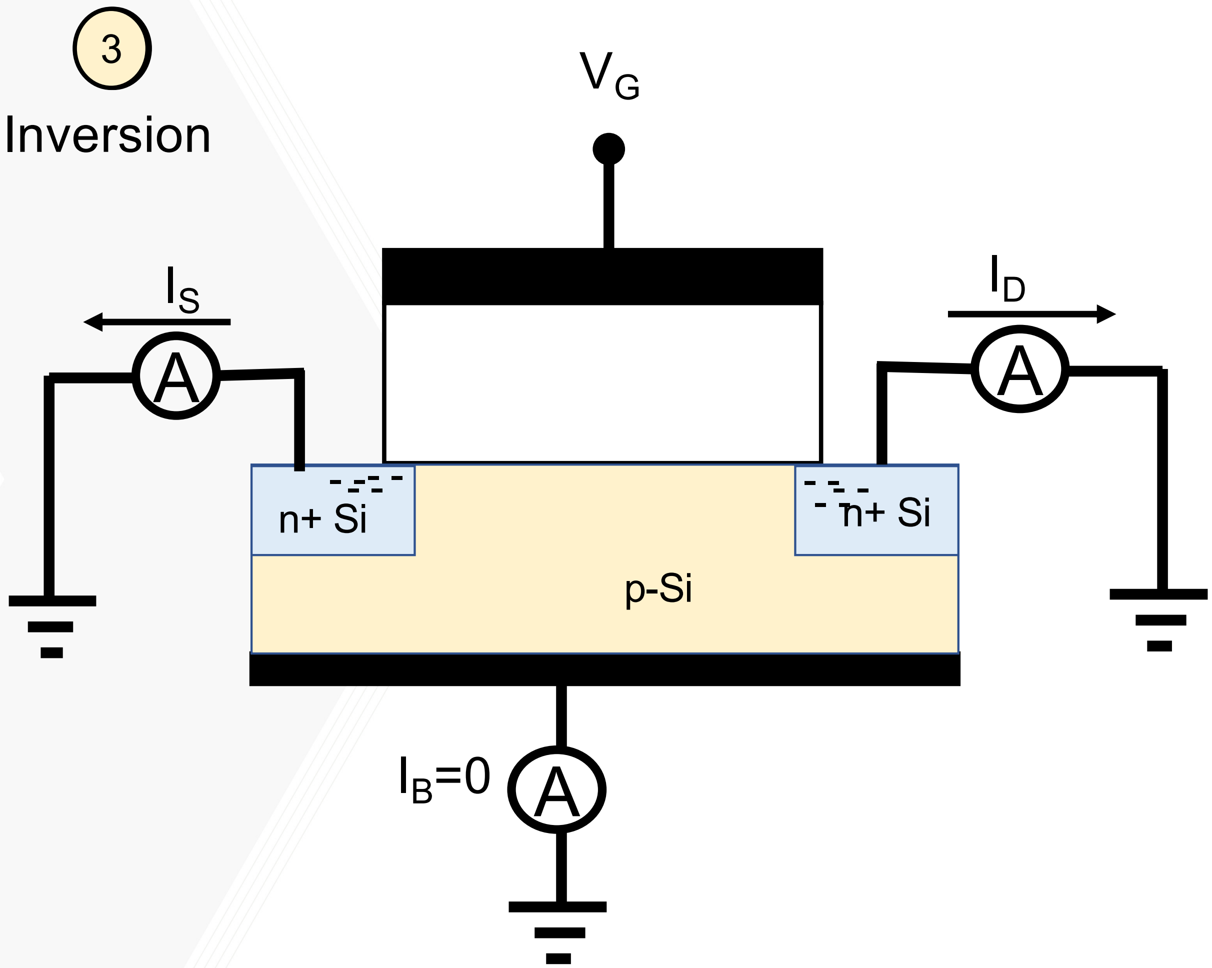
Carrier dynamics in a conventional MOSFET

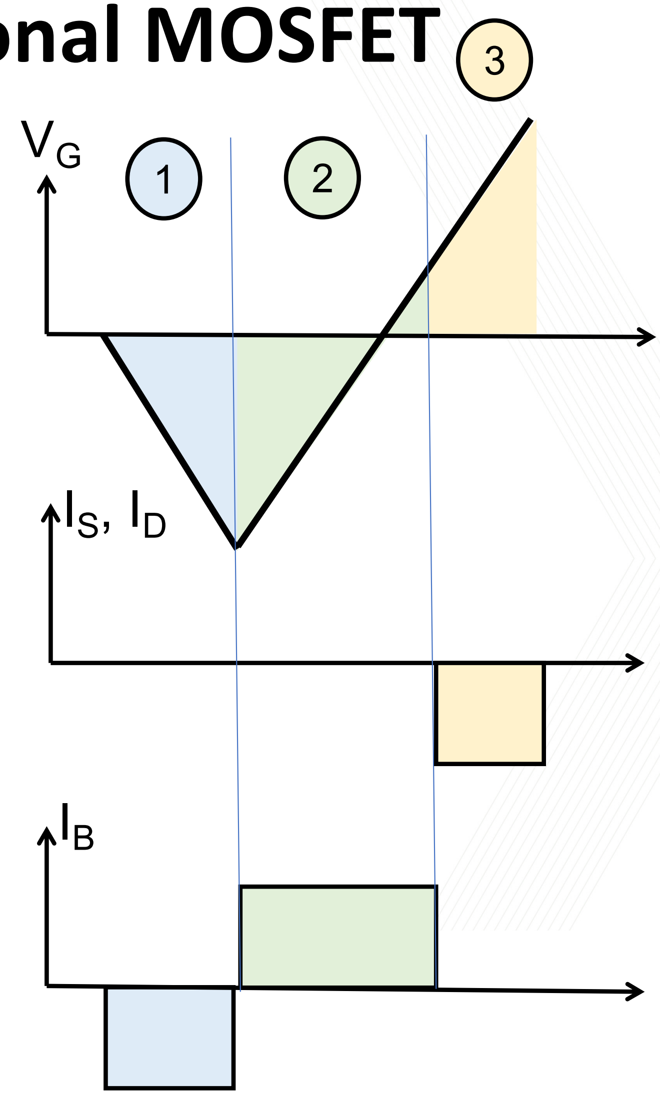


Carrier dynamics in a conventional MOSFET

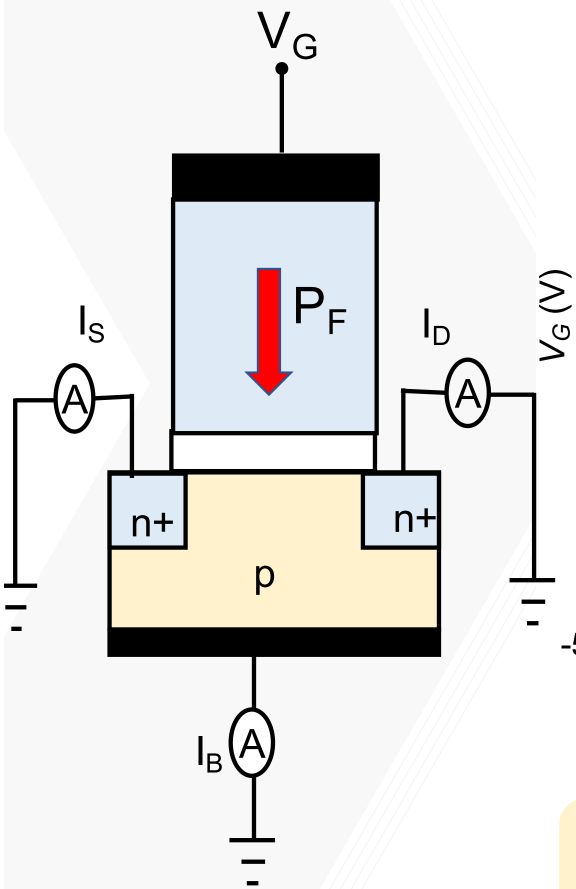


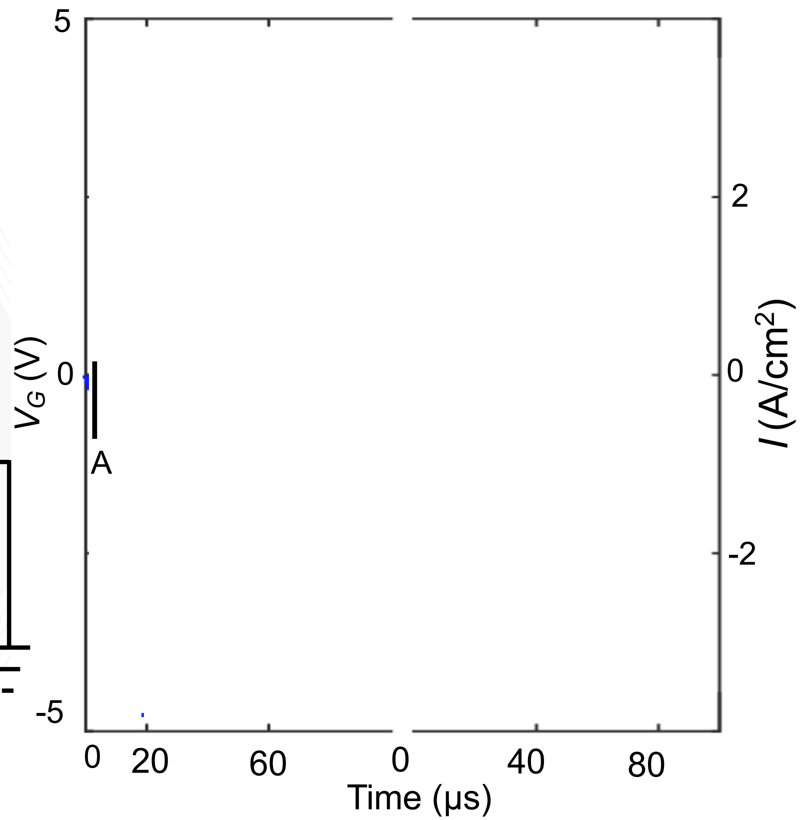
Carrier dynamics in a conventional MOSFET





Trap Emission and Capture During Write

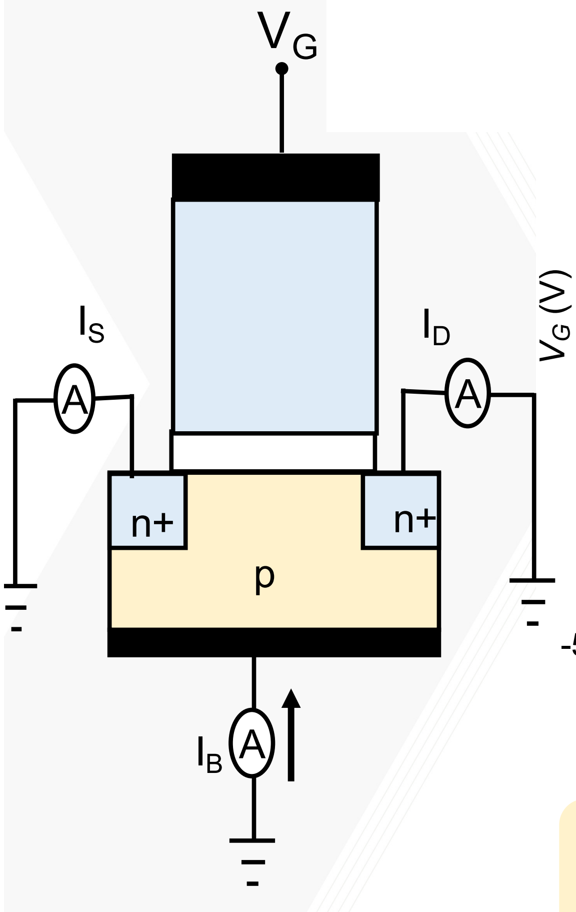


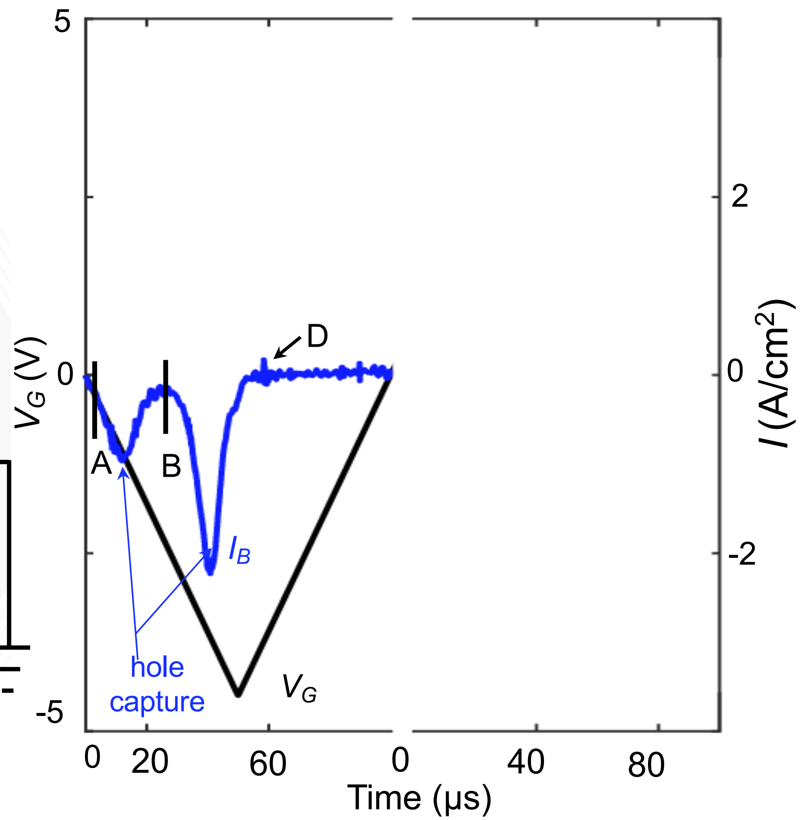


Emissions of electrons into the S/D during hole accumulation.

Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2021.

Trap Emission and Capture During Write

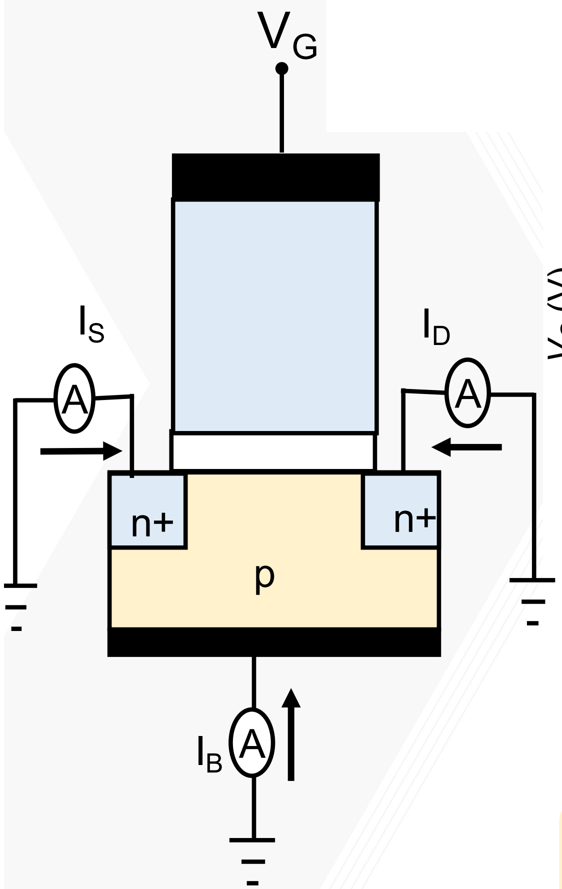


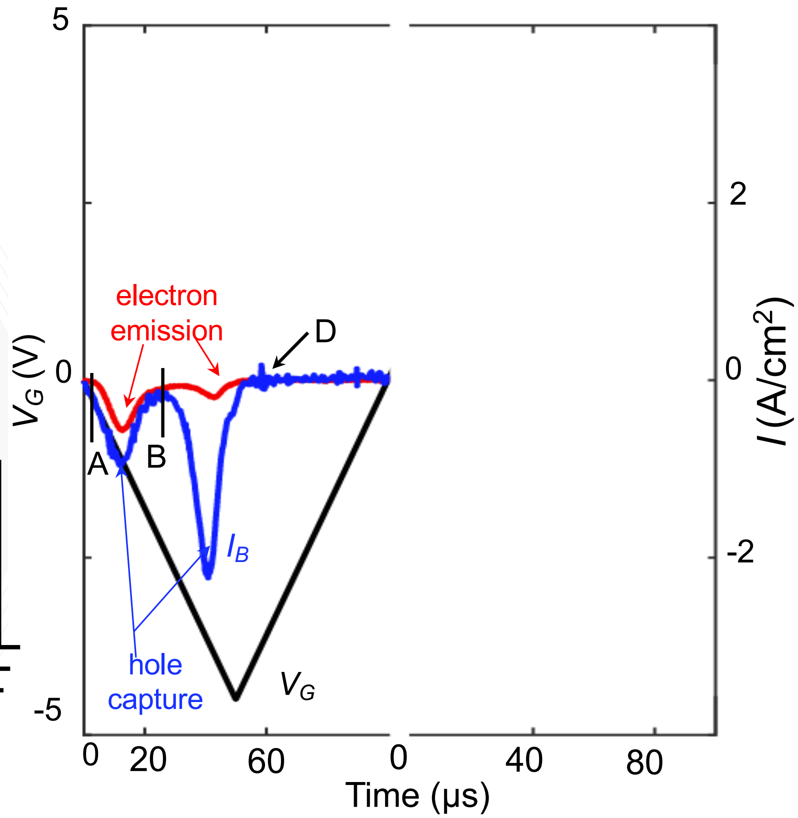


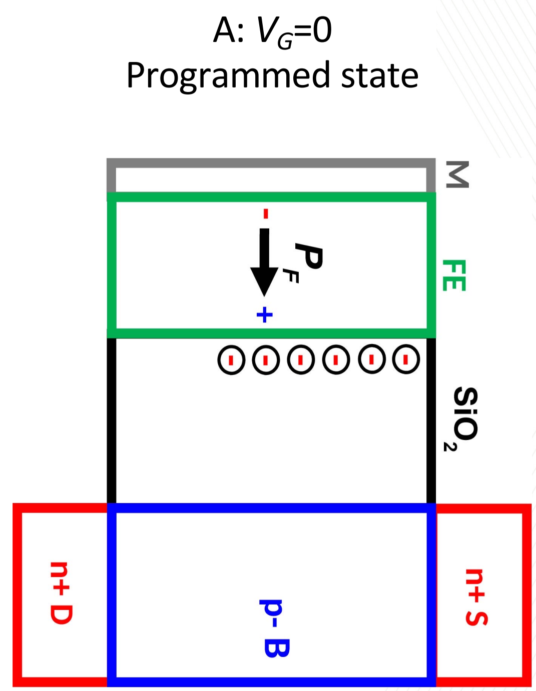
Emissions of electrons into the S/D during hole accumulation.

Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2021.

Trap Emission and Capture During Write



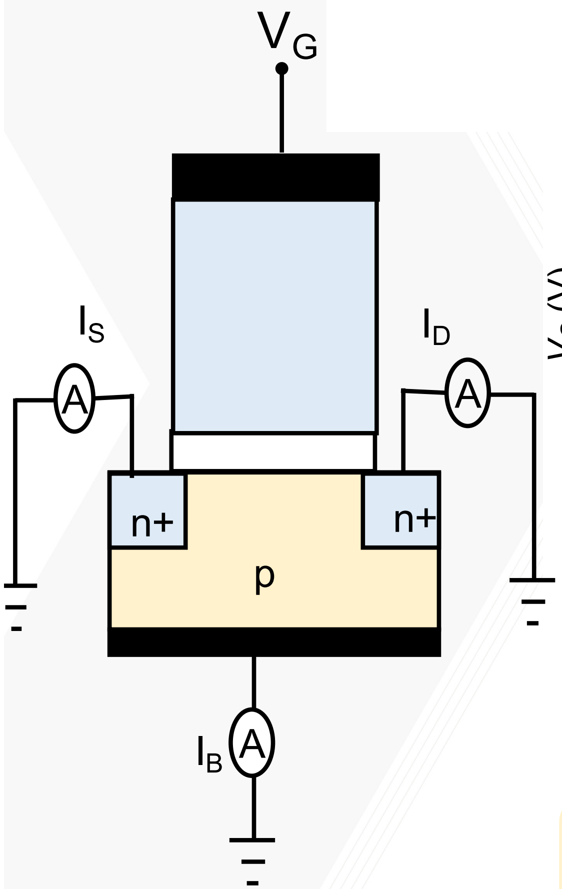


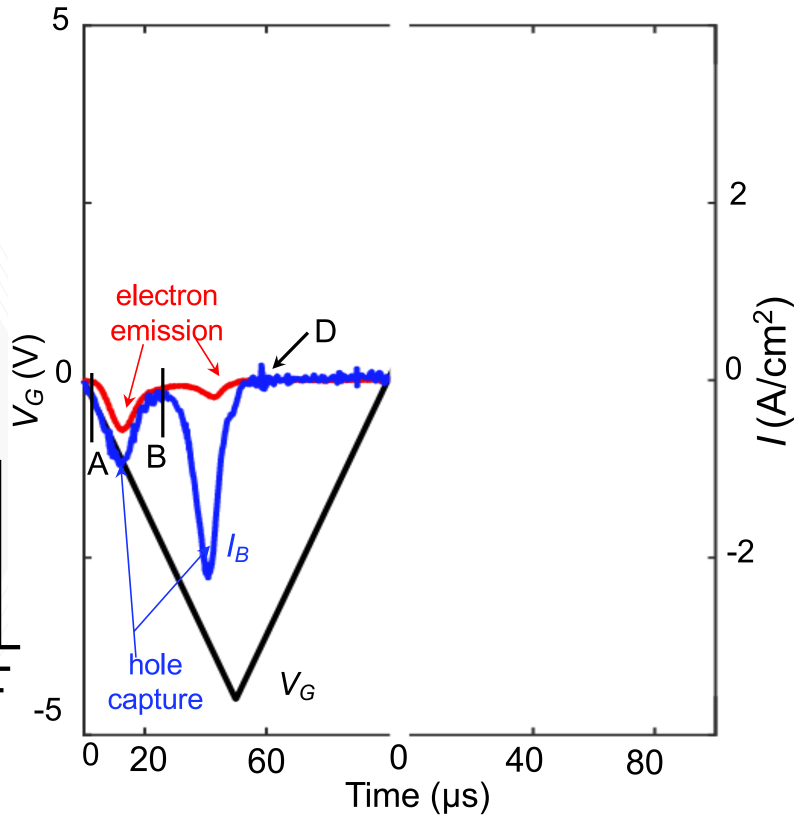


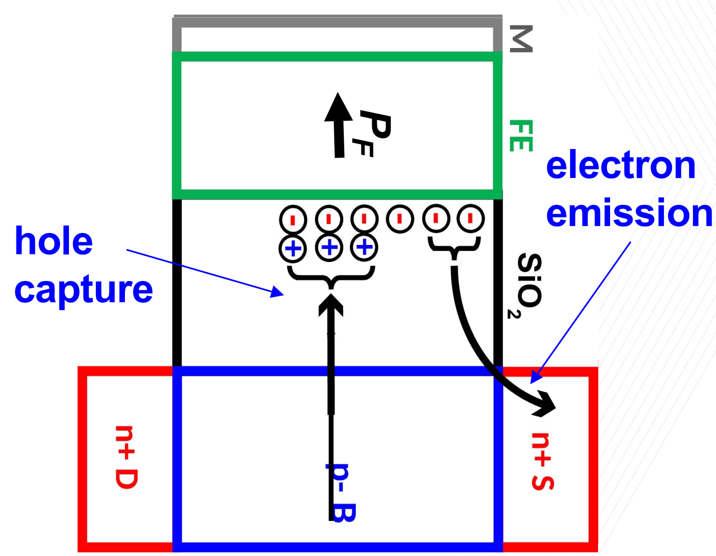
Emissions of electrons into the S/D during hole accumulation.

Tasneem et al. IEDM 2021.

Trap Emission and Capture During Write



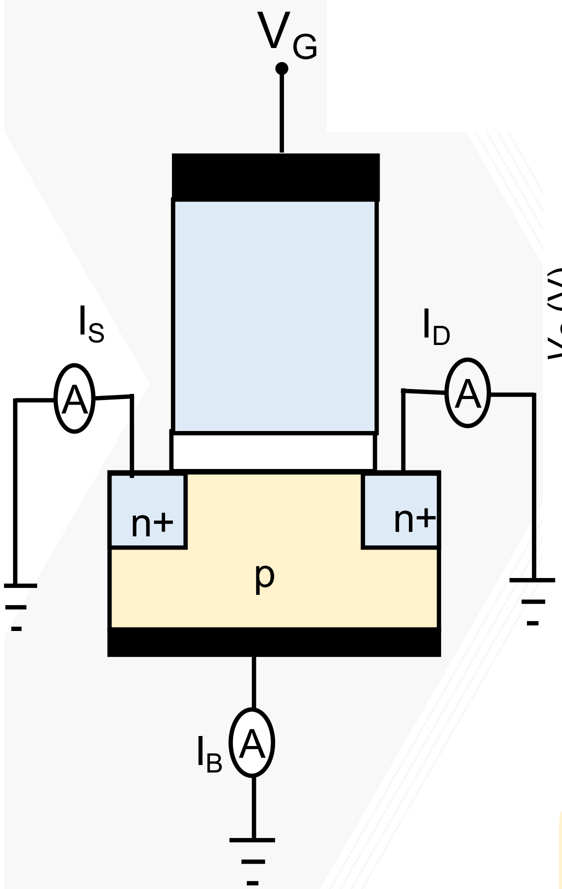


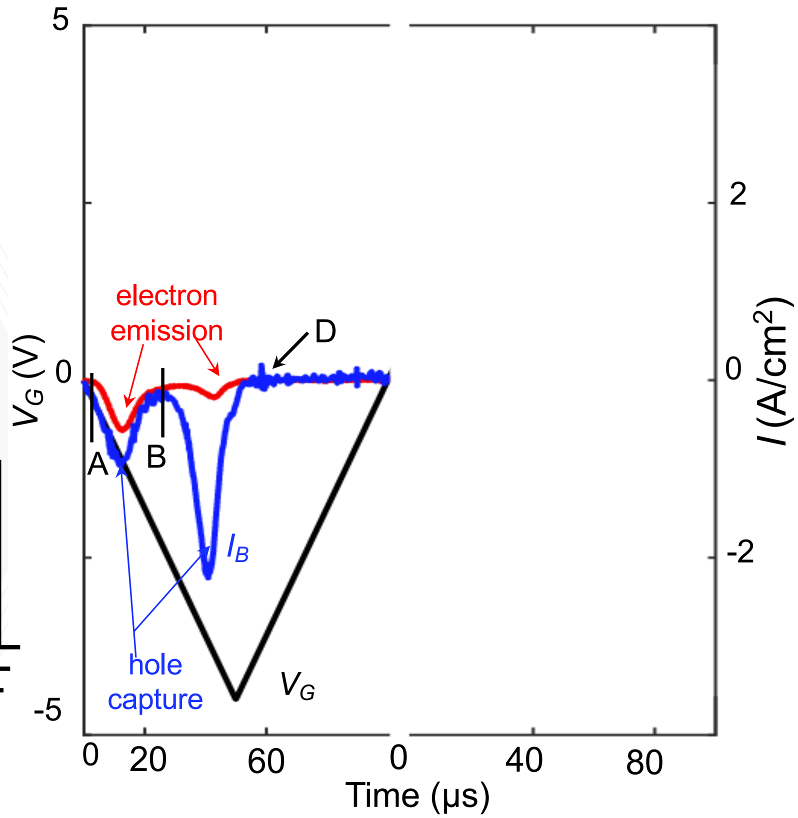


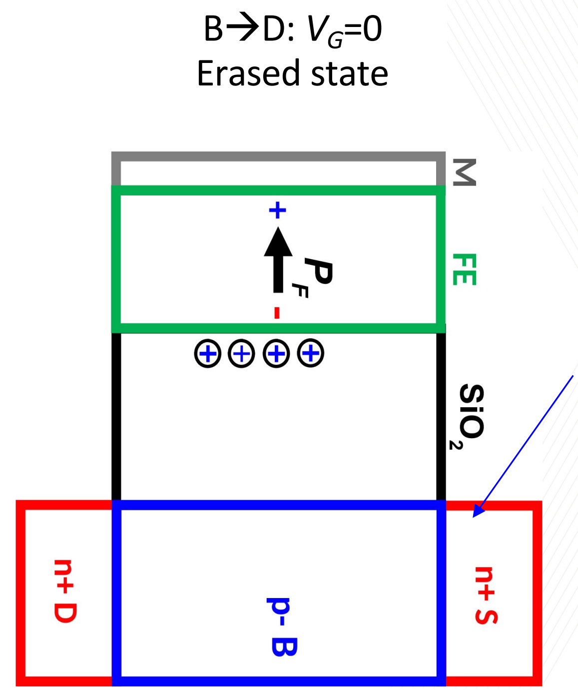
Emissions of electrons into the S/D during hole accumulation.

Tasneem et al. IEDM 2021.

Trap Emission and Capture During Write



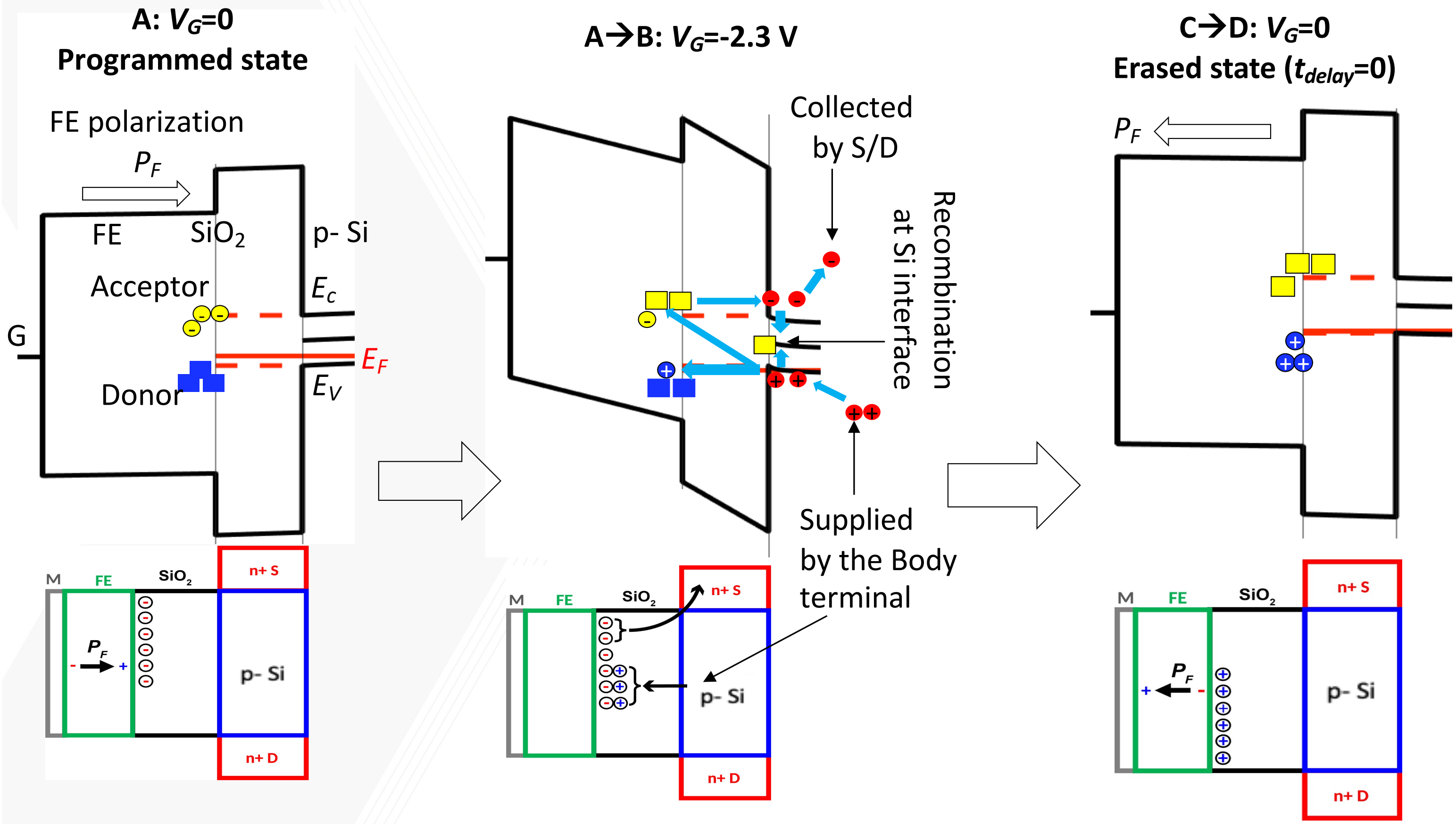




Emissions of electrons into the S/D during hole accumulation.

Tasneem et al. IEDM 2021.

Trap Capture and Emission Dynamics

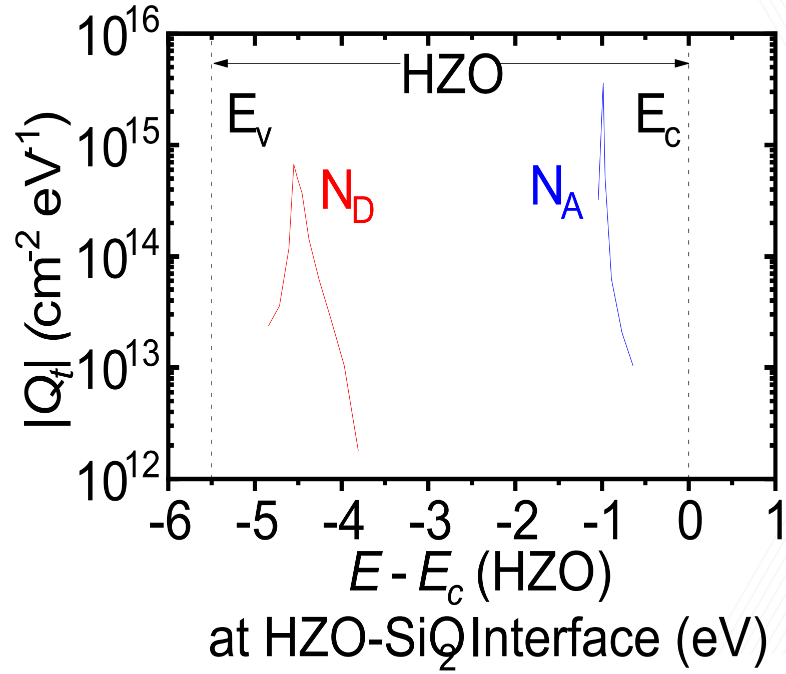


Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2021.

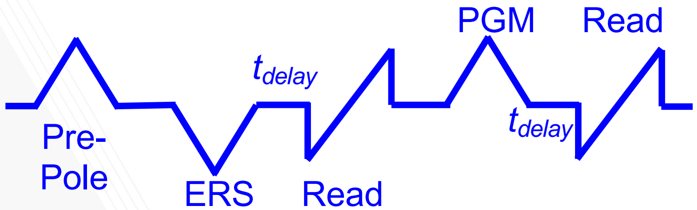
Trap Capture and Emission Dynamics

- Trap levels N_D and N_A are essentially discrete levels
- Donor type trap energy E_D is 0.93 eV above HZO E_v
- Acceptor type trap energy E_A is 0.98 eV below HZO E_c

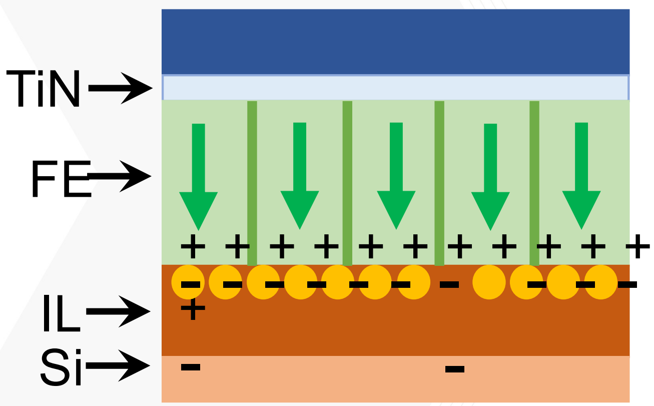
Passlack, Tasneem et al. IEDM 2022.

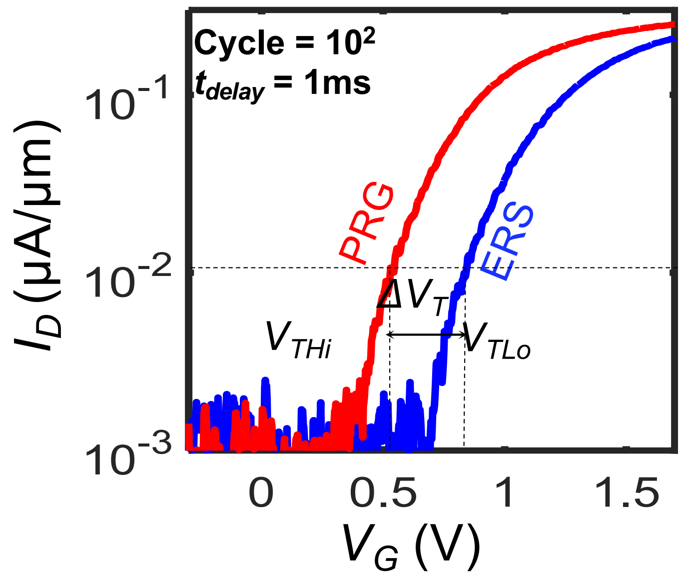


Read After Write Delay



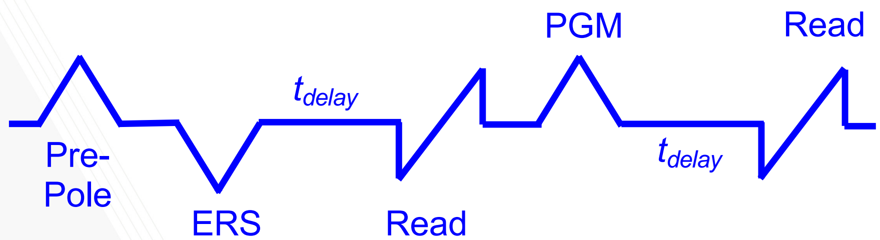
Wang et al. IEDM 2021.



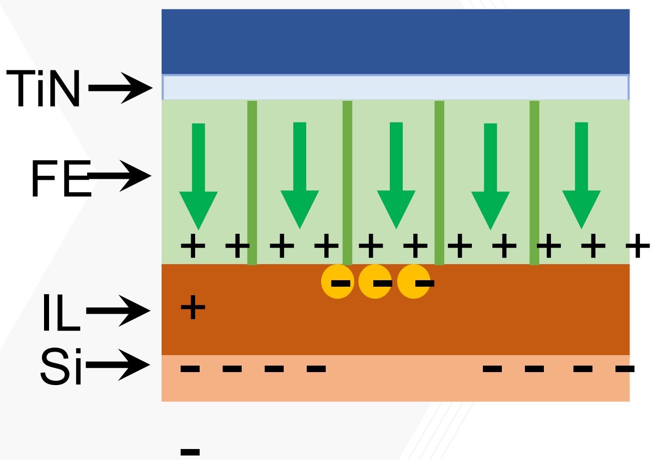


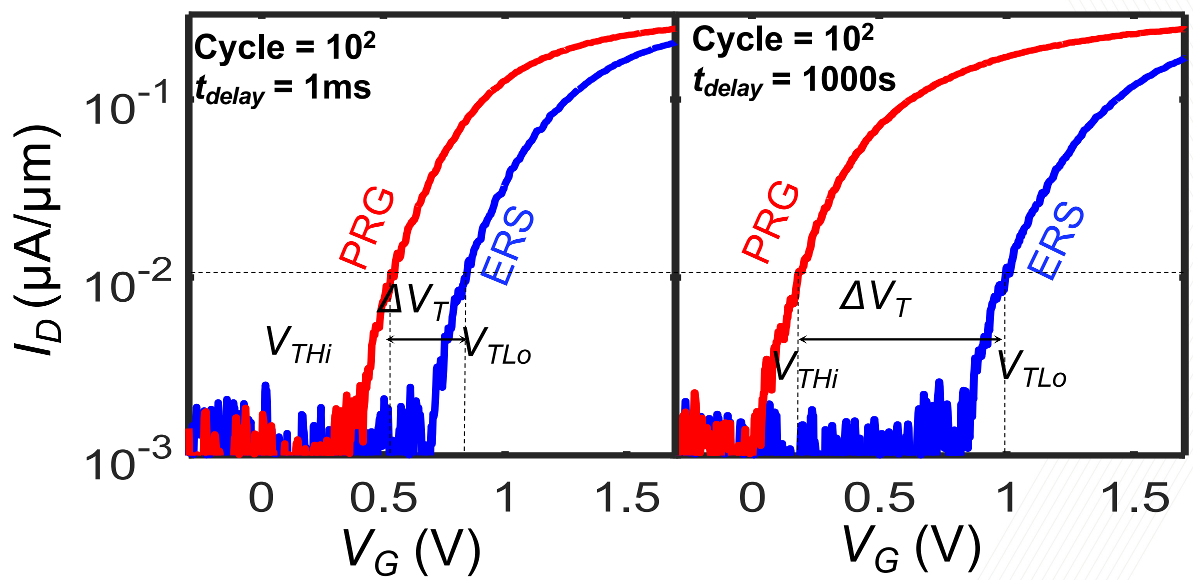
- Ferroelectric polarization is screened by interfacial traps.
- Delay allows for trap neutralization, increasing MW.

Read After Write Delay



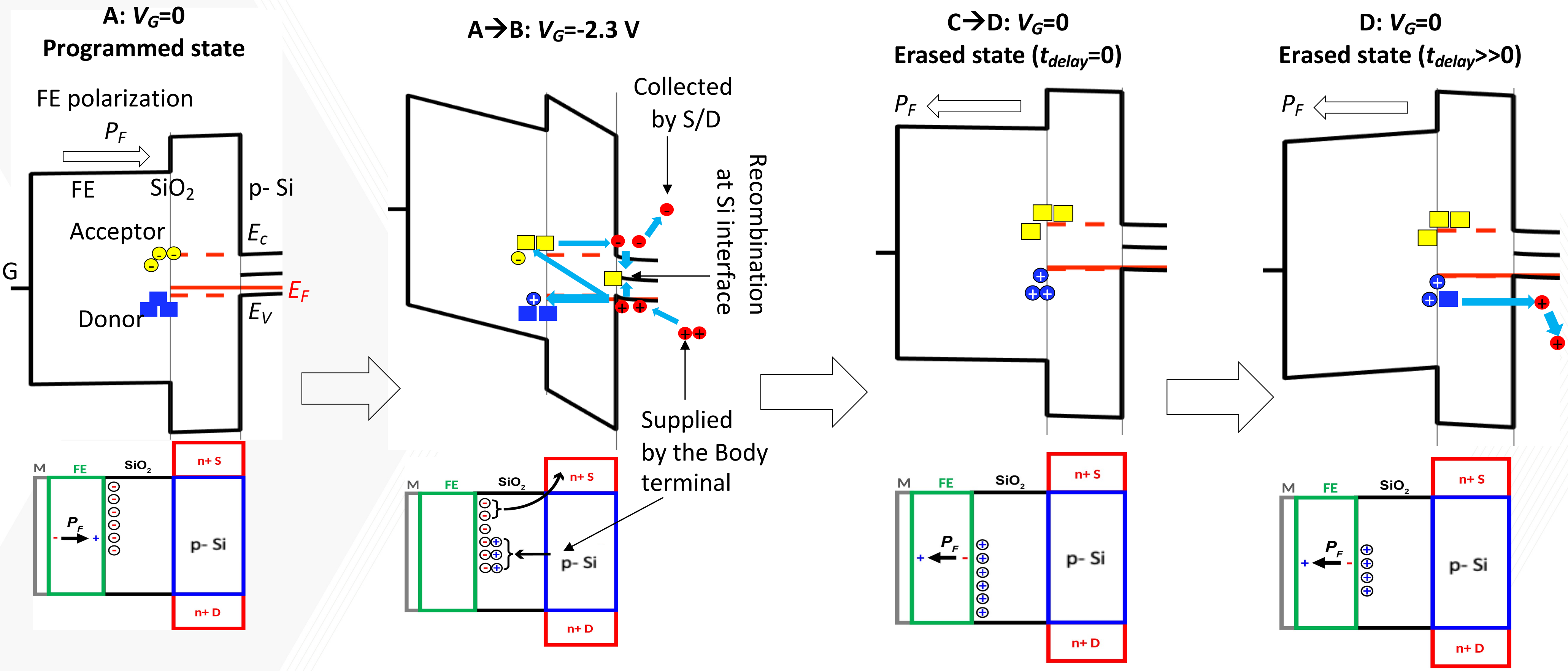
Wang et al. IEDM 2021.





- Ferroelectric polarization is screened by interfacial traps.
- Delay allows for trap neutralization, increasing MW.

Trap Capture and Emission Dynamics



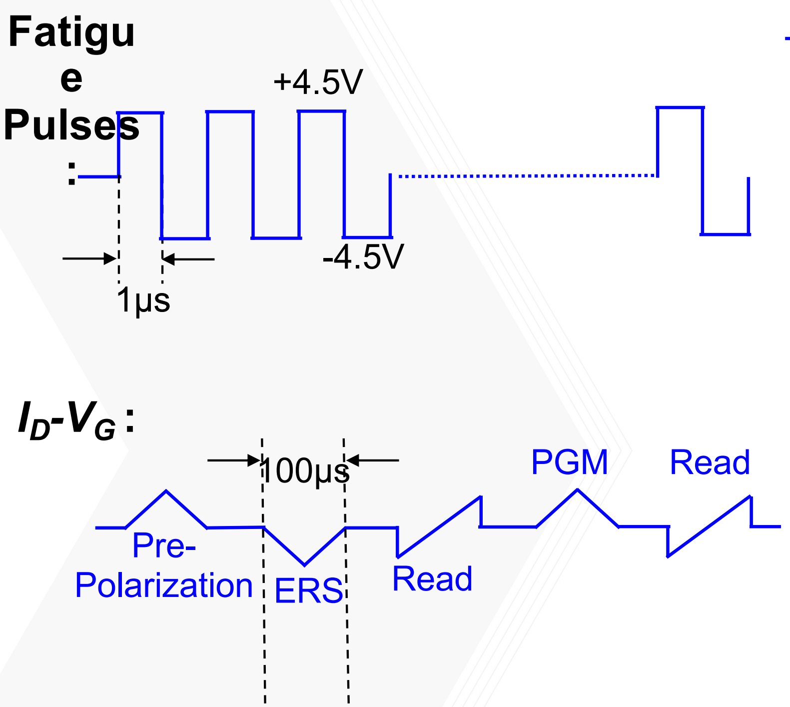
Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2011.

Take-away #2

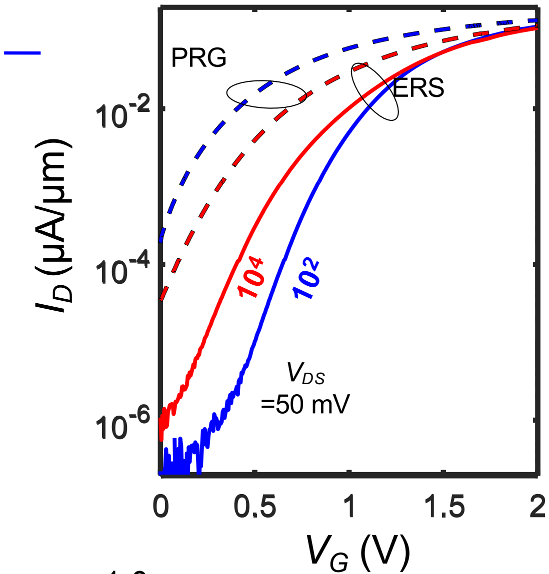
Ferroelectric switching in a FEFET requires assistance from trap capture and emission dynamics!

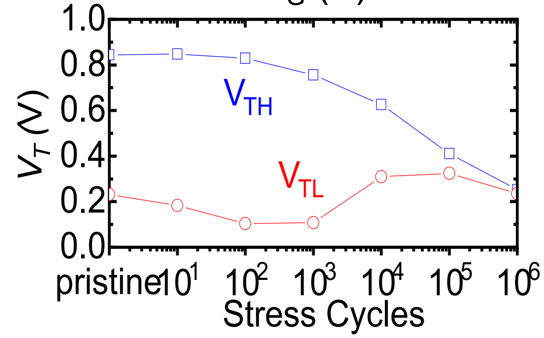
This is fundamental device physics of FEFETs!

I_D-V_G during Fatigue Cycling

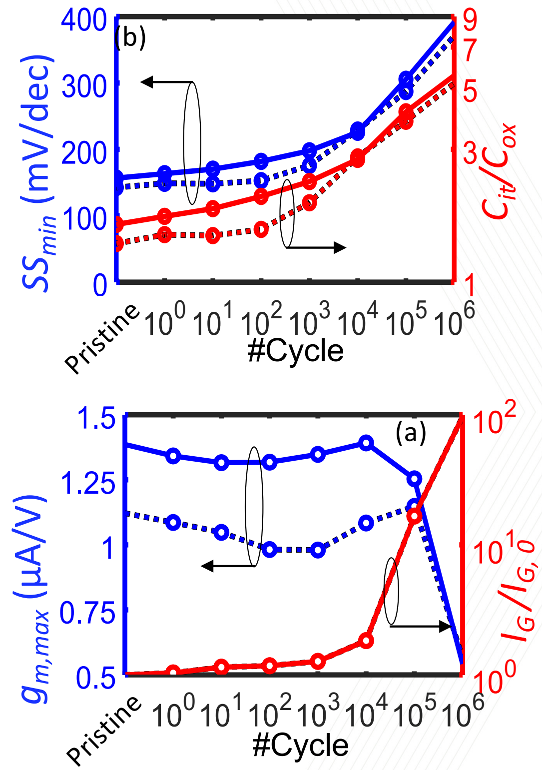


Tasneem et al. IEDM 2021.



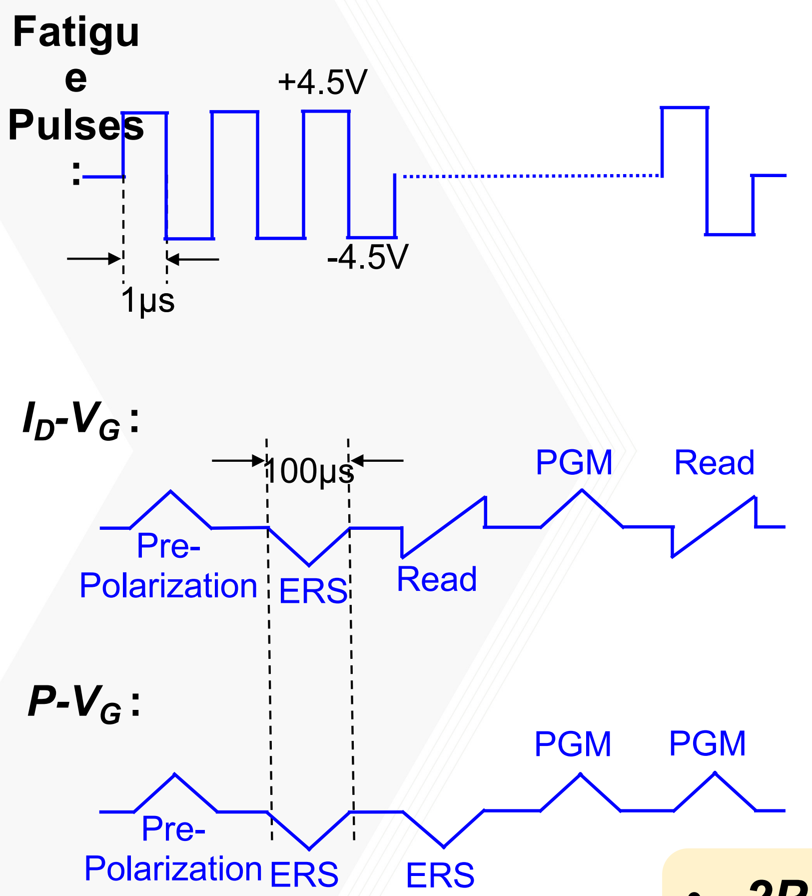


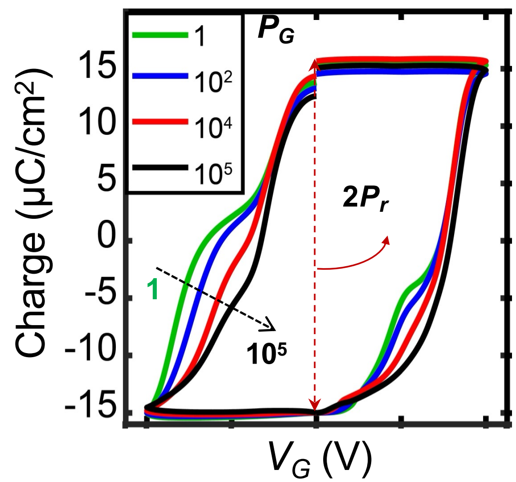
Tasneem et al. IEDM 2021



V_T decreases with cycling→Build-up of positive charge during cycling.

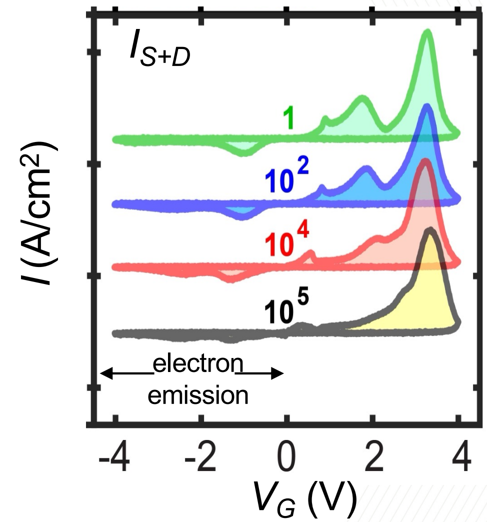
P_F-V_G during Fatigue Cycling





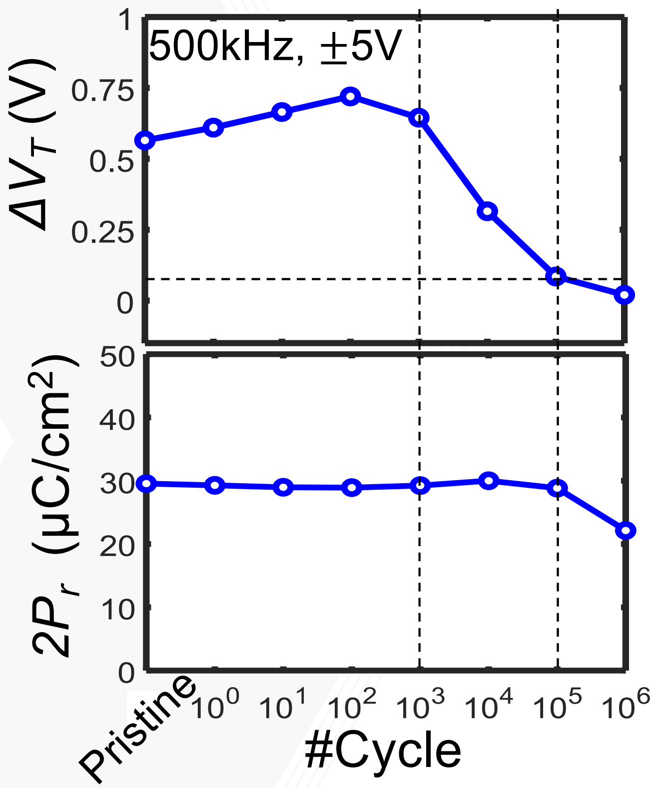
Tasneem et al. IEDM 2021.

Electron Emission During Hole Accumulation

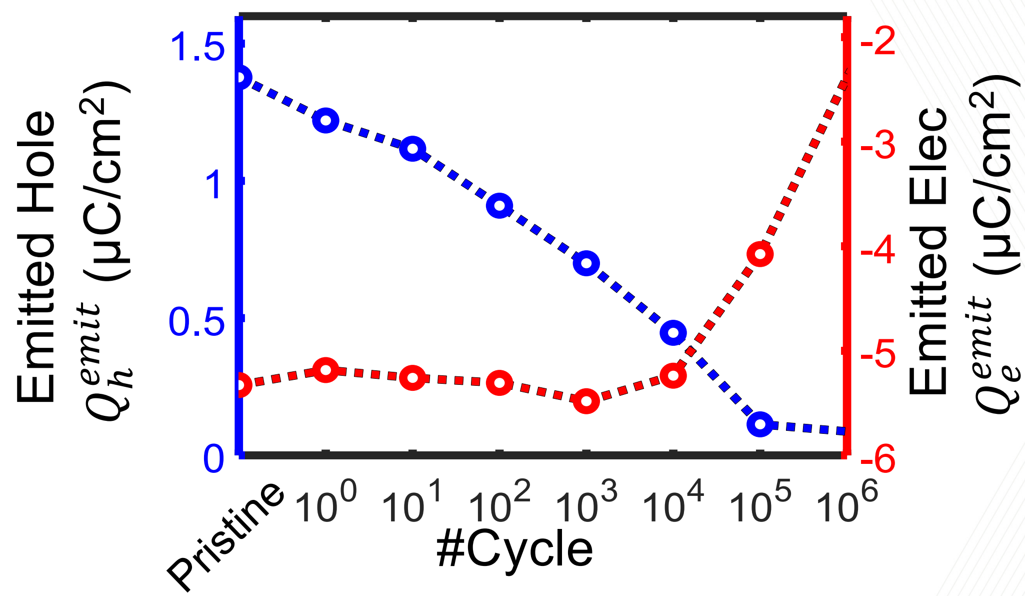


- ***2P_r*** does not change with cycling.
- Electron and hole emission changes with cycling

Trap Emission with Fatigue Cycling

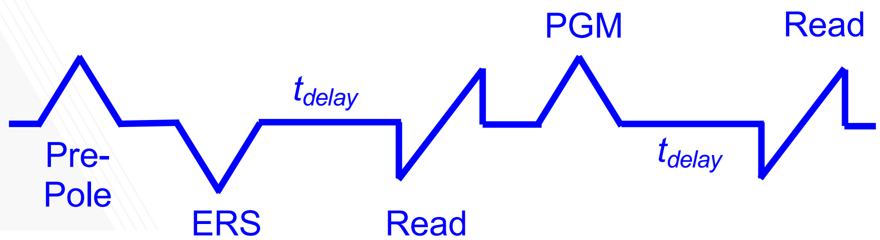


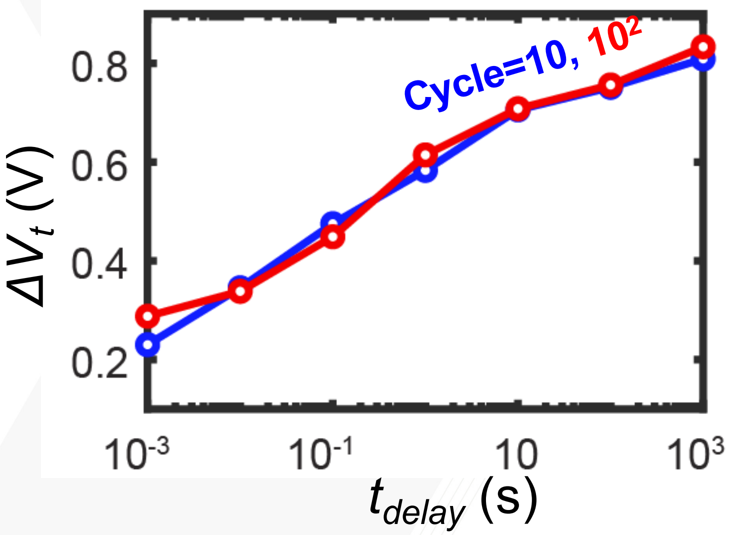
Tasneem et al. IEDM 2021.

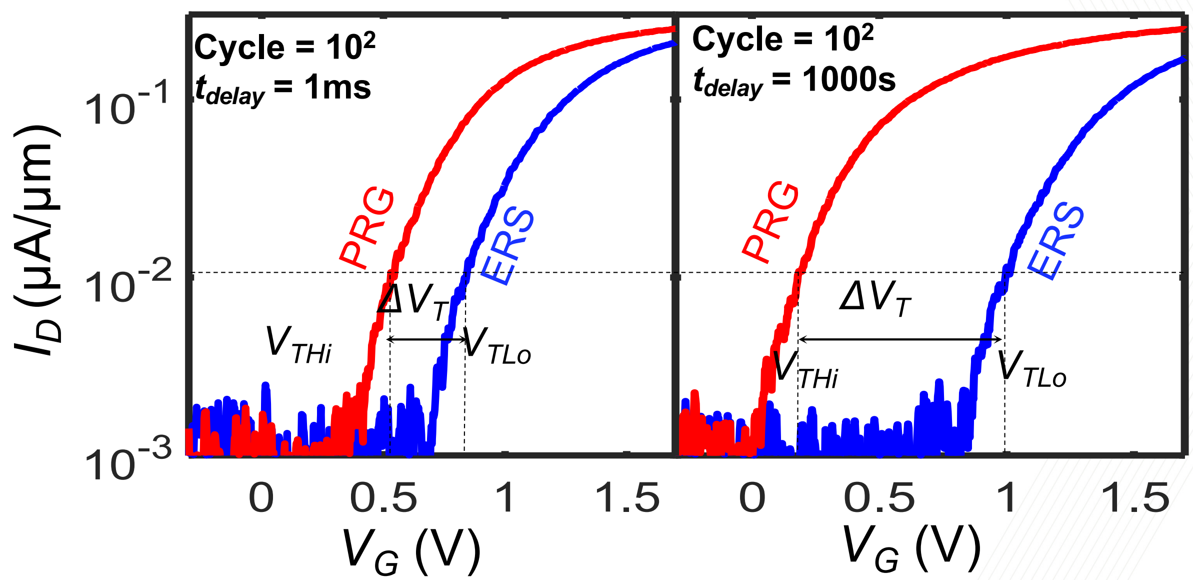


10^8/cm² holes get "permanently" trapped per cycle.

Delay with Cycling

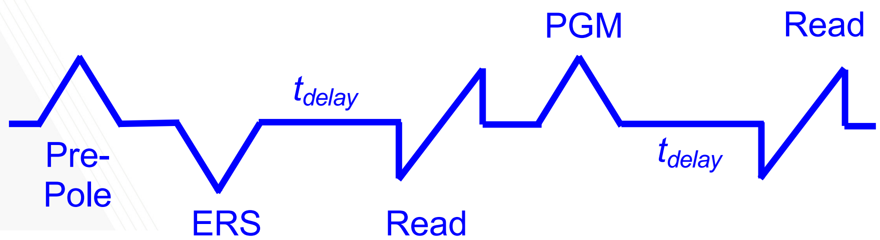




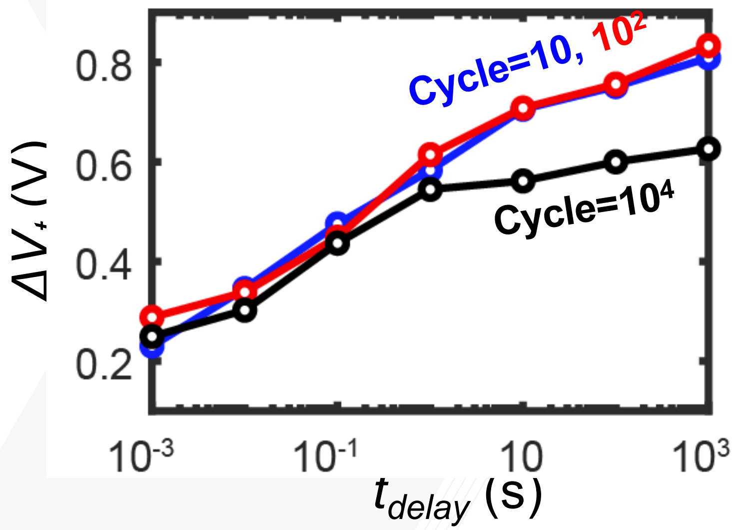


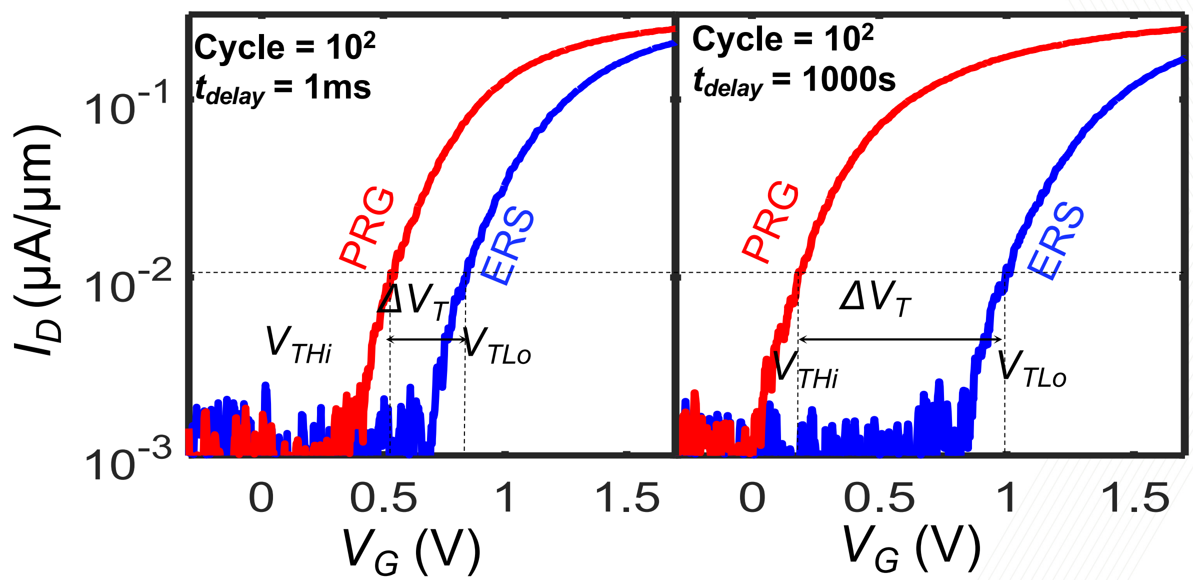
Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2021.

Delay with Cycling



Tasneem et al. IEDM 2021.

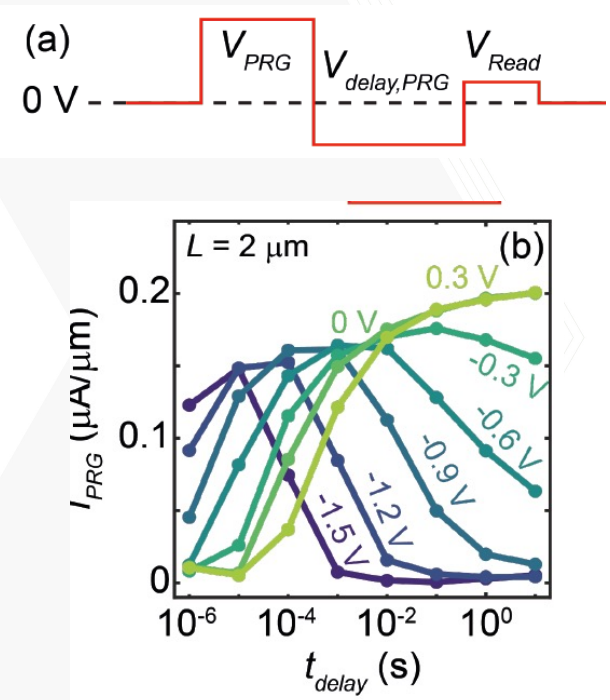


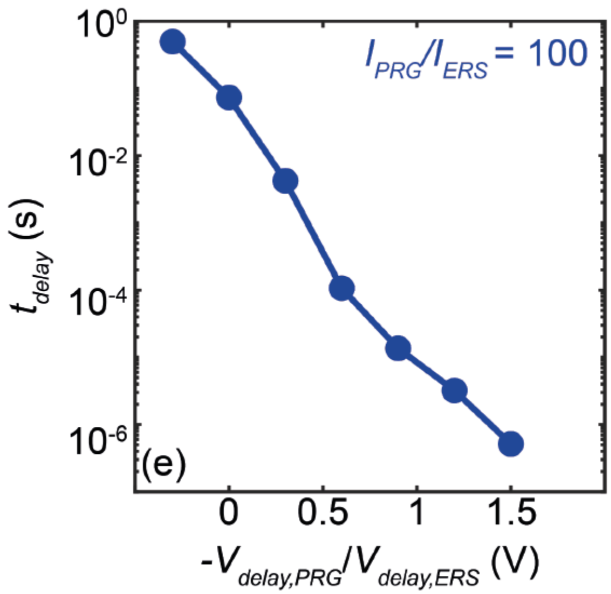


Change in MW recovery rate in fatigues devices indicate trapping in states with larger lifetimes.

Stand-by bias improvement in Read-After-Write Delay

Wang et al. IEDM 2021.

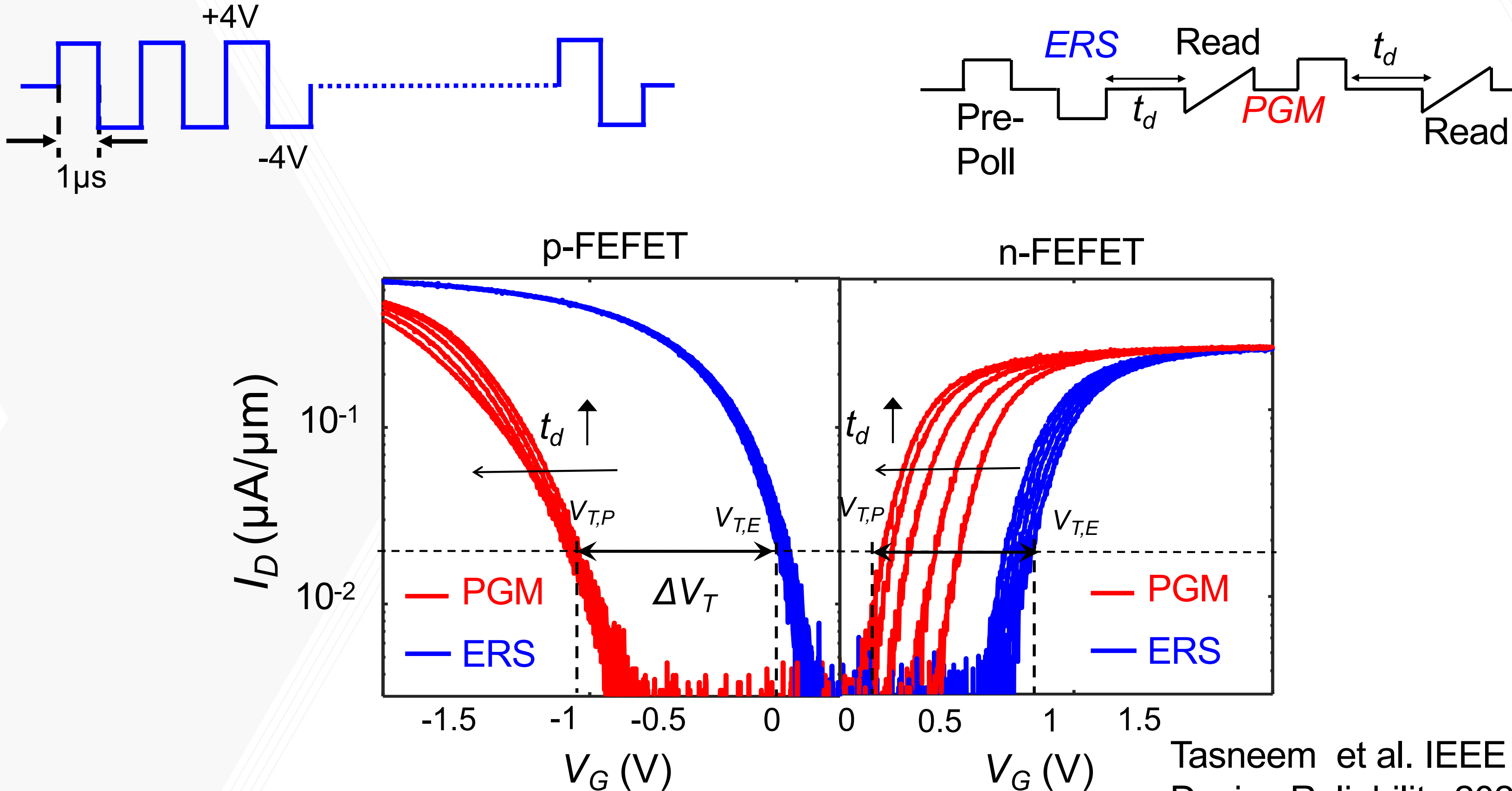




Stand-by bias enables fast neutralization of trapped charges and hence allows for faster read and better endurance.

Wang et al. Stand-by bias improvement in read-after-wrte delay in ferroelectric field-effect transistors, IEDM 2011.
Wang et al. Standby Bias Improves the Endurance in Ferroelectric Field Effect Transistors due to Fast Neutralization of Interface Traps, VLSI TSA 2011.

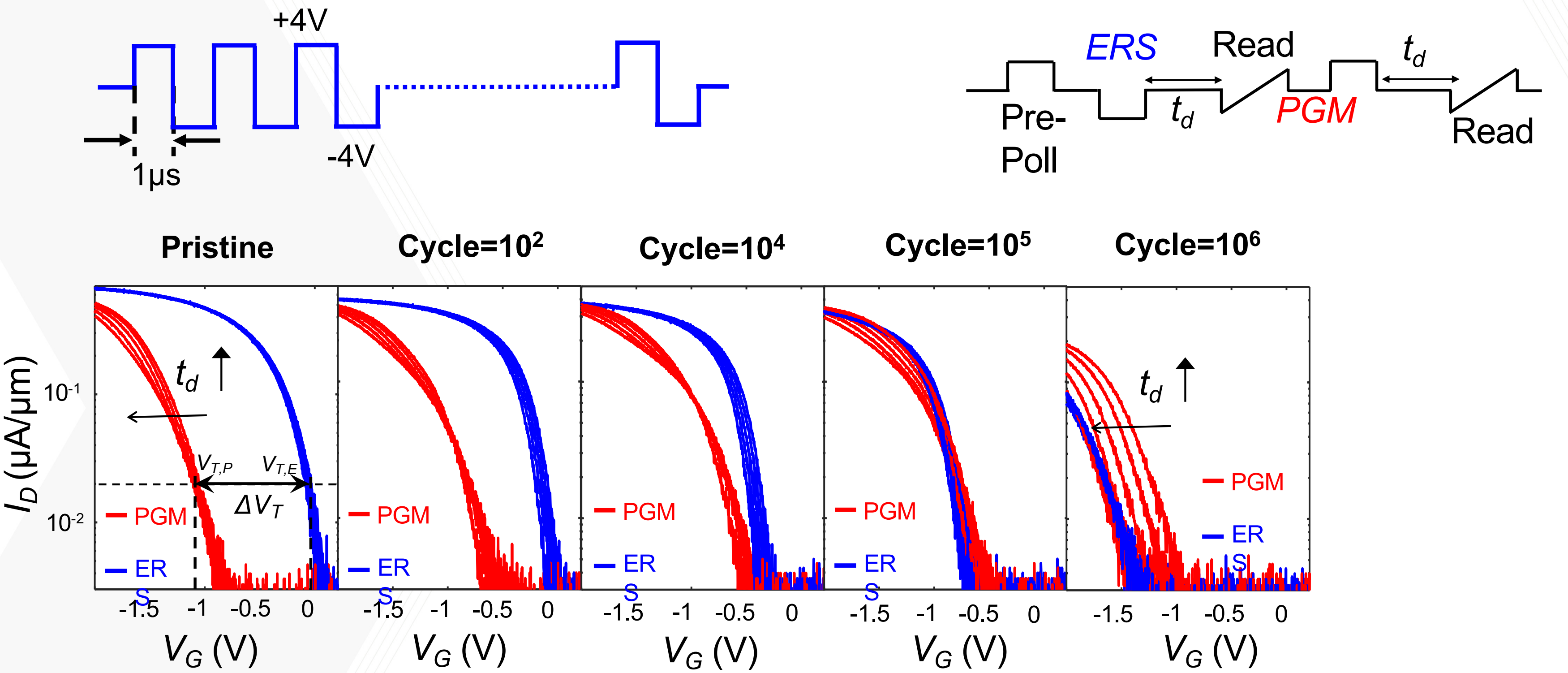
Read after Write Delay in p- vs n-type FEFETs



Tasneem et al. IEEE T Materials and Device Reliability 2023.

Immediate read after write capability in p-FEFETs

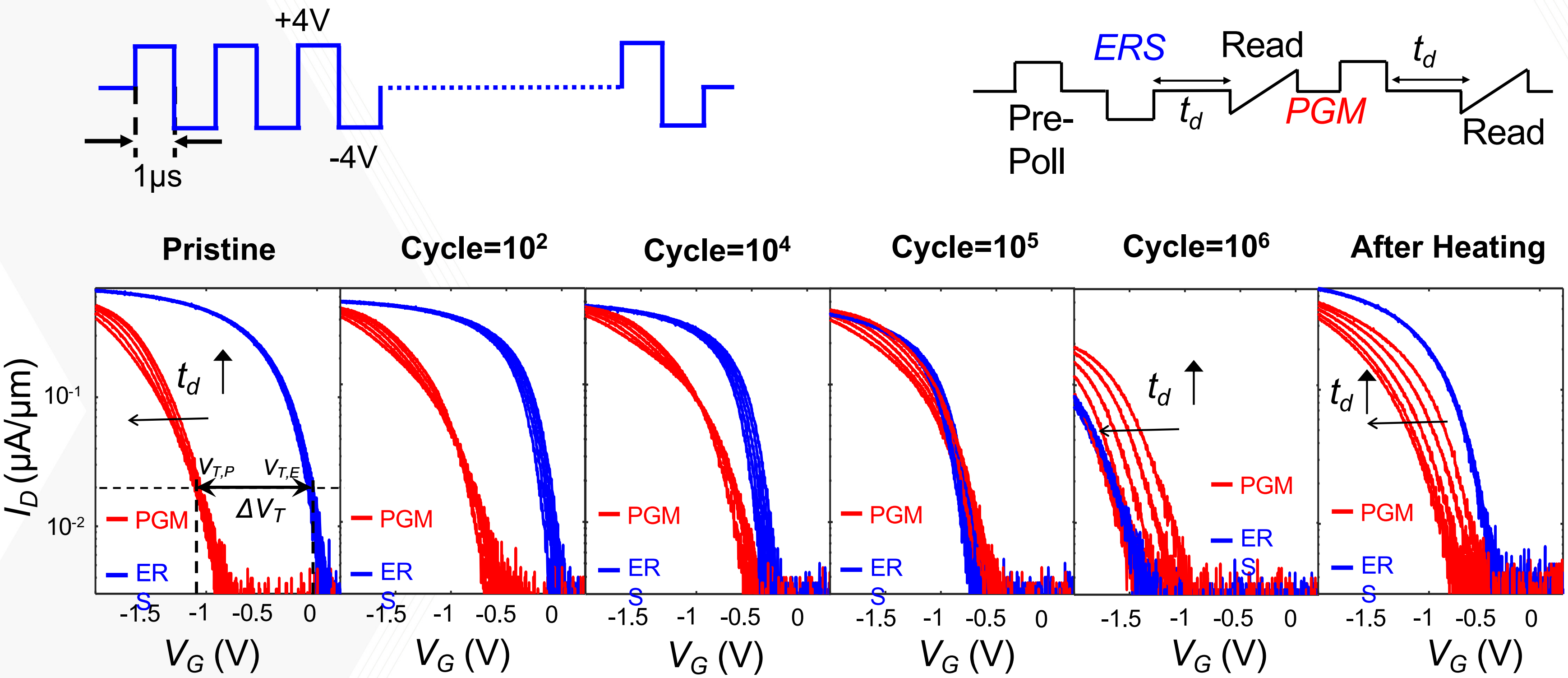
Read after Write Delay in p-FEFETs with cycling



Tasneem et al. IEEE T Materials and Device Reliability 2023.

MW (ΔV_T) is constant with delay until cycle # 10^6

Post-Stress Thermal Treatment



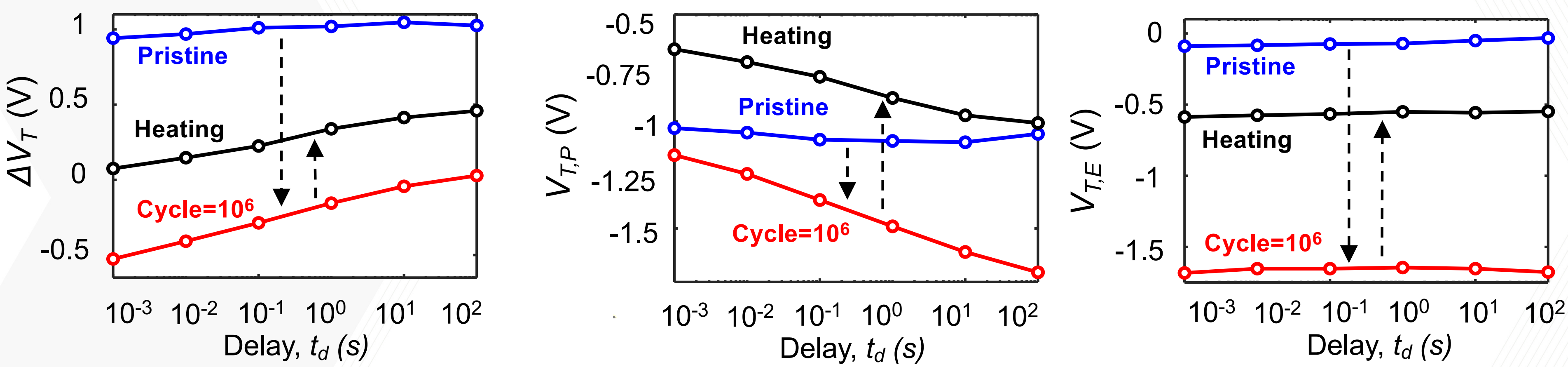
400C, 30min FGA:

- Partially recovers ~50% of pre-stress ΔV_T
- Retains post-stress, pre-treatment ΔV_T recovery characteristics

Tasneem et al. IEEE T Materials and Device Reliability 2023.

Read after Write Delay in p-FEFETs

Post-Stress Thermal Treatment



Tasneem et al. IEEE T Materials and Device Reliability (under review).

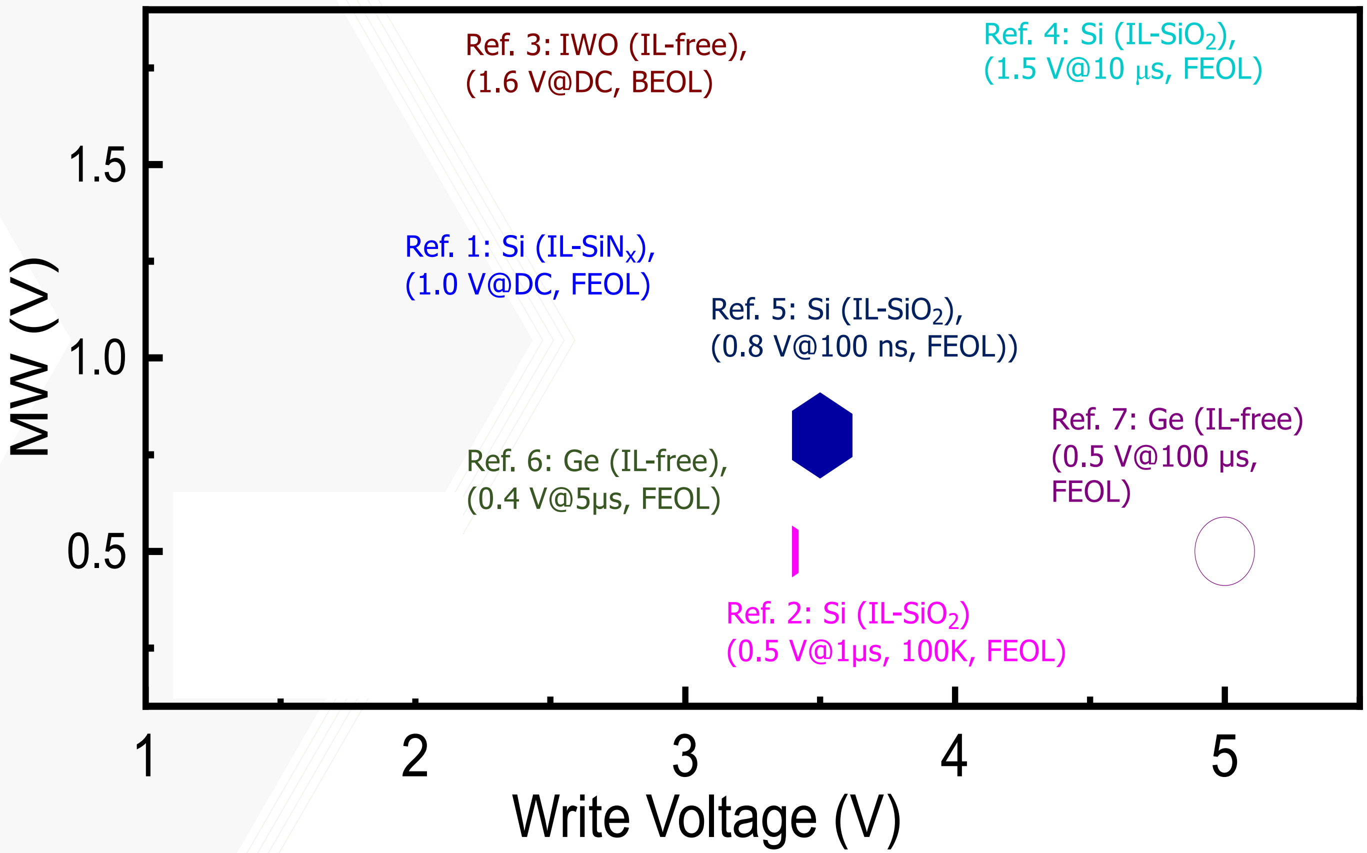
Slope of the curve *(MW recovery rate)* after the thermal treatment remains the same as that of 10^6 cycle

Take-away #3

Different types of traps are responsible for different performance degradation mechanism!

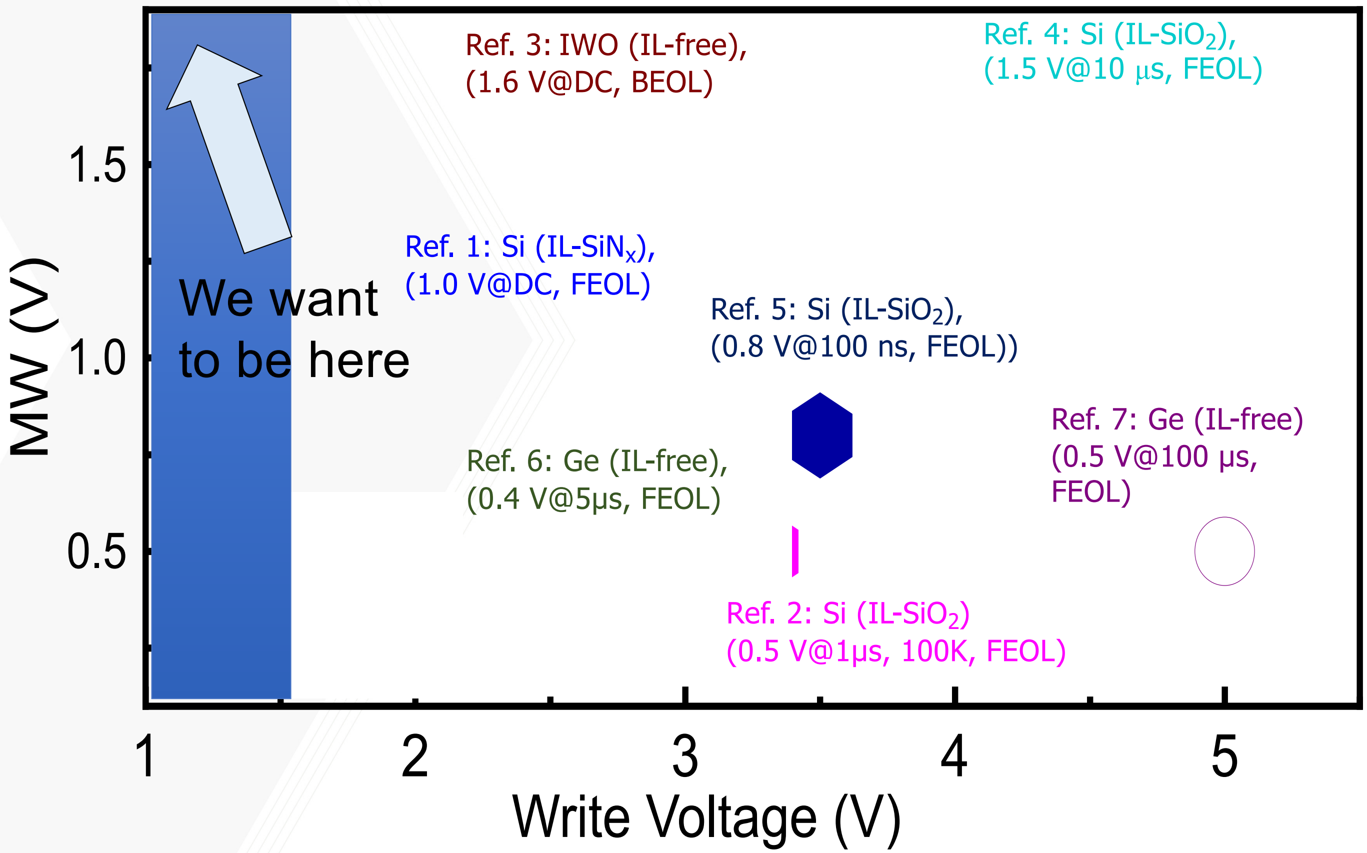
Georgia Tech
CREATING THE NEXT

Benchmarking Memory Window v. Write Voltage Tradeoff



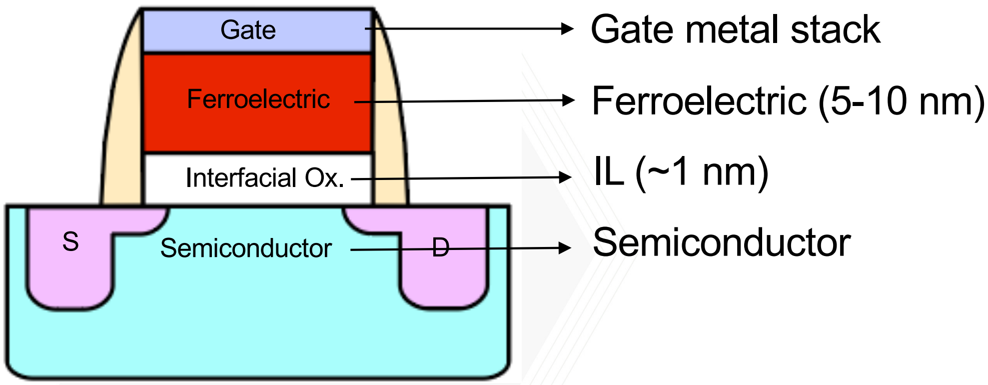
[1] Tan *et al., IEEE EDL*, 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

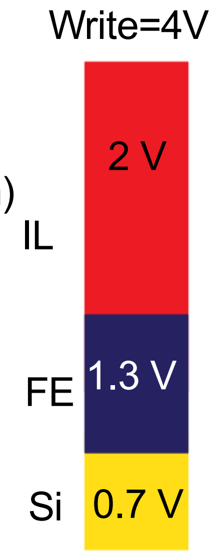
Benchmarking Memory Window v. Write Voltage Tradeoff

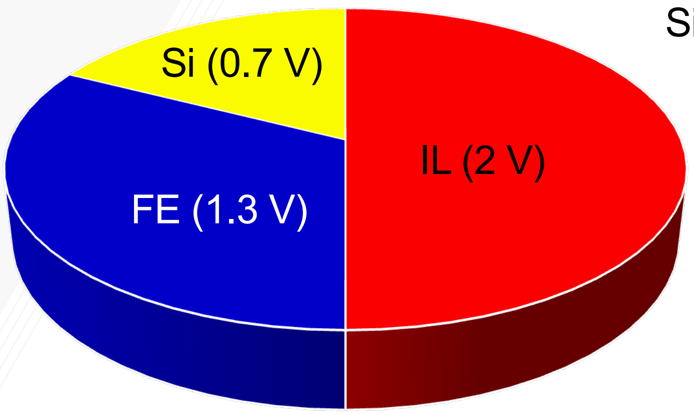


[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

Write voltage vs. memory window trade-off

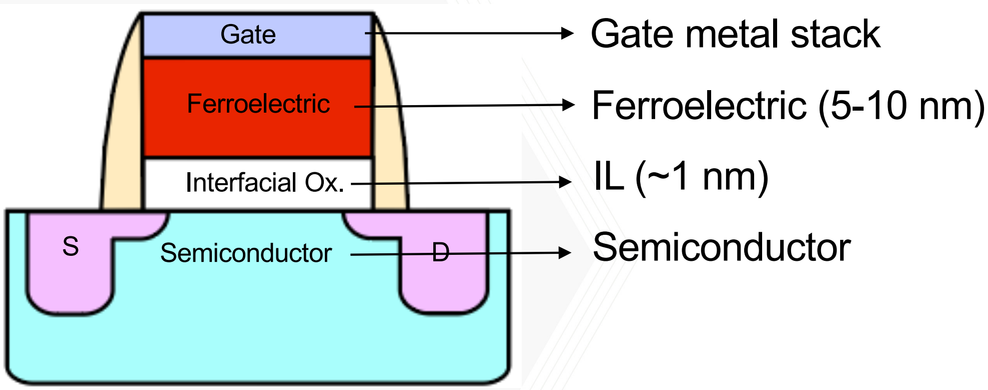


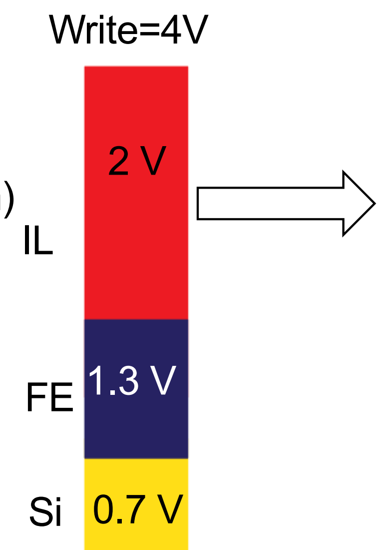




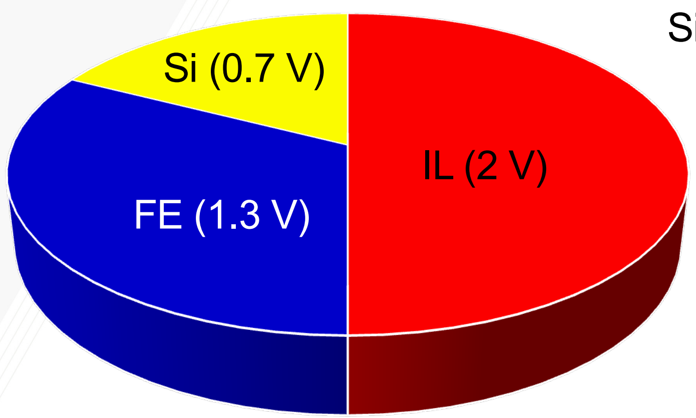
Georgia Tech
CREATING THE NEXT

Write voltage vs. memory window trade-off

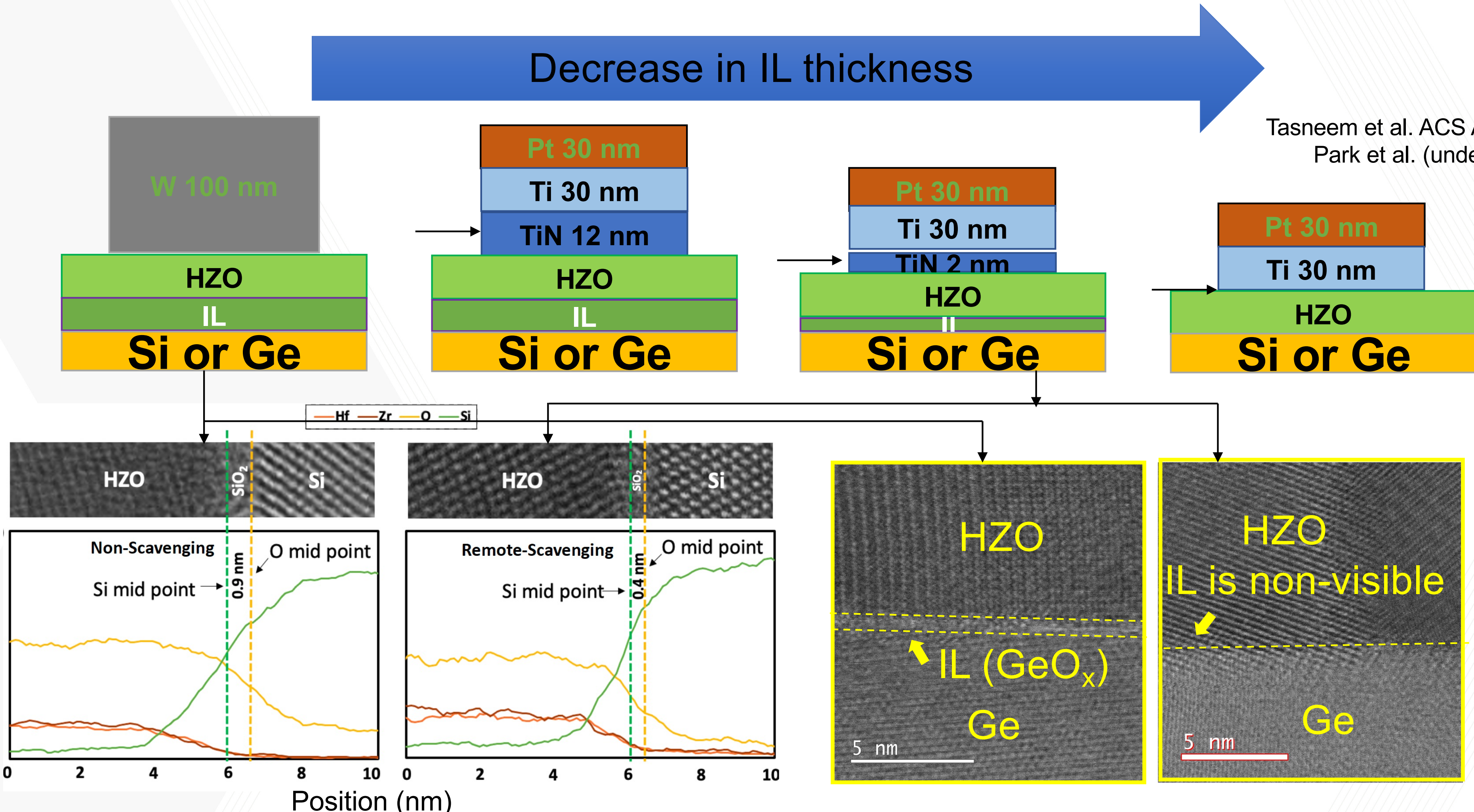




Reducing the thickness of the IL or increasing the K of the IL. *Reliability degradation is a concern.*



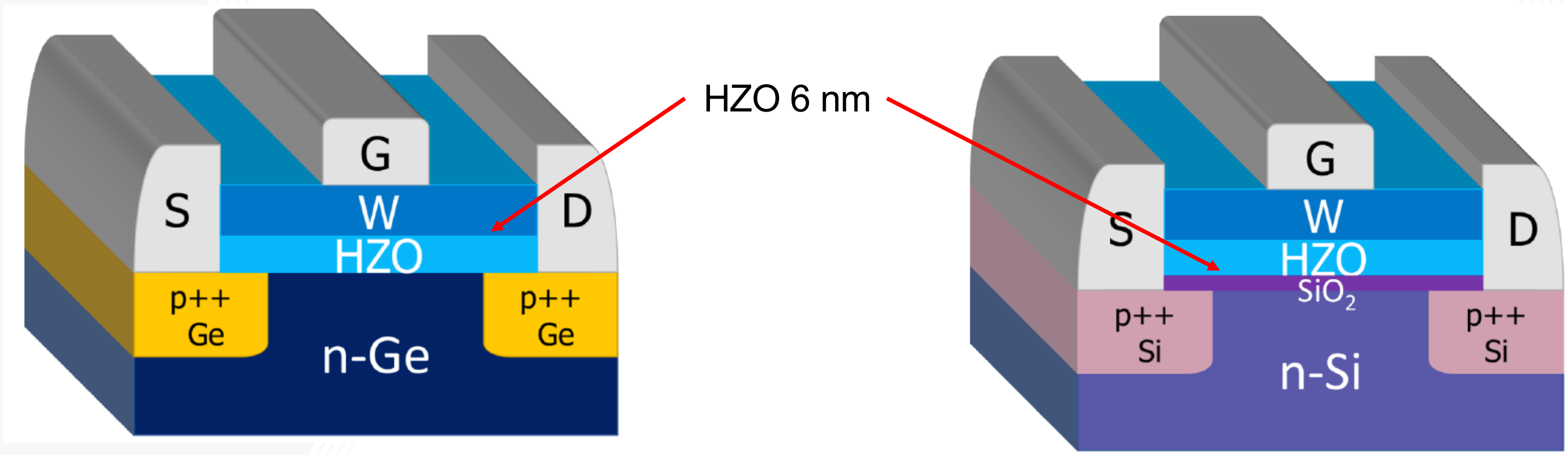
Georgia Tech
CREATING THE NEXT



Tasneem et al. ACS AMI 2022
Park et al. (under review)

Remote oxygen scavenging can result in controllable IL thickness.

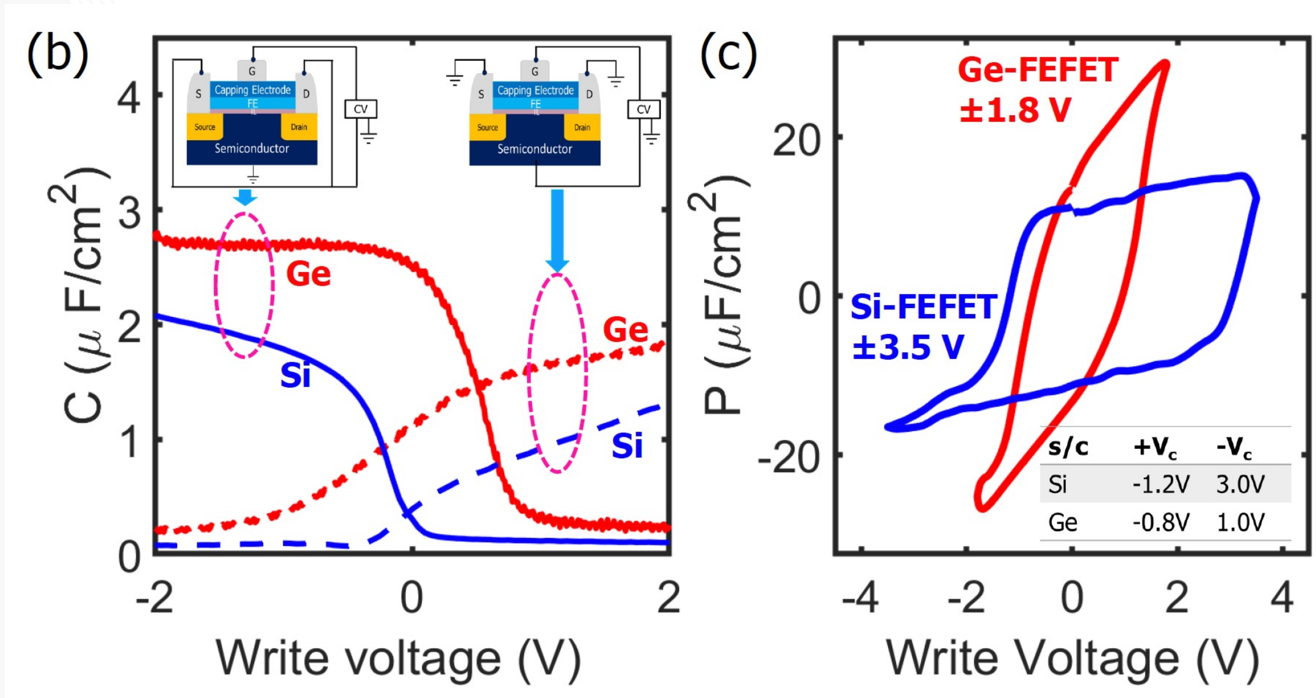
Ge-channel FEFETs with record-low write voltages



Si and Ge-channel FEFETs fabricated with the same 6 nm HZO layers, under similar process and fabrication conditions.

Das et al. A Ge-Channel Ferroelectric Field Effect Transistor with Logic compatible Write Voltage. (under review)

C-V and P-V comparison

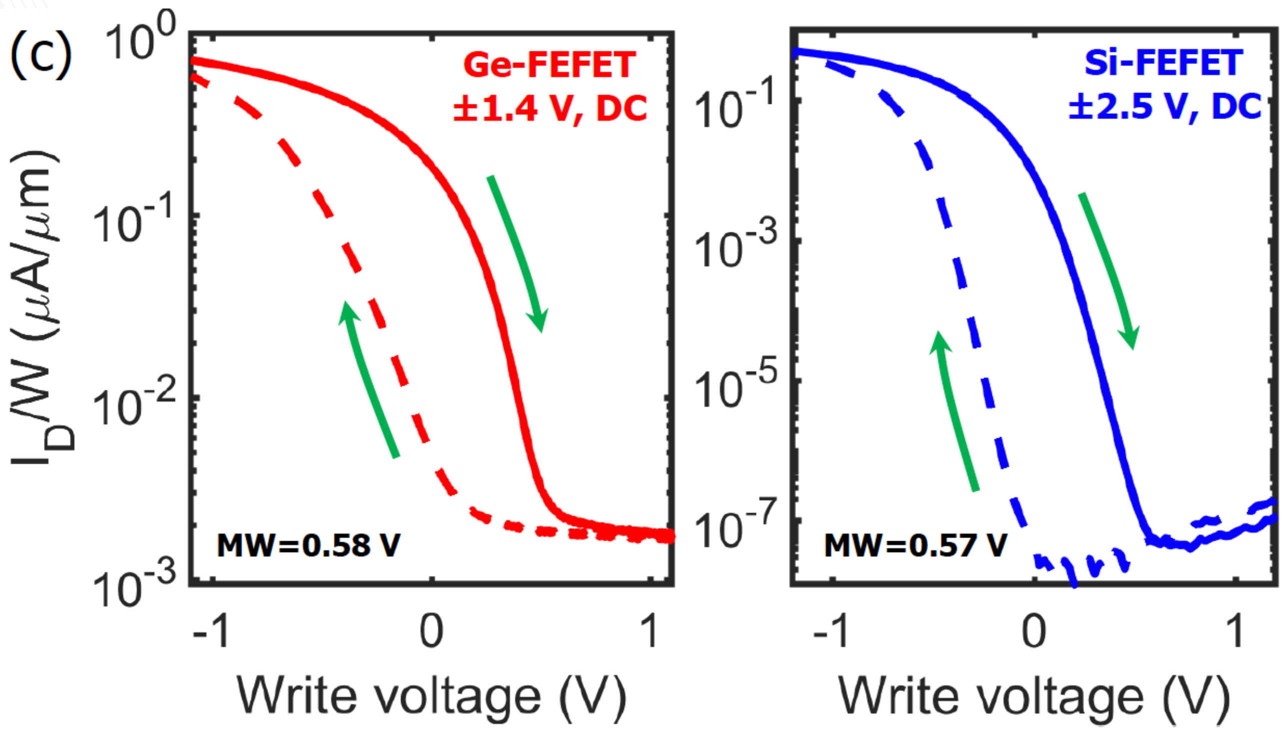


s/c	$+V_c$	$-V_c$
Si	-1.2V	3.0V
Ge	-0.8V	1.0V

Das et al. A Ge-Channel Ferroelectric Field Effect Transistor with Logic compatible Write Voltage. (under review)

Significant increase on the on-capacitance and reduction in coercive voltage in Ge-channel FEFET.

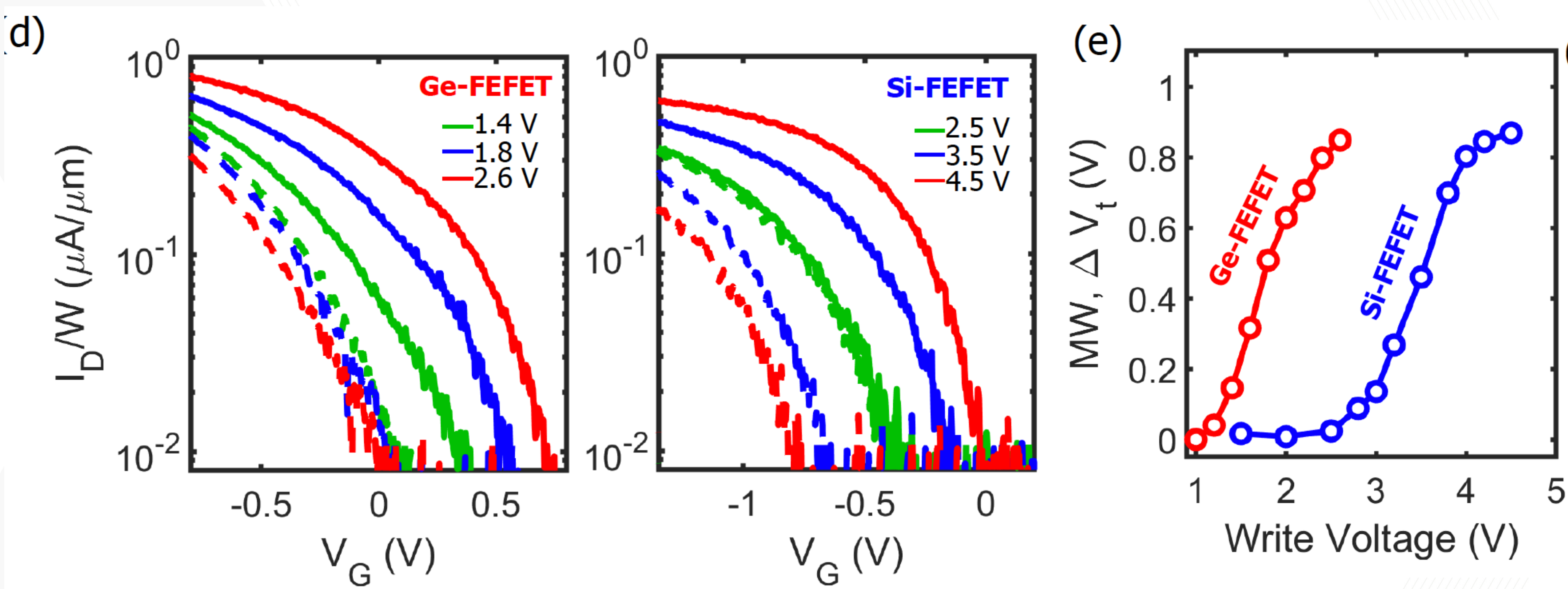
DC I_D-V_G characteristics



Das et al. A Ge-Channel Ferroelectric Field Effect Transistor with Logic compatible Write Voltage. (under review)

Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

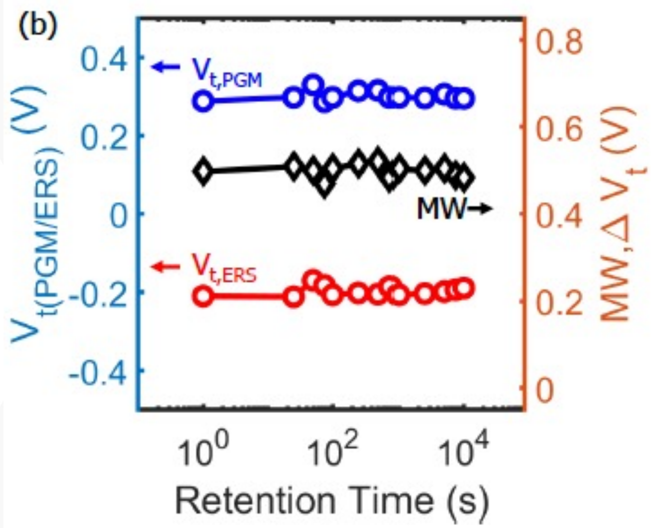
Pulsed I_D-V_G characteristics



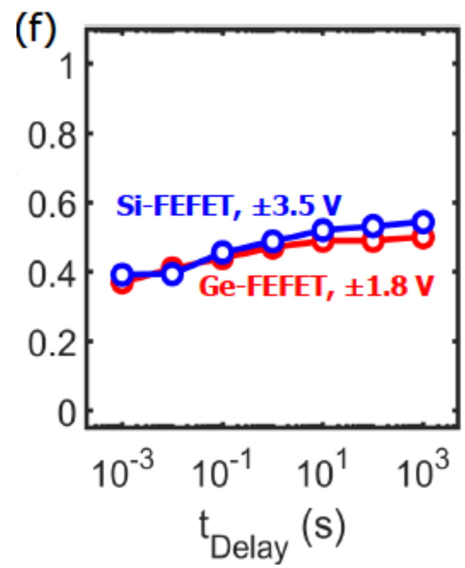
Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

Retention, endurance and read-after-write delay

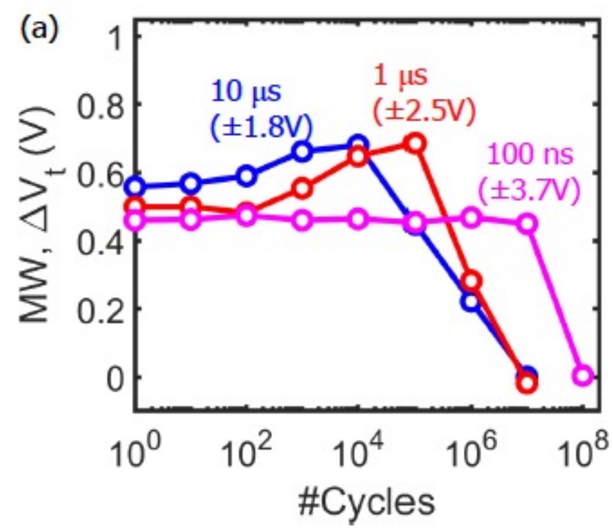
Retention



Read-after-write delay



Endurance

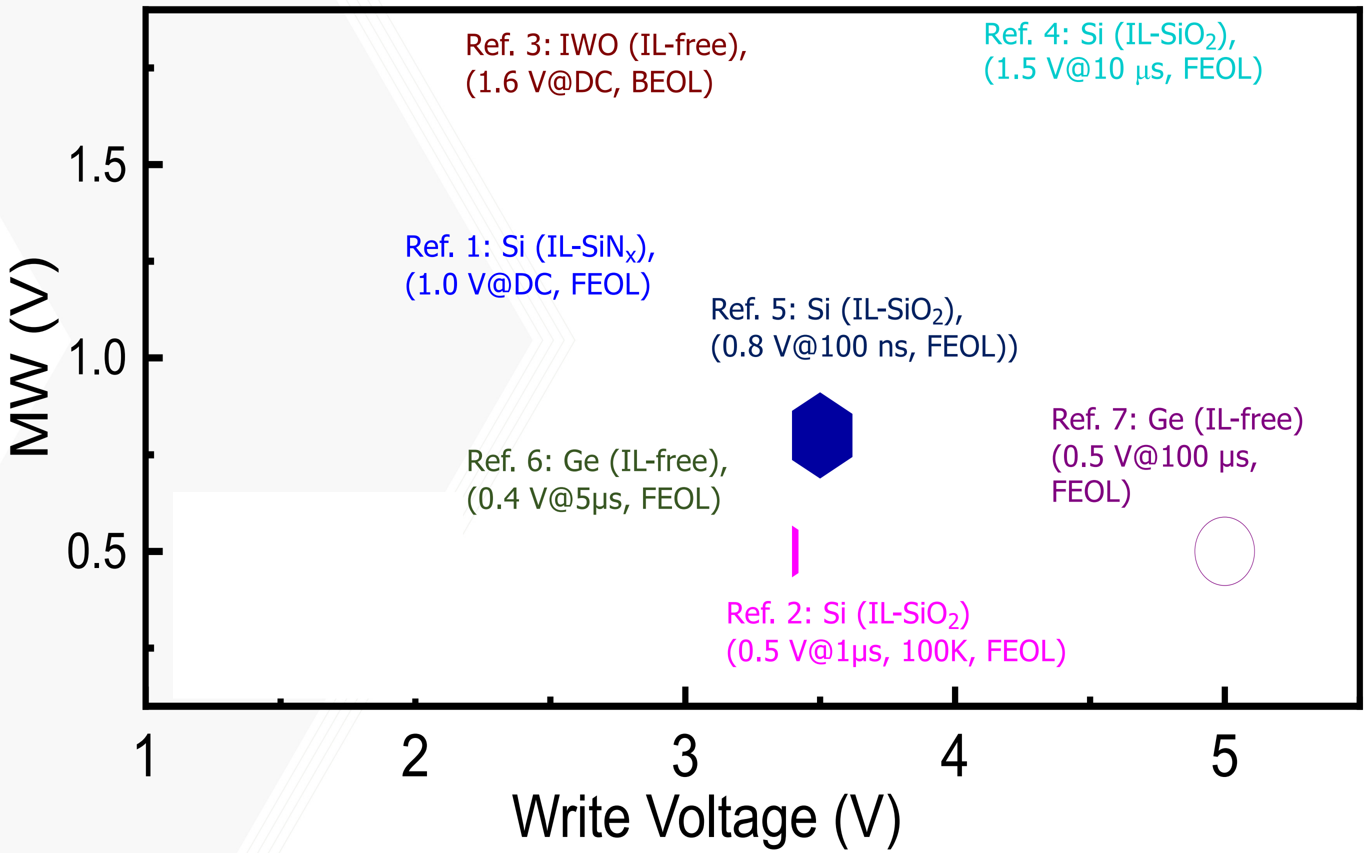


The Ge-FEFET show write endurance of 10^7 cycles, excellent data retention and immediate read-after-write capability.

Das et al. A Ge-Channel Ferroelectric Field Effect Transistor with Logic compatible Write Voltage. (under review)

Georgia Tech
CREATING THE NEXT

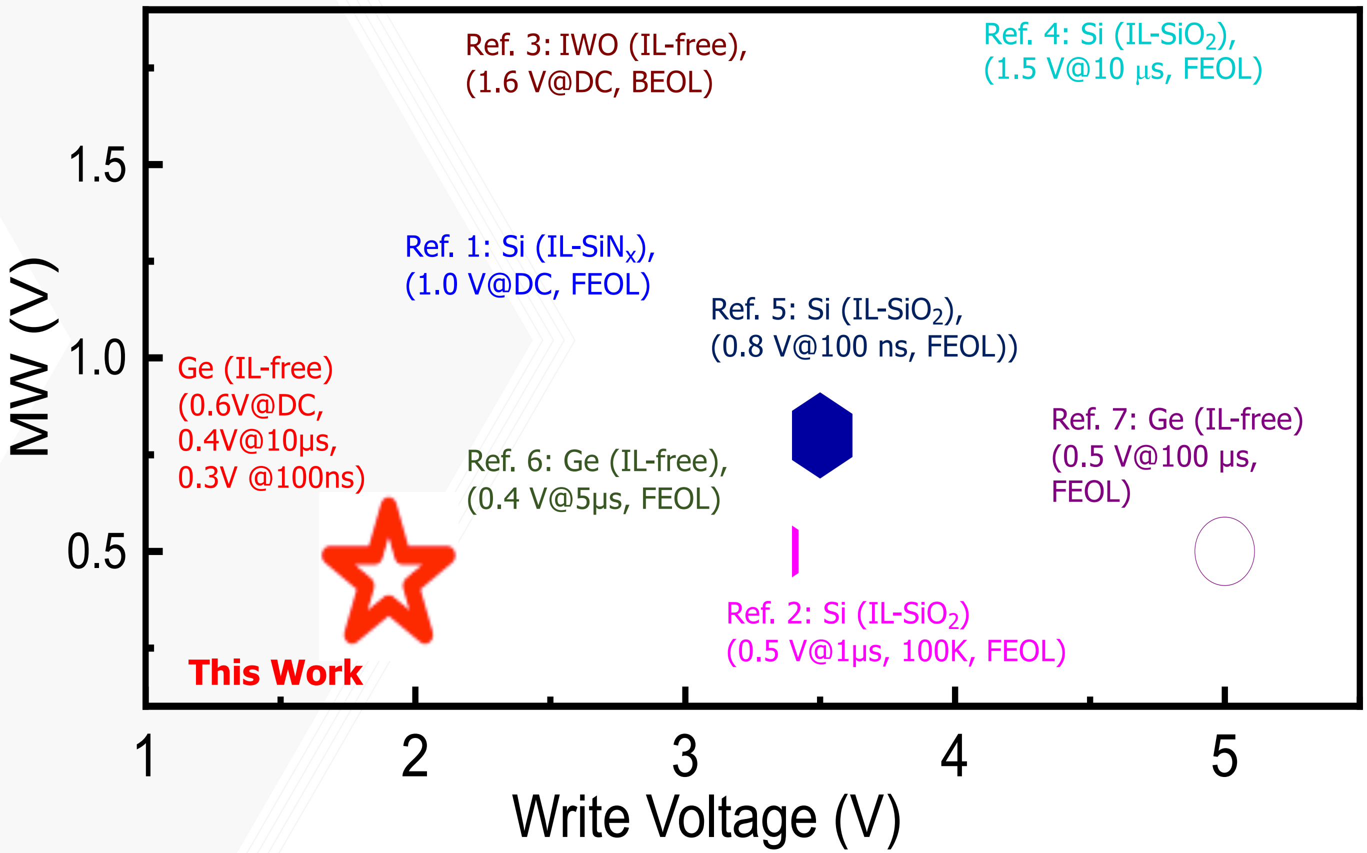
Benchmarking Memory Window v. Write Voltage Tradeoff



[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

Georgia Tech
CREATING THE NEXT

Benchmarking Memory Window v. Write Voltage Tradeoff

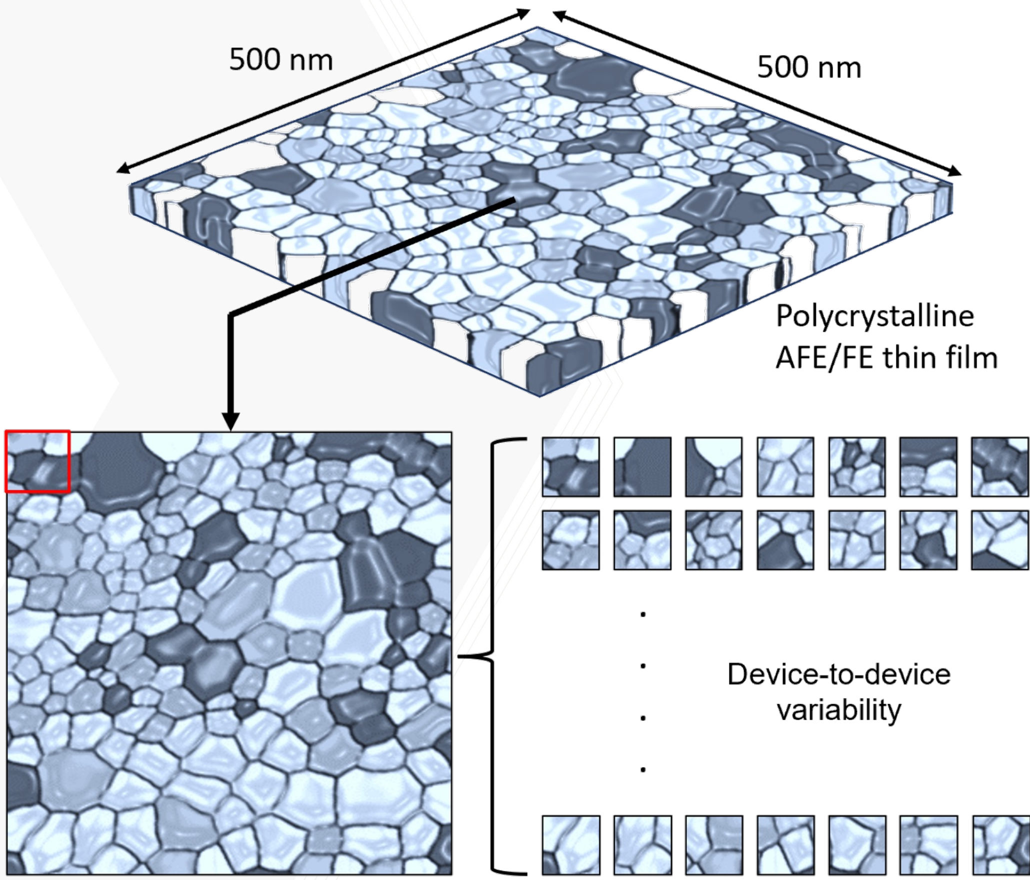


[1] Tan *et al.*, *IEEE EDL*, 42, 994, (2021).
[2] Tan *et al.*, *2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al.*, *IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al.*, *IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al.*, *IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

Take-away #4

There are significant scope for device engineering for application specific needs!

Microstructure in FEFETs



1. Phase (o-, m-, t-)	3. Sub-grain features (domain walls, interphase boundaries)	2. Grain size & orientation

Device-to-device variability

- Applied field causes changes in microstructure
  - Enables multi-level NVM
  - Poses challenges for (VLSI)

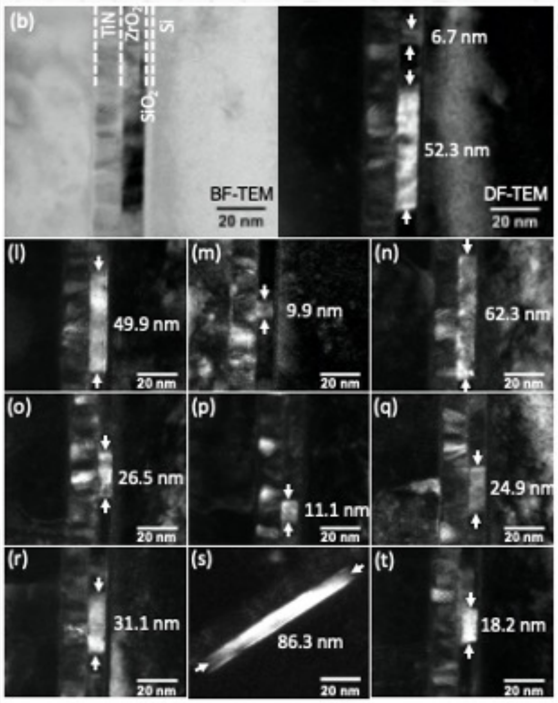
4.
Irreversible change of grain structure electric field cycling

Cycle-to-cycle variability

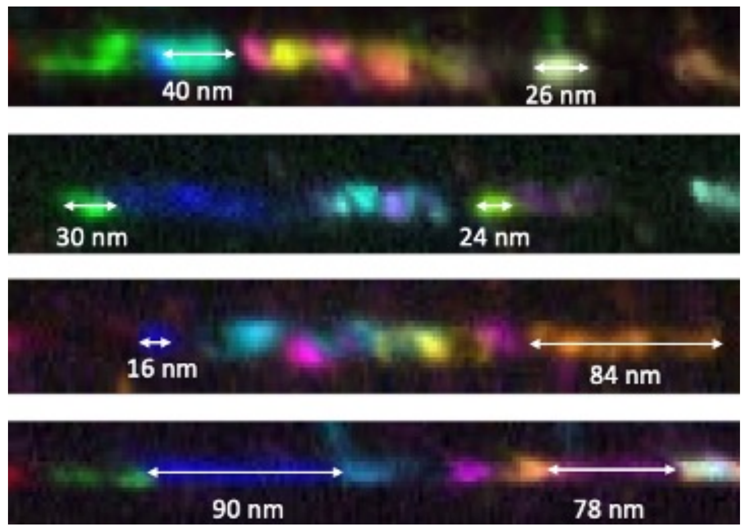
Georgia Tech
CREATING THE NEXT

Quantification of microstructure

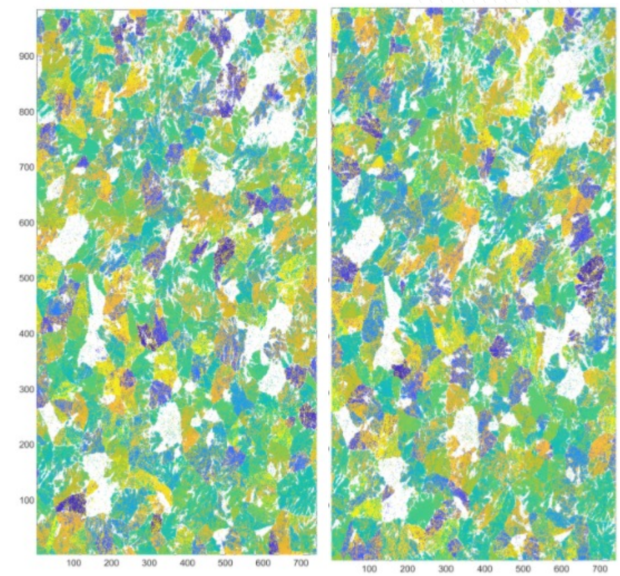
Dark field TEM



Nano-Beam Electron Diffraction (NBED)

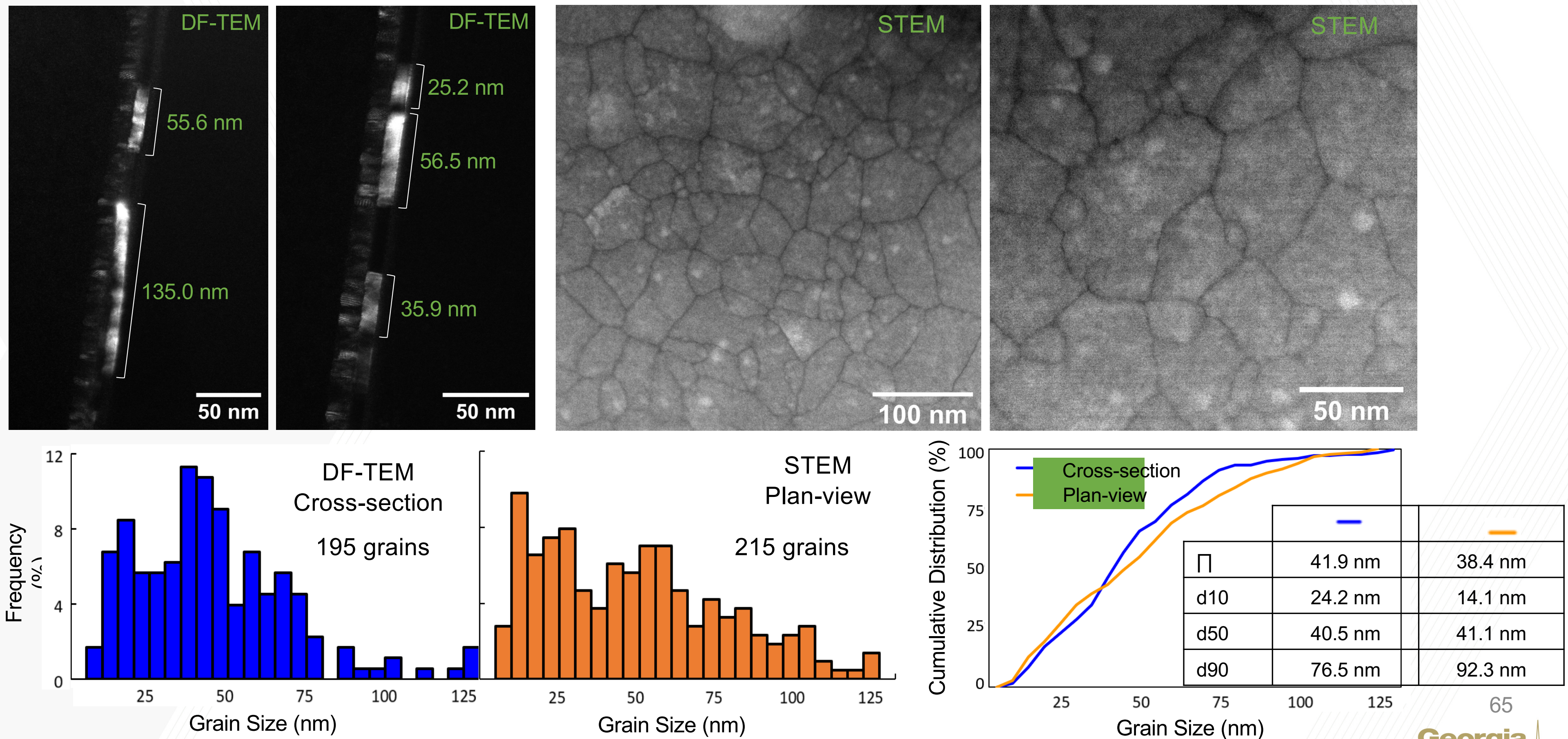


Transmission Kikuchi Diffraction (TKD)



Lombardo, S. F., et al. "Local epitaxial-like templating effects and grain size distribution in atomic layer deposited $Hf_{0.5}Zr_{0.5}O_2$ thin film ferroelectric capacitors." *Applied Physics Letters* 119.9 (2021): 092901.

Quantification of microstructure



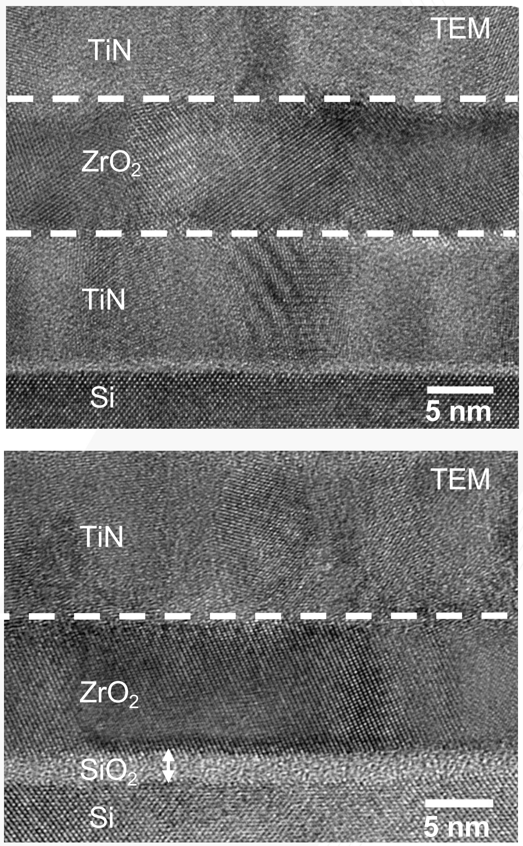
∏	41.9 nm	38.4 nm
d10	24.2 nm	14.1 nm
d50	40.5 nm	41.1 nm
d90	76.5 nm	92.3 nm

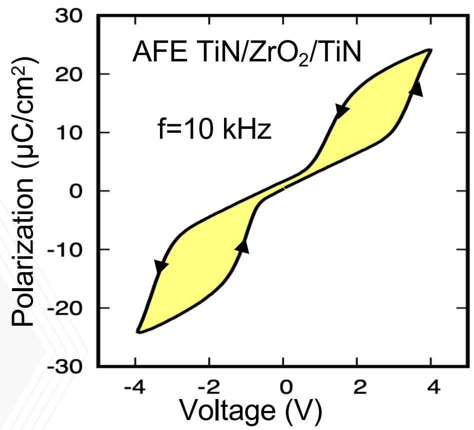
65

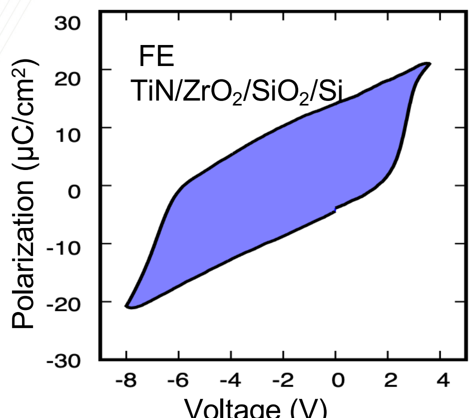
Georgia Tech
CREATING THE NEXT

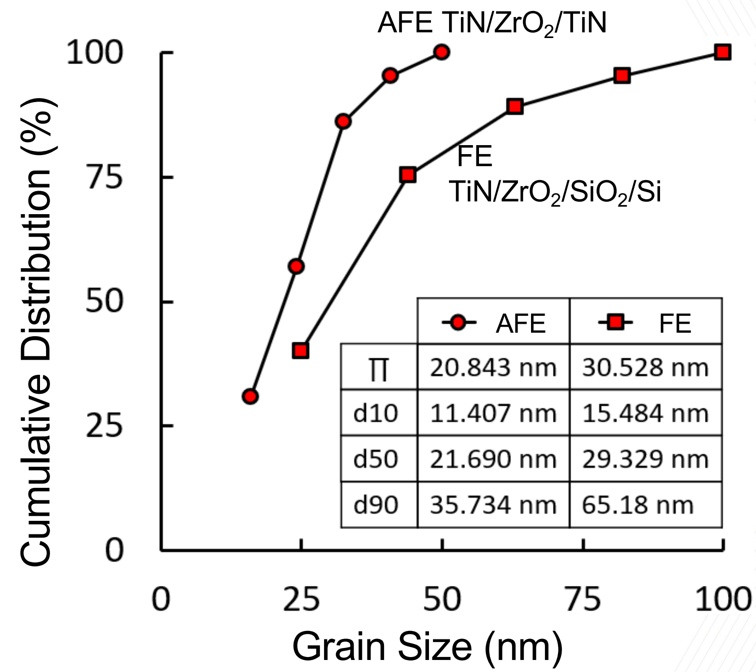
Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

Microstructural origin of AFE and FE in ZrO_2







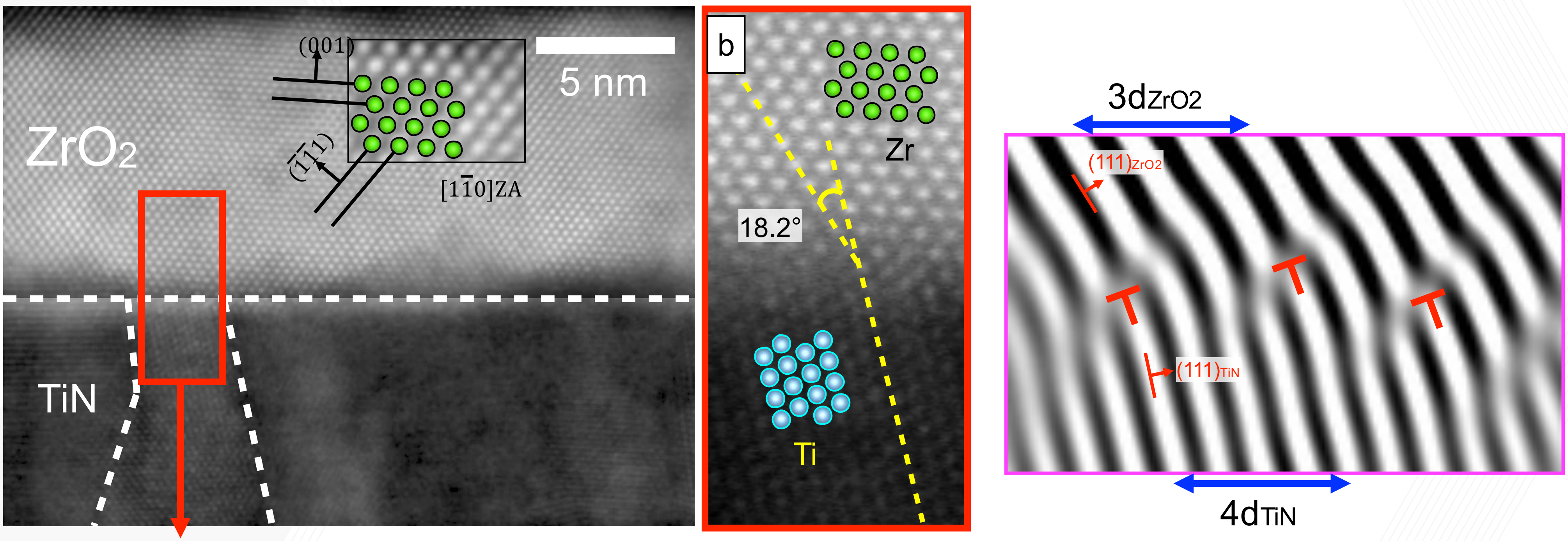


	AFE	FE
Π	20.843 nm	30.528 nm
d10	11.407 nm	15.484 nm
d50	21.690 nm	29.329 nm
d90	35.734 nm	65.18 nm

Smaller grain size favored by Tetragonal phase over FE Orthorhombic phase

Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

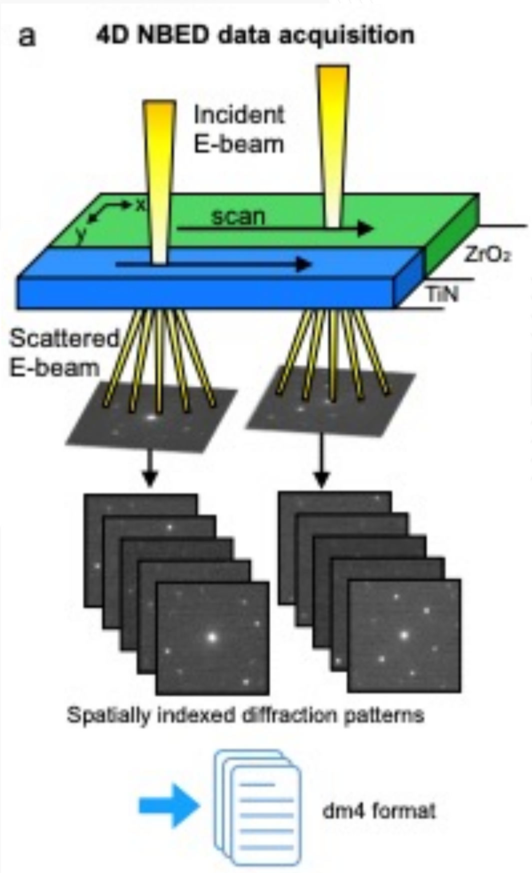
Epitaxial-like templating: Near coincidence site epitaxy

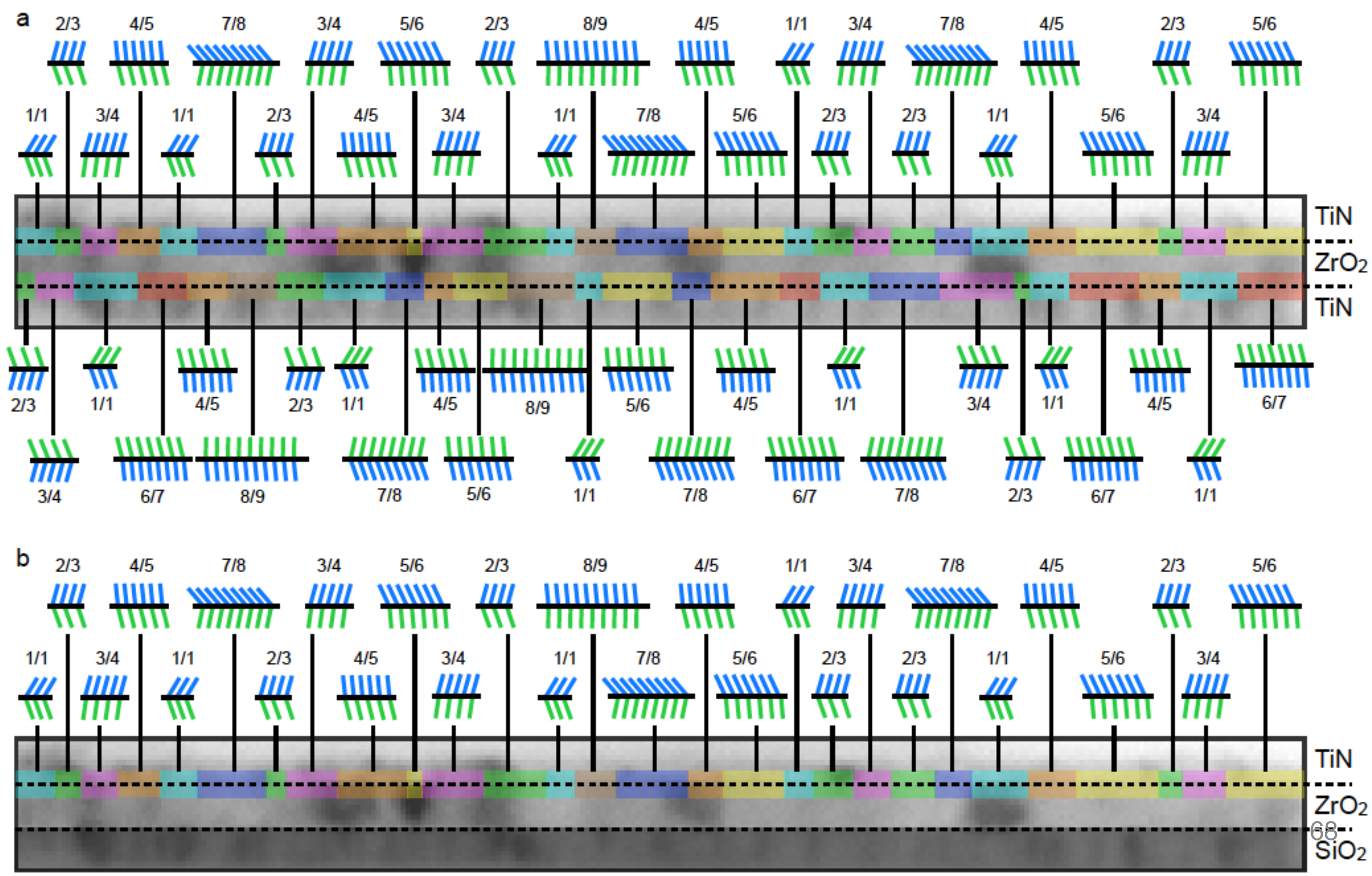


Orientations in TiN and ZrO_2 are often correlated.

Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

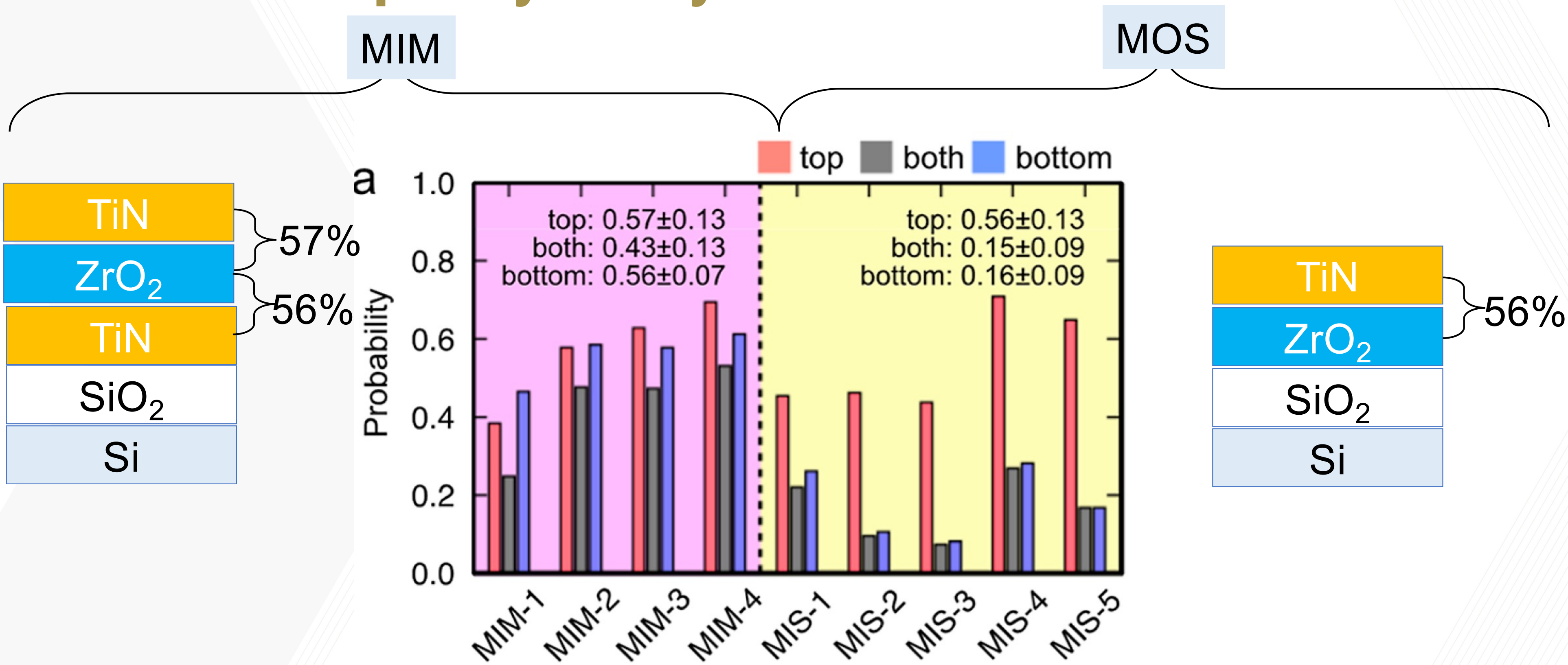
Epitaxial-like templating: Near coincidence site epitaxy





Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

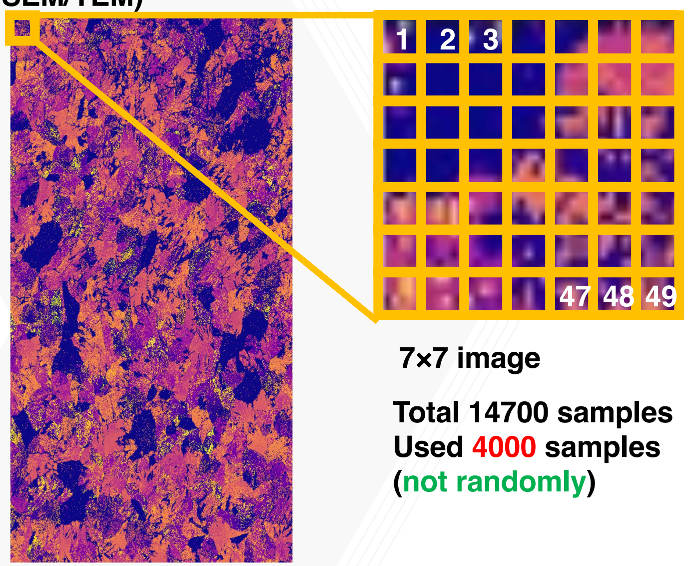
Statistical Epitaxy Analysis via Automated NBED



Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

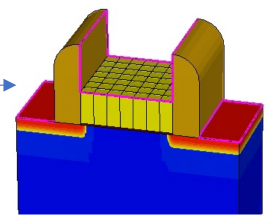
Machine Learning Assisted Predictive TCAD Modeling (from Metrology to Device Metrics)

Ferro polarization map (from TKD data from SEM/TEM)



7×7 image

Total 14700 samples
Used 4000 samples
(not randomly)



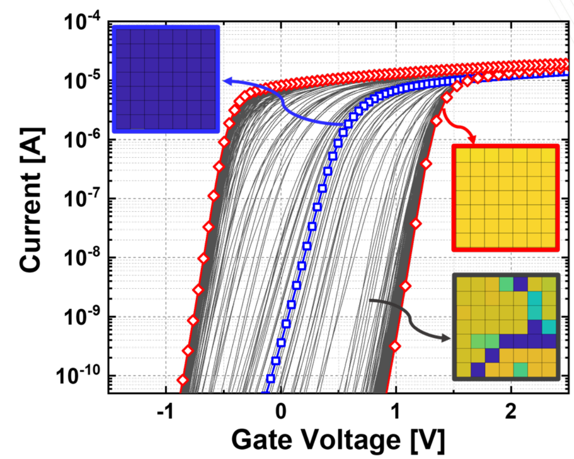


TABLE II. Average, 3-sigma and percentage of prediction error

	TCAD	ML-based prediction		
	μ	μ	3σ	Error
HVT [V]	1.05	1.05	0.08	**1.2%**
LVT [V]	–0.53	–0.53	0.07	**2.0%**
I_{on} [μA]	6.68	6.68	1.01	**2.1%**
SS [mV/dec]	94.52	94.48	9.0	**1.6%**

G. Choe, P. V. Ravindran, A. Lu, J. Hur, M. Lederer, A. Reck, S. Lombardo, N. Afroze, J. Kacher, A. I. Khan, S. Yu, "Machine learning assisted statistical variation analysis of ferroelectric transistors: from experimental metrology to predictive modeling," IEEE Symposium on VLSI Technology and Circuits (VLSI) 2022.

Georgia Tech
CREATING THE NEXT

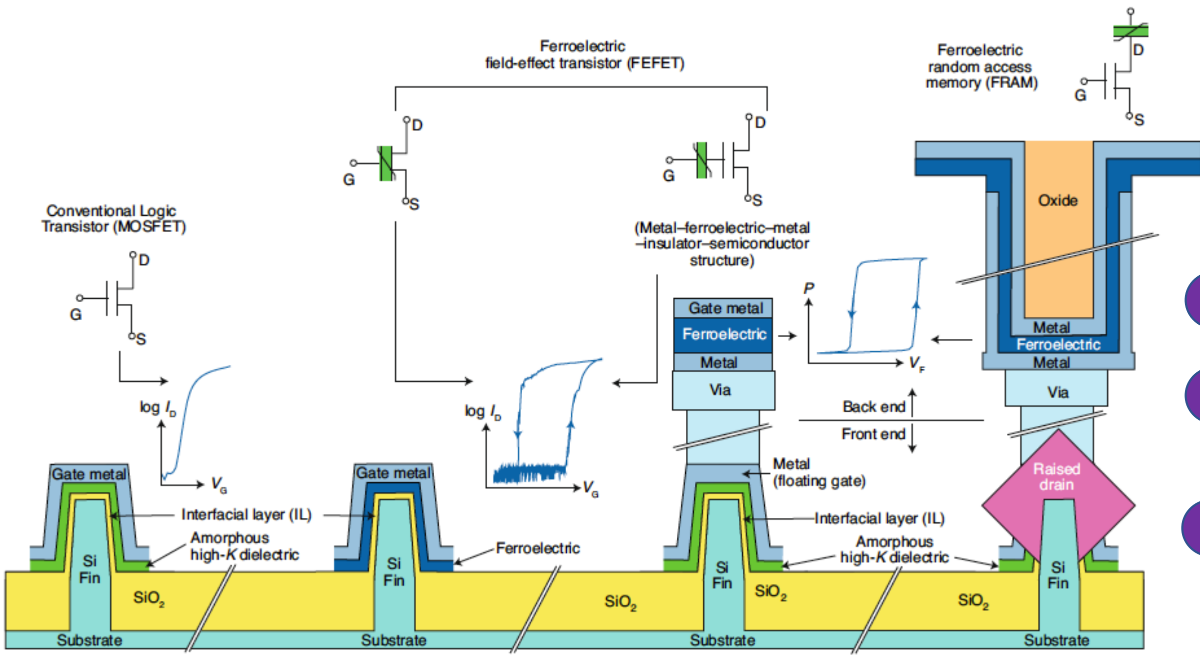
Take-away #5

More work needed to correlate the microstructure with the electrical characteristics of ferroelectric devices.

Georgia Tech
CREATING THE NEXT

The era of ferroelectronics

The next wave of exponential growth of the semiconductor industry depends on how well the electronic hardware can support the explosion of data-centric computing.



Ferroelectric technology will be a key component because of

1. Performance
2. Energy and area efficiency
3. Logic and memory functionalities

Georgia Tech CREATING THE NEXT

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

Thank you

Semiconductor
Research
Corporation