Ferroelectric field-effect transistors: Logic compatibility and microstructure

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3/9/2023


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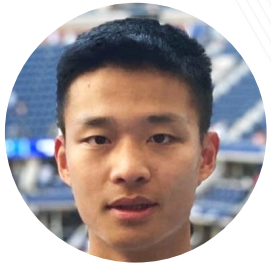

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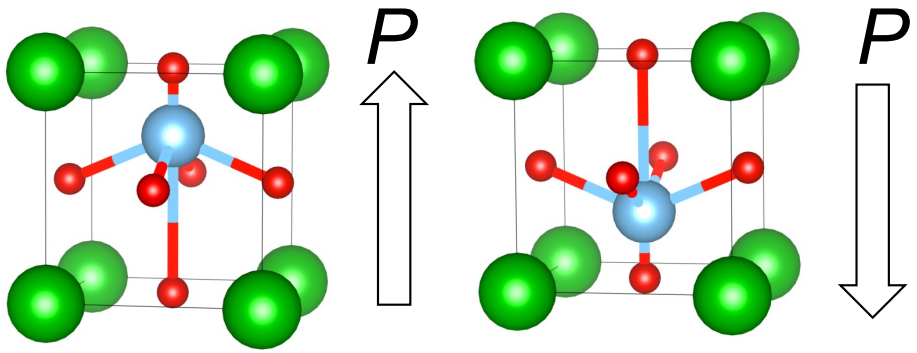
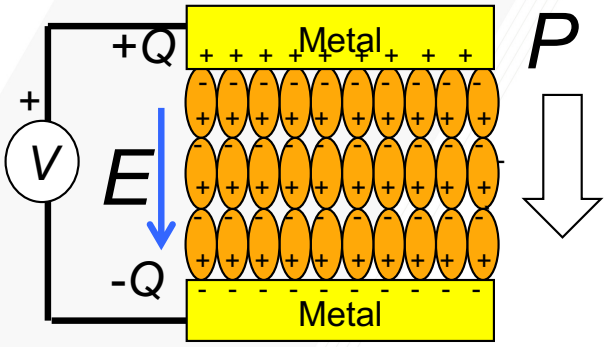
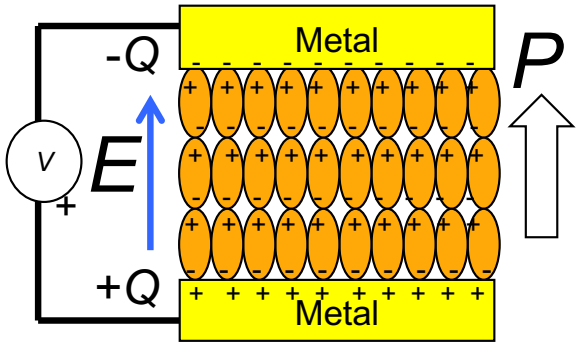
Ferroelectricity

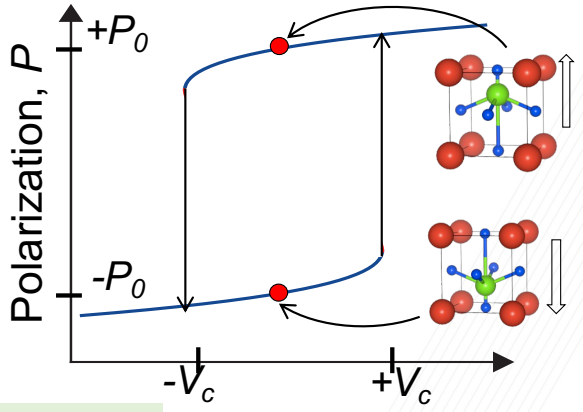
Classical Ferroelectric
$PbTiO_3$, $BaTiO_3$ etc.

Emerging CMOS compatible
Ferroelectrics:
Doped HfO_2









A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

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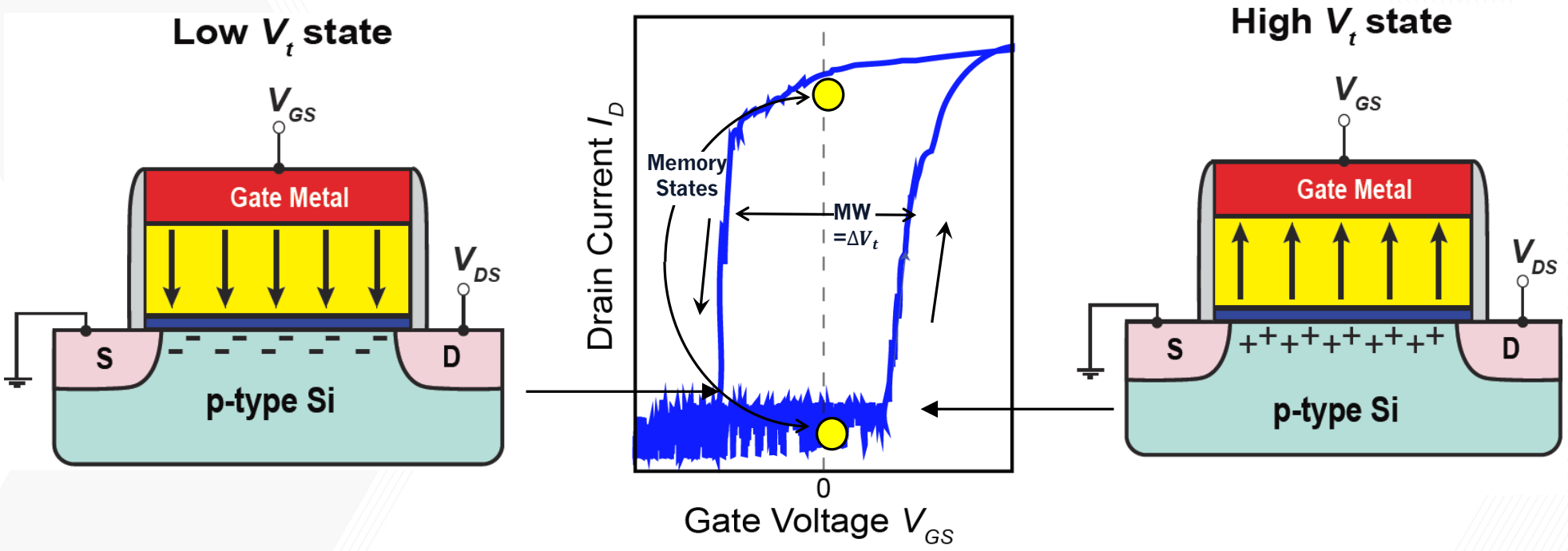
Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET wherein the threshold voltage gets shifted by the direction and magnitude of the "remnant" polarization.

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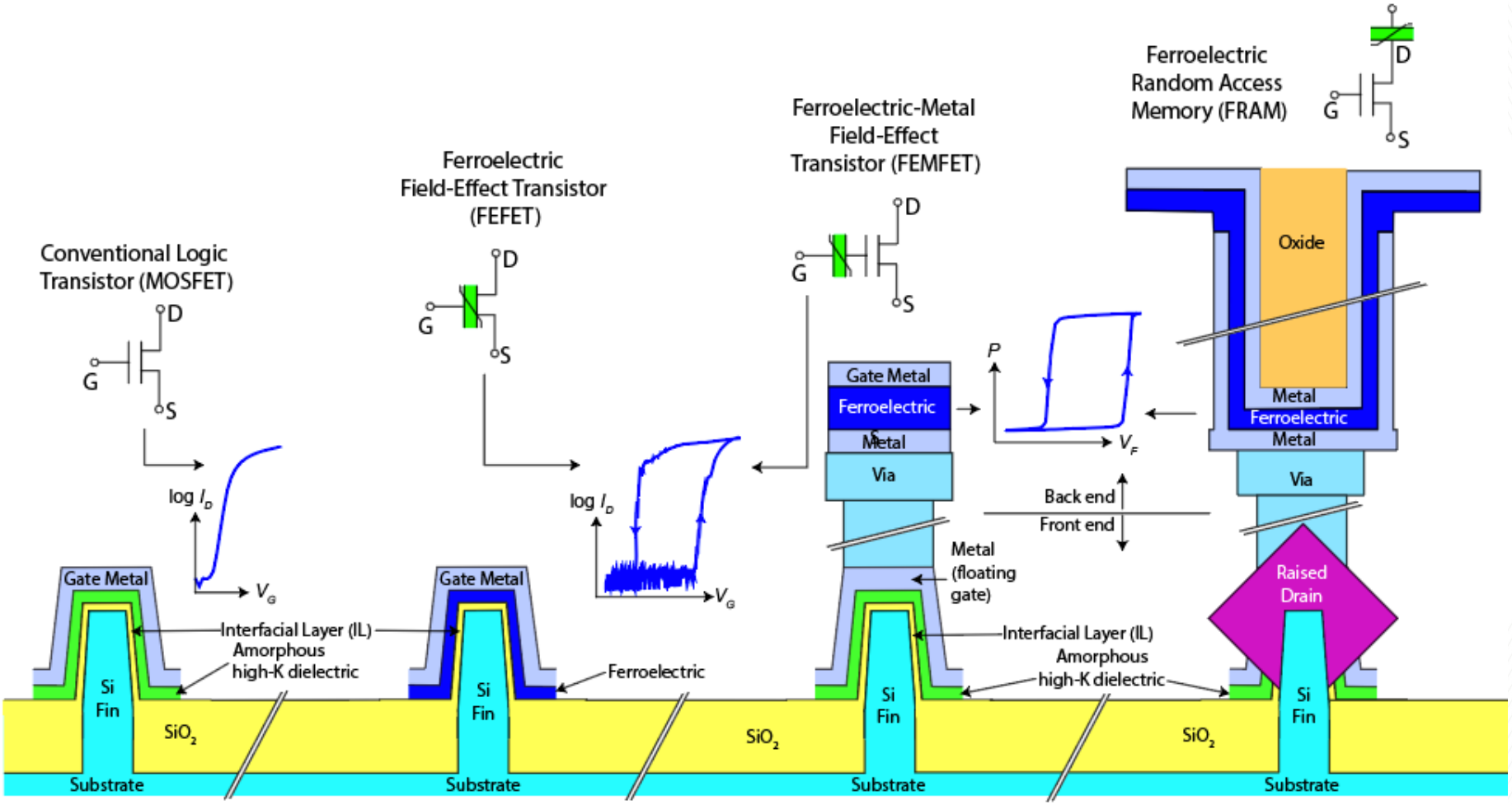
Ferroelectric devices (1 of 2)



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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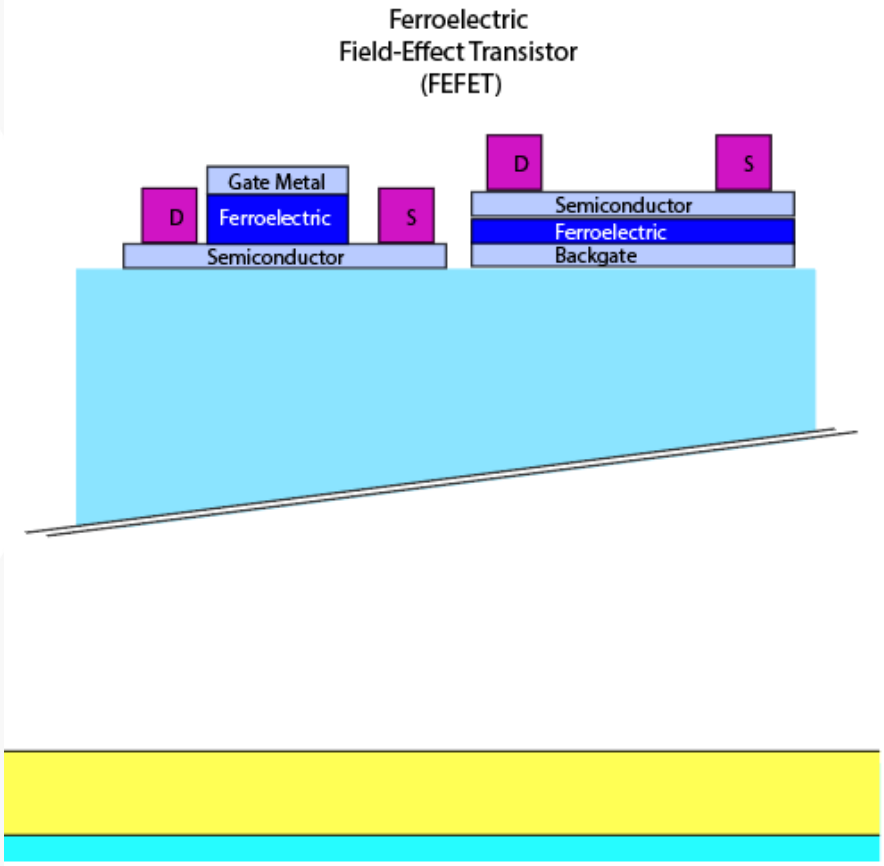
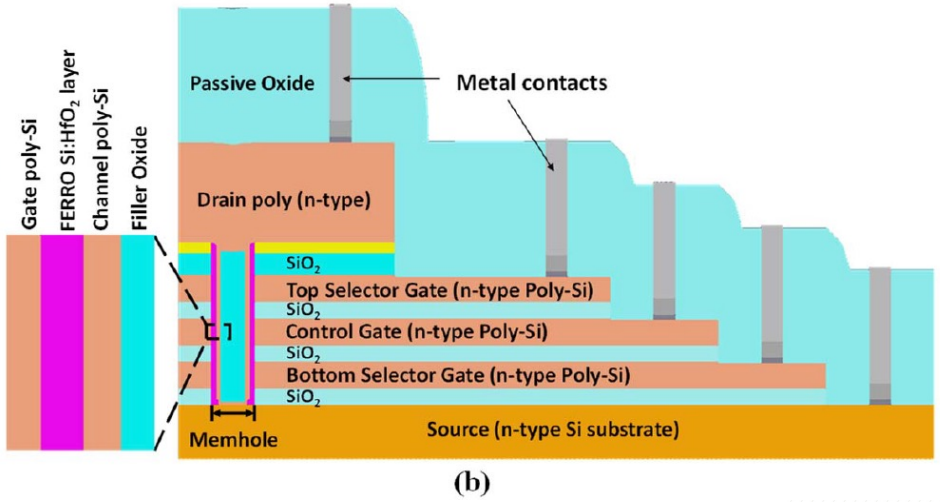
Ferroelectric devices (2 of 2)

BEOL FEFET



Vertical FEFET for NAND Storage



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FEFET as an embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM[70]	eFlash (FG)	eFlash (SG MONOS)[42]	eFlash (SONOS)[41]	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based)[67]
Cell size	120–150F^2	40F^2	40–60F^2	40–50F^2	50–60F^2	10–30F^2	10–30F^2	30–40F^2	50–60F^2
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 µs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	>10^{16}	>10^{16}	~10^4	~10^5	~10^6	10^5–10^9	>10^{10}	>10^{12}	>10^{14}

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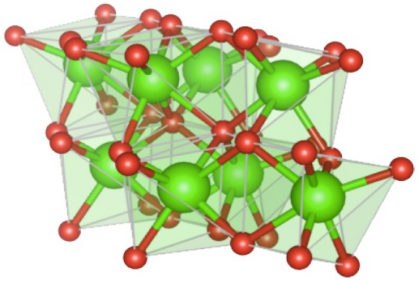
Ferroelectric field-effect transistors (FEFETs)

Ferroelectric Oxide



Properties of Ferroelectric oxides

- Non-volatility and hysteresis
- Plasticity, Meta-plasticity and Anti-plasticity
- Negative dielectric permittivity/negative capacitance
- Stochasticity

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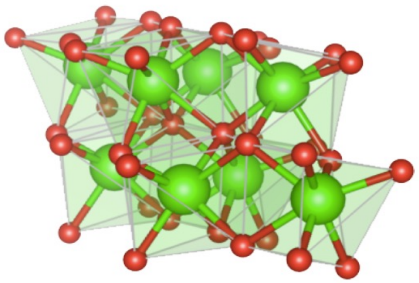
Ferroelectric field-effect transistors (FEFETs)

Ferroelectric Oxide



Properties of Ferroelectric oxides

- Non-volatility and hysteresis
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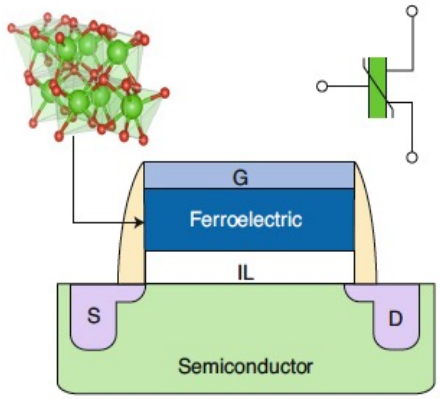
Properties enabled by a transistor structure

- Transistor physics
- Transconductance gain
- Circuit-level design

Ferroelectric field-effect transistor



Ferroelectric FET is one of most versatile transistor technologies – ever conceived.

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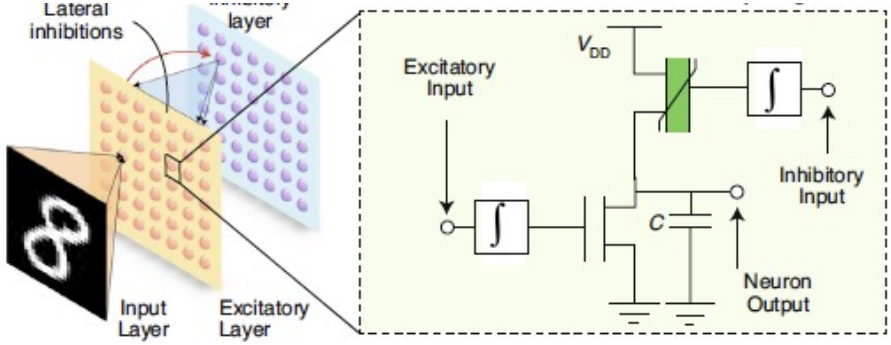
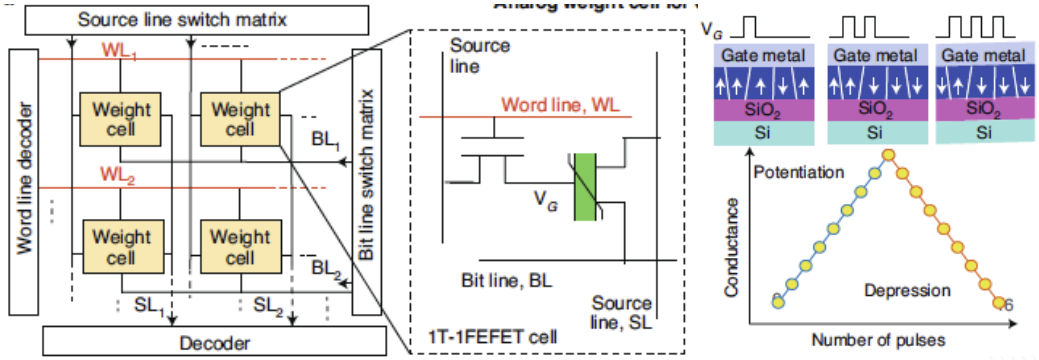
Ferroelectric FET Applications

Ferroelectric neurons for spiking neural networks



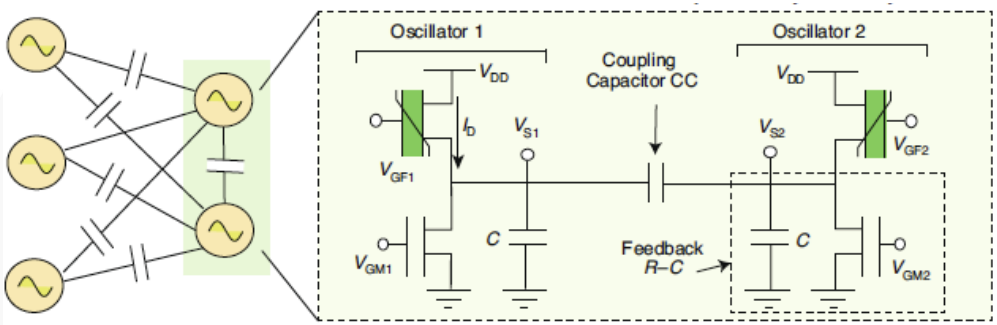
Wang et al. Int. Electron Dev. Meeting (IEDM) 2018.

FE synapses for deep neural network accelerators



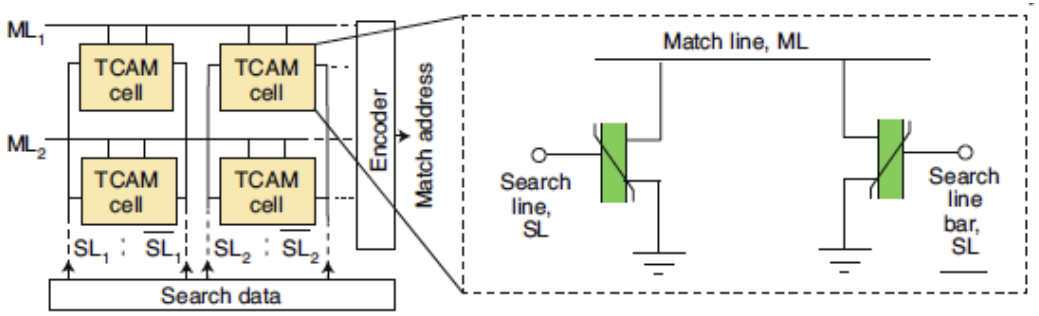
Aabrar et al. VLSI Symp. 2022.

Ferroelectric oscillators for time dynamical systems



Z. Wang et al. EDL 2017

Ferroelectric content addressable memory (CAM)



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Progress in FEFET technology

1 Write voltage and Memory Window	2 Read/Write Speed	3 Device-to-device variation	4 Reliability and endurance
Specs			
<1.5 V write voltage >0.5 V memory window	<10 ns write speed <10 ns read-after-write delay	$\Delta V_{t,3\sigma} =$ 20-50 mV (7 nm node)	>10^{12} cycles

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Progress in FEFET technology

1	2	3	4
Write voltage and Memory Window	Read/Write Speed	Device-to-device variation	Reliability and endurance

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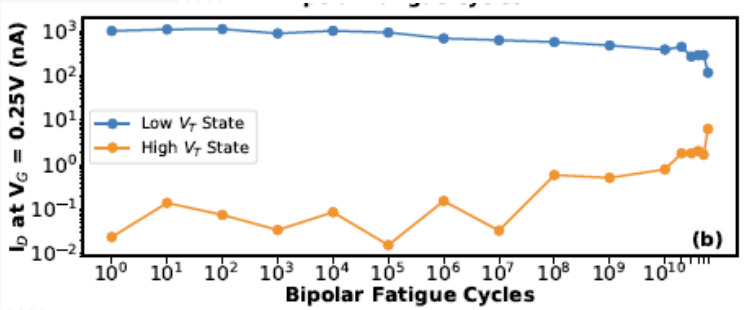
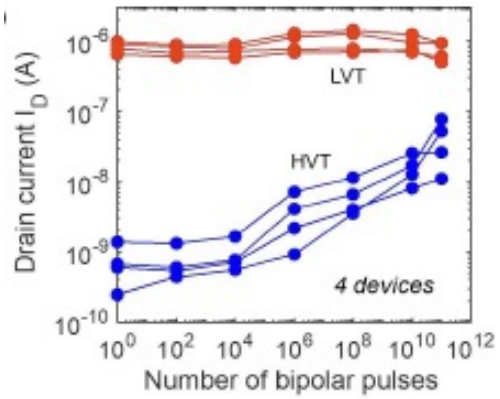


Tan et al. IEEE EDL 42, 994 (2021).



Dutta et al. IEEE EDL 43, 383 (2022).

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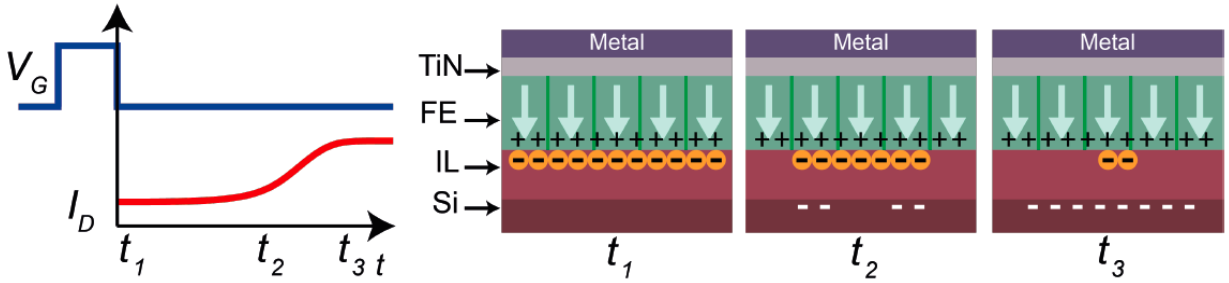

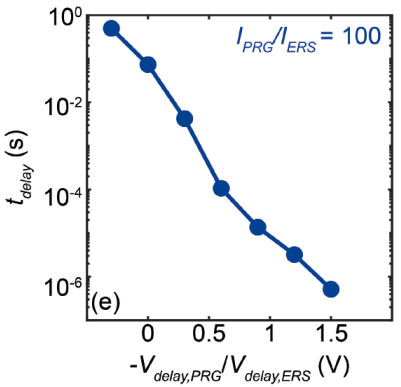

Wang, Z., Tasneem, N., Hur, J., Chen, H., Yu, S., Chern, W., & Khan, A. (2021, December). Standby bias improvement of read after write delay in ferroelectric field effect transistors. In *2021 IEEE International Electron Devices Meeting (IEDM)* (pp. 19-3). IEEE.

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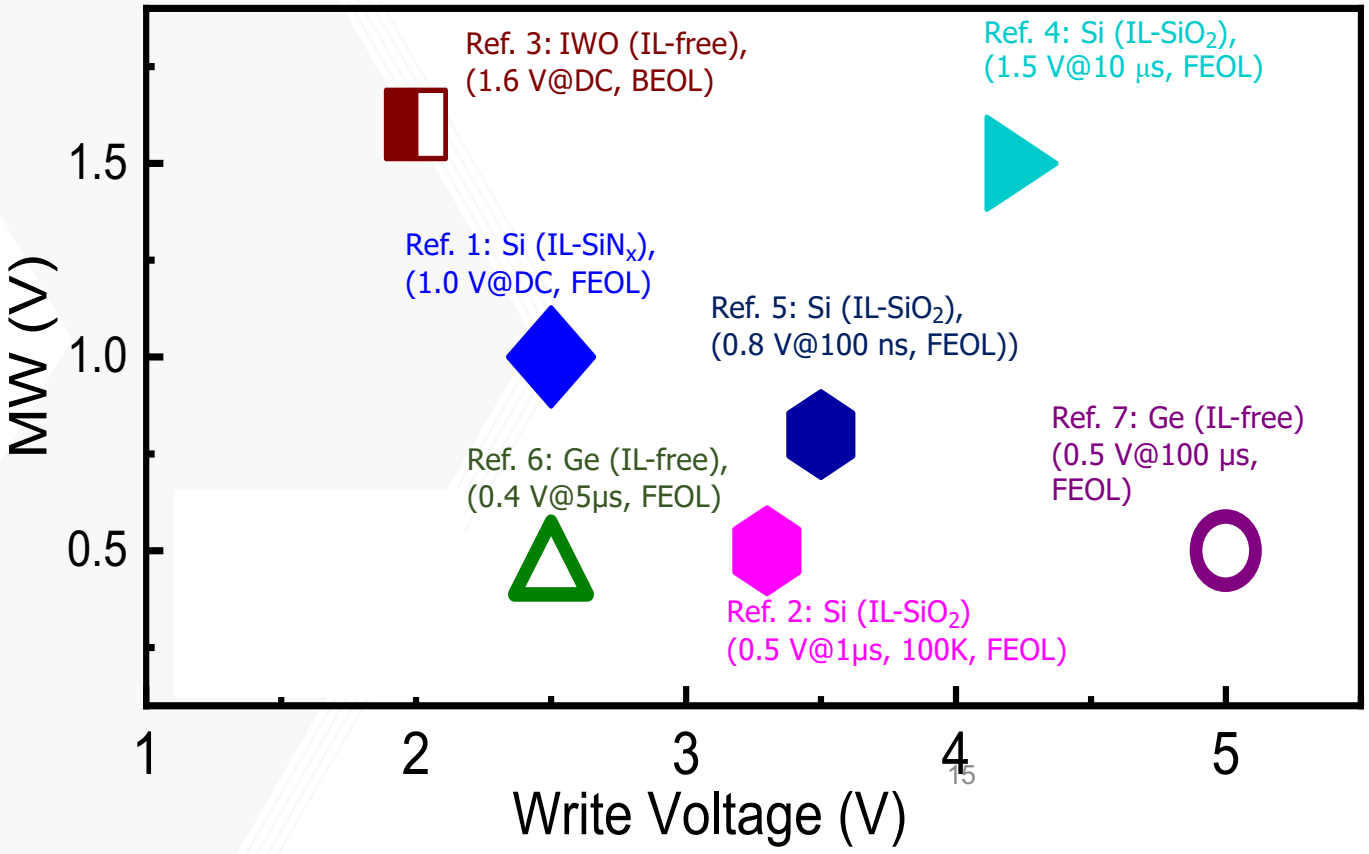
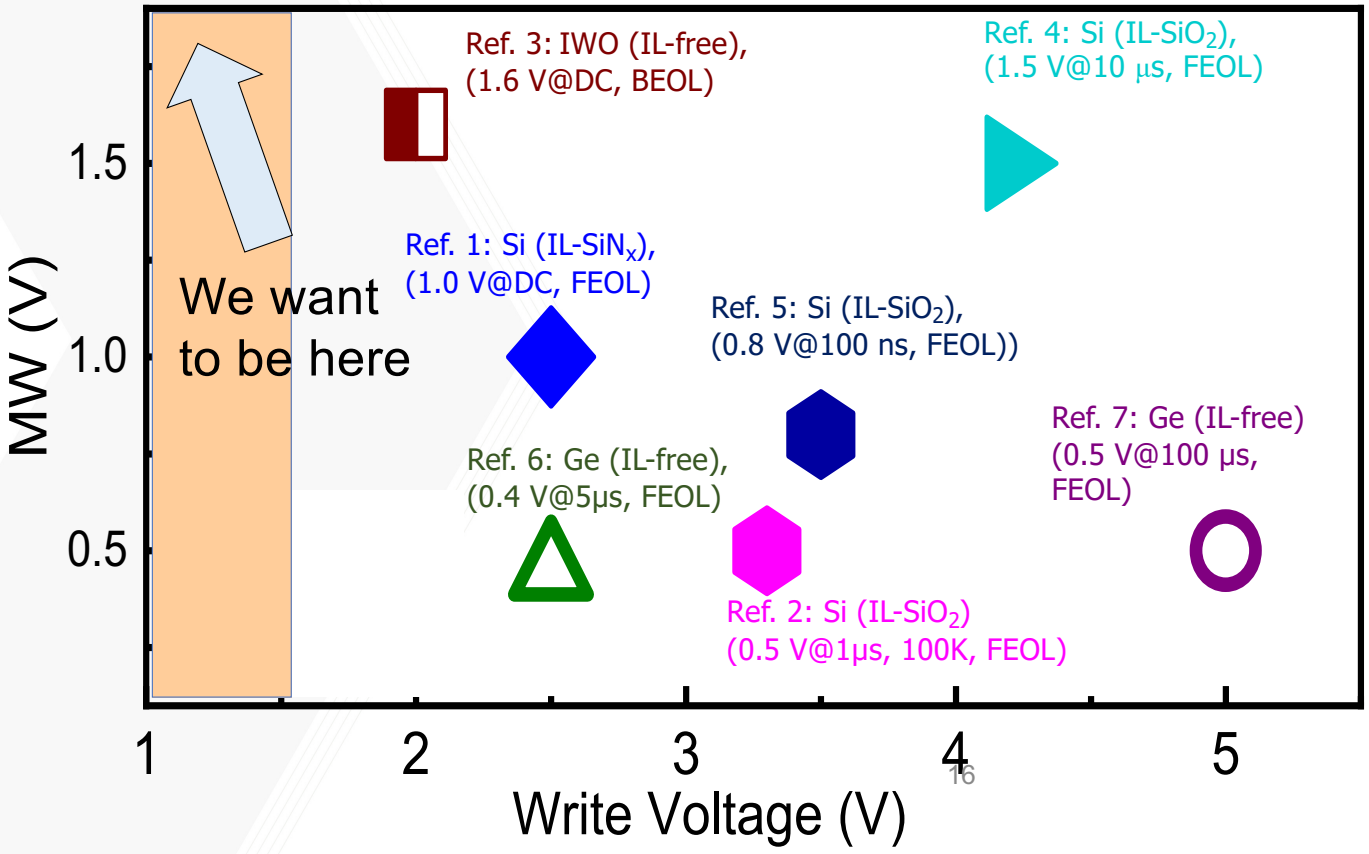
Benchmarking Memory Window v. Write Voltage Tradeoff



[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

Benchmarking Memory Window v. Write Voltage Tradeoff



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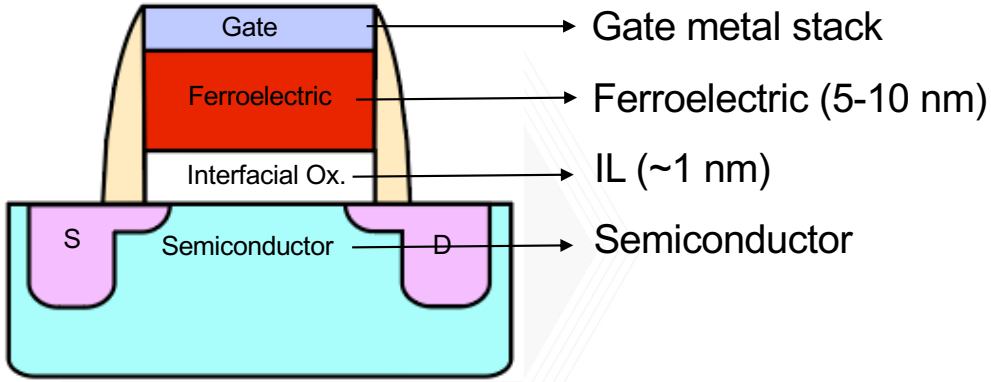
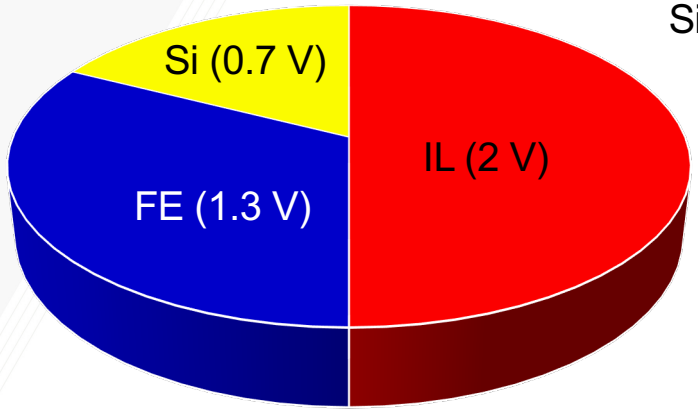
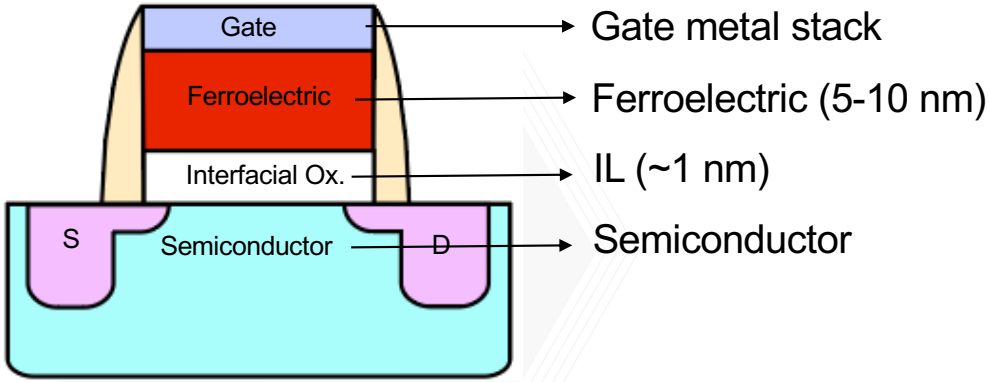
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

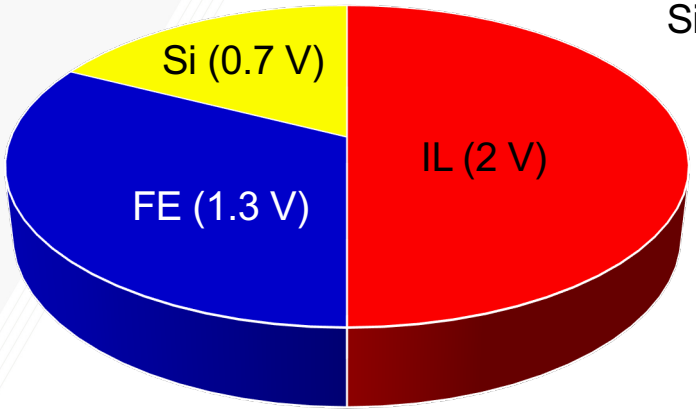
Write voltage vs. memory window trade-off

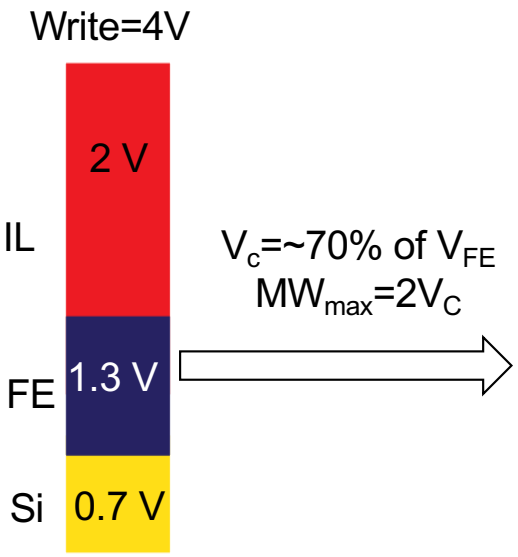


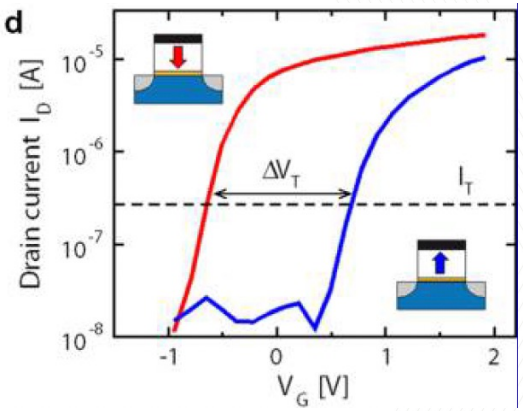


Write voltage vs. memory window trade-off









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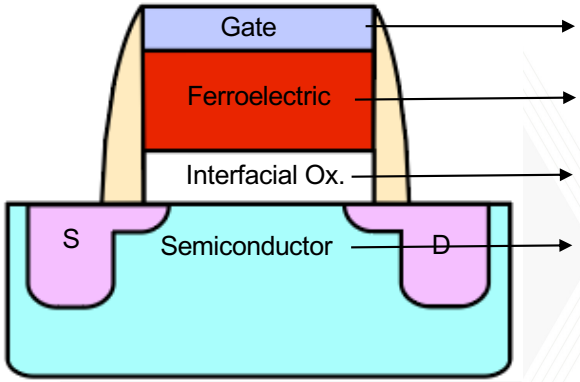
Write voltage vs. memory window trade-off

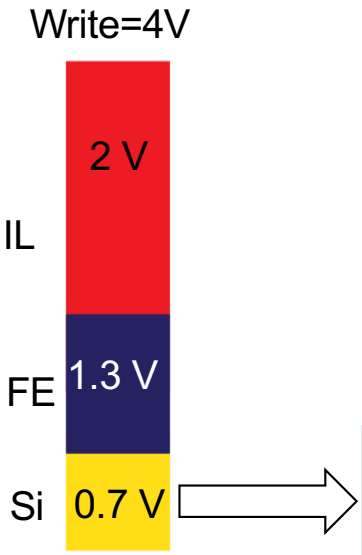


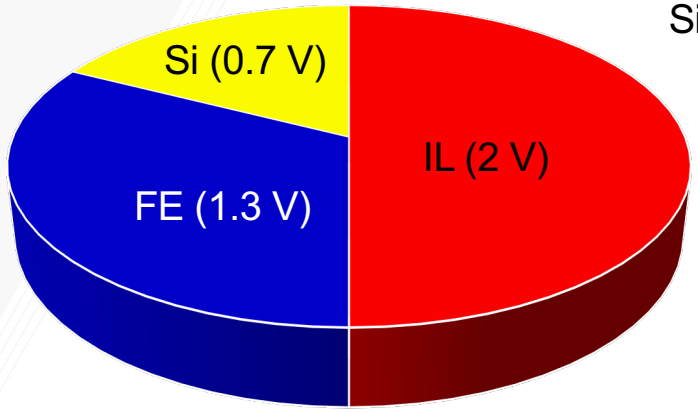
Gate metal stack

Ferroelectric (5-10 nm)

IL (~1 nm)

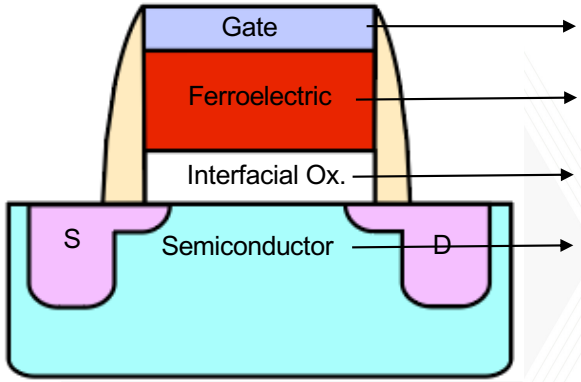
Semiconductor





Changing the band-gap of the semiconductor By changing the channel material from Si to SiGe or Ge.

Write voltage vs. memory window trade-off



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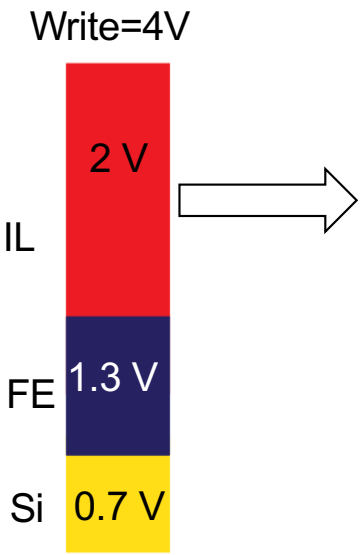
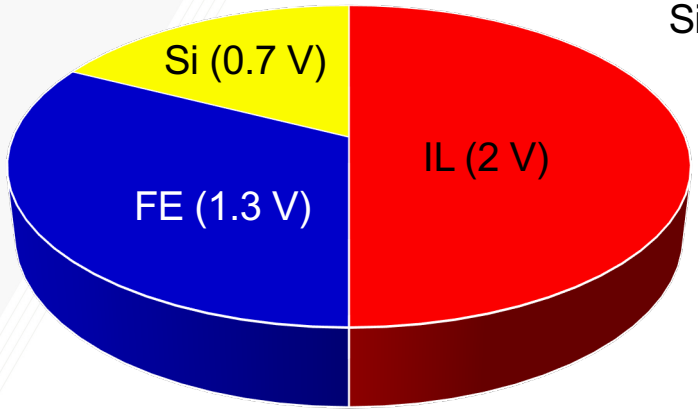
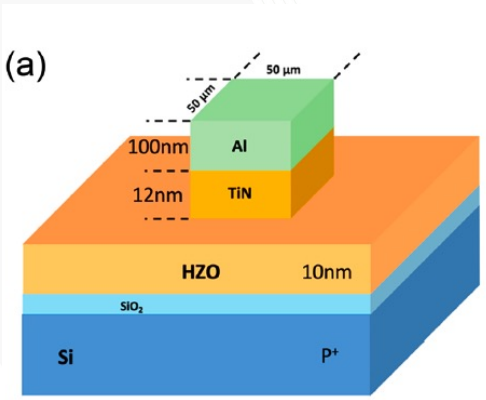




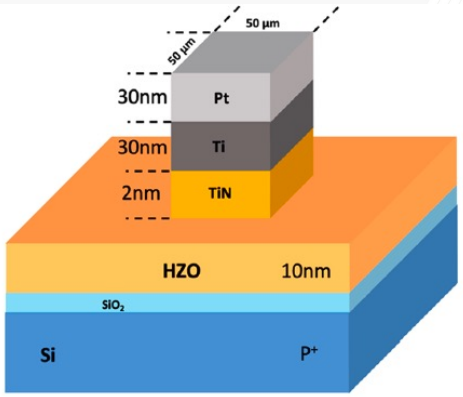
Reducing the thickness of the IL or increasing the K of the IL.

Reliability degradation is a concern.

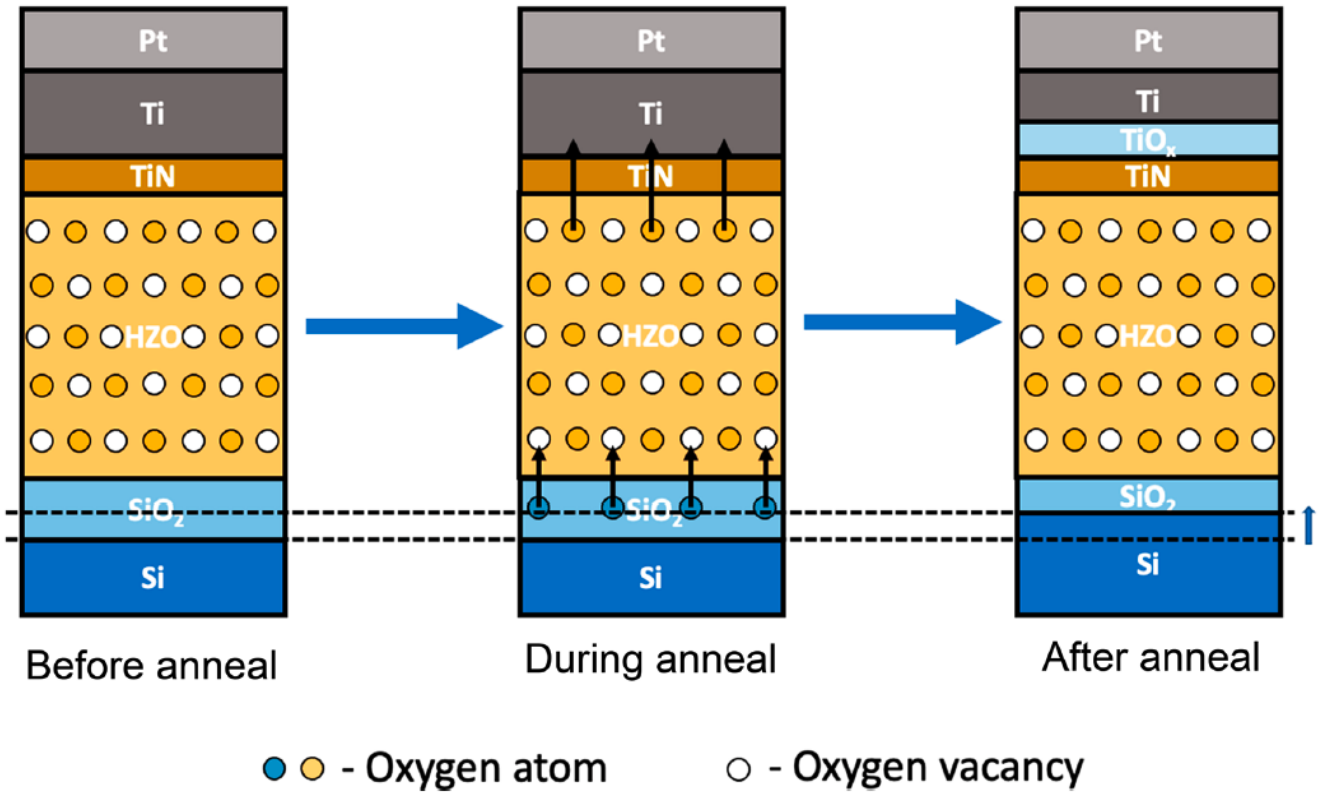
Remote oxygen scavenging to reduce IL thickness



Non-Scavenging

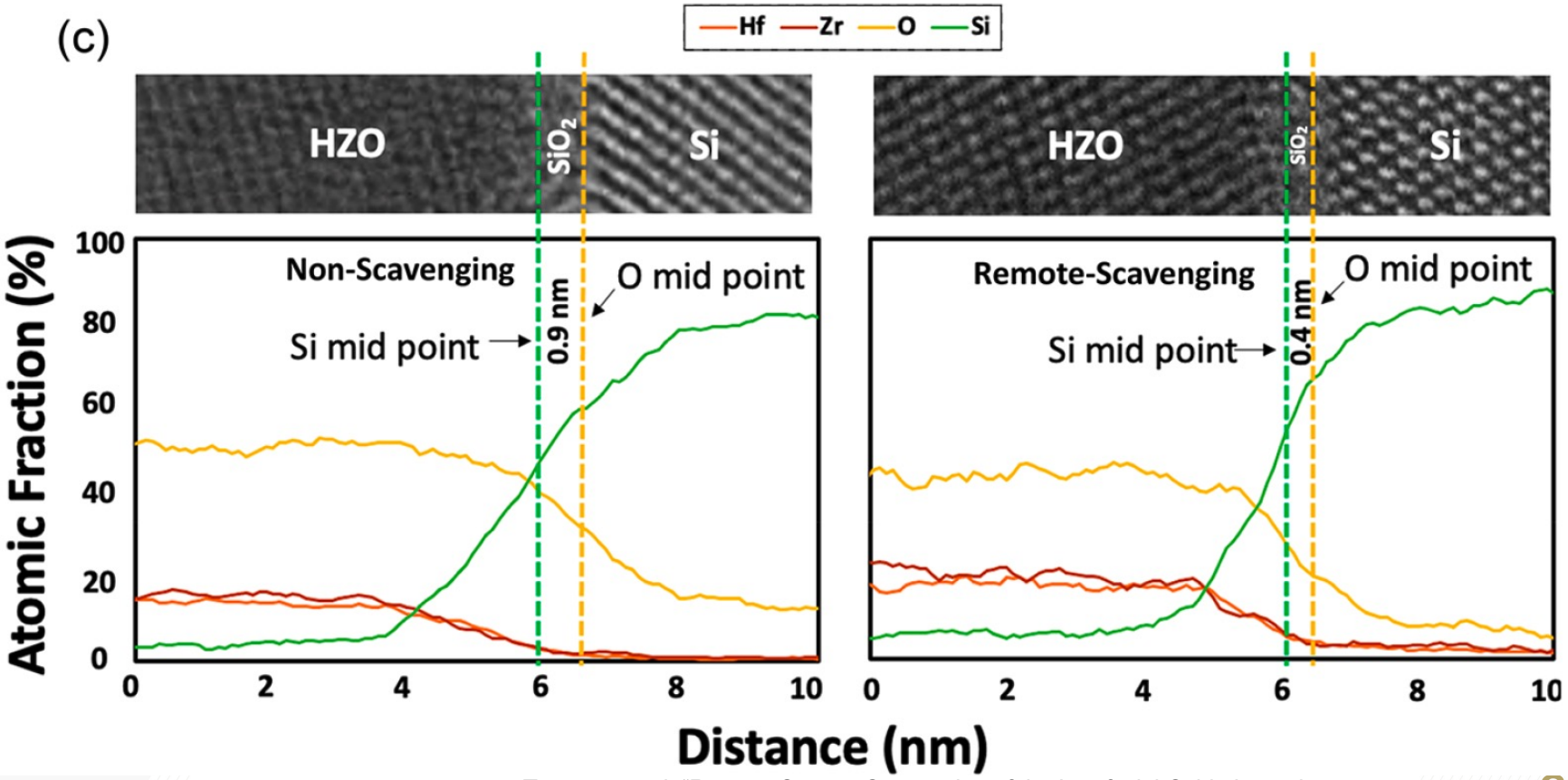


Remote-Scavenging



Tasneem et al. “Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium–Zirconium Oxide-Based Metal–Oxide–Semiconductor Structures”, ACS Appl. Mater. Interfaces 2022, 14, 43897–43906

Remote oxygen scavenging to reduce IL thickness



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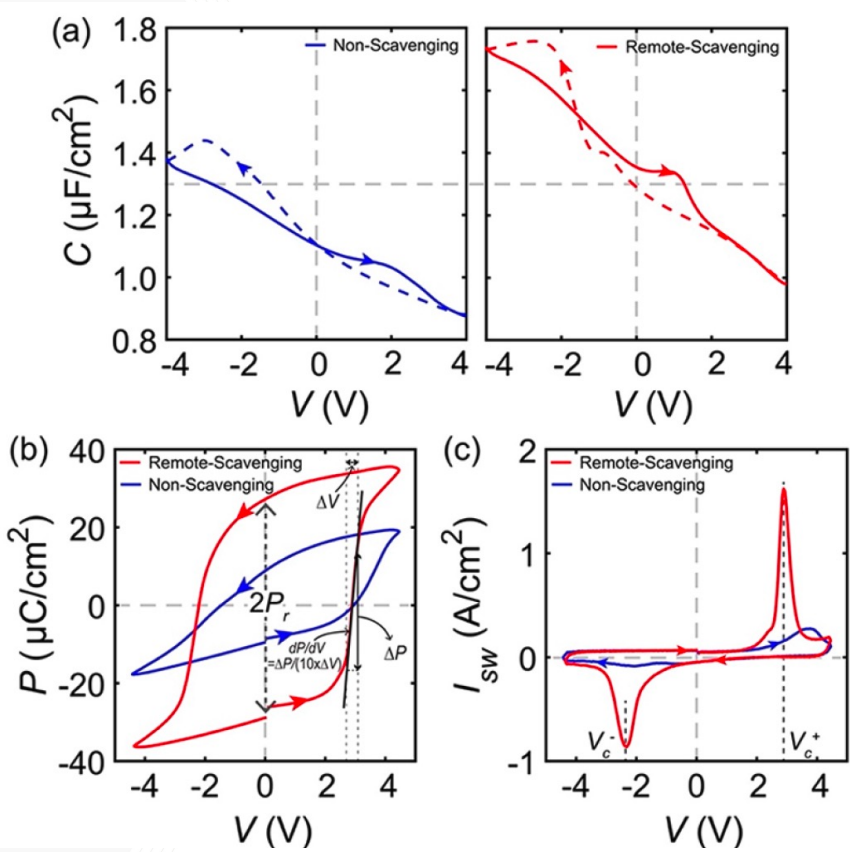
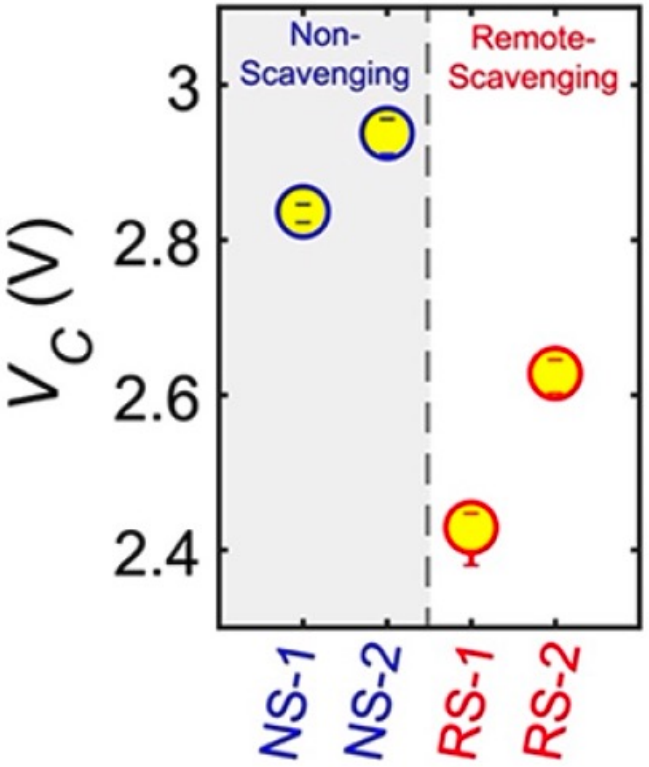
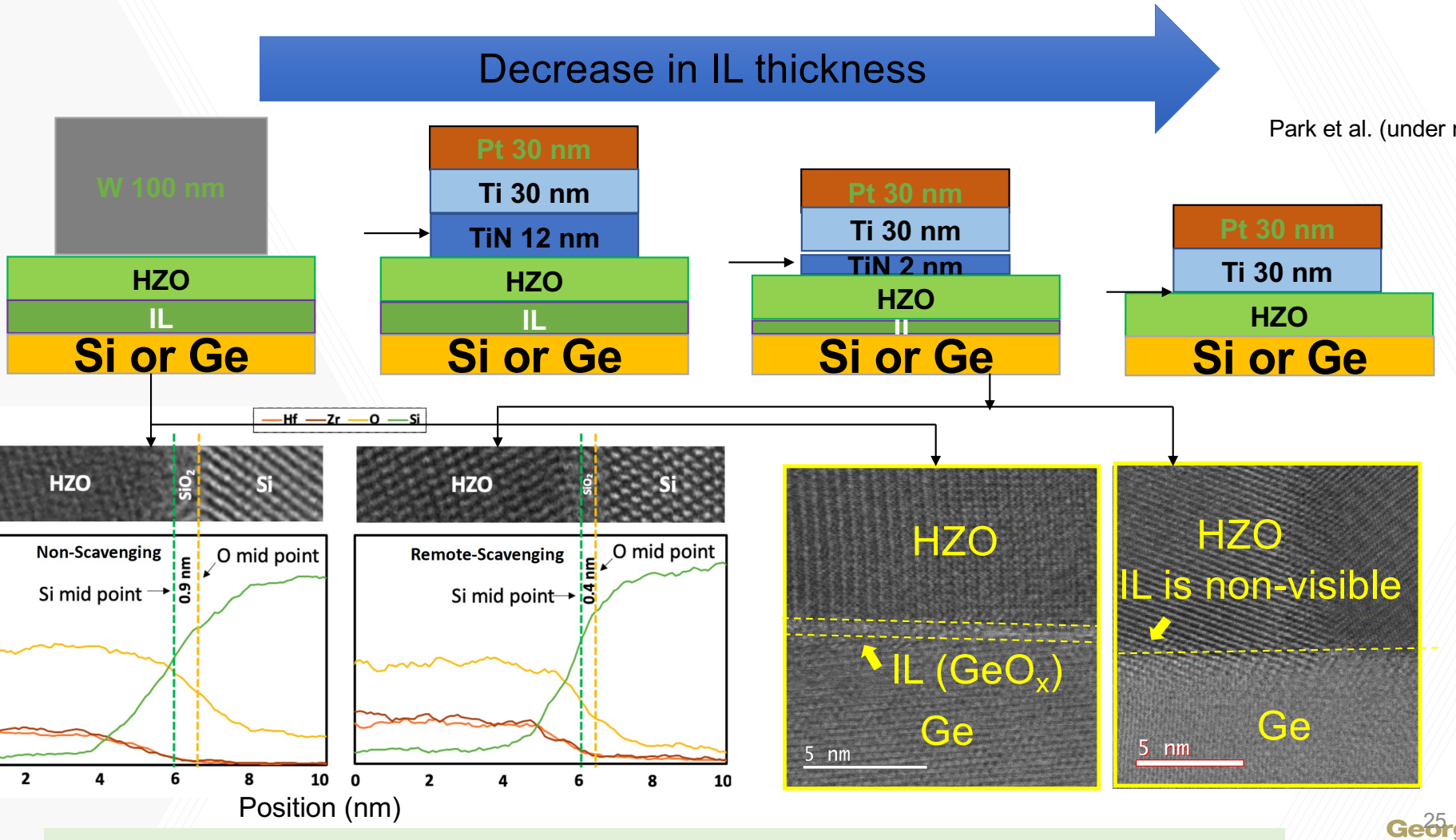




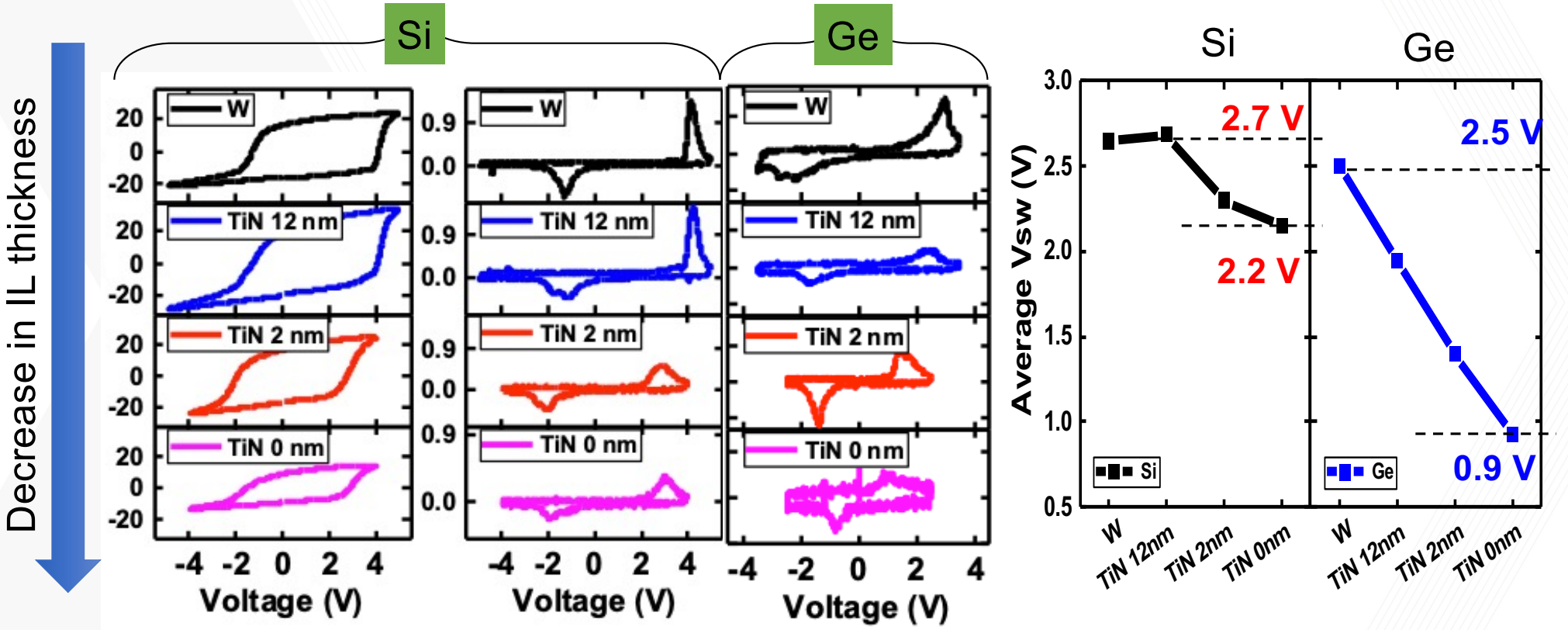
Tasneem et al. "Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium−Zirconium Oxide-Based Metal−Oxide−Semiconductor Structures", ACS Appl. Mater. Interfaces 2022, 14, 43897–43906



Park et al. (under review)

Remote oxygen scavenging can result in controllable IL thickness.

The effect of the IL thickness on Vc



Dramatic reduction in coercive voltage is observed in Ge platform with the change of the gate metal stack.

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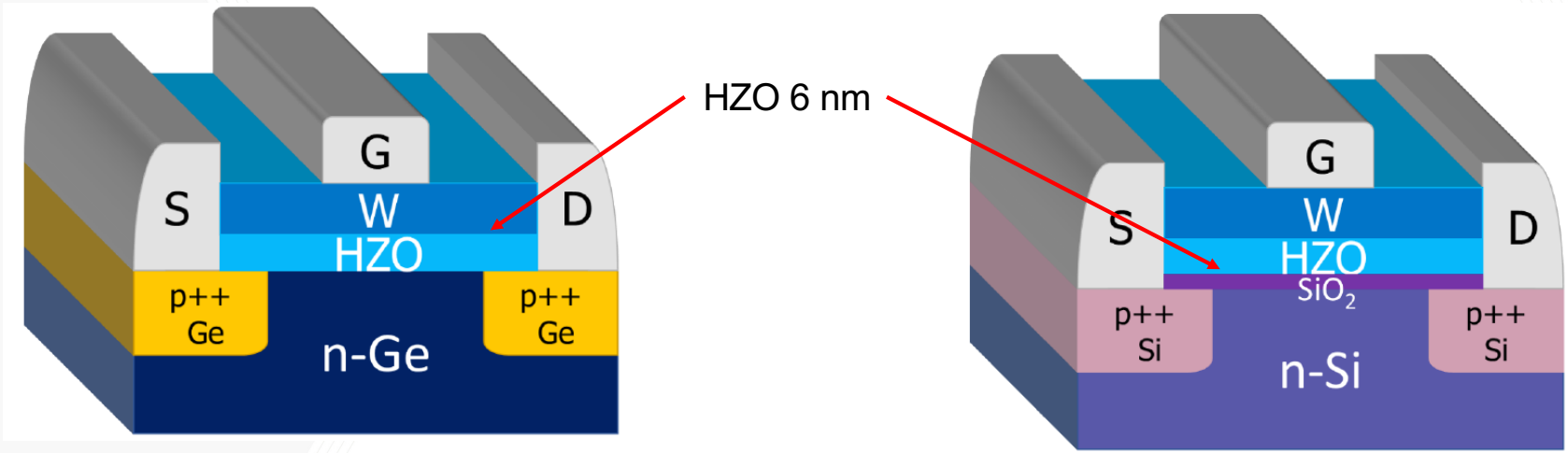
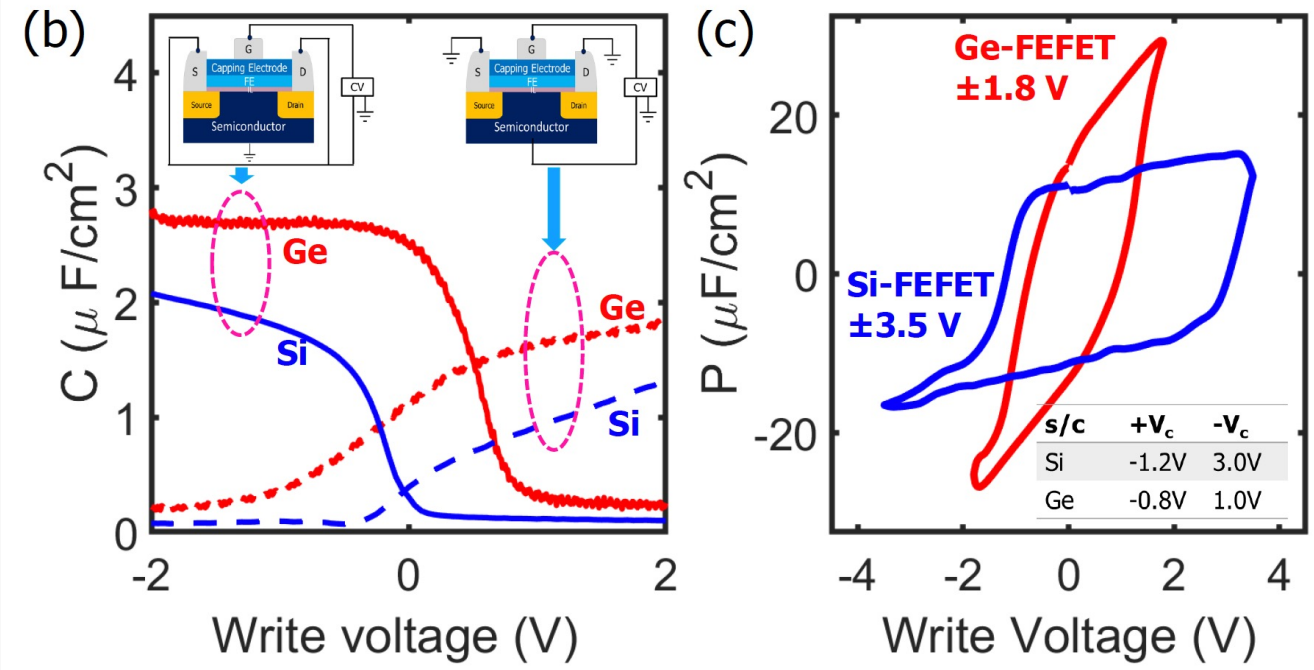
Ge-channel FEFETs with record-low write voltages



Si and Ge-channel FEFETs fabricated with the same 6 nm HZO layers, under similar process and fabrication conditions.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

Ge-channel FEFETs with record-low write voltages



Significant increase on the on-capacitance and reduction in coercive voltage in Ge-channel FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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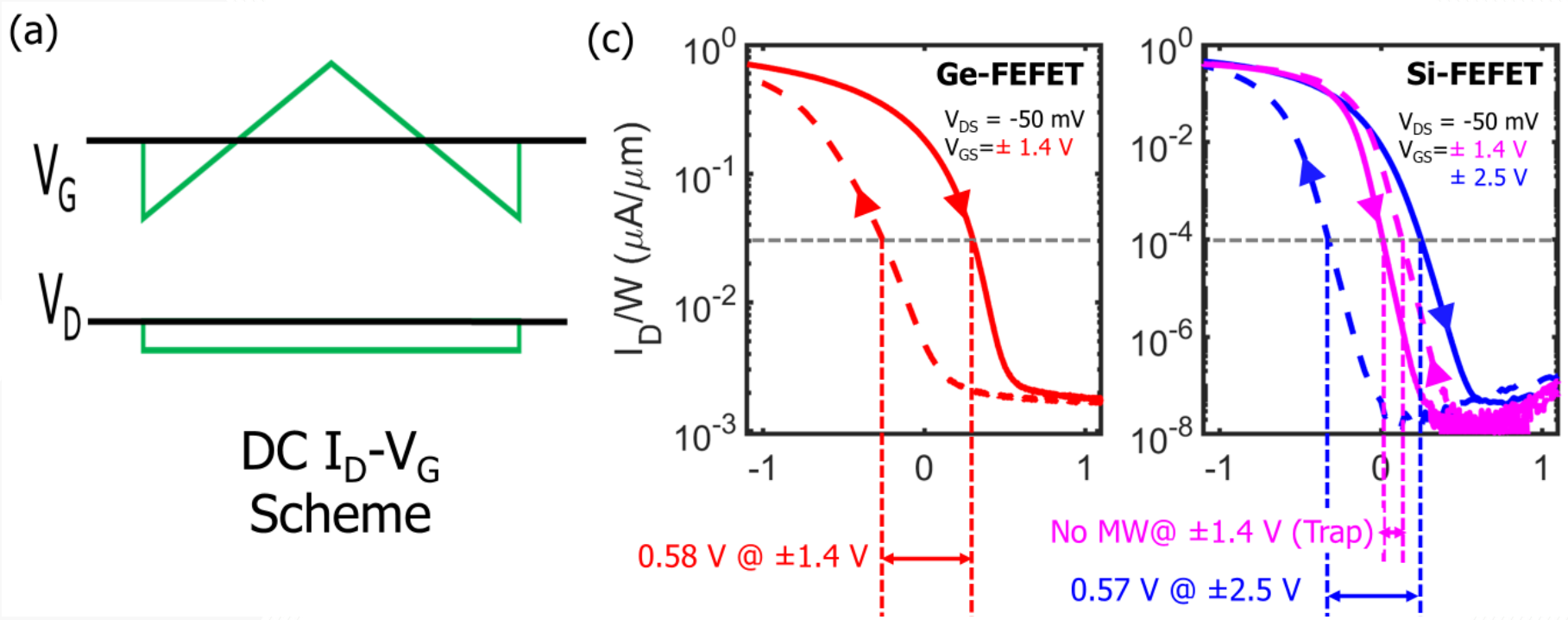
DC I_D-V_G characteristics



Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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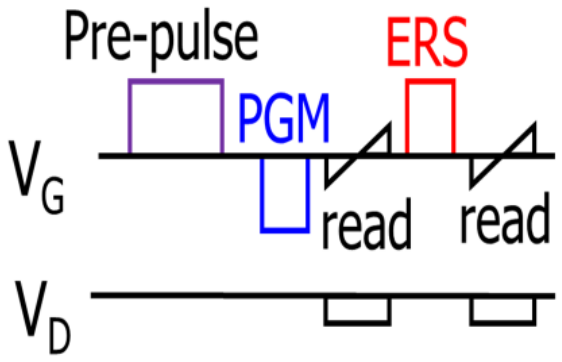
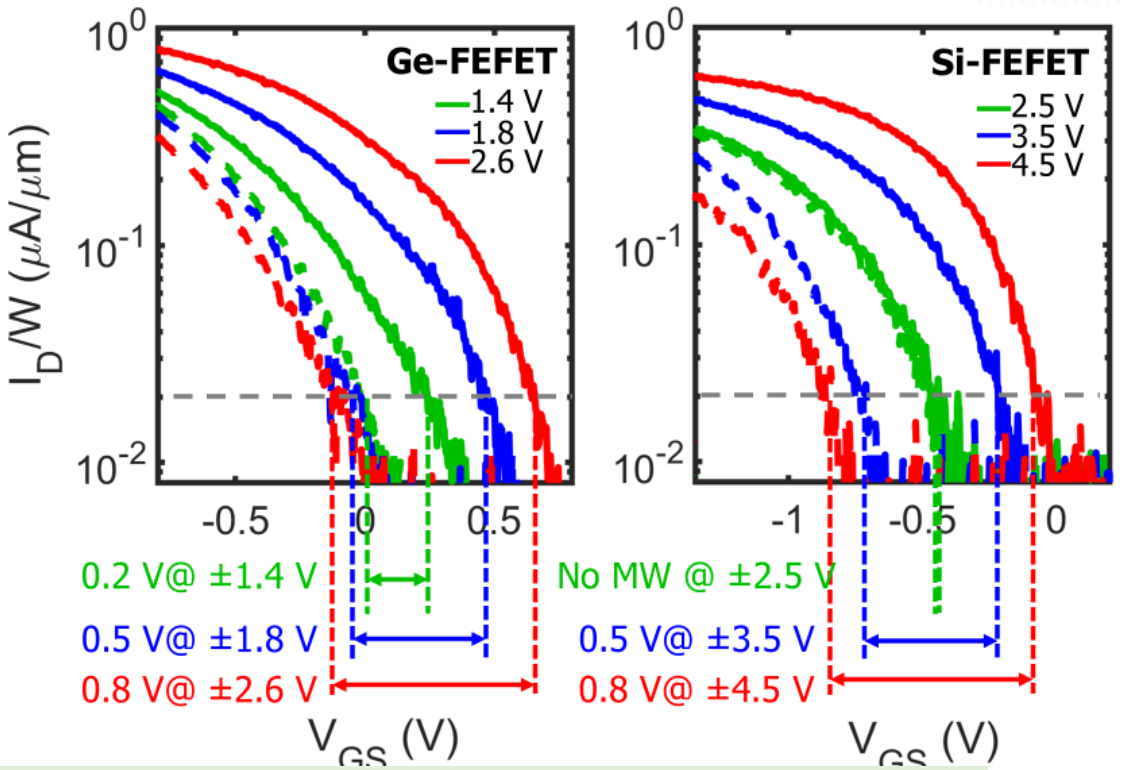
Pulsed I_D-V_G characteristics



Pulsed I_D-V_G Scheme



Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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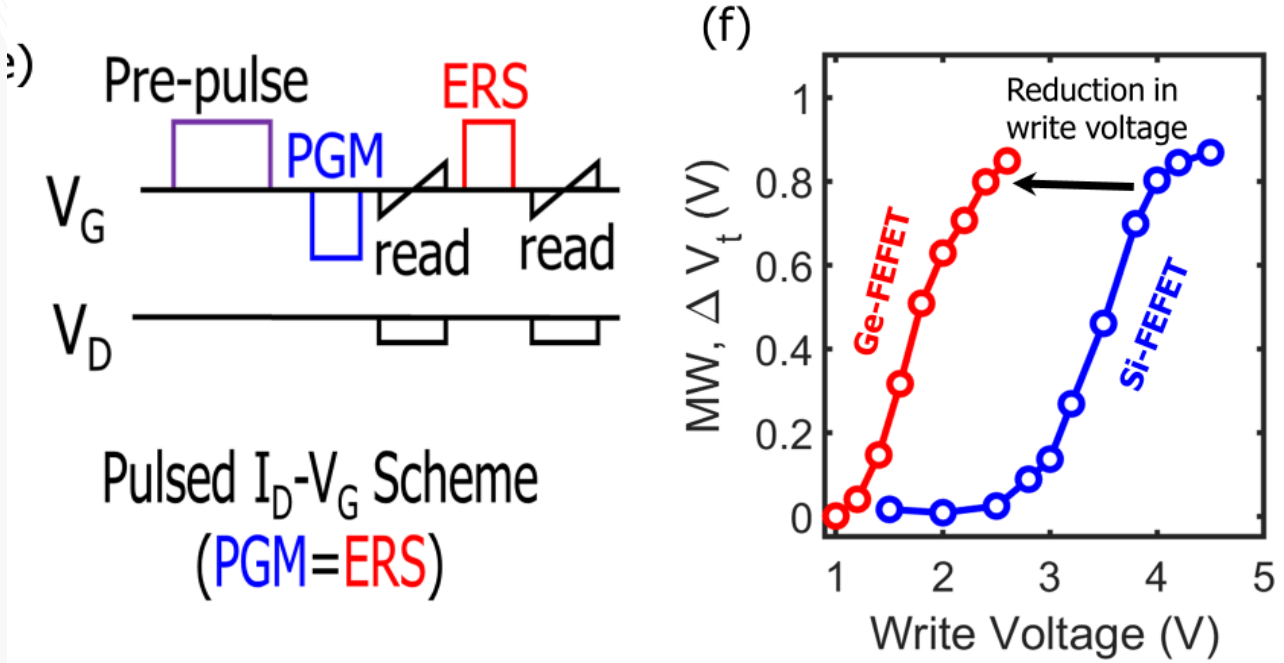
Pulsed I_D-V_G characteristics



Significant reduction in the write voltage for iso-memory MW condition in Ge-FEFET.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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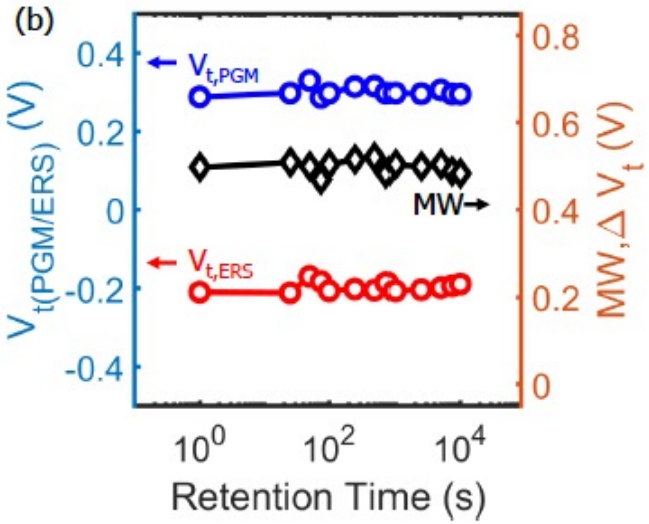
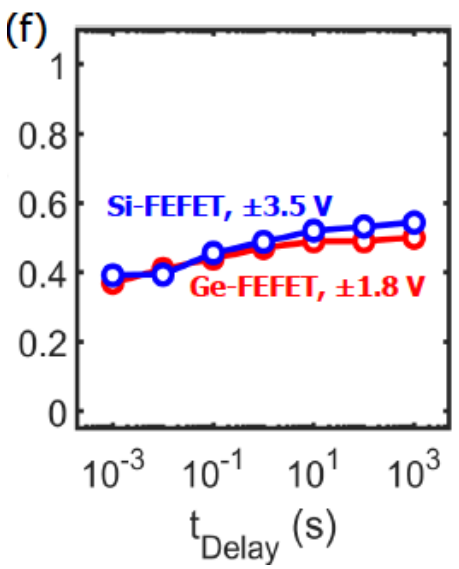
Retention, endurance and read-after-write delay

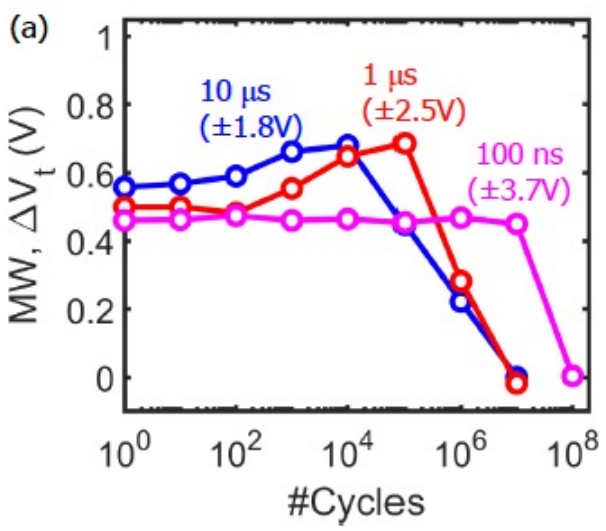
Retention



Read-after-write delay



Endurance



The Ge-FEFET show write endurance of 107 cycles, excellent data retention and immediate read-after-write capability.

Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

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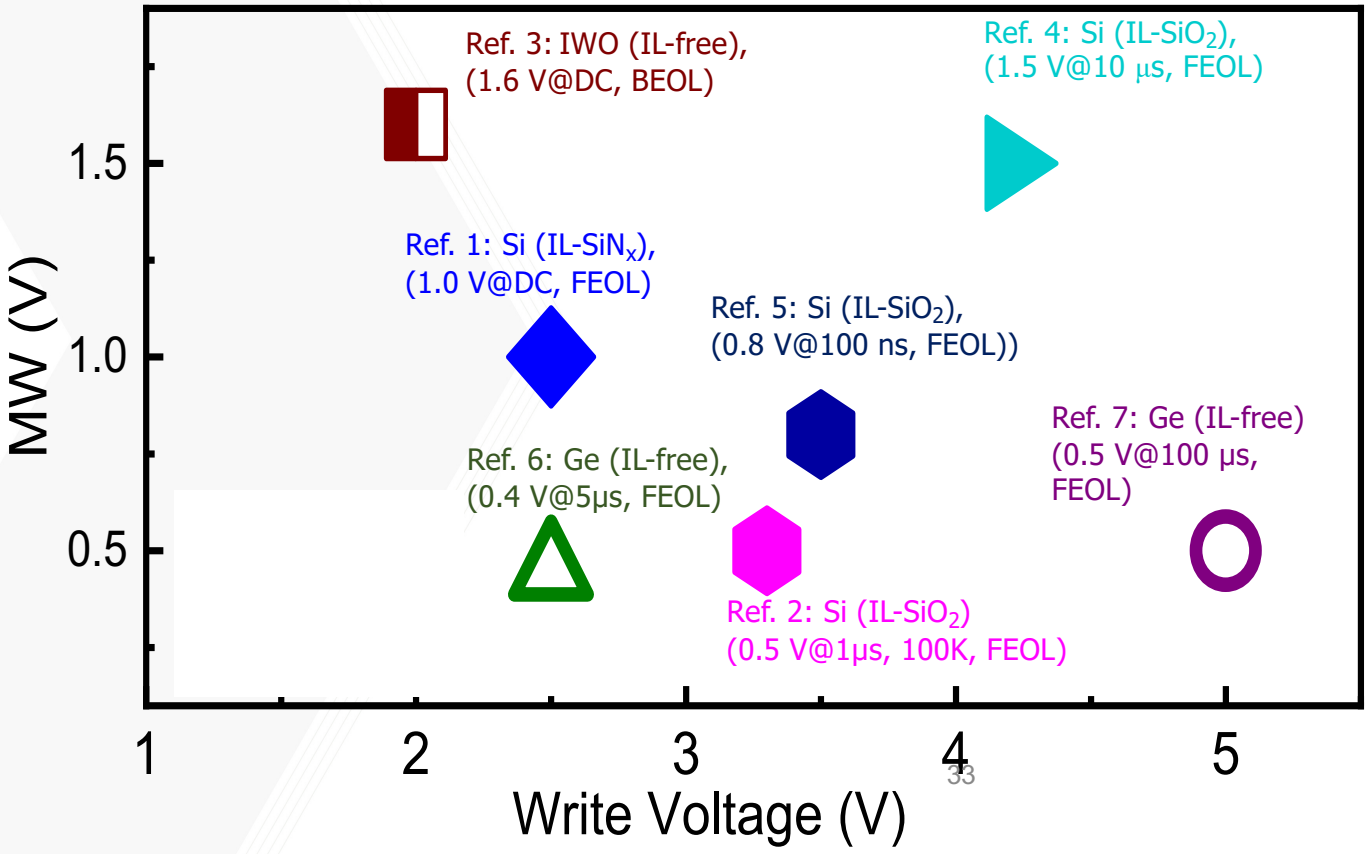
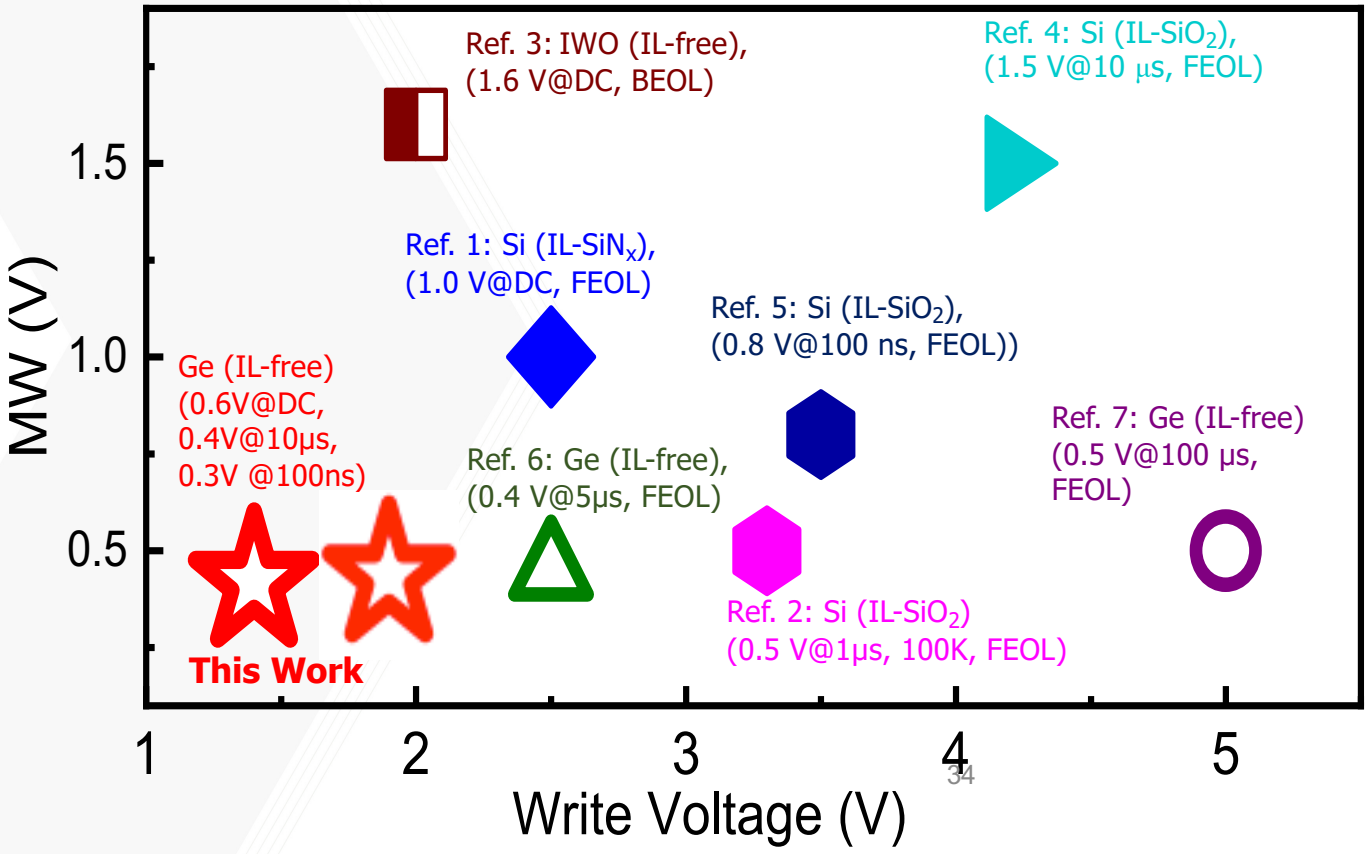
Benchmarking Memory Window v. Write Voltage Tradeoff



[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

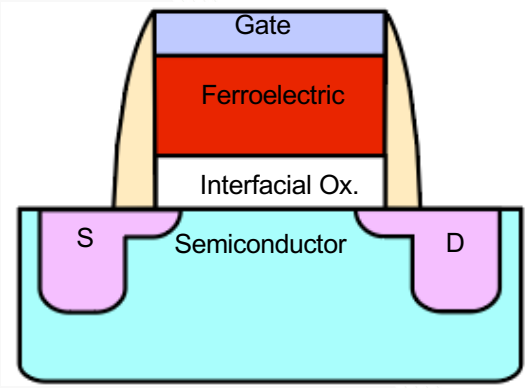
Benchmarking Memory Window v. Write Voltage Tradeoff



Das, Dipjyoti, et al. "A Ge-Channel Ferroelectric Field Effect Transistor with Logic-Compatible Write Voltage." *IEEE Electron Device Letters* (2022).

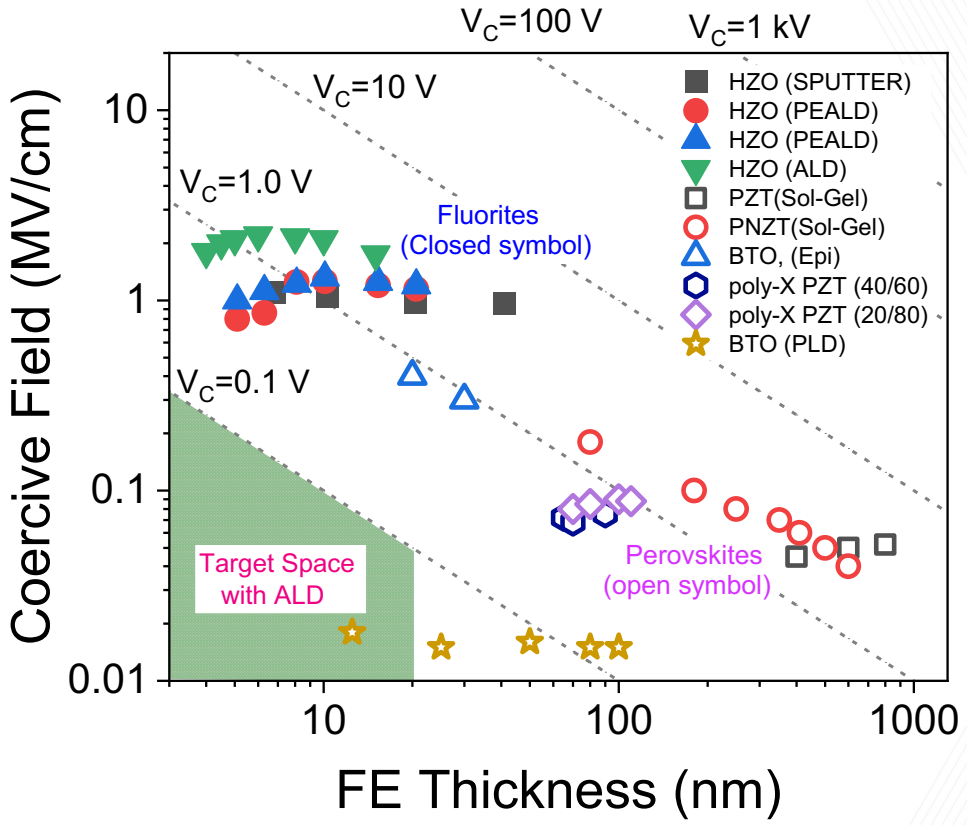
[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

Towards 0.5 V Ferroelectric Memories



Classical Ferroelectrics:
$BaTiO_3$ etc.

Emerging CMOS compatible Ferroelectrics:
Doped HfO_2



Is there a case for classical ferroelectric oxides such as BaTiO3 for emerging memory applications?

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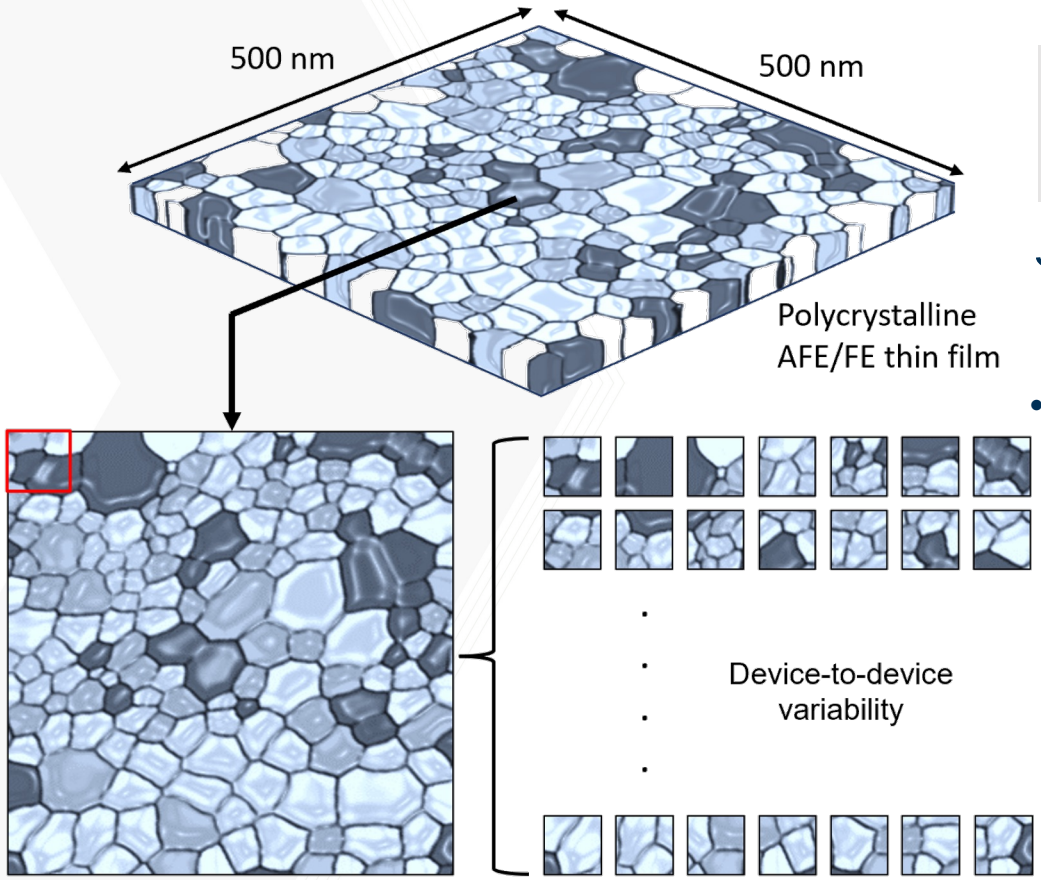
Microstructure in FEFETs



1. Phase (o-, m-, t-)
3. Sub-grain features (domain walls, interphase boundaries)
2. Grain size & orientation

Device-to-device variability

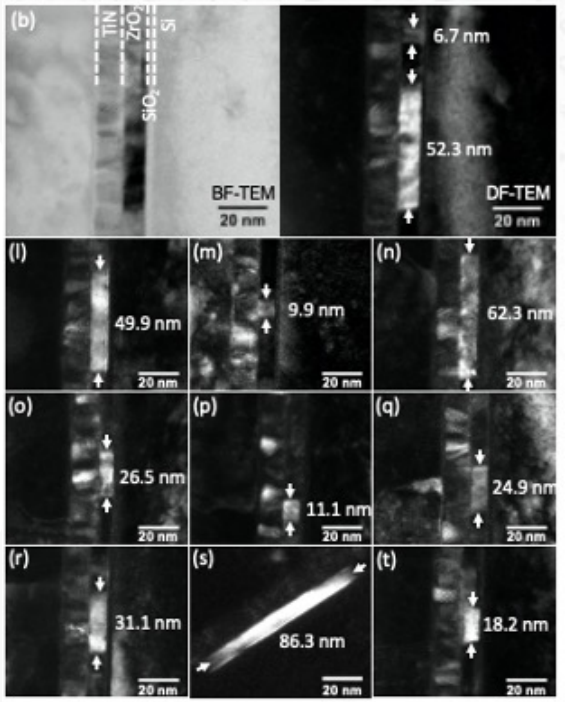
- Applied field causes changes in microstructure
  - Enables multi-level NVM
  - Poses challenges for (VLSI)

4. Irreversible change of grain structure electric field cycling

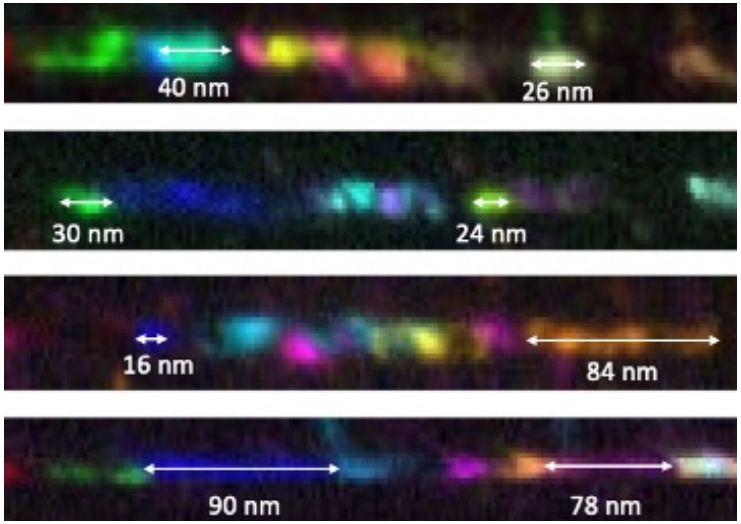
Cycle-to-cycle variability

Quantification of microstructure

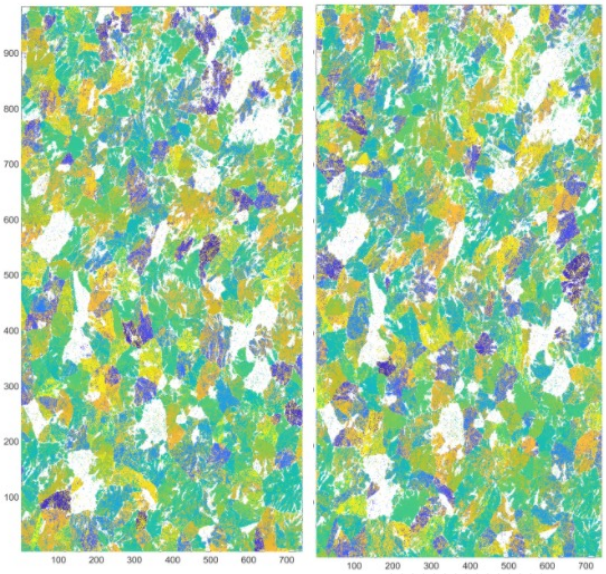
Dark field TEM



Nano-Beam Electron Diffraction (NBED)

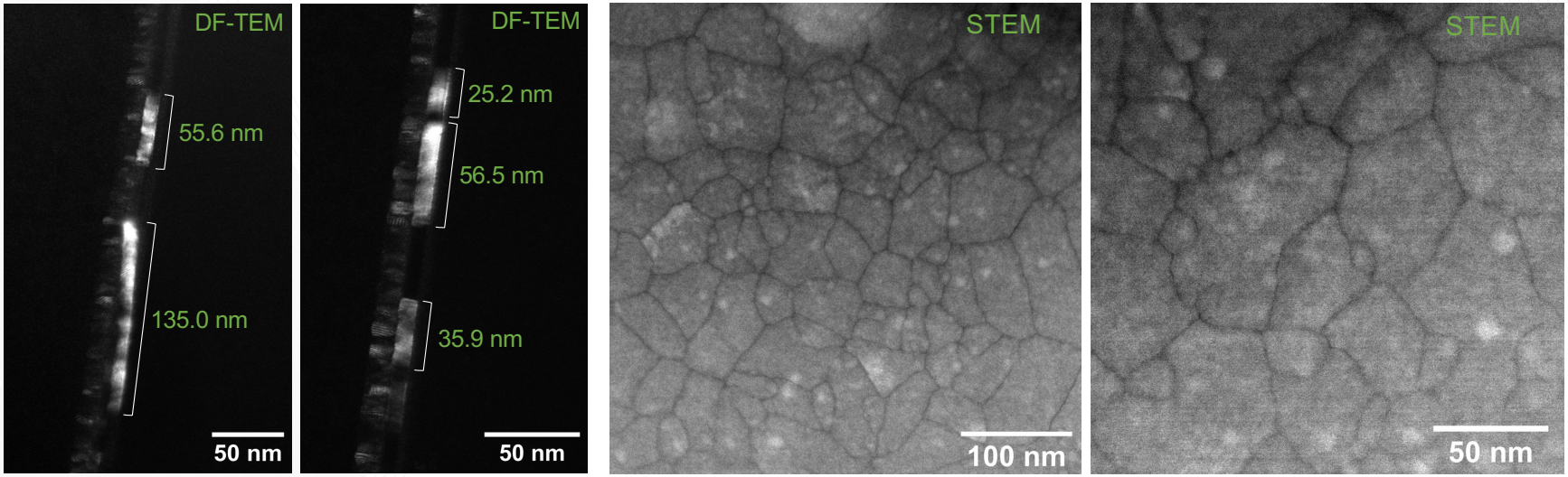


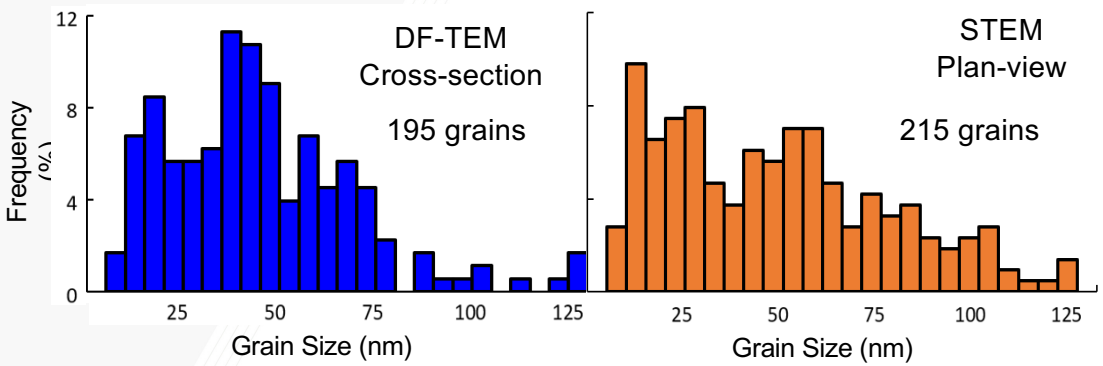
Transmission Kikuchi Diffraction (TKD)

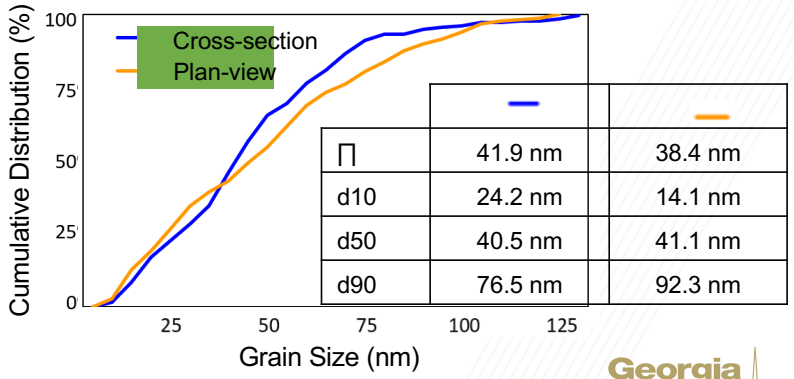


Lombardo, S. F., et al. "Local epitaxial-like templating effects and grain size distribution in atomic layer deposited $Hf_{0.5}Zr_{0.5}O_2$ thin film ferroelectric capacitors." *Applied Physics Letters* 119.9 (2021): 092901.

Quantification of microstructure



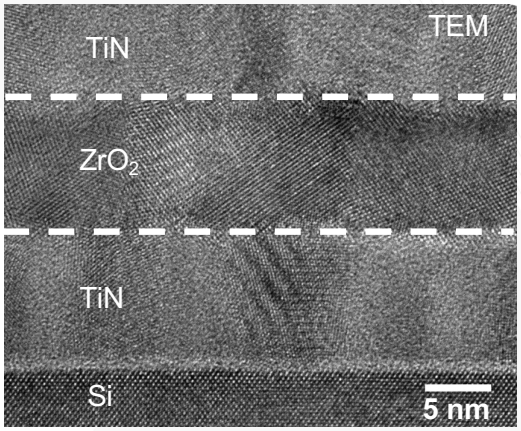


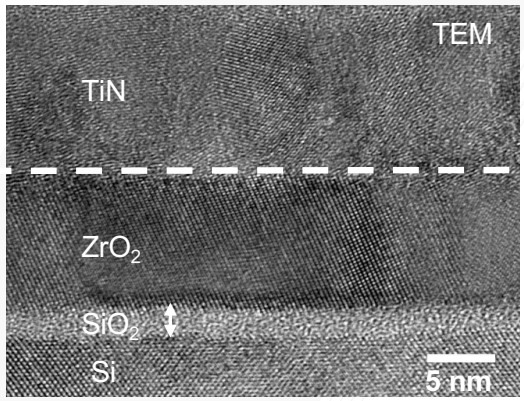


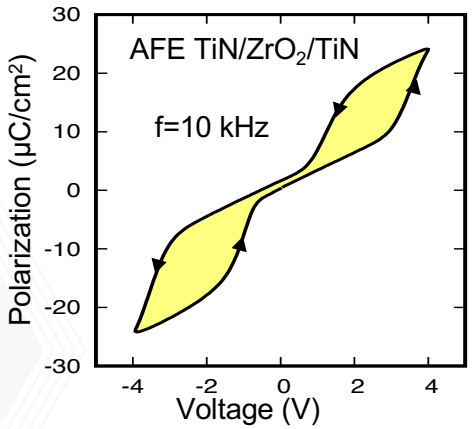
	—	—
∏	41.9 nm	38.4 nm
d10	24.2 nm	14.1 nm
d50	40.5 nm	41.1 nm
d90	76.5 nm	92.3 nm

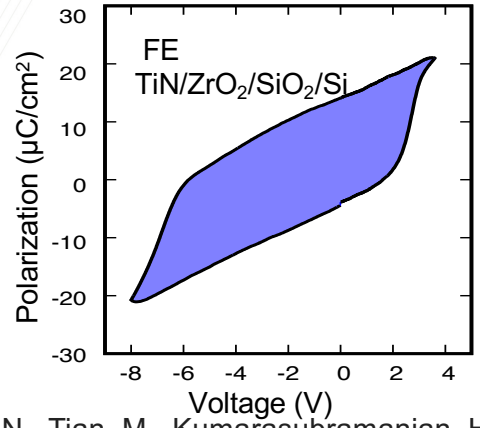
Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

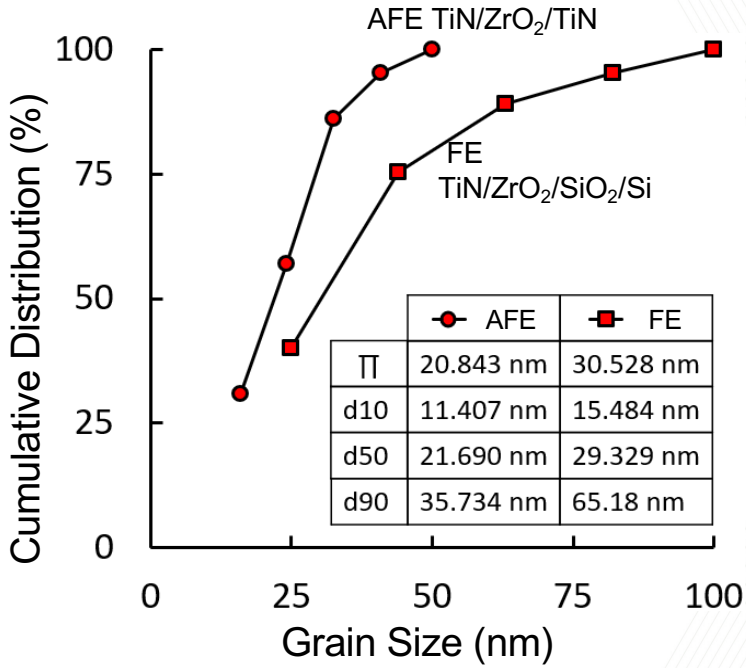
Microstructural origin of AFE and FE in ZrO_2







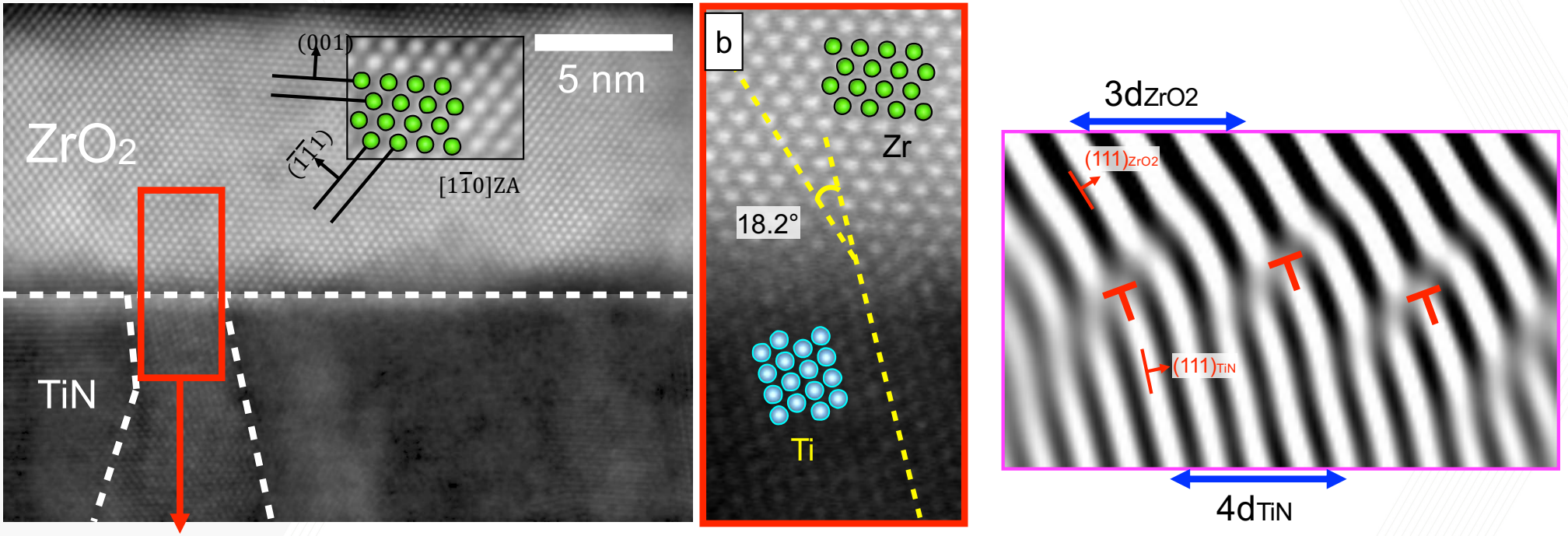




Smaller grain size favored by Tetragonal phase over FE Orthorhombic phase

Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

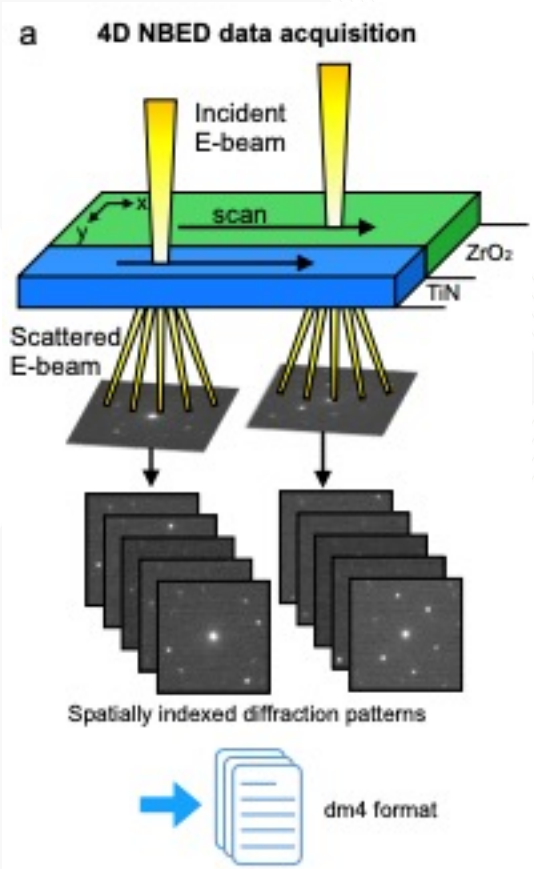
Epitaxial-like templating: Near coincidence site epitaxy

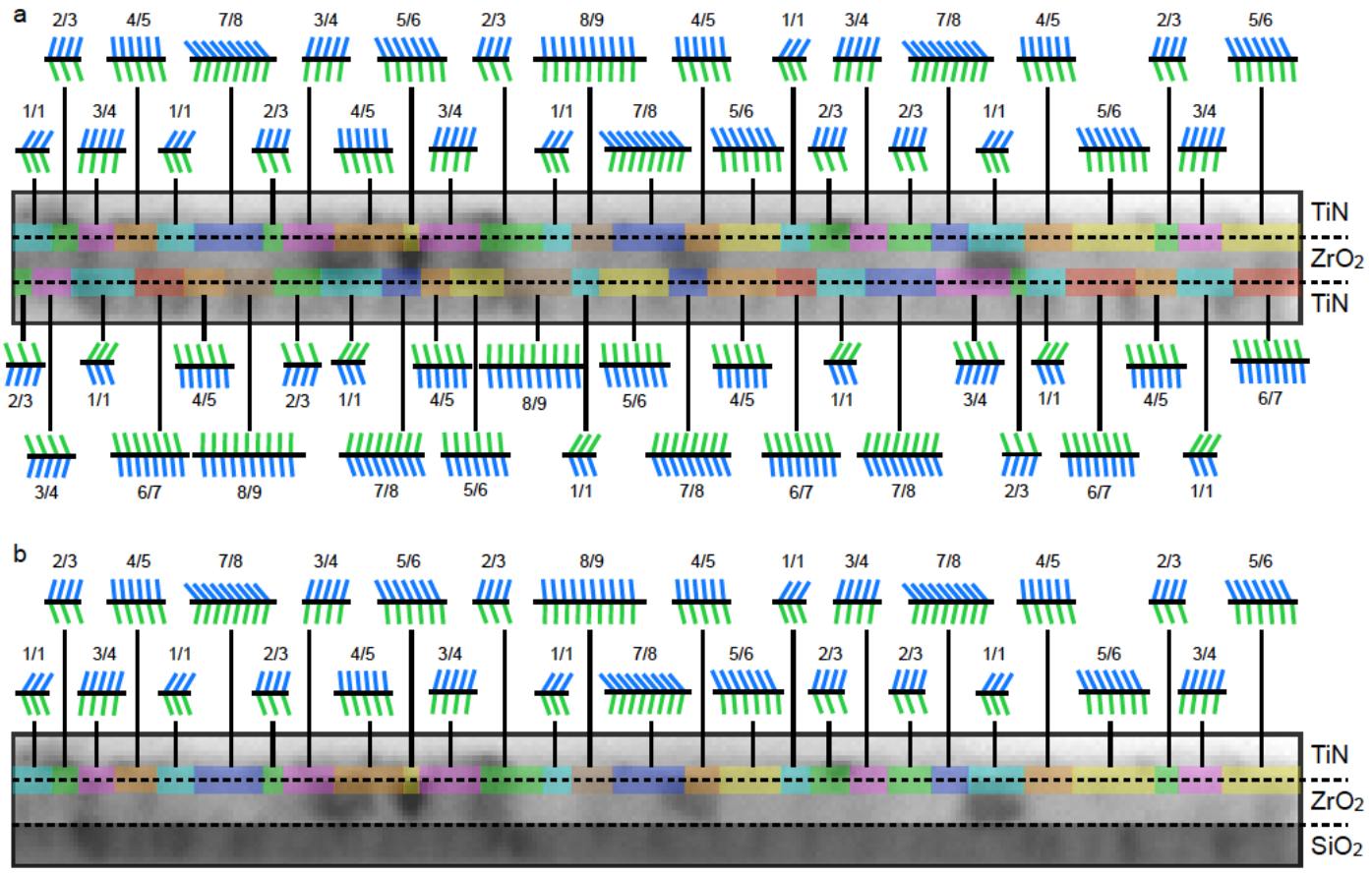


Orientations in TiN and ZrO_2 are often correlated.

Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

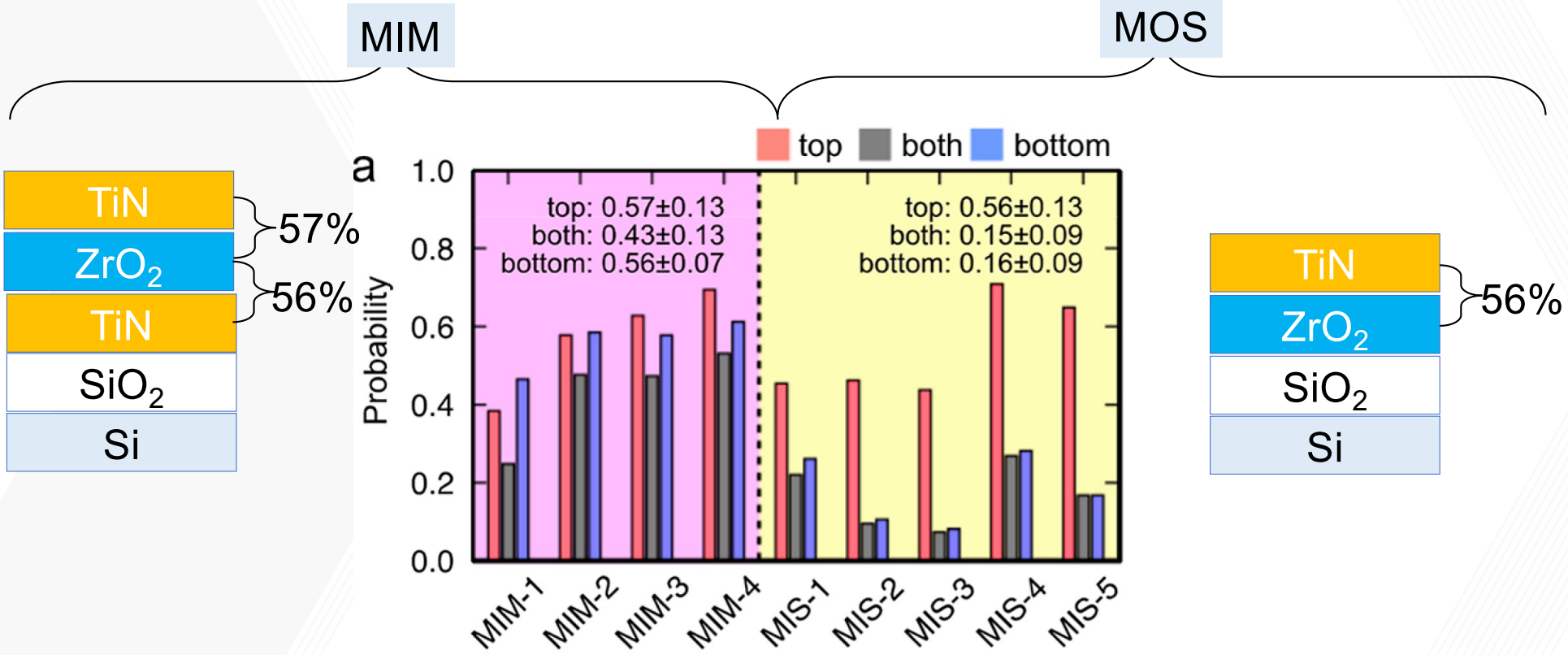
Epitaxial-like templating: Near coincidence site epitaxy





Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

Statistical Epitaxy Analysis via Automated NBED



Chae, K., Lombardo, S. F., Tasneem, N., Tian, M., Kumarasubramanian, H., Hur, J., ... & Khan, A. I. (2022). Local Epitaxial Templating Effects in Ferroelectric and Antiferroelectric ZrO2. *ACS Applied Materials & Interfaces*, *14*(32), 36771-36780.

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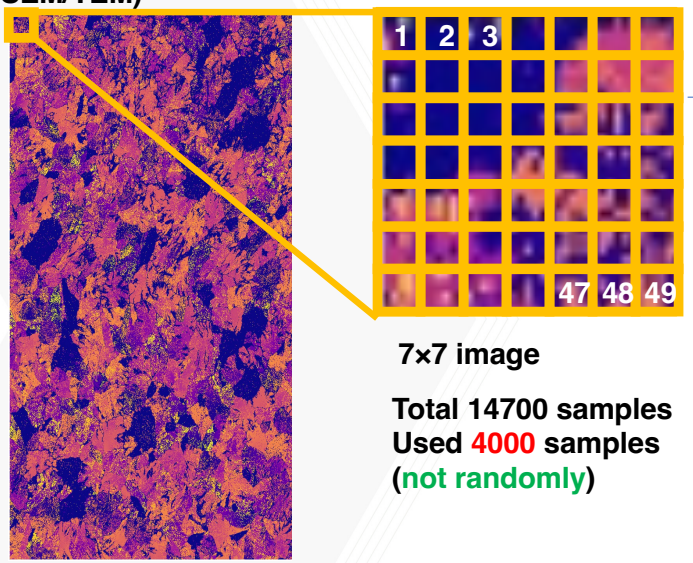
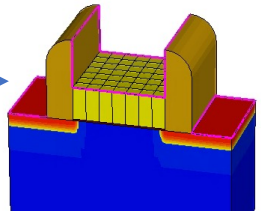
Machine Learning Assisted Predictive TCAD Modeling (from Metrology to Device Metrics)

Ferro polarization map (from TKD data from SEM/TEM)



7×7 image

Total 14700 samples
Used 4000 samples
(not randomly)



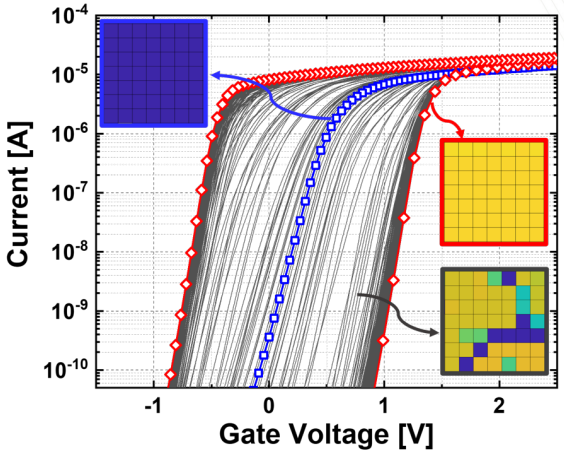


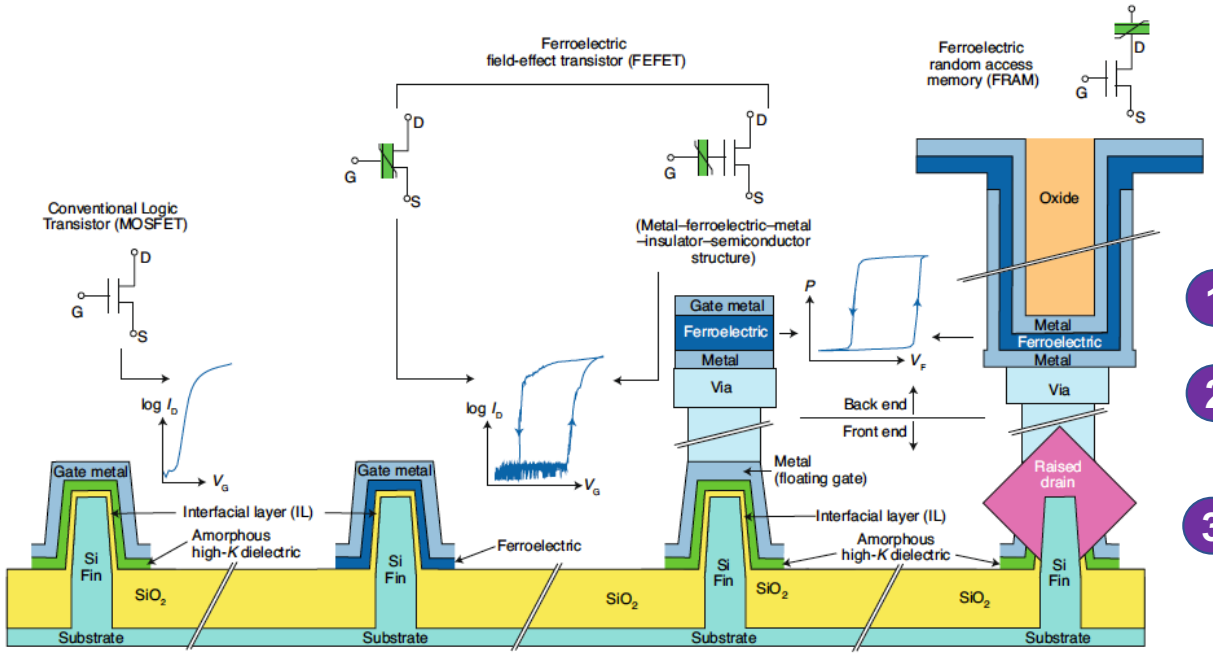
TABLE II. Average, 3-sigma and percentage of prediction error

	TCAD	ML-based prediction		
	μ	μ	3σ	Error
HVT [V]	1.05	1.05	0.08	**1.2%**
LVT [V]	–0.53	–0.53	0.07	**2.0%**
I_{on} [μA]	6.68	6.68	1.01	**2.1%**
SS [mV/dec]	94.52	94.48	9.0	**1.6%**

G. Choe, P. V. Ravindran, A. Lu, J. Hur, M. Lederer, A. Reck, S. Lombardo, N. Afroze, J. Kacher, A. I. Khan, S. Yu, "Machine learning assisted statistical variation analysis of ferroelectric transistors: from experimental metrology to predictive modeling," IEEE Symposium on VLSI Technology and Circuits (VLSI) 2022.

The era of ferroelectronics

The next wave of exponential growth of the semiconductor industry depends on how well the electronic hardware can support the explosion of data-centric computing.



Ferroelectric technology will be a key component because of

1. Performance
2. Energy and area efficiency
3. Logic and memory functionalities

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistor technology." *Nature Electronics* 3.10 (2020): 588-597.

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Thank you

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