

Domains in ferroelectric semiconductors

Why do ferroelectric devices fail?

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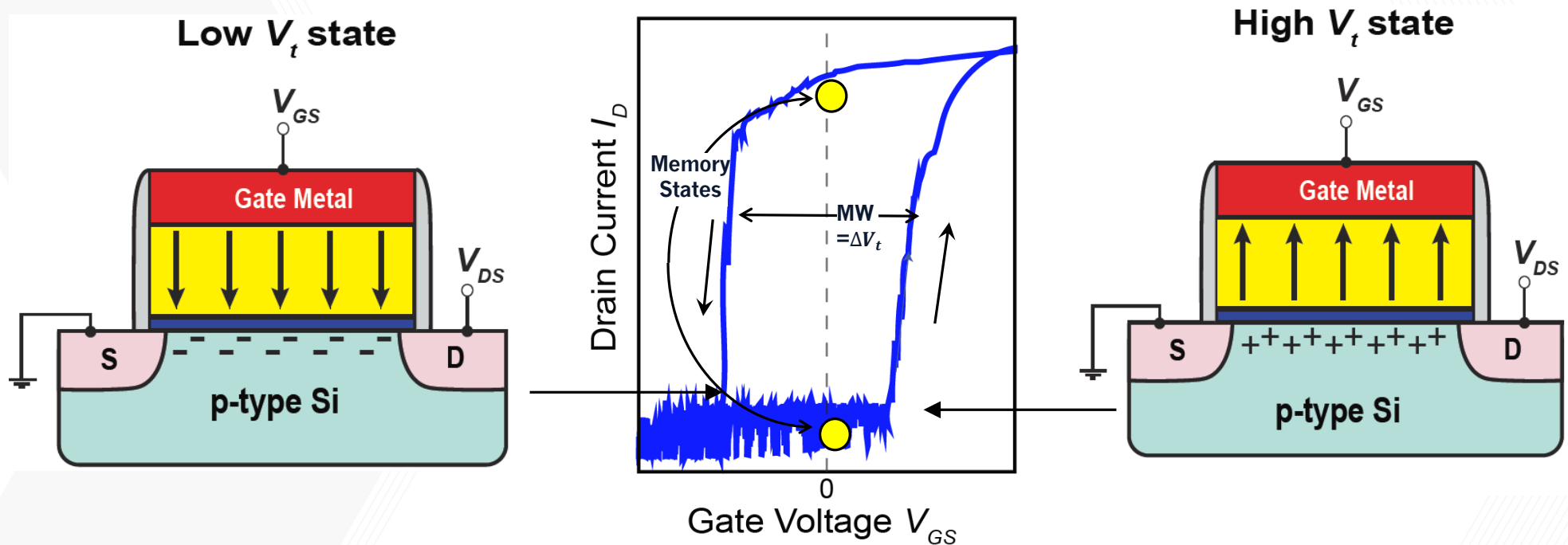
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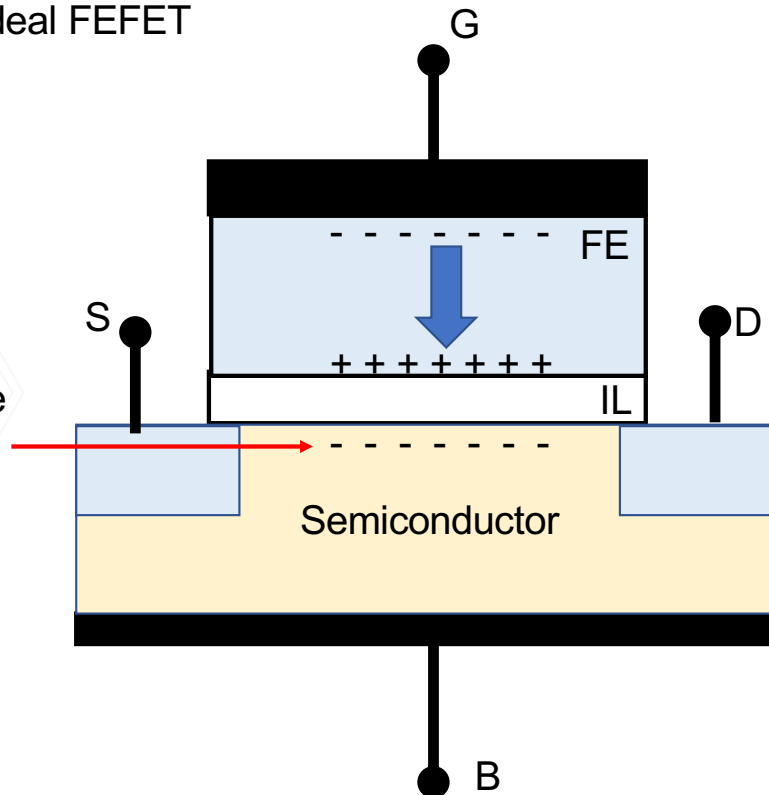
Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET with the threshold voltage correlated with the polarization state of the ferroelectric layer.

How does a FEFET work?

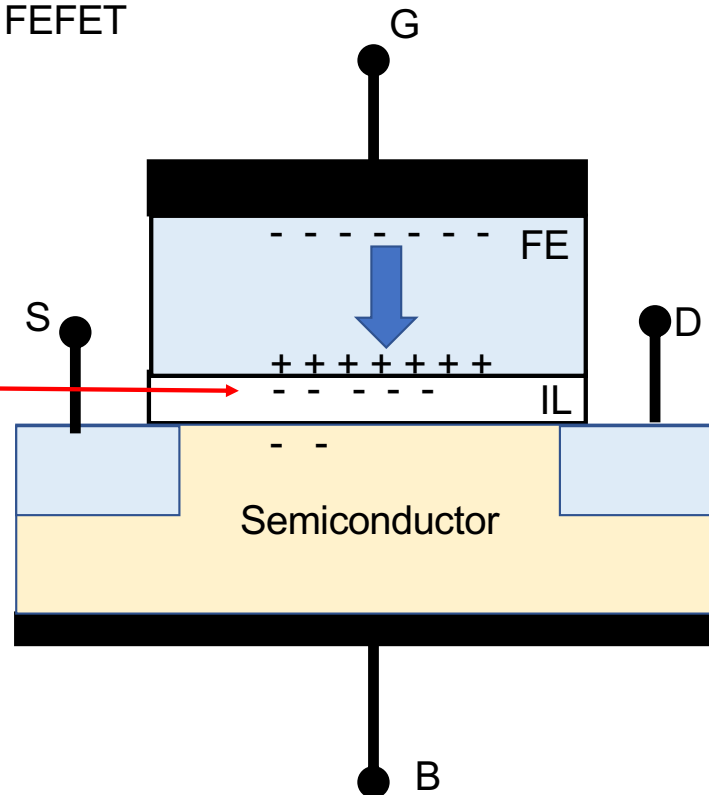
Ideal FEFET



All of the polarization charge is “reflected” as carriers in the semiconductor channel

How does a FEFET work?

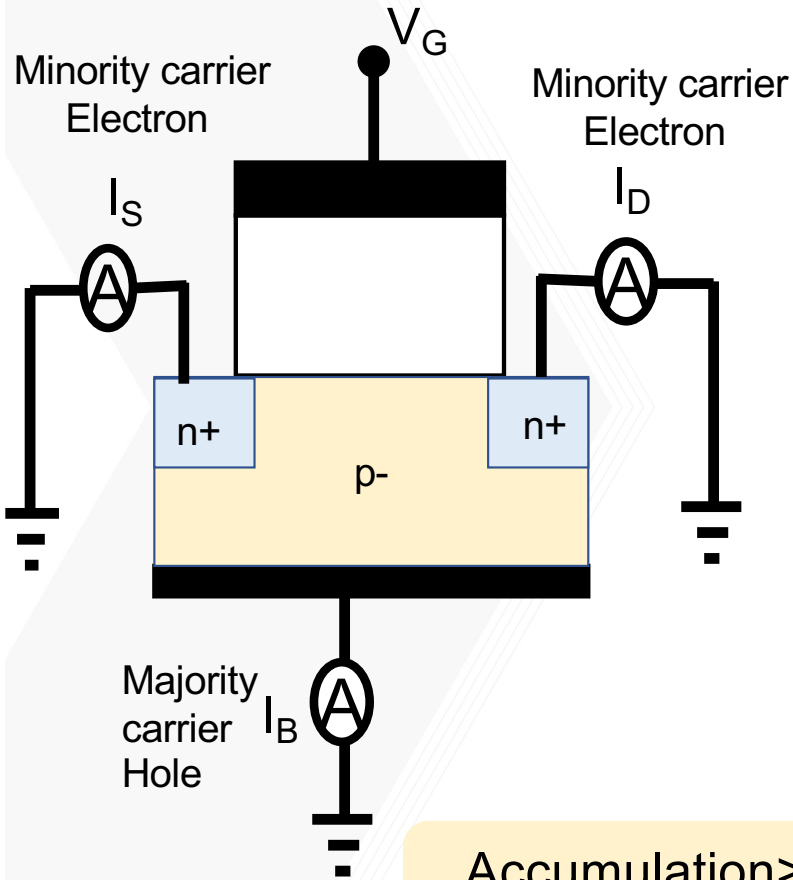
Real FEFET



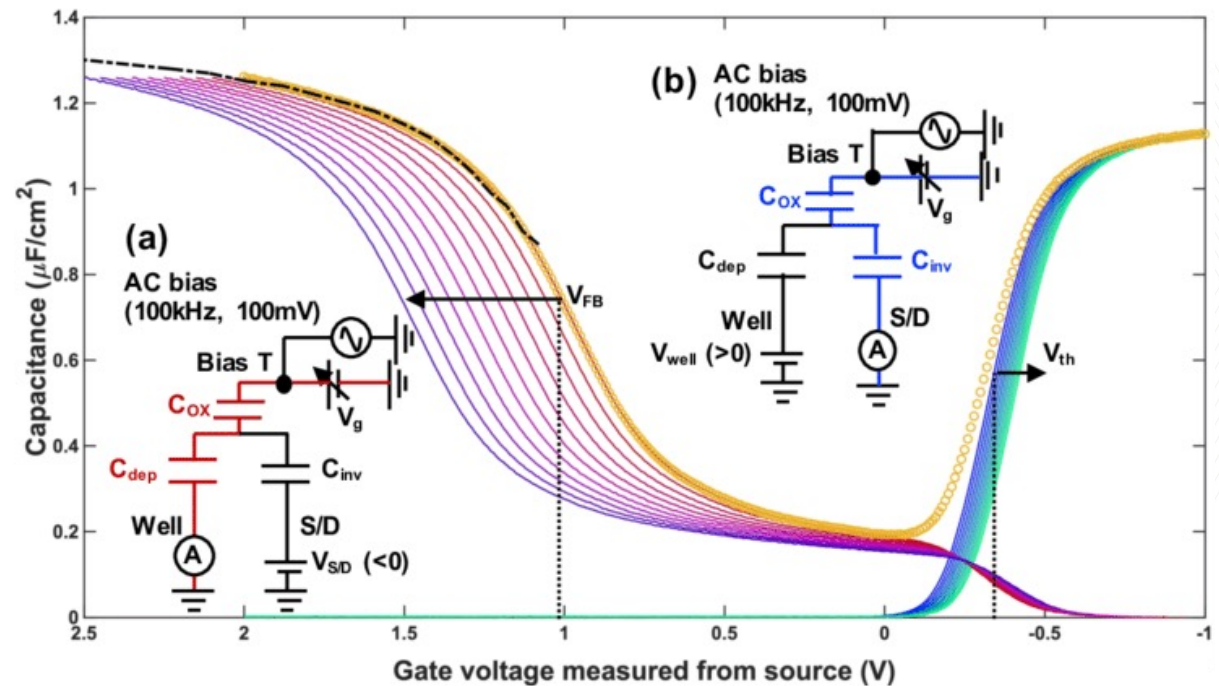
More than 90% of polarization charge is "screened" at the FE interface by defects.

Carrier dynamics in a conventional MOSFET

n-type MOSFET

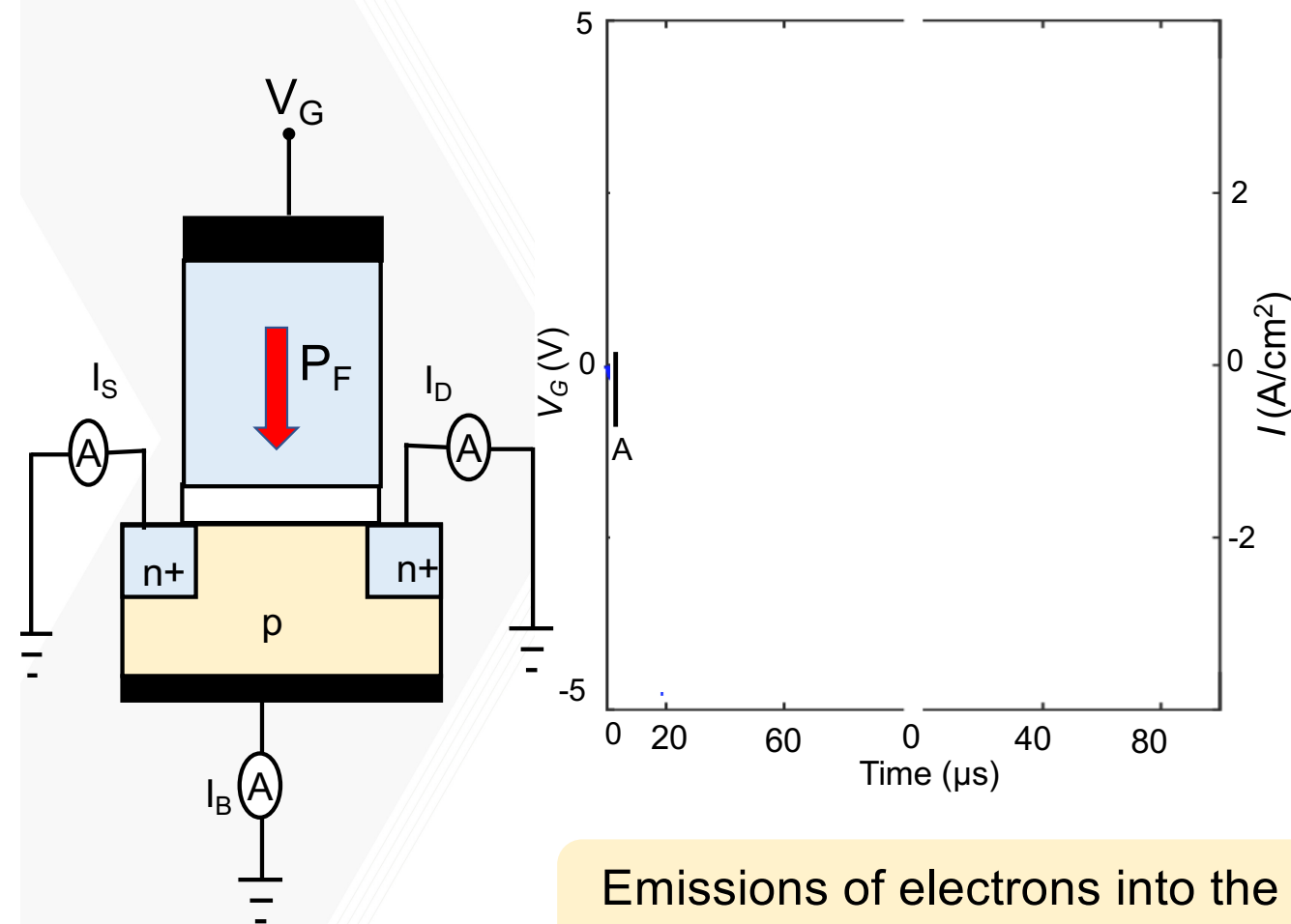


Split CV characteristics of a MOSFET



Accumulation >> only hole from body and no electron from source/drain.

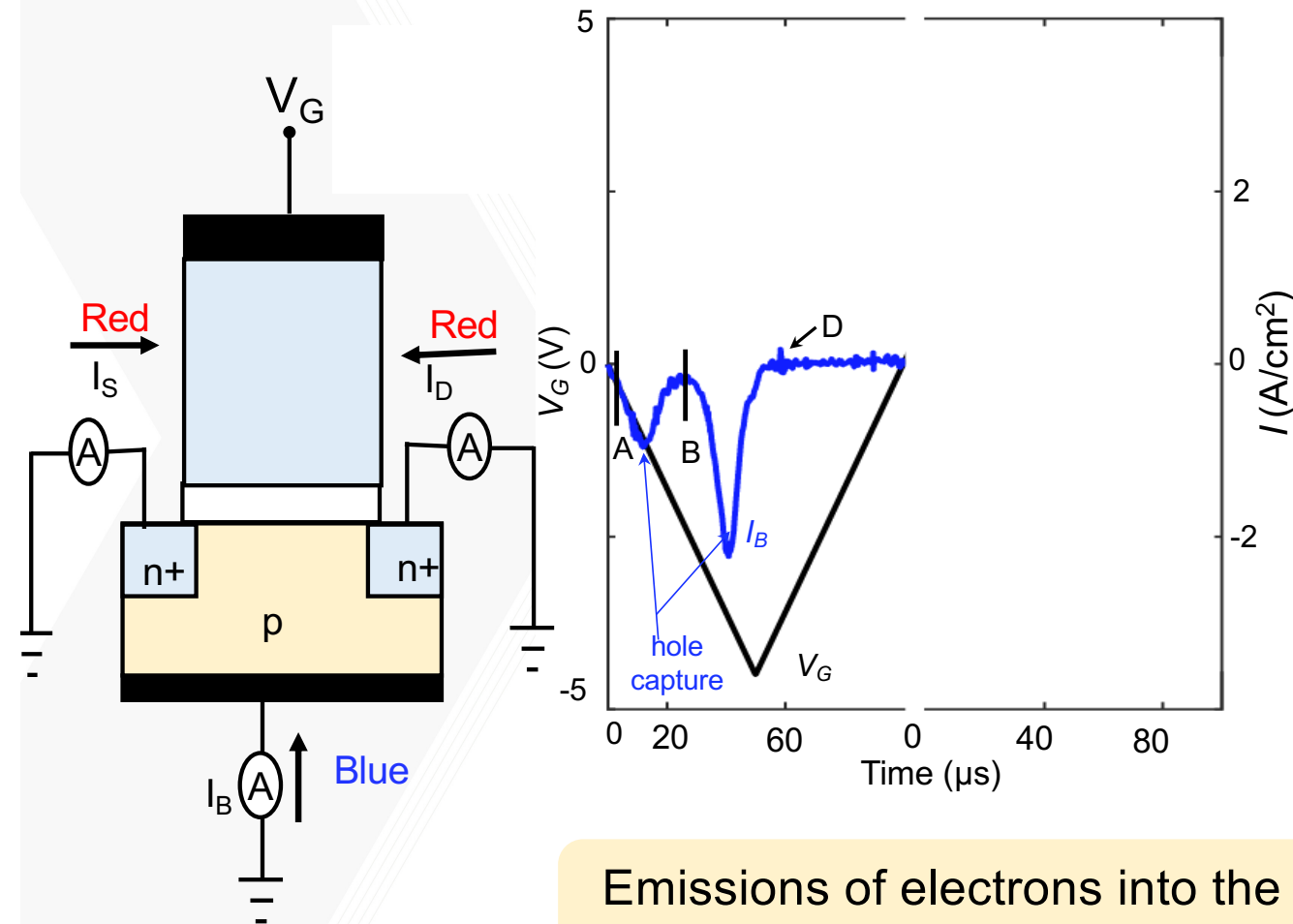
Trap Emission and Capture During Write



Emissions of electrons into the S/D during hole accumulation.

Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2011.

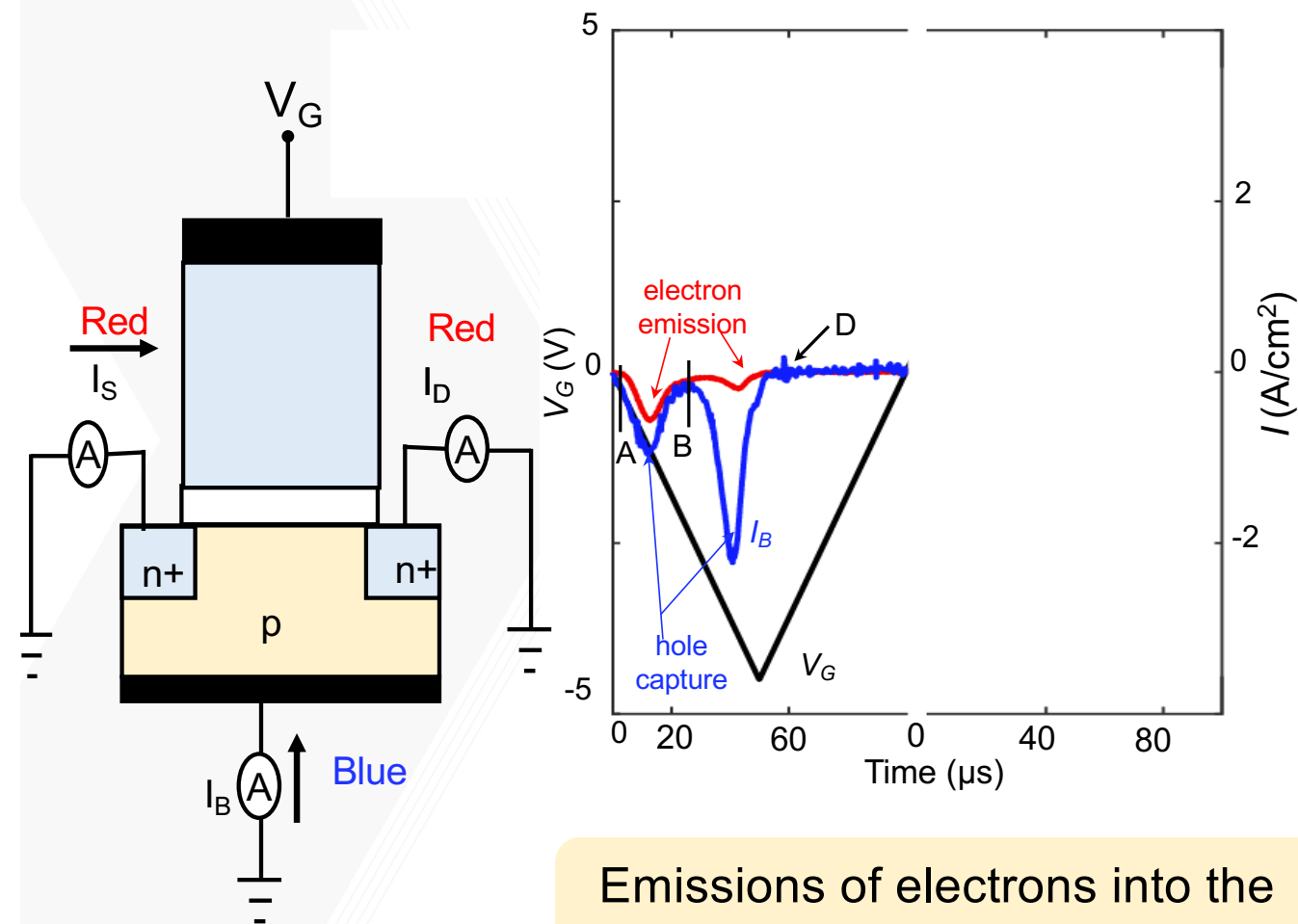
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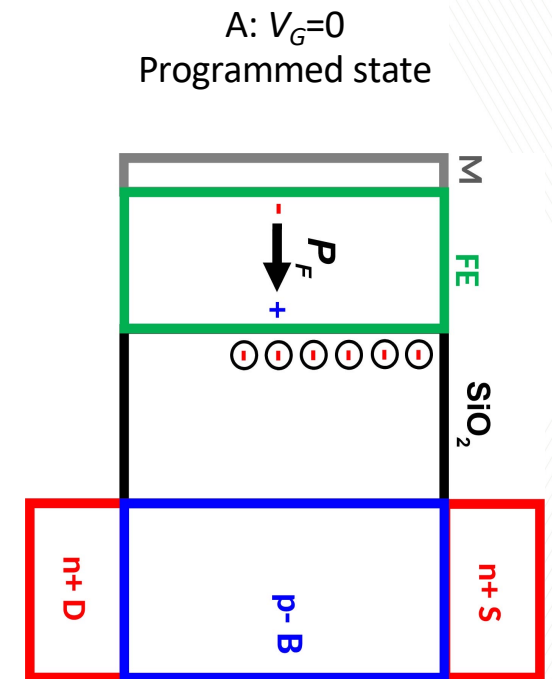
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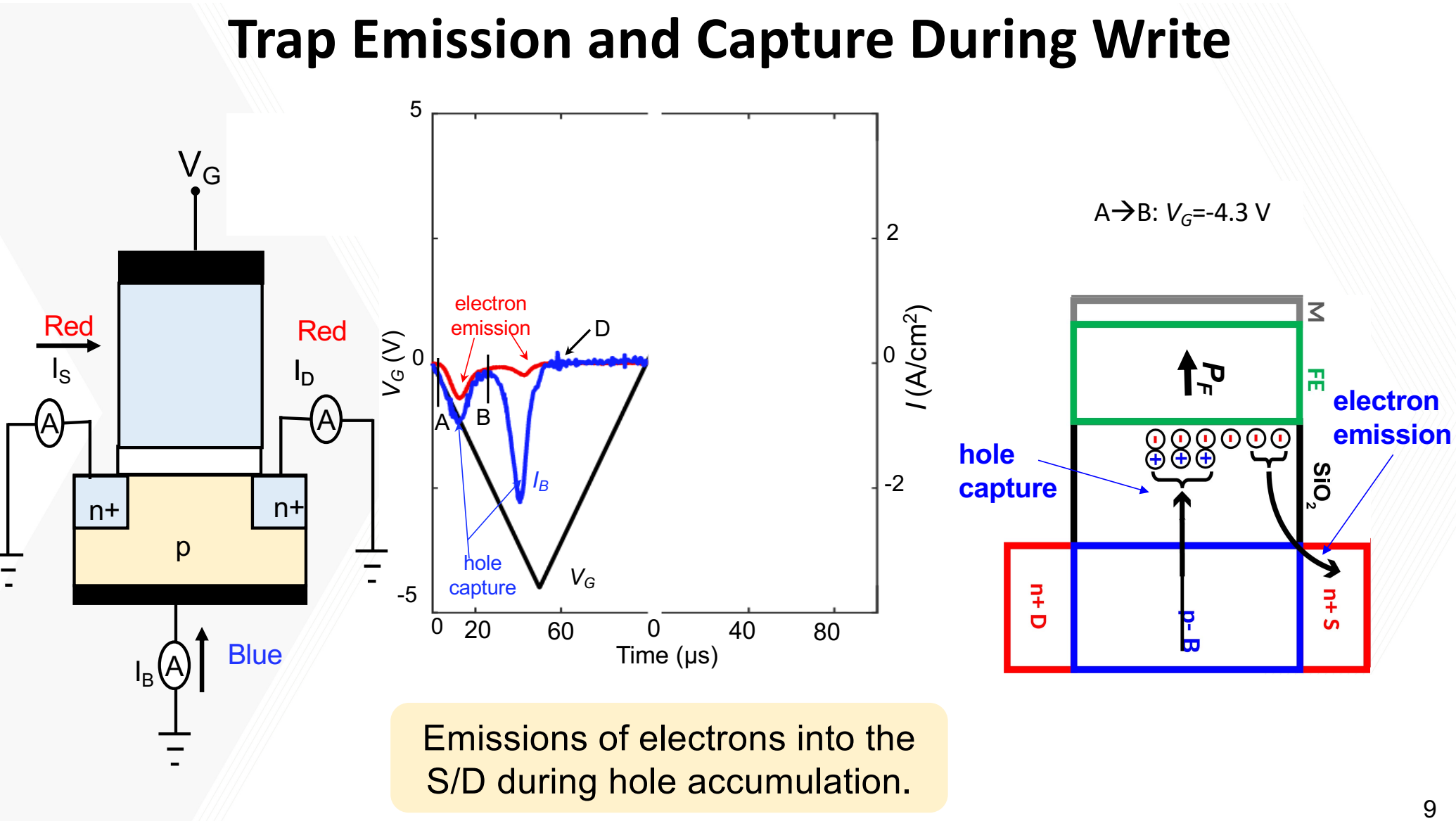
Trap Emission and Capture During Write

The figure illustrates the process of trap emission and capture during a write operation in a 1T1R device. It consists of three main parts:

- Device Schematic:** A cross-sectional diagram of a 1T1R device. The top gate is labeled V_G . The source and drain electrodes are labeled I_S (Red) and I_D (Red). The bottom electrode is labeled I_B (Blue). The device structure shows n^+ regions, a p region, and a SiO_2 layer.
- Graph:** A plot of current I (A/cm²) versus gate voltage V_G (V) and time (μs). The graph shows a red curve for I_S and a blue curve for I_D . The red curve shows a peak labeled "electron emission" and a dip labeled "hole capture". The blue curve shows a peak labeled "hole capture" and a dip labeled "electron emission". The gate voltage V_G is shown as a black line that ramps up and then down. The time axis is marked from 0 to 80 μs .
- Band Diagram:** A schematic diagram of the energy bands. The top band is labeled P_F (Fermi level). The middle band is labeled SiO_2 . The bottom band is labeled n^+D (donor) and n^+S (source). The diagram shows "hole capture" (blue arrow) and "electron emission" (red arrow) processes. The transition is labeled $A \rightarrow B: V_G = -4.3 V$.

Emissions of electrons into the S/D during hole accumulation.

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Trap Emission and Capture During Write

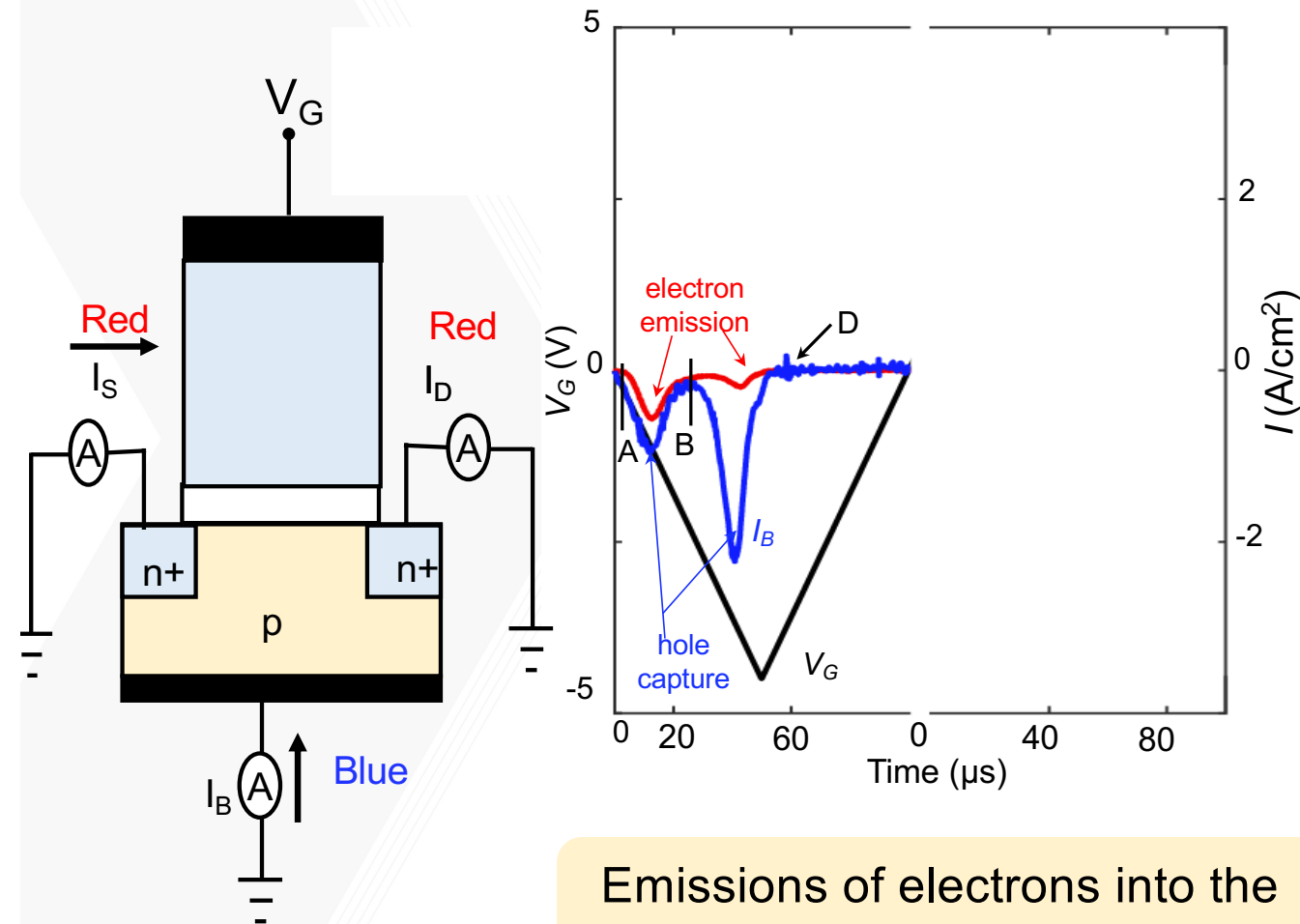
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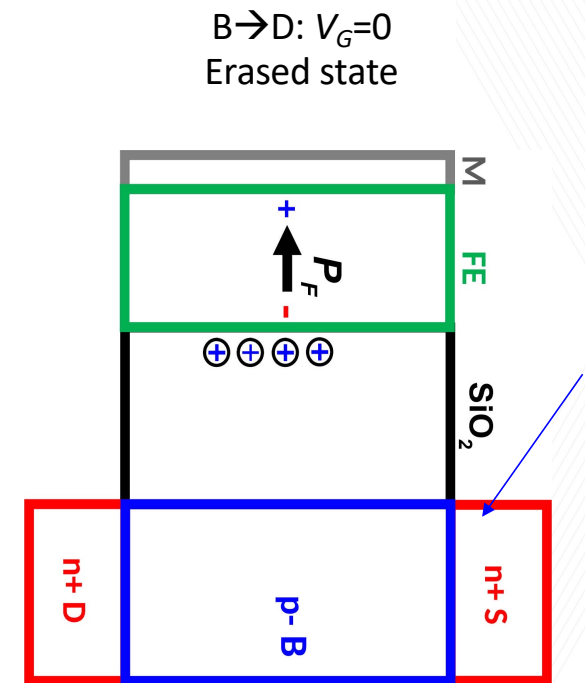
Emissions of electrons into the S/D during hole accumulation.

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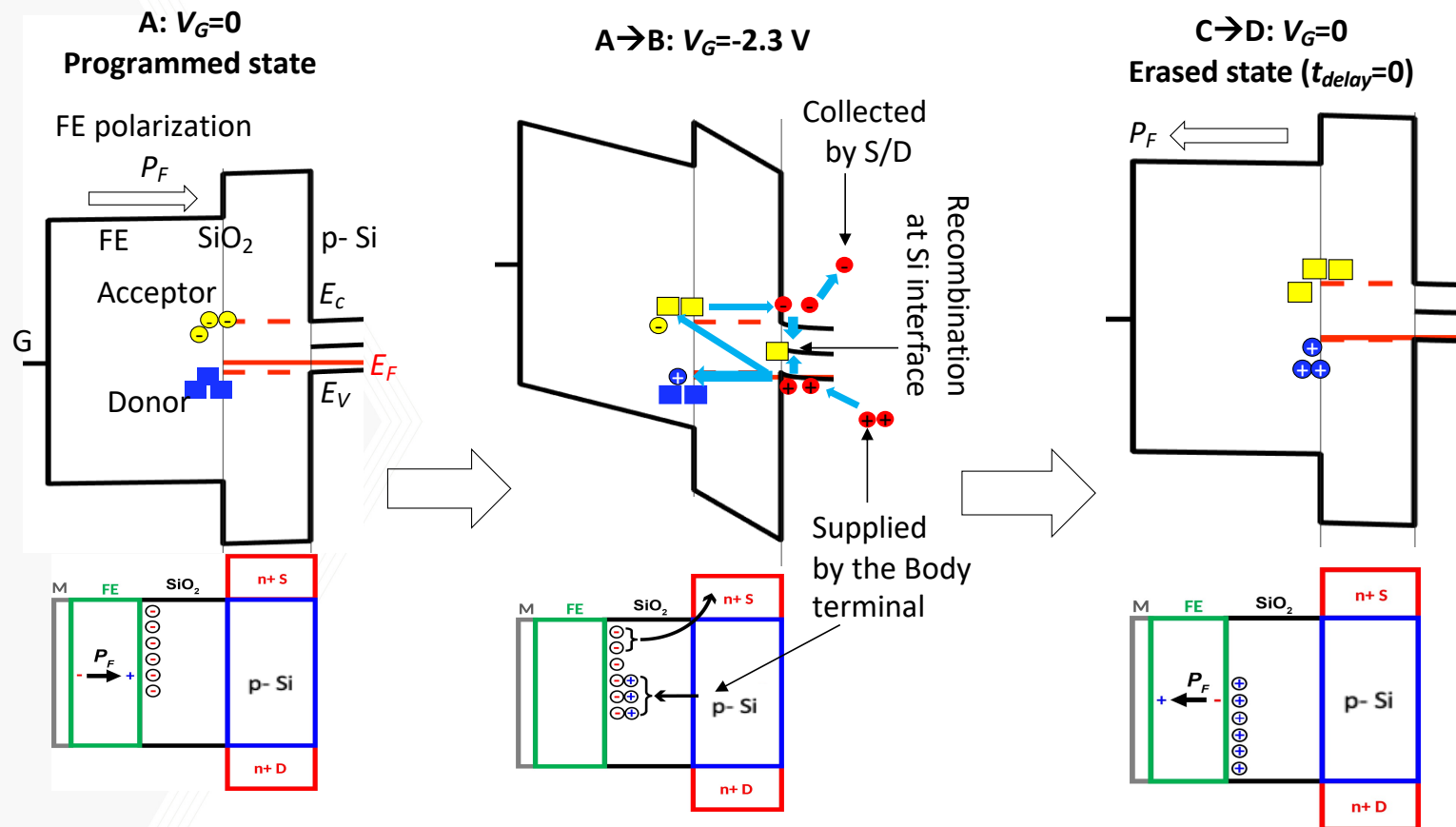
Trap Emission and Capture During Write



Emissions of electrons into the S/D during hole accumulation.



Trap Capture and Emission Dynamics



Tasneem et al. IEDM 2021.

Both acceptor and donor type defects are needed to enable FE switching.

Trap Capture and Emission Dynamics

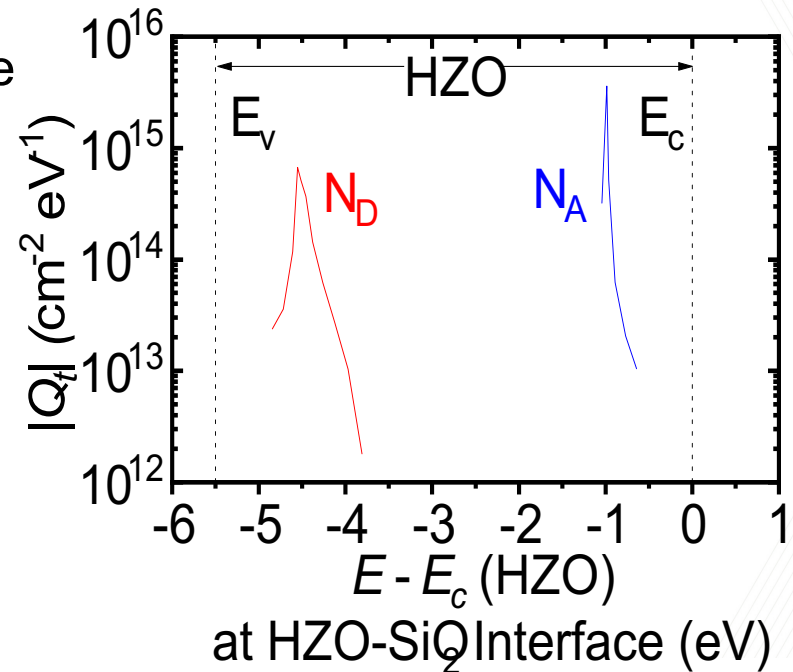
- Trap levels N_D and N_A are essentially discrete levels
- Donor-type trap energy E_D is 0.93 eV above HZO E_v .
- Acceptor type trap energy E_A is 0.98 eV below HZO E_c .

If there were no screening:

$$n_{semi} = P_r = 20 \mu\text{C}/\text{cm}^2 = 1.25 \times 10^{14} / \text{cm}^2$$

$$E_{Si} = \frac{P_r}{\epsilon_0 \epsilon_{Si}} = 18 \text{ MV}/\text{cm}$$

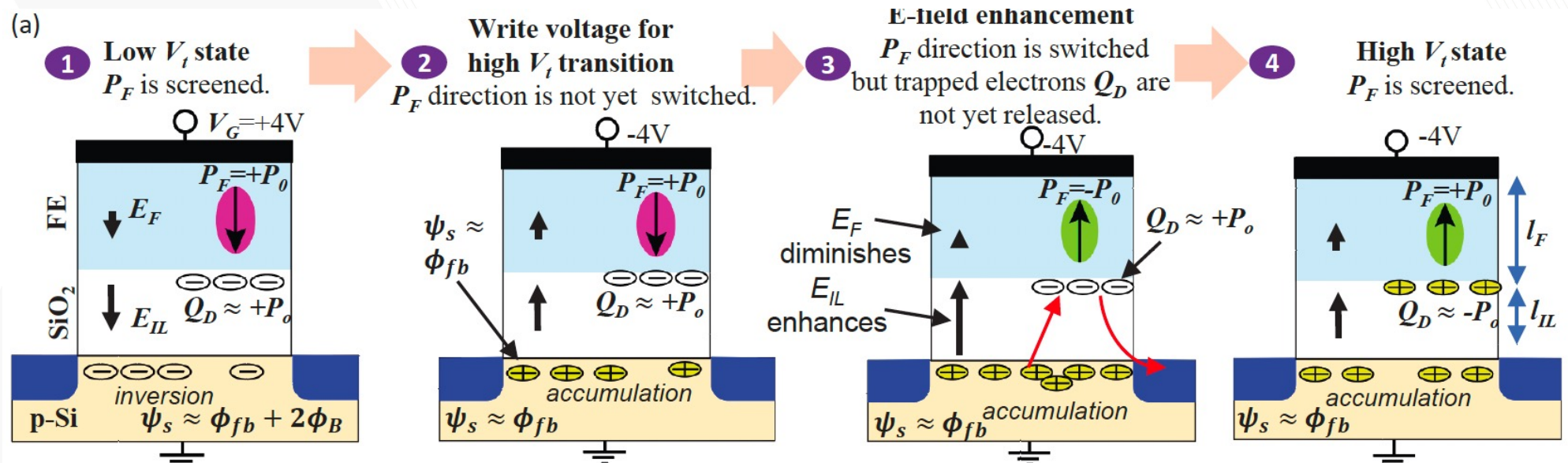
$$E_{ox} = \frac{P_r}{\epsilon_0 \epsilon_{ox}} = 58 \text{ MV}/\text{cm}$$



Passlack, Tasneem et al. IEDM 2022.

Why ferroelectric devices fail?

- Polarization switching is faster than defect dynamics.
- Electric field gets “amplified” due to the lag.



Tasneem et al. (under review).

Take-away

**A lower remnant polarization will lead to
less interface defect and better reliability
in
Ferroelectric Field-Effect Transistors.**

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