~~Domains in ferroelectric semiconductors~~

Why do ferroelectric devices fail?

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2/21/2023

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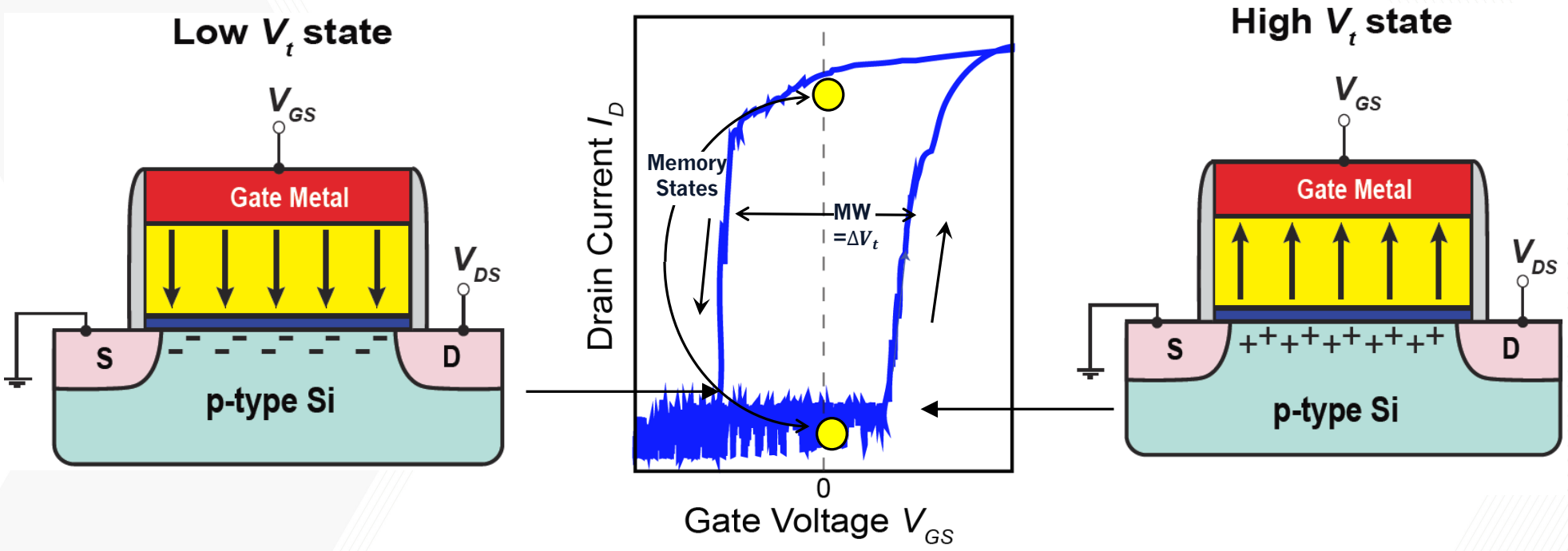
WOCSEMMAD 2023
Workshop on Compound Semiconductor Materials and Devices
February 19–22, 2023 · San Antonio, TX

Ferroelectric field-effect transistors (FEFETs)



FEFET is a FET with the threshold voltage correlated with the polarization state of the ferroelectric layer.

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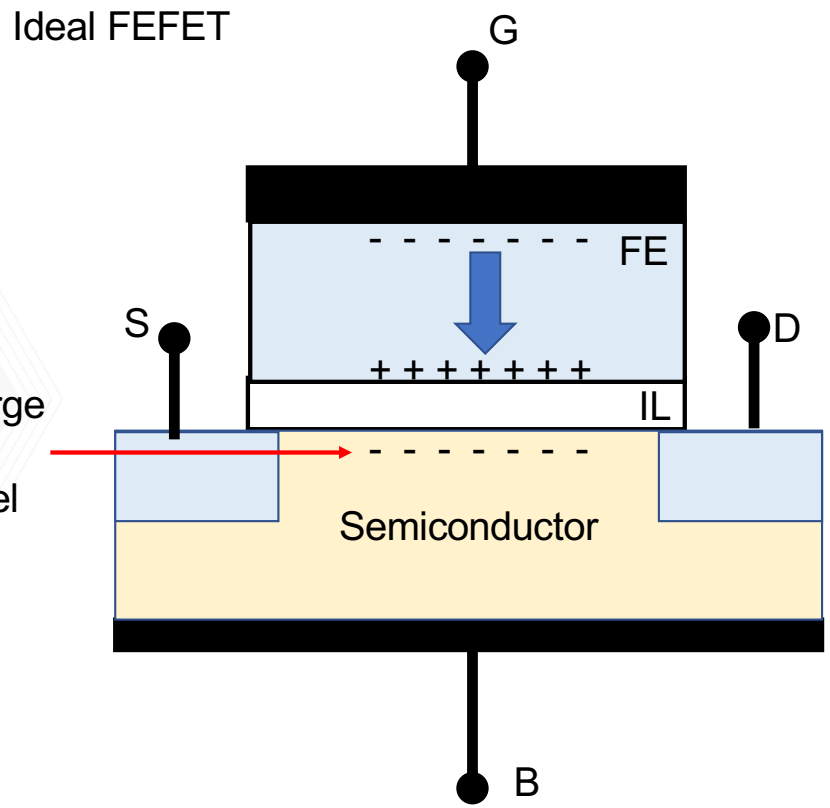
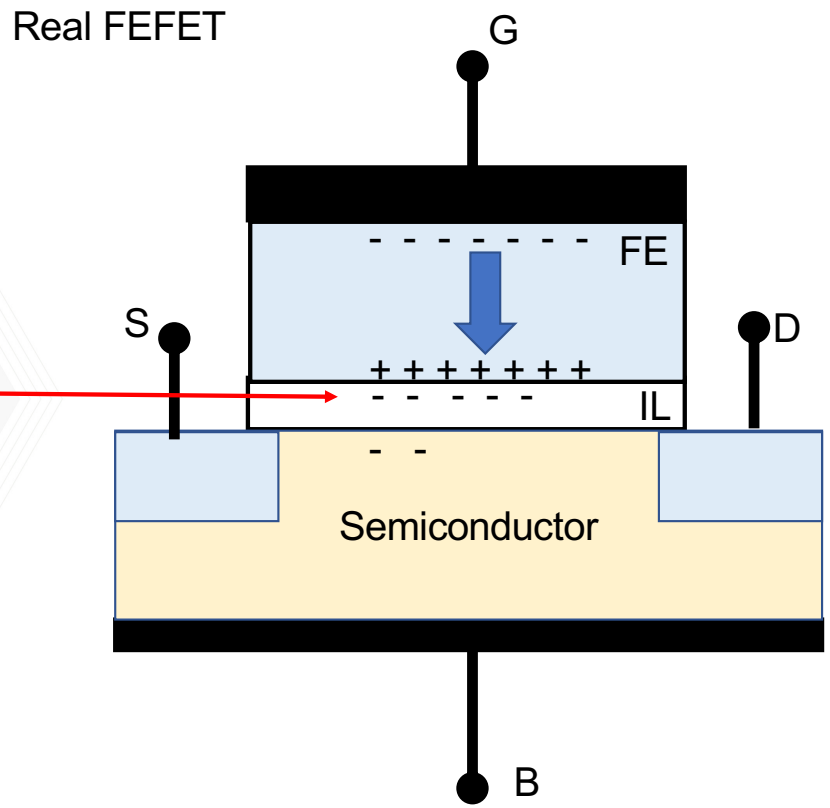
How does a FEFET work?

All of the polarization charge is “reflected” as carriers in the semiconductor channel



How does a FEFET work?

More than 90% of polarization charge is “screened” at the FE interface by defects.



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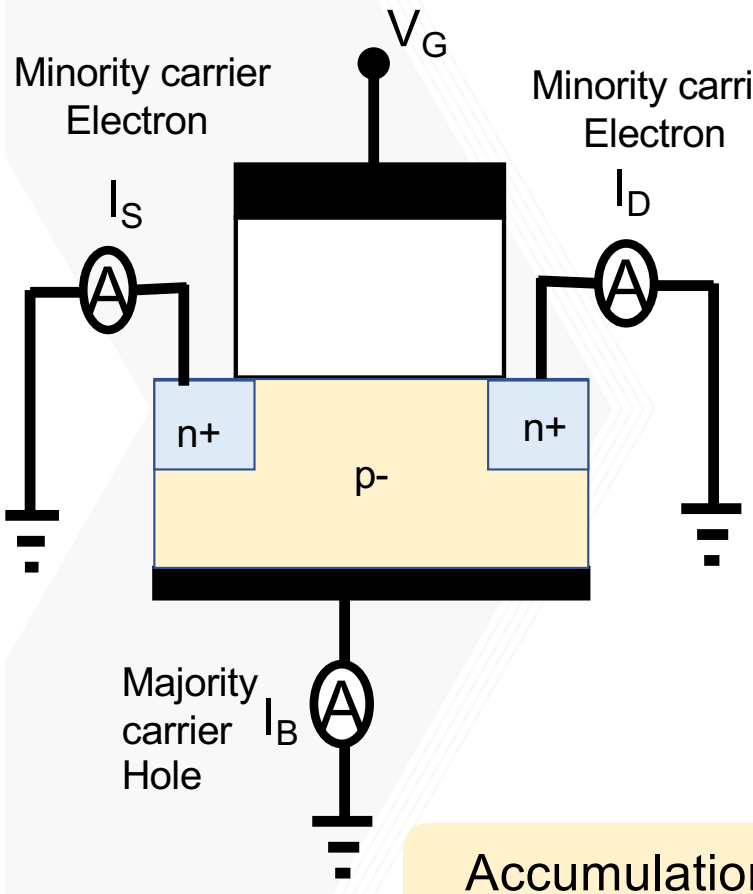
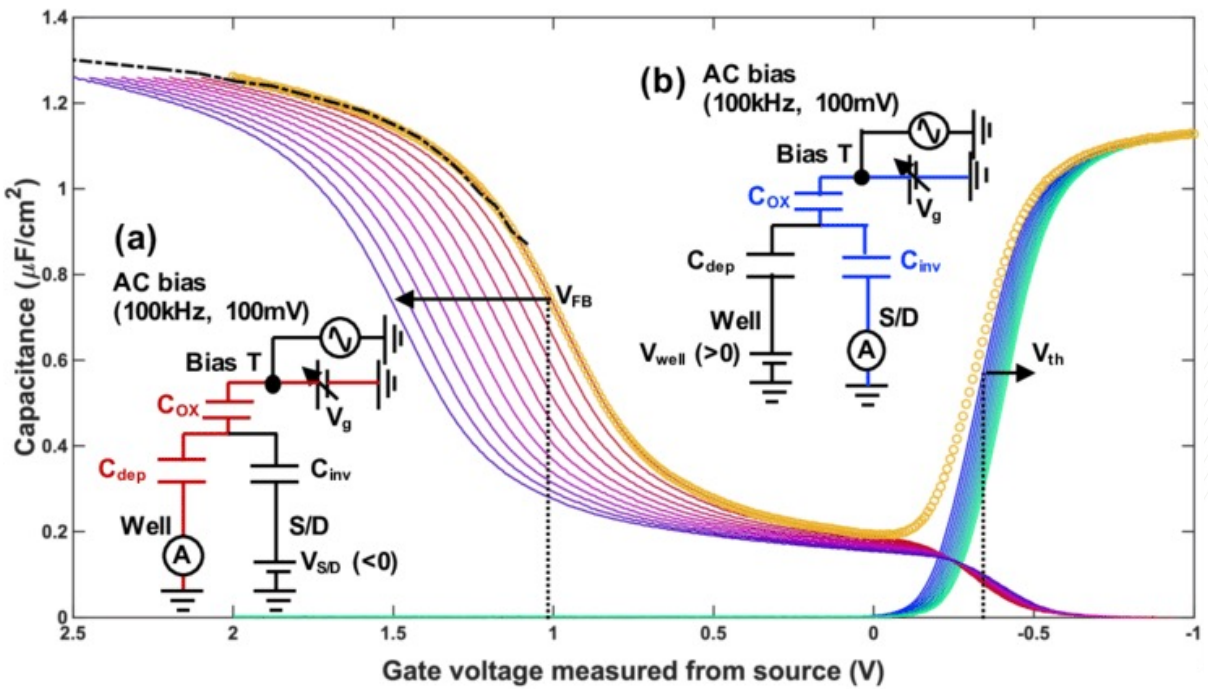
Carrier dynamics in a conventional MOSFET

n-type MOSFET

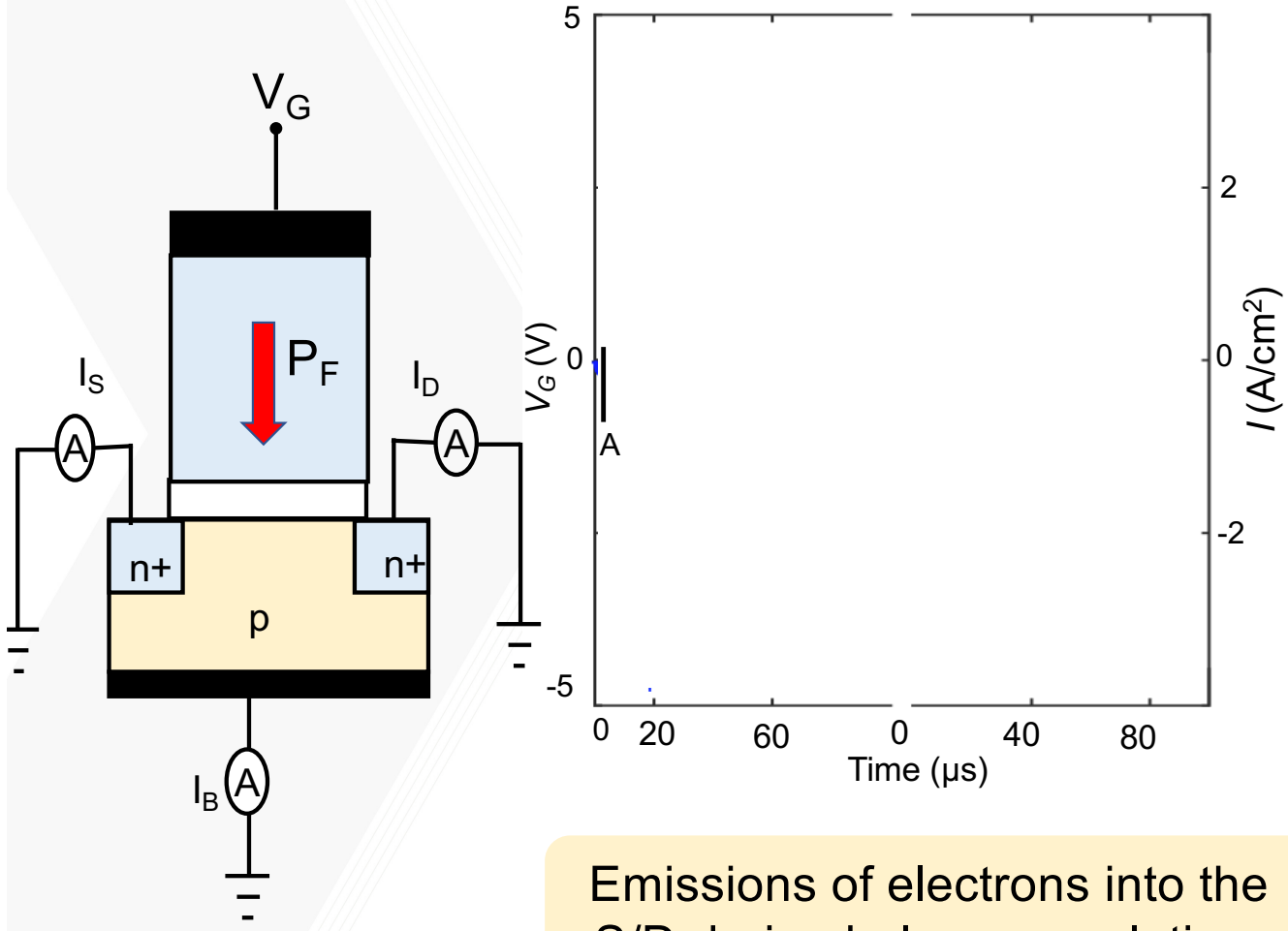


Split CV characteristics of a MOSFET



Accumulation>>only hole from body and no electron from source/drain.

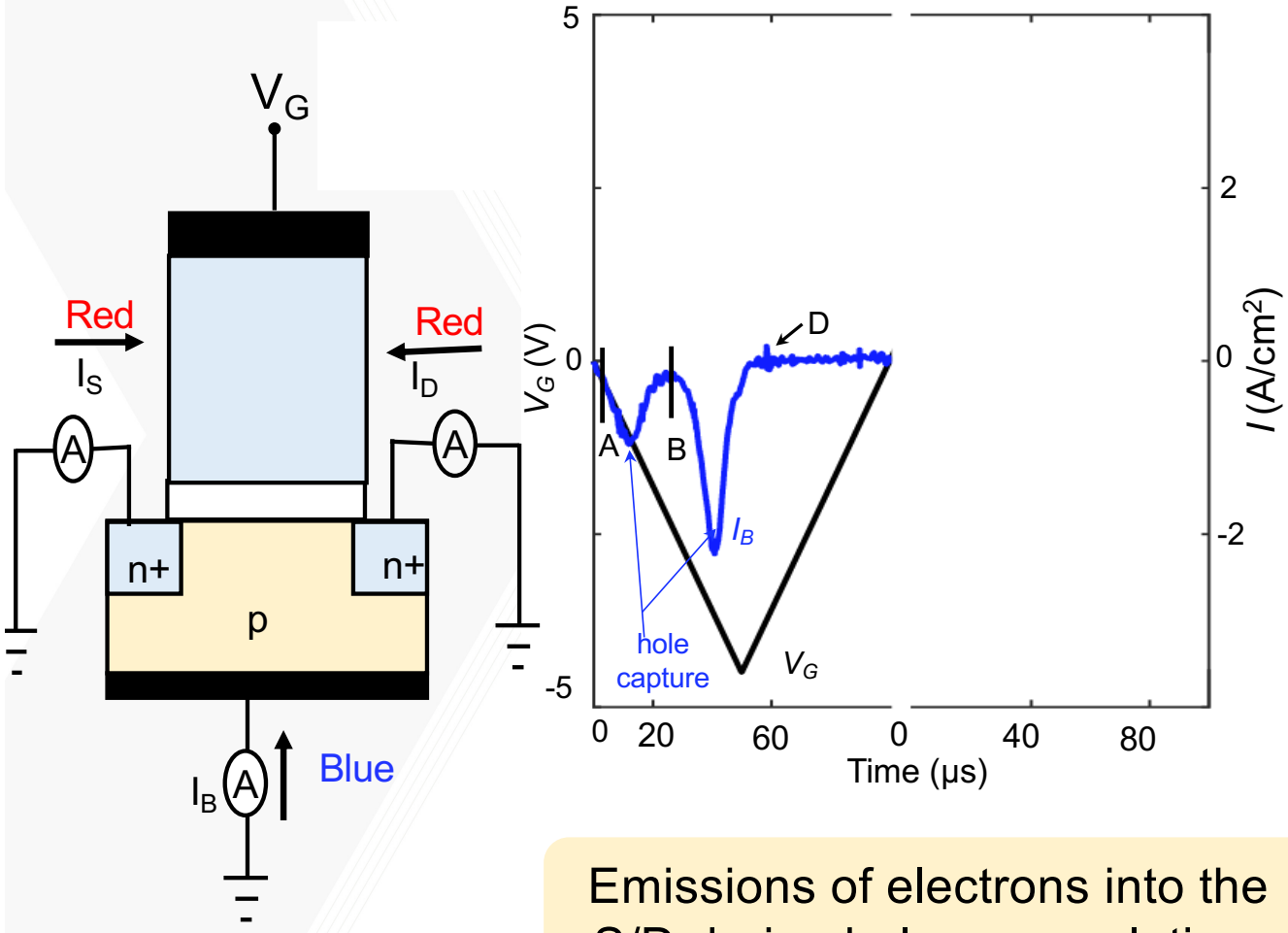
Trap Emission and Capture During Write



Emissions of electrons into the S/D during hole accumulation.

Tasneem et al. Trap Capture and Emission Dynamics in Ferroelectric Field-Effect Transistors and their Impact on Device Operation and Reliability, IEDM 2011.

Trap Emission and Capture During Write



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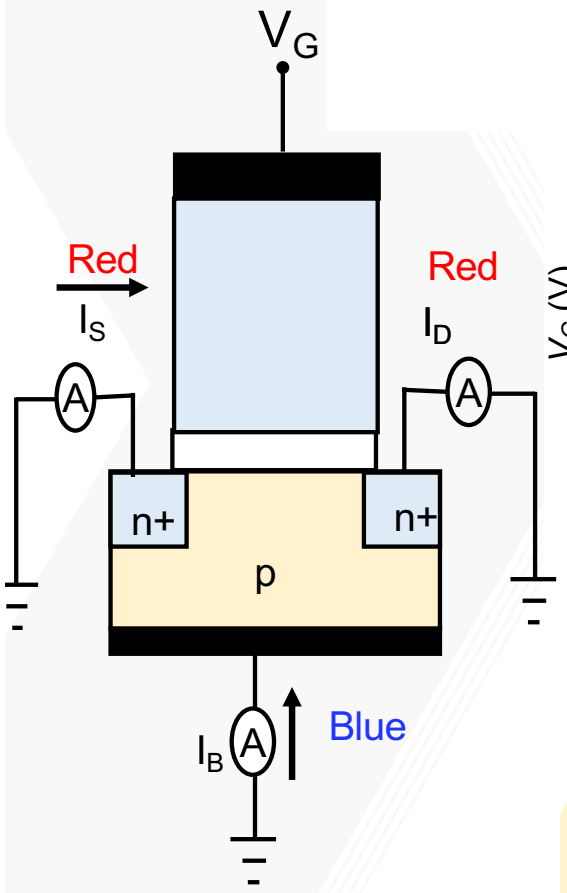

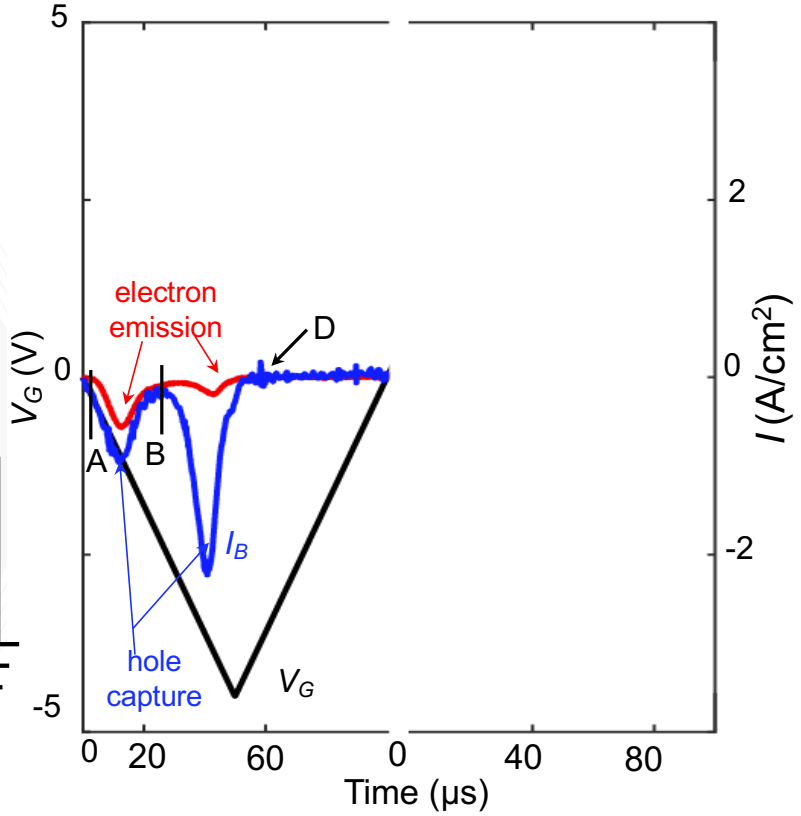

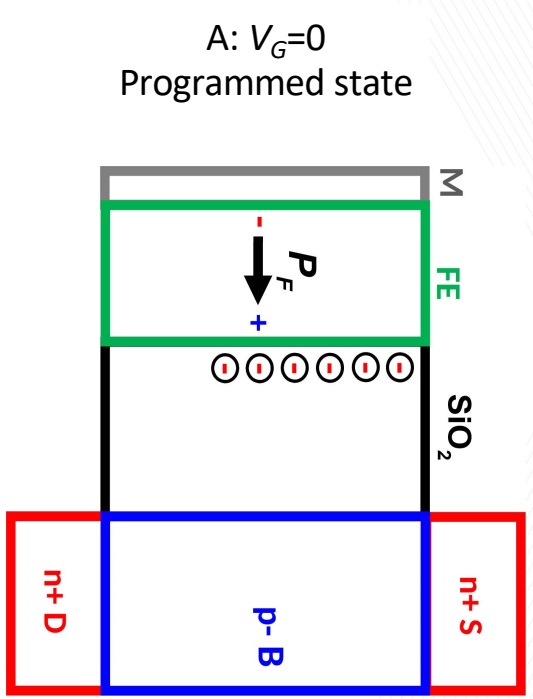

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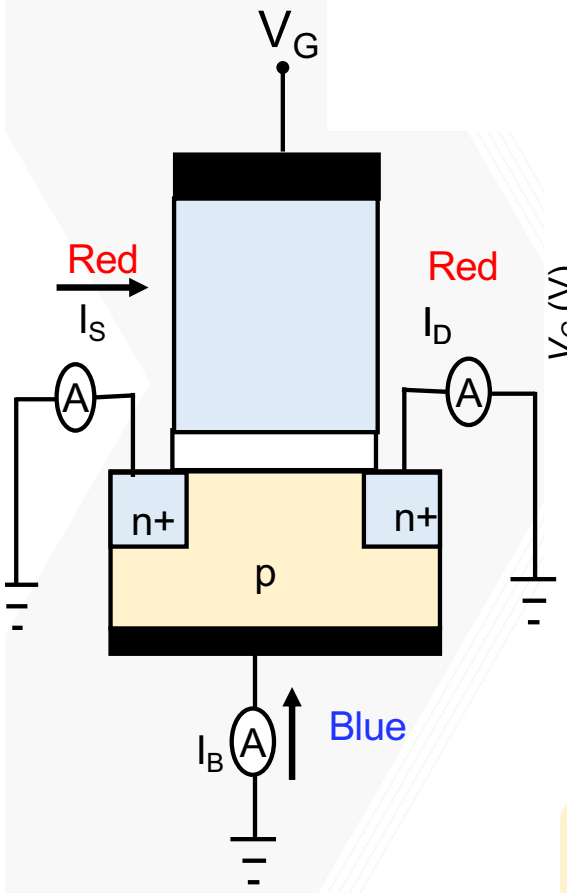
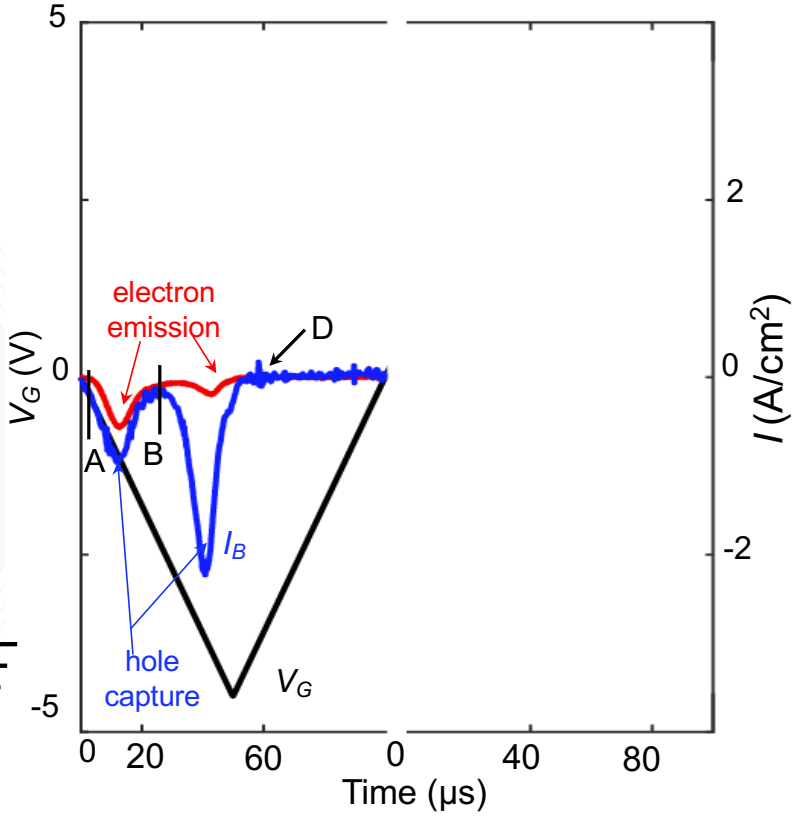
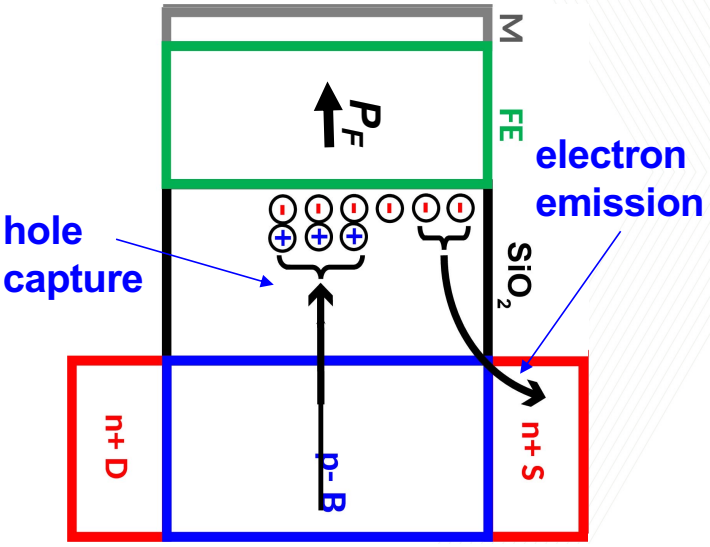


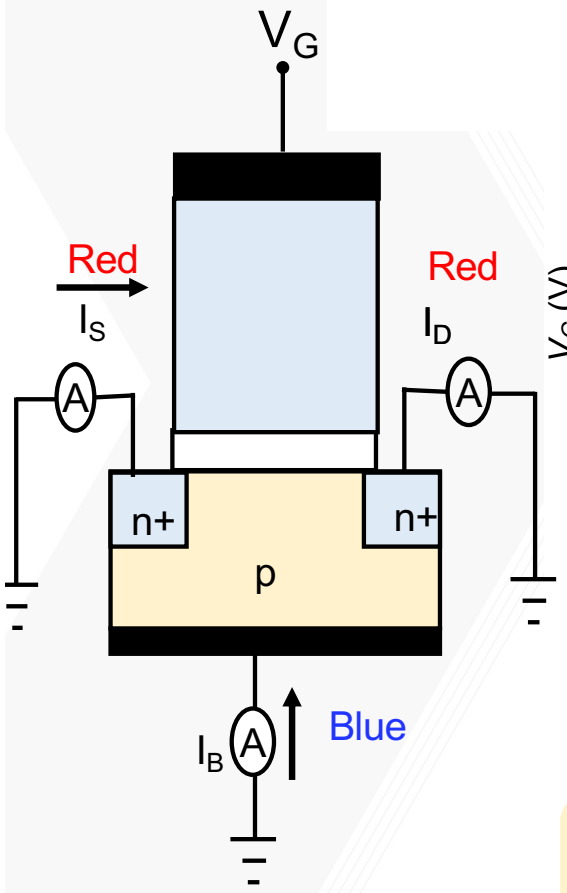


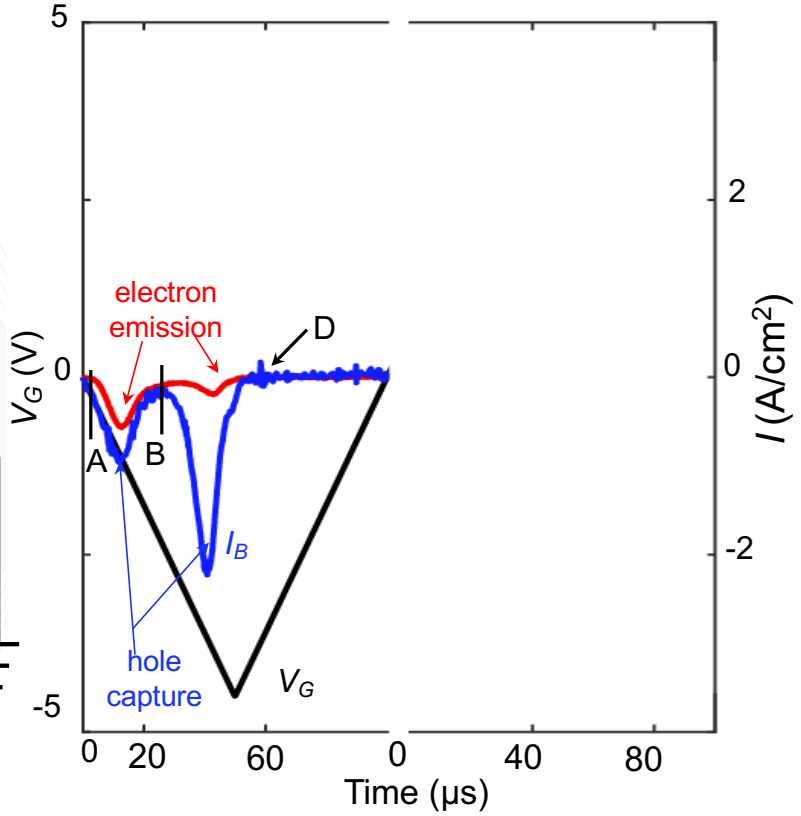
A→B: V_G=-4.3 V



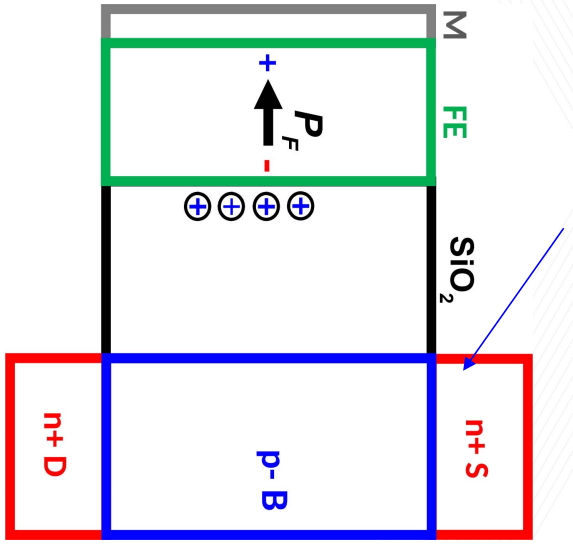
Emissions of electrons into the S/D during hole accumulation.

Trap Emission and Capture During Write



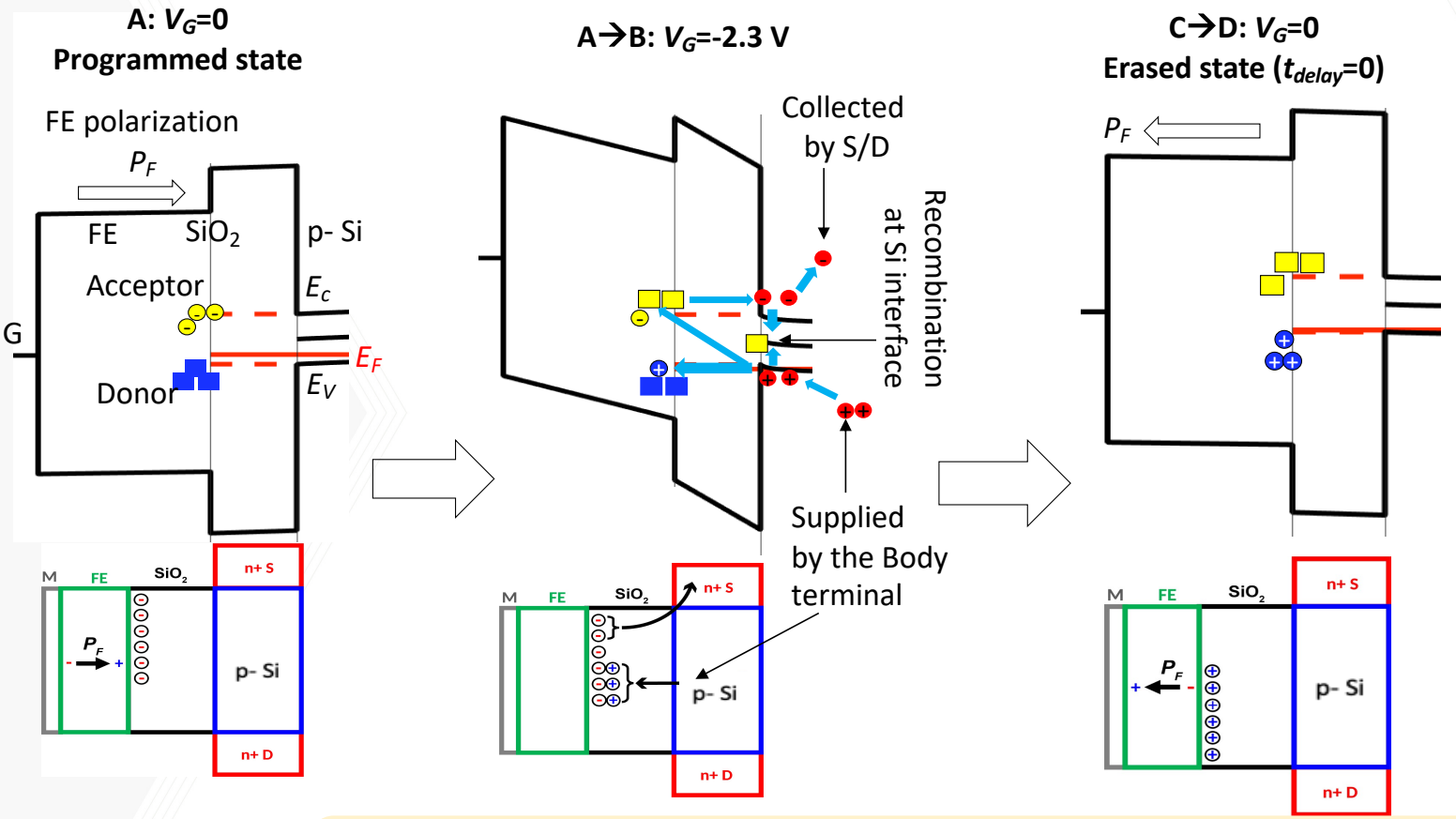


B→D: V_G=0
Erased state



Emissions of electrons into the S/D during hole accumulation.

Trap Capture and Emission Dynamics



Tasneem et al. IEDM 2021.

Both acceptor and donor type defects are needed to enable FE switching.

Trap Capture and Emission Dynamics

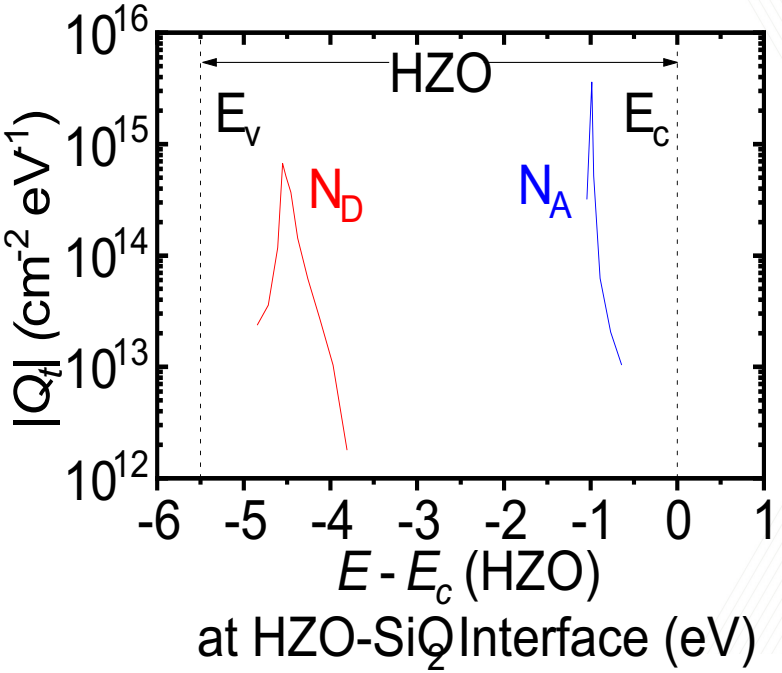
- Trap levels N_D and N_A are essentially discrete levels
- Donor-type trap energy E_D is 0.93 eV above HZO E_v.
- Acceptor type trap energy E_A is 0.98 eV below HZO E_c.

If there were no screening:

$n_{semi} = P_r = 20\ \mu C/cm^2 = 1.25 \times 10^{14}\ /cm^2$

$$E_{Si} = \frac{P_r}{\varepsilon_0 \varepsilon_{Si}} = 18 \text{ MV/cm}$$

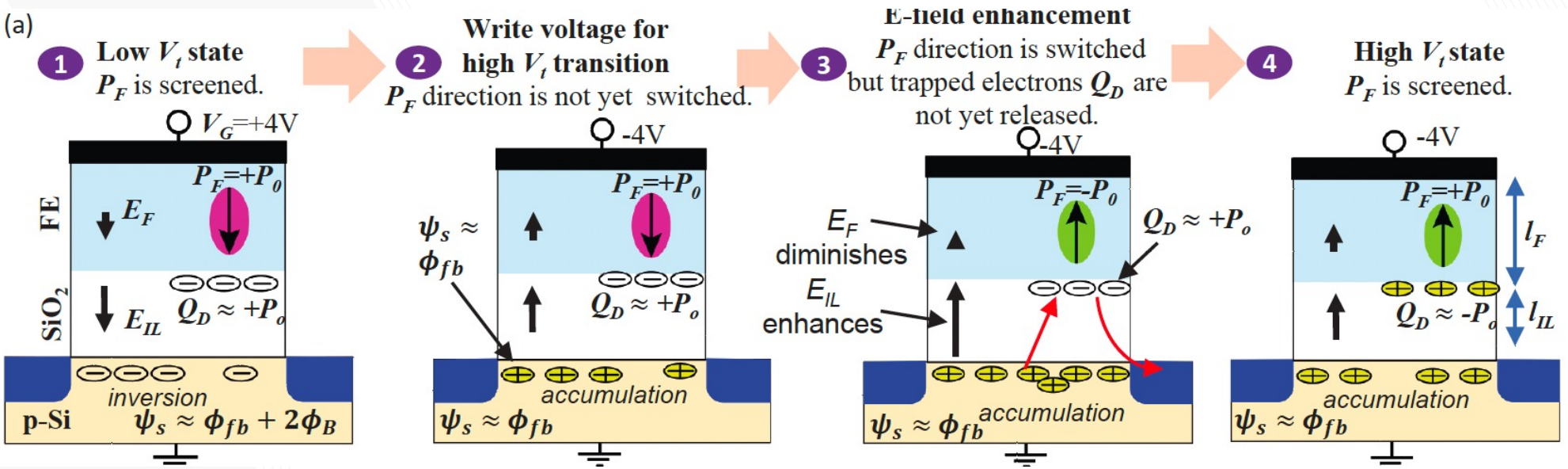
$$E_{ox} = \frac{P_r}{\varepsilon_0 \varepsilon_{ox}} = 58 \text{ MV/cm}$$



Passlack, Tasneem et al. IEDM 2022.

Why ferroelectric devices fail?

- Polarization switching is faster that defect dynamics.
- Electric field gets “amplified” due to the lag.



Tasneem et al. (under review).

Take-away

A lower remnant polarization will lead to

less interface defect and better reliability

in
Ferroelectric Field-Effect Transistors.

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