
# Ferroelectric Field-effect Transistors: Progress and Challenges

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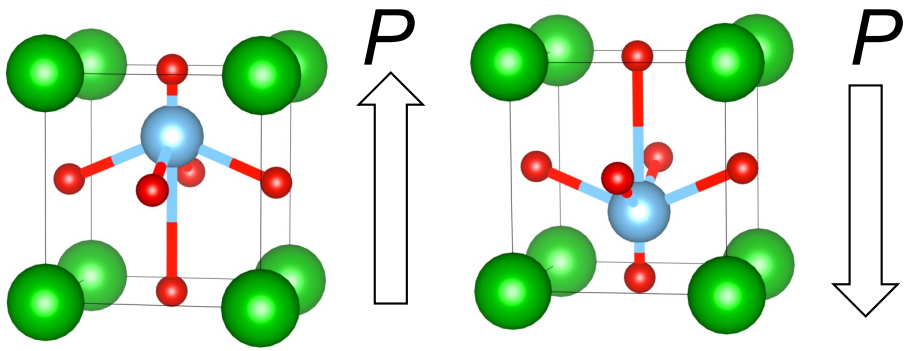
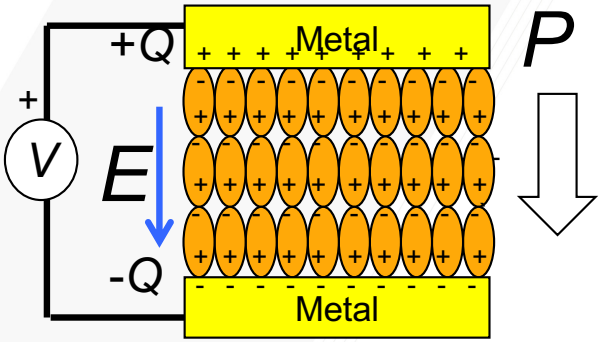
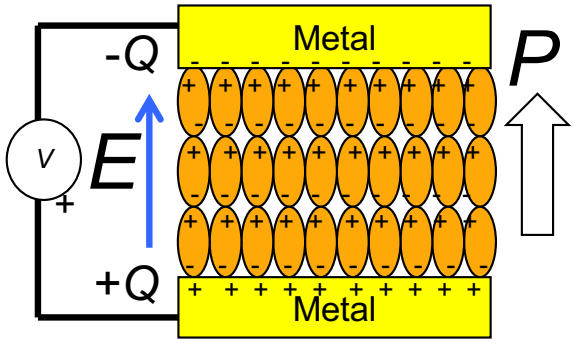
# Ferroelectricity

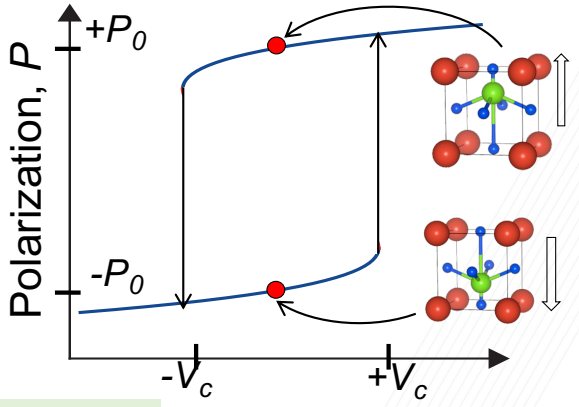
Classical Ferroelectric
$PbTiO_3$ , $BaTiO_3$ etc.

Emerging CMOS compatible
Ferroelectrics:
Doped $HfO_2$




A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

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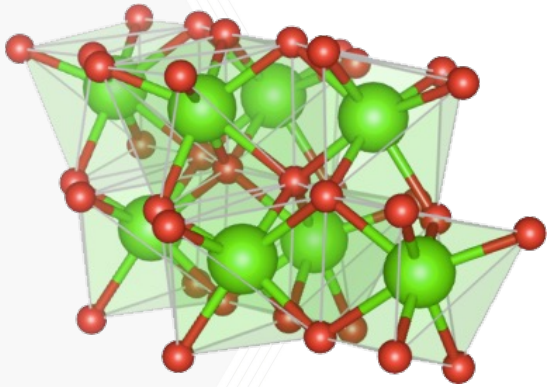
# A historical perspective

- Semiconductor community was heavily invested in Perovskite based FEs in 1990s and 2000s.
- FRAM products with perovskite-based FE were commercialized; total market cap ~1B$.
- Ferroelectrics activities in semiconductor community slowed down because perovskites are not scalable below 130 nm node.
- 2011! discovery of ferroelectricity in CMOS compatibility in $HfO_2$ renewed the interests

# CMOS compatible ferroelectrics

New class of ferroelectric and antiferroelectric materials have emerged which can be introduced in commercial fabs!



Controlled annealing in $HfO_2$ doped with Zr, Al, Si, Sr, Ti, La etc. induces a ferroelectric orthorhombic phase!

Boscke et al APL 99, 112904 (2011)
Boscke et al IEDM 2011

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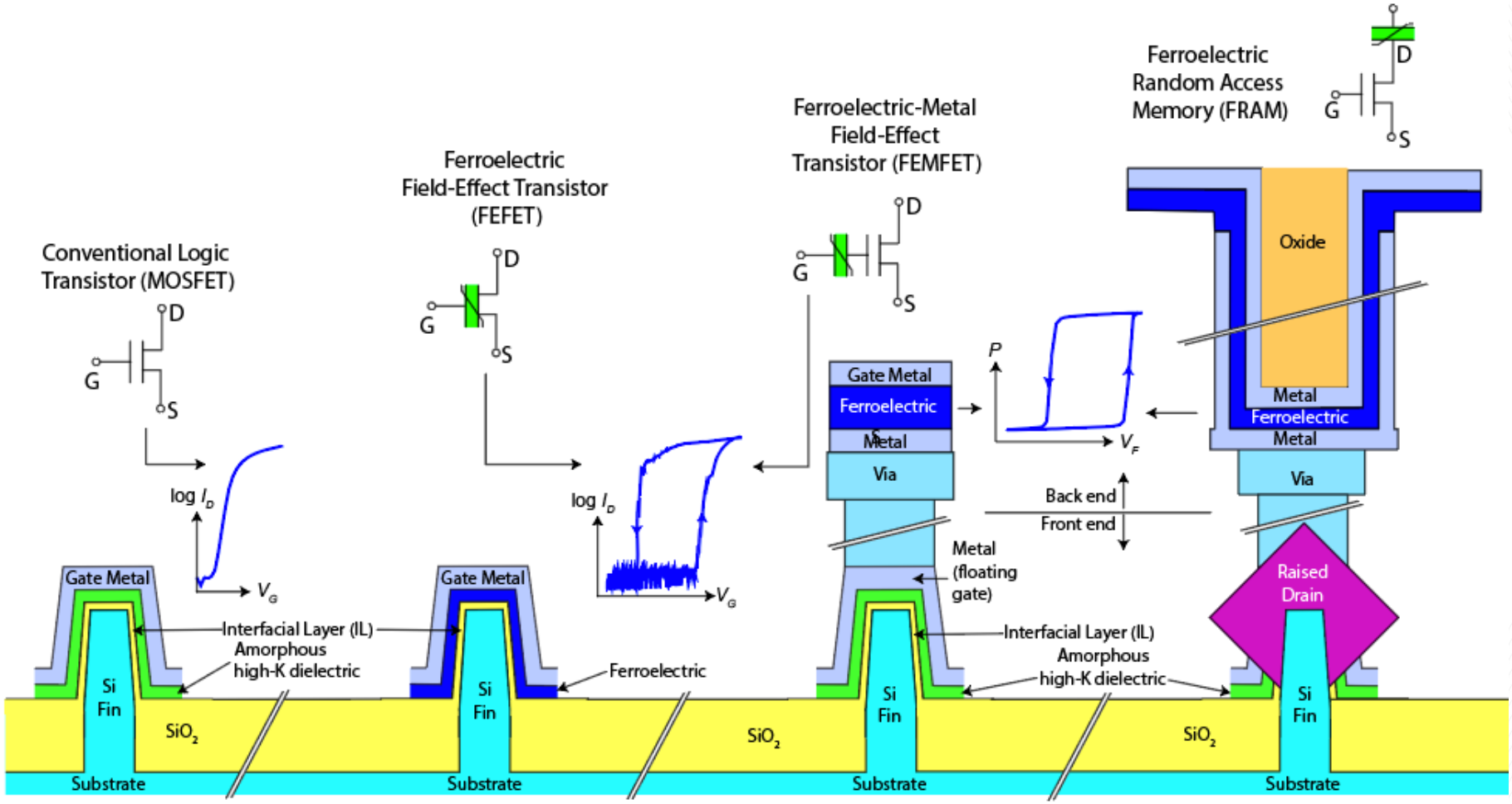
# Ferroelectric devices (1 of 2)




Khan, Keshavarzi, Datta, “The future of ferroelectric field-effect transistor technology”, Nature Electronics 2020

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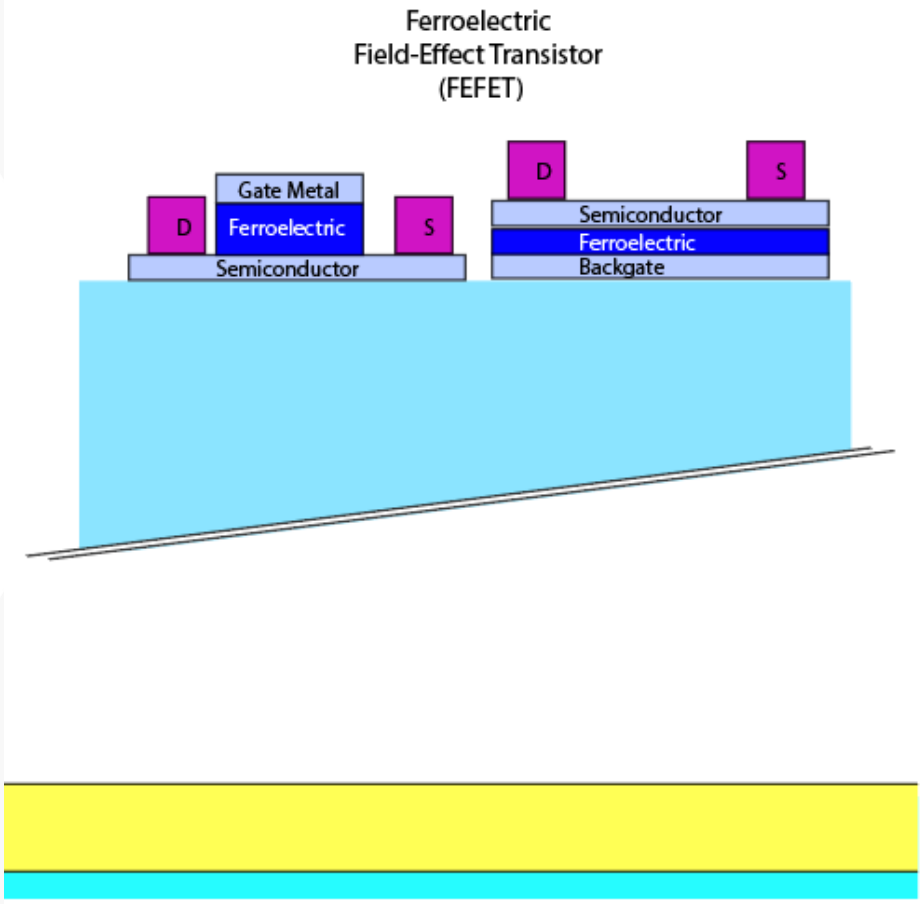
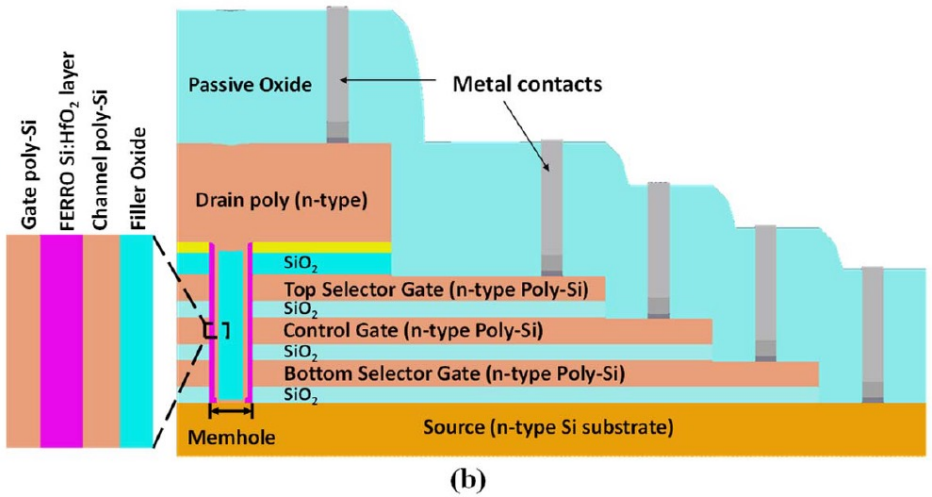
# Ferroelectric devices (2 of 2)

BEOL FEFET




Vertical FEFET for NAND Storage

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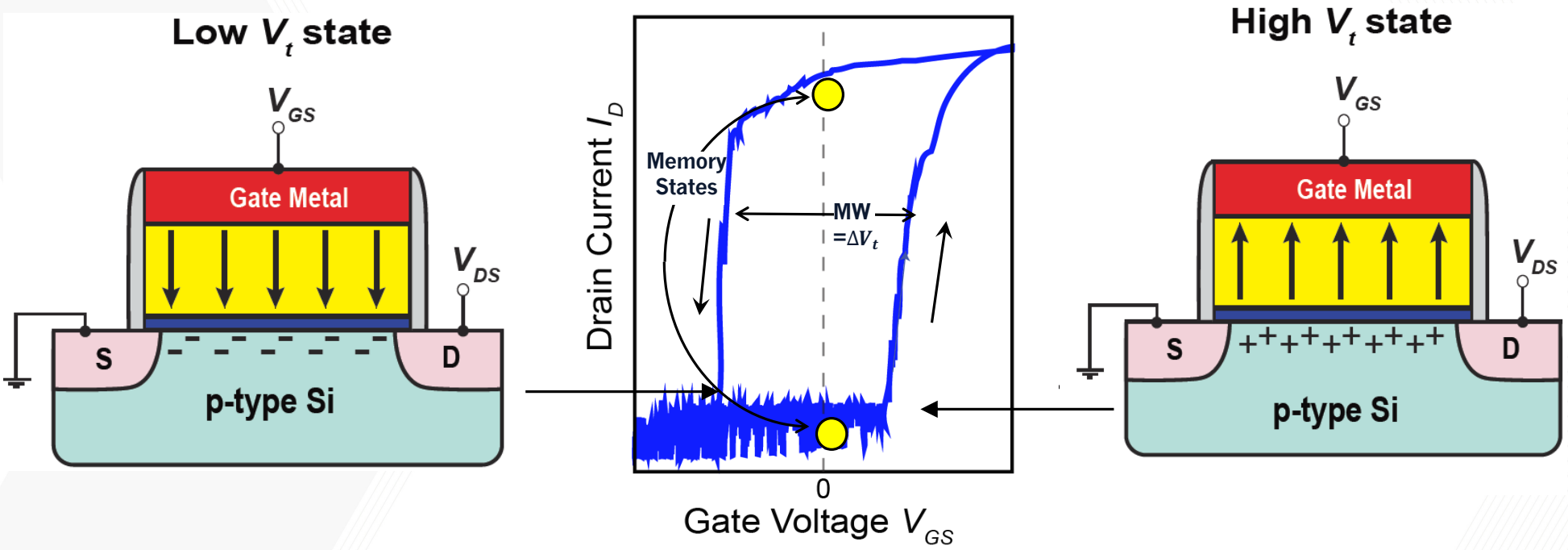
# Ferroelectric field-effect transistors (FEFETs)




FEFET is a FET with the threshold voltage shifted by the remnant polarization.

# FEFET as an embedded memory

| Metrics | Mainstream embedded memory | | | | | Embedded ferroelectric memory | | | |
|---|---|---|---|---|---|---|---|---|---|
| | eSRAM | eDRAM[70] | eFlash (FG) | eFlash (SG MONOS)[42] | eFlash (SONOS)[41] | FEFET (hafnia based, MFIS structure) | FEFET (hafnia based, MFMIS structure) | FRAM (hafnia based) | FRAM (perovskite based)[67] |
| Cell size | 120–150$F^2$ | 40$F^2$ | 40–60$F^2$ | 40–50$F^2$ | 50–60$F^2$ | 10–30$F^2$ | 10–30$F^2$ | 30–40$F^2$ | 50–60$F^2$ |
| Cell structure | 6T | 1T1C | 1.5T | 1.5T | 2T | 1T | 1T1FE, 1T | 1T1FE, 2T2FE | 1T1FE, 2T2FE |
| Non-volatile | No | No | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Multi-bit operation | No | No | Yes | Yes | Yes | Yes | Yes | No | No |
| Non-destructive read | Yes | No | Yes | Yes | Yes | Yes | Yes | No | No |
| Status | Av. | Dev. | Av. | Dev. | Dev. | Res. | Res. | Res. | Av. |
| Advanced node demonstration | 7 nm FinFET | 22 nm FinFET | 40 nm | 16 nm FinFET | 28 nm HKMG | 22 nm FDSOI | N/A | N/A | 130 nm |
| Write voltage | <1 V | <1 V | ~12 V | ~12 V | ~5 V | 1.5–4 V | ~1.5 V | 1–3 V | 1.5 V |
| Write energy | ~1 fJ | ~1 pJ | ~100 pJ | ~100 pJ | 1–10 pJ | 1–10 fJ | 1–10 fJ | ~100 fJ | ~1 pJ |
| Standby power | High | Medium | Low | Low | Low | Low | Low | Low | Low |
| Write speed | <1 ns | >10 ns | ~100 ns | <100 ns | ~100 ns | 1–10 ns | 1–10 ns | 1–10 ns | 1 µs |
| Read speed | <1 ns | >10 ns | ~10 ns | <10 ns | ~10 ns | 1–10 ns | 1–10 ns | 1–25 ns | 50–100 ns |
| Endurance | >$10^{16}$ | >$10^{16}$ | ~$10^4$ | ~$10^5$ | ~$10^6$ | $10^5$–$10^9$ | >$10^{10}$ | >$10^{12}$ | >$10^{14}$ |

Khan, Keshavarzi, Datta, “The future of ferroelectric field-effect transistor technology”, Nature Electronics 2020

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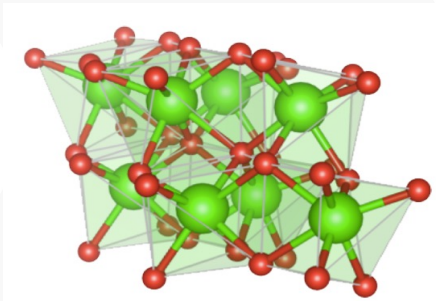
# Ferroelectric field-effect transistor

Ferroelectric Oxide



Properties of Ferroelectric oxides

- Non-volatility and hysteresis
- Plasticity, Meta-plasticity and Anti-plasticity
- Negative dielectric permittivity/negative capacitance
- Stochasticity

Ferroelectric FET is one of most versatile transistor technologies – ever conceived.

Khan, Keshavarzi, Datta. “The future of ferroelectric field-effect transistors.” *Nature Electronics* 3, 588 (2020).

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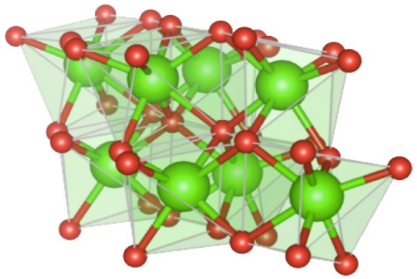
Ferroelectric Oxide



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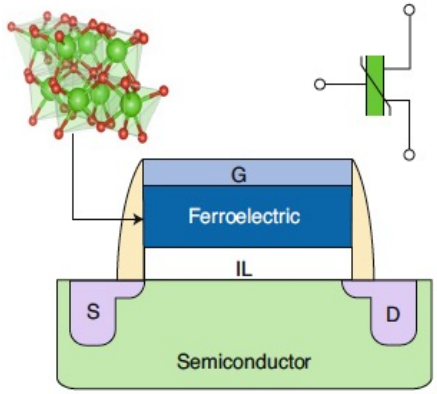
Properties enabled by a transistor structure

- Transistor physics
- Transconductance gain
- Circuit-level design

Ferroelectric field-effect transistor

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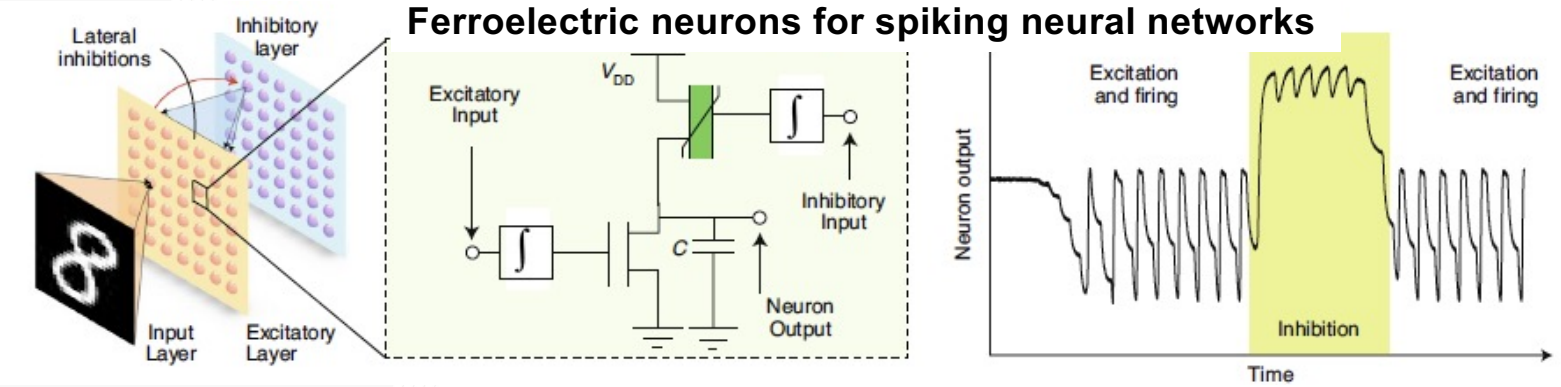
# Ferroelectric FET Applications

1

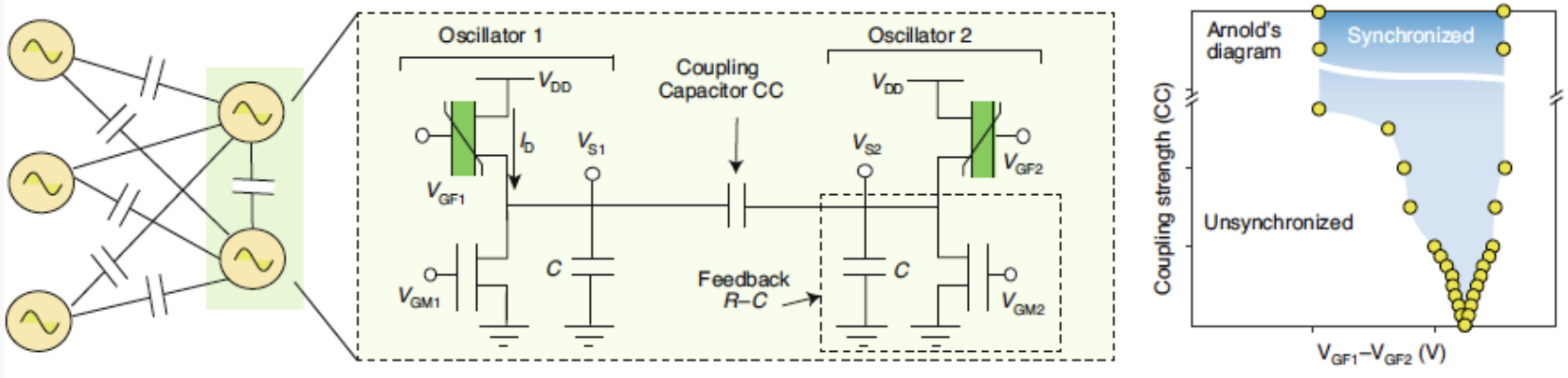
## Ferroelectric neurons for spiking neural networks




Wang et al. Int. Electron Dev. Meeting (IEDM) 2018.

2

## Ferroelectric oscillators for time dynamical systems




Z. Wang et al. EDL 2017

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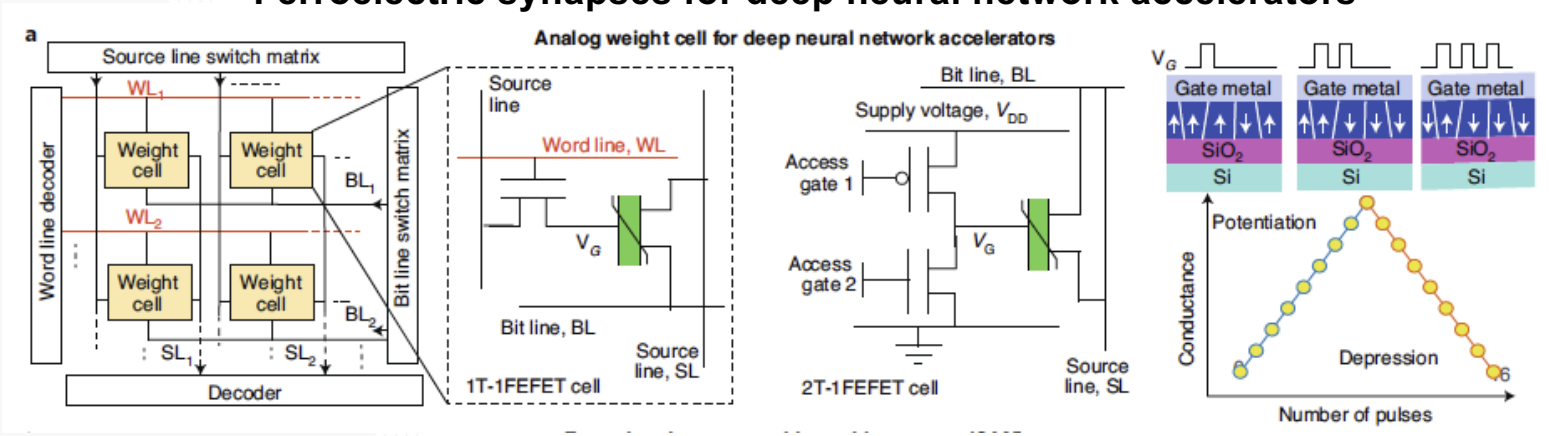
# Ferroelectric FET Applications

3

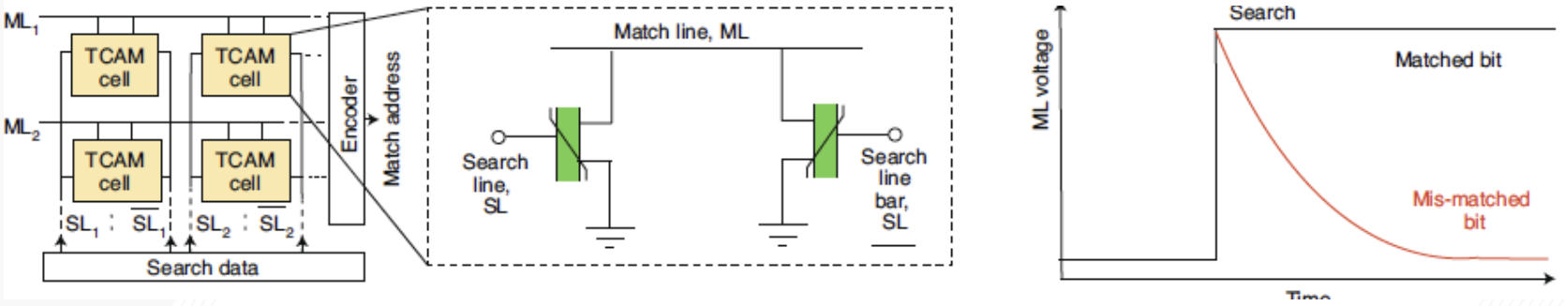
## Ferroelectric synapses for deep neural network accelerators




Aabrar et al. A Thousand State Superlattice (SL) FEFET Analog Weight Cell. VLSI Symp. 2022.

4

## Ferroelectric content addressable memory (CAM)




Tan et al. IEEE EDL 41, 240 (2019)

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# Progress in FEFET technology

| 1<br>Write voltage<br>and Memory Window | 2<br>Read/Write<br>Speed | 3<br>Device-to-device<br>variation | 4<br>Reliability and endurance |
|---|---|---|---|
| **Specs** | | | |
| <1.5 V write voltage<br>>0.5 V memory window | <10 ns write speed<br><10 ns read-after-write delay | $\Delta V_{t,3\sigma}$ = 20-50 mV<br>(7 nm node) | >$10^{12}$ cycles |

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# Progress in FEFET technology

| 1 | 2 | 3 | 4 |
|---|---|---|---|
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**Specs**

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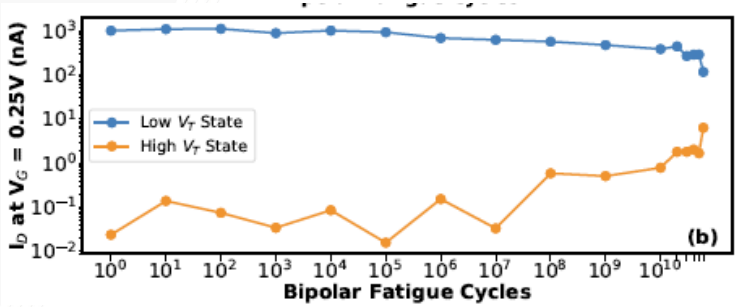
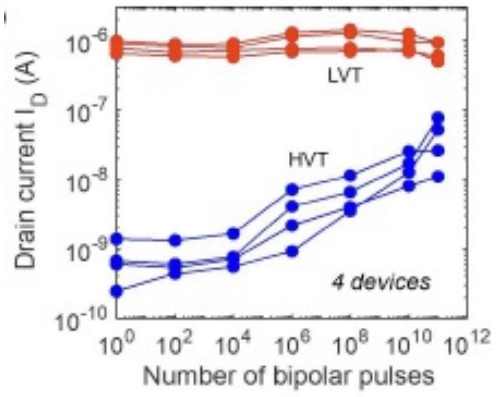



Tan et al. IEEE EDL 42, 994 (2021).




Dutta et al. IEEE EDL 43, 383 (2022).

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# Progress in FEFET technology

**1** Write voltage and Memory Window

**2** Read/Write Speed

**3** Device-to-device variation

**4** Reliability and endurance

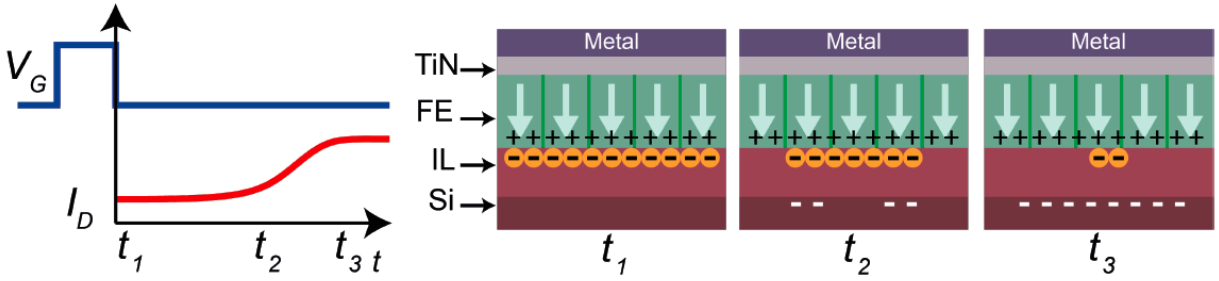
**Specs**

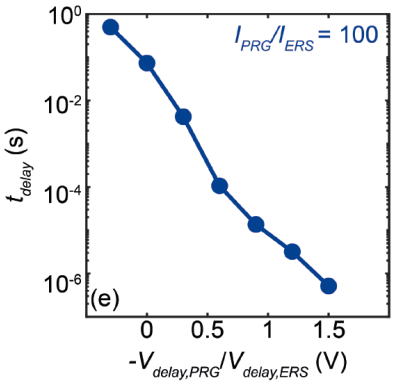
<1.5 V write voltage
>0.5 V memory window

<10 ns write speed
<10 ns read-after-write delay

$\Delta V_{t,3\sigma}$ = 20-50 mV
(7 nm node)

>$10^{12}$ cycles




Wang et al. IEDM (2021).

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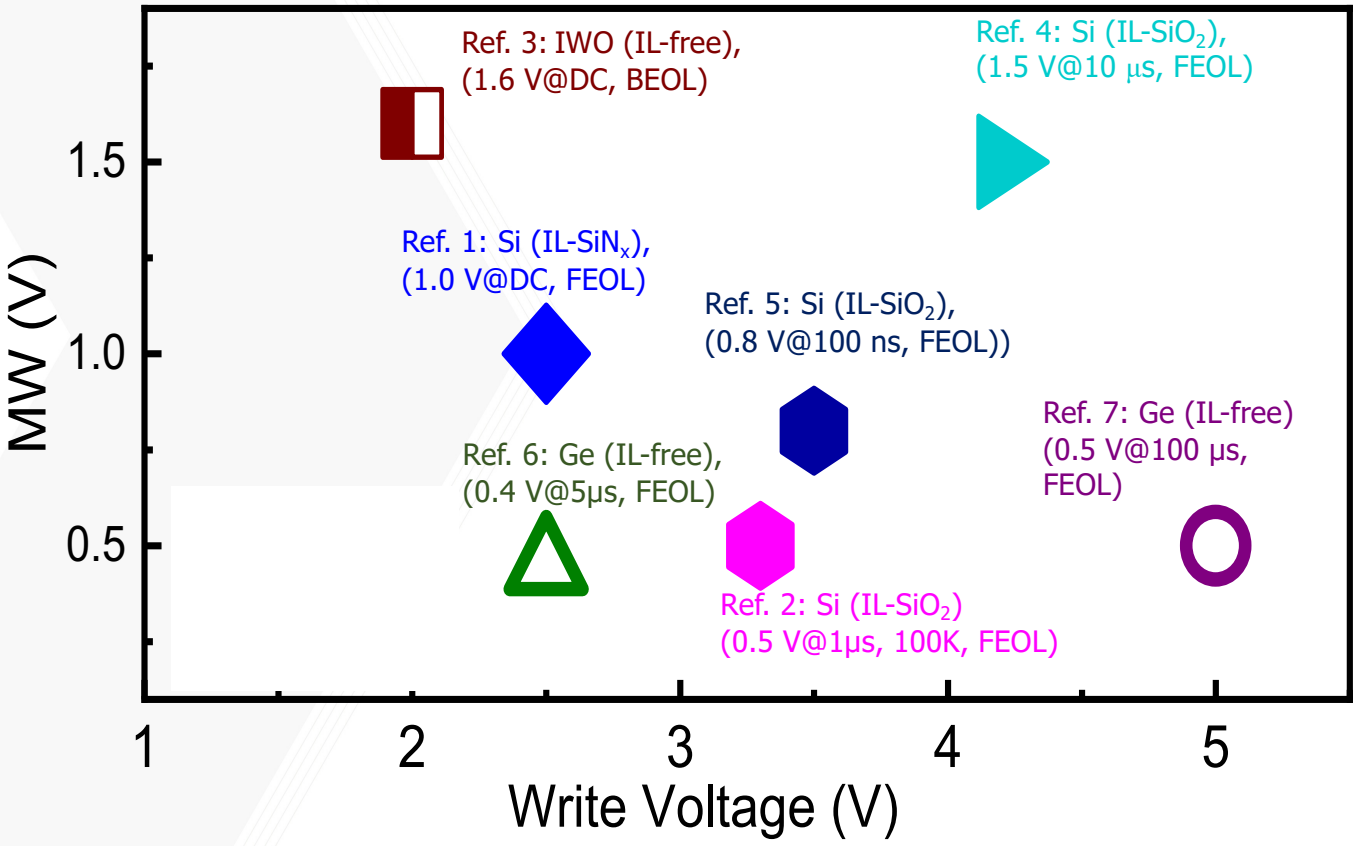
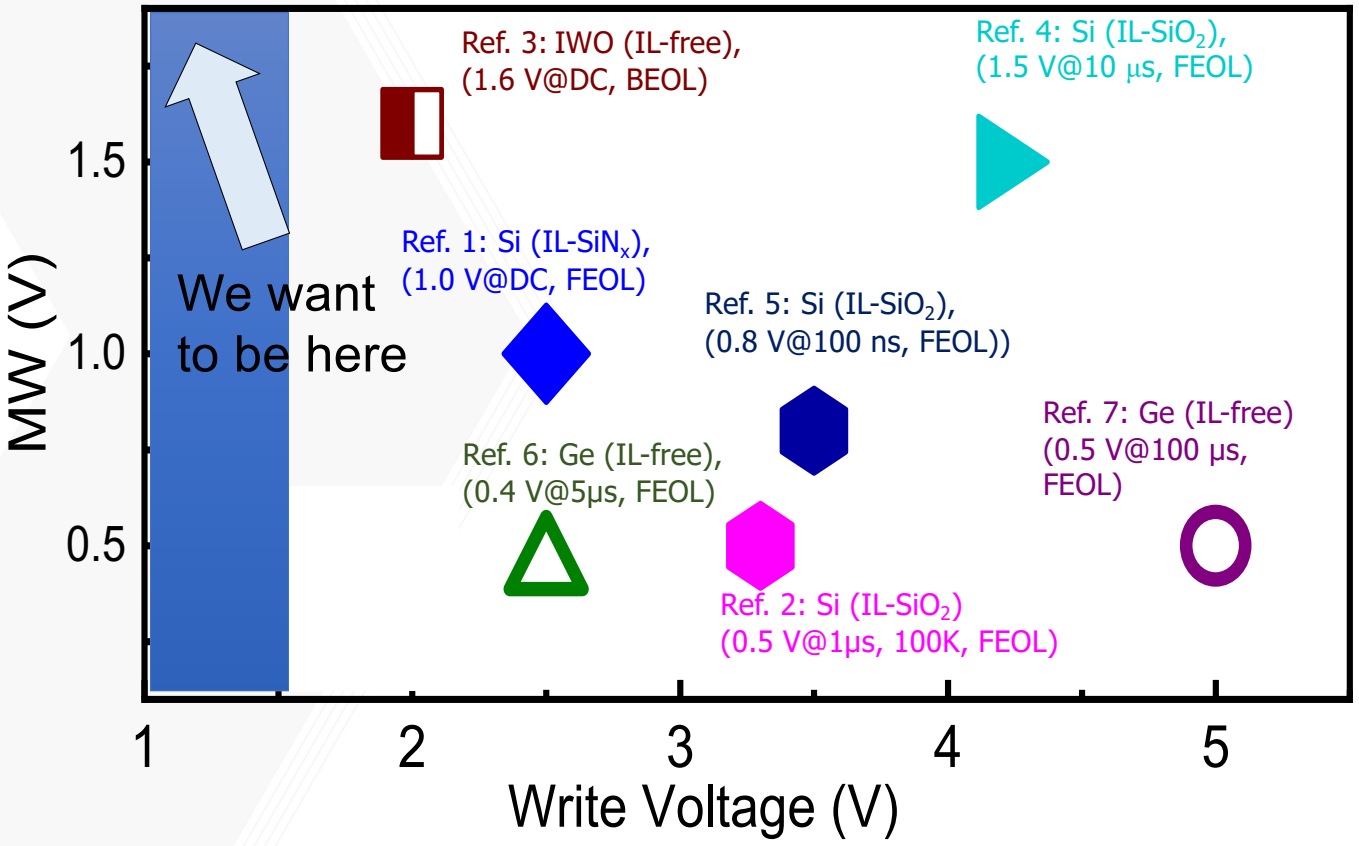
# Benchmarking Memory Window v. Write Voltage Tradeoff





[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

# Benchmarking Memory Window v. Write Voltage Tradeoff





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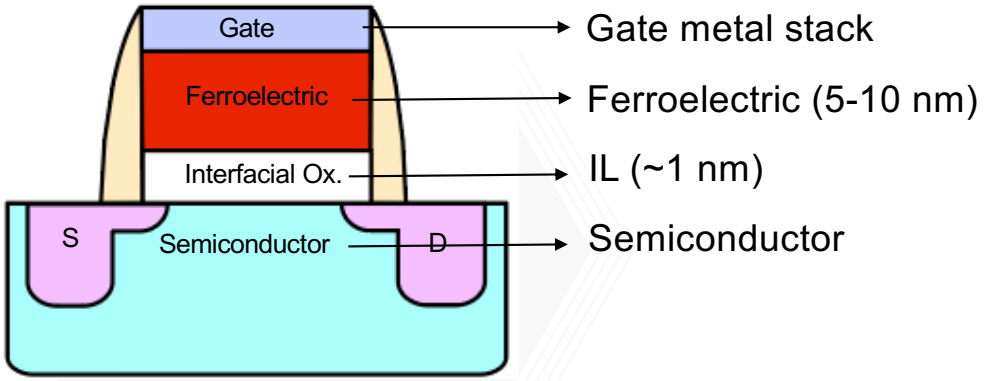
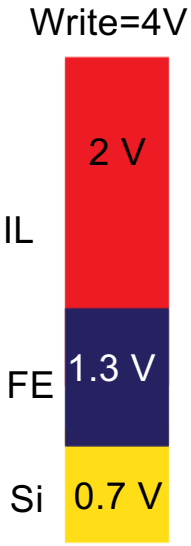
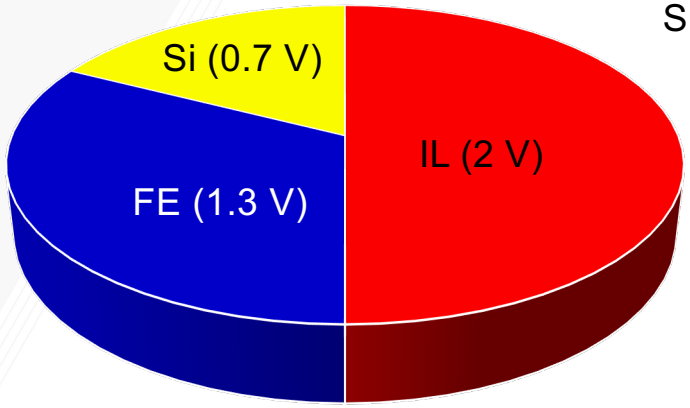
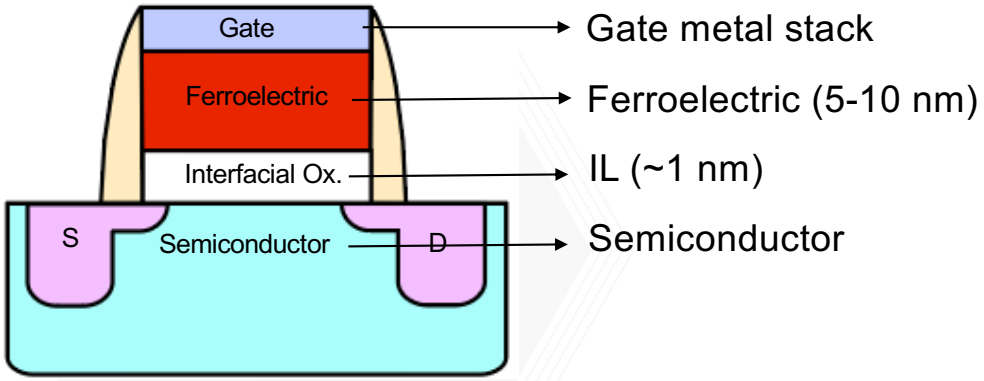
# Write voltage vs. memory window trade-off

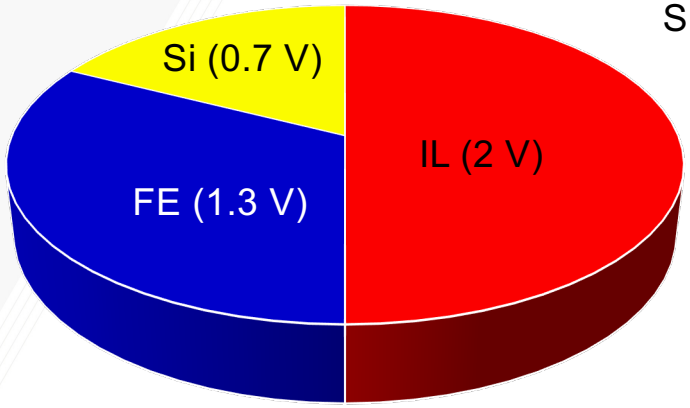


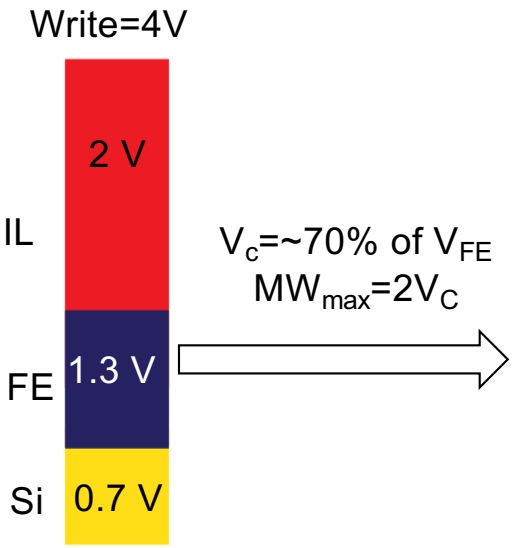



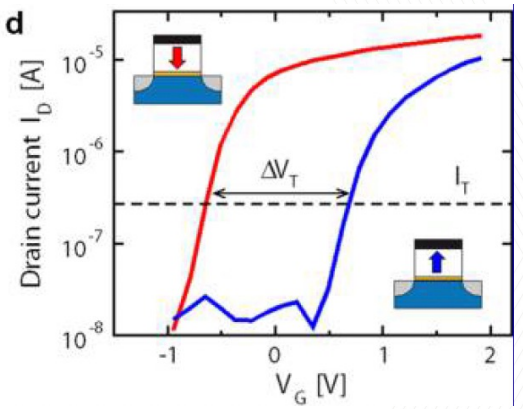



# Write voltage vs. memory window trade-off



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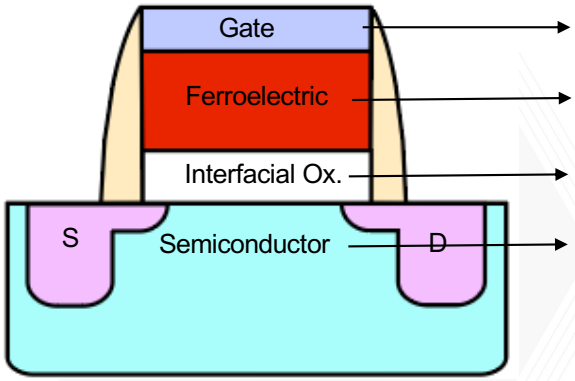
# Write voltage vs. memory window trade-off

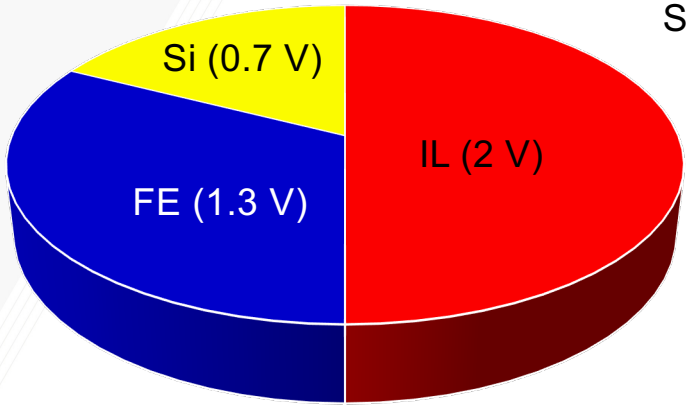


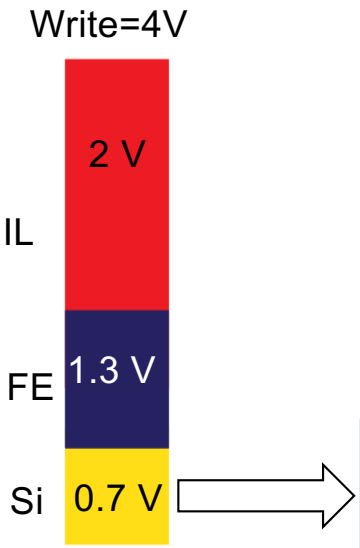

Gate metal stack

Ferroelectric (5-10 nm)

IL (~1 nm)

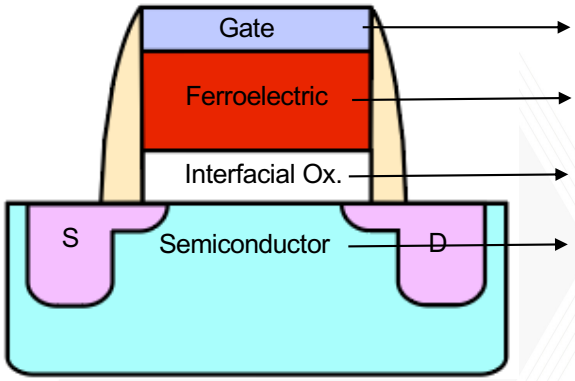
Semiconductor




Changing the band-gap of the semiconductor By changing the channel material from Si to SiGe or Ge.

# Write voltage vs. memory window trade-off

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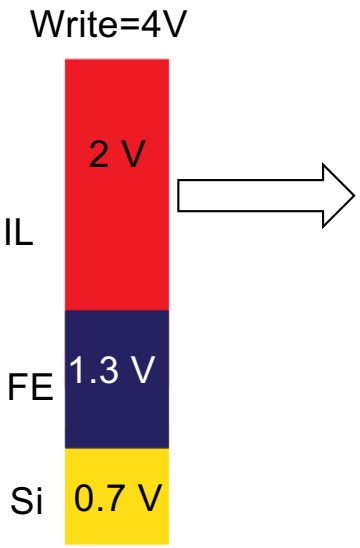
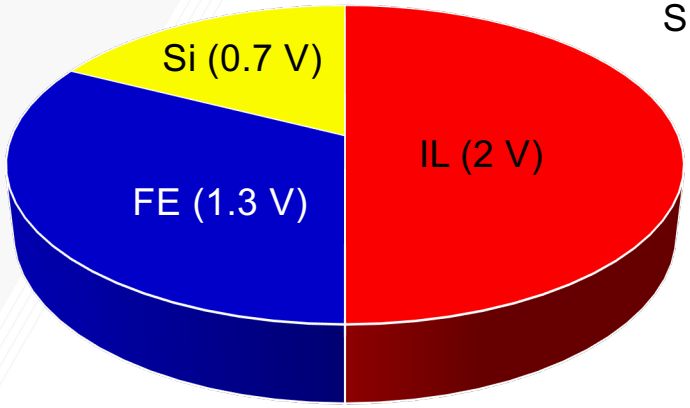
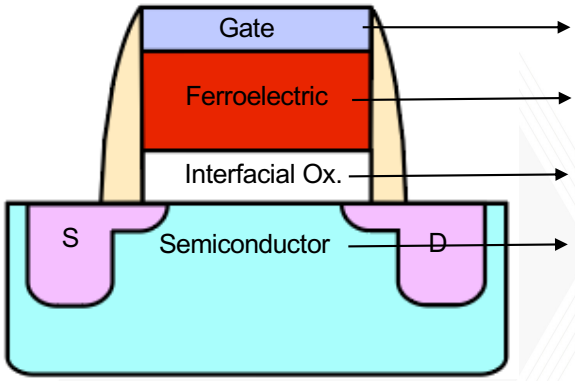



Reducing the thickness of the IL or increasing the K of the IL.

*Reliability degradation is a concern.*

# Write voltage vs. memory window trade-off

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IL (~1 nm)

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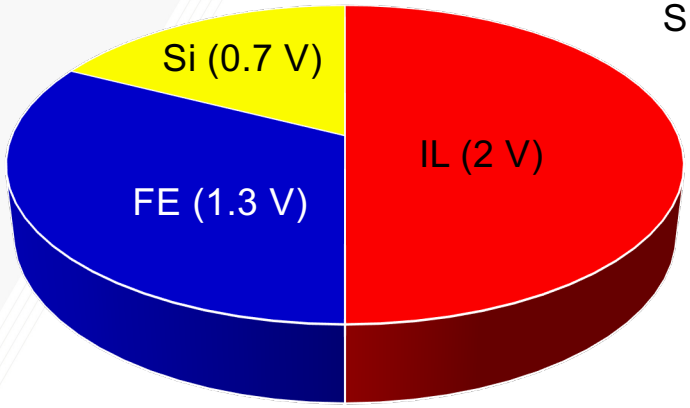


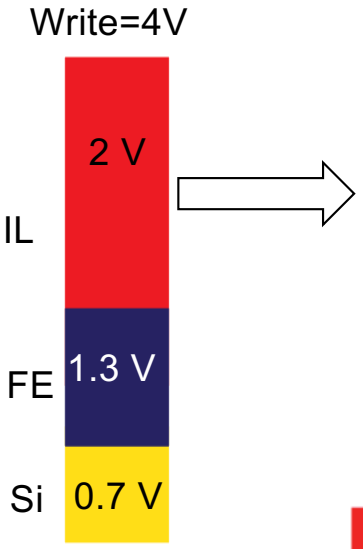


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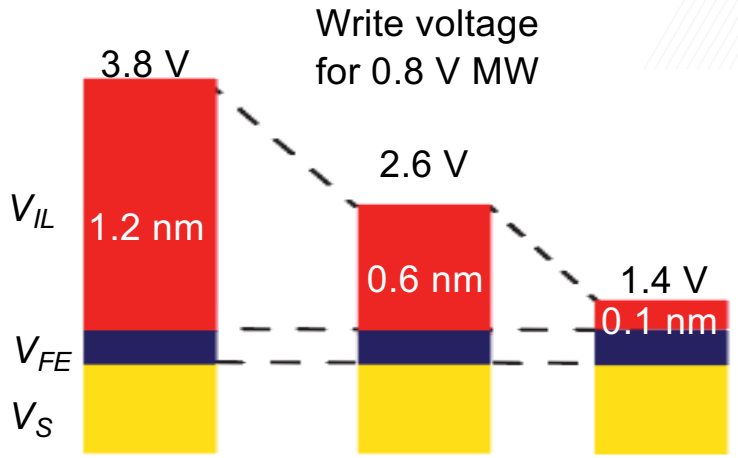
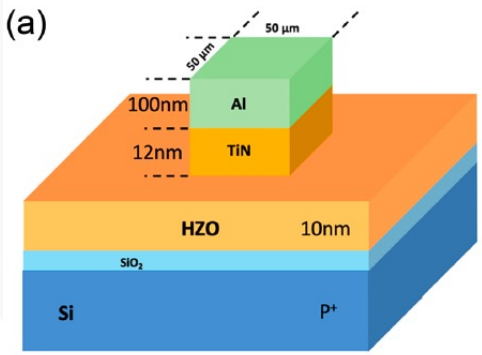
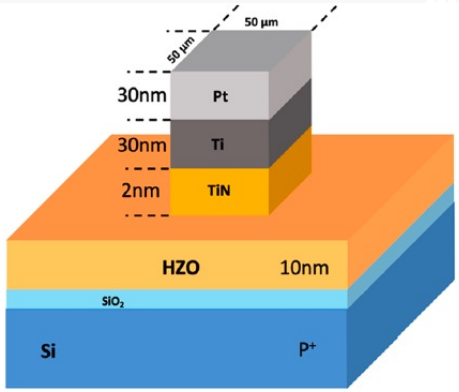


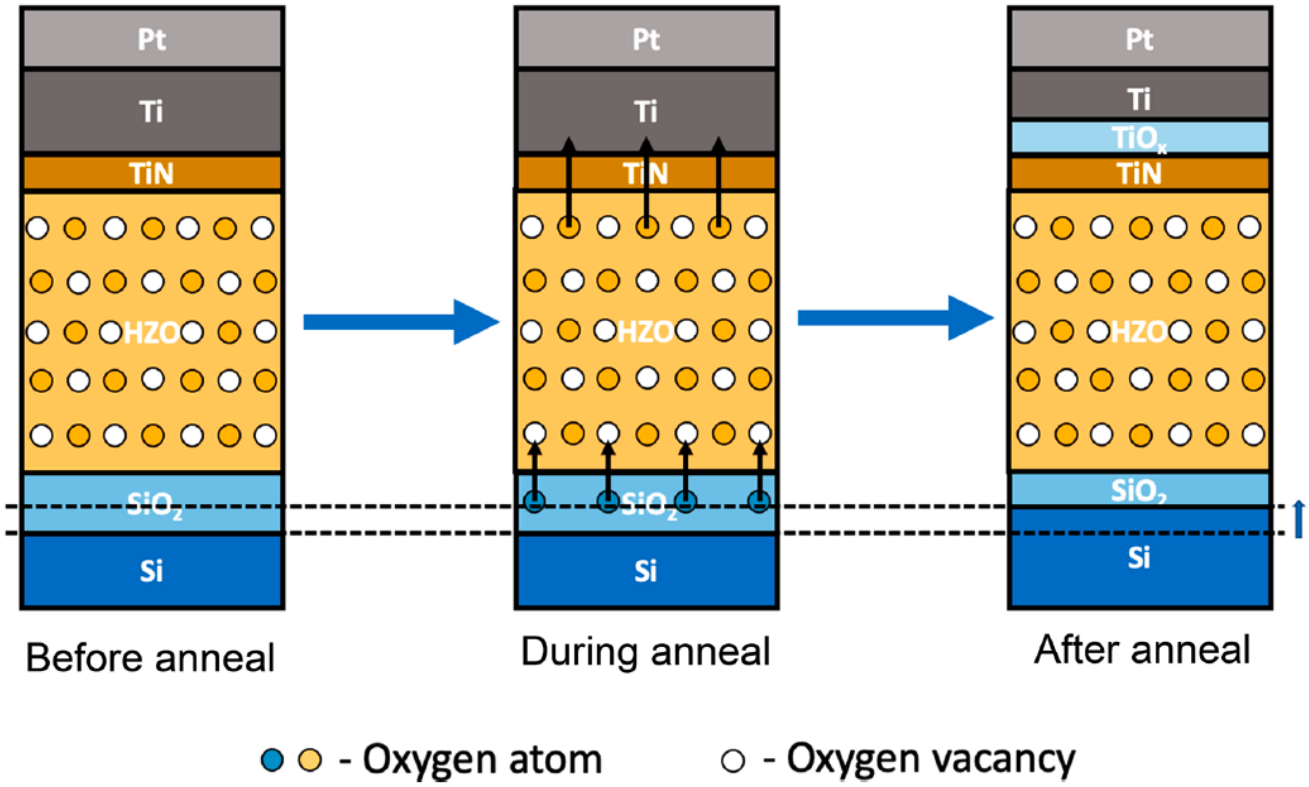
# Remote oxygen scavenging to reduce IL thickness




Non-Scavenging




Remote-Scavenging




Tasneem et al. "Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium–Zirconium Oxide-Based Metal–Oxide–Semiconductor Structures", ACS Appl. Mater. Interfaces 2022, 14, 43897–43906



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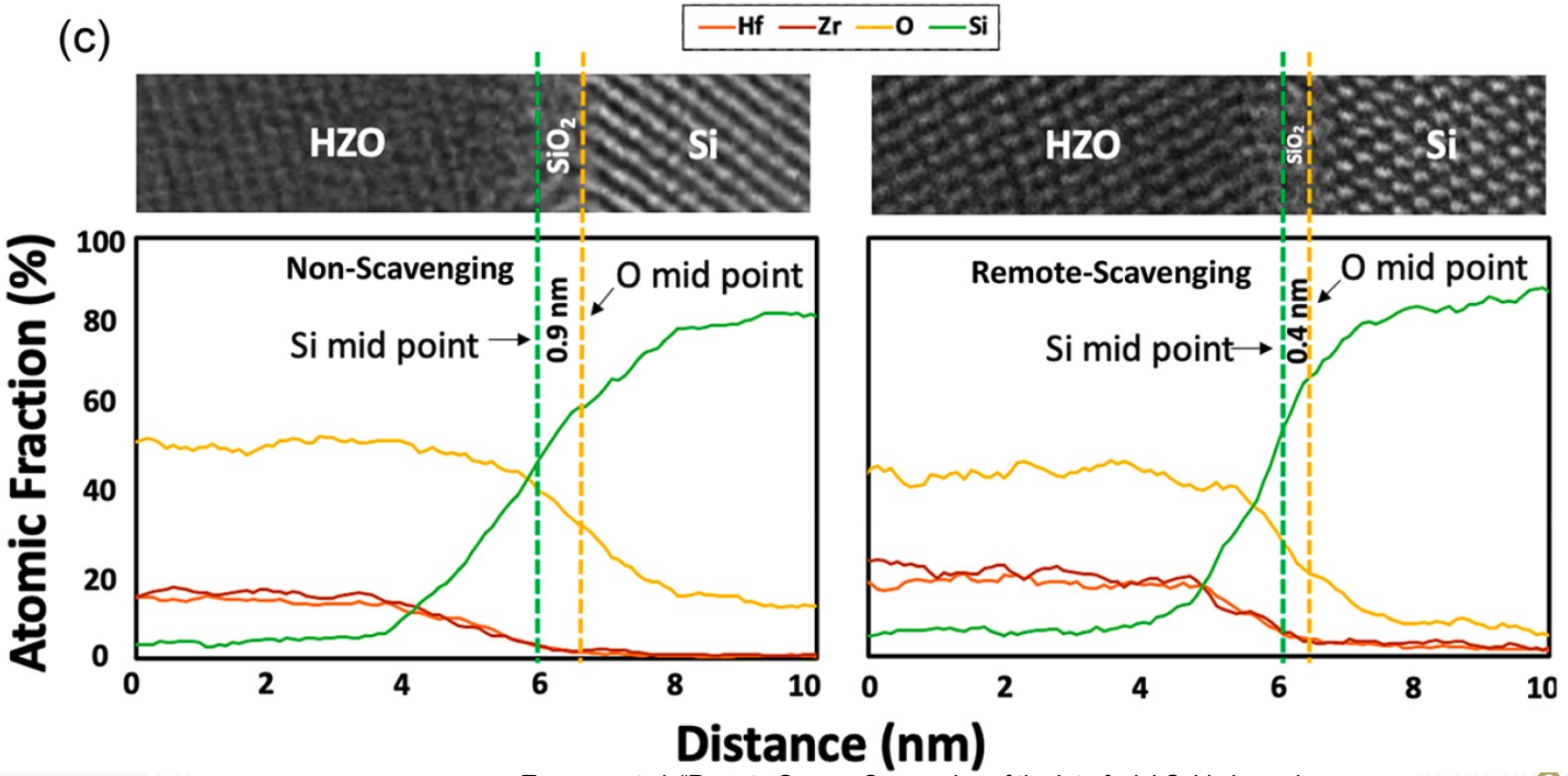
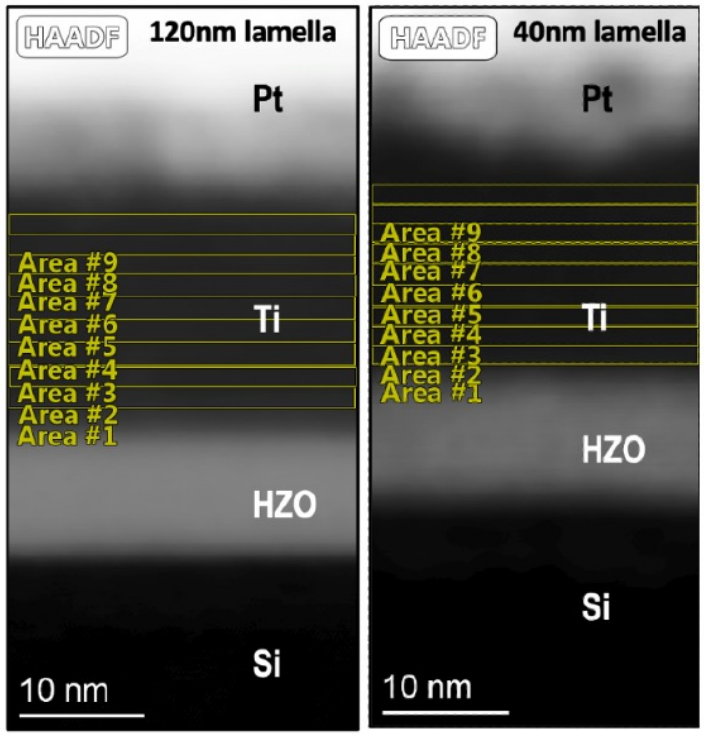
# Remote oxygen scavenging to reduce IL thickness



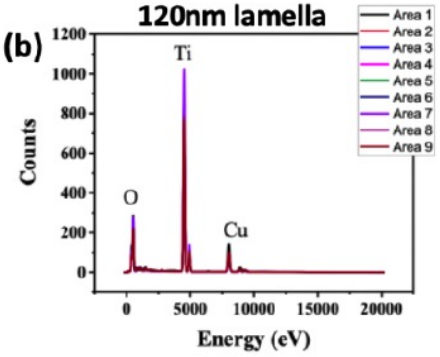

Tasneem et al. "Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium–Zirconium Oxide-Based Metal–Oxide–Semiconductor Structures", ACS Appl. Mater. Interfaces 2022, 14, 43897–43906

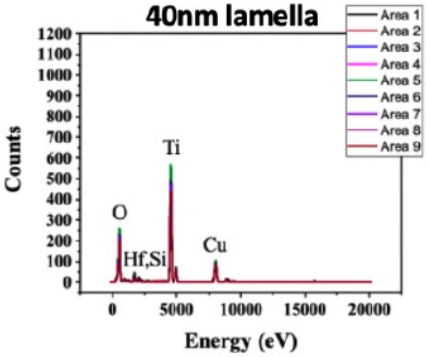
# Remote oxygen scavenging to reduce IL thickness

(a)




(b)




(c)

120nm lamella

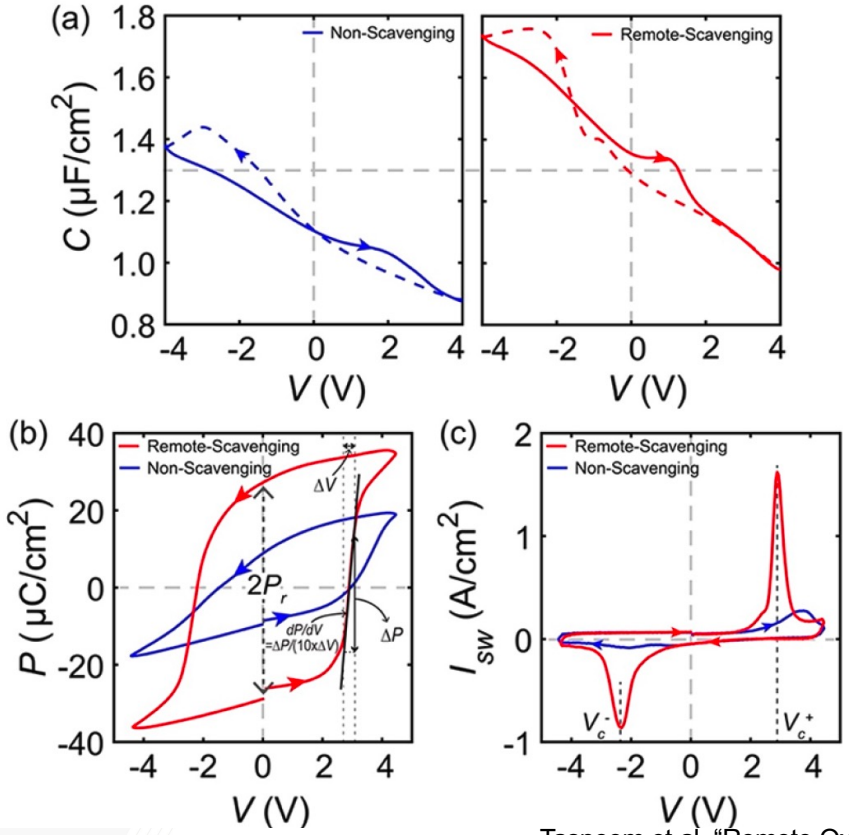
| | Ti | N | O |
|---|---|---|---|
| Area 1 | 48.89 | 8.80 | 42.31 |
| Area 2 | 52.61 | 4.89 | 42.50 |
| Area 3 | 52.33 | 4.56 | 43.11 |
| Area 4 | 52.43 | 5.29 | 42.49 |
| Area 5 | 53.03 | 1.05 | 41.79 |
| Area 6 | 54.00 | 3.52 | 42.48 |
| Area 7 | 55.71 | 2.57 | 41.72 |
| Area 8 | 55.69 | 2.20 | 42.11 |
| Area 9 | 54.98 | 2.87 | 42.15 |

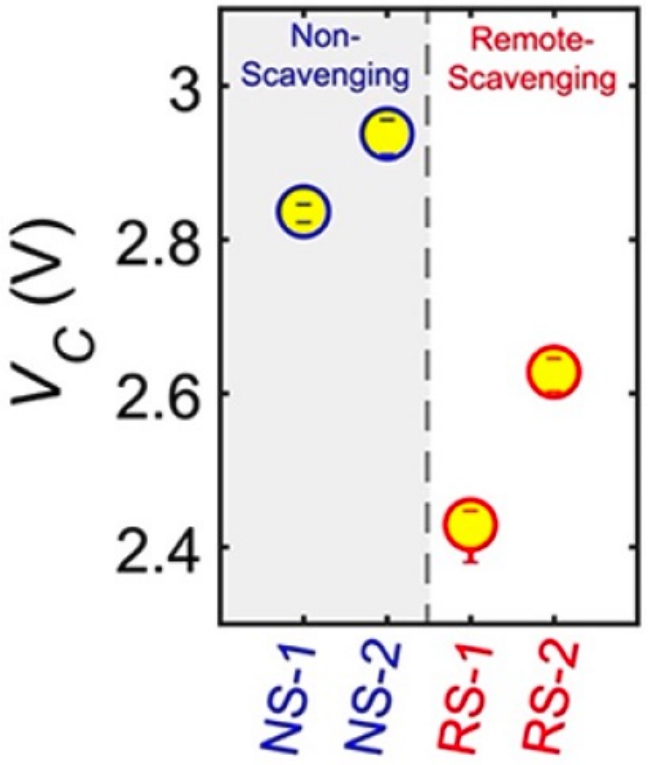
40nm lamella

| | Ti | N | O |
|---|---|---|---|
| Area 1 | 30.35 | 11.34 | 55.45 |
| Area 2 | 33.15 | 8.40 | 57.58 |
| Area 3 | 34.55 | 6.79 | 58.16 |
| Area 4 | 35.09 | 5.29 | 58.63 |
| Area 5 | 35.54 | 5.98 | 57.53 |
| Area 6 | 35.61 | 5.73 | 58.08 |
| Area 7 | 35.96 | 5.50 | 57.81 |
| Area 8 | 37.06 | 4.98 | 57.38 |
| Area 9 | 36.07 | 4.40 | 58.79 |

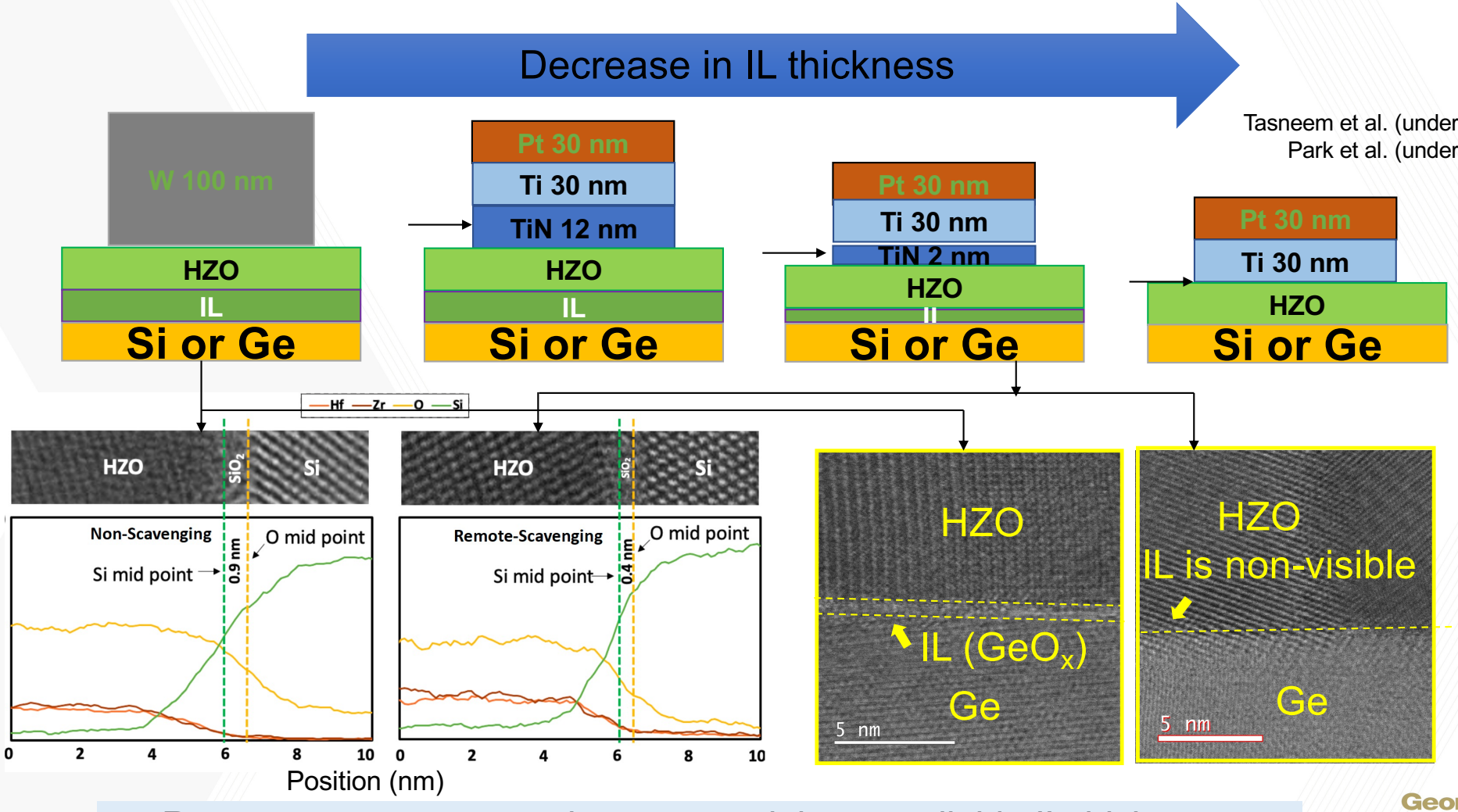
Tasneem et al. “Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium−Zirconium Oxide-Based Metal−Oxide−Semiconductor Structures”, ACS Appl. Mater. Interfaces 2022, 14, 43897–43906

# Remote oxygen scavenging to reduce IL thickness




Tasneem et al. "Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium–Zirconium Oxide-Based Metal–Oxide–Semiconductor Structures", ACS Appl. Mater. Interfaces 2022, 14, 43897–43906




Tasneem et al. (under review)
Park et al. (under review)

Remote oxygen scavenging can result in controllable IL thickness.



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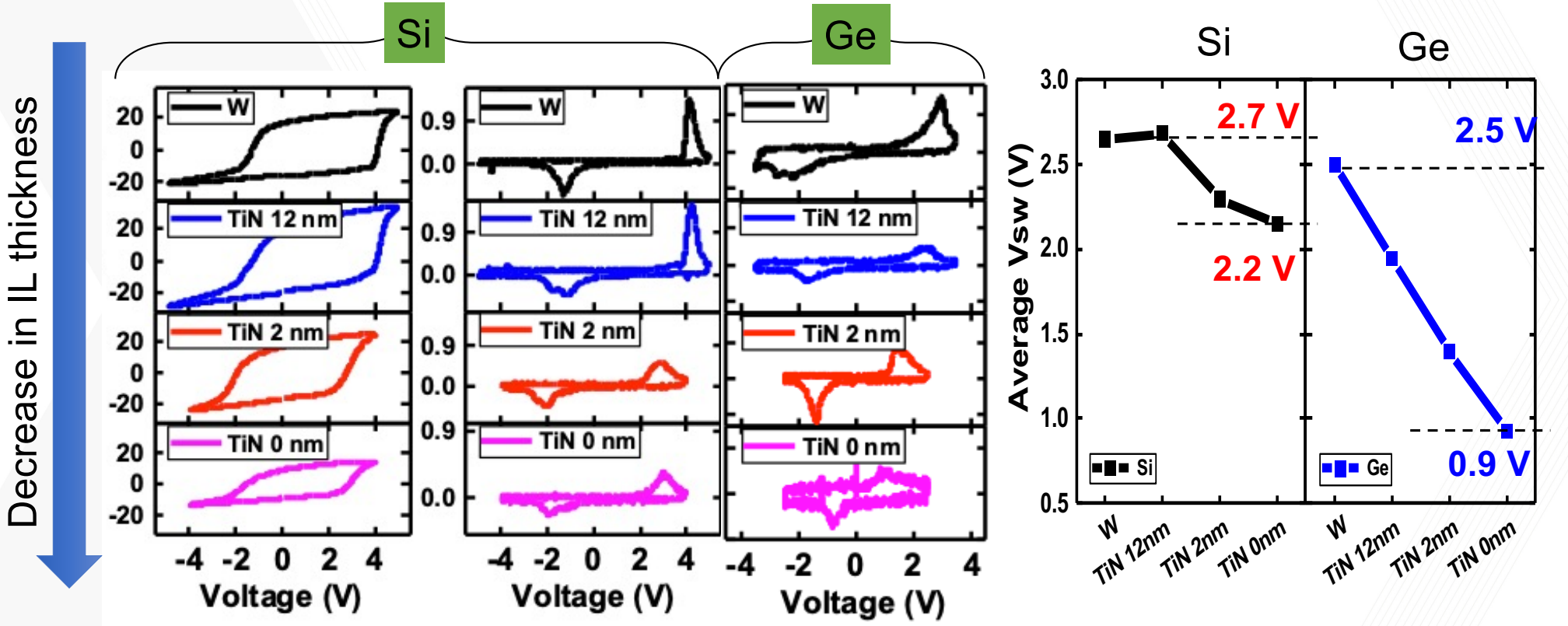
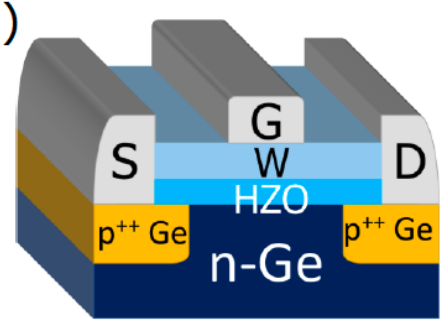
# The effect of the IL thickness on Vc



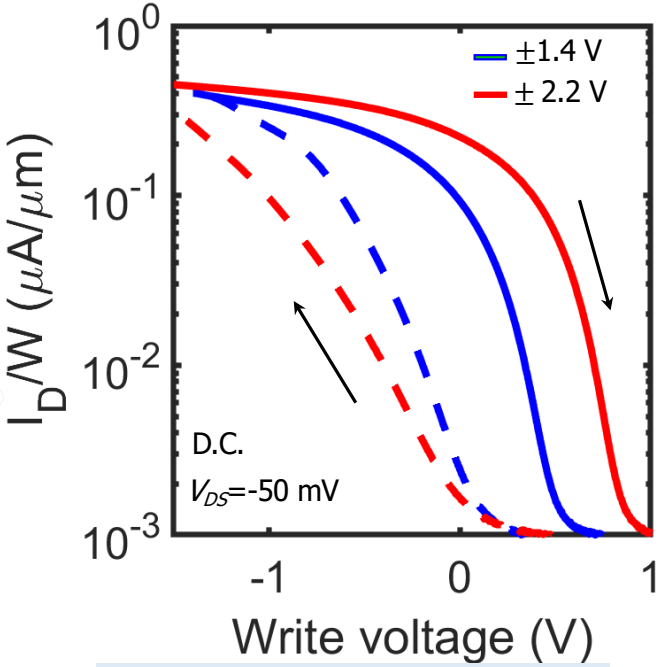

Dramatic reduction in coercive voltage is observed in Ge platform with the change of the gate metal stack.

# Ge-channel FEFETs with record-low write voltages

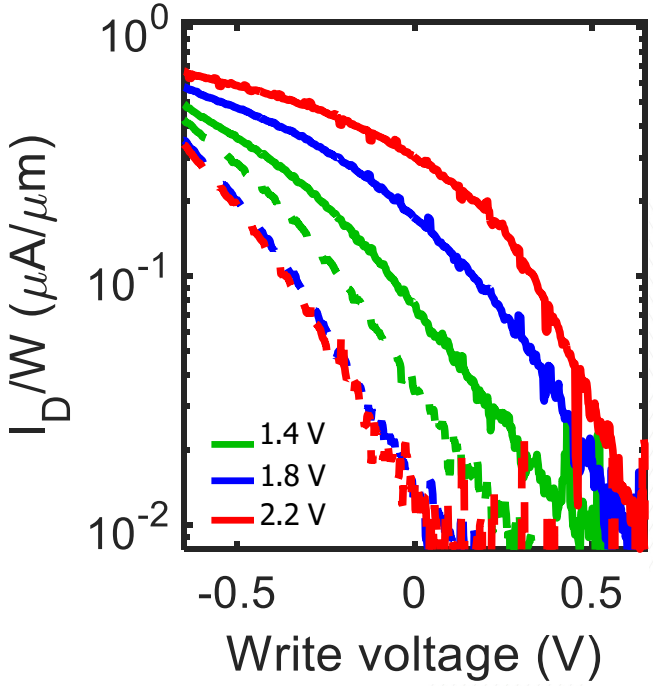
(a)




- S/D Implantation
- Screening oxide etch
- ALD of gate stack
- 500 °C, 30 sec anneal
- HZO Dry etch
- Standard ILD
- Al Metallization
- FGA (400 °C, 30 min)




0.55 V MW at 1.4 V
1.2 V MW at 2.2 V




0.5 V MW at 1.8 V
(10 µs)



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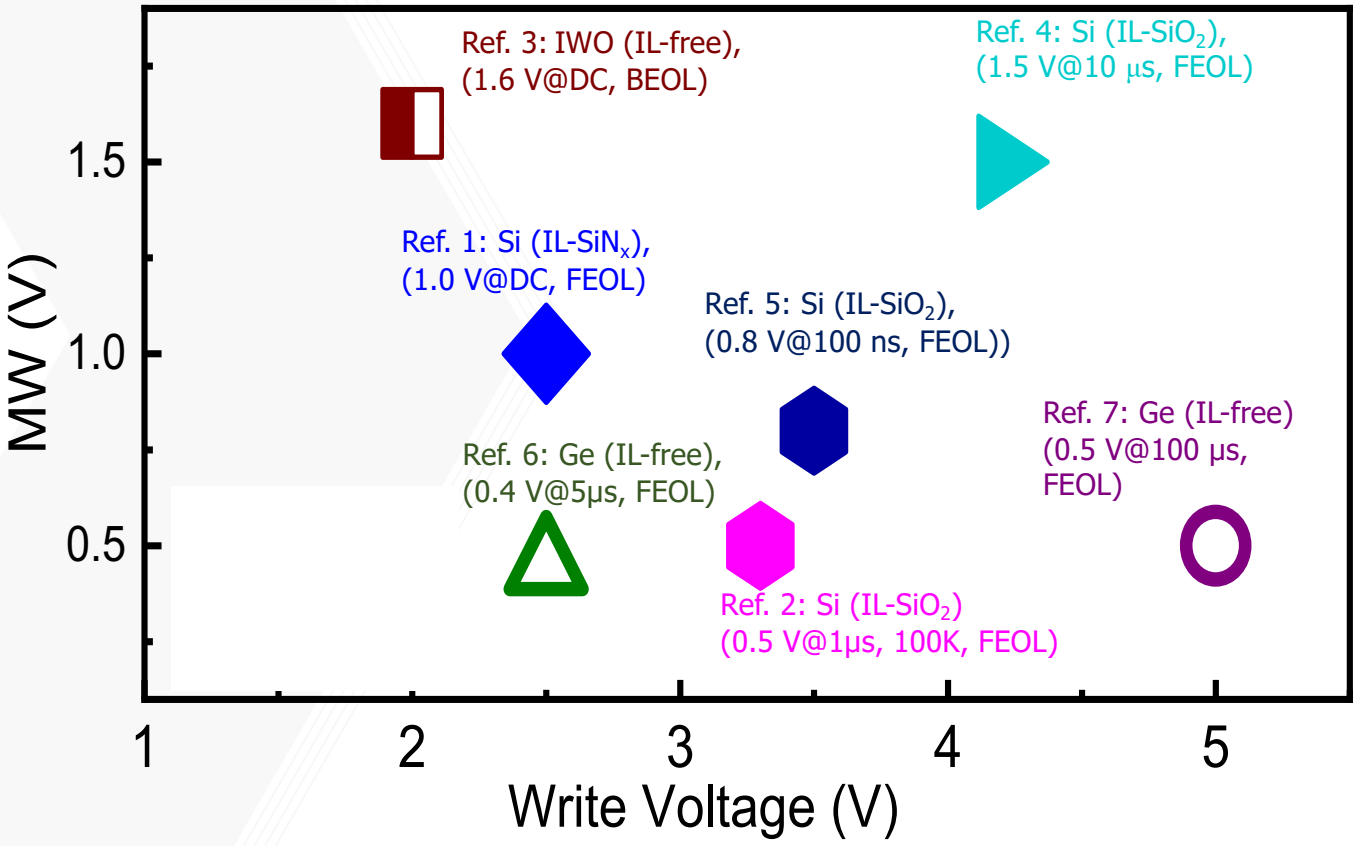
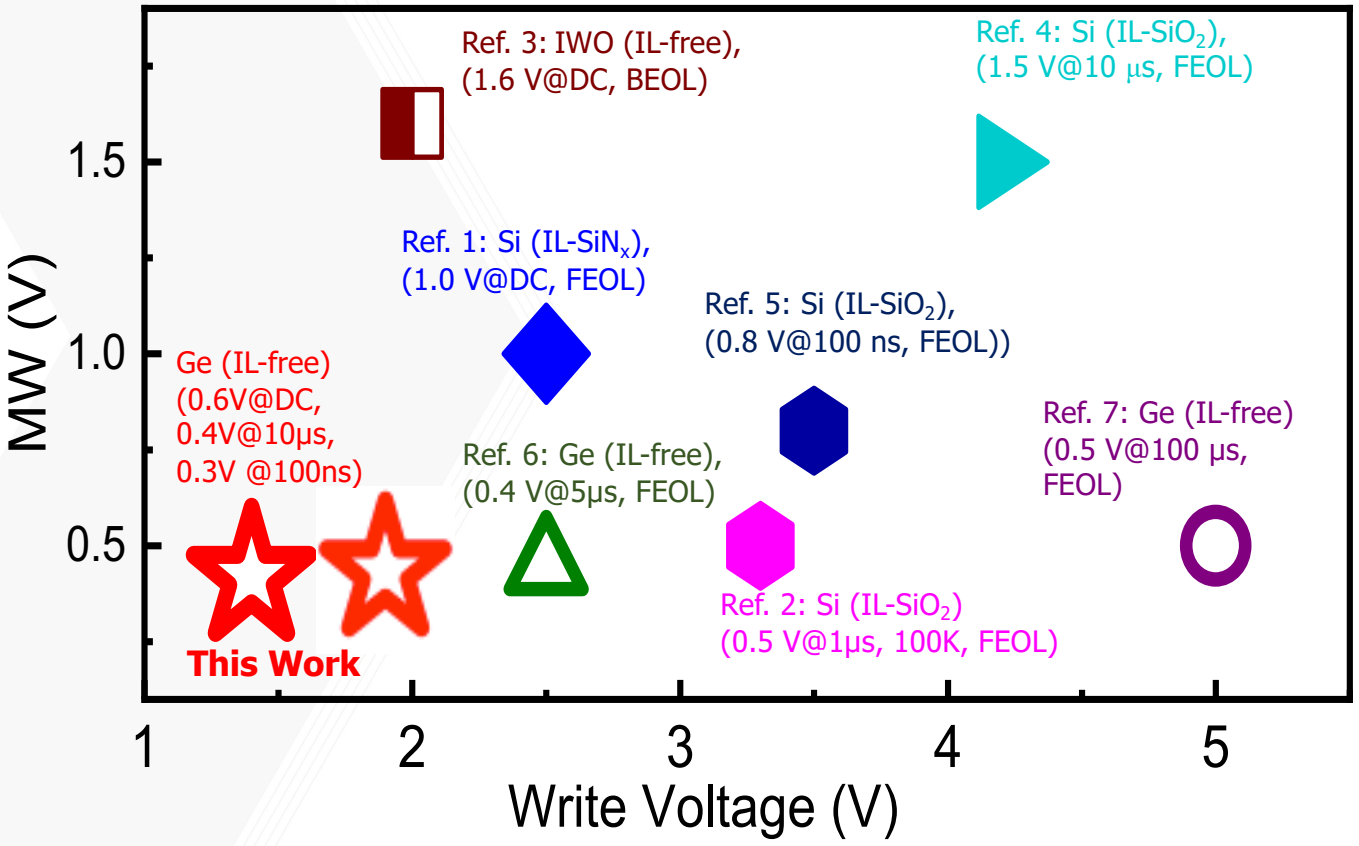
# Benchmarking Memory Window v. Write Voltage Tradeoff





[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

# Benchmarking Memory Window v. Write Voltage Tradeoff





[1] Tan *et al., IEEE EDL,* 42, 994, (2021).
[2] Tan *et al., 2020 IEEE Symposium on VLSI Technology* (2020).
[3] Dutta *et al., IEEE EDL*, 43, 382 (2022).
[4] Dünkel *et al., IEDM* (2017).
[5] Nguyen et al., *IEEE EDL*, 42, 1295, (2021).
[6] Liu *et al., IEEE EDL*, 40, 1419, (2019).
[7] Zacharaki et al., *ACS Appl. Electron. Mater.* , 4, (2022).

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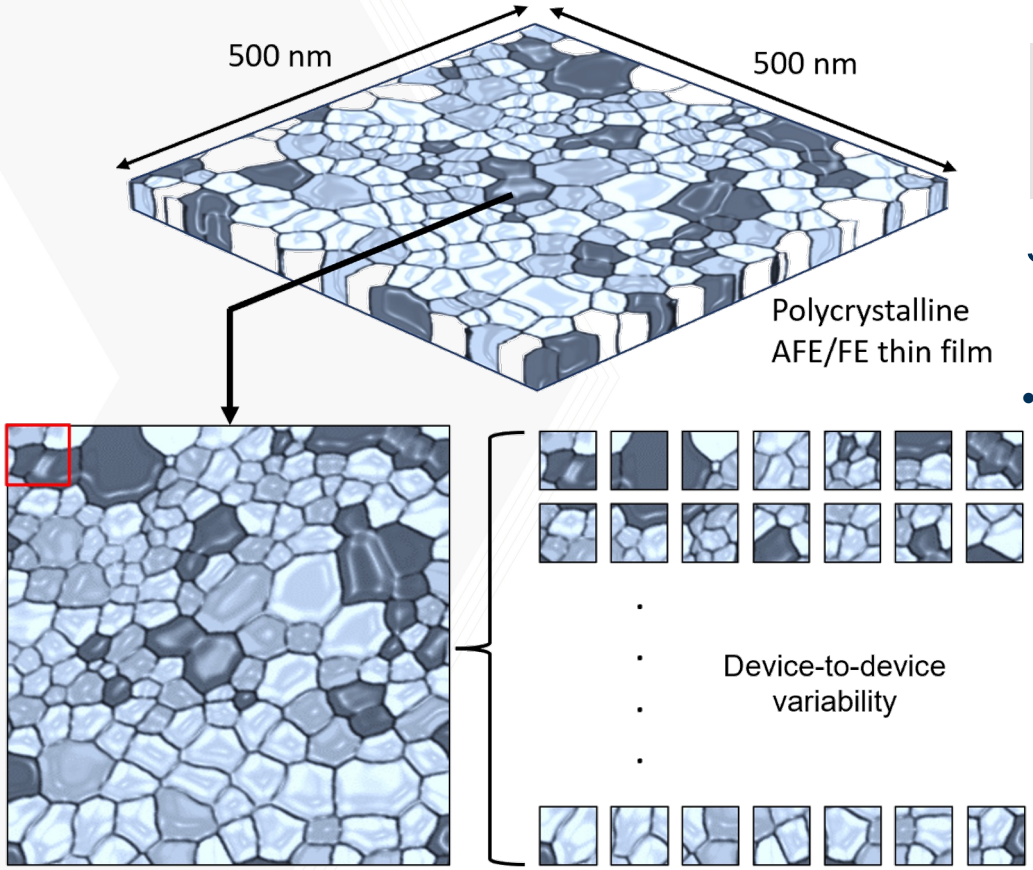
# Microstructure in FEFETs




1. Phase (o-, m-, t-)

3. Sub-grain features (domain walls, interphase boundaries)

2. Grain size & orientation

Device-to-device variability

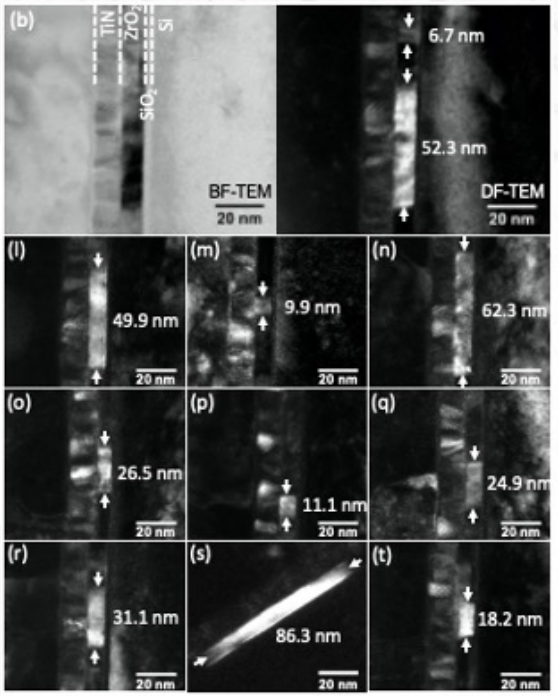
- Applied field causes changes in microstructure
  - Enables multi-level NVM
  - Poses challenges for (VLSI)

4. Irreversible change of grain structure electric field cycling

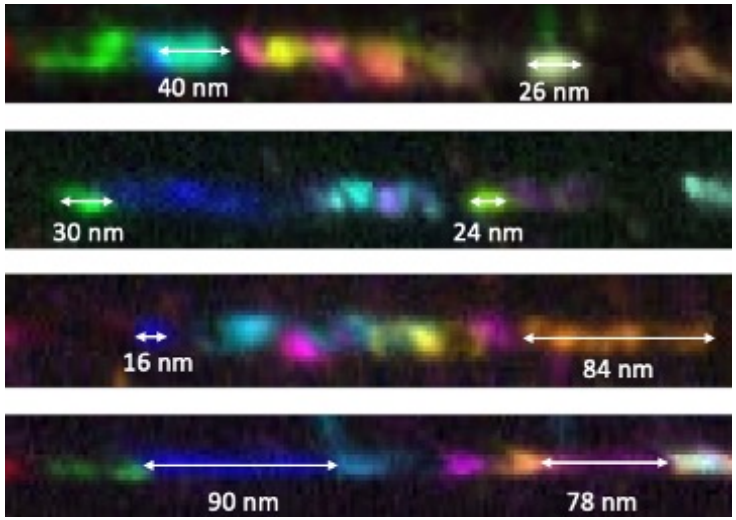
Cycle-to-cycle variability

# Quantification of microstructure

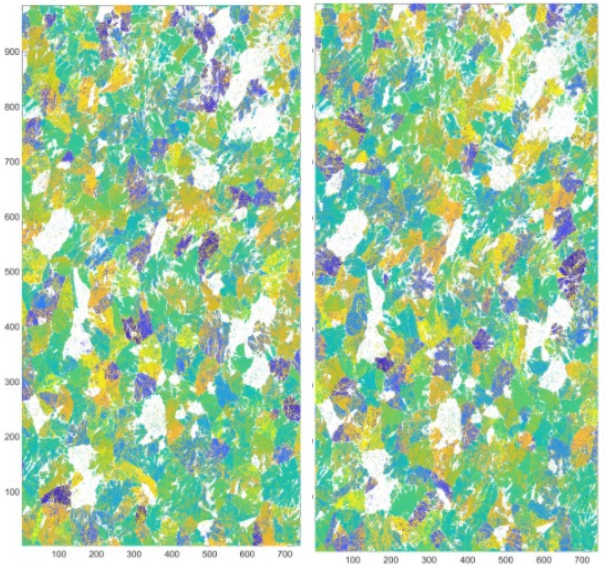
Dark field TEM




Nano-Beam Electron Diffraction (NBED)

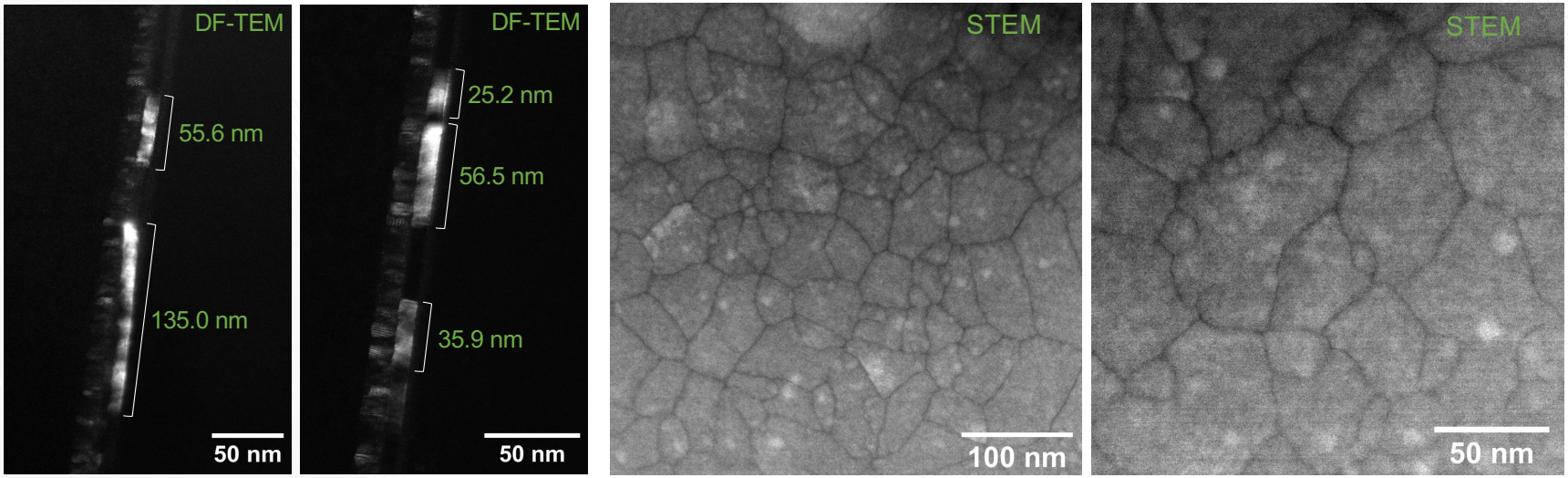


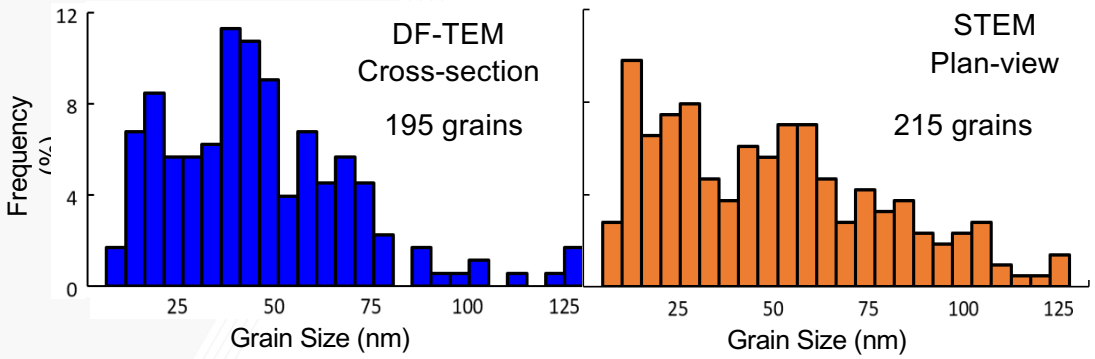

Transmission Kikuchi Diffraction (TKD)

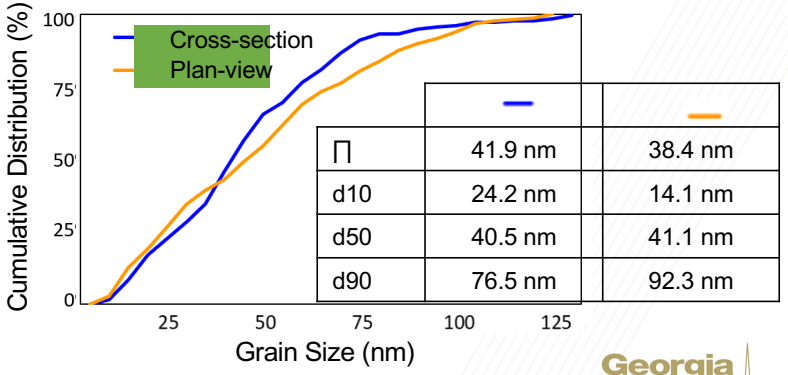


Lombardo, S. F., et al. "Local epitaxial-like templating effects and grain size distribution in atomic layer deposited Hf0. 5Zr0. 5O2 thin film ferroelectric capacitors." *Applied Physics Letters* 119.9 (2021): 092901.

# Quantification of microstructure

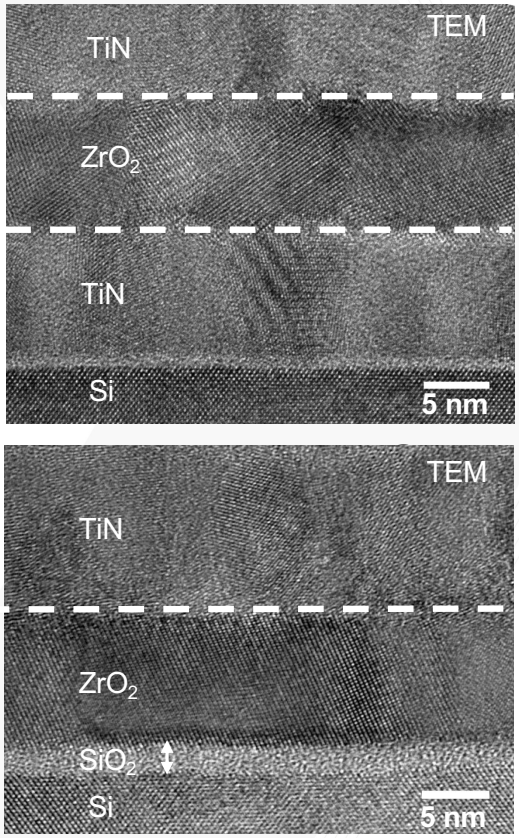


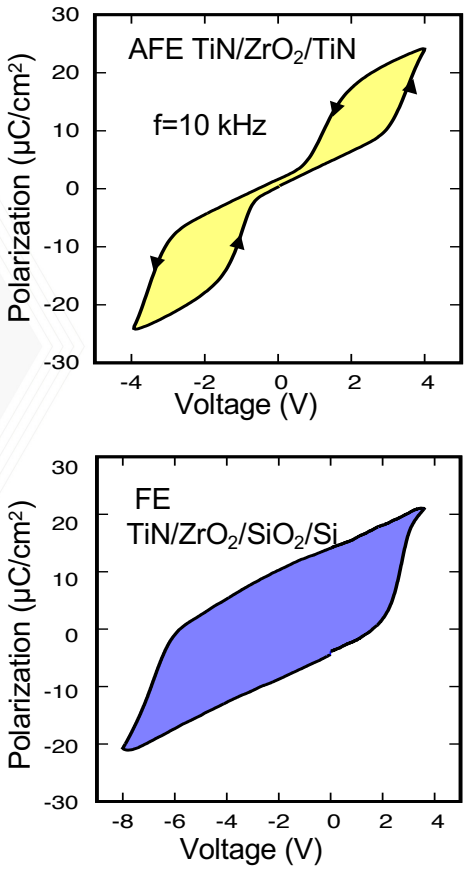



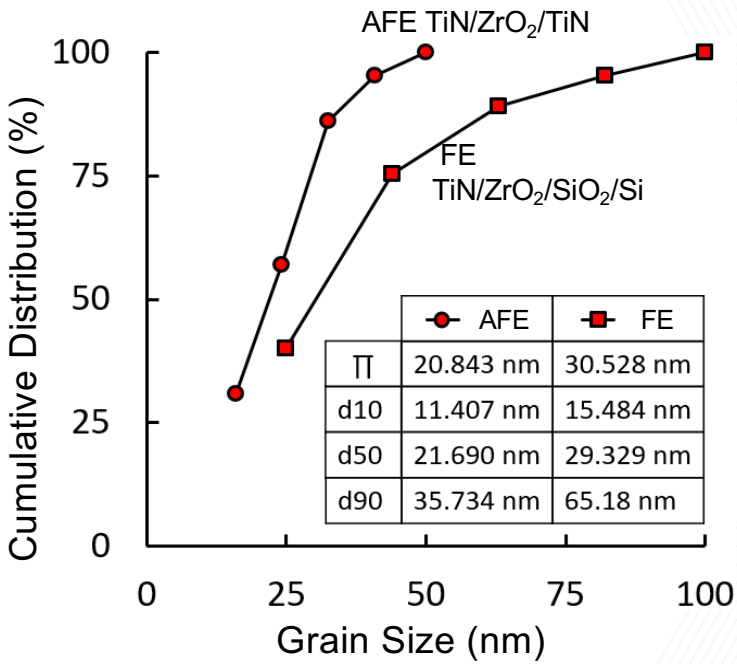




| | | |
|---|---|---|
| | | |
| ∏ | 41.9 nm | 38.4 nm |
| d10 | 24.2 nm | 14.1 nm |
| d50 | 40.5 nm | 41.1 nm |
| d90 | 76.5 nm | 92.3 nm |

# Microstructural origin of AFE and FE in $ZrO_2$




Smaller grain size favored by Tetragonal phase over FE Orthorhombic phase

Chae* & Lombardo* et al. *ACS Adv. Mat. & Int.*, (2022).

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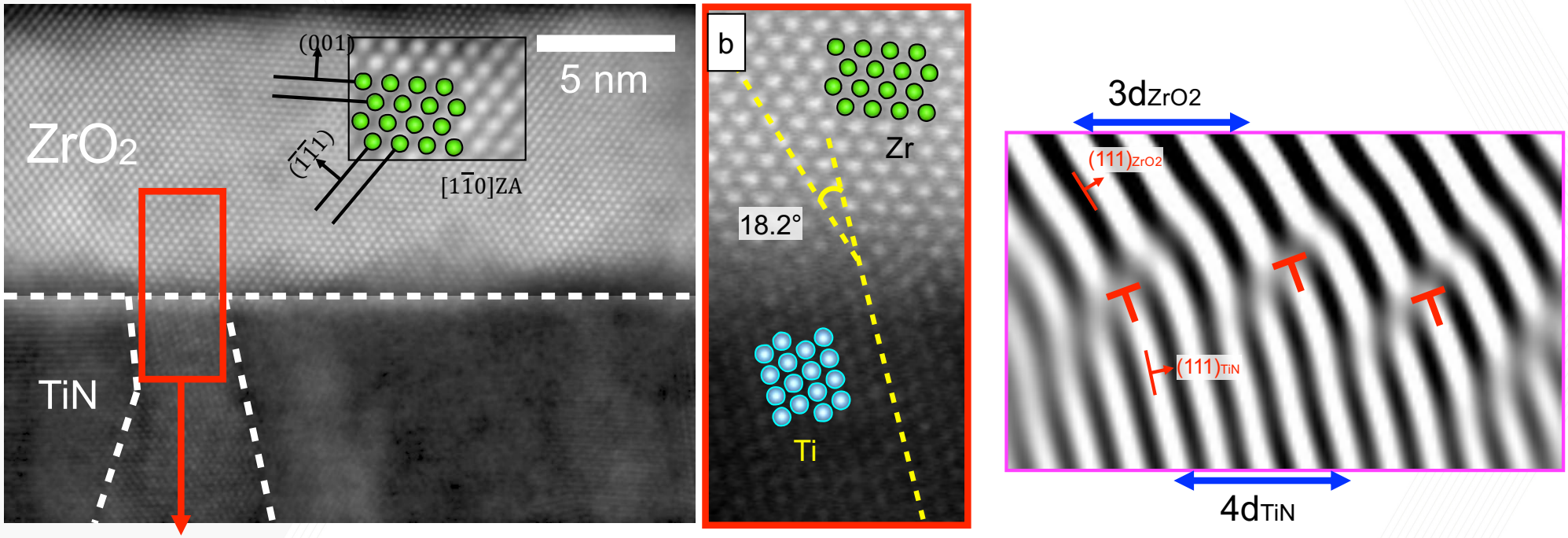
# Epitaxial-like templating: Near coincidence site epitaxy




Orientations in TiN and $ZrO_2$ are often correlated.

Chae* & Lombardo* et al. *ACS Adv. Mat. & Int.*, (2022).

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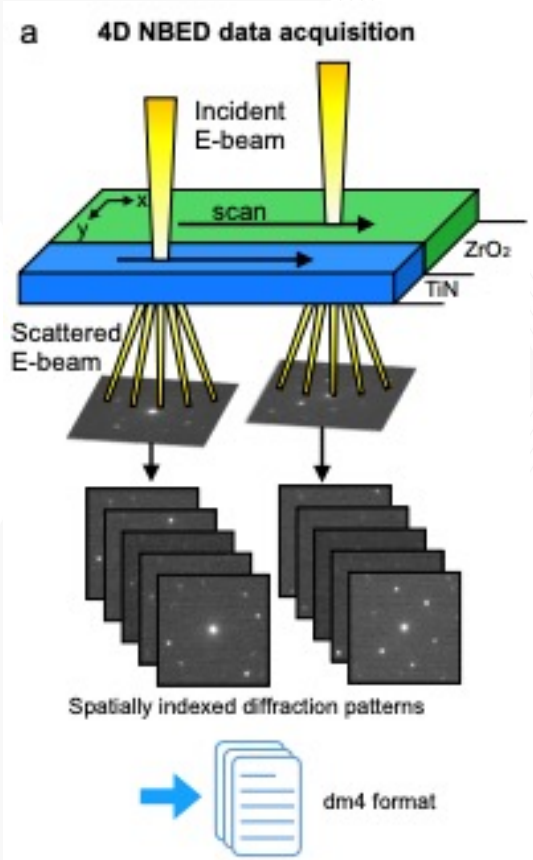
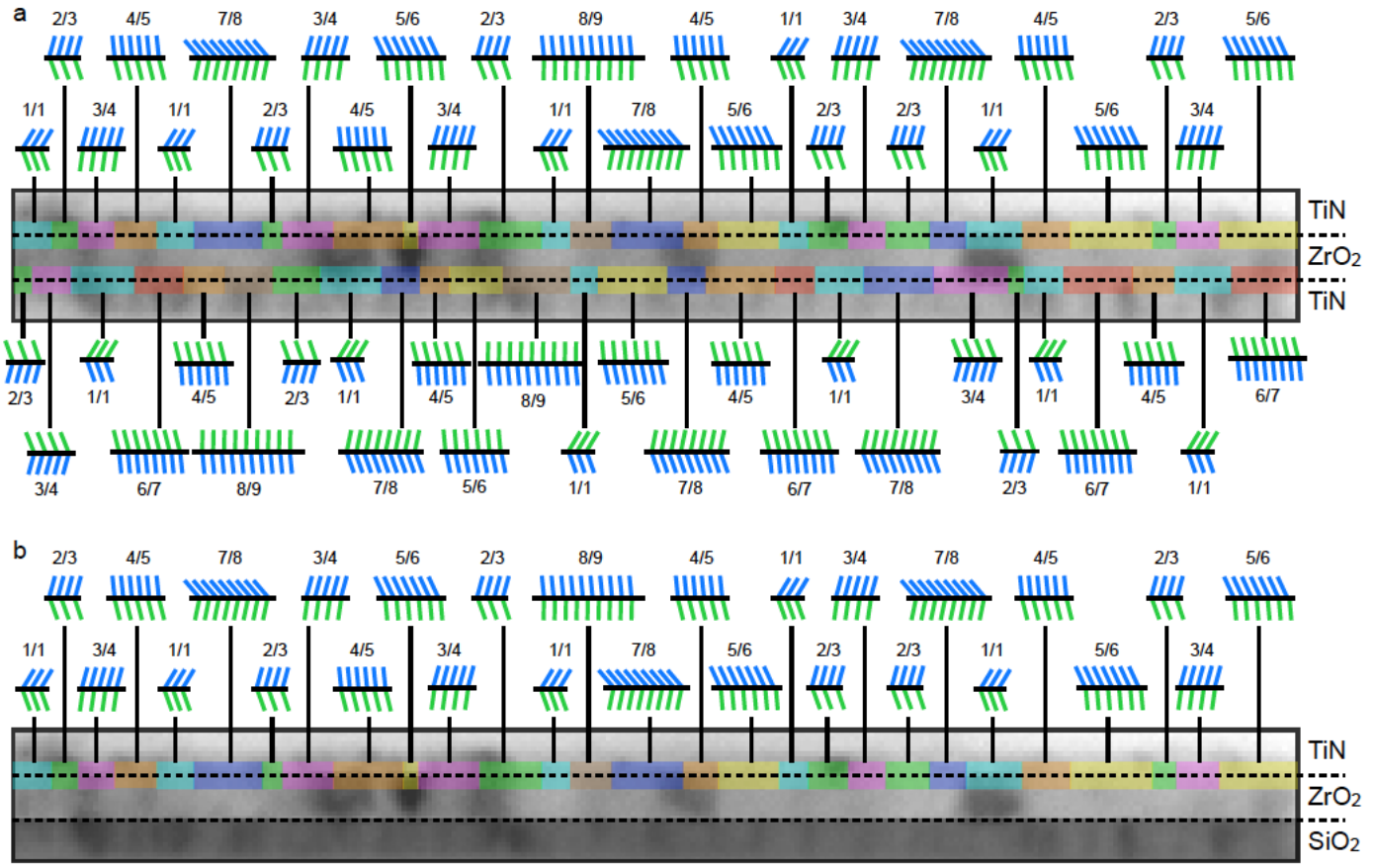
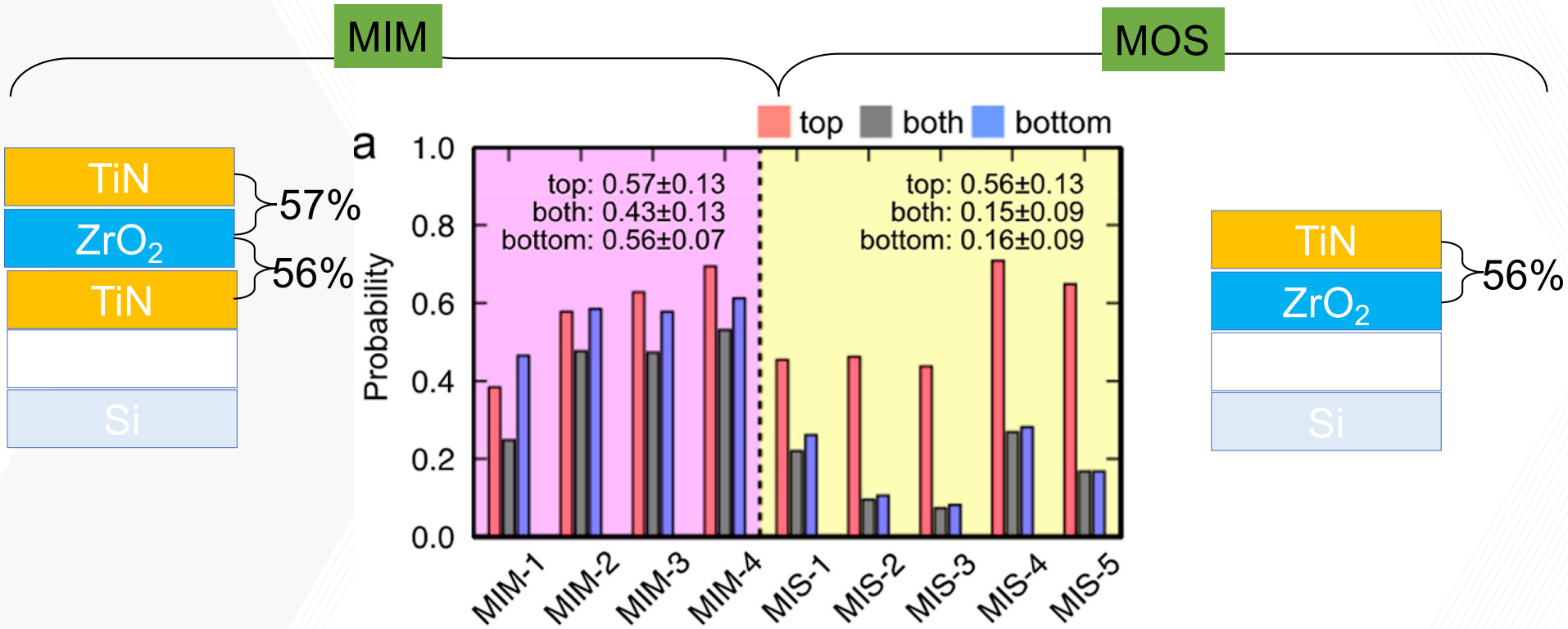
# Epitaxial-like templating: Near coincidence site epitaxy




Chae, Lombardo et al. (under review)

# Statistical Epitaxy Analysis via Automated NBED




Chae* & Lombardo* et al. *ACS Adv. Mat. & Int.*, (2022).

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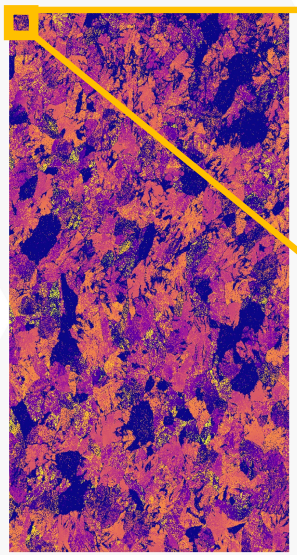
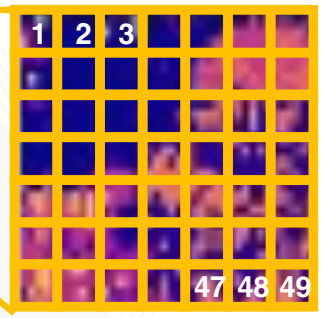
# Machine Learning Assisted Predictive TCAD Modeling (from Metrology to Device Metrics)

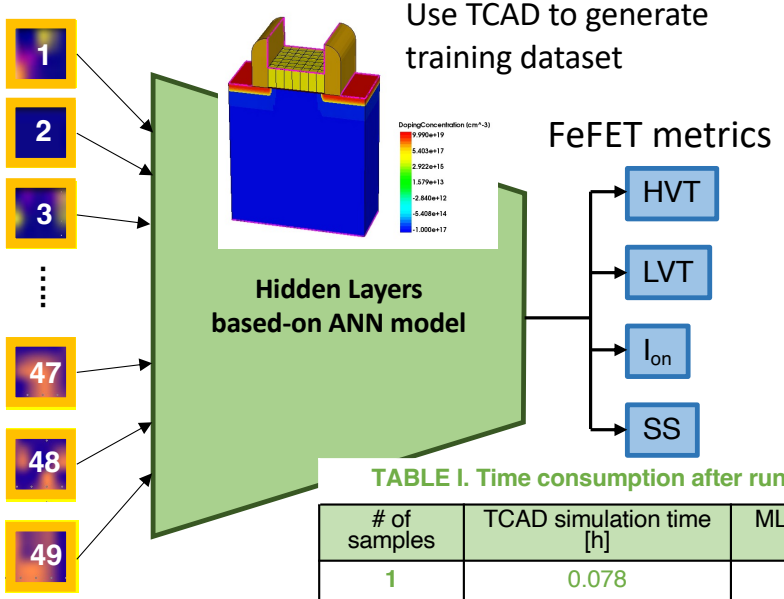


Ferro polarization map (from TKD data from SEM/TEM)




7×7 image

Total 14700 samples
Used 4000 samples
(not randomly)




1×49 array

Use TCAD to generate training dataset

FeFET metrics

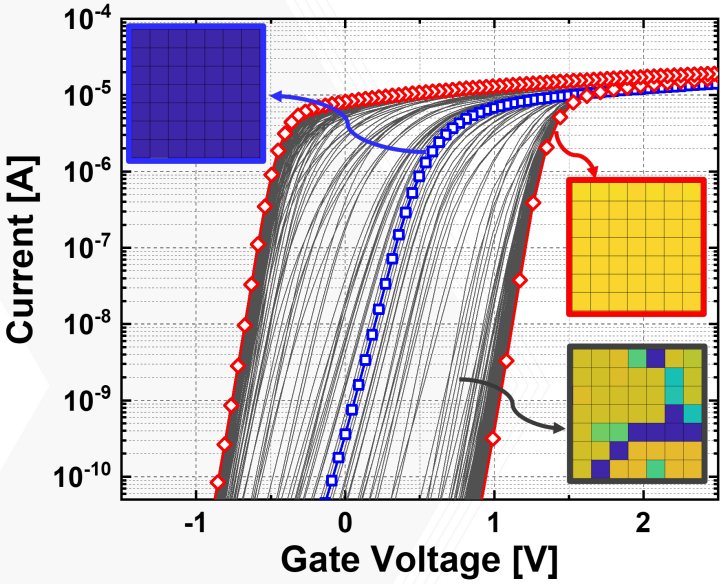
TABLE I. Time consumption after running test samples

| # of samples | TCAD simulation time [h] | ML-based inference time [h] |
|---|---|---|
| 1 | 0.078 | 5e-8 |
| 500 | 39 | 2.5e-5 |
| 1,000 | 78 | 5.3e-5 |
| 2,000 | 156 | 1.07e-4 |
| 10,000 | 780 | 5.3e-4 |
| 14,700 | 1146.6 (=48 days) | 7.79e-4 (=2.8 secs) |

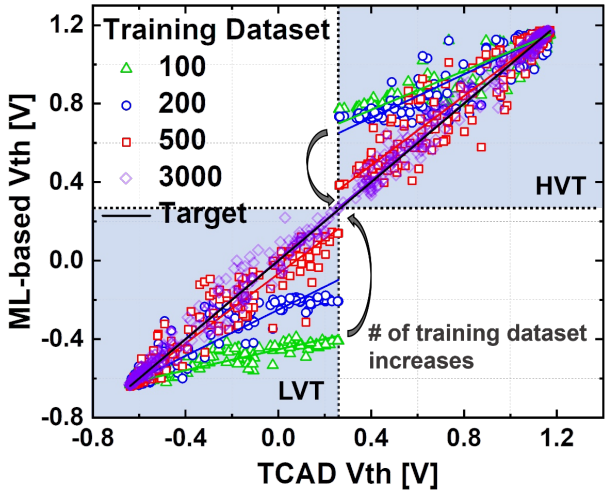
Significant speed up (ML vs. TCAD)

G. Choe, et al, VLSI 2022

# ML assisted Device Variation Modeling




G. Choe, P. V. Ravindran, A. Lu, J. Hur, M. Lederer, A. Reck, S. Lombardo, N. Afroze, J. Kacher, A. I. Khan, S. Yu, "Machine learning assisted statistical variation analysis of ferroelectric transistors: from experimental metrology to predictive modeling," IEEE Symposium on VLSI Technology and Circuits (VLSI) 2022




TCAD results vs. ML-based results of HVT/LVT. Symbols represent the data points and lines are linearly fitted trend lines.

**TABLE II. Average, 3-sigma and percentage of prediction error**

| | TCAD | ML-based prediction | | |
|---|---|---|---|---|
| | μ | μ | 3σ | Error |
| **HVT [V]** | 1.05 | 1.05 | 0.08 | **1.2%** |
| **LVT [V]** | –0.53 | –0.53 | 0.07 | **2.0%** |
| **$I_{on}$ [μA]** | 6.68 | 6.68 | 1.01 | **2.1%** |
| **SS [mV/dec]** | 94.52 | 94.48 | 9.0 | **1.6%** |



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# Our Team and Sponsors

## Our group at Georgia Tech

## Collaborators

Joshua Kacher, Georgia Tech
Andrew Kummel, UCSD
Shimeng Yu, Georgia Tech
Kyeongjae Cho, UTD,
Kisung Chae, UTD, UCSD
Nazanin Bassiri-Gharb, Georgia Tech
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