Ferroelectric Memories

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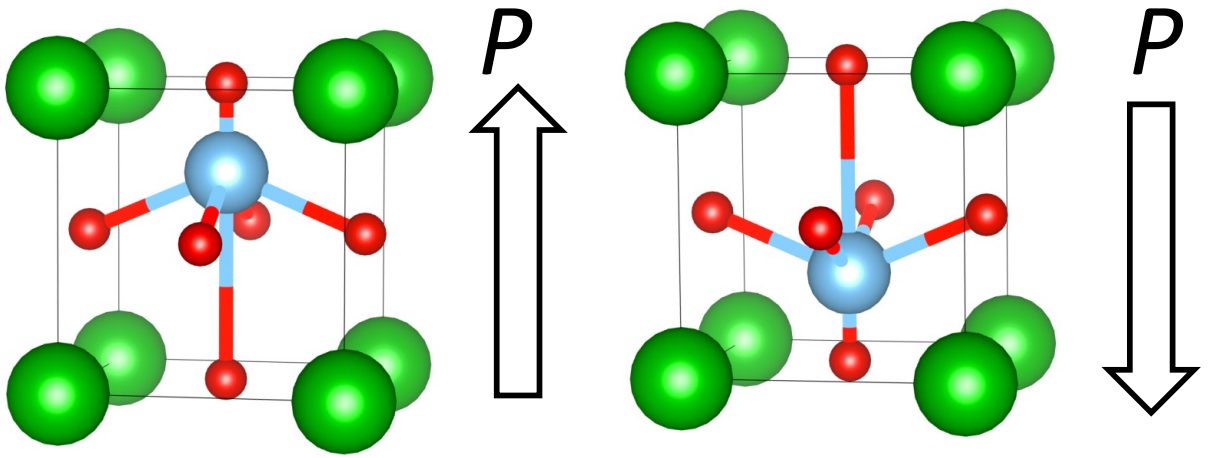
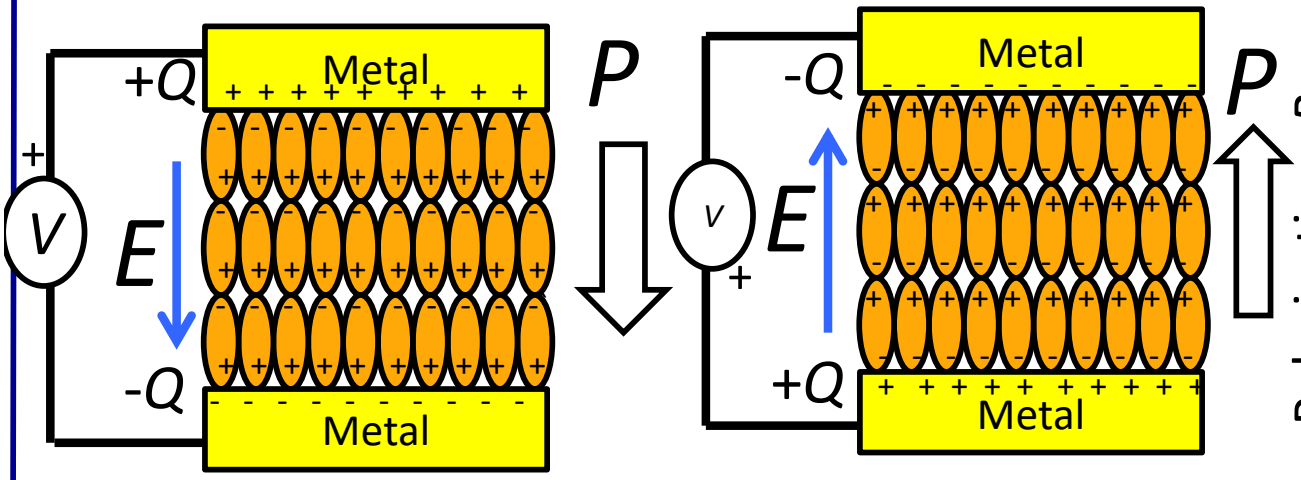
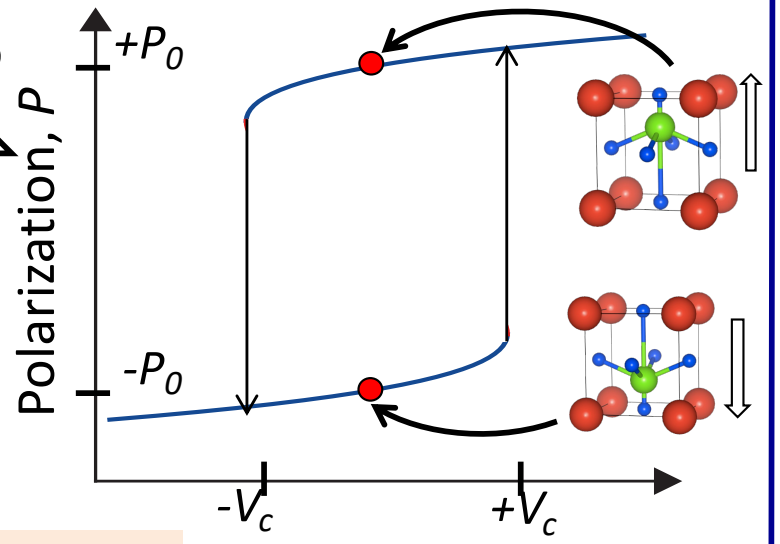
Ferroelectric Oxides

Classical Ferroelectric
$PbTiO_3$, $BaTiO_3$ etc.

Emerging CMOS compatible Ferroelectrics:
Doped HfO_2







A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercive voltage .

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A historical perspective

- Semiconductor community was heavily invested in Perovskite based FEs in 1990s and 2000s.
- FRAM products with perovskite-based FE were commercialized; total market cap ~1B$.
- Ferroelectrics activities in semiconductor community slowed down because perovskites are not scalable below 130 nm node.
- 2011 discovery of ferroelectricity in CMOS compatibility in HfO_2 renewed the interests!

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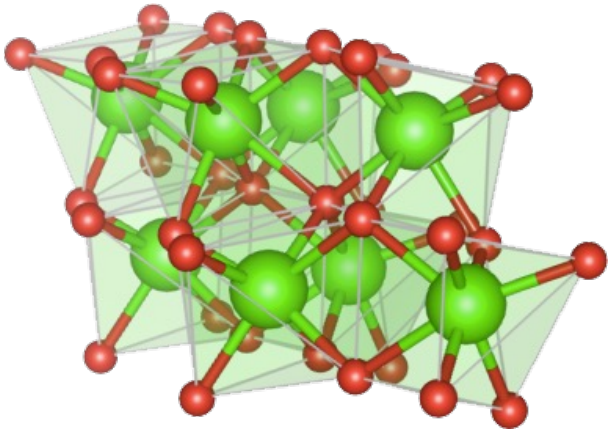
CMOS Compatible Ferroelectrics

New class of ferroelectric and antiferroelectric materials have emerged which can be introduced in commercial fabs!



Controlled annealing in **HfO_2** doped with Zr, Al, Si, Sr, Ti, La etc. induces a ferroelectric orthorhombic phase!

Boscke et al APL 99, 112904 (2011)
Boscke et al IEDM 2011

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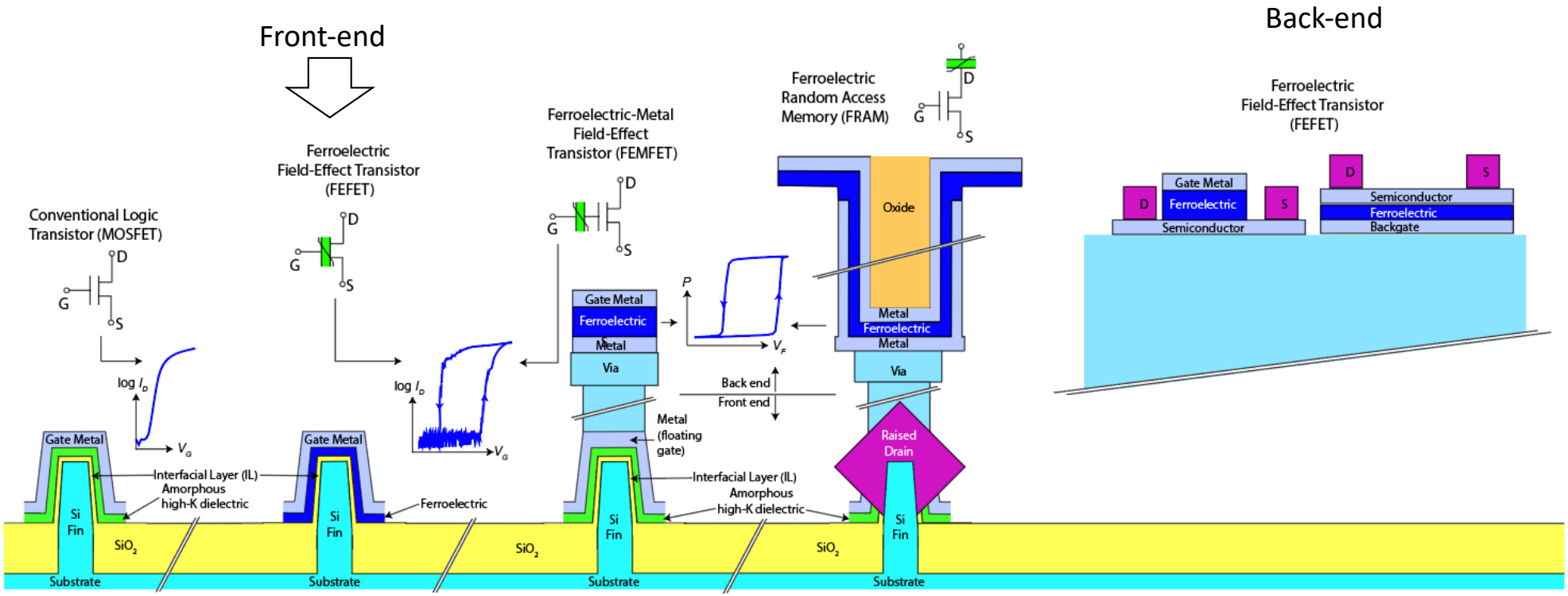
The Suite of Ferroelectric devices



Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

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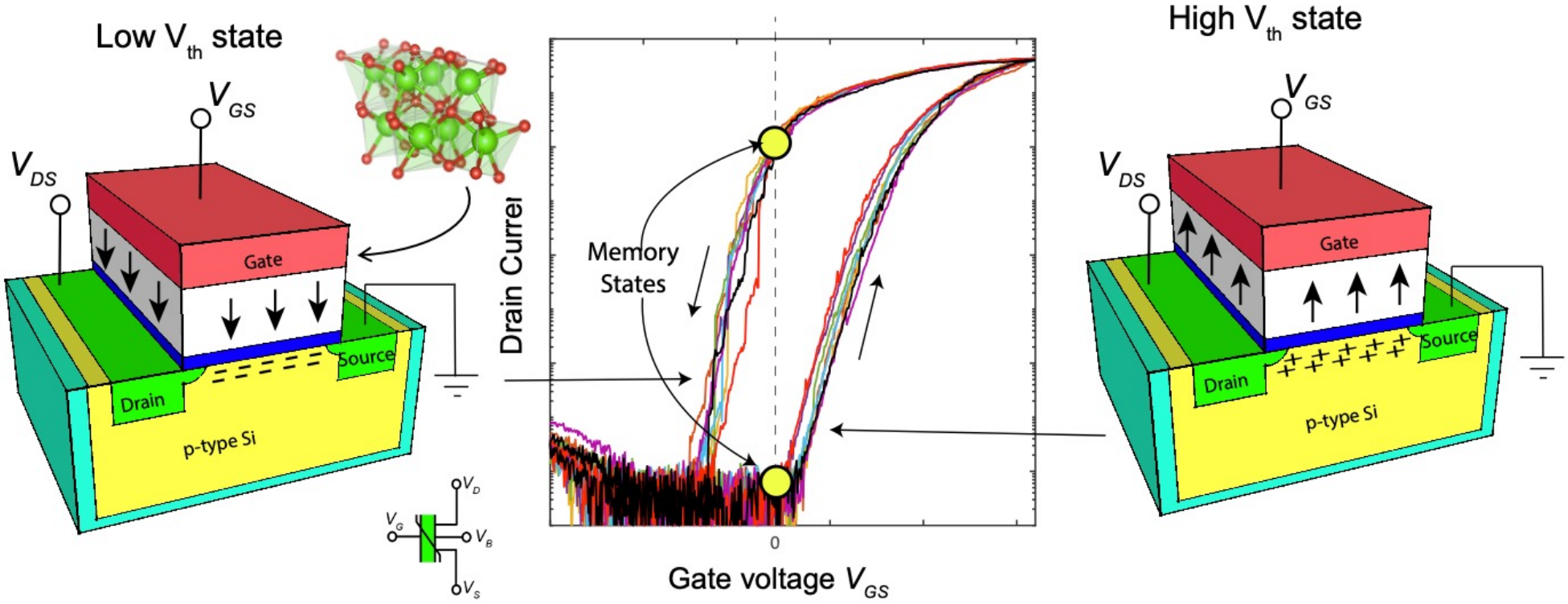
A ferroelectric field-effect transistor

Ferrroelectric Transistors (FEFET): Gate oxide stack includes a FE oxide



A ferroelectric transistor is a non-volatile memory device where the data is encoded in its threshold voltage.

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FEFET as embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM[70]	eFlash (FG)	eFlash (SG MONOS)[42]	eFlash (SONOS)[41]	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based)[67]
Cell size	120–150F^2	40F^2	40–60F^2	40–50F^2	50–60F^2	10–30F^2	10–30F^2	30–40F^2	50–60F^2
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 µs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	>10^{16}	>10^{16}	~10^4	~10^5	~10^6	10^5–10^9	>10^{10}	>10^{12}	>10^{14}

Khan, Keshavarzi, Datta, “The future of ferroelectric field-effect transistor technology”, Nature Electronics 2020

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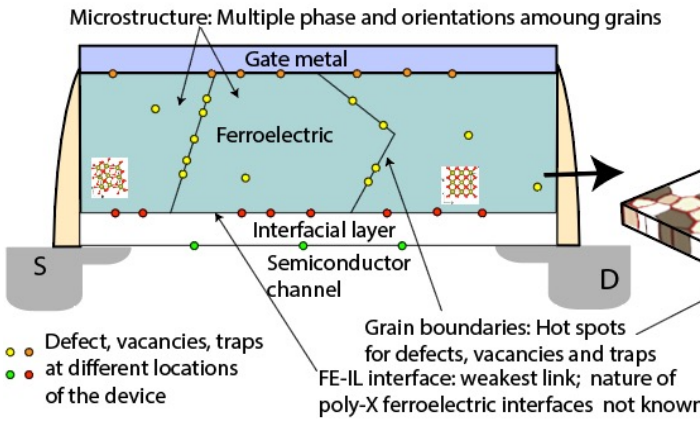
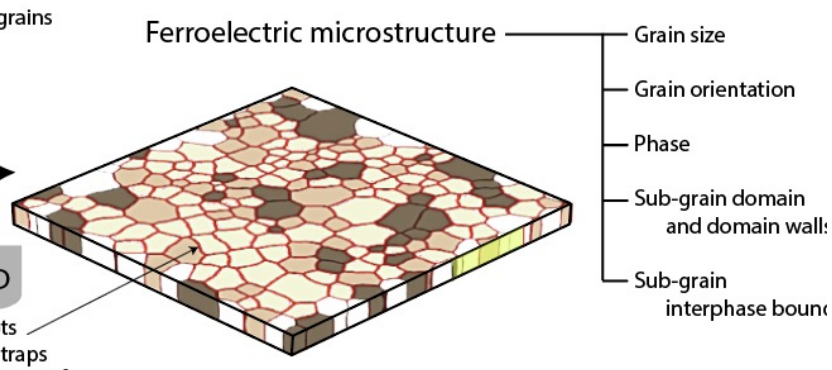
FEFET challenges (2020)

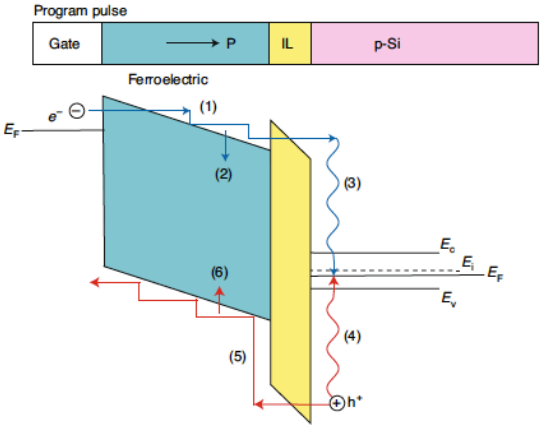
1
Write voltage and memory window

2
Device-to-device and cycle-to-cycle variation

3
Reliability and endurance







Goals (on the ambitious side)

<1.5 V write voltage
>0.5 V memory window

$\Delta V_{t,3\sigma}$ = 20-50 mV (7 nm node)

>10^{12} cycles

State-of-the-art

3-9 V write for 0.5-1.2 V memory window

$\Delta V_{t,3\sigma}$ = 200-500 mV (W,L=200 nm)
(Maekawa et al. VLSI 2019)

10^{8} cycles

"The future of ferroelectric field-effect transistor technology", Nature Ele. 2020.

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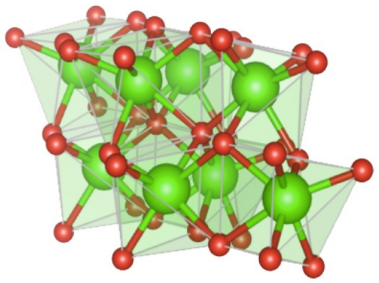
Ferroelectric field-effect transistor

Ferroelectric Oxide



Properties of Ferroelectric oxides

- Non-volatility and hysteresis
- Plasticity, Meta-plasticity and Anti-plasticity
- Negative dielectric permittivity/negative capacitance
- Stochasticity

Ferroelectric FET is one of most versatile transistor technologies – ever conceived.

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

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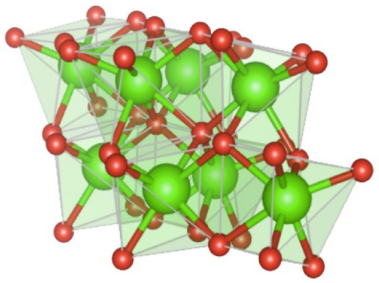
Ferroelectric field-effect transistor

Ferroelectric Oxide



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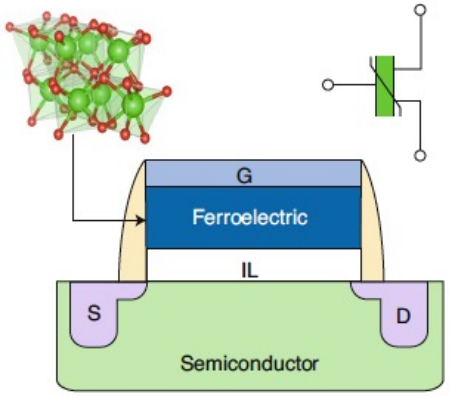
Ferroelectric field-effect transistor



Properties enabled by a transistor structure

- Transistor physics
- Transconductance gain
- Circuit-level design

Ferroelectric FET is one of most versatile transistor technologies – ever conceived.

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

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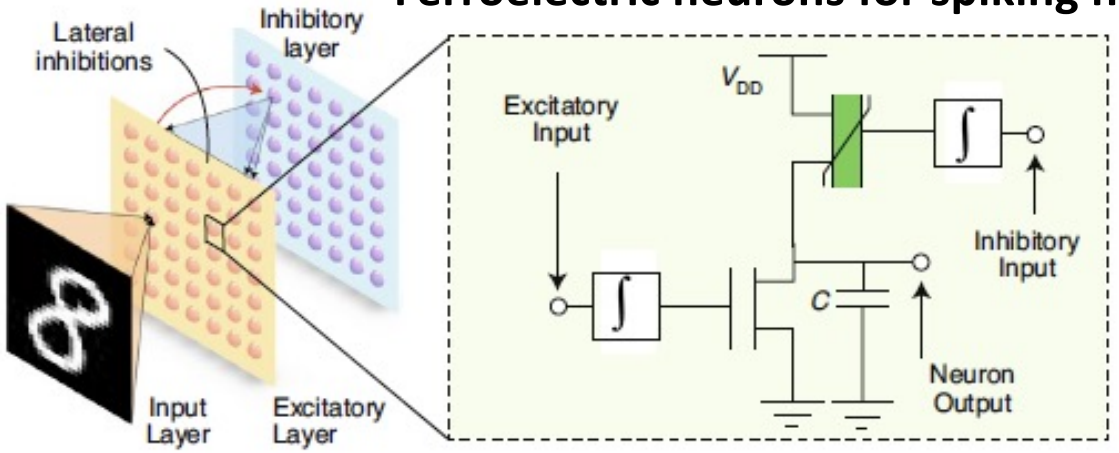
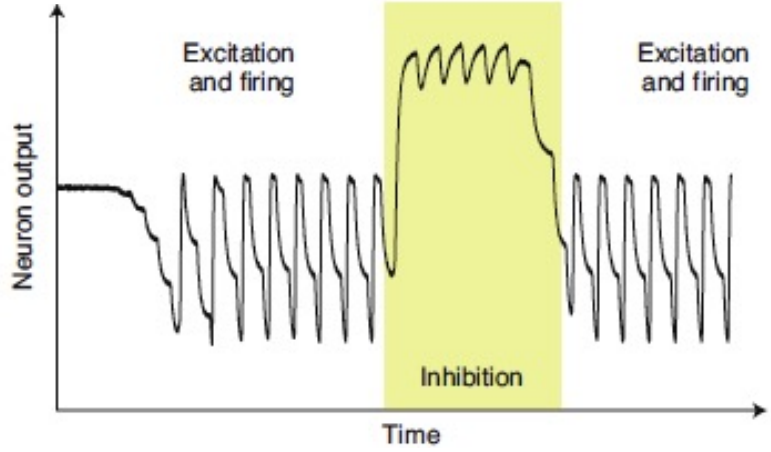
Ferroelectric FET Applications

1

Ferroelectric neurons for spiking neural networks

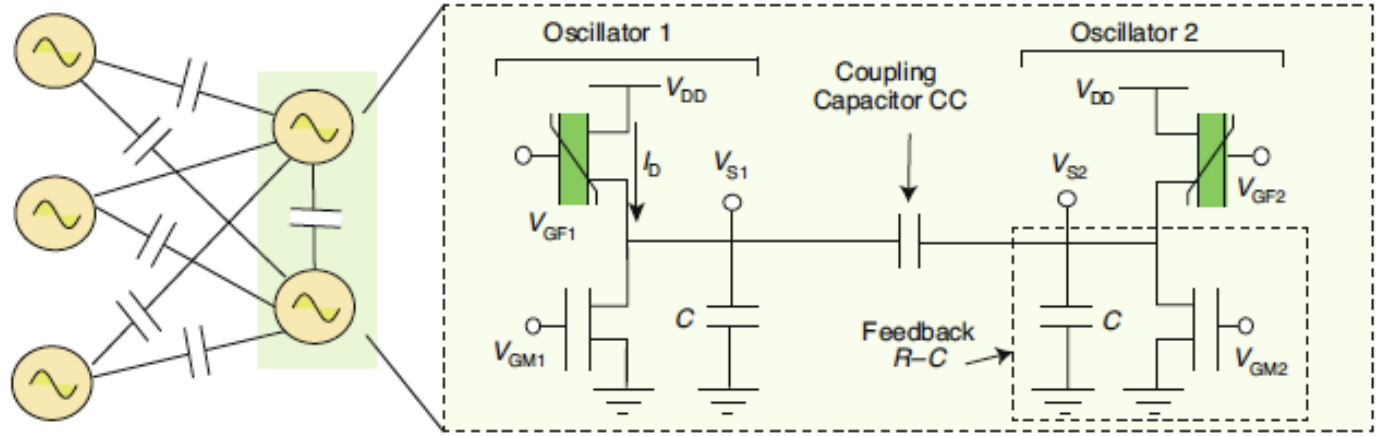


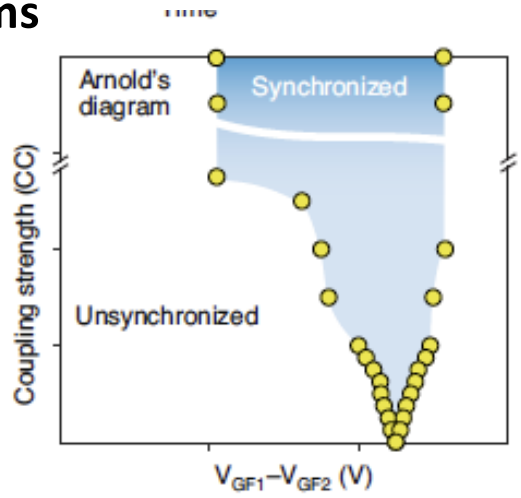


Wang et al. Int. Electron Dev. Meeting (IEDM) 2018.

2

Ferroelectric oscillators for time dynamical systems





Z. Wang et al. EDL 2017

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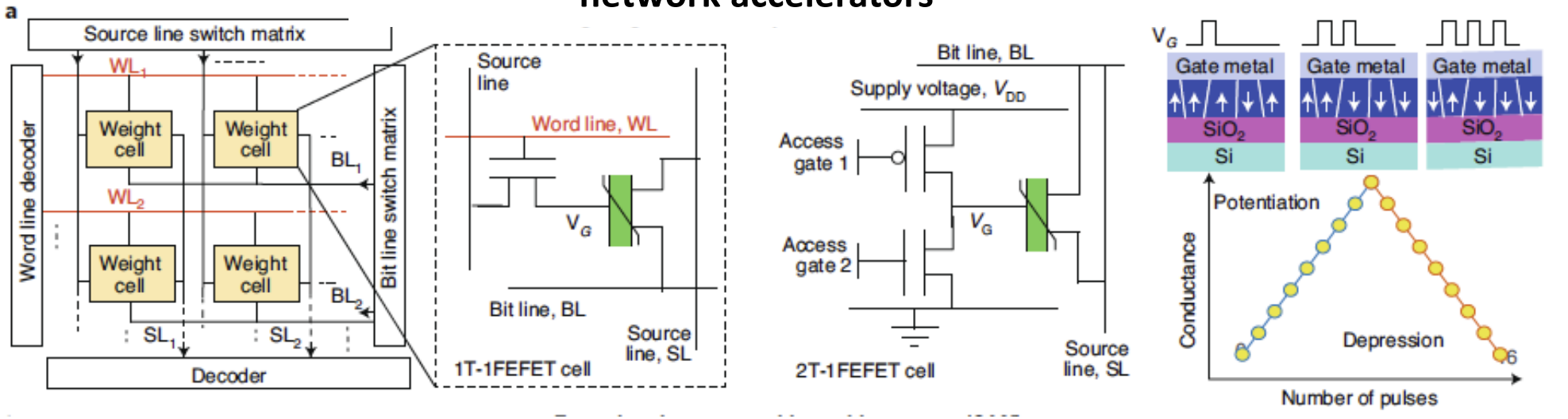
Ferroelectric FET Applications

3

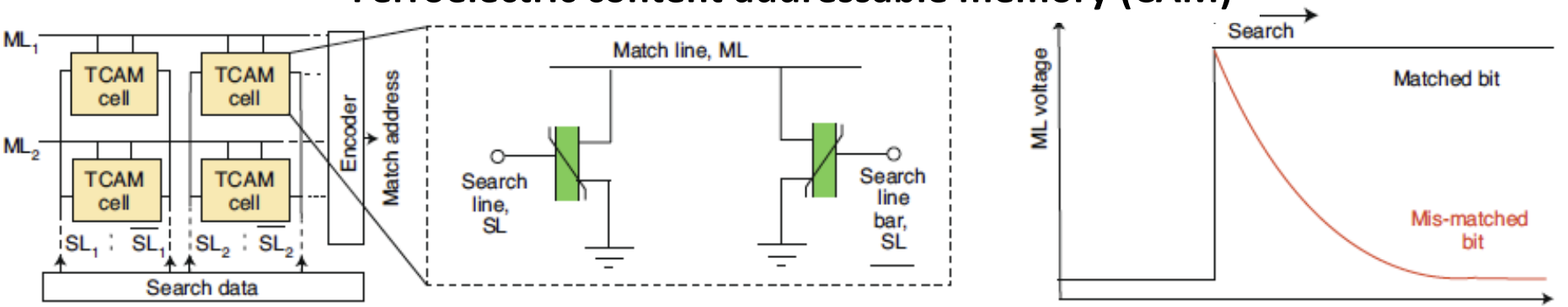
Ferroelectric synapses for deep neural network accelerators



Aabrar et al. A Thousand State Superlattice (SL) FEFET Analog Weight Cell. VLSI Symp. 2022.

4

Ferroelectric content addressable memory (CAM)



Tan et al. IEEE EDL 41, 240 (2019)

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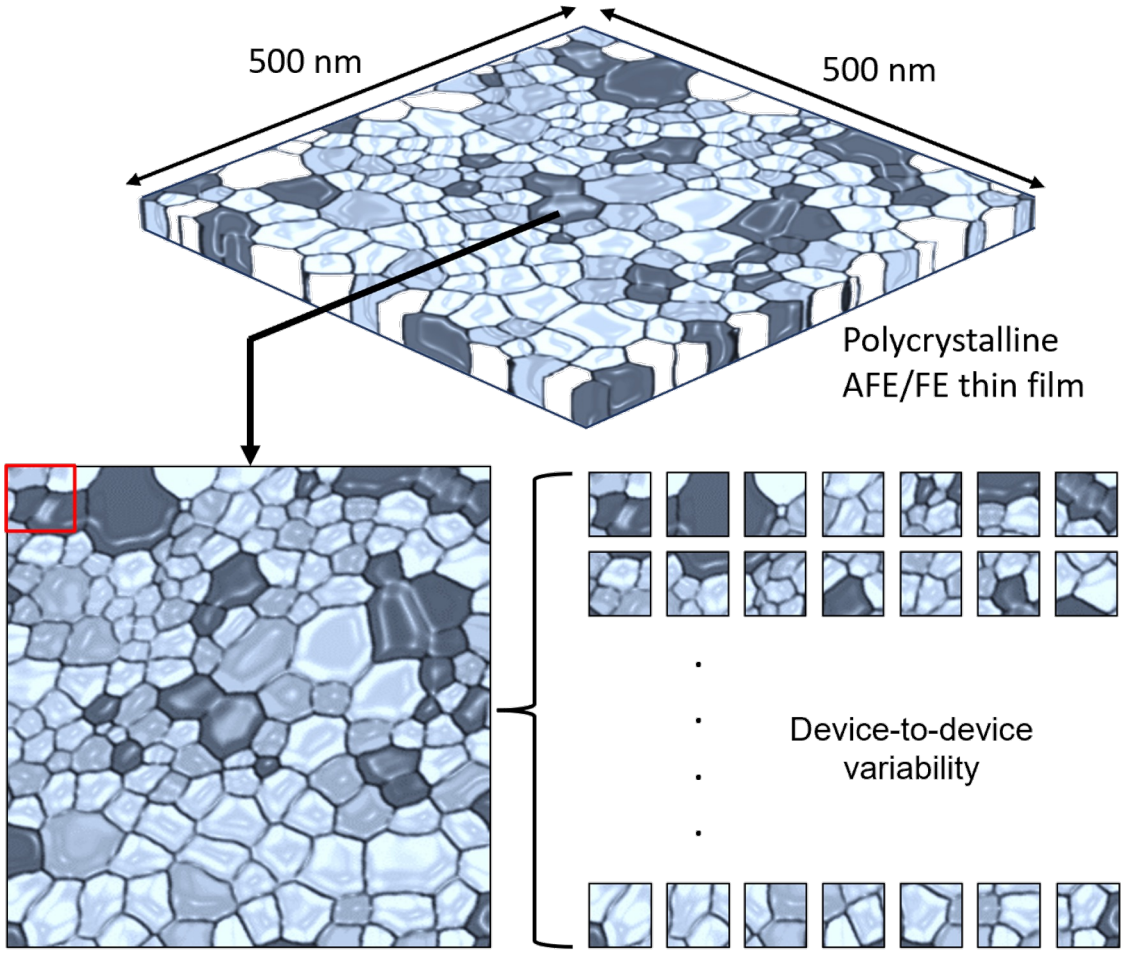
Ferroelectric Microstructure



1. Phase (o-, m-, t-)
2. Grain size
3. Grain orientation

Device to device variability

4. Grain boundaries
5. Domain Walls
6. Inter-phase boundaries

Trapping hot-spots

7. Irreversible change of micro-structure with electric field cycling

Cycle to cycle variability

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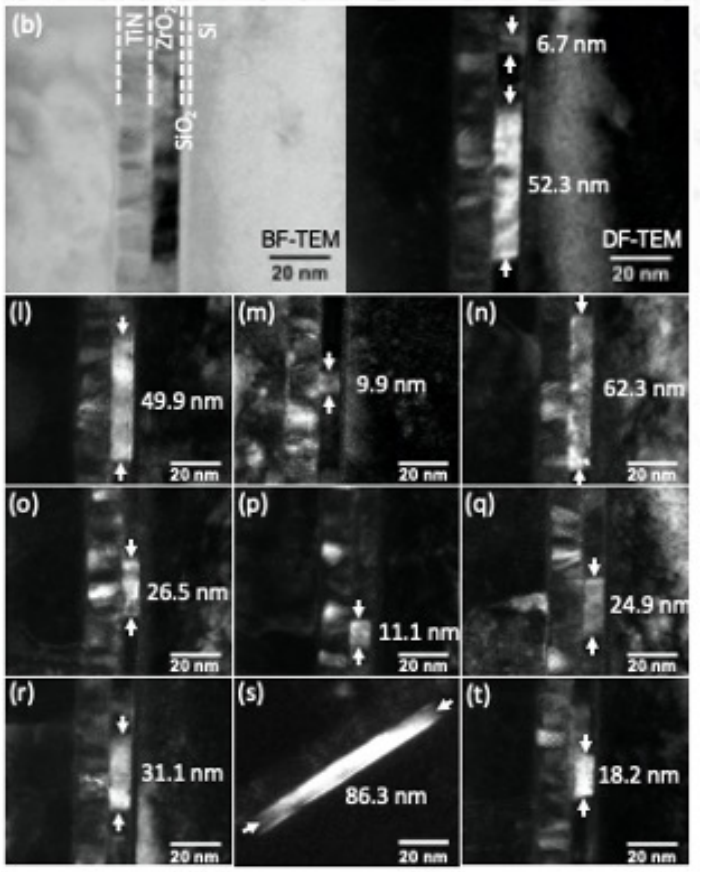
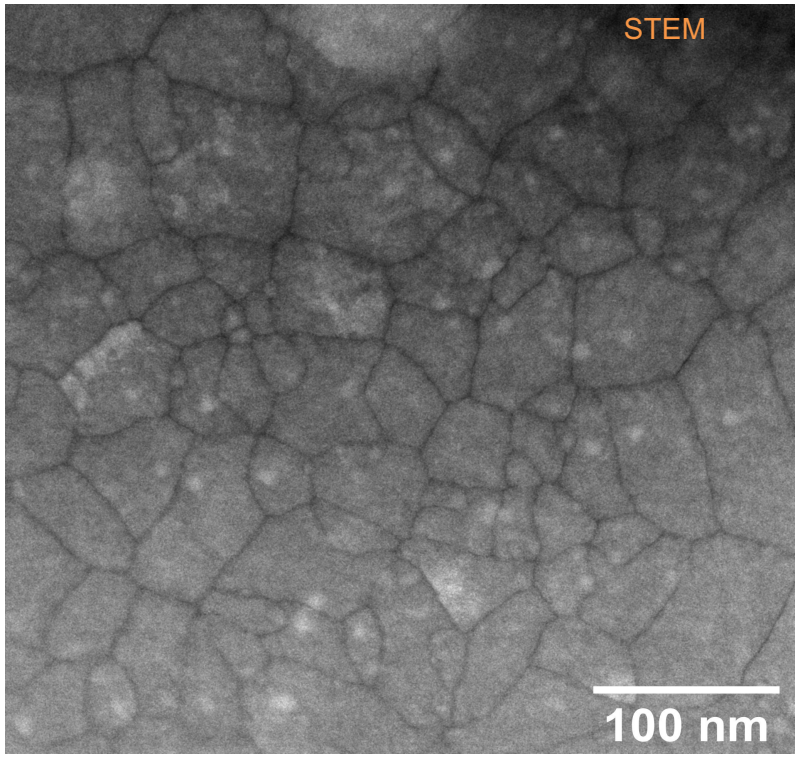
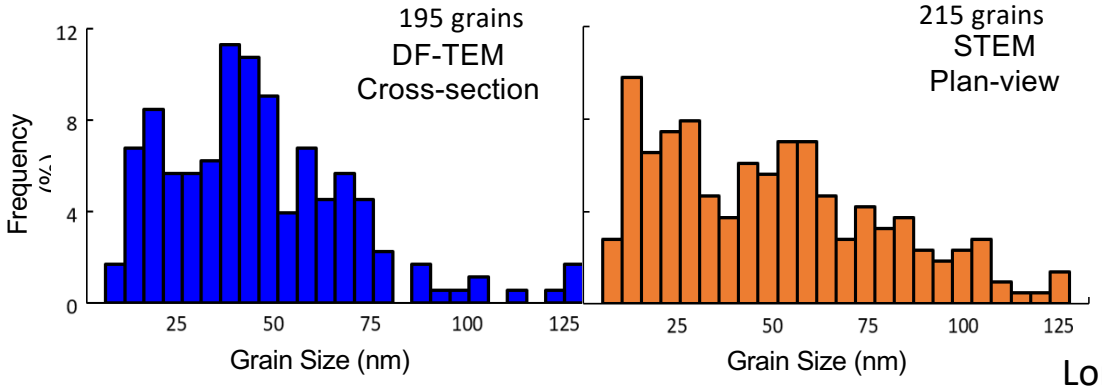
Quantification of Microstructure

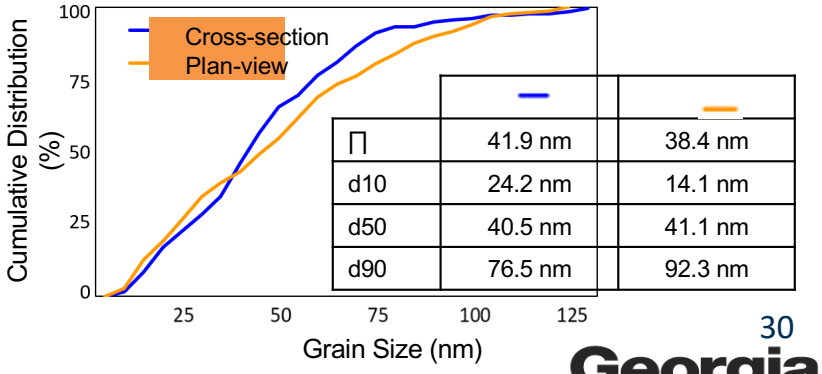
Dark Field TEM



Plan-view STEM







∏	41.9 nm	38.4 nm
d10	24.2 nm	14.1 nm
d50	40.5 nm	41.1 nm
d90	76.5 nm	92.3 nm

Lombardo et al. APL 119, 092901 (2021)

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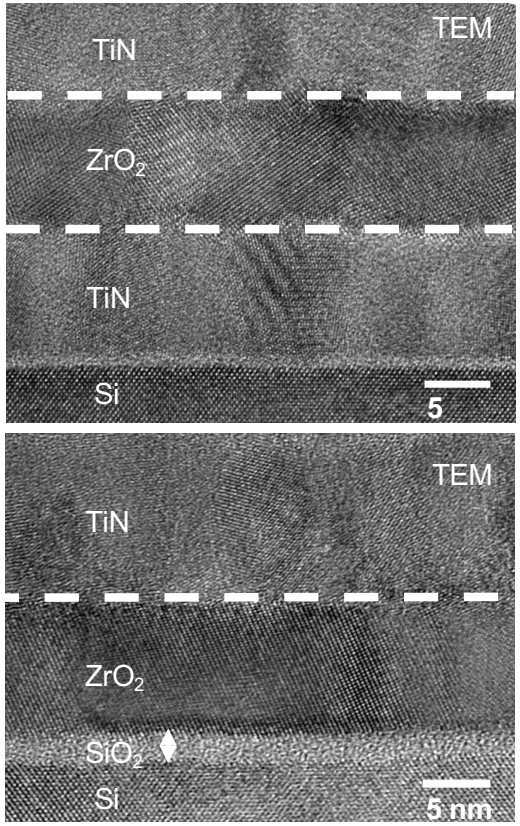
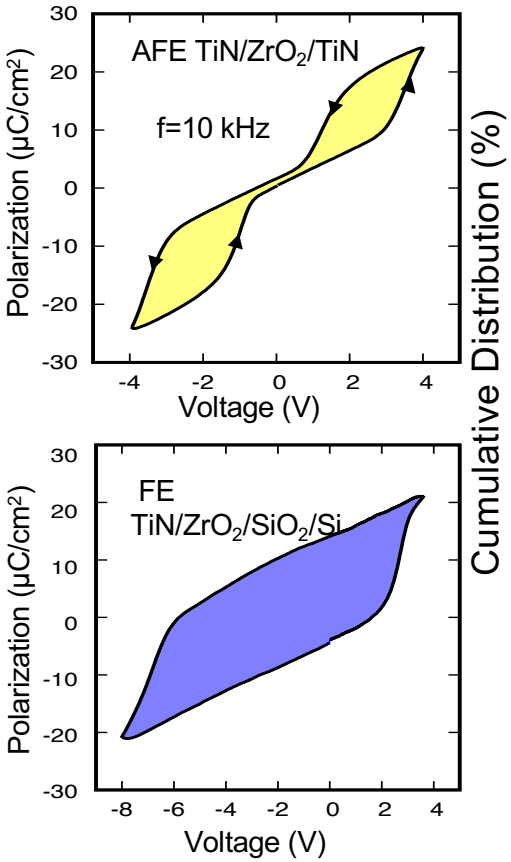
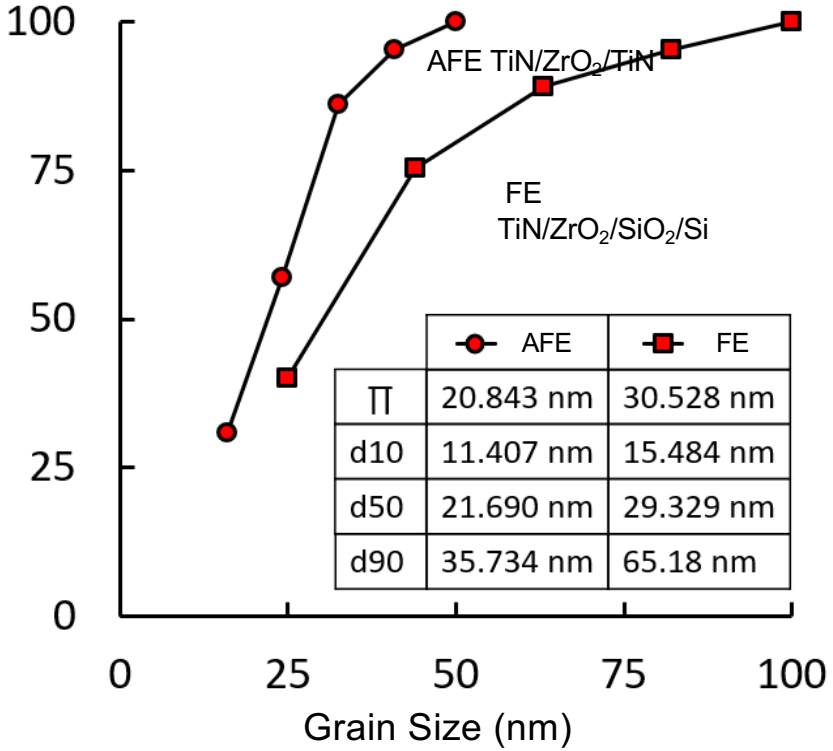
Microstructural origin of AFE and FE in zirconia







	AFE	FE
T	20.843 nm	30.528 nm
d10	11.407 nm	15.484 nm
d50	21.690 nm	29.329 nm
d90	35.734 nm	65.18 nm

Chae* & Lombardo* et al. *ACS Adv. Mat. & Int.*, (2022).

Smaller grain size favored by Tetragonal phase over FE Orthorhombic phase

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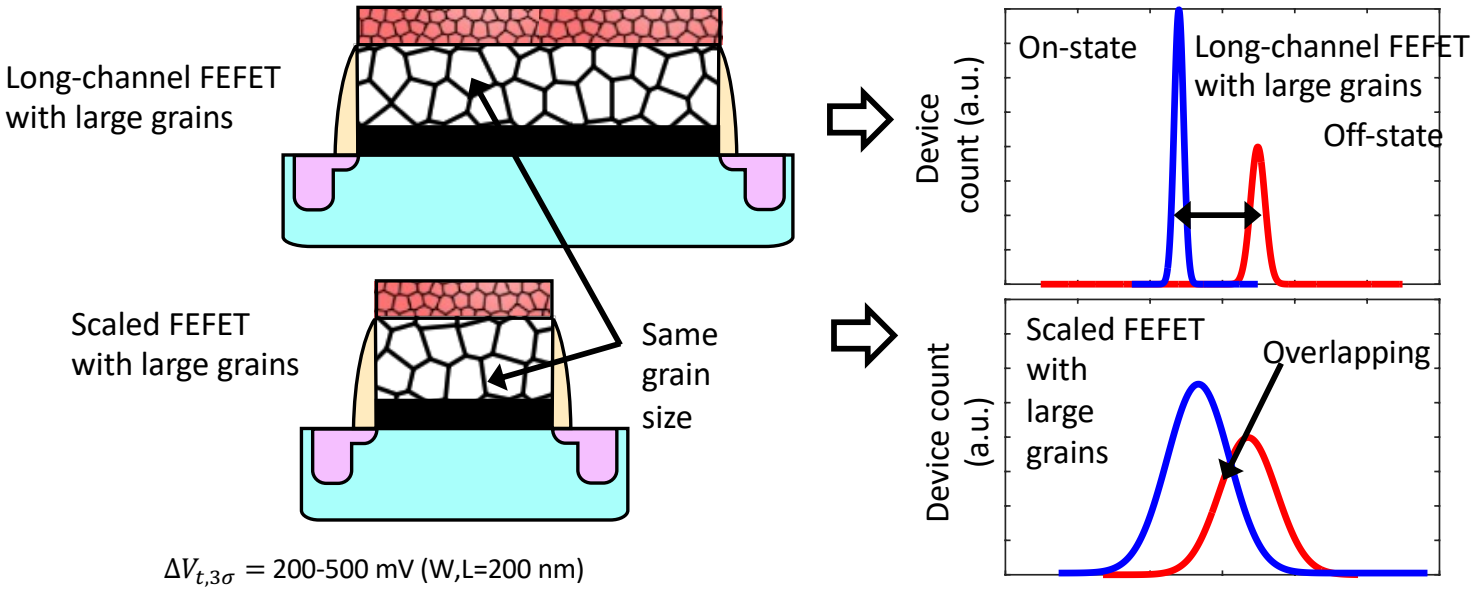
Ferroelectric Microstructure and Variation

Variation



$\Delta V_{t,3\sigma}$ = 200-500 mV (W,L=200 nm)
(Maekawa et al. VLSI 2019)

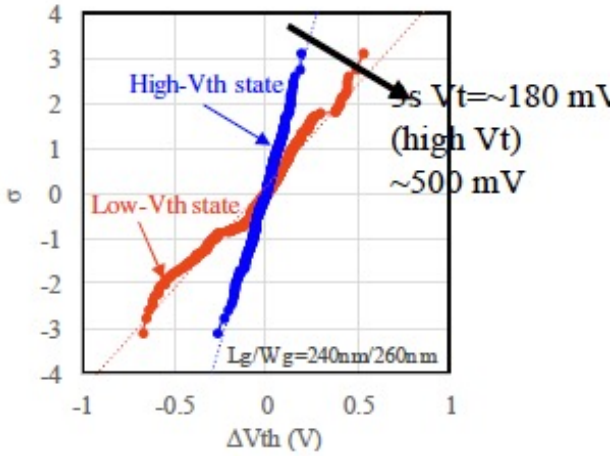


Fig. 5 Cumulative frequency distribution of relative Vth after Vg sweep in the non-doped FeFET for the two polarization states.

at

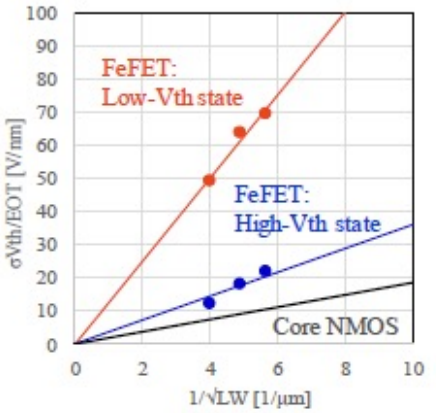


Fig. 7 Vth variation divided by the dielectric thickness in the non-doped FeFET and core NMOSFET (Pelgrom plot).

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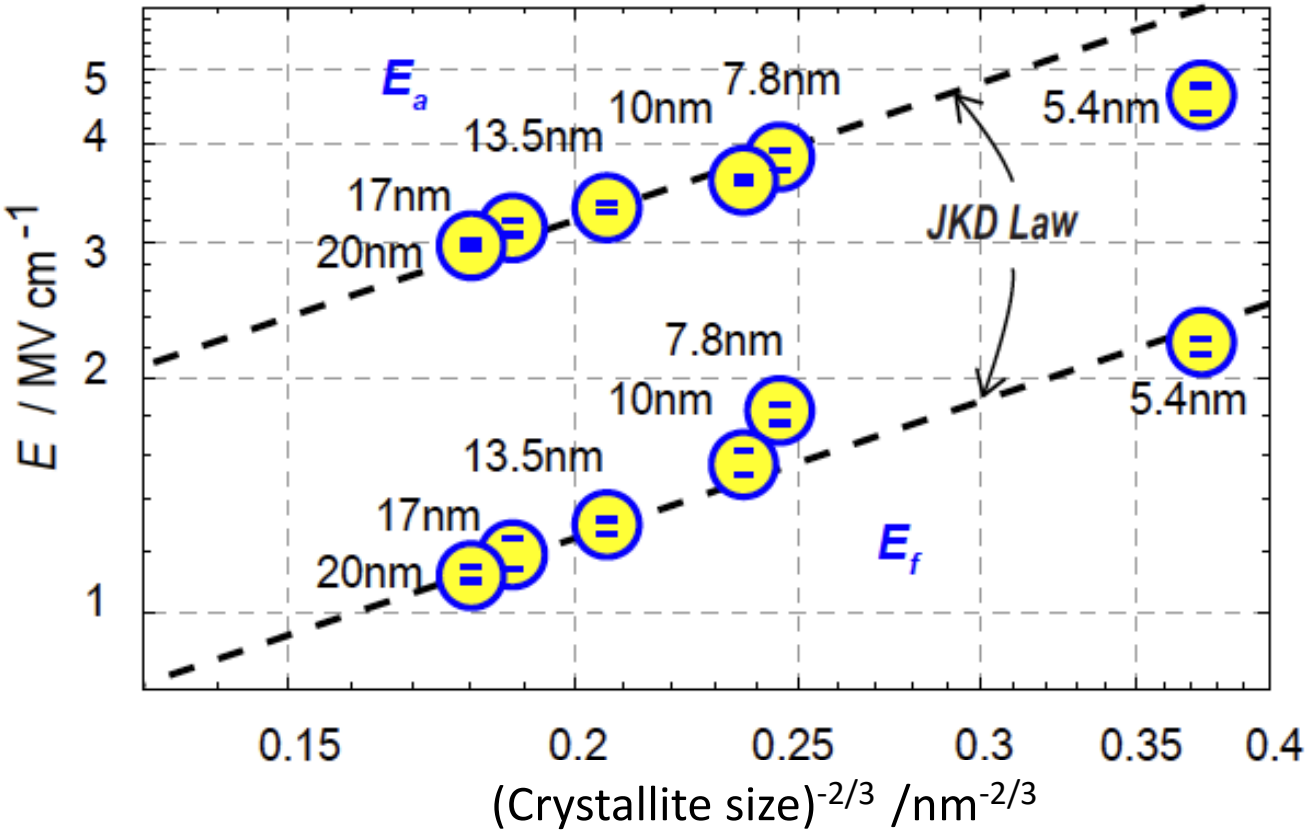
Microstructure and Functional Responses

Modified Jannovec-Kay-Dunn law for ZrO_2

Critical field ∝ (crystallite size)$^{-2/3}$



Tasneem *et al.* "A Janovec-Kay-Dunn-like behavior at thickness scaling in ultra-thin antiferroelectric ZrO_2 films." (under review.)

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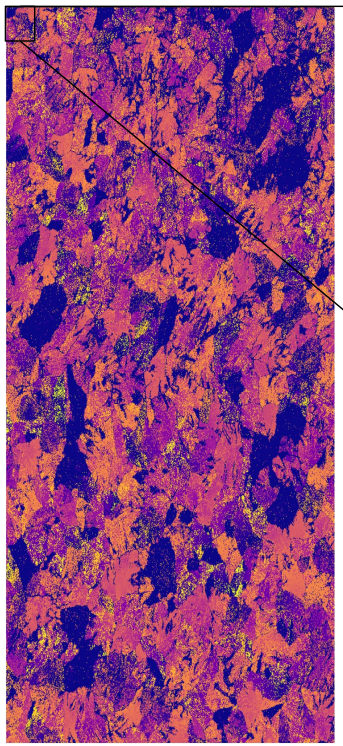
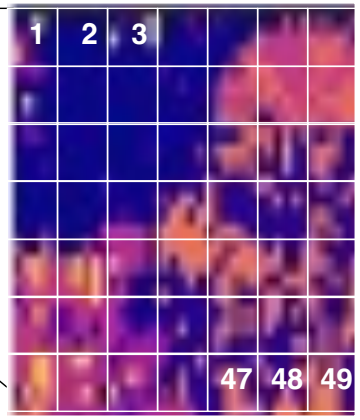
Machine Learning Assisted Predictive TCAD Modeling (from Metrology to Device Metrics)



Ferro polarization map (from TKD data from SEM/TEM)



7×7 image

Total 14700 samples
Used 4000 samples
(not randomly)

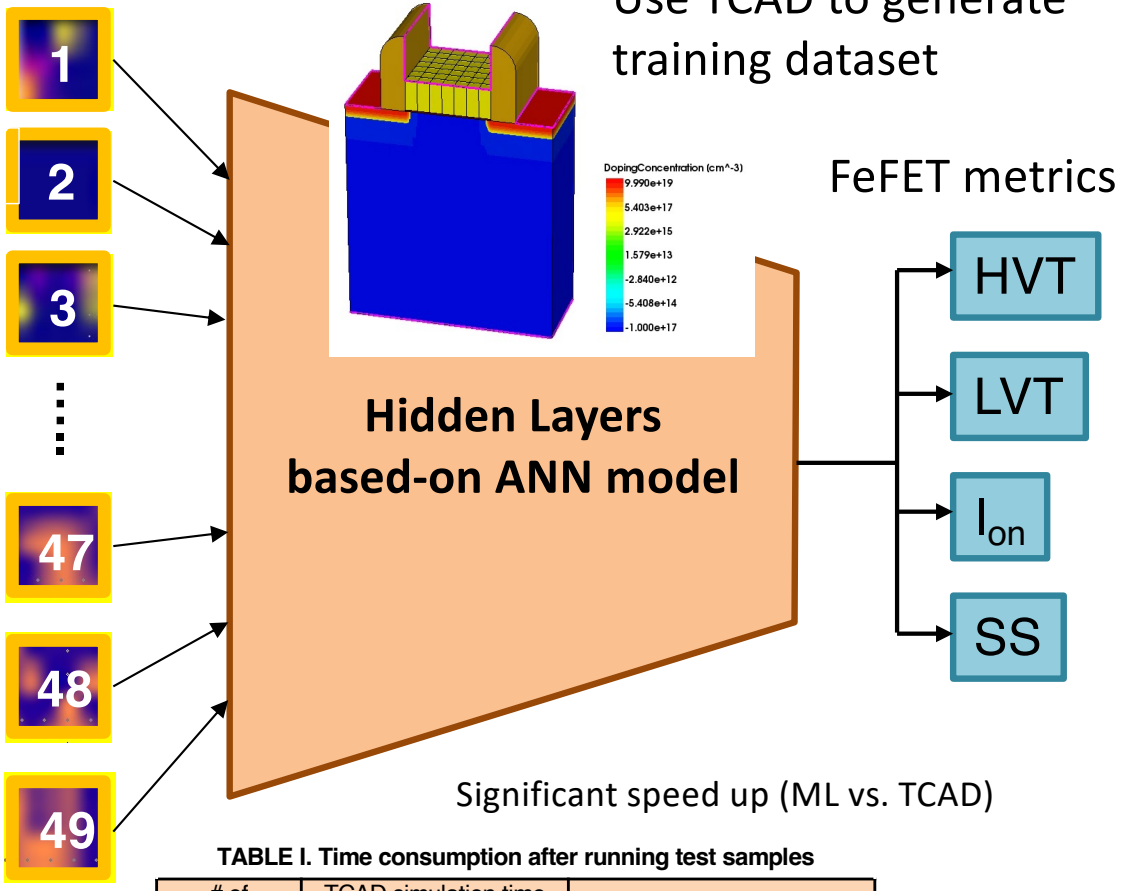


TABLE I. Time consumption after running test samples

# of samples	TCAD simulation time [h]	ML-based inference time [h]
1	0.078	5e-8
500	39	2.5e-5
1,000	78	5.3e-5
2,000	156	1.07e-4
10,000	780	5.3e-4
14,700	1146.6 (=48 days)	7.79e-4 (=2.8 secs)

G. Choe, P. V. Ravindran, A. Lu, J. Hur, M. Lederer, A. Reck, S. Lombardo, N. Afroze, J. Kacher, A. I. Khan, S. Yu, "Machine learning assisted statistical variation analysis of ferroelectric transistors: from experimental metrology to predictive modeling," IEEE Symposium on VLSI Technology and Circuits (VLSI) 2022

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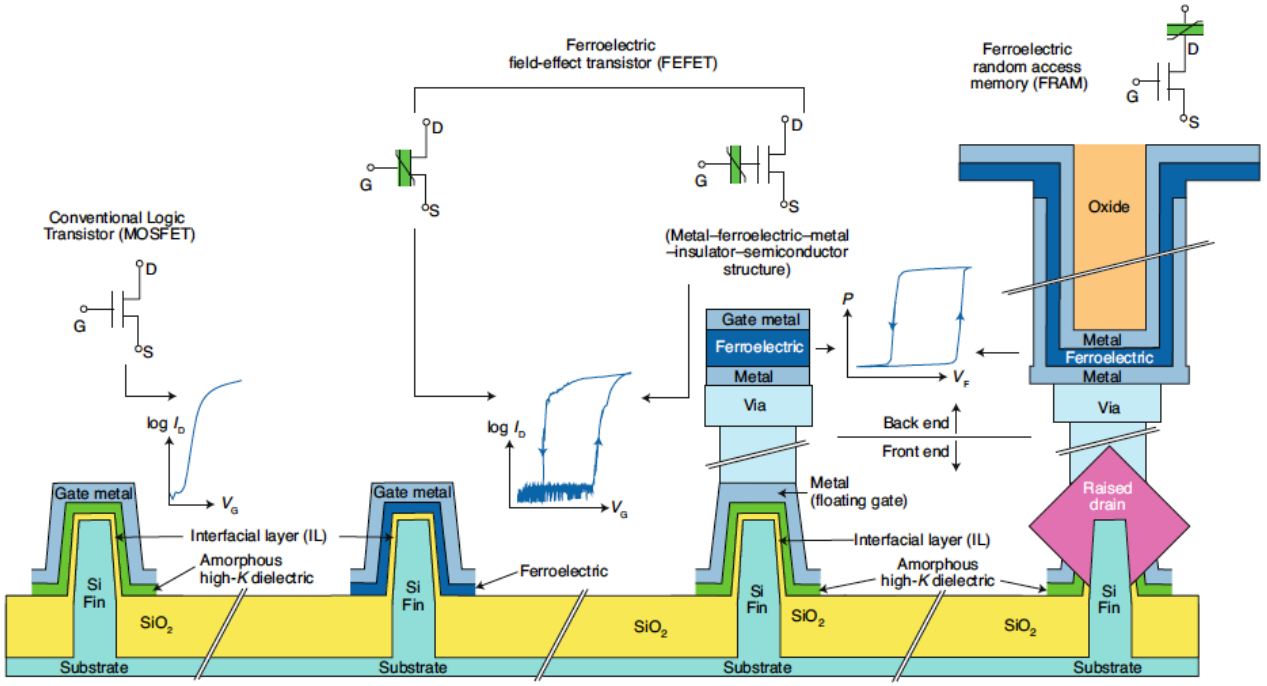
Thank you!



PERSPECTIVE
https://doi.org/10.1038/s41928-020-00492-7
nature electronics
Check for updates

The future of ferroelectric field-effect transistor technology

Asif Islam Khan[1,2] ✉, Ali Keshavarzi[3] ✉ and Suman Datta[4] ✉

Khan, Keshavarzi, Datta. "The future of ferroelectric field-effect transistors." *Nature Electronics* 3, 588 (2020).

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