Ferroelectric Field-effect Transistors as High-density, Ultra-fast, Embedded Non-volatile Memories

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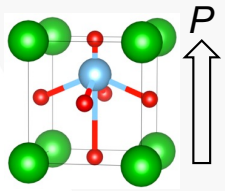
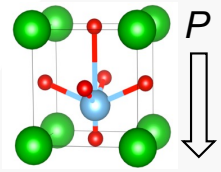
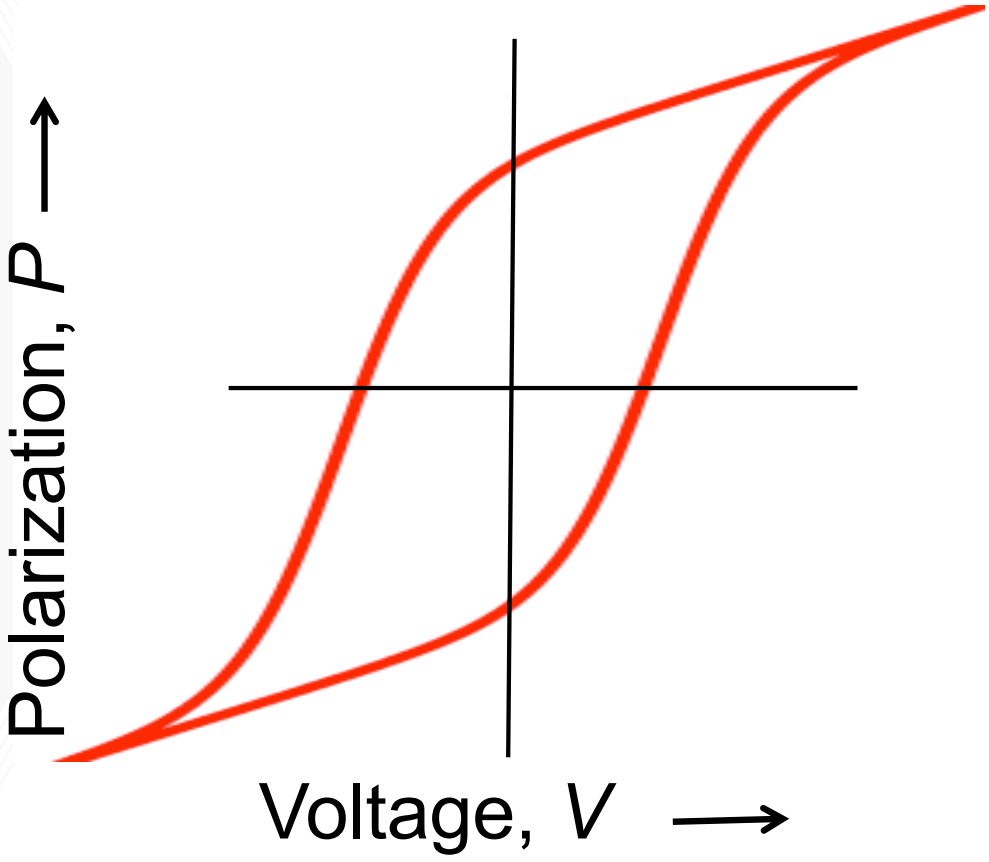
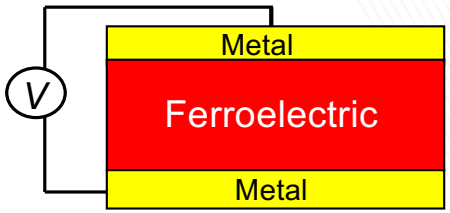
Ferroelectricity



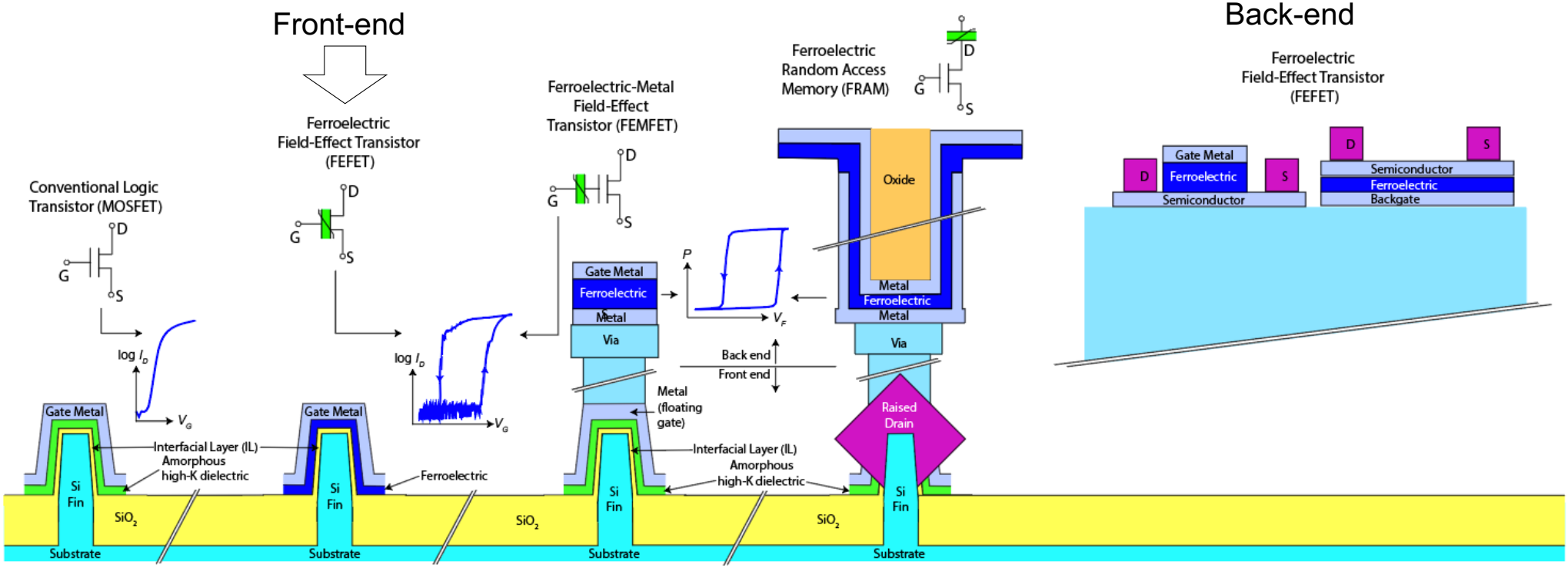


Pb^{2+} Ti^{4+} O^{2-}





Ferroelectric devices



Khan, Keshavarzi, Datta, “The future of ferroelectric field-effect transistor technology”, Nature Electronics 2020

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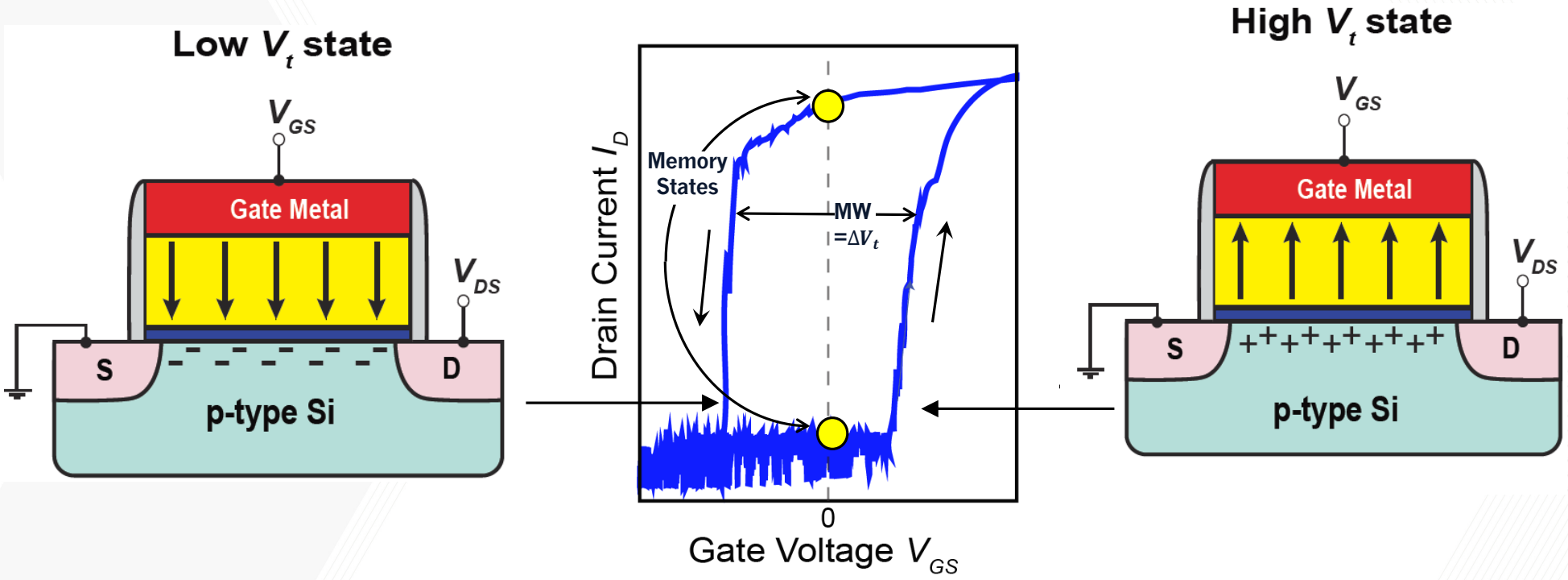
Ferroelectric Field Effect Transistors



FEFET is a FET with the threshold voltage shifted by the remnant polarization.

FEFET as embedded memory

Metrics	Mainstream embedded memory					Embedded ferroelectric memory			
	eSRAM	eDRAM[70]	eFlash (FG)	eFlash (SG MONOS)[42]	eFlash (SONOS)[41]	FEFET (hafnia based, MFIS structure)	FEFET (hafnia based, MFMIS structure)	FRAM (hafnia based)	FRAM (perovskite based)[67]
Cell size	120–150F^2	40F^2	40–60F^2	40–50F^2	50–60F^2	10–30F^2	10–30F^2	30–40F^2	50–60F^2
Cell structure	6T	1T1C	1.5T	1.5T	2T	1T	1T1FE, 1T	1T1FE, 2T2FE	1T1FE, 2T2FE
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-bit operation	No	No	Yes	Yes	Yes	Yes	Yes	No	No
Non-destructive read	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
Status	Av.	Dev.	Av.	Dev.	Dev.	Res.	Res.	Res.	Av.
Advanced node demonstration	7 nm FinFET	22 nm FinFET	40 nm	16 nm FinFET	28 nm HKMG	22 nm FDSOI	N/A	N/A	130 nm
Write voltage	<1 V	<1 V	~12 V	~12 V	~5 V	1.5–4 V	~1.5 V	1–3 V	1.5 V
Write energy	~1 fJ	~1 pJ	~100 pJ	~100 pJ	1–10 pJ	1–10 fJ	1–10 fJ	~100 fJ	~1 pJ
Standby power	High	Medium	Low	Low	Low	Low	Low	Low	Low
Write speed	<1 ns	>10 ns	~100 ns	<100 ns	~100 ns	1–10 ns	1–10 ns	1–10 ns	1 µs
Read speed	<1 ns	>10 ns	~10 ns	<10 ns	~10 ns	1–10 ns	1–10 ns	1–25 ns	50–100 ns
Endurance	>10^{16}	>10^{16}	~10^4	~10^5	~10^6	10^5–10^9	>10^{10}	>10^{12}	>10^{14}

Khan, Keshavarzi, Datta, “The future of ferroelectric field-effect transistor technology”, Nature Electronics 2020

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Progress in FEFET Technology

1 Write voltage and speed	2 Device-to-device variation	3 Reliability and endurance
Goals (on the ambitious side)		
<1.5 V write voltage >0.5 V memory window <10 ns read-after-write delay	$\Delta V_{t,3\sigma}$ = 20-50 mV (7 nm node)	>10^{12} cycles

1. **Write voltage:**
   BEOL: ~1.6 V write with >0.7 V memory window (Sharma et al. IEDM 2020; Dutta et al. EDL 2022)
   FEOL: 3-9 V write for 0.5-1.2 V memory window
2. **Read-after-write delay:**
   "Immediate" read after write (Kleimaier et al. EDL 2021, Wang IEDM 2021; Hoffmann et al. EDL 2022).
3. **Endurance:**
   BEOL: >10^{12} cycles w/ <1 ns write (Sharma et al. IEDM 2020)
   FEOL: >10^{10} cycles (Tan et al. EDL 2021)
4. **Device-to-device variation:**
   $\Delta V_{t,3\sigma}$ = 200-500 mV (W,L=200 nm) (Maekawa et al. VLSI 2019)

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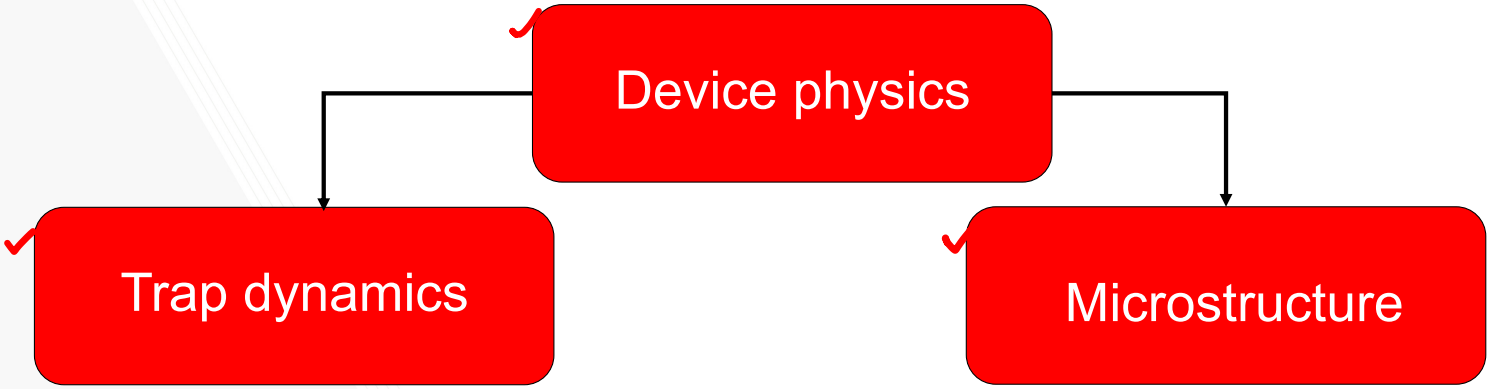
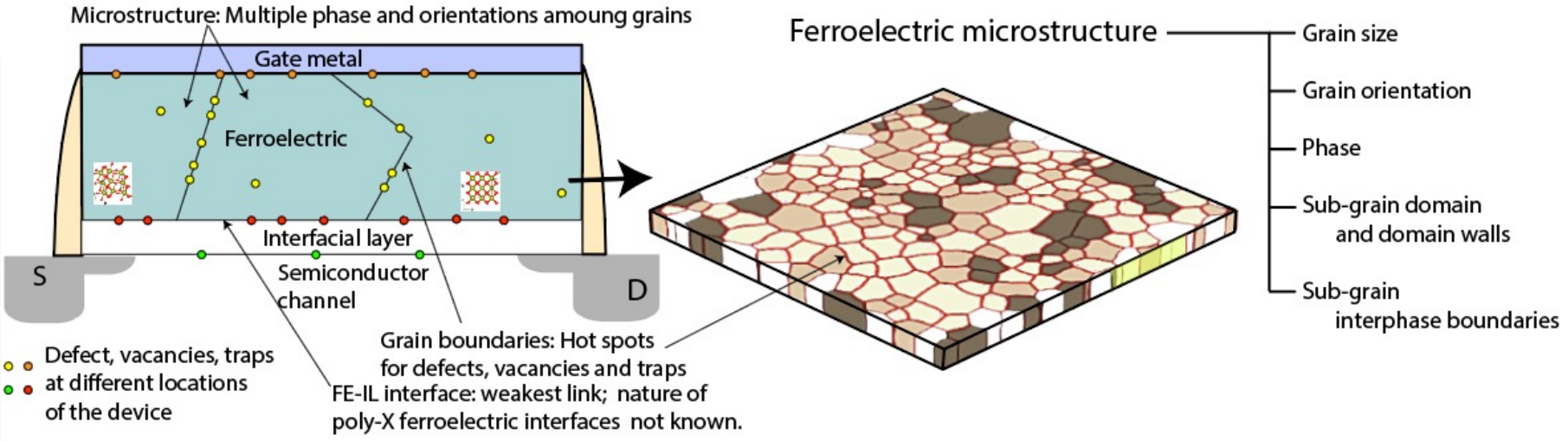
Progress in FEFET Technology





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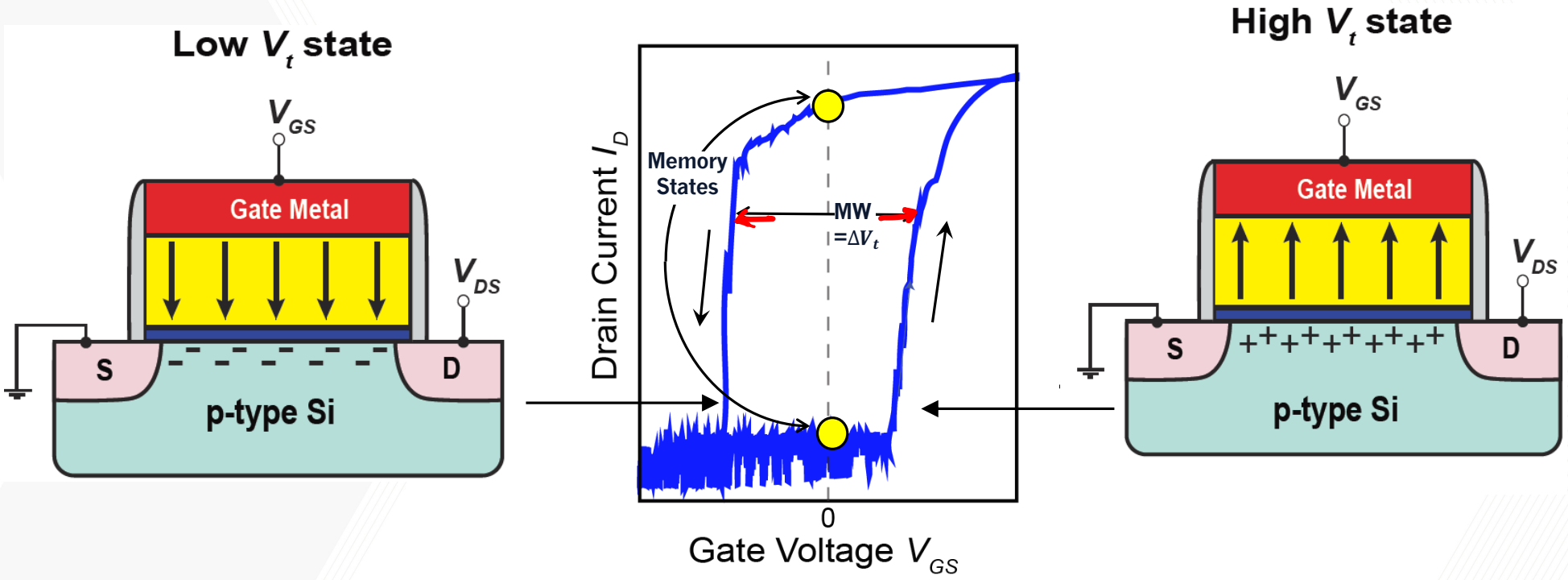
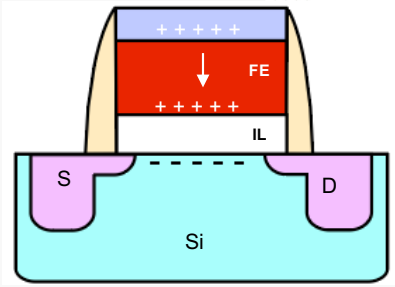
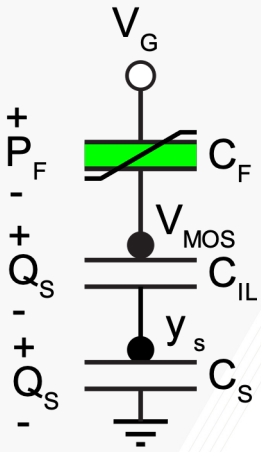
Ferroelectric Field Effect Transistors

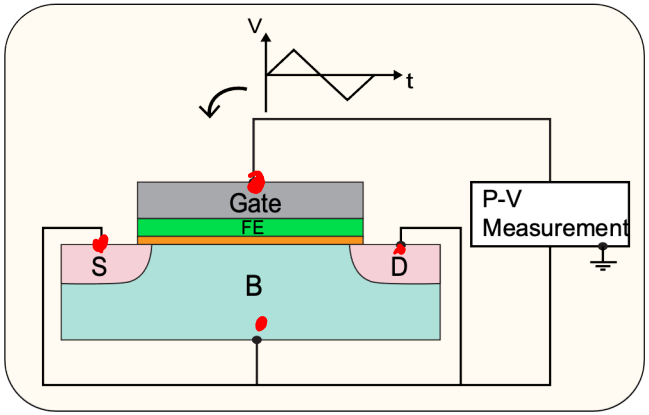


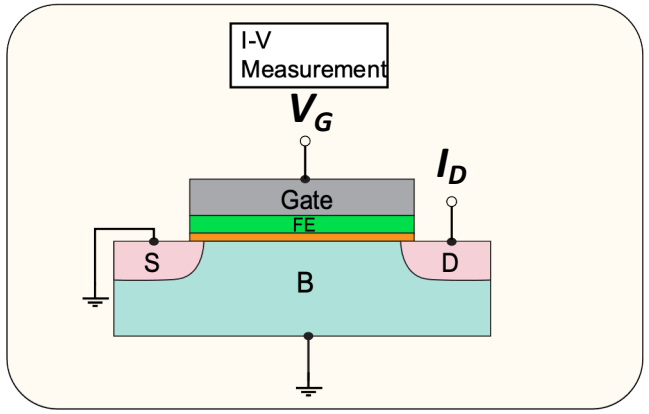
FEFET is a FET with the threshold voltage shifted by the remnant polarization.

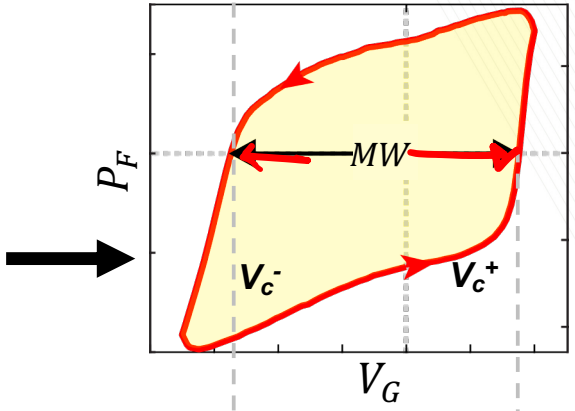
Ferroelectric Field Effect Transistors: Ideal theory

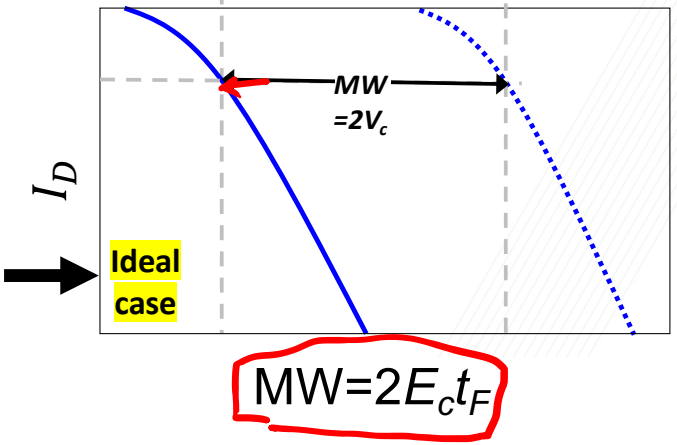










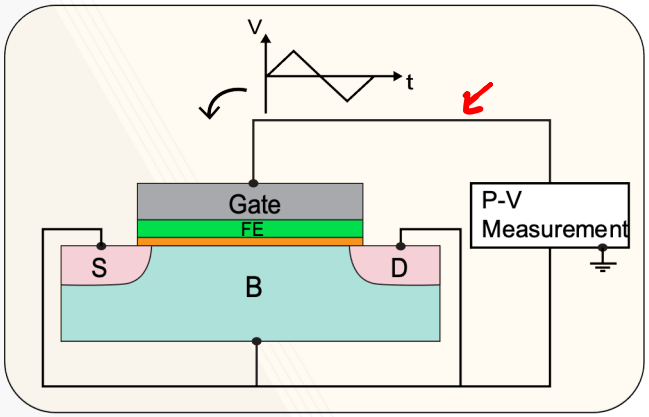


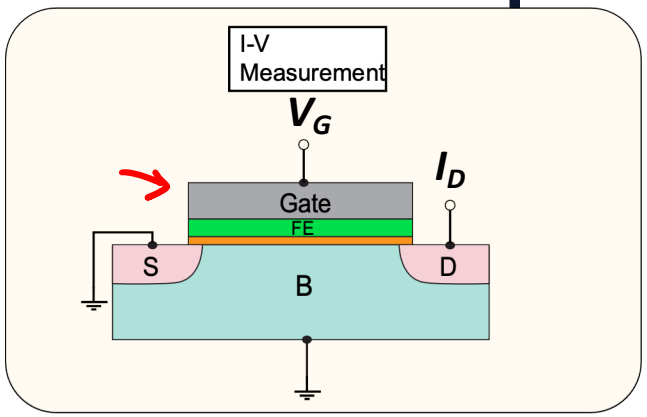
MW=2$E_c t_F$

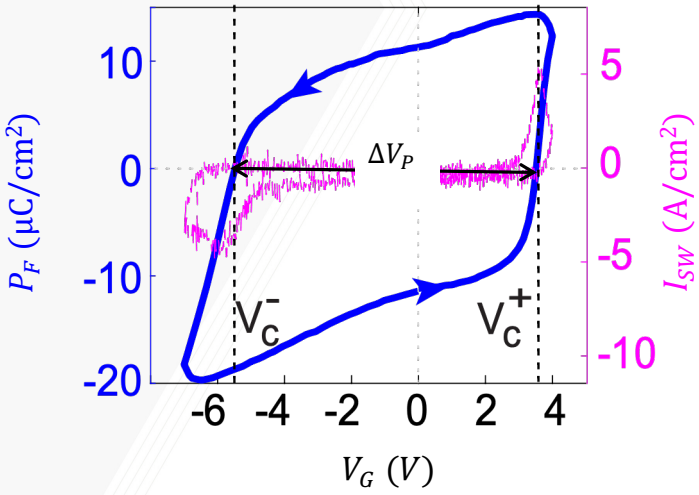
The maximum memory window is 2$E_c t_F$.

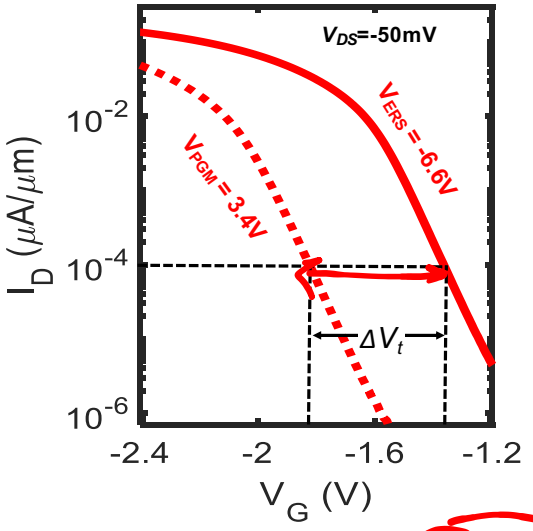
Tasneem *et. al.*, IEDM 2021, TED (submitted)

Ferroelectric Field Effect Transistors: Experimental





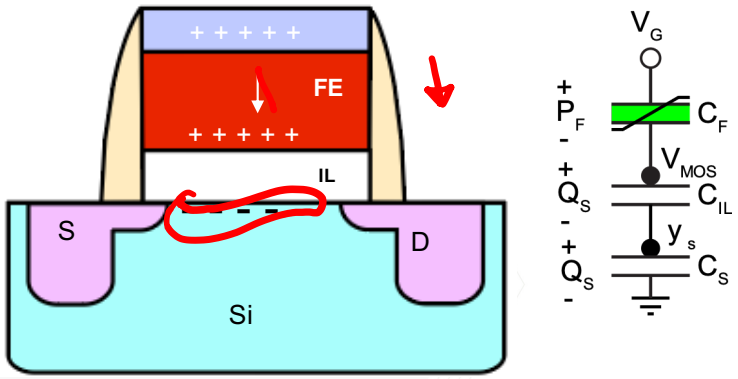




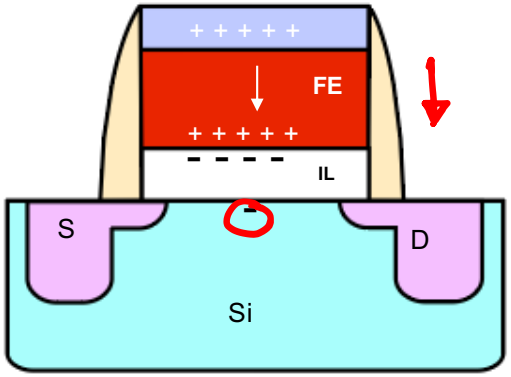
Experimentally, the maximum memory window is $<<2E_c t_F$

Fundamental deviation from Ideal FEFET theory

Ideal FEFET



Actual front-end FEFET model



1. Ferroelectric polarization switches completely, gets screened at interface.
2. The switching current flows through the IL as dissipative current, not a displacive/capacitive one – i.e., switching happens as a IL leakage.
3. ΔQ_S is only ~2-10% of ΔP_F
4. ΔV_t is only ~2-10% of ΔV_F

Toprasertpong *et al.* Proc. IEDM, 23.7 (2019).

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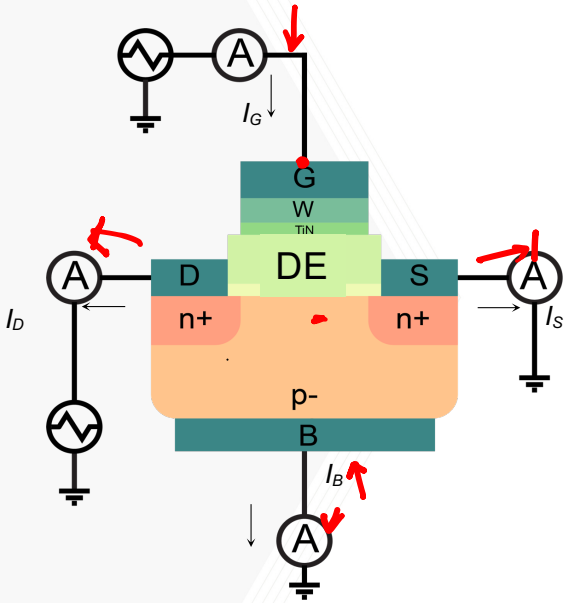
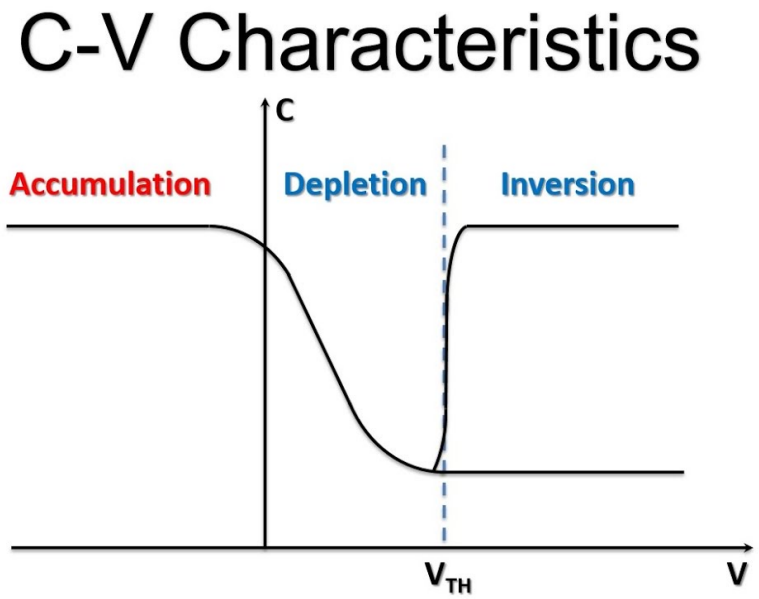
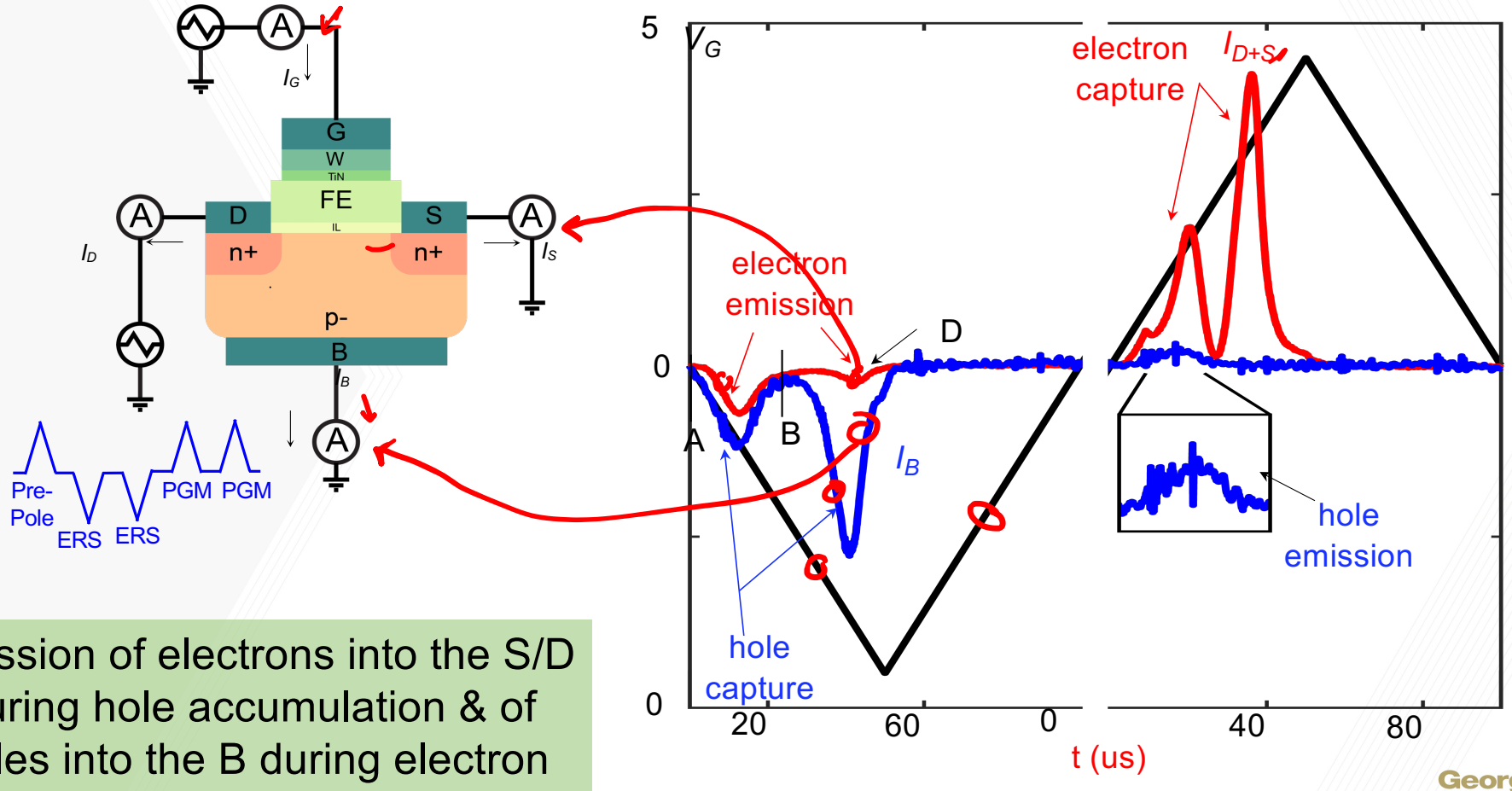
Carrier dynamics in a standard MOSFET





Inversion charge flows through the source and drain terminals.
Accumulation charge flows through the body terminal.

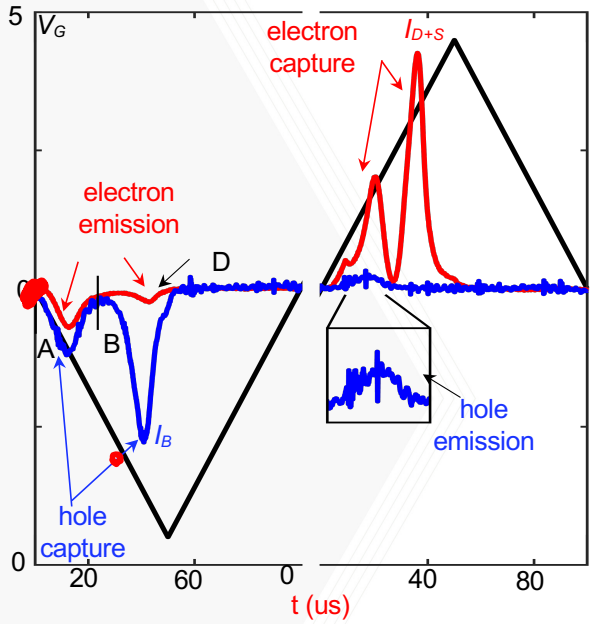
Trap emission & capture during write in FEFET



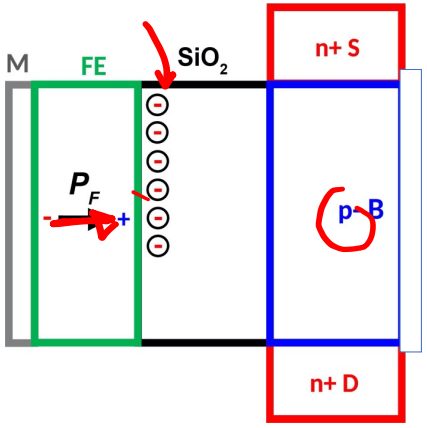
Emission of electrons into the S/D during hole accumulation & of holes into the B during electron inversion

Tasneem et al. IEDM 2021.

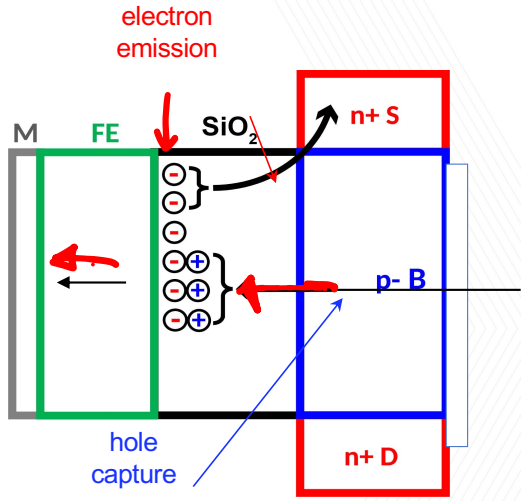
Trap emission & capture during write



A: V_G=0
Programmed state



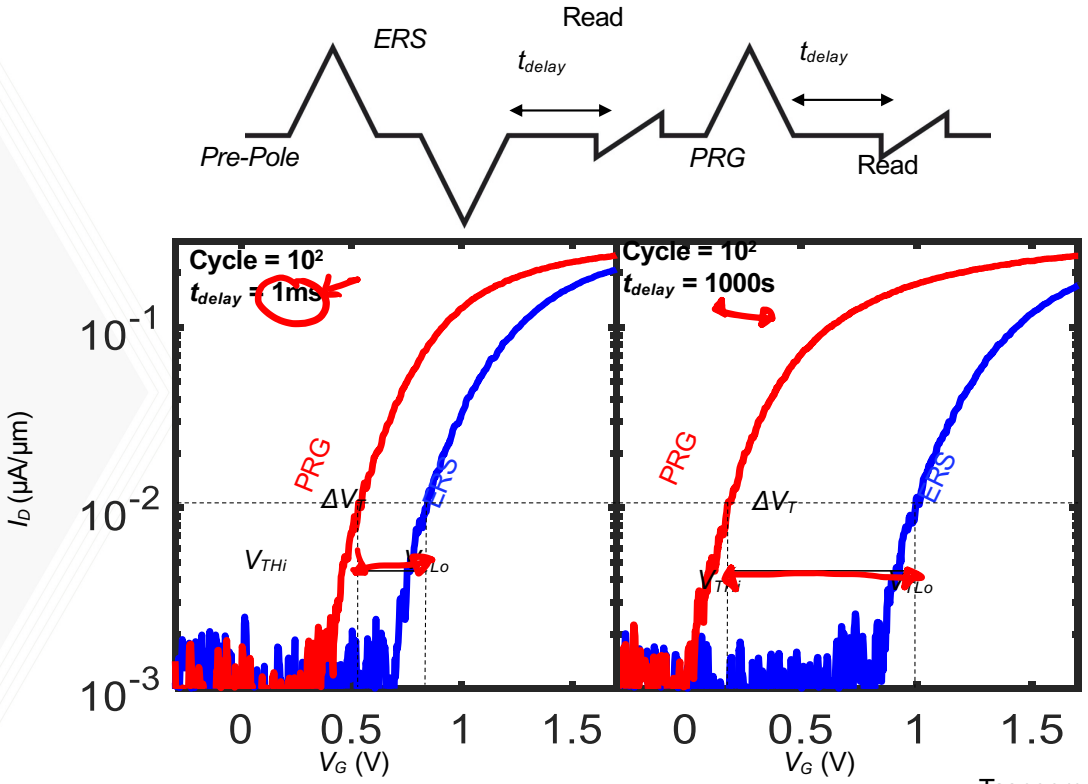
A→B: V_G=-2.3 V



Tasneem et al. IEDM 2021.

Emission of electrons into the S/D during hole accumulation & of holes into the B during electron inversion

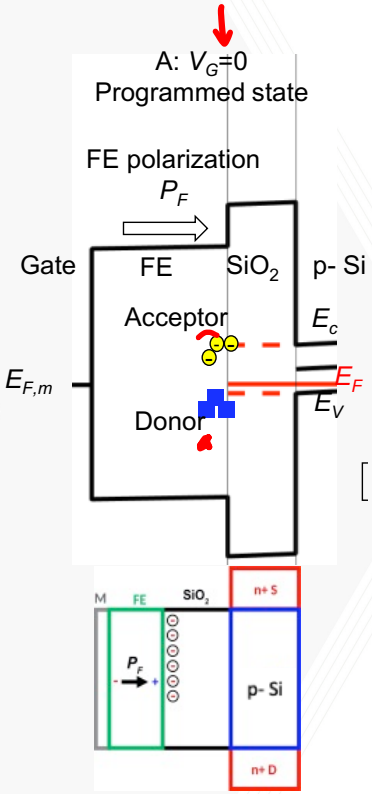
Delay for read after write



Tasneem et al. IEDM 2021.

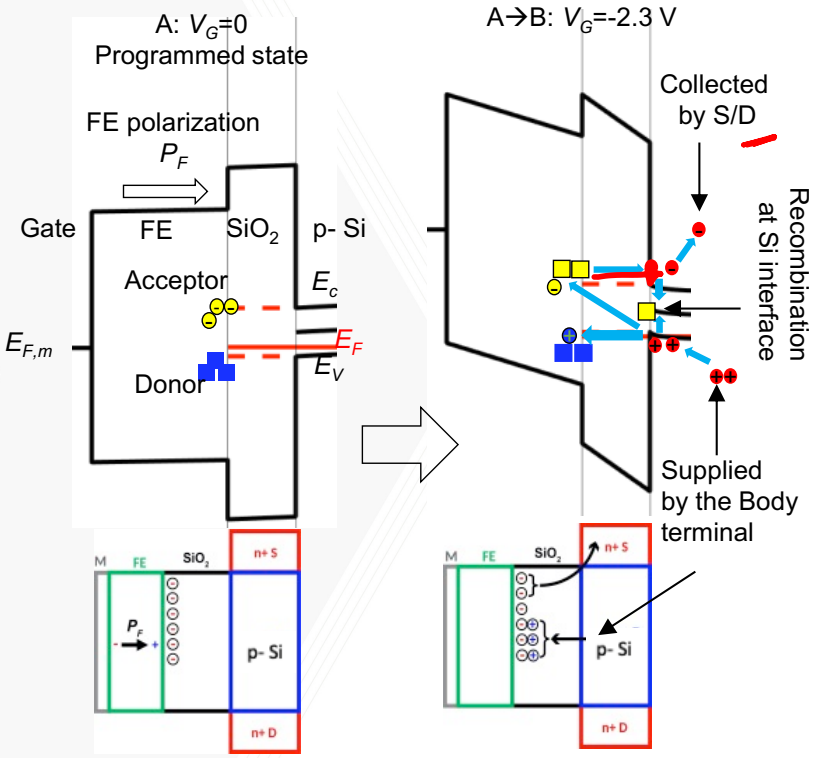
Typical read delay in n-type Si FEFETs are 100 us-1 ms.

Proposed trap locations



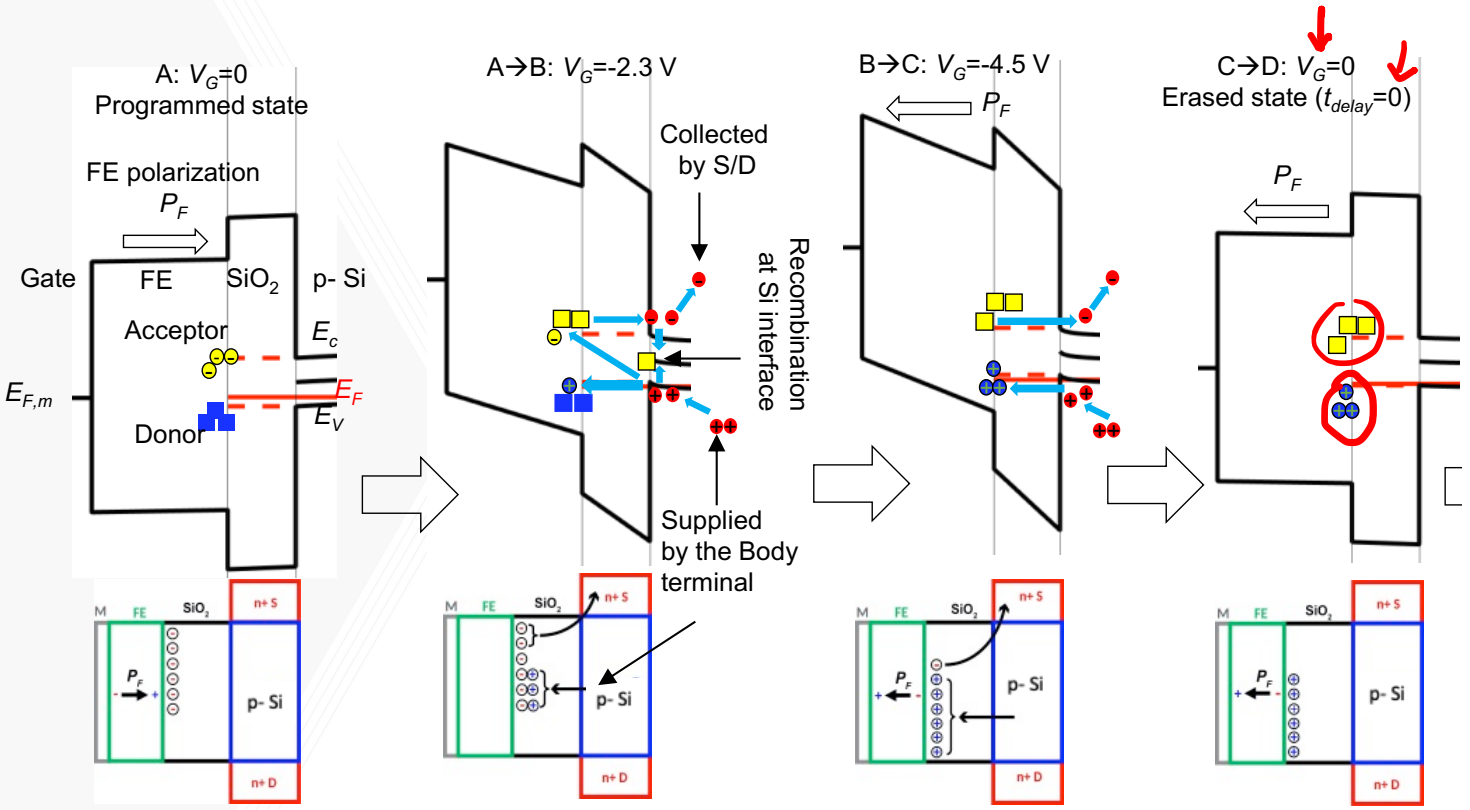
Tasneem et al. IEDM 2021.

Proposed trap locations



Tasneem et al. IEDM 2021.

Proposed trap locations



Tasneem et al. IEDM 2021.

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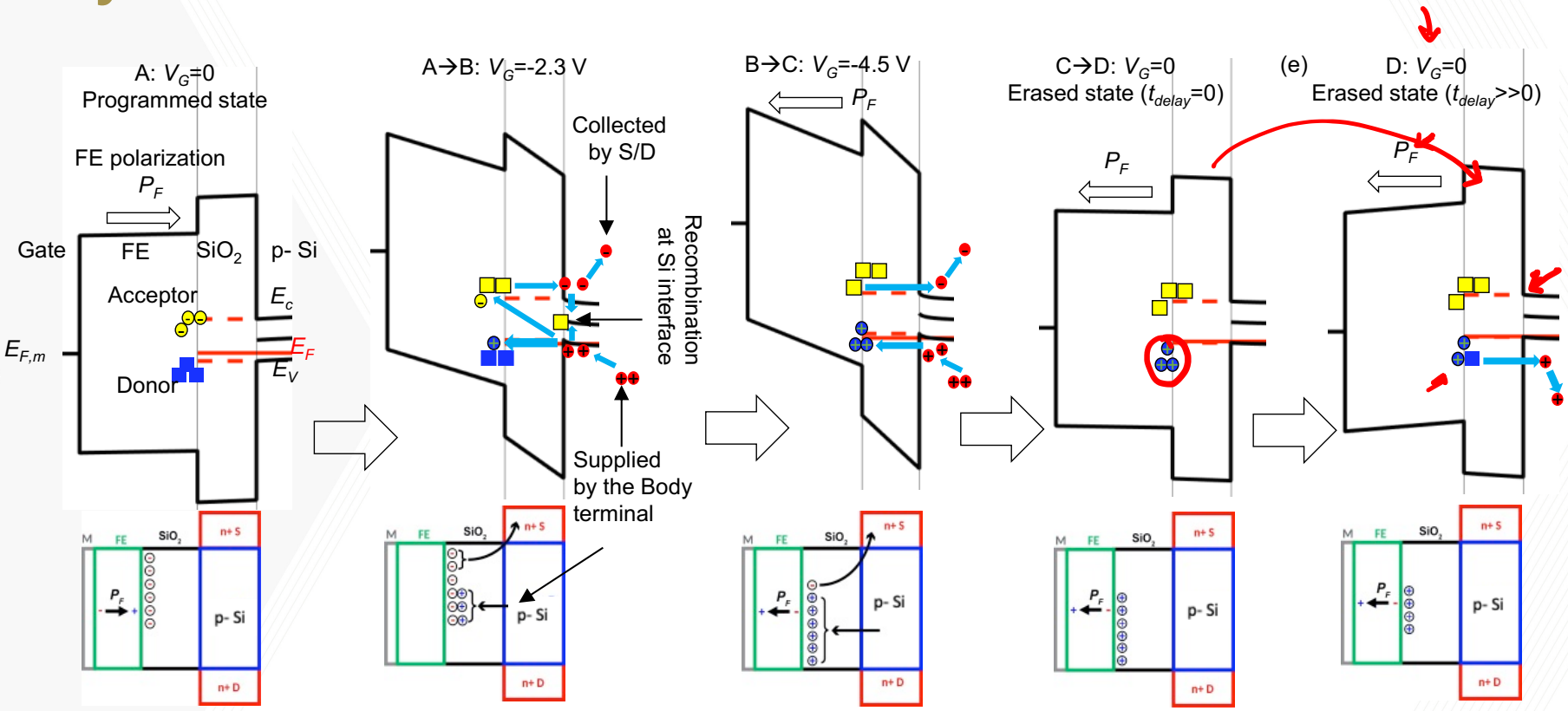
Delay for read after write



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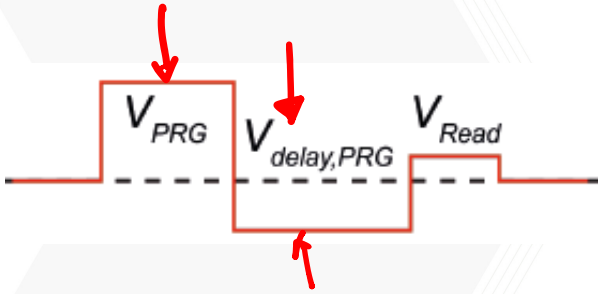
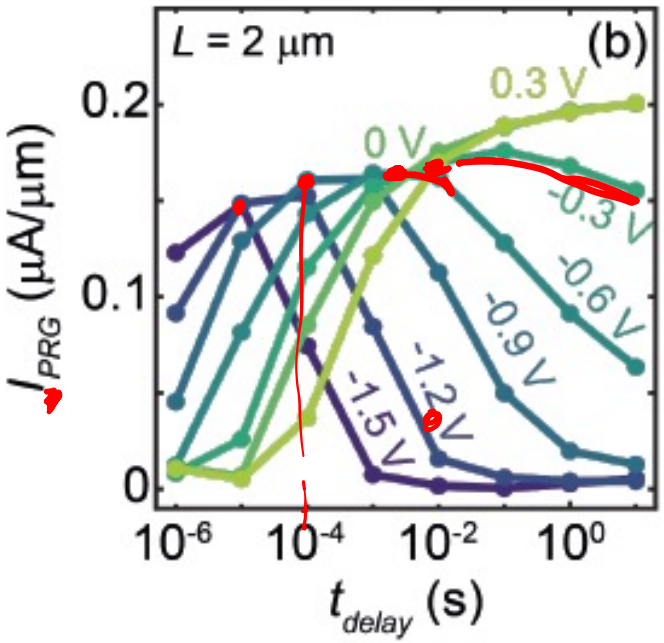
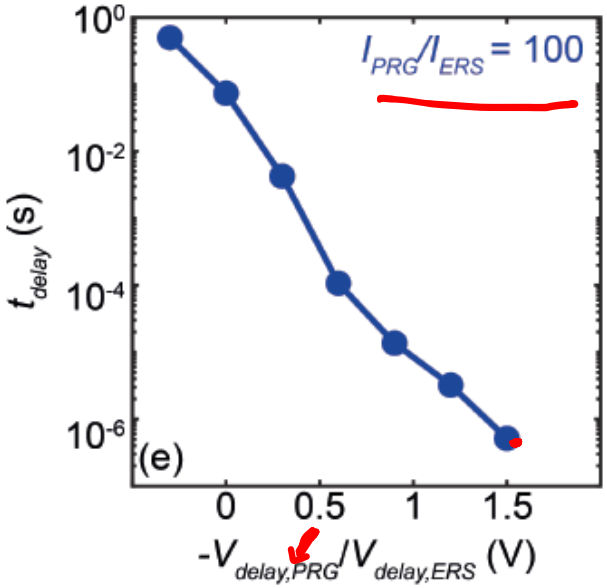
Accelerating Read after write delay



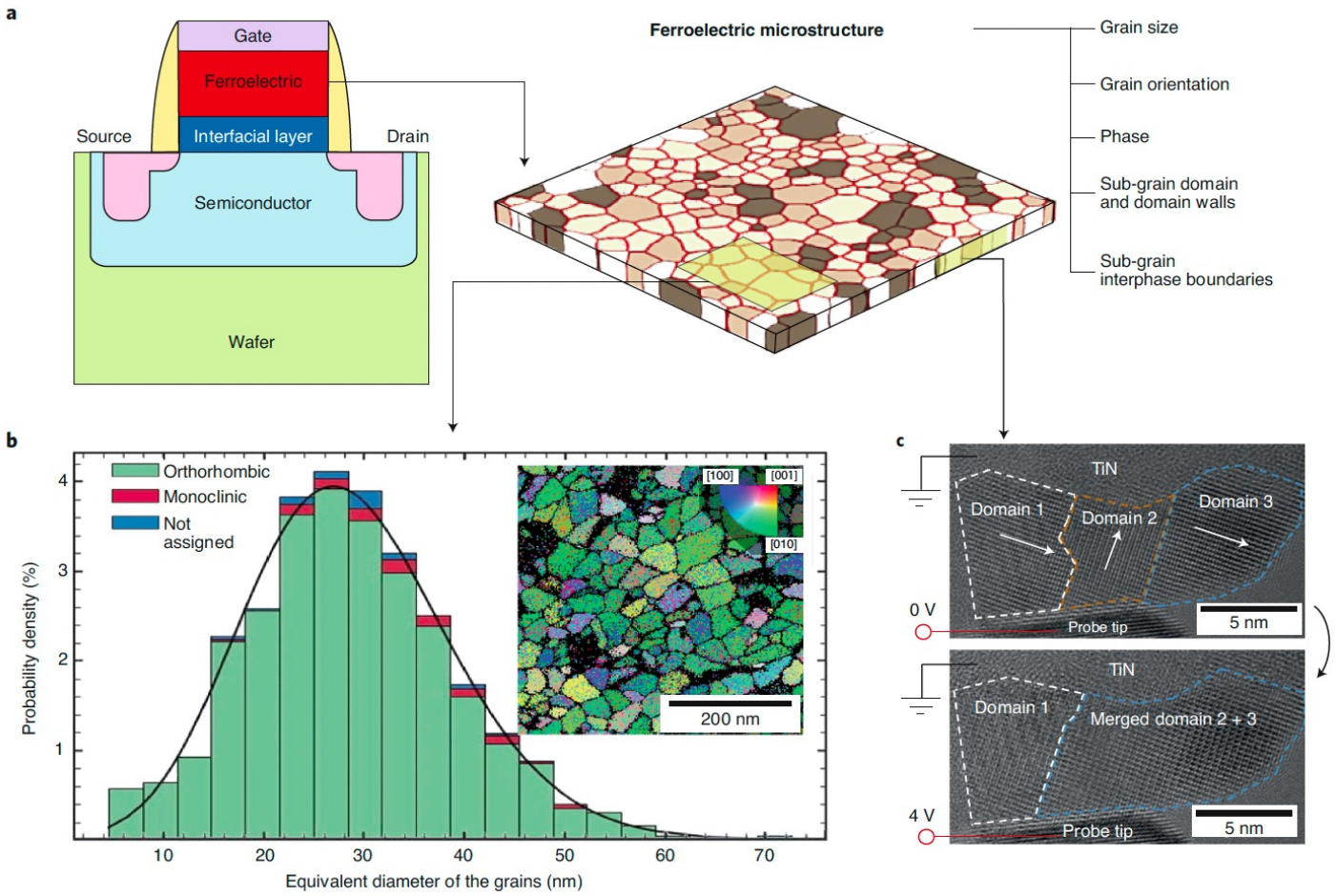




Wang et al. IEDM 2021.

Delay for read after write can be decreased to ~400 ns from 1 ms appropriate pulse engineering.

Microstructure in FEFET



Khan, Keshavarzi, Datta, "The future of ferroelectric field-effect transistor technology", Nature Electronics 2020

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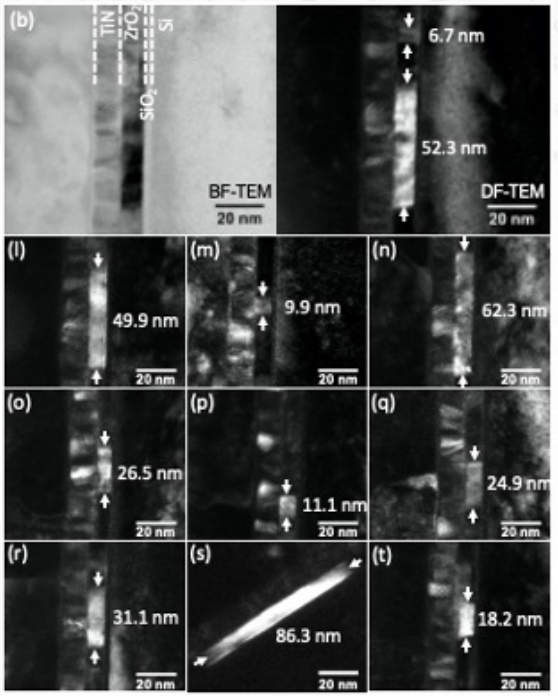
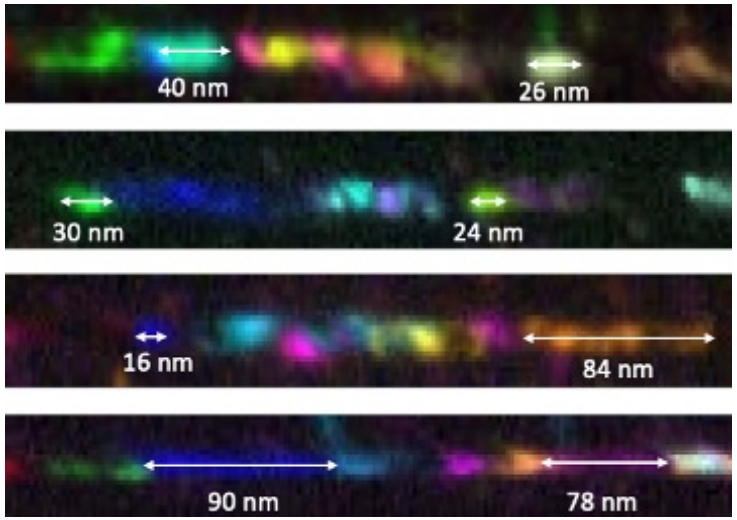
Quantification of microstructure

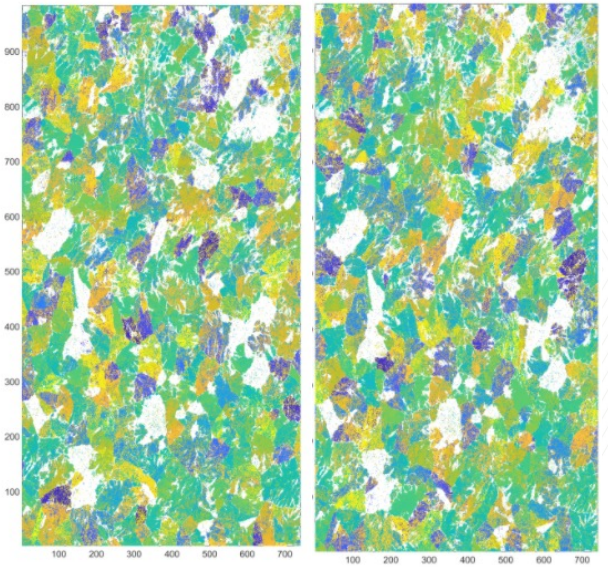
Dark field TEM



Nano-Beam Electron Diffraction (NBED)



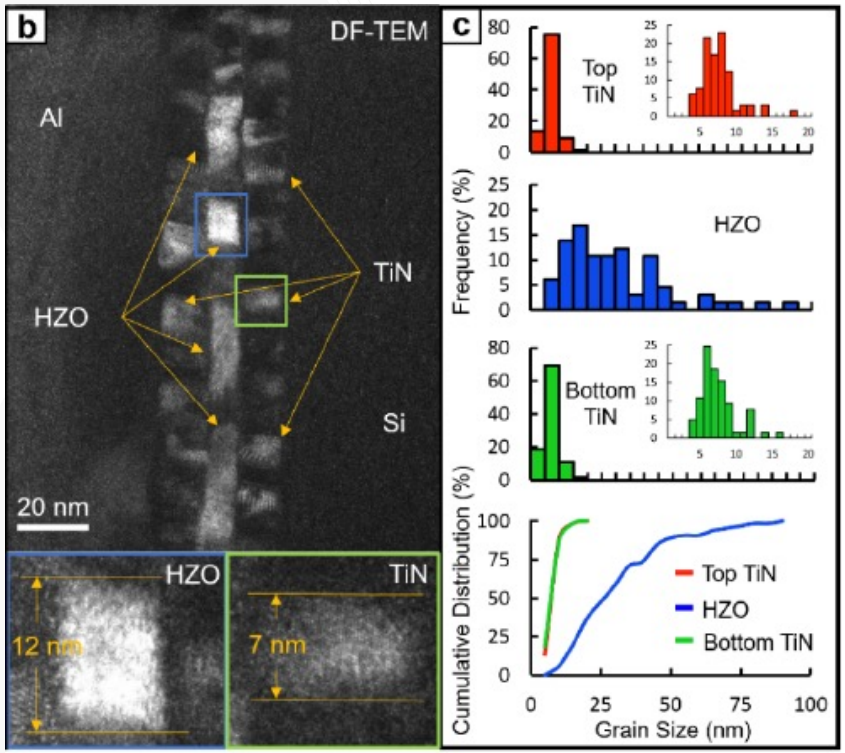
Transmission Kikuchi Diffraction (TKD)



Lombardo, S. F., et al. "Local epitaxial-like templating effects and grain size distribution in atomic layer deposited Hf0. 5Zr0. 5O2 thin film ferroelectric capacitors." *Applied Physics Letters* 119.9 (2021): 092901.

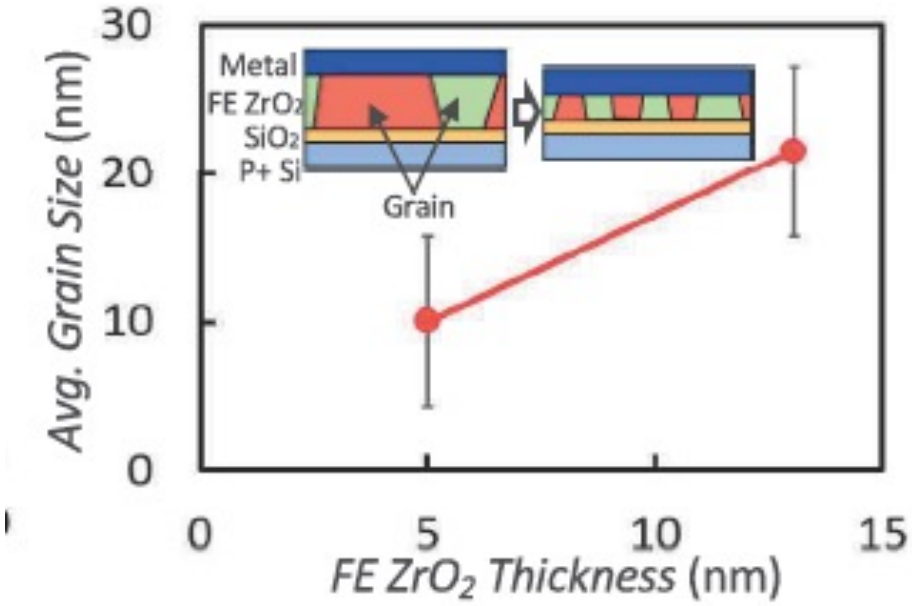
Impact of FE thickness on grain size

FE MIM: TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN



Lombardo et al. APL 2021.

FE MOS: TiN/FE ZrO_2/SiO_2/Si

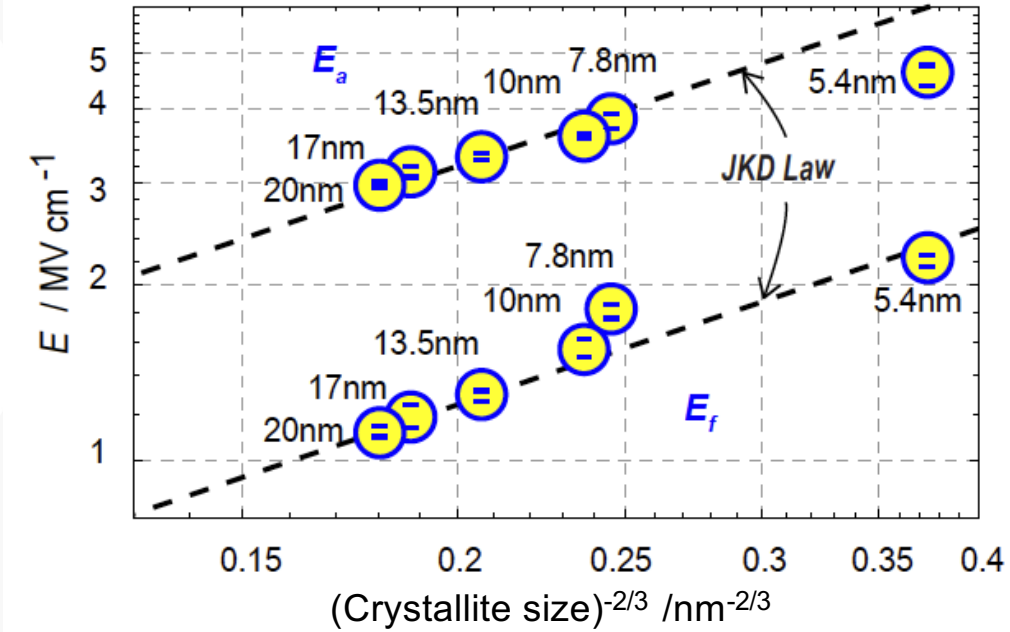


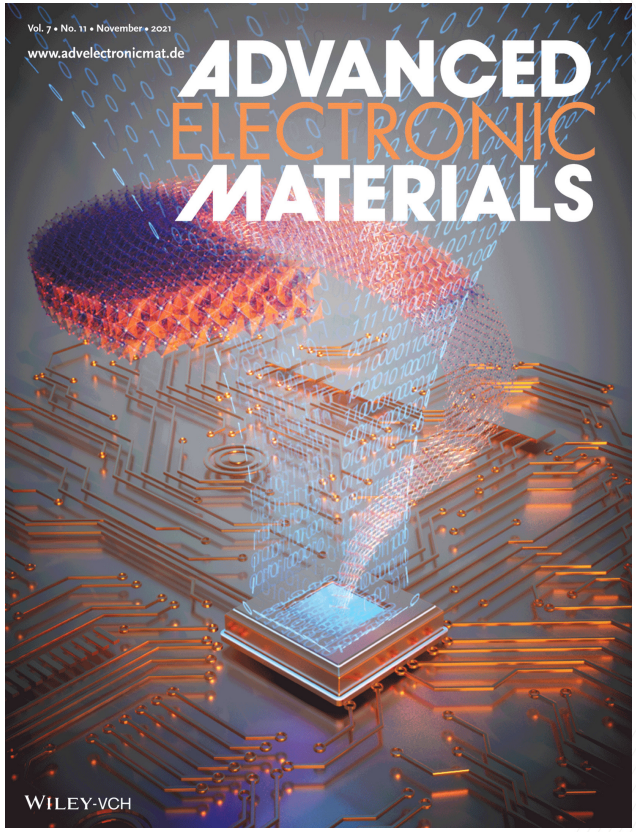
Grain size reduces from 20+nm to 10 nm as FE thickness is reduced from 10 nm to 5 nm

Functional response and microstructure

Modified Jannovec-Kay-Dunn law for ZrO_2

Critical field ∝ (crystallite size)$^{-2/3}$

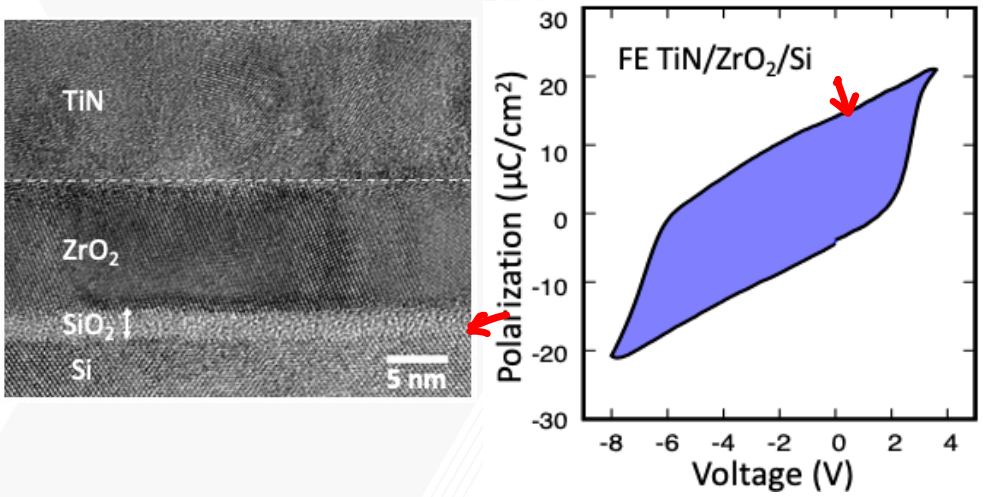




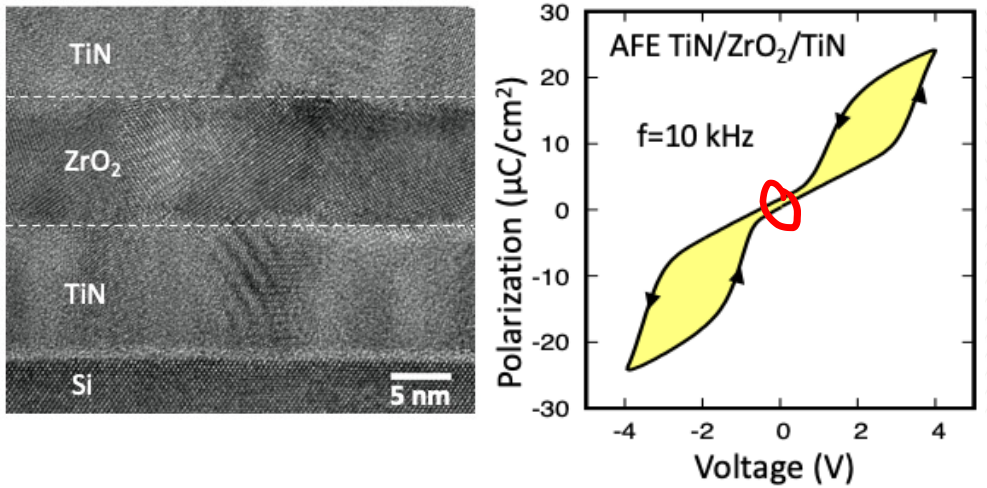
Tasneem *et al.* "A Janovec-Kay-Dunn-like behavior at thickness scaling in ultra-thin antiferroelectric ZrO_2 films." Advanced Electronic Materials, 7, 2100485 (2021).

Impact of substrate on Ferroelectricity and Antiferroelectricity in ZrO_2

Ferroelectricity in MIS



Antiferroelecticity in MIM



ZrO_2 becomes ferroelectric on SiO_2/Si which otherwise is AFE on TiN

Chae, Lombardo et al. (under review)

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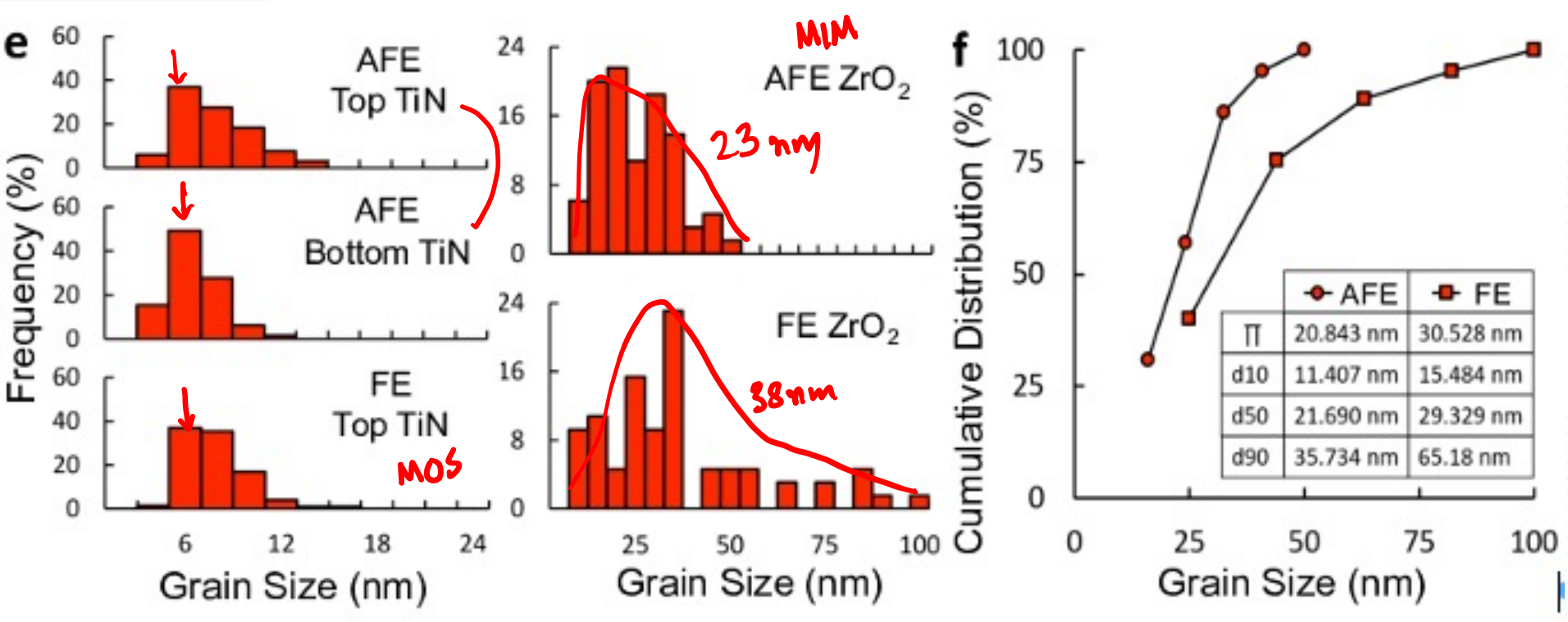
Microstructure (DF-TEM) of AFE and FE ZrO_2



TiN grain size: ~8 nm

Chae, Lombardo et al. (under review)

FE ZrO_2: Grain size =38 nm

AFE ZrO_2: Grain size =23 nm

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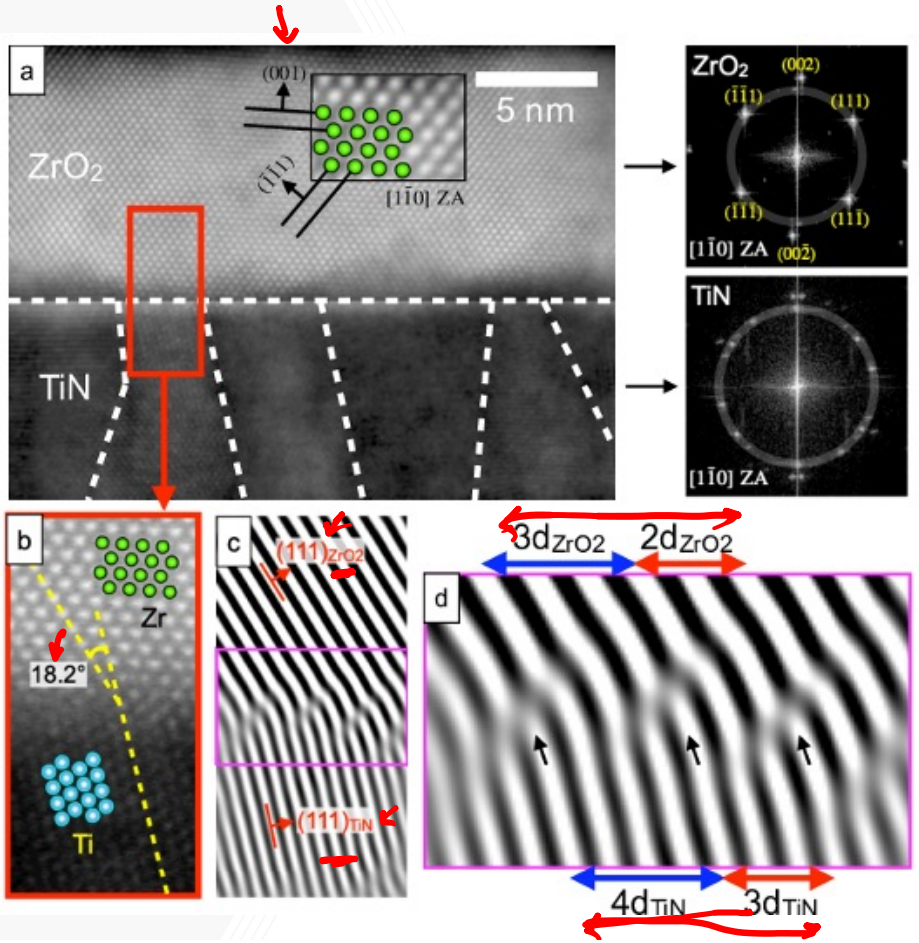
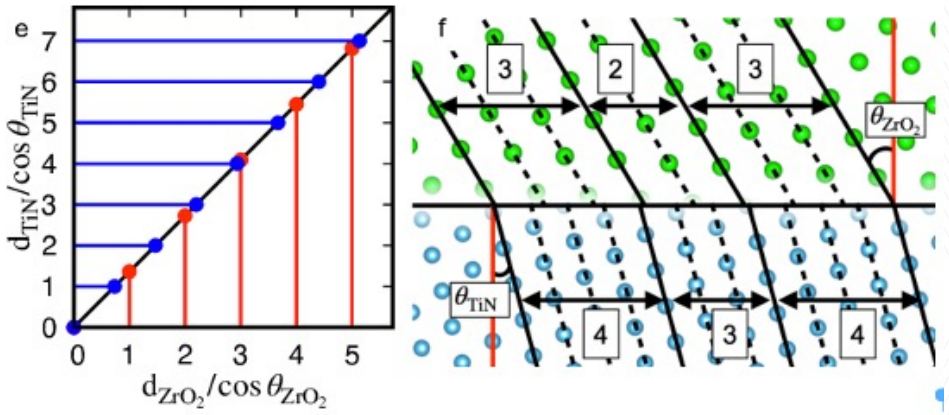
Local "Epitaxy" in ZrO_2 in MOS and MIM Structures





Evidence of near-coincident site epitaxy from both top and bottom TiN

Chae, Lombardo et al. (under review)

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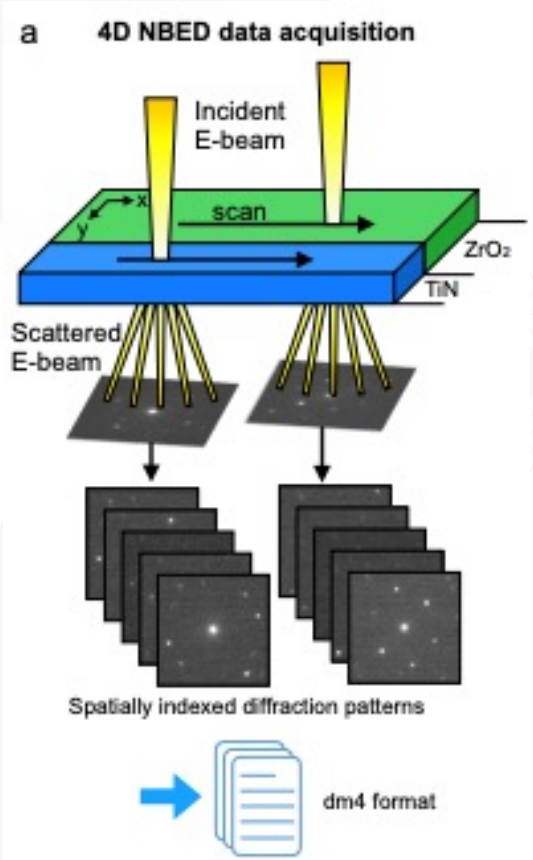
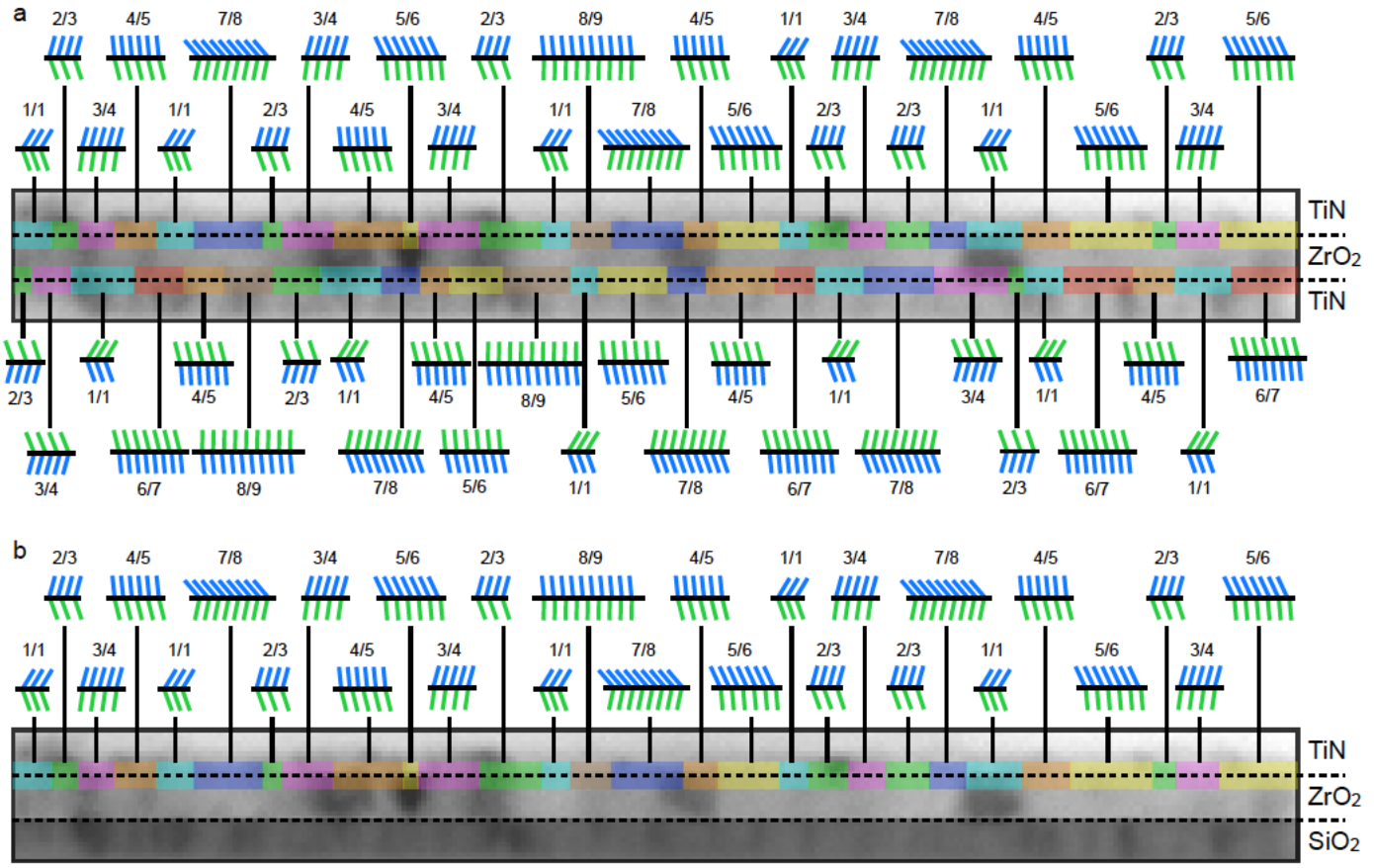
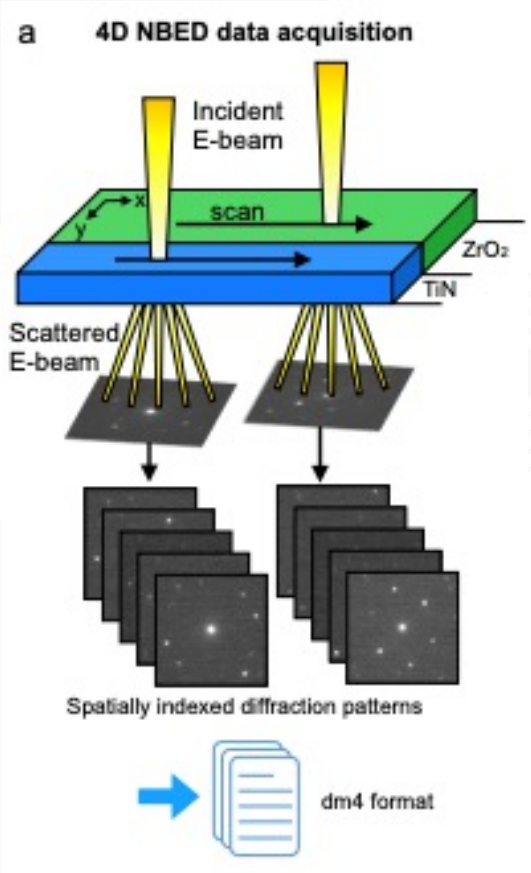
Local Epitaxy in ZrO_2 in MOS and MIM Structures



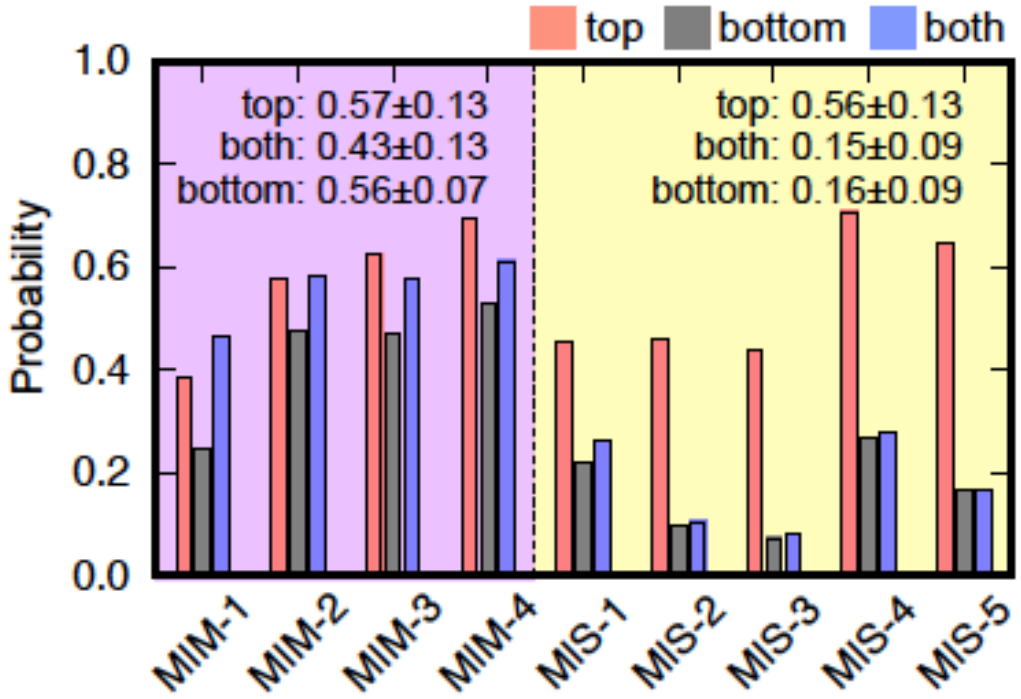


Chae, Lombardo et al. (under review)

Local Epitaxy in ZrO_2 in MOS and MIS Structures



Lombardo and Chae



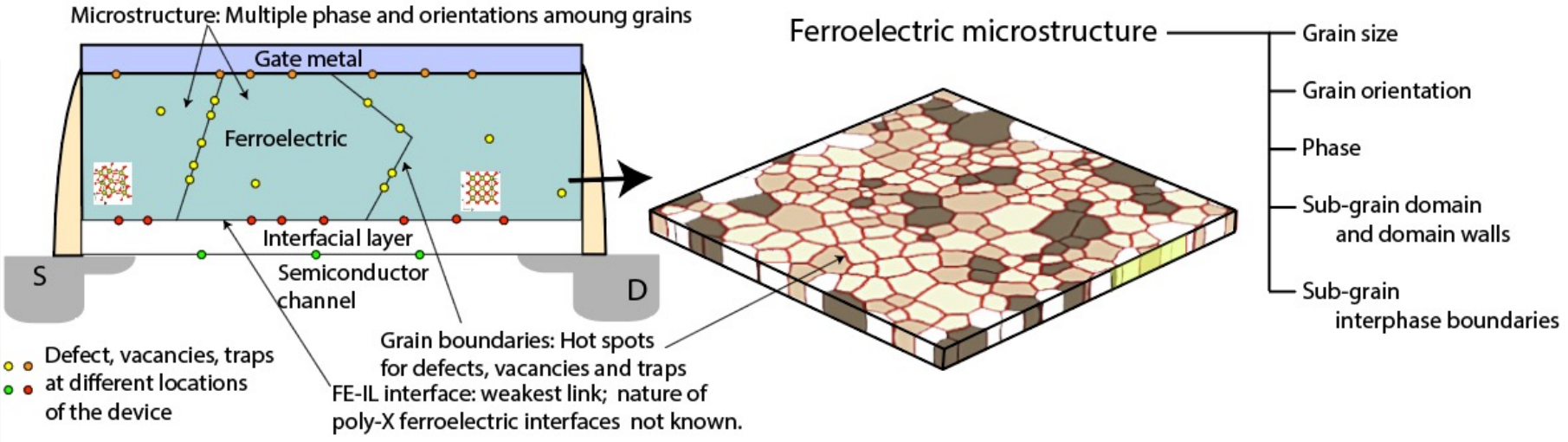
Same probability of epitaxy with top electrode for both FE and AFE ZrO_2.

Progress in FEFET Technology

Device physics

Trap dynamics

Microstructure



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