Negative Capacitance for Ultra-low Power Computing:

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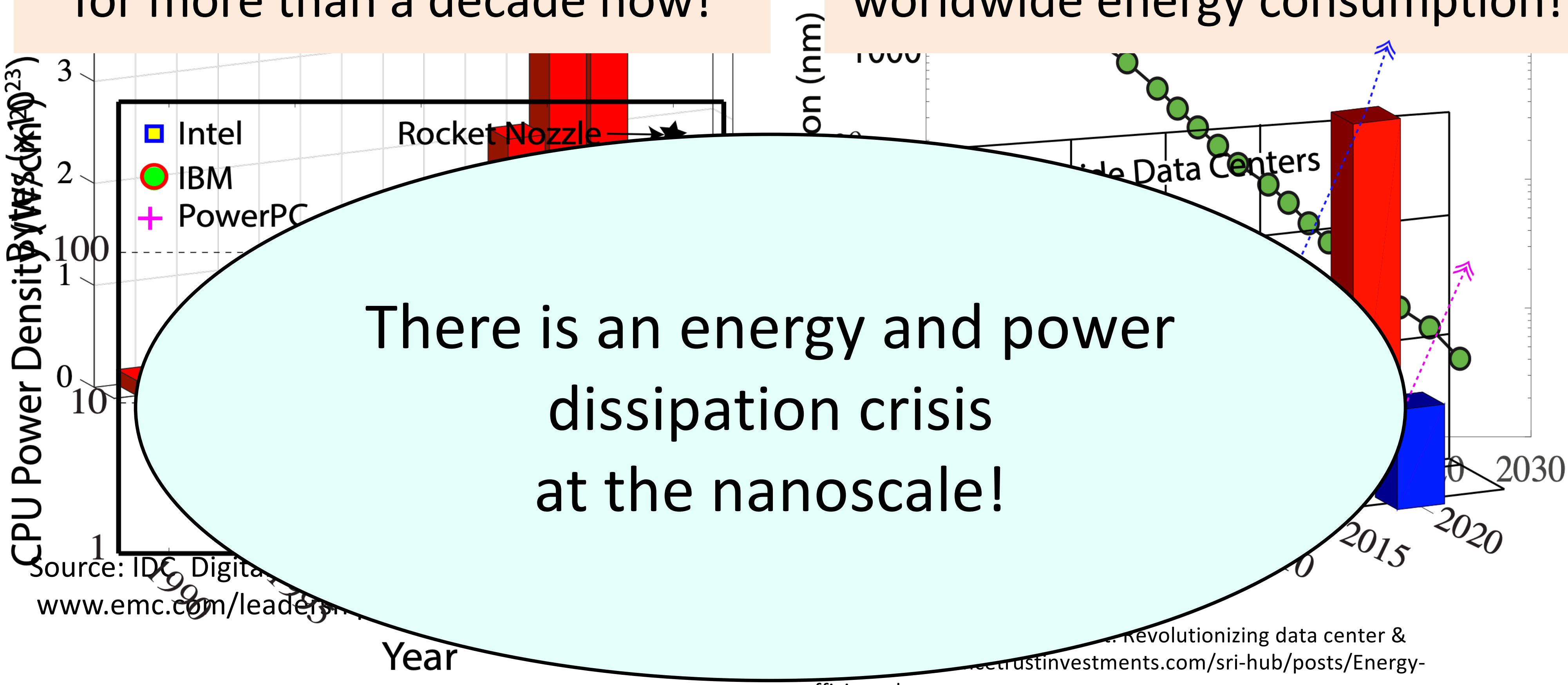
Computing and Global Challenges

Computable data grows 50x every ten year!

Extreme scaling has been the driver!

Clock frequency stuck at 3 GHz for more than a decade now!

Computing constitutes 2-5% of worldwide energy consumption!



There is an energy and power dissipation crisis at the nanoscale!

Adapted from: Danowitz et al. Comm. of ACM 55.1 (2012).

...Revolutionizing data center & ...etrustinvestments.com/sri-hub/posts/Energy-efficient-data-centres

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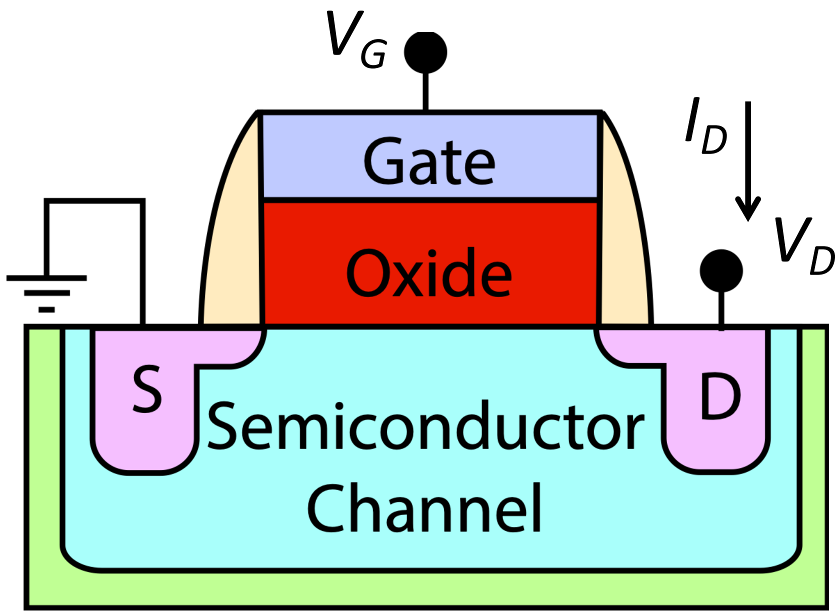
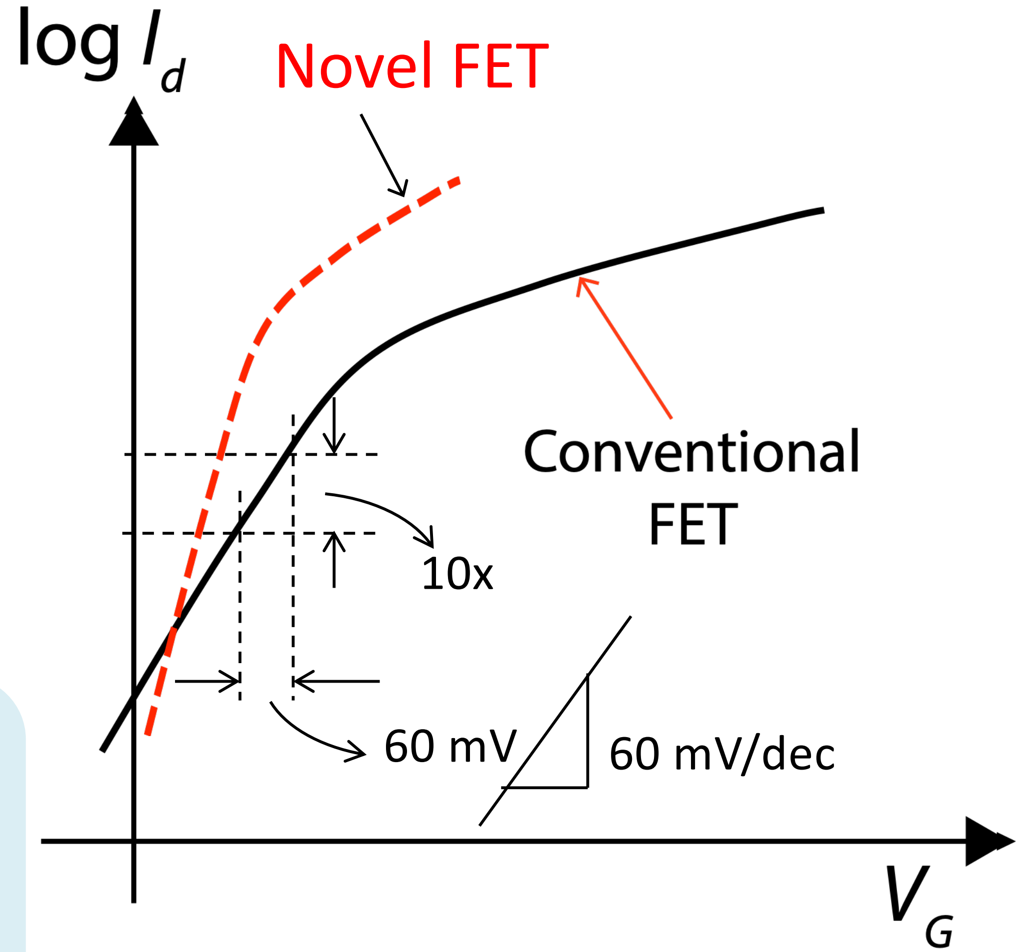
Energy Challenge in Computing





Boltzmann distribution dictates that Channel charge, $Q \propto e^{\frac{q\psi_s}{k_B T}}$

Minimum Subthreshold Swing

$$S_{\min} = \frac{k_B T}{q} \log_e(10)$$

$$= 60mV / dec$$

We are in search of an Ultra-low Power MOSFET!

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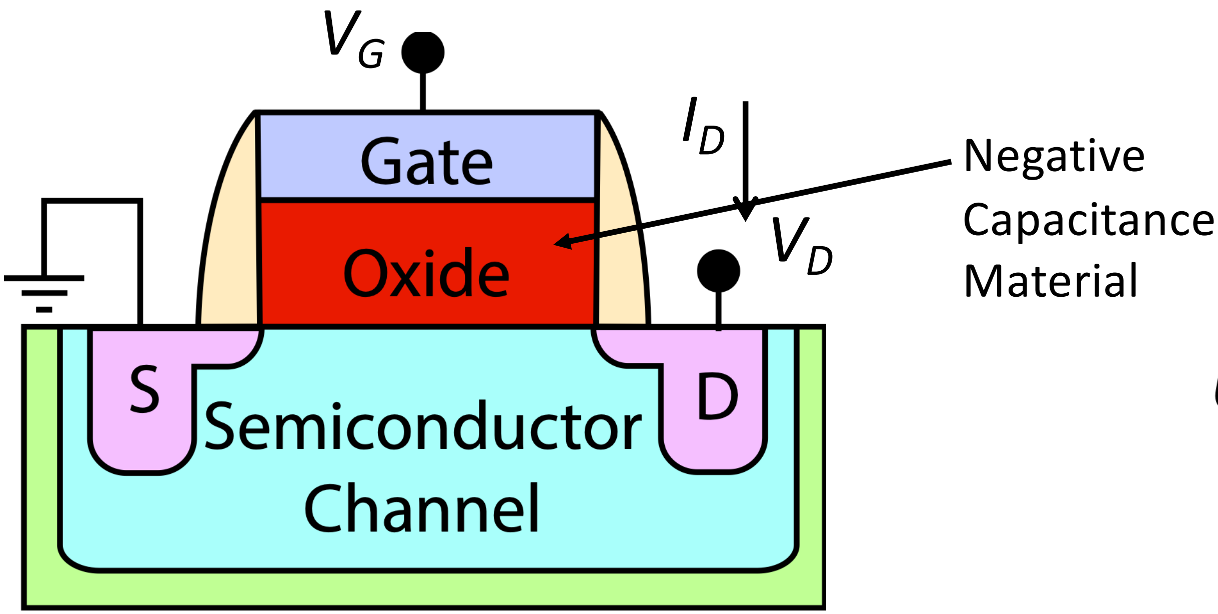
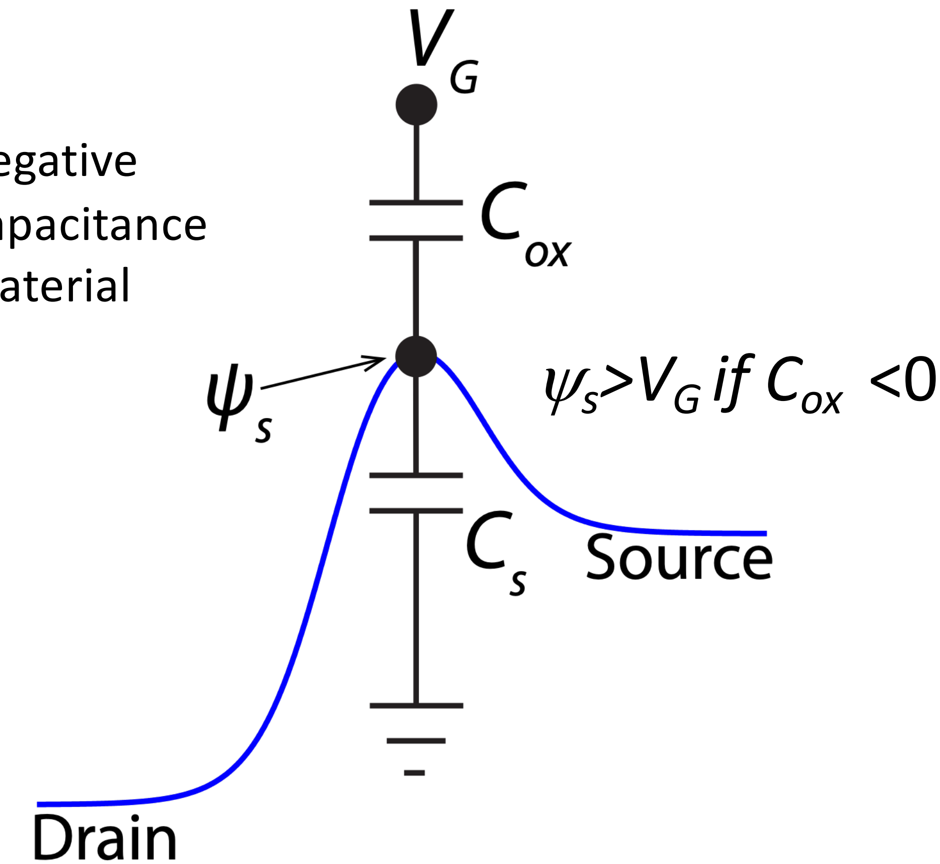
The Negative Capacitance Approach





Subthreshold Swing

$$S = \frac{\partial V_G}{\partial(\log_{10} I_D)}$$

$$= \underbrace{\frac{\partial V_G}{\partial \psi_s}}_{\equiv \mathrm{m}} \frac{\partial \psi_s}{\partial(\log_{10} I_D)}$$

$$= m \times 60 \text{ mV/decade}$$

Body Factor

$$m = \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_s}{C_{ox}}$$

$$m = 1 + \frac{C_s}{C_{ox}} < 1$$ if C_{ox} is negative

Negative capacitance can result in a $S < 60$ mV/decade

Salahuddin et al. Nano Lett. 8, 405 (2008)

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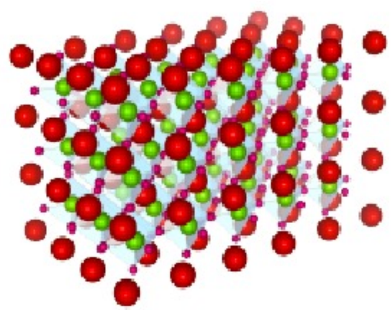
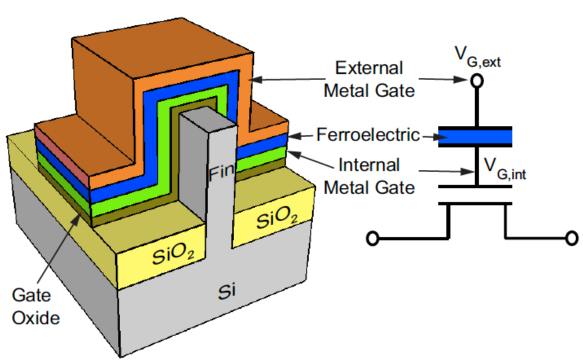
What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors



What do we need to know?

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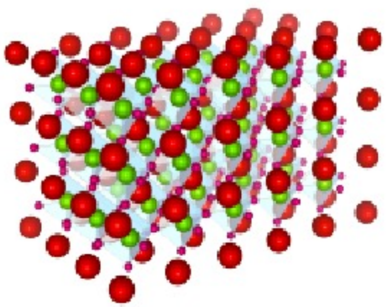
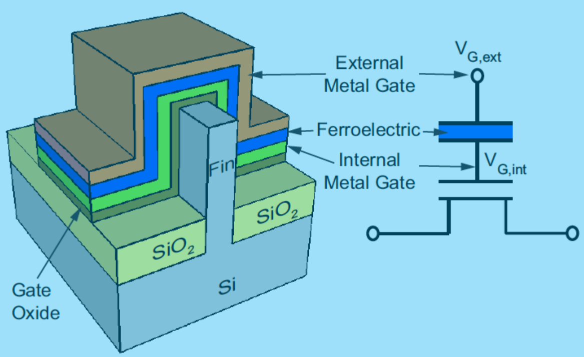
What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors



What do we need to know?

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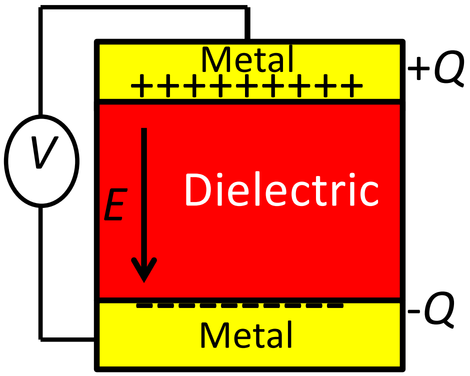
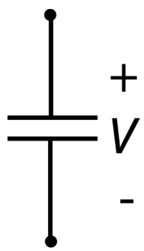
Capacitance: Positive and Negative



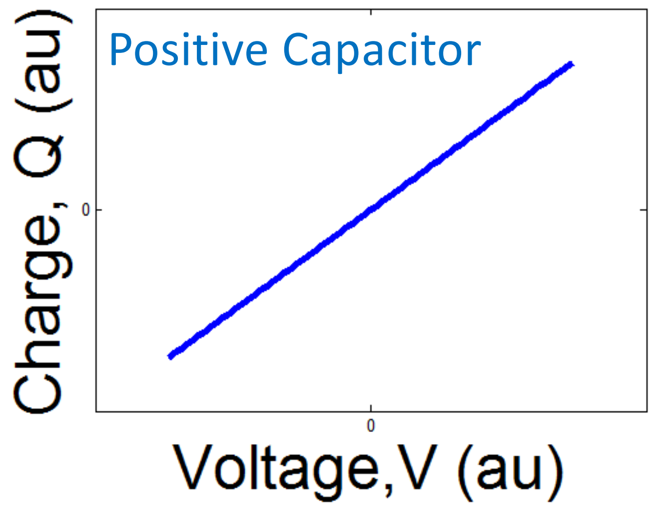


Capacitance $C = \frac{dQ}{dV}$

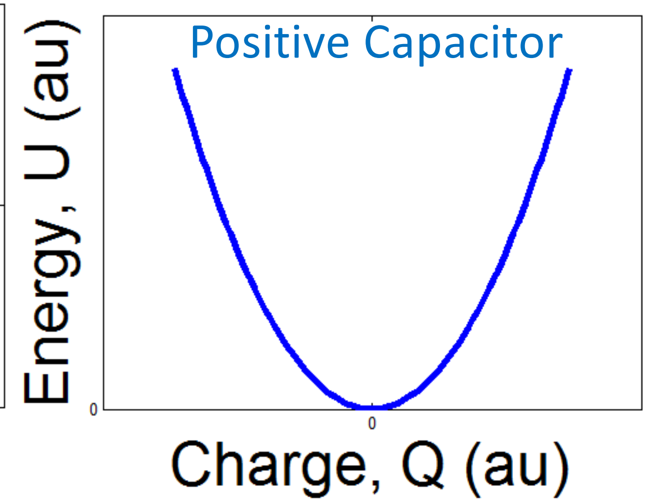
Stored Energy $U = \frac{Q^2}{2C}$

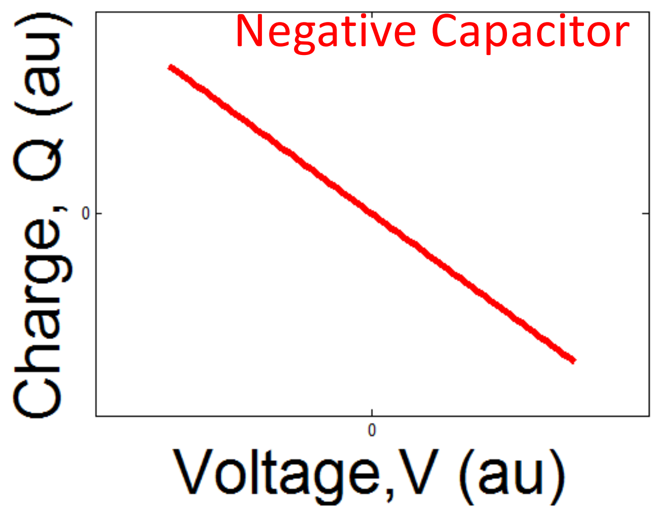
$$C = \left[\frac{d^2U}{dQ^2}\right]^{-1}$$

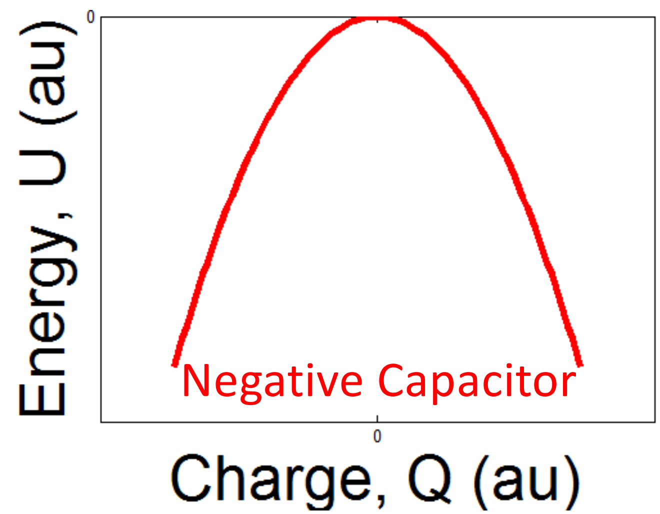
Q-V Characteristics



Q-U Characteristics (Energy Landscape)







C is inverse of radius of curvature of energy landscape

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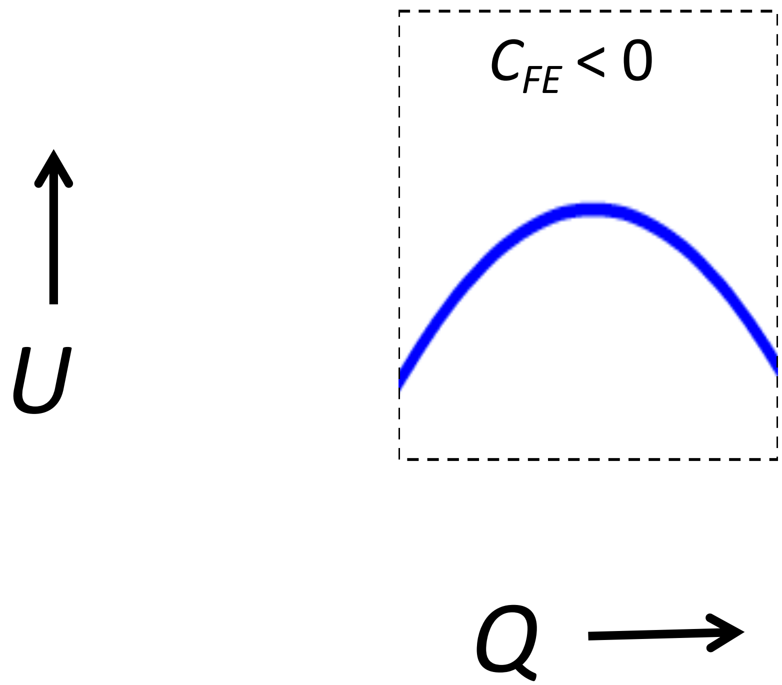
How to get Negative Capacitance Material



Landau Theory of Ferroelectrics

Free energy of a ferroelectric

$$U = \alpha Q^2 + \beta Q^4 + \gamma Q^6; \alpha < 0$$

α, β, γ = Anisotropy Constants
Q = Charge

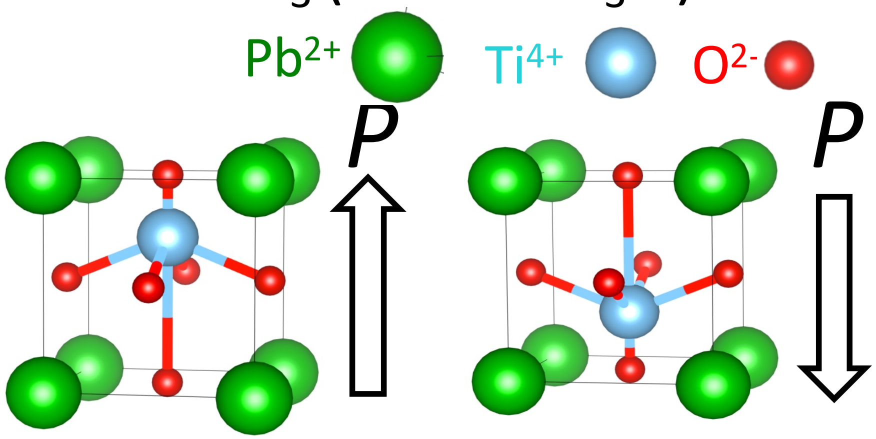
According to the Landau theory of ferroelectric, ferroelectric oxides could give an effective negative capacitance

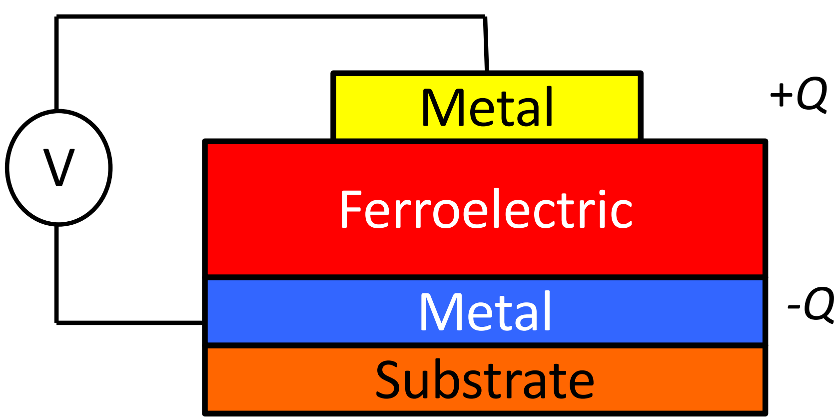
Landau & Khalatnikov. Dokl. Akad. Nauk 96, 85 469472 (1954).

Ferroelectric Oxides

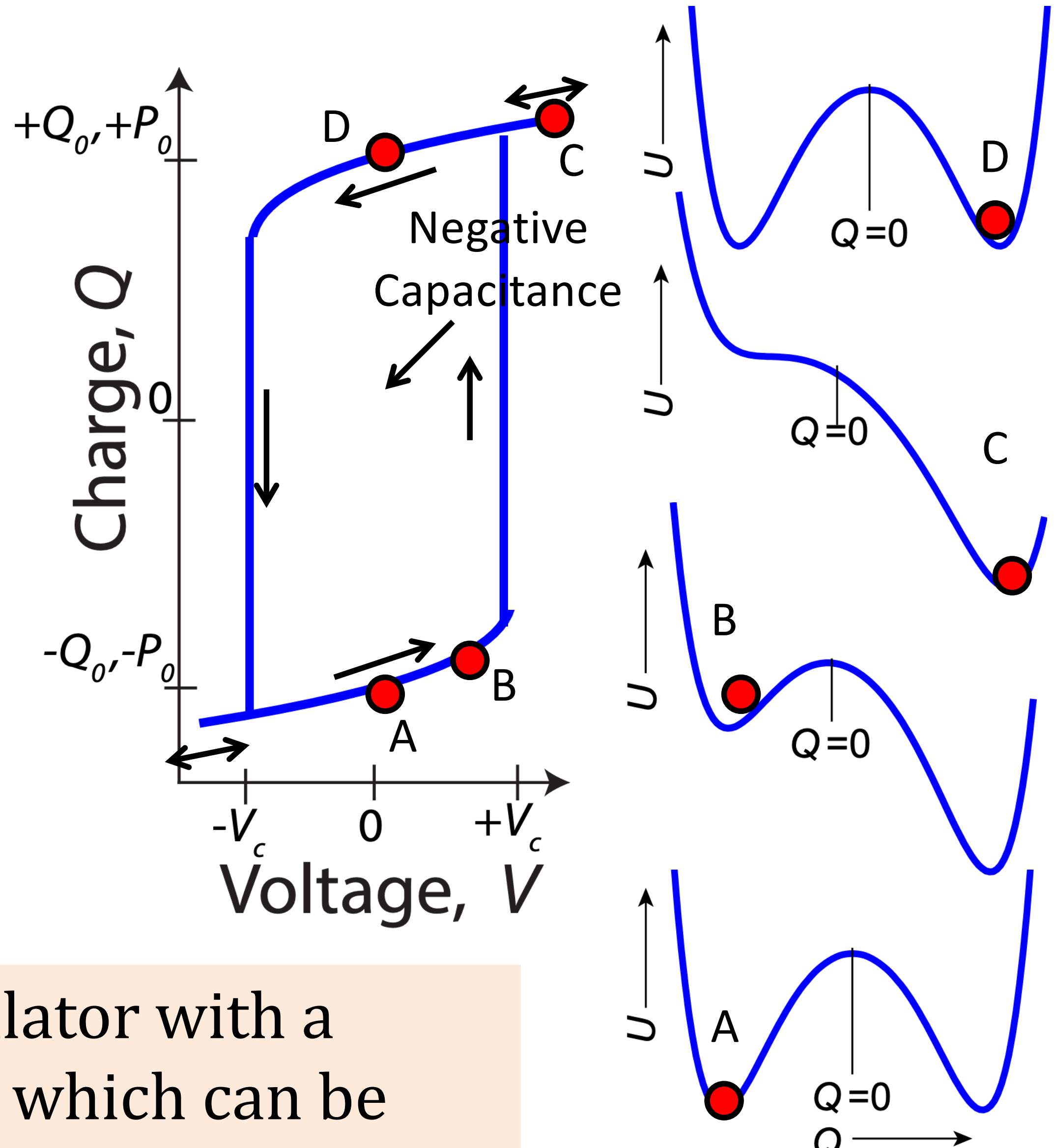
Classical Ferroelectric

$PbTiO_3$ ($Pb^{2+}Ti^{4+}O_3^{6-}$)





Charge Voltage Characteristics



A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercivity voltage .

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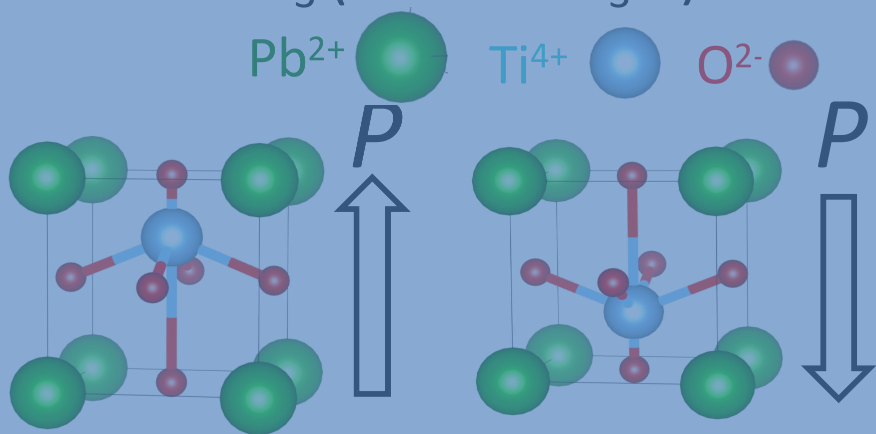

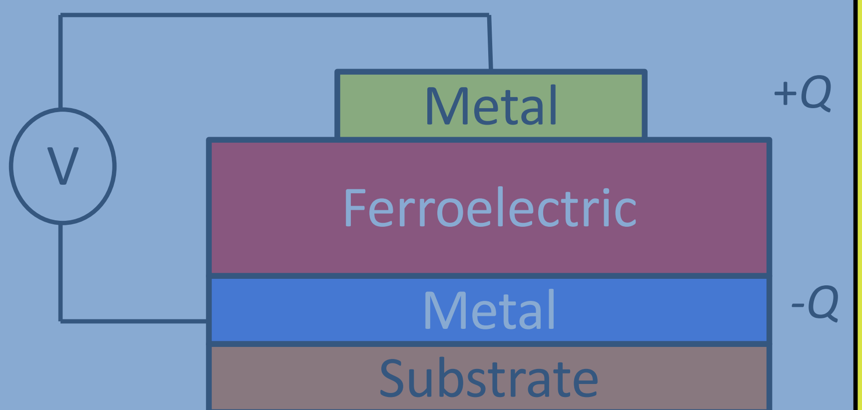

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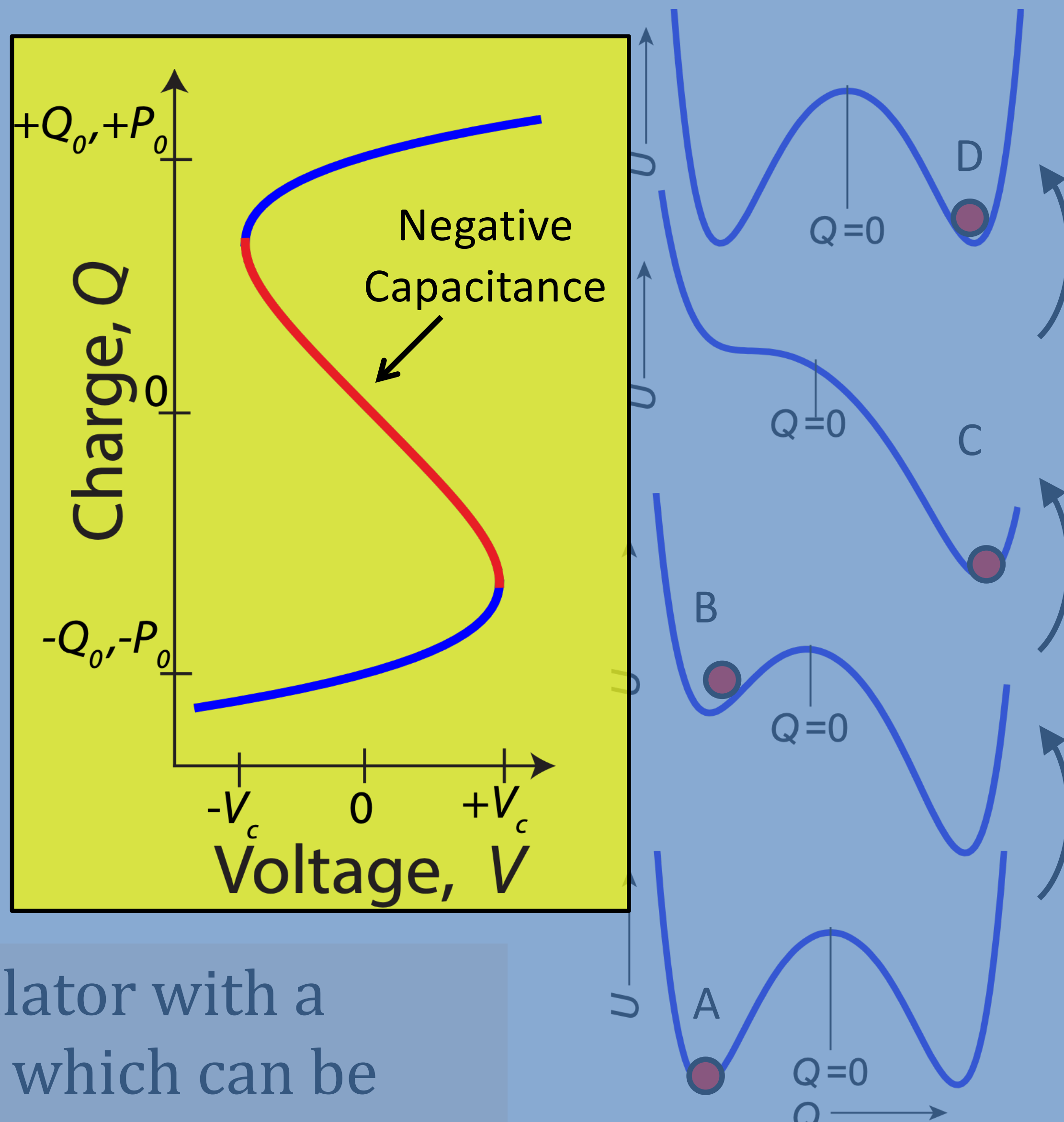

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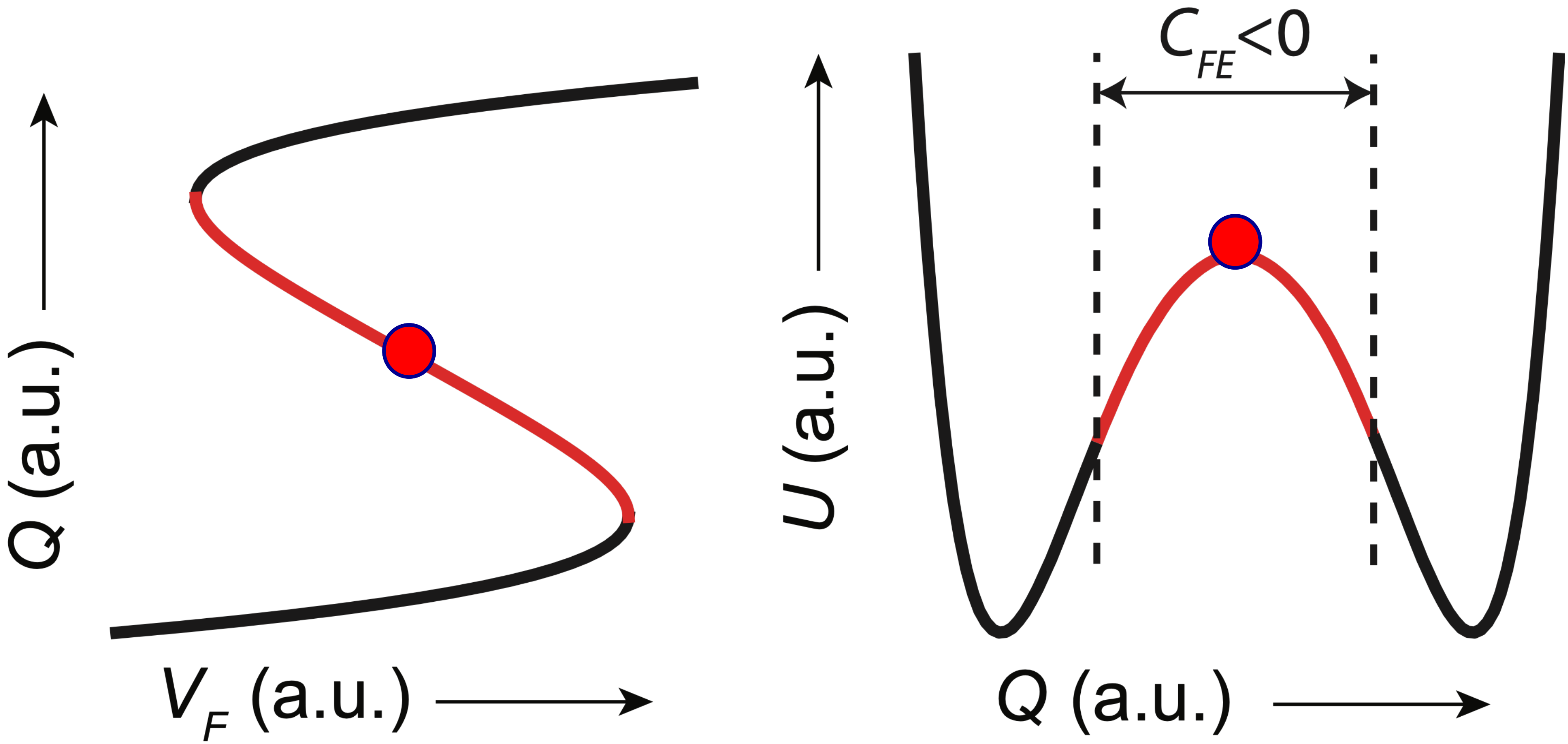
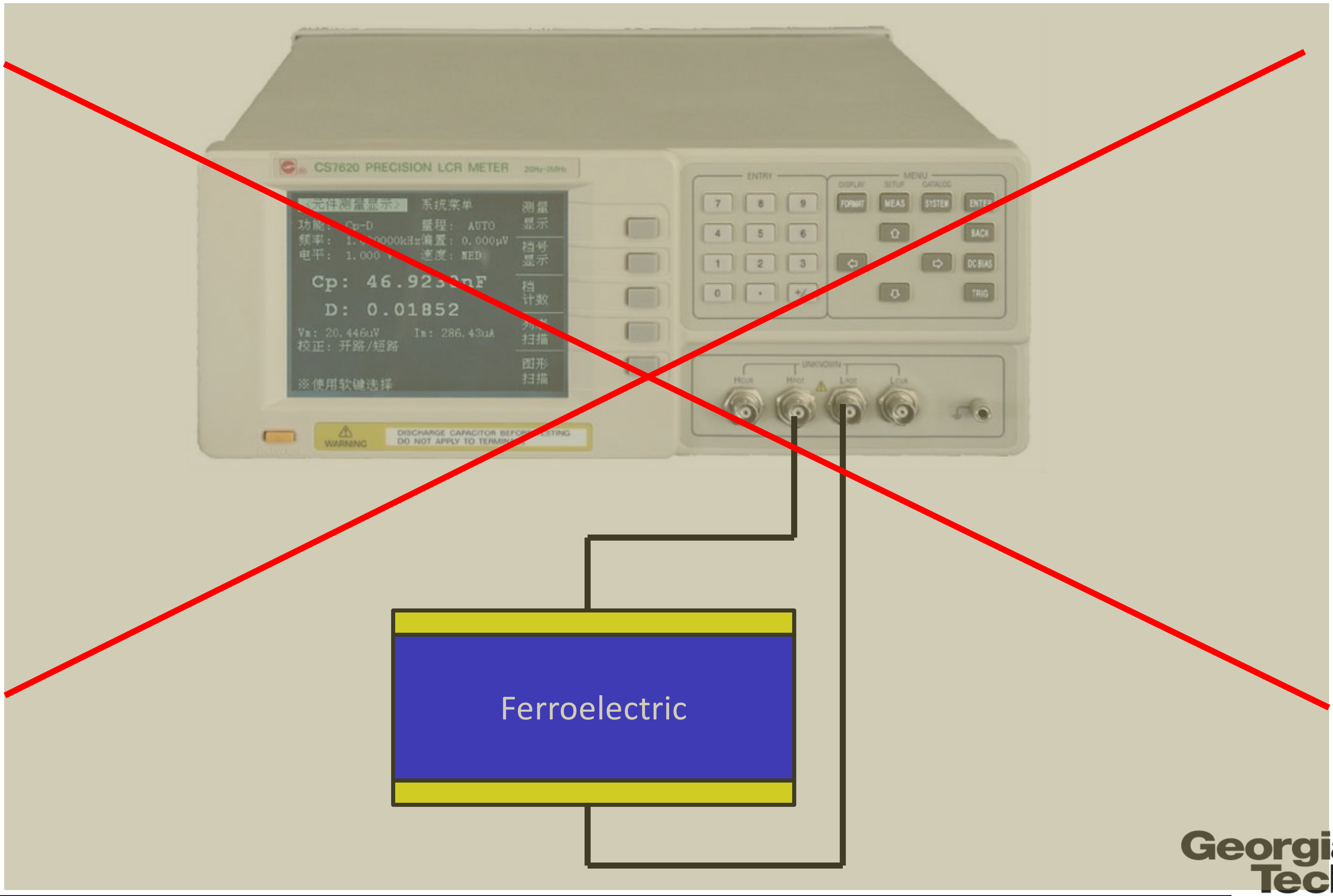
Why is it difficult to measure?

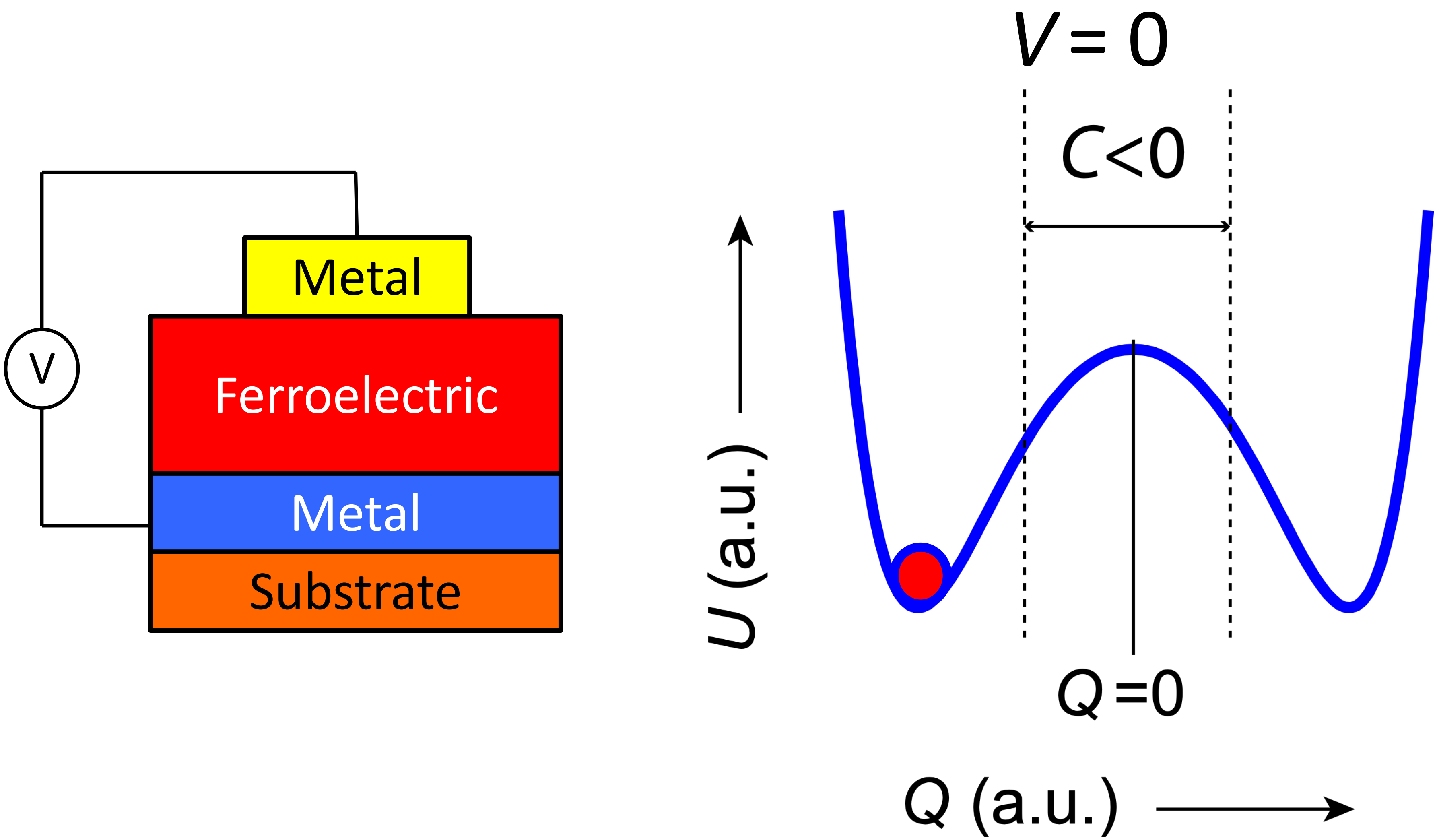


Ferroelectric Negative Capacitance is unstable and cannot be accessed in a time independent equilibrium measurement.

Why is it difficult to measure?



Direct Measurement of Negative Capacitance



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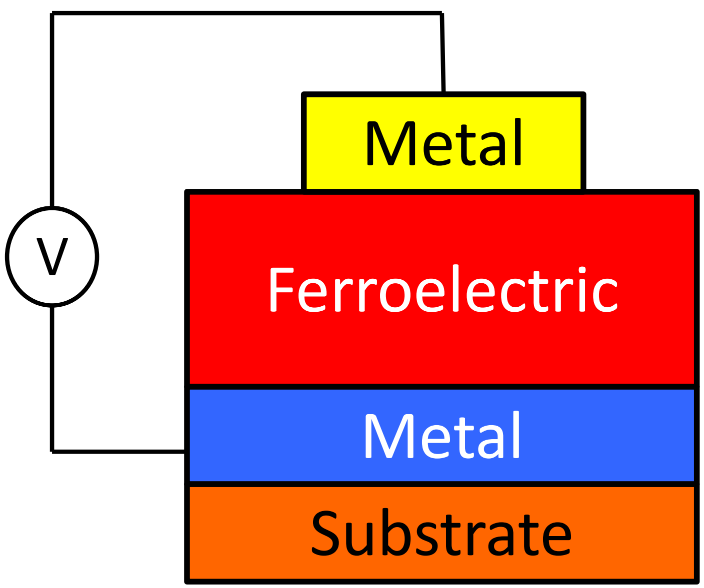
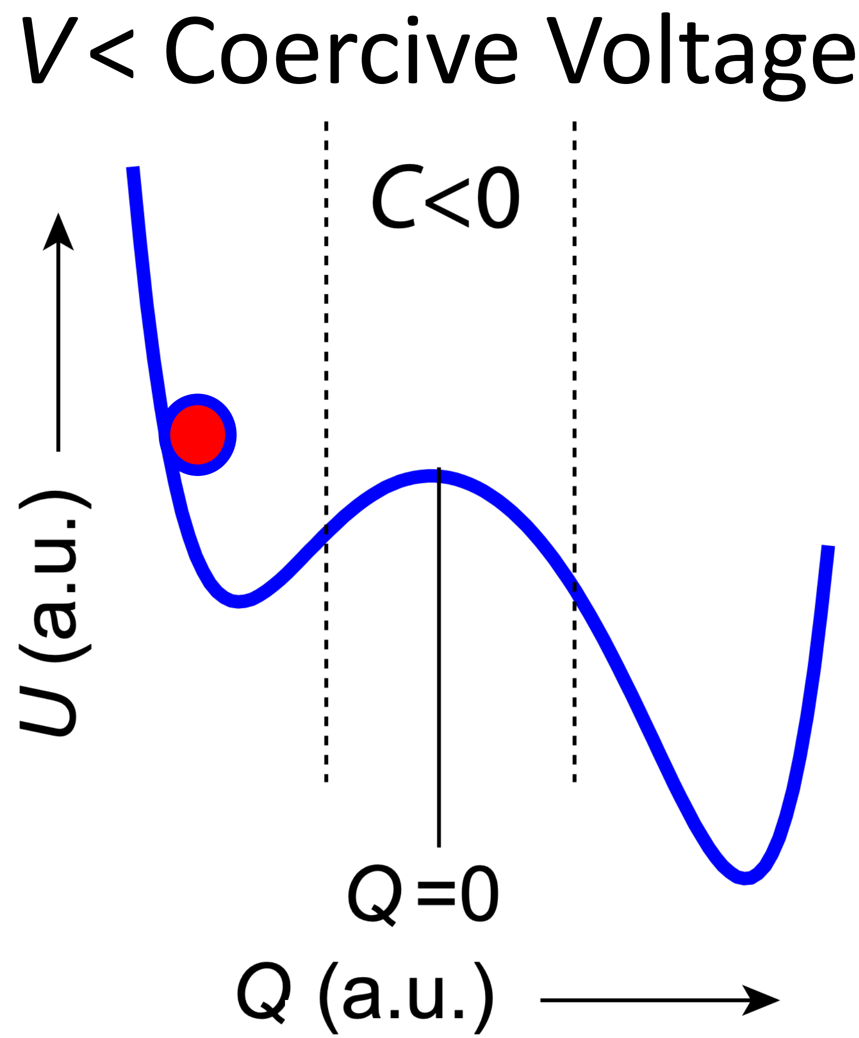
Direct Measurement of Negative Capacitance





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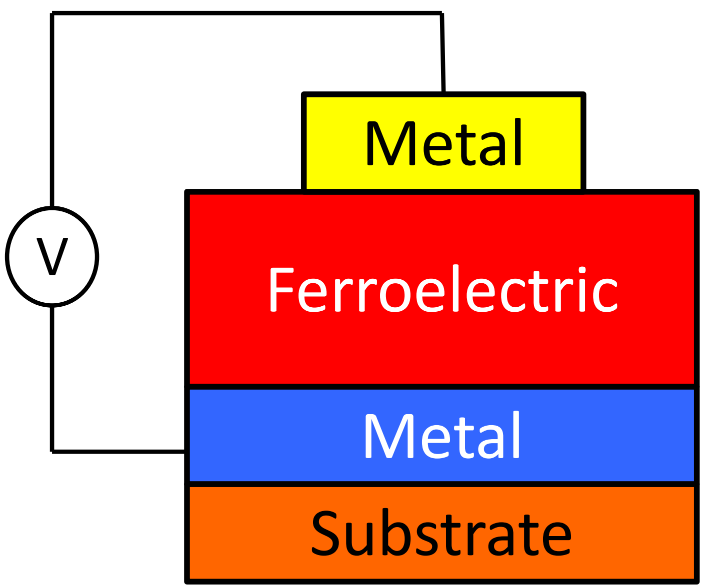
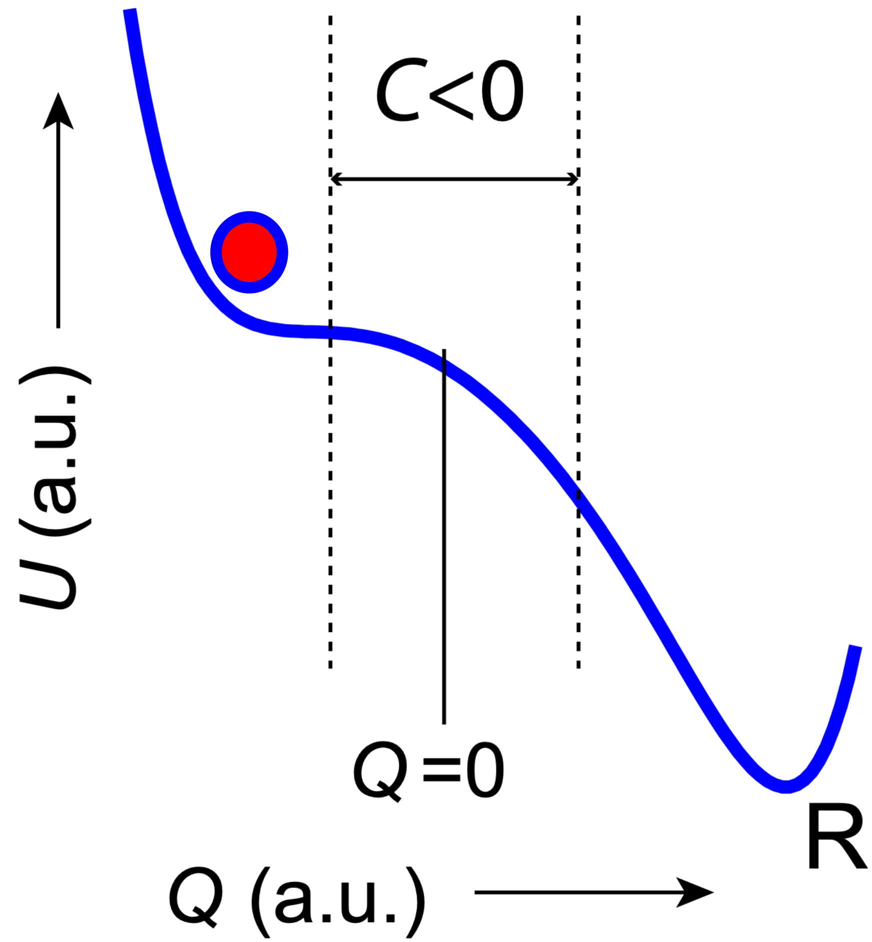


V > Coercive Voltage



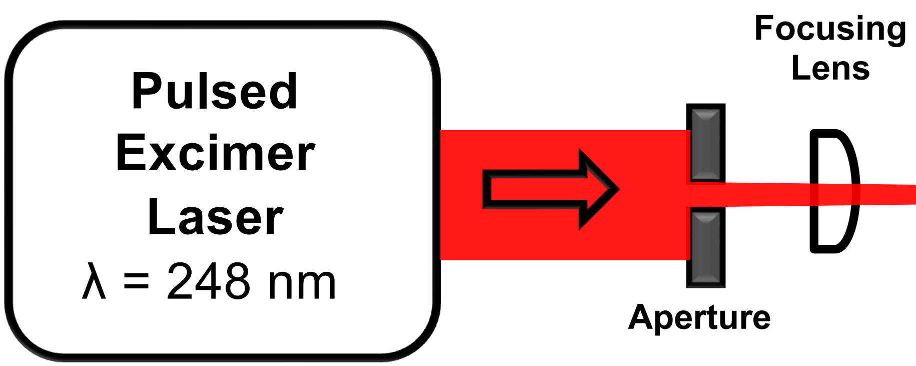
A ferroelectric capacitor goes through the unstable negative capacitance states during switching.

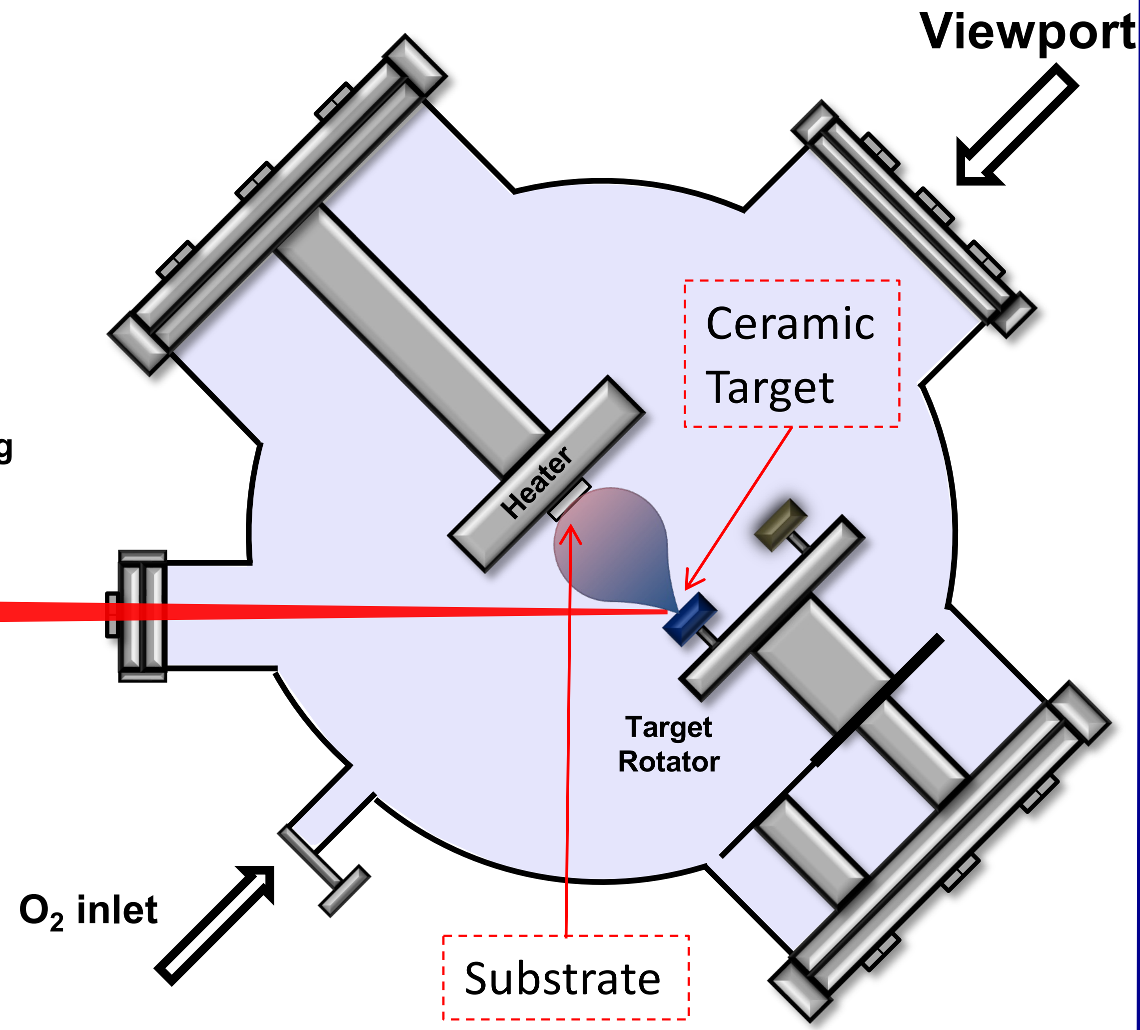
Growth of Ferroelectric Oxides

Experimental Heterostructure

Layer	In-plane lattice parameter
Ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$	a_{PZT}=0.393 nm
Metallic $SrRuO_3$	a_{SRO}=0.394 nm
Substrate $SrTiO_3$	a_{STO}=0.3905 nm

Pulsed laser deposition technique





Typical Growth Conditions:

$SrRuO_3$: 720°C, 100 mTorr, 1.2 J/cm^2, 5-15 Hz

$Pb(Zr_{0.2}Ti_{0.8})O_3$: 630 °C, 100 mTorr, 1-1.5 J/cm^2, 5-15 Hz

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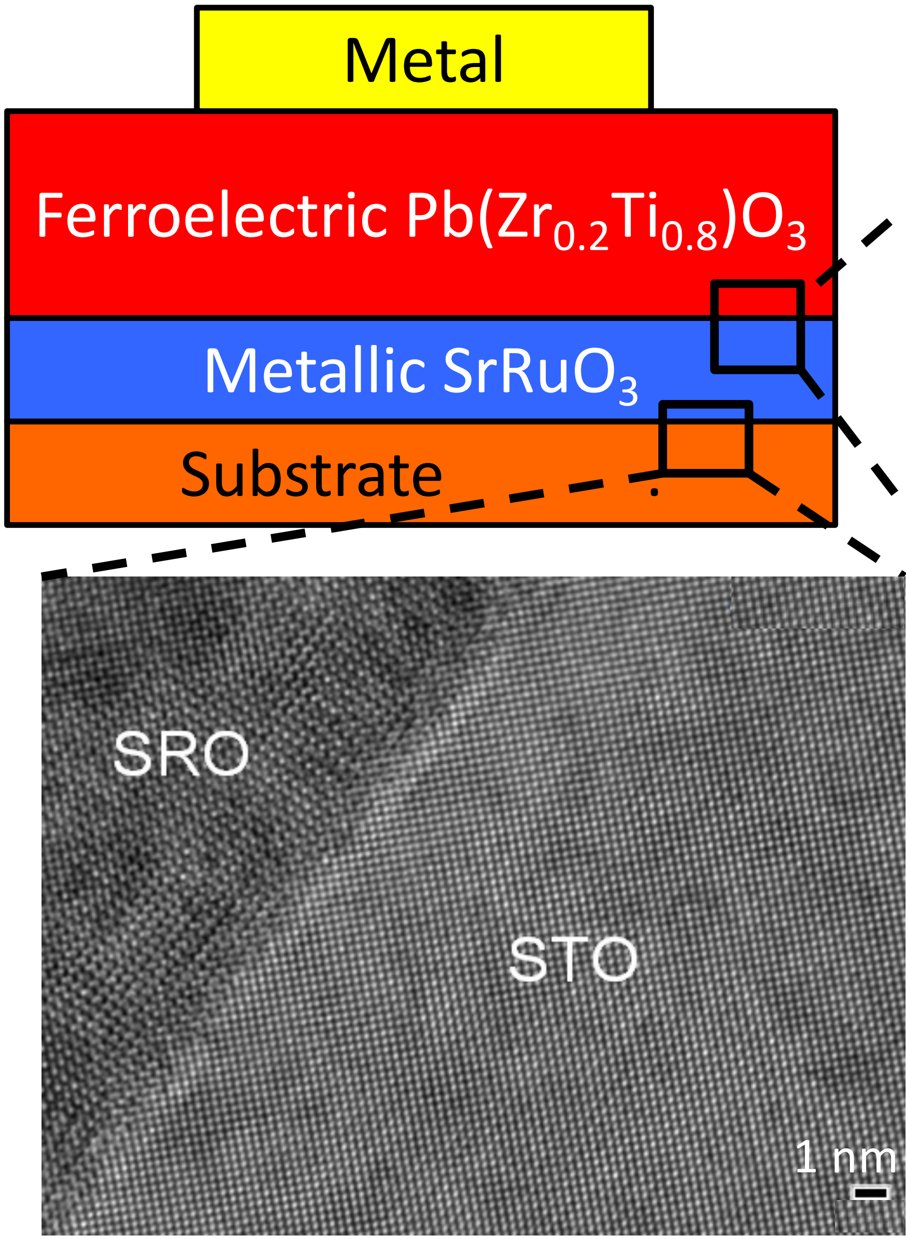
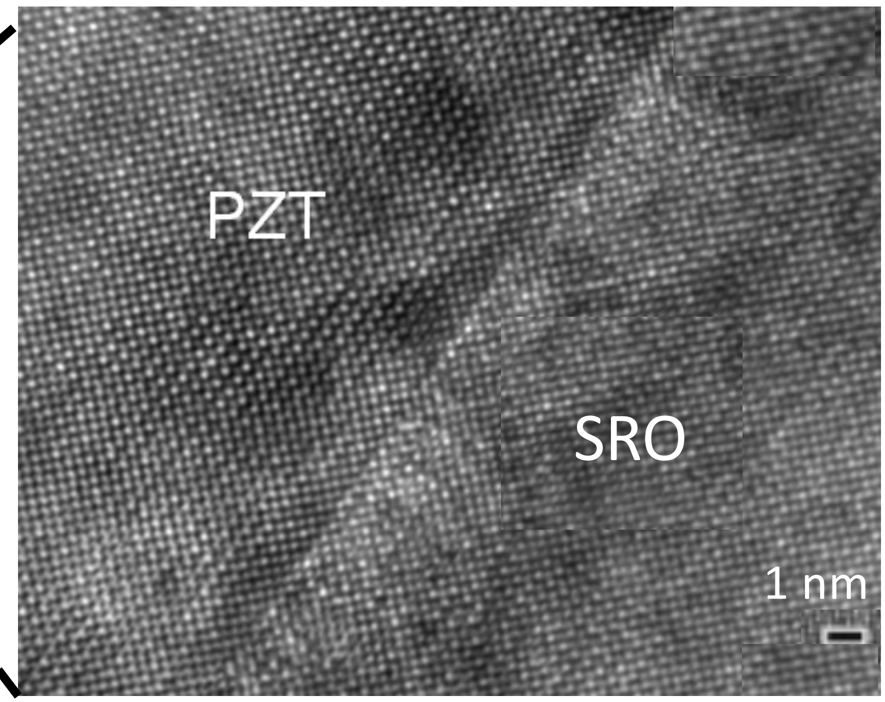
Ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$

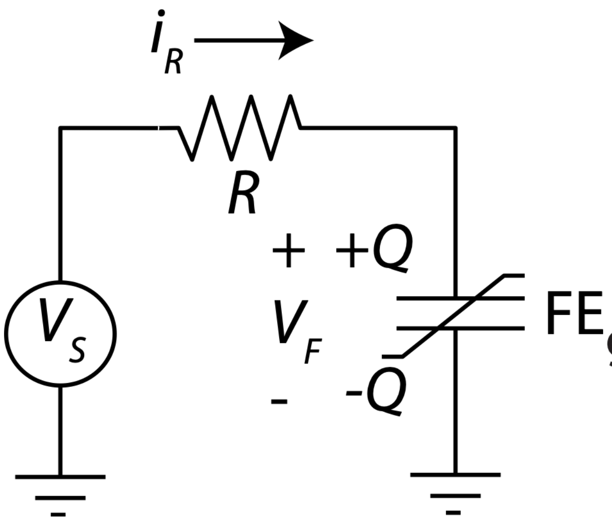


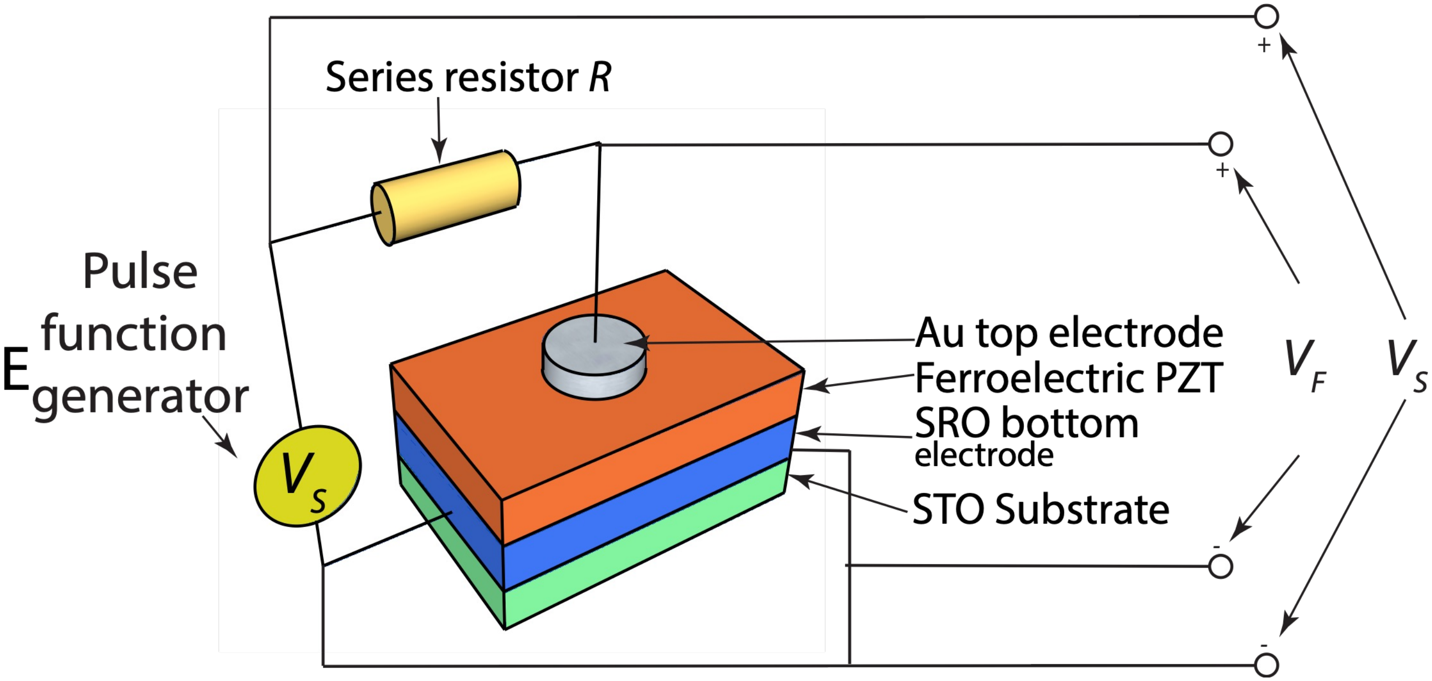


Courtesy: Pan group, U. Mich.

Excellent epitaxial quality!

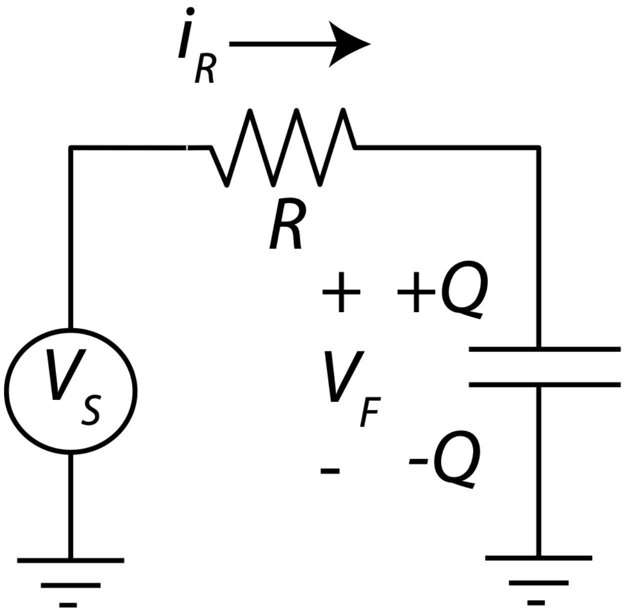
Direct Measurement of Negative Capacitance





A ferroelectric capacitor connected in series with an external resistor.

What happens in an *R*-*C* Series circuit?

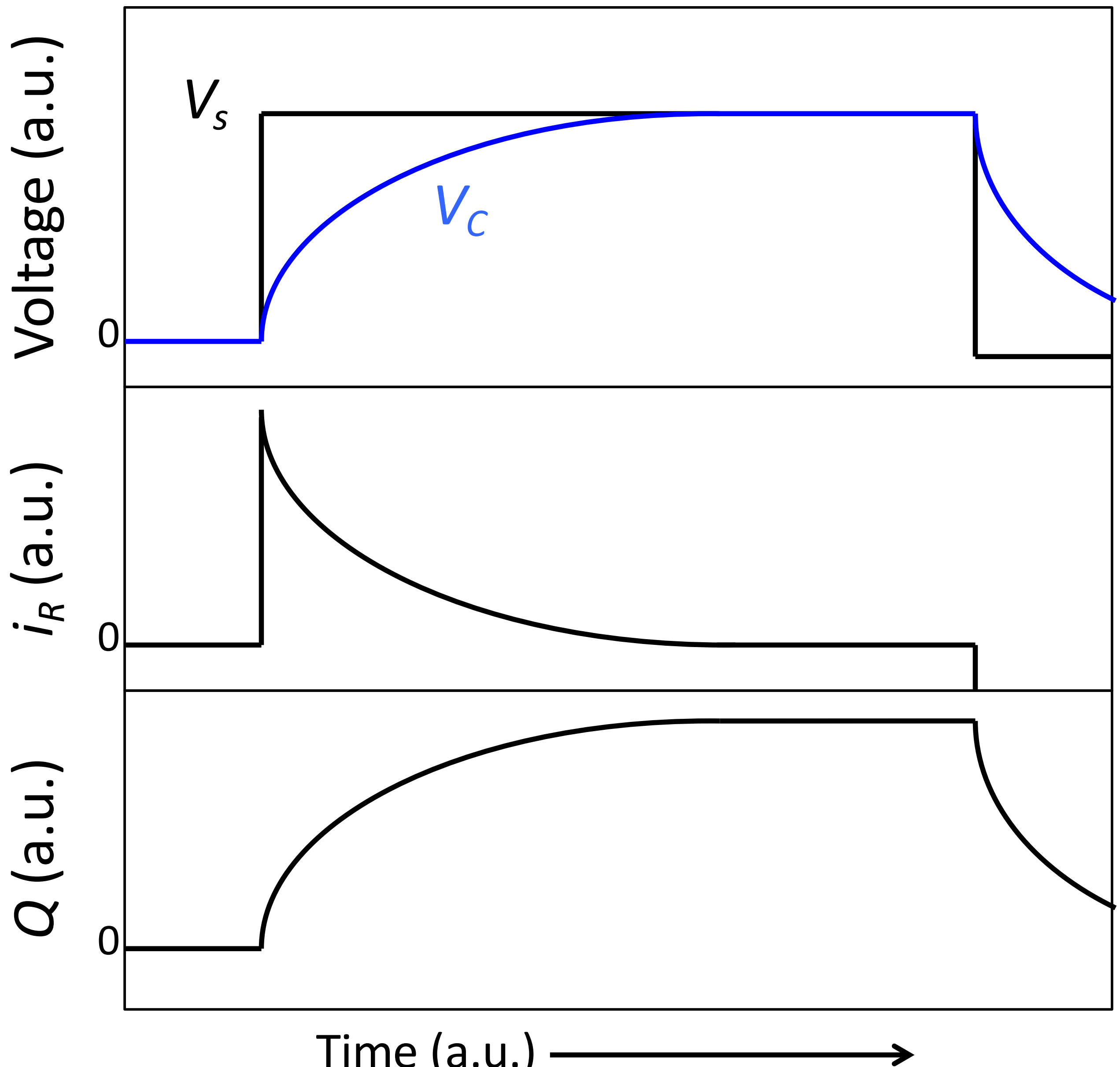


Voltage: $V_C = V_S(1-e^{-t/RC})$

Current: $i_R = V_S e^{-t/RC}/R$

Charge: $Q = CV_S(1-e^{-t/RC})$

At any time t,
$dQ/dV_C = C > 0$.



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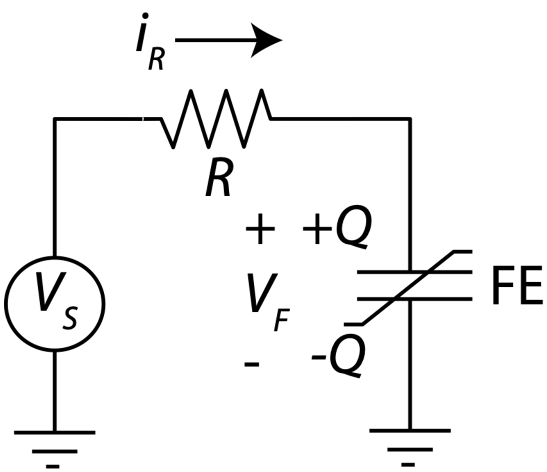
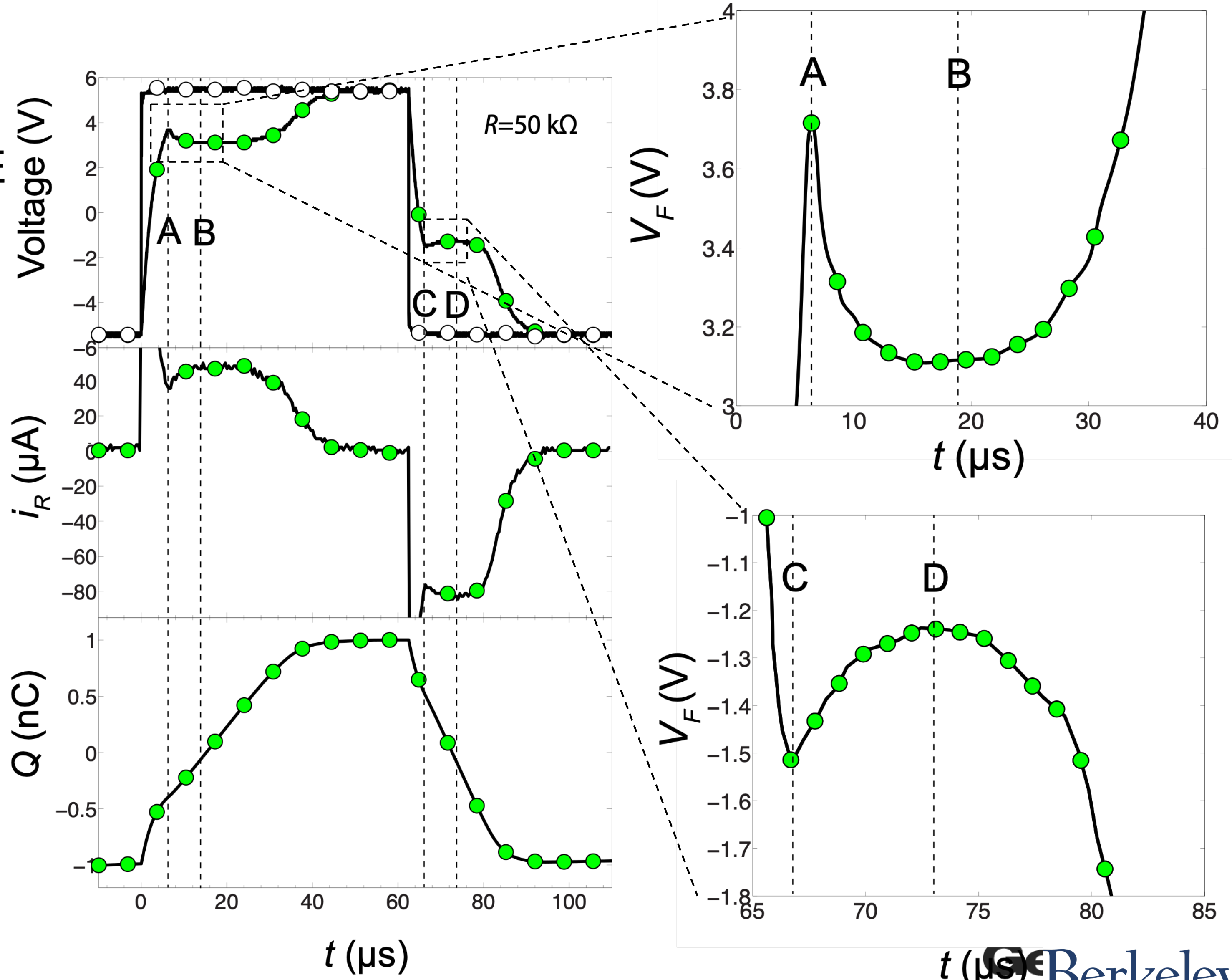
Direct Measurement of Negative Capacitance



60 nm $Pb(Zr_{0.2}Ti_{0.8})O_3$) (Coercive voltage=~2.5 V)

V_s: -5.4 V → +5.4 V → -5.4 V

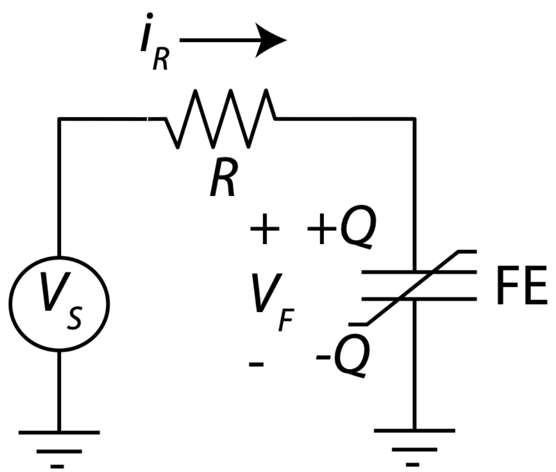


During AB & CD, dQ & dV_F has opposite signs indicating $dQ/dV_F<0$.

Khan et al. Nature Mater. 14, 182 (2015)

Berkeley
UNIVERSITY OF CALIFORNIA

Direct Measurement of Negative Capacitance



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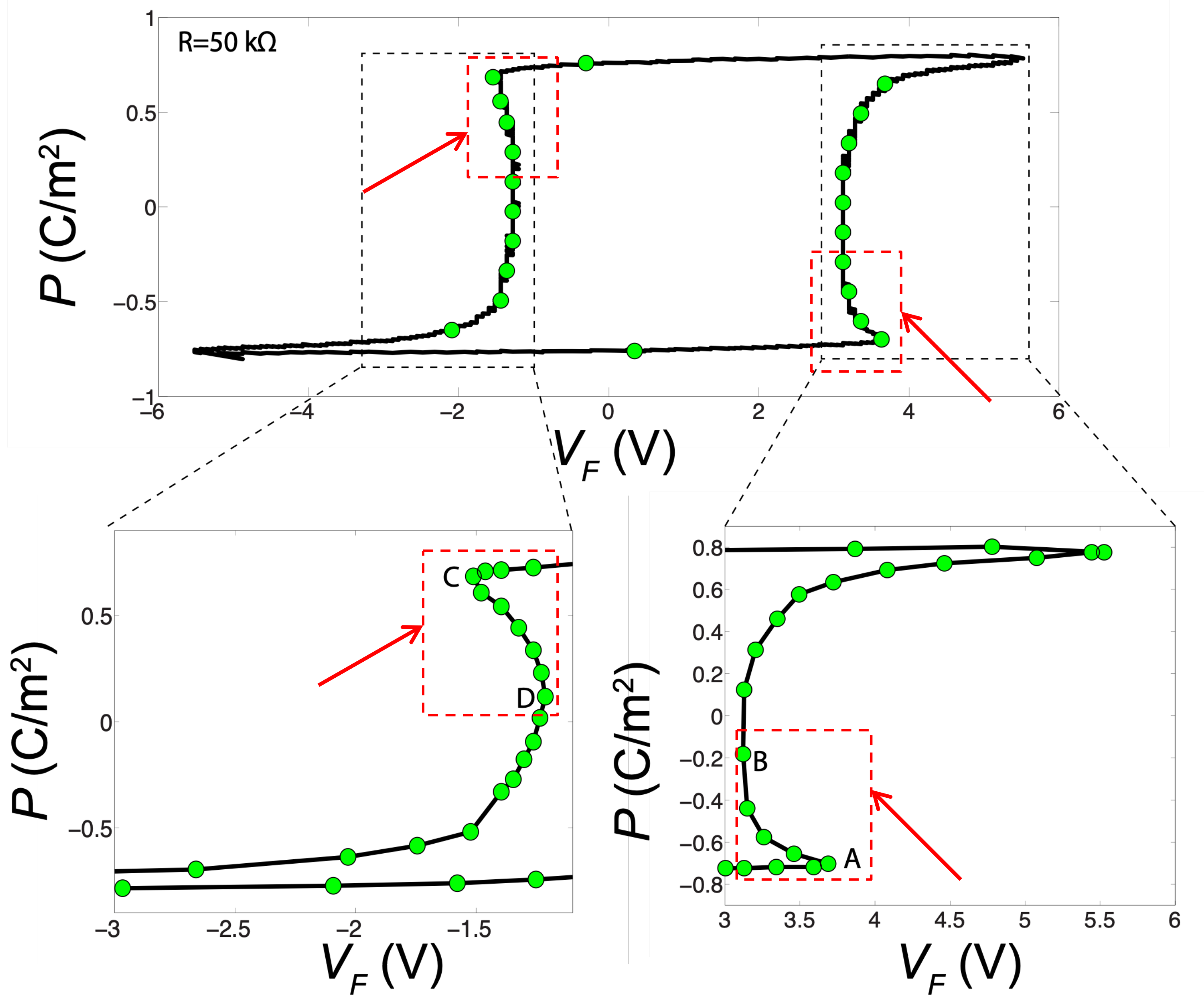

A negative dQ/dV_F directly observed in an isolated ferroelectric.

Khan et al. Nature Mater. 14, 182 (2015)

Perspective

Nature Nanotech. 3, 77 (2008)

NEWS & VIEWS

NANOELECTRONICS

Negative capacitance to the rescue?

Victor V. Zhirnov* and Ralph K. Cavin
are at the Semiconductor Research Corporation, Research Triangle Park, North Carolina 27709, USA.
*e-mail: Victor.Zhirnov@src.org

At this point the proposed negative capacitance mechanism has not been observed in experiments, and it remains

Nature Materials 14, 137 (2015)

news & views

FERROELECTRICS

Negative capacitance detected

The experimental detection of negative capacitance in ferroelectrics rekindles hopes that the phenomenon could be used to further push the miniaturization of conventional transistors.

Gustau Catalan, David Jiménez and Alexei Gruverman

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Negative Capacitance in 1956!

Landauer et al. Polarization reversal in the Barium Titanate hysteresis loops.
J. Appl. Phys. 27, 752 (1956)

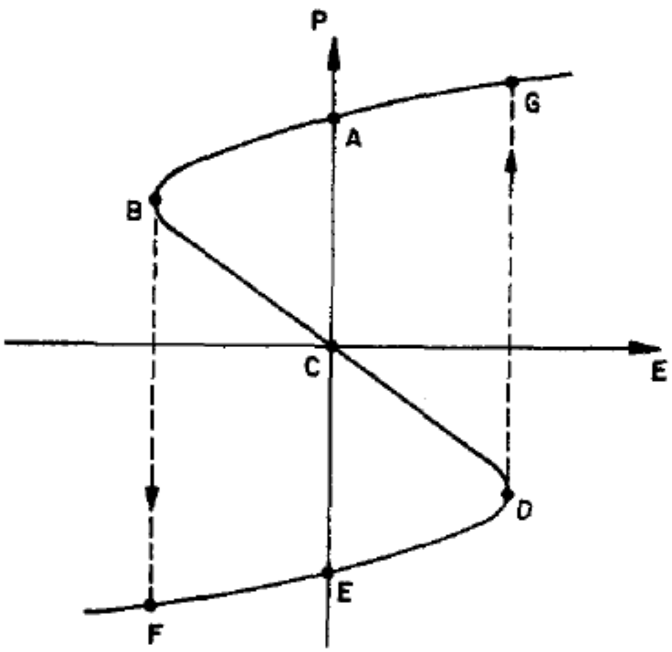

FIG. 1. Plot of polarization against field, at room temperature, as given by Devonshire's theory. P = polarization, E = field. Direction of field and polarization are taken to be the same, and parallel to the "c" axis of a single domain crystal. The solid line $GABCDEF$ gives the theoretical relationship.

Merz. Switching time in BaTiO3 and its dependence on its crystal thickness. **J. Appl. Phys.** 27, 938 (1956)

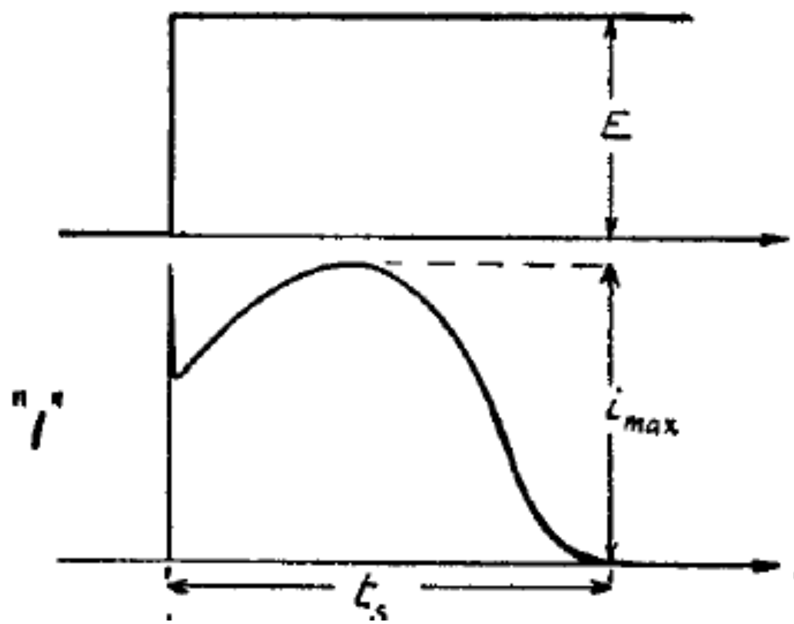

FIG. 1. Pulsing field and pulsing current *versus* time.

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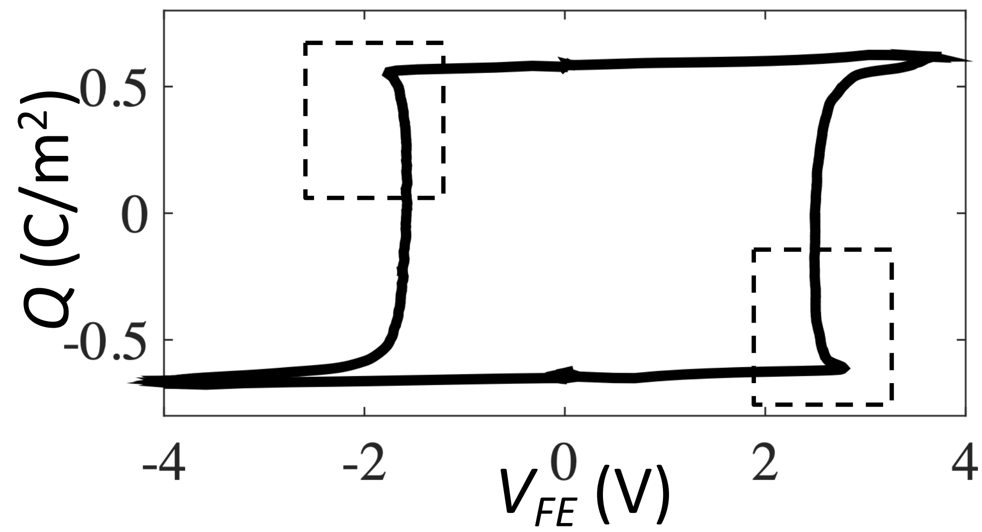
What's next?

Now that negative capacitance has been detected...



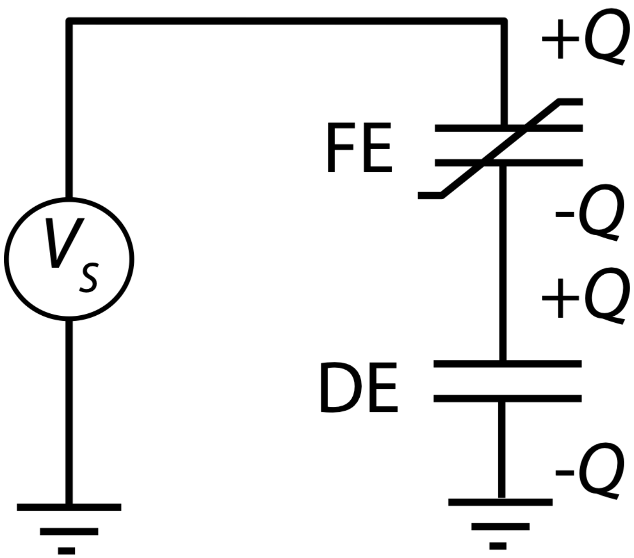
1. Can we see capacitance enhancement?

2. Can we see voltage amplification in a ferroelectric-dielectric network?

3. Can we see sub-60 mV/decade of subthreshold swing?

Breaking the Circuit Laws using Neg. Cap.

Ferroelectric-Dielectric
Series Combination



Equivalent Capacitance $C_{FE+DE} = \left[\dfrac{1}{C_{FE}} + \dfrac{1}{C_{DE}}\right]^{-1}$

$C_{FE+DE} > C_{DE}$ If $C_{FE} < 0$

Enhancement of capacitance in a FE-DE Series combination!

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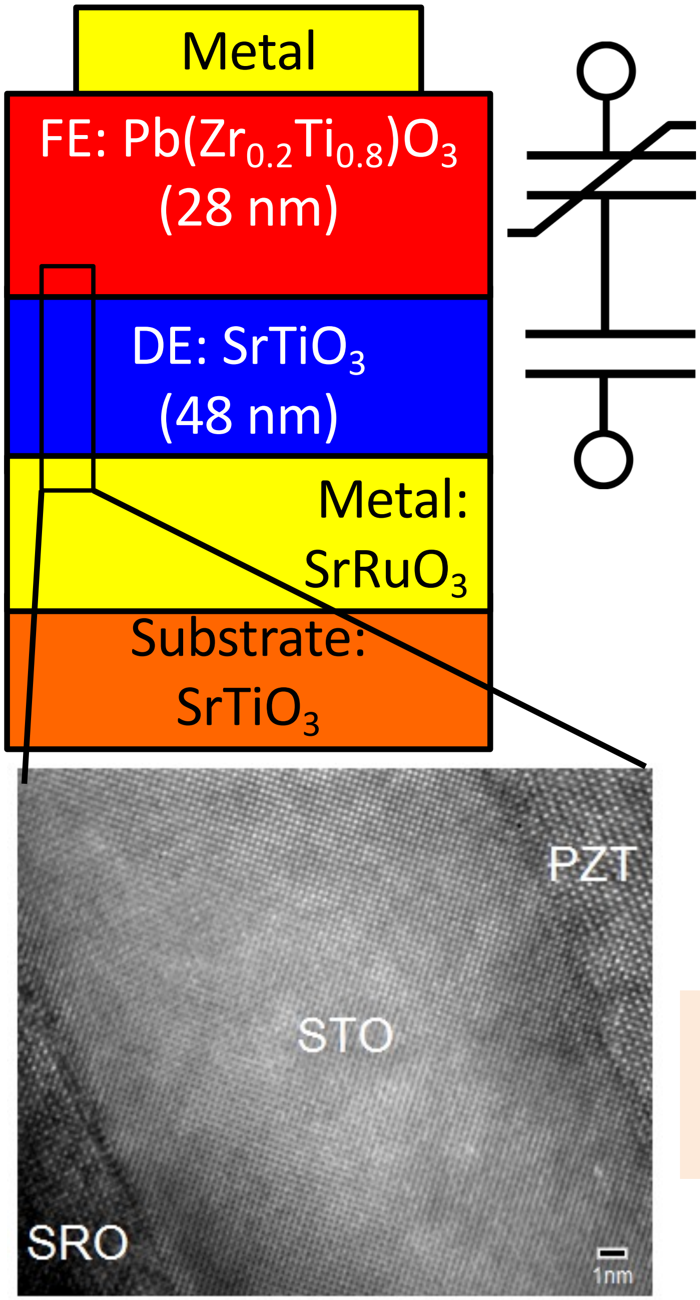
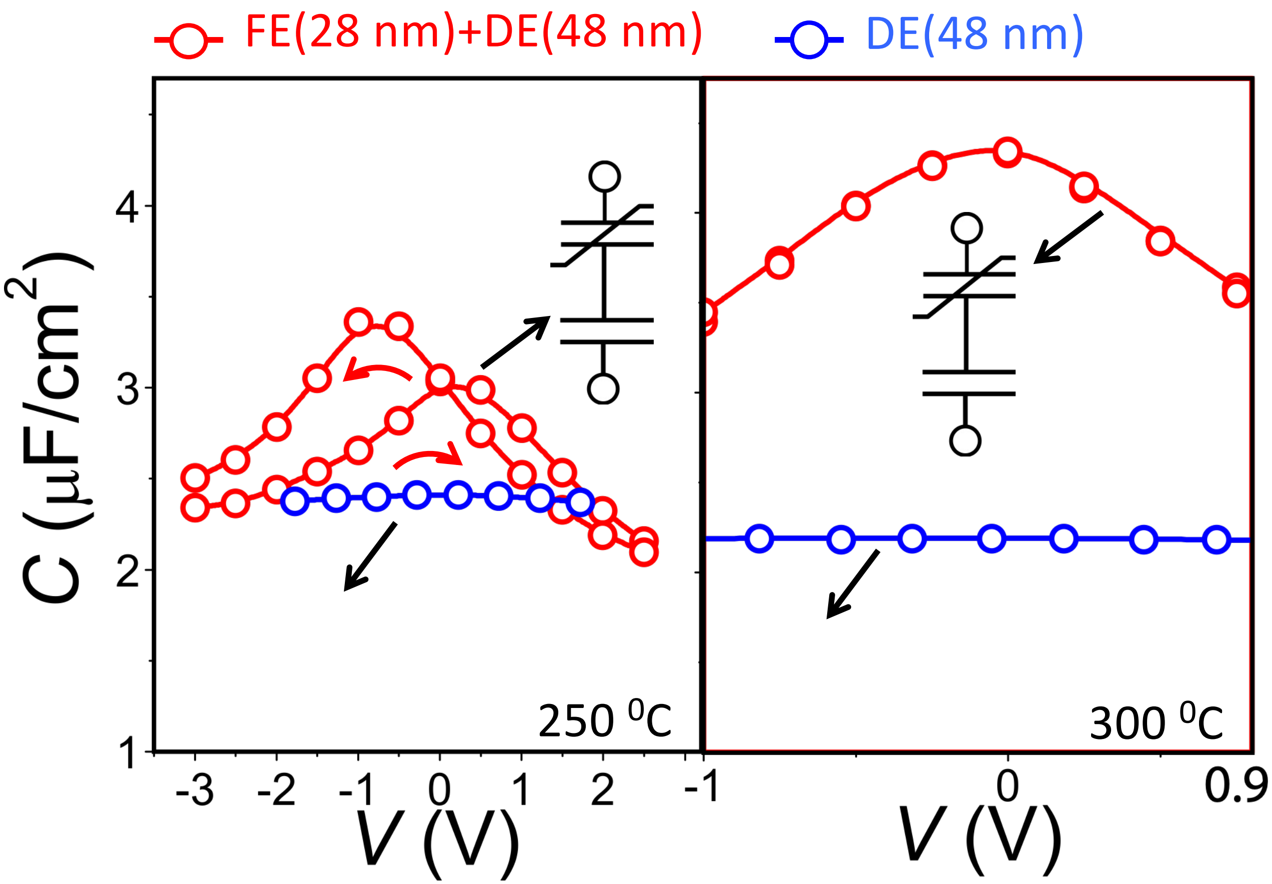
Breaking the Circuit Laws using Neg. Cap.



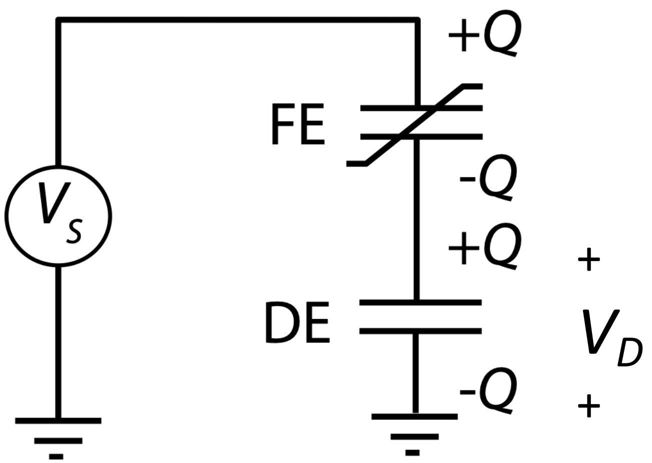
C-V Characteristics

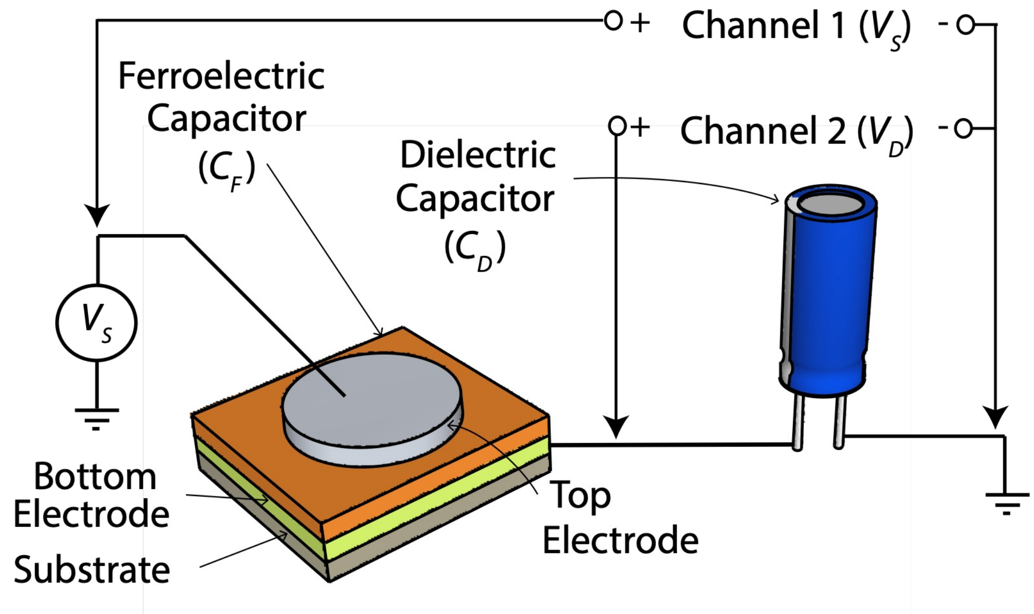


Capacitance Enhancement in a FE-DE heterostructure experimentally observed!

Khan et al. Appl. Phys. Lett. 100, 113501 (2011)
(cover article, most downloaded Aug/Sep 2011).
Gao, Khan et al. Nano Lett. 14, 5814 (2014)

Breaking the Circuit Laws using Neg. Cap.

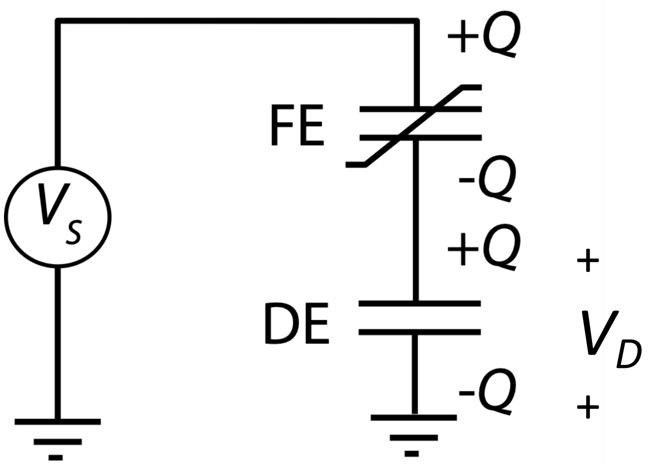


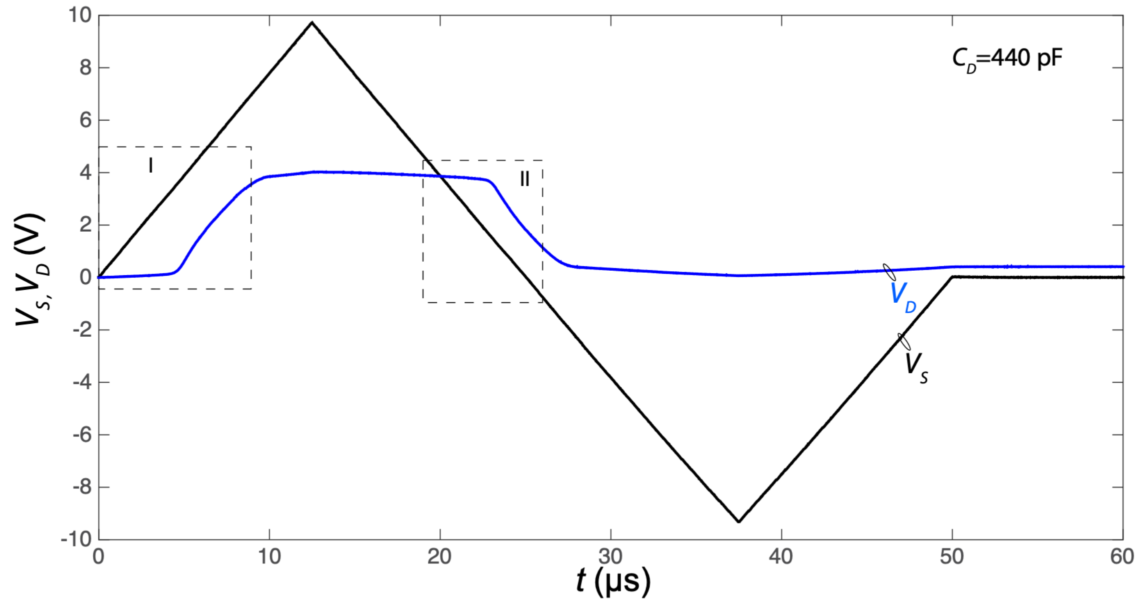


Voltage amplification: $\dfrac{dV_D}{dV_S} = \dfrac{C_F}{C_F + C_D} = \dfrac{|C_F|}{|C_F| - C_D}$ If $|C_F| > C_D$, $\boxed{\dfrac{dV_D}{dV_S} > 1}$

Khan, Hoffmann et al. (under review)

Breaking the Circuit Laws using Neg. Cap.





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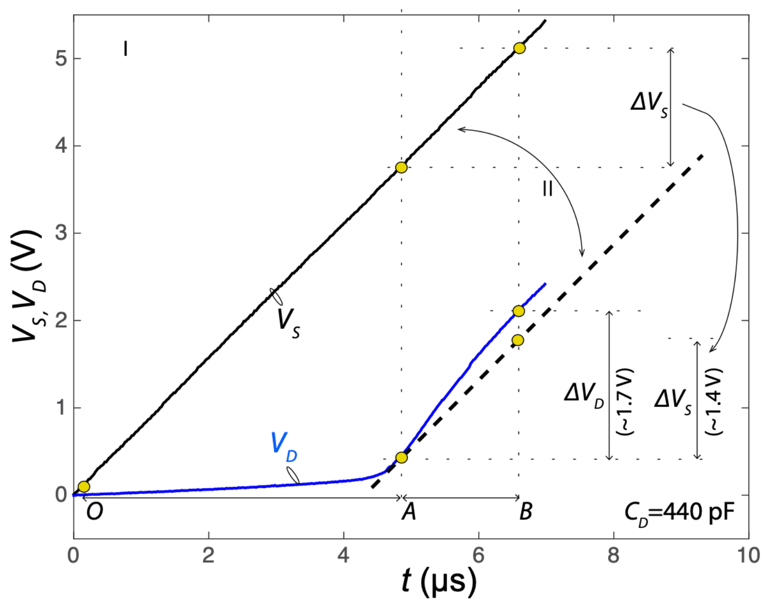

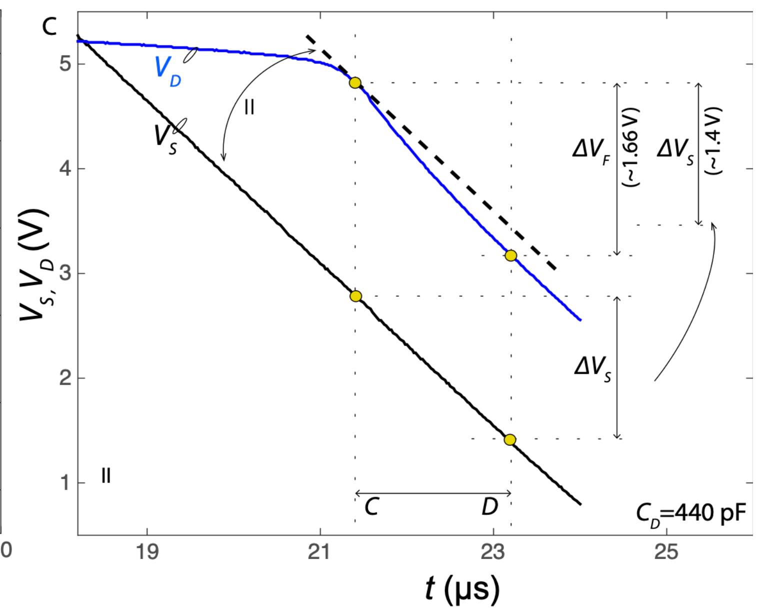

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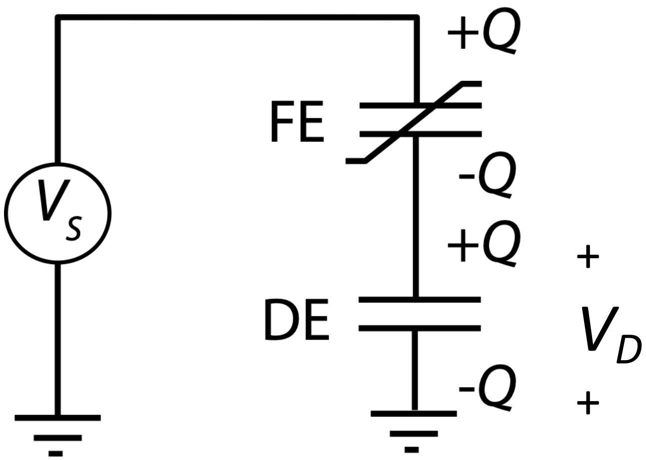
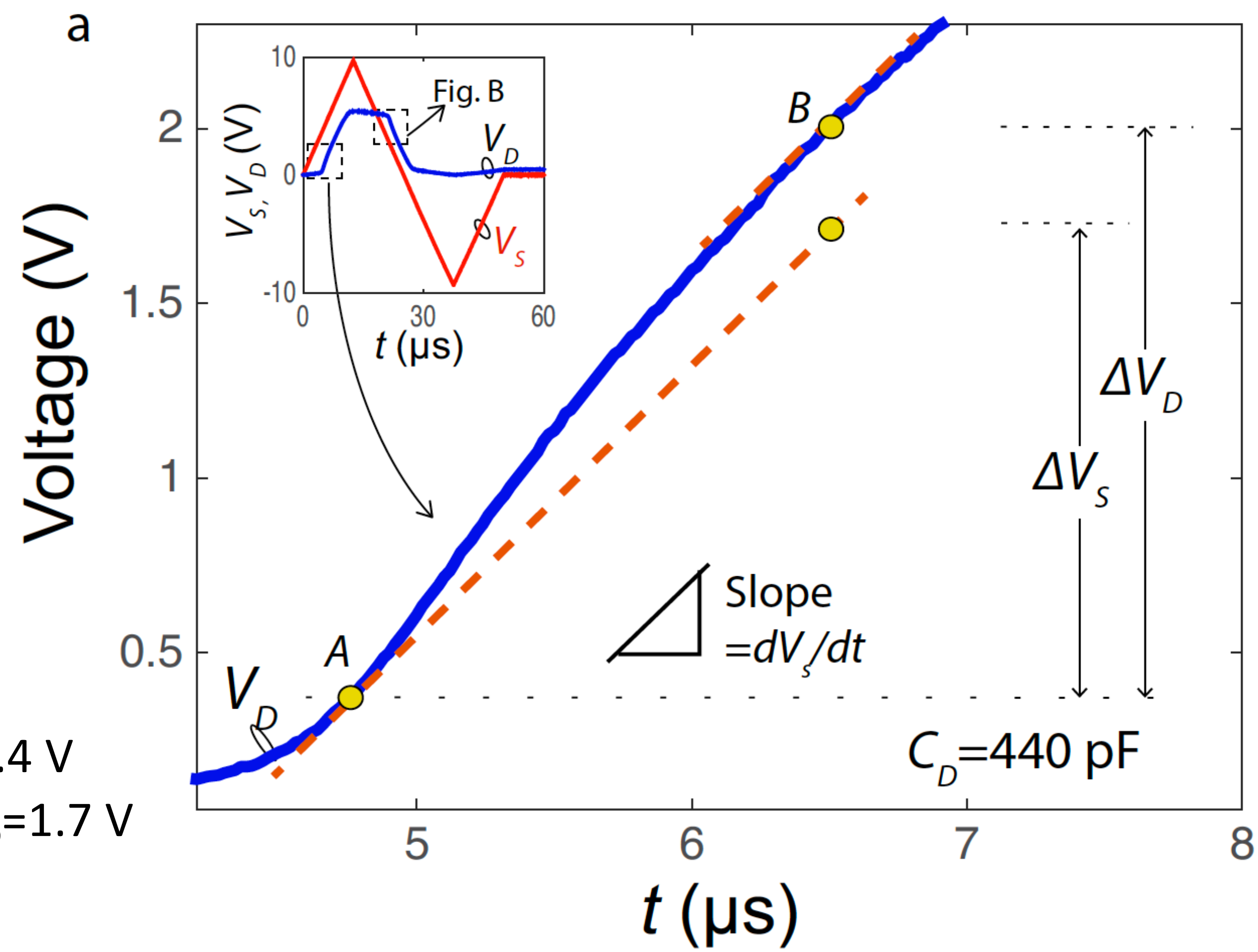
Breaking the Circuit Laws using Neg. Cap.





Khan, Hoffmann et al. (under review)

Change in source voltage ΔV_S=1.4 V
Change in dielectric voltage ΔV_D=1.7 V

$$\frac{\Delta V_D}{\Delta V_S} = \frac{1.7\ V}{1.4\ V} \approx 1.21 = \frac{|C_F|}{|C_F| - C_D}$$

Voltage amplification in a FE-DE series network experimentally observed!

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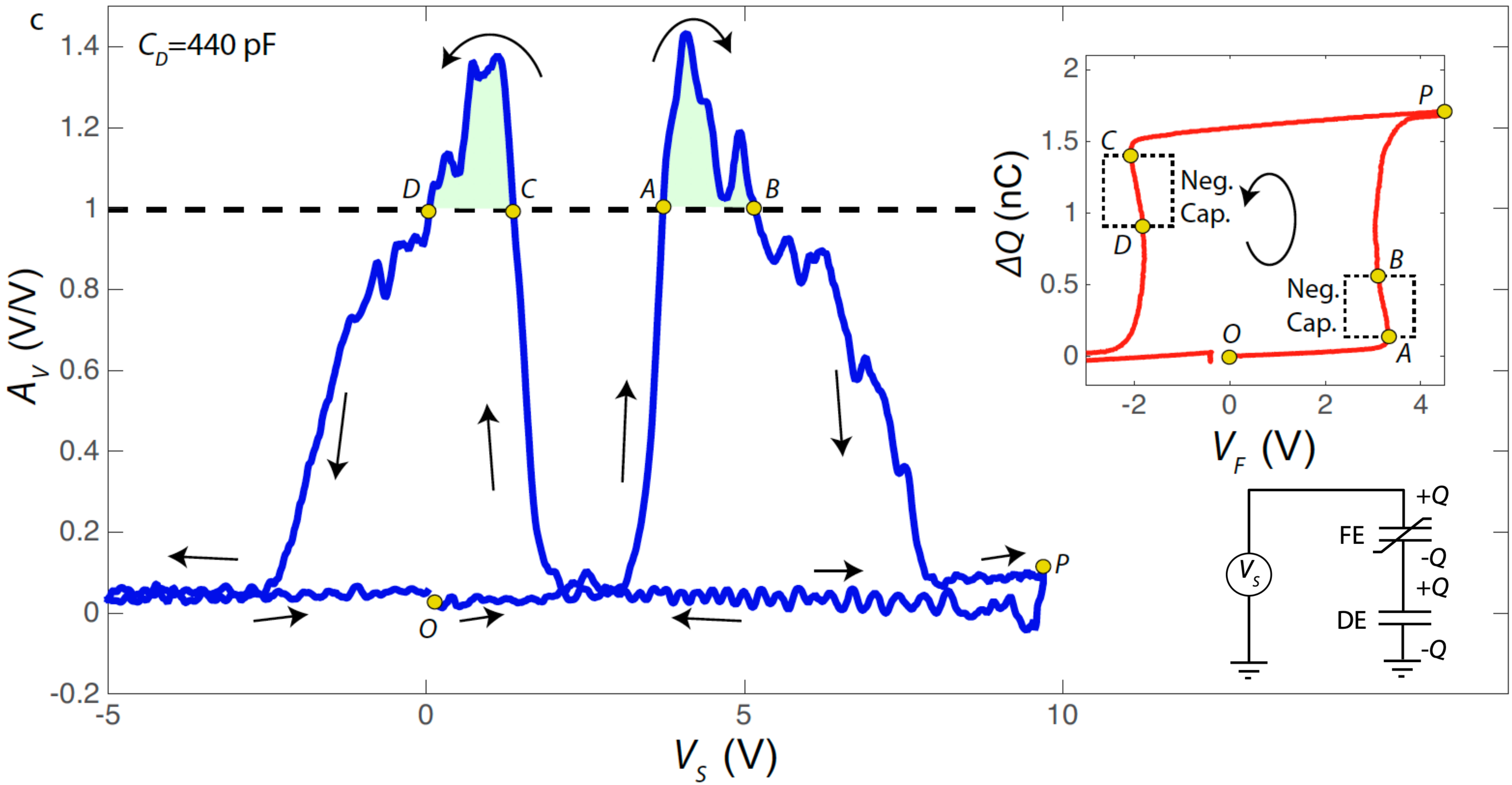
Ferroelectric+Dielectric Capacitor

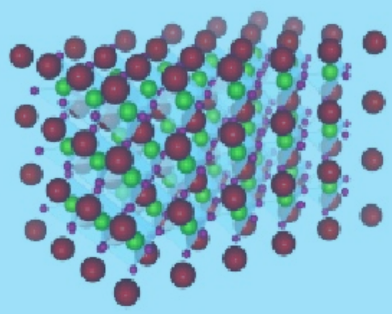


Khan, Hoffmann et al. (under review)

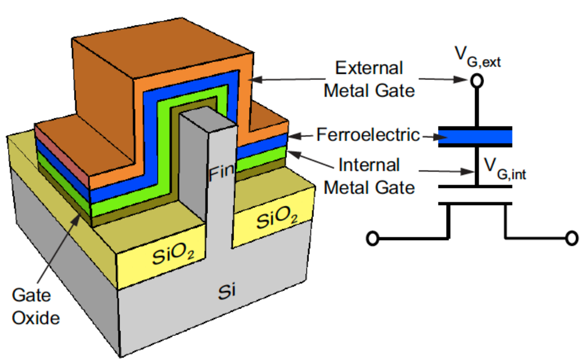
Voltage amplification in a FE-DE series network experimentally observed!

What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors



What do we need to know?

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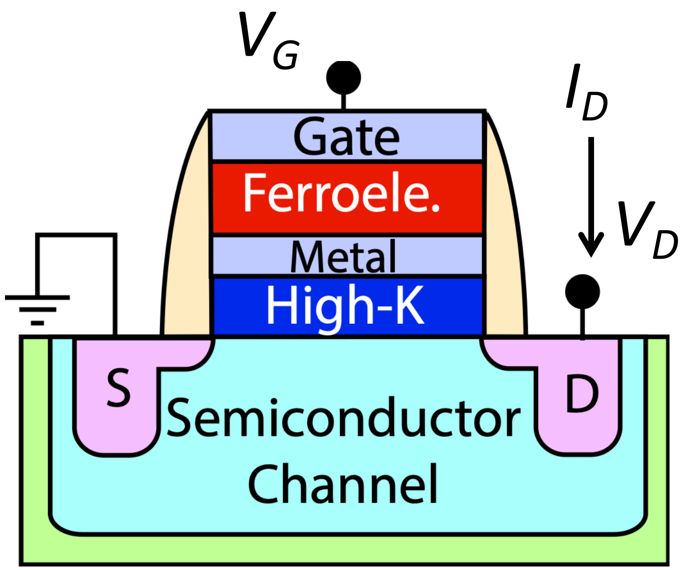
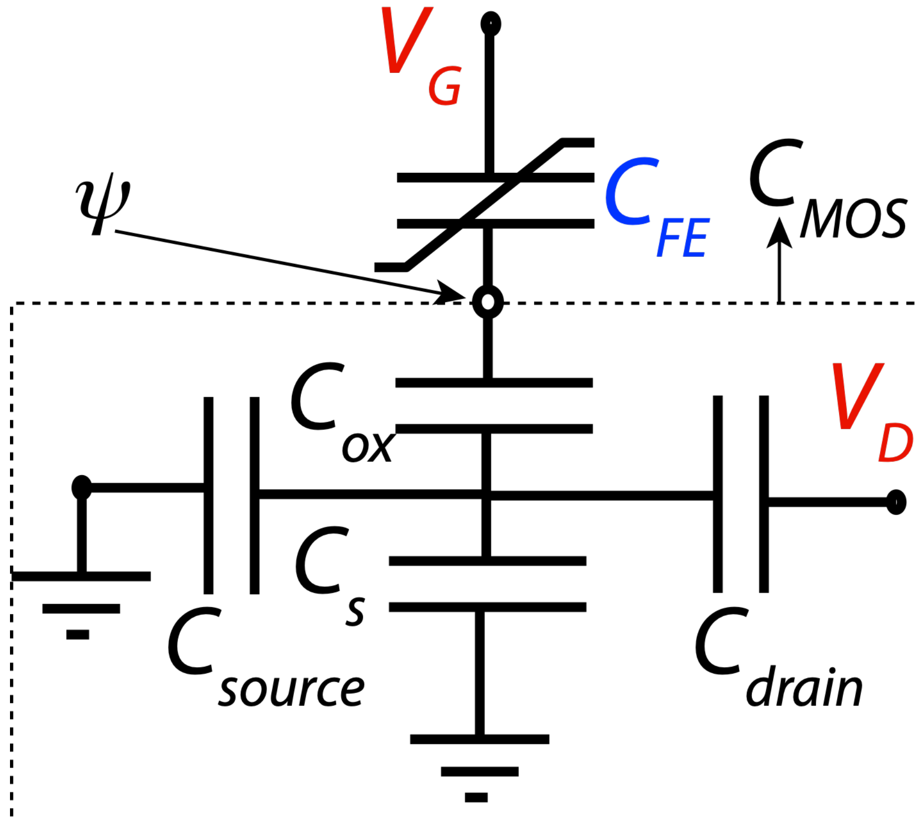
Physics of Negative Capacitance FET

NCFET Structure





Baseline MOSFET: TCAD Simulation.

Ferroelectric: 1-D Landau Simulation with $Pb(Zr_{0.5}Ti_{0.5})O_3$ and Doped HfO_2

Ideal Switch: ~0 mV/decade ⇐
$|C_{FE}| \approx C_{MOS}, |C_{FE}| > C_{MOS}$

Khan et al. IEDM 2011
Yeung, Khan et al. VLSI-TSA 2013
Yeung, Khan et al. SISPAD 2012
Hu, Khan et al. DRC 2015
Cheng-I, Khan et al. IEEE T-ED 2016 (Just accepted)
Khandelwal, Khan et al. VLSI Tech. (submitted)

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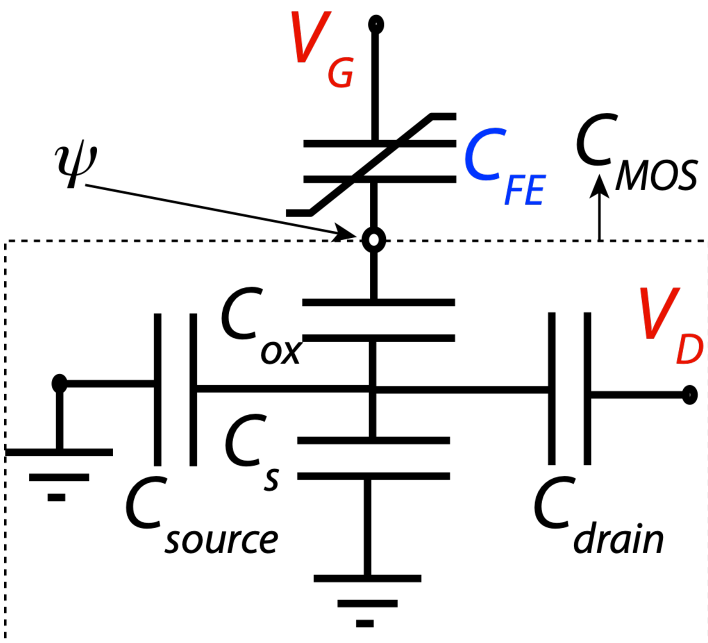
Physics of Negative Capacitance FET

NCFET Structure



Equivalent Circuit Diagram

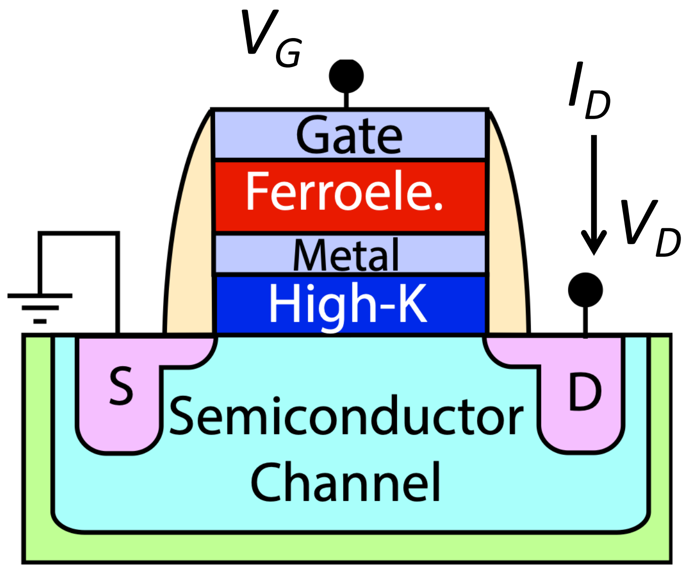
Amplification Factor $$\frac{d\psi}{dV_G} = \frac{C_{FE}}{C_{MOS} + C_{FE}}$$

Modified Body Factor $$m^o = \frac{dV_G}{d\psi} = 1 - \frac{C_{MOS}}{|C_{FE}|}$$

Subthreshold Swing $$S^{NC} = S^{original} \times \left(1 - \frac{C_{MOS}}{|C_{FE}|}\right)$$

Condition	Characteristics	Mode
$C_{FE}<0$, $\lvert C_{FE}\rvert>C_{MOS}$	$0<m^o<1$, $S^{NC}<S^{original}$	Logic
$C_{FE}<0$, $\lvert C_{FE}\rvert<C_{MOS}$	$m^o<0$, $S^{NC}<0$	Memory

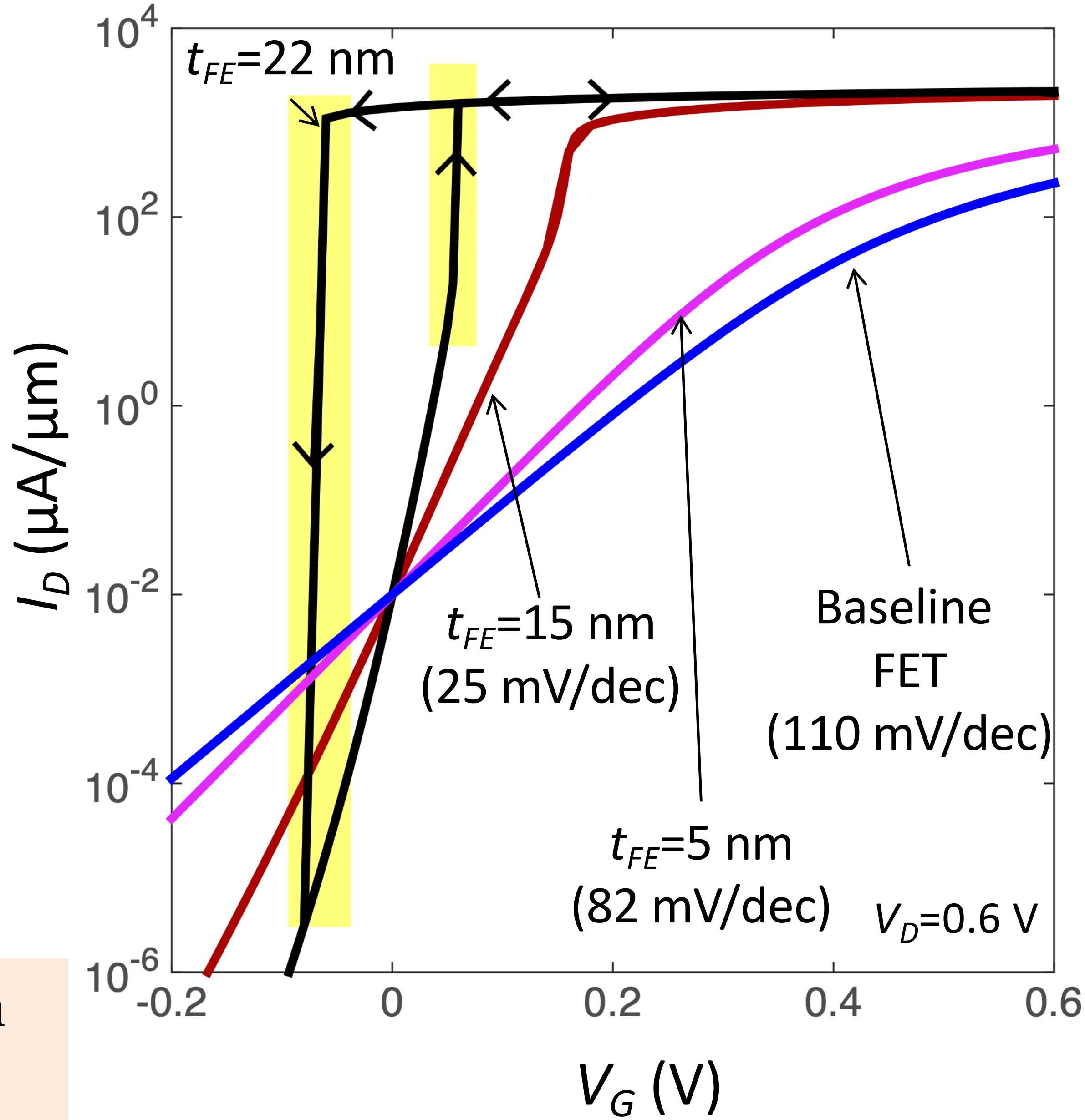
Physics of Negative Capacitance FET



Ferroelectric Capacitance $|C_{FE}| = \sim \frac{P_o}{E_{FE} t_{FE}}$

Intel 45 nm node, MIT MVS Model
Collaboration with
Dimitri Antoniadis, MIT

Capacitance Matching can lead to wide range of behavior in NCFETs!



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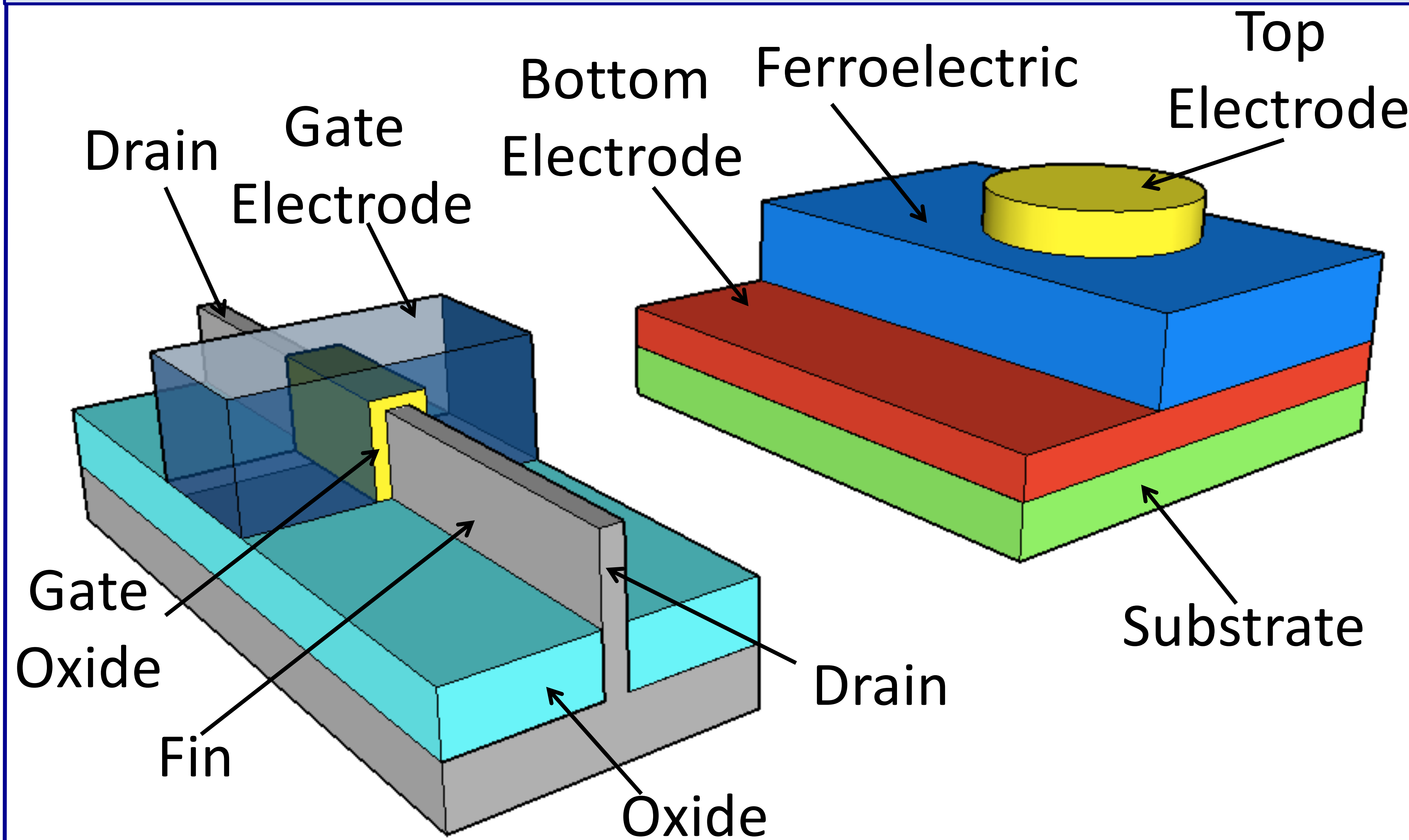
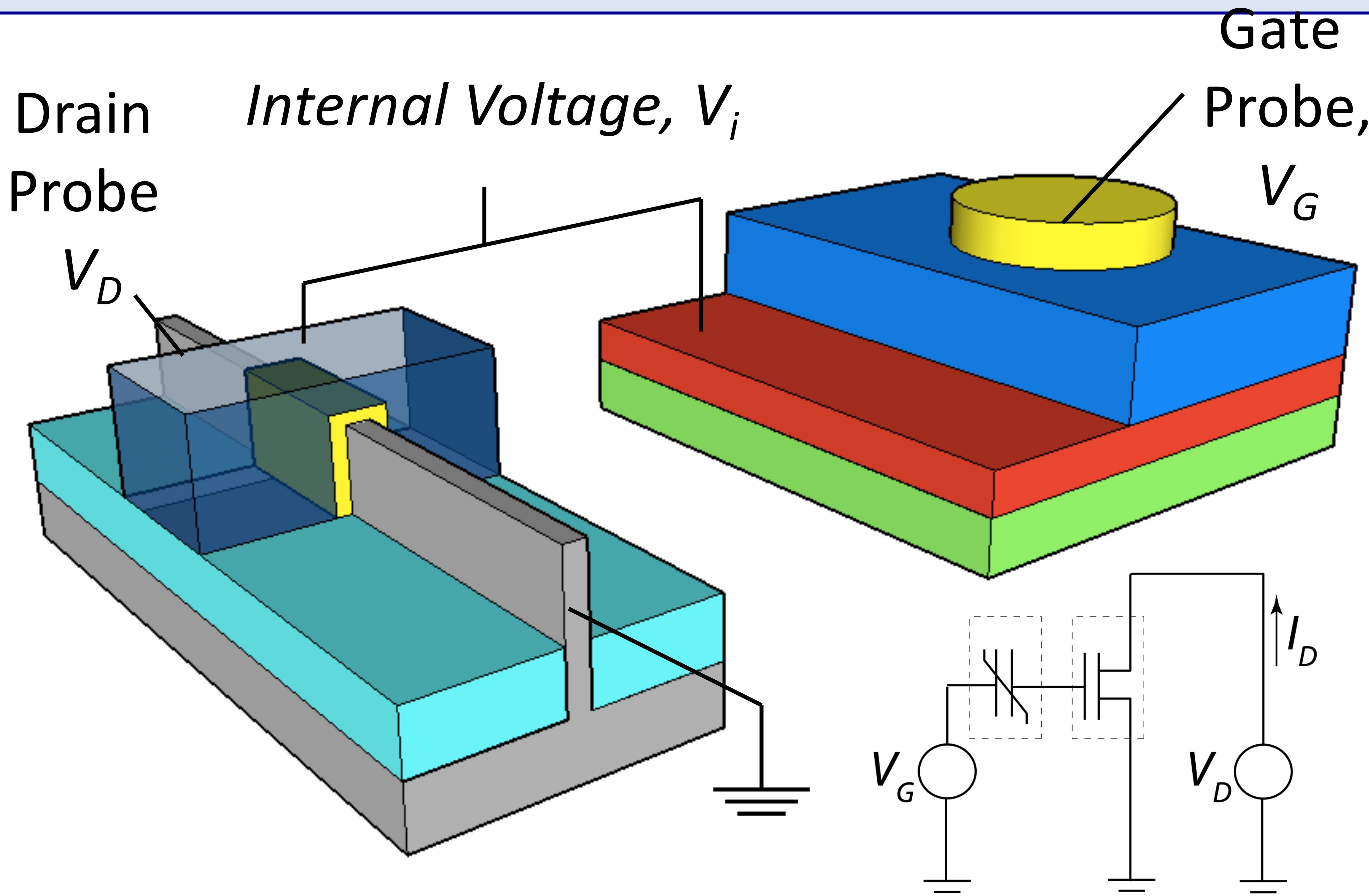
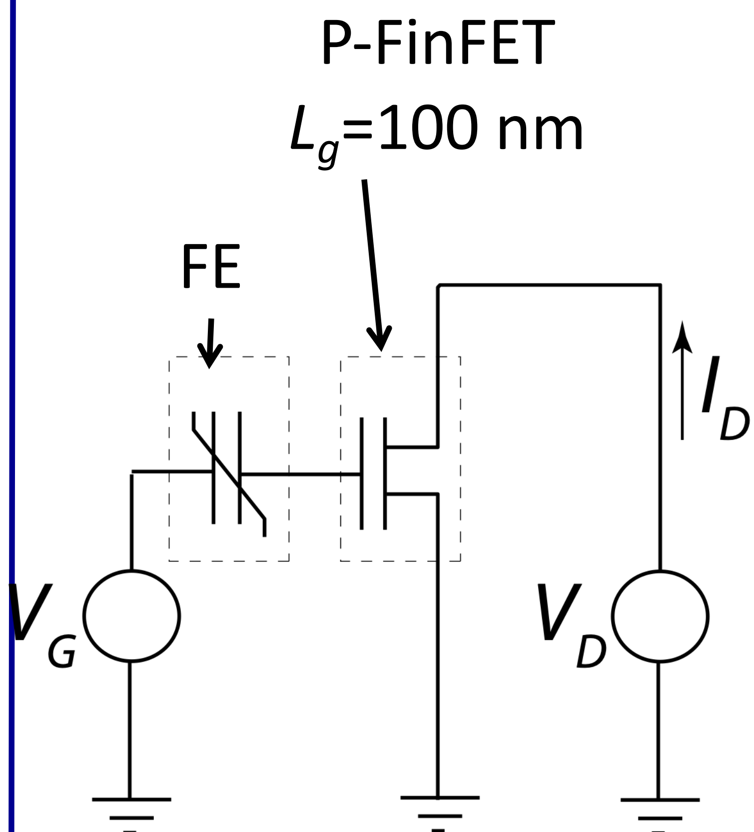
Externally Connected NCFET

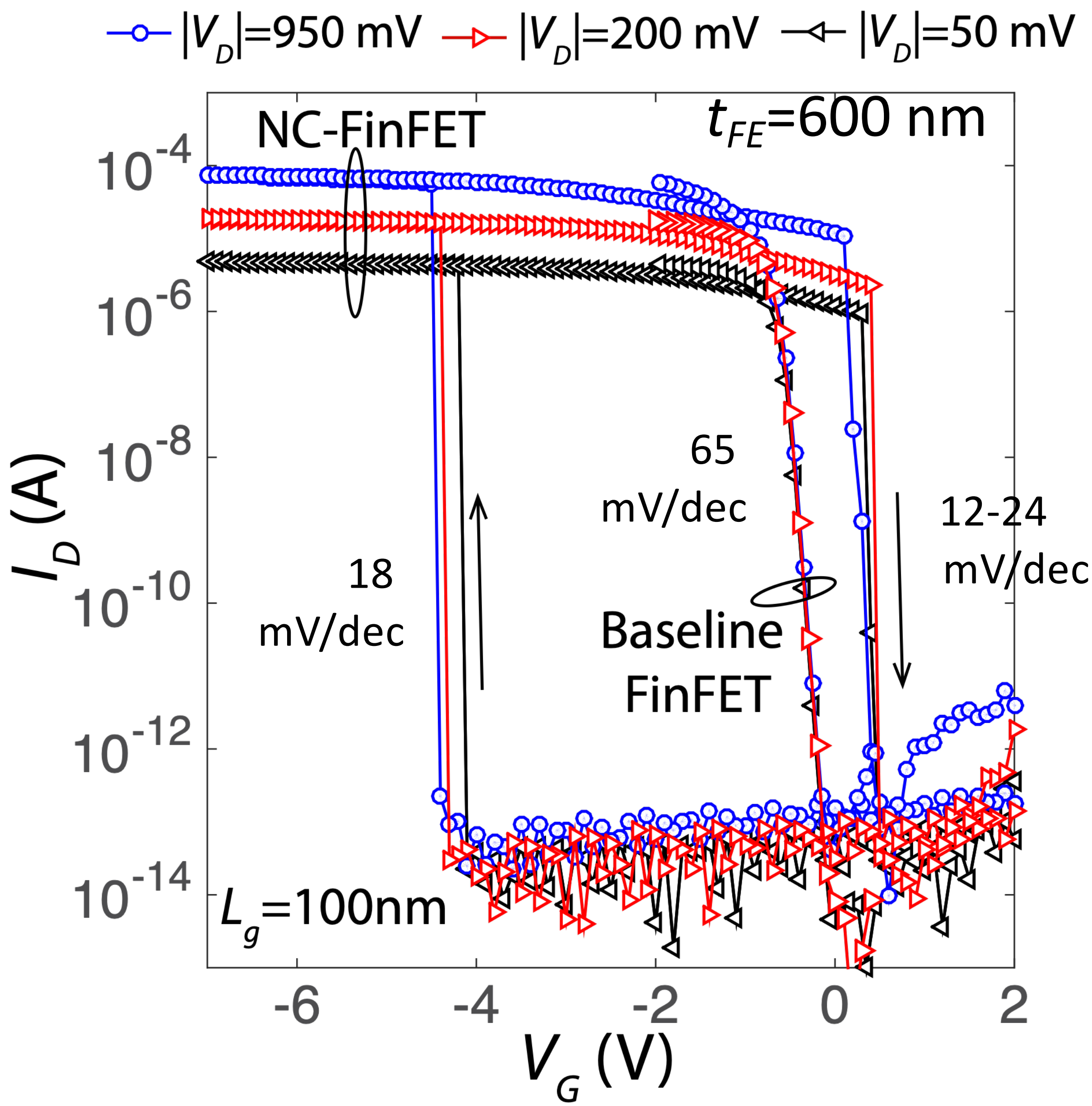


Externally Connected NCFET



Externally Connected NCFET



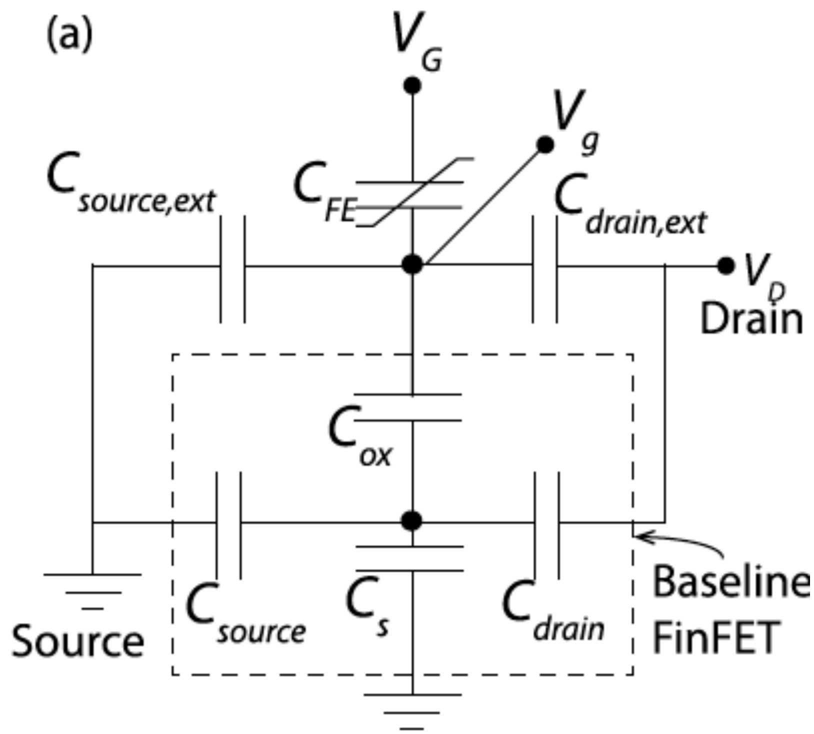


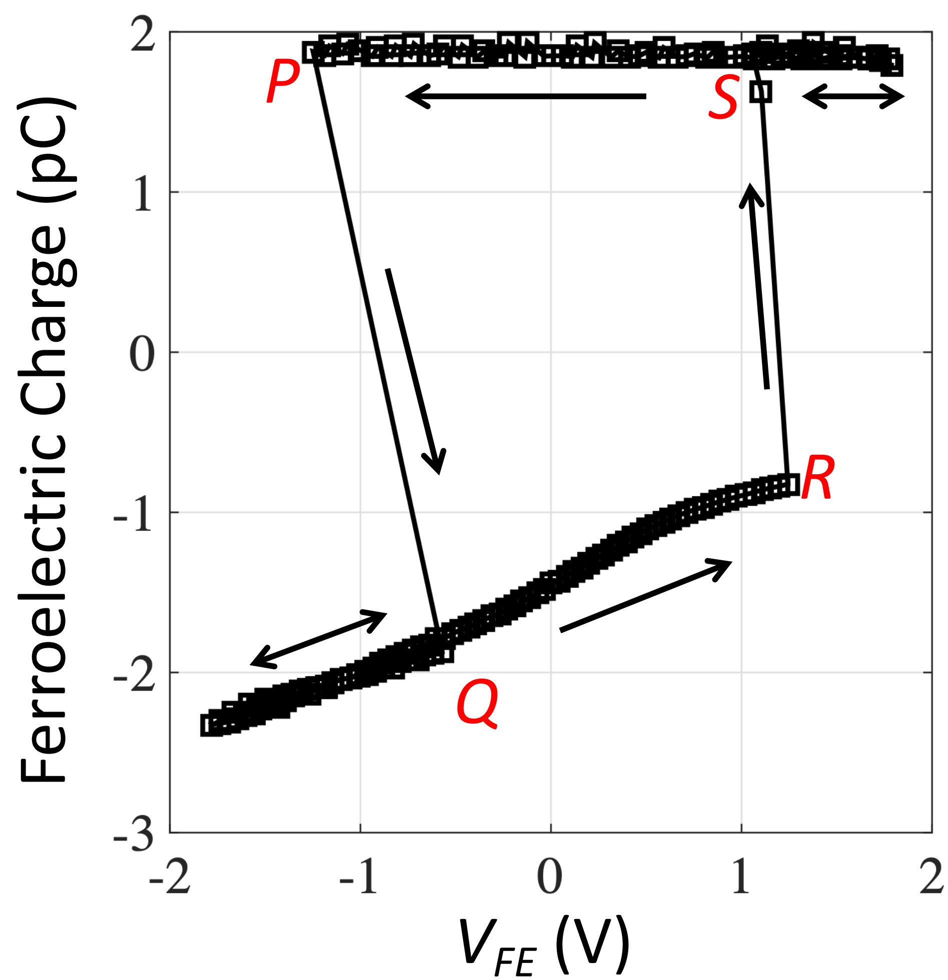
FinFET L_G=100 nm
Fin width=35 nm
Fin height=25 nm
EOT=1.4 nm

Khan et al. IEEE EDL 37, 111 (2016)

Berkeley
UNIVERSITY OF CALIFORNIA

Externally Connected NC-FET



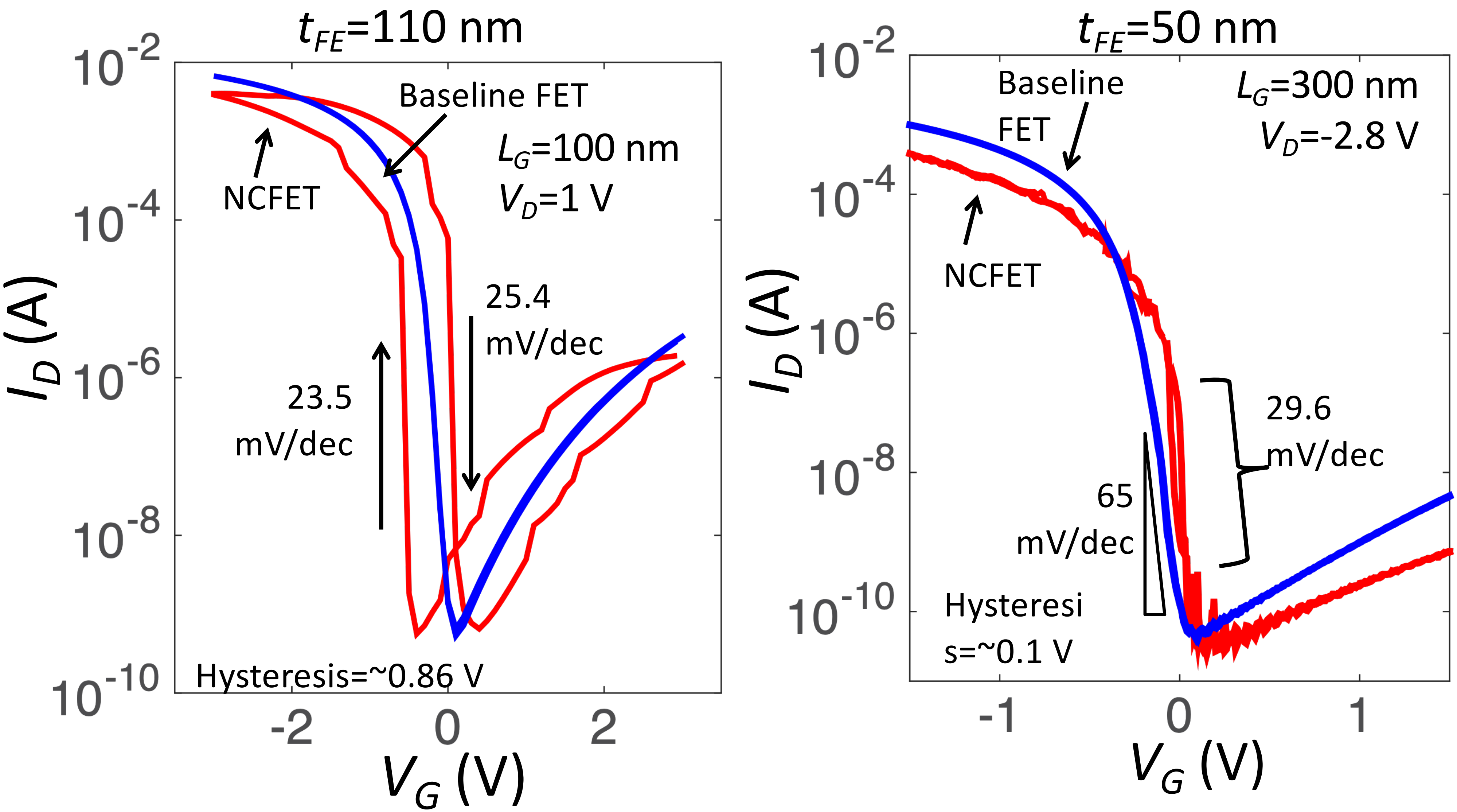


Sharp switching occurs due to ferroelectric negative capacitance!

Negative Capacitance Regions: PQ and RS

Khan et al. IEEE EDL 37, 111 (2016)

Externally Connected NC-FET



Negative capacitance can reduce subthreshold swing below 60 mV/dec!

Khan, Jo et al. (unpublished)

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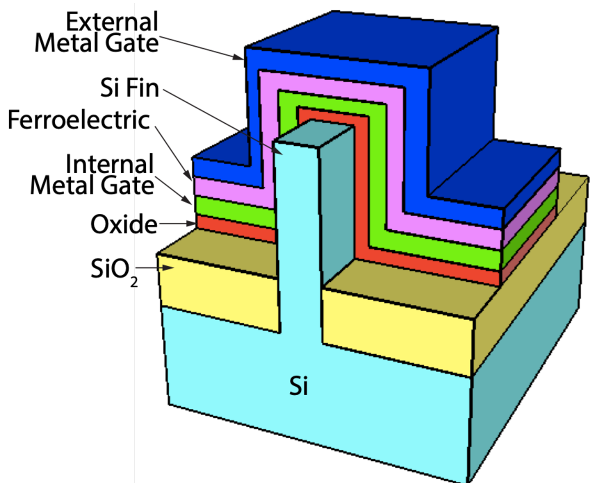
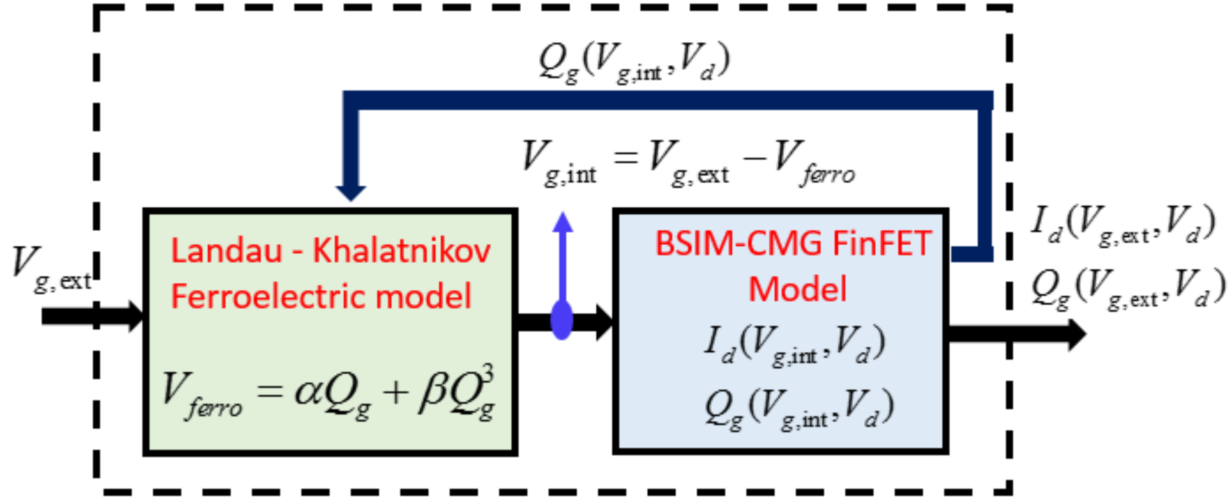
Performance Projection of NCFETs

14 nm FinFET Node

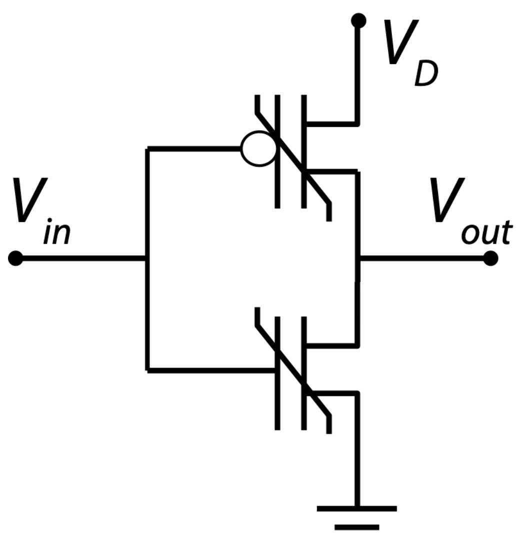


Experiments: Li et al. IEDM 2015

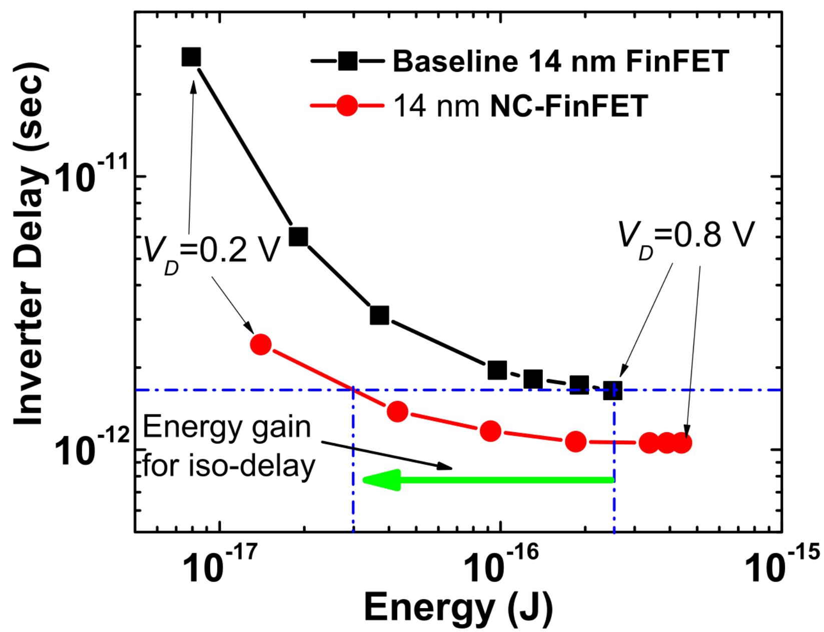
Compact Model



Inverter



Energy-Delay Curve



Significant reduction of energy-delay product is possible with negative capacitance

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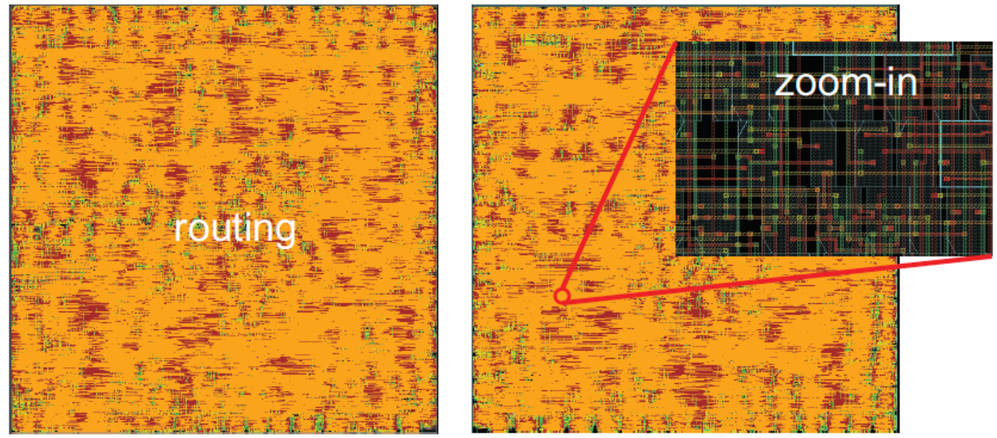
Full Chip Power Benefits of NCFETs

- Advanced Encryption Core (AES) Engine: ~120,000 gates, ~800,000 devices
- Iso-performance analysis (2 GHz)
- Steps:
  - 14 nm NCFET BSIM models based on experimental results (Li et al. IEDM 2015)
  - NCFET-based standard-cell library characterization
  - Full-chip NCFET-based GDSII-level design implementations



baseline FET @ 0.8V NCFET @ 0.4V

Metric	BaseFET@0.8V	NCFET@0.5V	△	NCFET@0.4V	△
WNS (ps)	+3.9	+3.4		+9.3	
Wire switching (mW)	16.5	6.5	-61%	4.6	-72%
Cell-pin switching (mW)	98.0	62.5	-36%	38.2	-61%
Cell internal (mW)	182.2	75.8	-58%	46.6	-74%
Leakage (mW)	6.25	0.94	-85%	0.96	-85%
Total (mW)	**303.0**	**145.8**	**-52%**	**90.4**	**-70%**
Clock (mW)	141.8	62.2	-56%	36.8	-74%
Combinational (mW)	122.1	66.1	-46%	42.9	-65%
Registers (mW)	39.1	17.5	-55%	10.6	-73%

- **70% power saving obtained at 0.4V!**

Samal et al. ISLPED 2017

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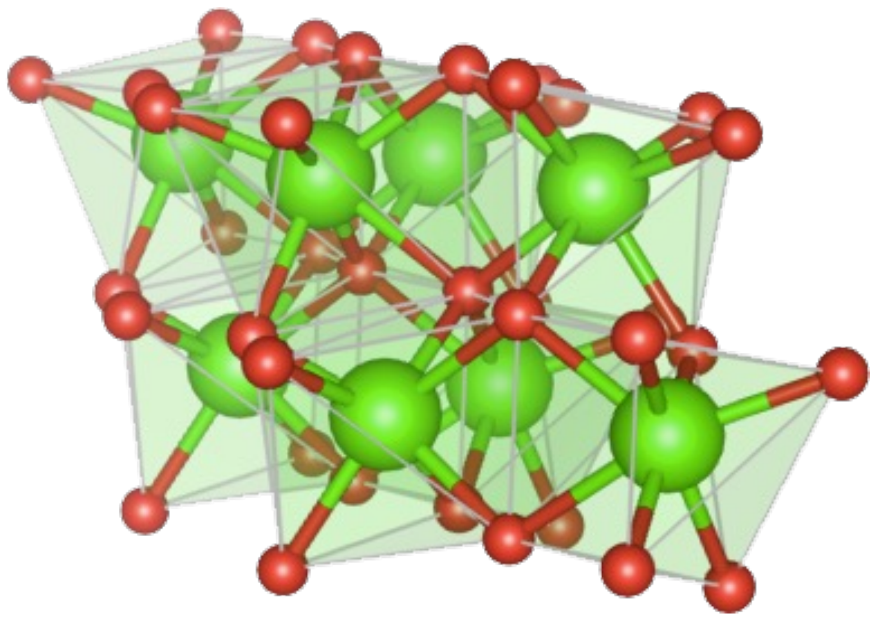
Why am I excited
And
Why everyone can/should
be excited?

New CMOS Compatible Ferroelectrics

New class of ferroelectric materials have emerged which can be introduced in commercial fabs!



Controlled annealing in **HfO_2** doped with Zr, Al, Si, Sr, Ti, La etc. induces a ferroelectric orthorhombic phase!

Commercial Fabs!

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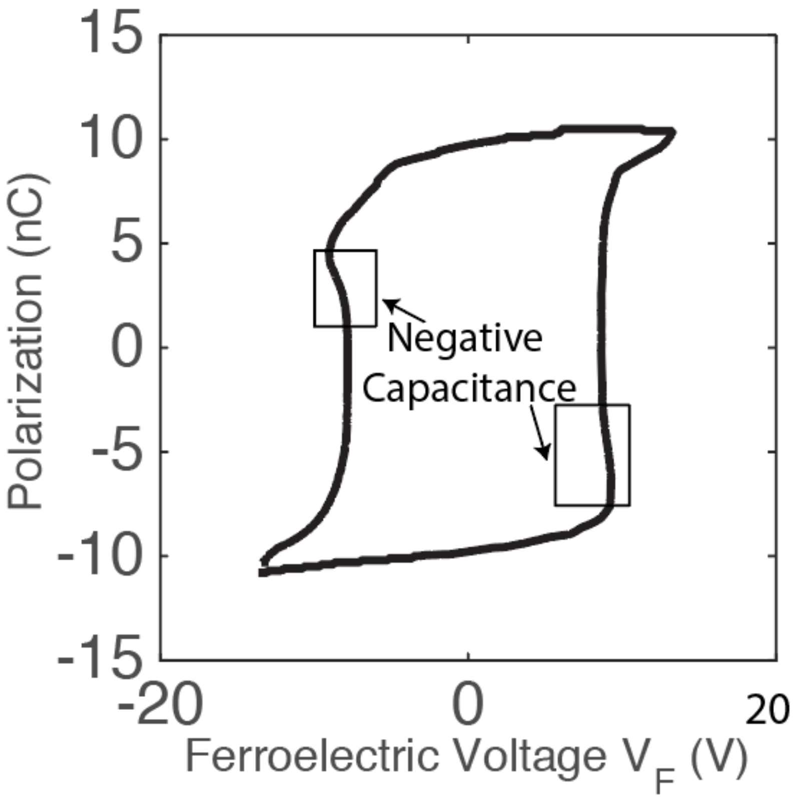
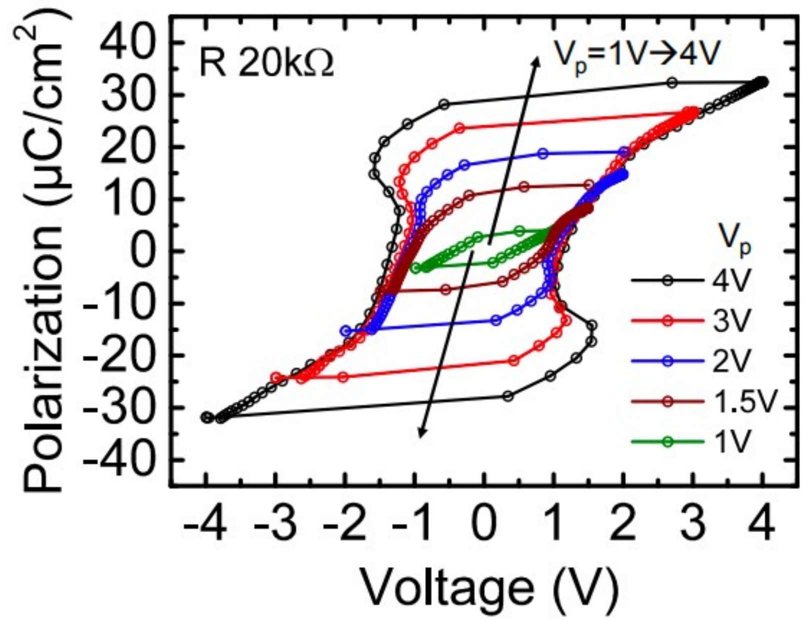
Negative Cap. in Doped HfO_2 Ferroelectrics

Ferroelectric Gd-doped HfO_2 (27 nm)



Hoffmann et al. Direct Observation of Negative Capacitance in Polycrystalline Ferroelectric HfO_2. Advanced Functional Materials 2016.

Ferroelectric $HfZrO_2$ (10 nm)



Kobayashi et al. Experimental study on polarization-limited operation speed of negative capacitance FET with ferroelectric HfO_2. IEDM 2016

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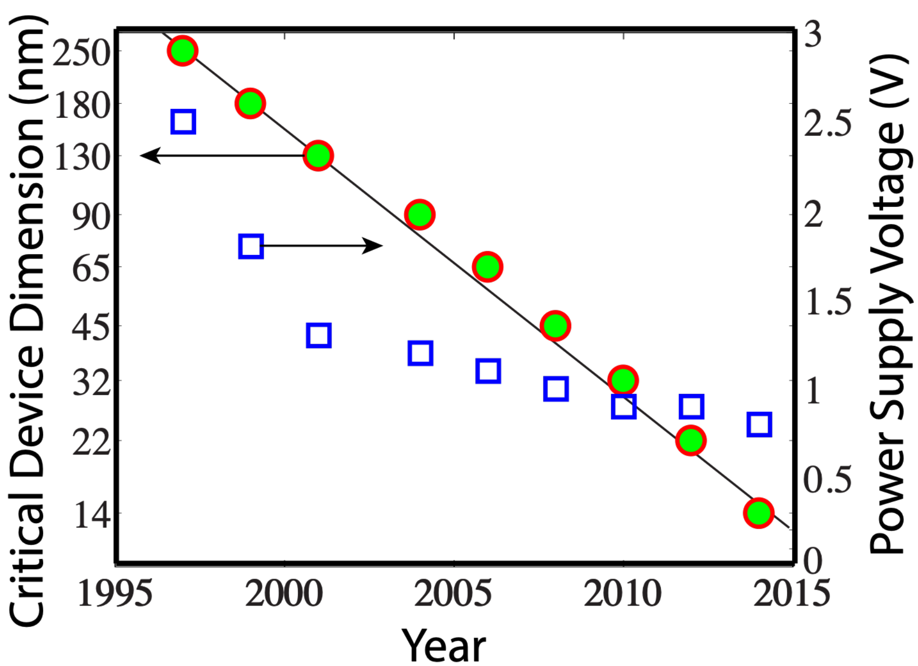
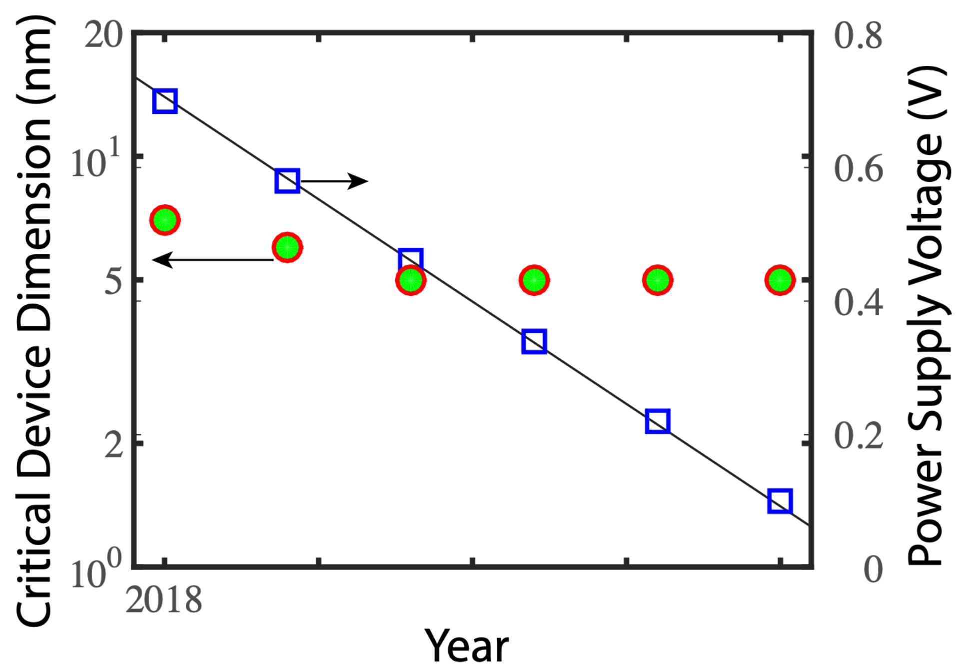
Advanced CMOS with Negative Capacitance

Current CMOS Technology



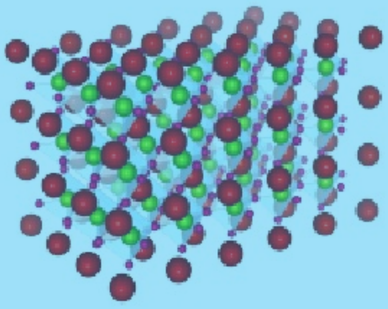
Beyond CMOS with Negative Capacitance



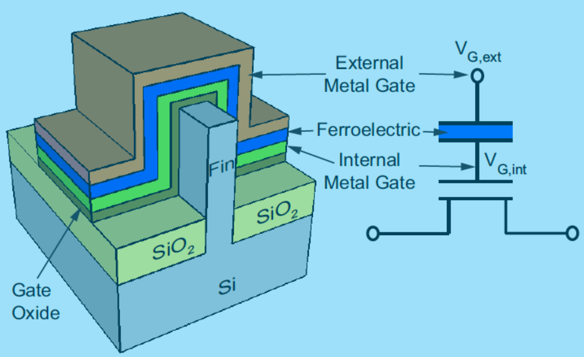
Negative capacitance technology could continue the performance enhancement after scaling ends!

What am I going to do today?

Physics of Negative Capacitance in Materials



Physics of Negative Capacitance Transistors



What do we need to know?

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What do we need to know?

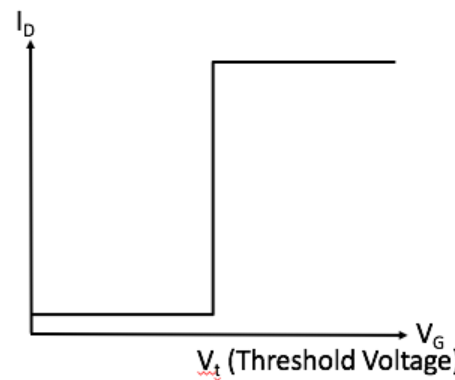
How to design an NCFET? ~0 mV/decade swing?

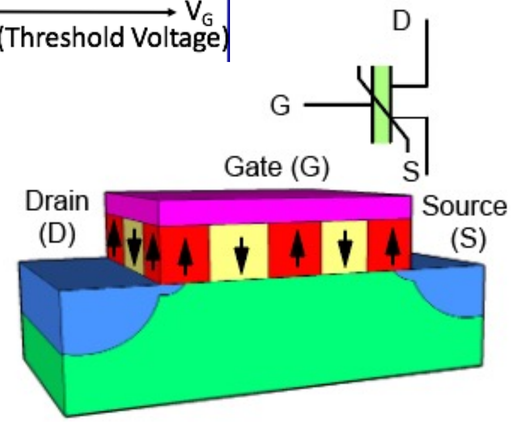
What role does domain dynamics play in negative capacitance?

What is the speed of negative capacitance mechanisms?

Ideal Switch: ~0 mV/decade $\Leftarrow$

$|C_{FE}| \approx C_{MOS}, |C_{FE}| > C_{MOS}$





~ps scale atomic displacement in ferroelectrics: Chen et al. Ultrafast terahertz-field-driven ionic response in ferroelectric BaTiO3. Physical Review B 94, 180104(R) (2016).

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Acknowledgements

People

Sayeef Salahuddin, UC Berkeley
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Uwe Schroeder, NaMLab
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Zheng Wang, Georgia Tech
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Office of Naval Research

STARNET LEAST

NSF E3S Center

FCRP MSD Center

THANKS

QUESTIONS

&

COMMENTS

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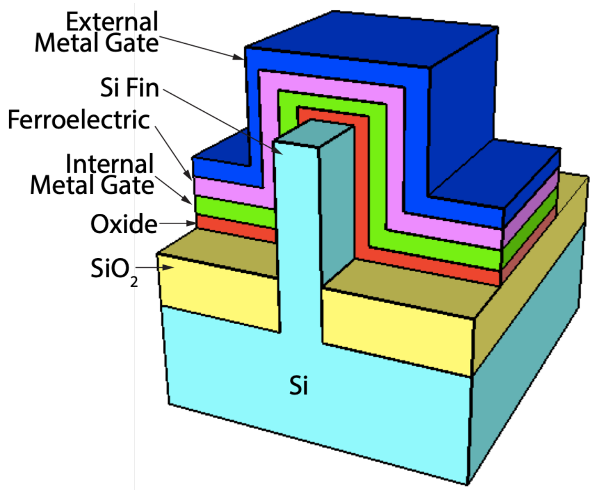
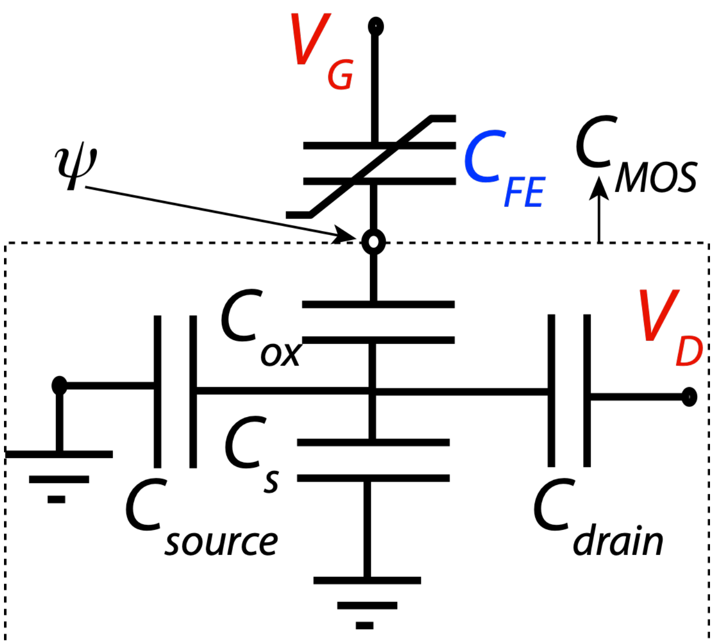
Physics of Negative Capacitance FET

14 nm FinFET Node





Modified Body Factor $m^o = \dfrac{dV_G}{d\psi} = 1 - \dfrac{C_{MOS}}{|C_{FE}|}$ <1

Subthreshold Swing $S = S^{baseline} \times m^o < S^{baseline}$

Input gate capacitance $C_G = \dfrac{C_{G,baseline}}{m} > C_{G,baseline}$

Power $P = \alpha C_L V_{DD}^2 f$

Where does the power benefits come from?

$C_L \uparrow V_{DD} \downarrow\downarrow P \downarrow\downarrow$

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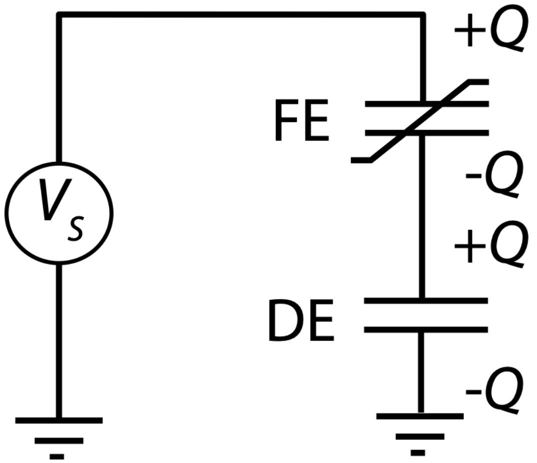
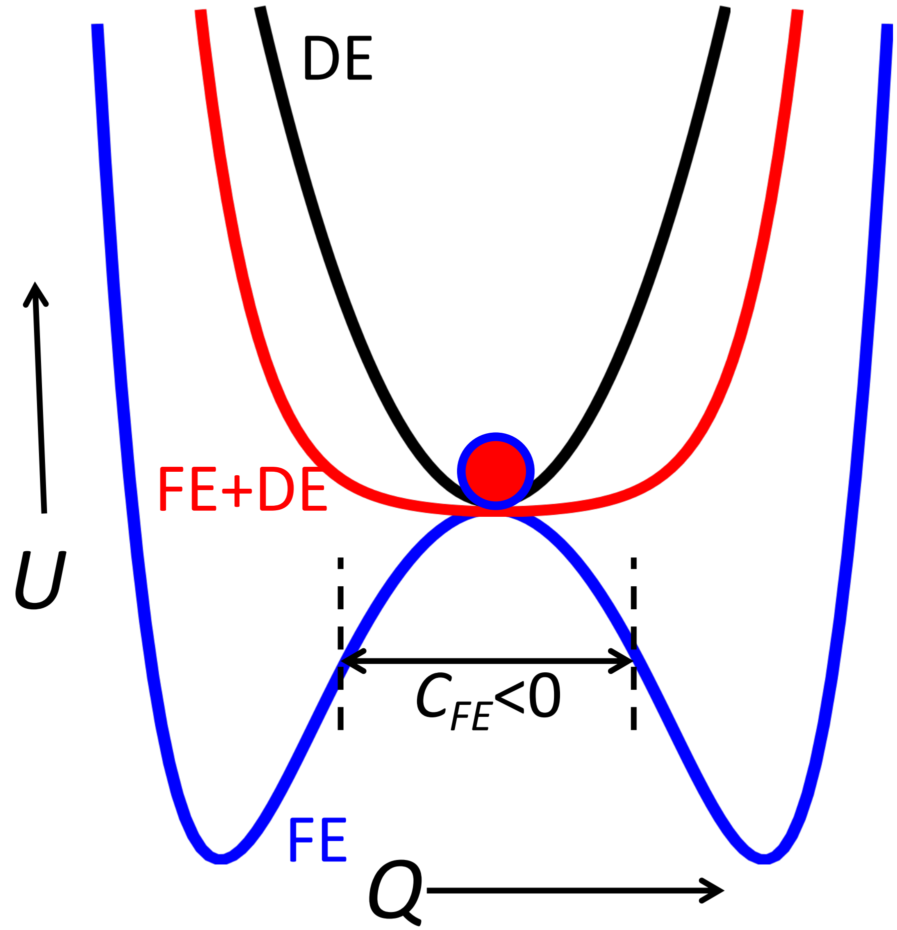
Breaking the Circuit Laws using Neg. Cap.

Ferroelectric-Dielectric Series Combination



$$C = \left[\frac{d^2U}{dQ^2}\right]^{-1}$$

Energy Landscapes



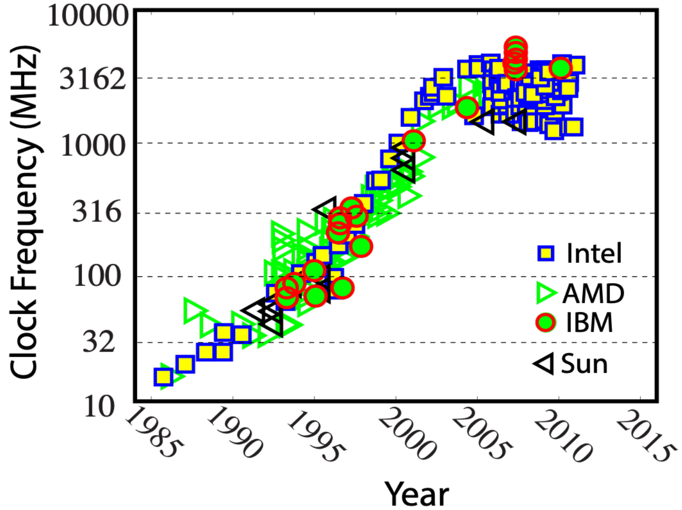
Equivalent Capacitance $C_{FE+DE} = \left[\frac{1}{C_{FE}} + \frac{1}{C_{DE}}\right]^{-1}$

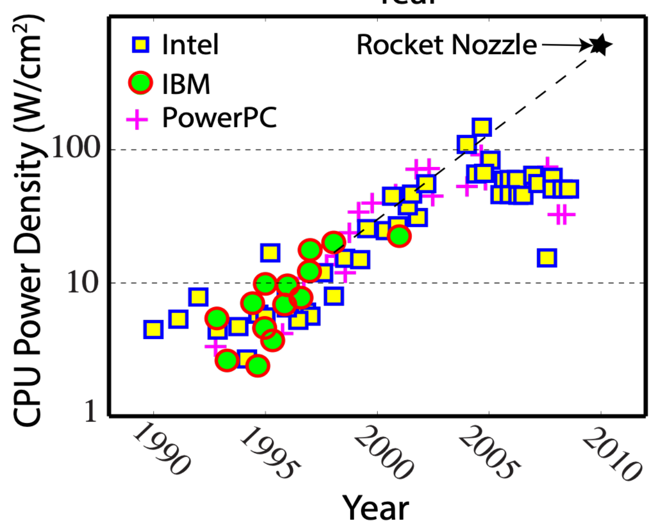
$C_{FE+DE} > C_{DE}$ If $C_{FE} < 0$

Enhancement of capacitance in a FE-DE Series combination!

Energy Challenge in Computing

Clock Frequency Scaling





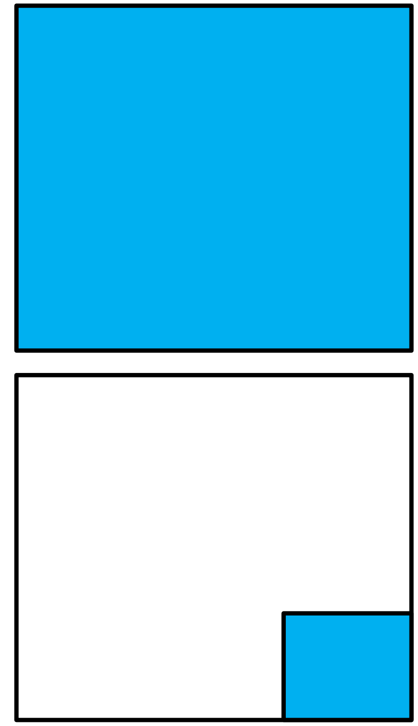
Adapted from: Danowitz et al. Comm. of ACM 55.1 (2012).

Clock frequency has been stuck at ~3 GHz since 2005.

Dark Silicon

45 nm
(2008)
100% active

7 nm
(2022)
10% active



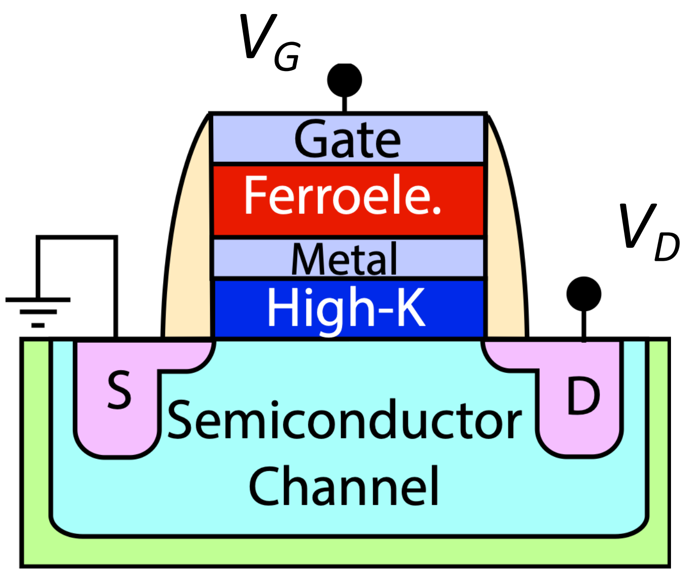
Only a small fraction of the chip can be powered on!

There is a fundamental energy challenge for computing!

What do we need to know?

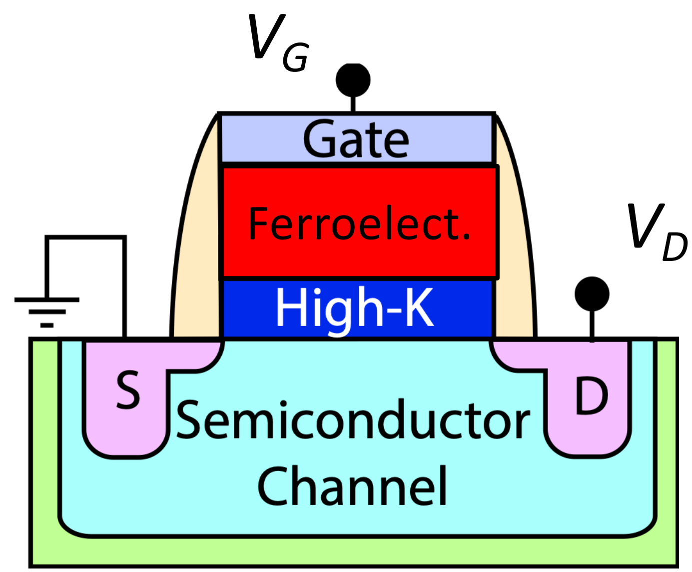
How to design an NCFET?
$\sim$0 mV/decade swing?

With Internal metal



OR

No Internal metal



Khan et al. A Simulation Study of Negative Capacitance Field-Effect Transistors: The Effects of Leakage through Ferroelectric Negative Capacitor. IEEE Trans. Electron Dev. 63, 4416 (2016).

$\sim$0 mV/decade swing: Make $|C_{FE}|=C_{MOS}$ >>Parasitic capacitances help!

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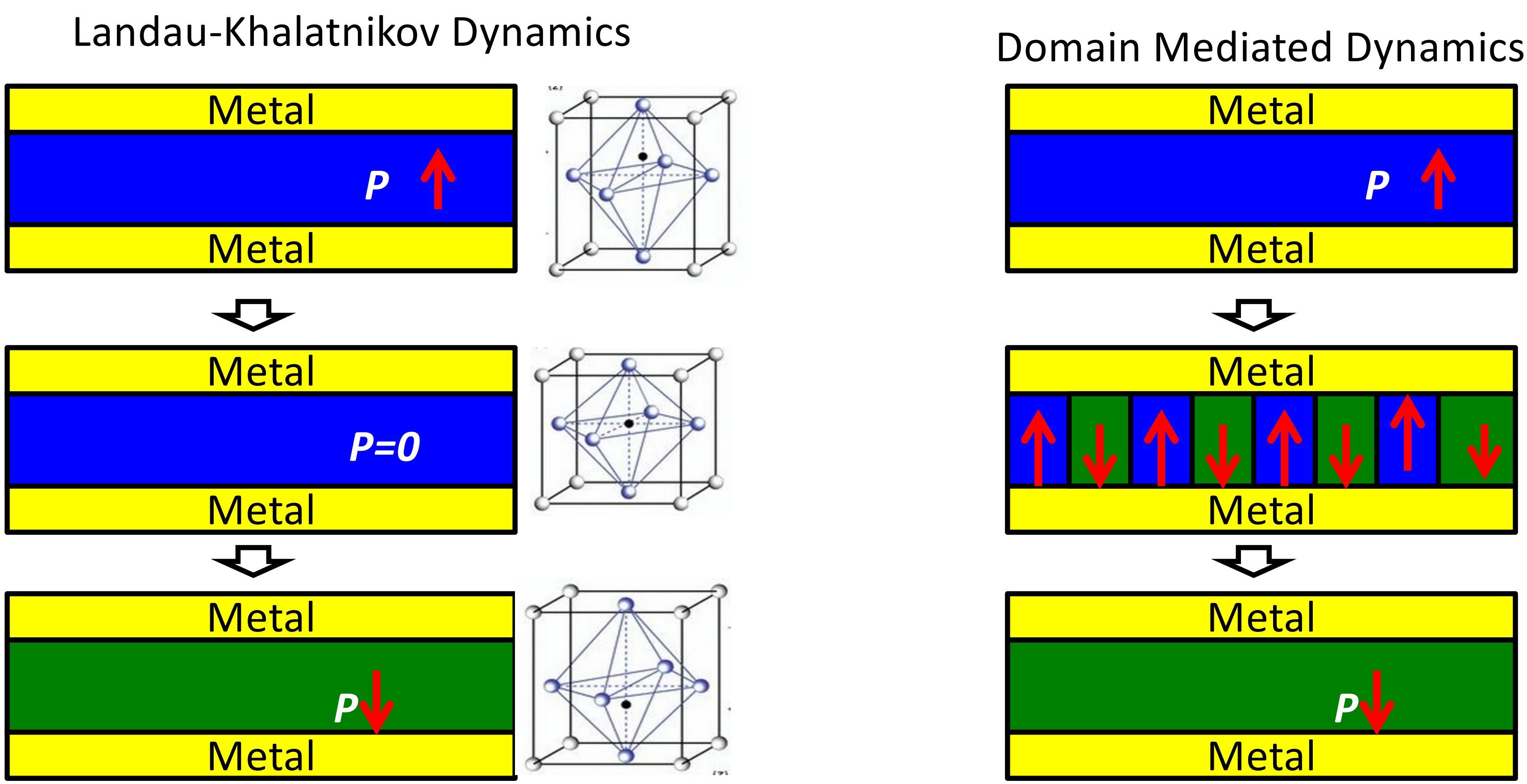
Effects of Domain Mechanisms



The Negative Capacitance effect is present even though the ferroelectric does not switch in a single domain fashion.

Speed

What is the speed of negative capacitance mechanisms?

1. **10-100 ns in HFO2 FETs**
Müller et al. Nanosecond Polarization Switching and Long Retention in a Novel MFIS-FET Based on Ferroelectric HfO2. IEEE Electron Devices Letters33, 185 (2011).

2. ~220 ps in micron size PZT capacitors:
Li et al. Ultrafast polarization switching in thin-film ferroelectrics. Applied Physics Letters 84, 1175 (2004).

3. ~ps scale atomic displacement in BaTiO3:
Chen et al. Ultrafast terahertz-field-driven ionic response in ferroelectric BaTiO3. Physical Review B 94, 180104(R) (2016).

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