Ultra-Low Power Computing with New Materials:

Ferroelectrics for Logic, Memory and Neuromorphic Applications

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FCRP MSD Center

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Computing and Global Challenges

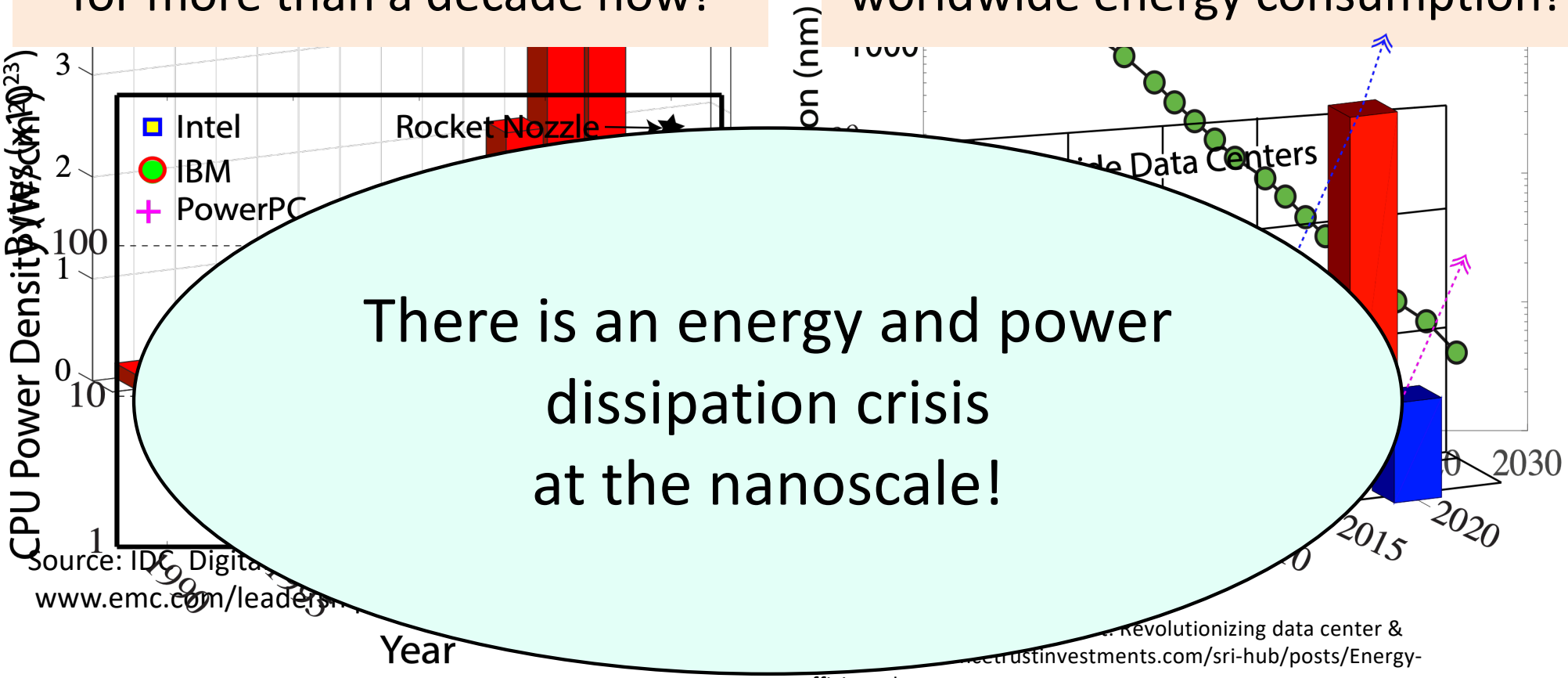
Computable data grows 50x every ten year!

Extreme scaling has been the driver!

Clock frequency stuck at 3 GHz for more than a decade now!

Computing constitutes 2-5% of worldwide energy consumption!

There is an energy and power dissipation crisis at the nanoscale!



Source: IDC Digita… www.emc.com/leaders…

Adapted from: Danowitz et al. Comm. of ACM 55.1 (2012).

…Revolutionizing data center & …electrustinvestments.com/sri-hub/posts/Energy-efficient-data-centres

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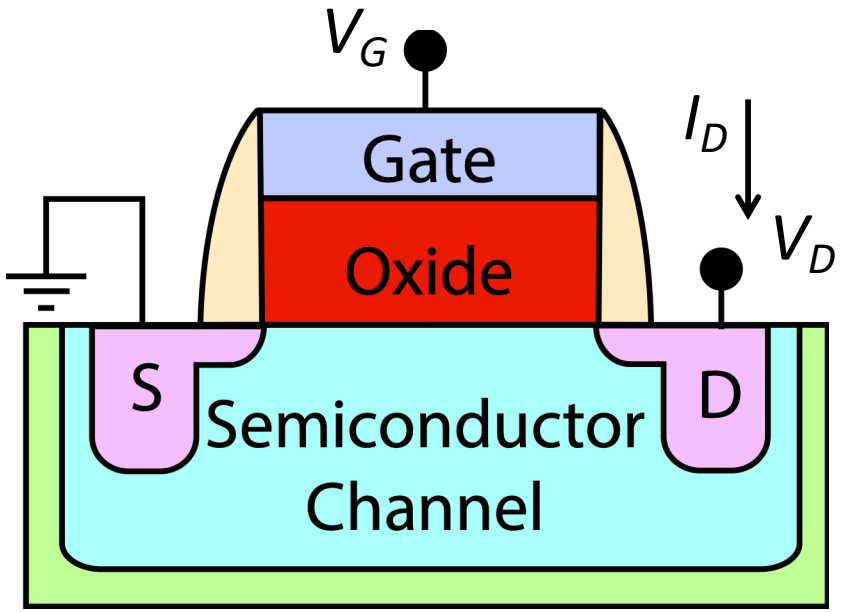
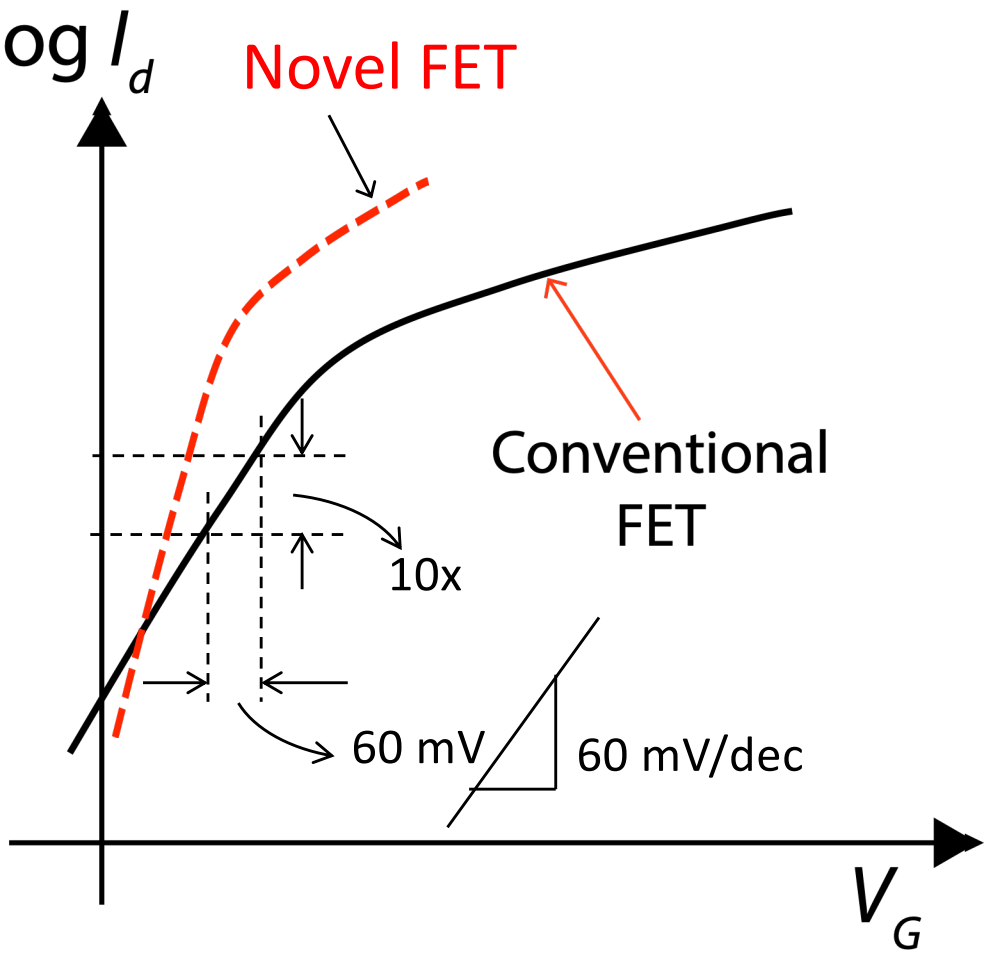
Energy Challenge in Computing





Boltzmann distribution dictates that Channel charge, $Q \alpha e^{\frac{q\psi_s}{k_B T}}$

Minimum Subthreshold Swing

$$S_{\min} = \frac{k_B T}{q}\log_e(10) = 60mV/dec$$

We are in search of an Ultra-low Power MOSFET!

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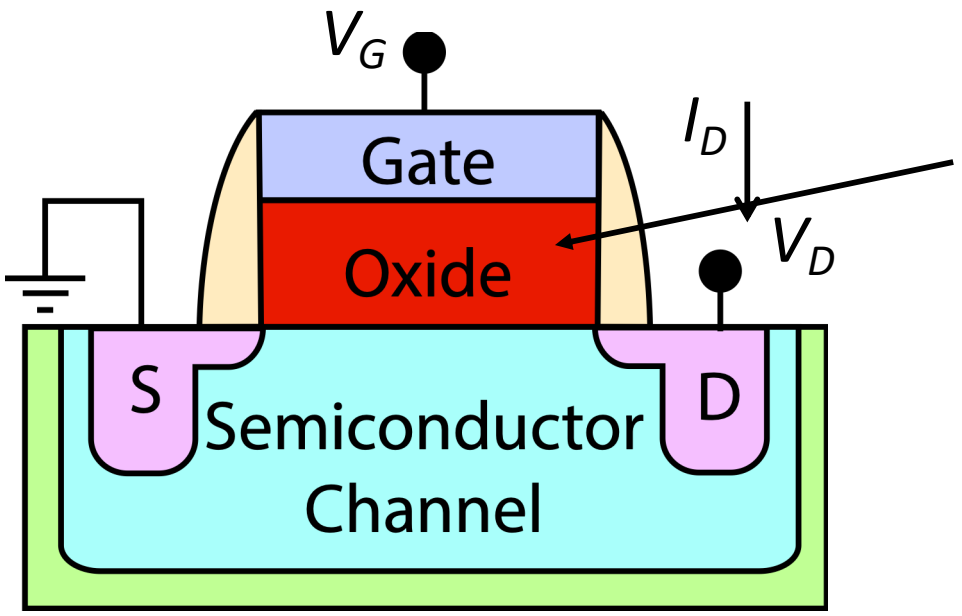
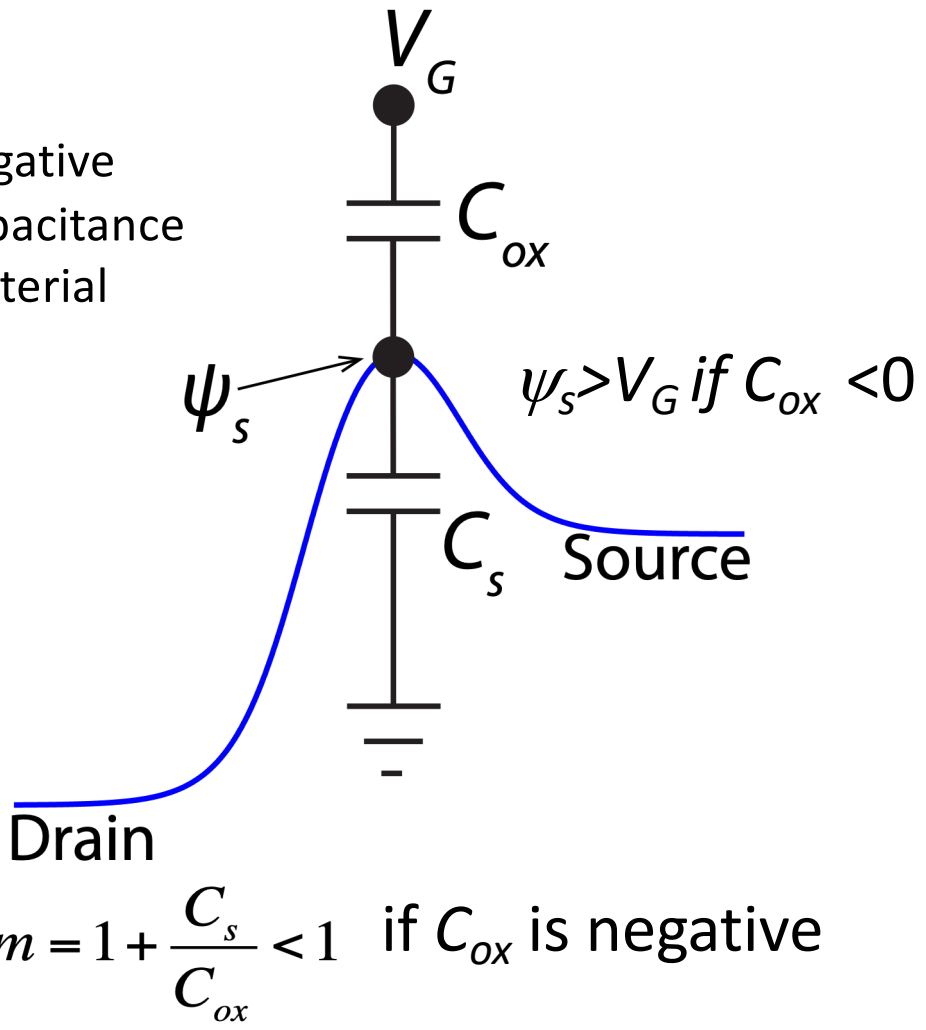
The Negative Capacitance Approach





Subthreshold Swing

$$S = \frac{\partial V_G}{\partial(\log_{10} I_D)} = \frac{\partial V_G}{\underbrace{\partial \psi_s}_{\equiv m}} \frac{\partial \psi_s}{\partial(\log_{10} I_D)} = m \times 60 \text{ mV/decade}$$

Body Factor

$$m = \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_s}{C_{ox}}$$

$$m = 1 + \frac{C_s}{C_{ox}} < 1 \quad \text{if } C_{ox} \text{ is negative}$$

Negative capacitance can result in a $S < 60$ mV/decade

Salahuddin et al. Nano Lett. 8, 405 (2008)

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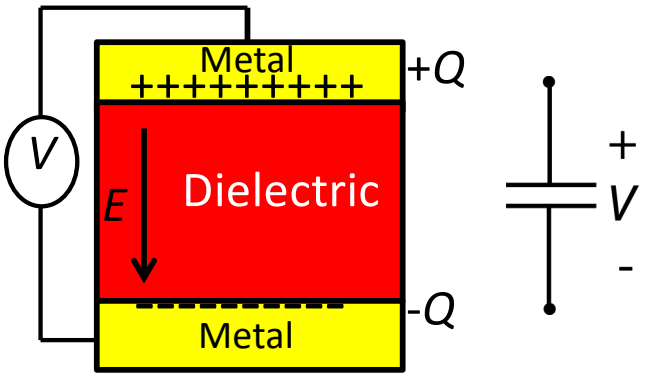
Capacitance: Positive and Negative

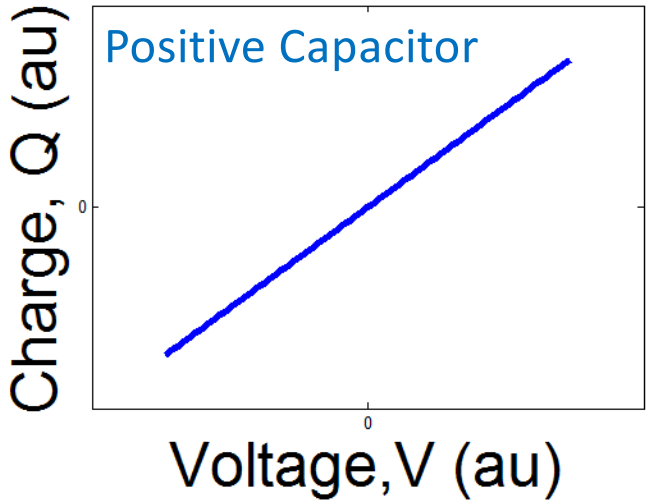


Capacitance $C = \frac{dQ}{dV}$

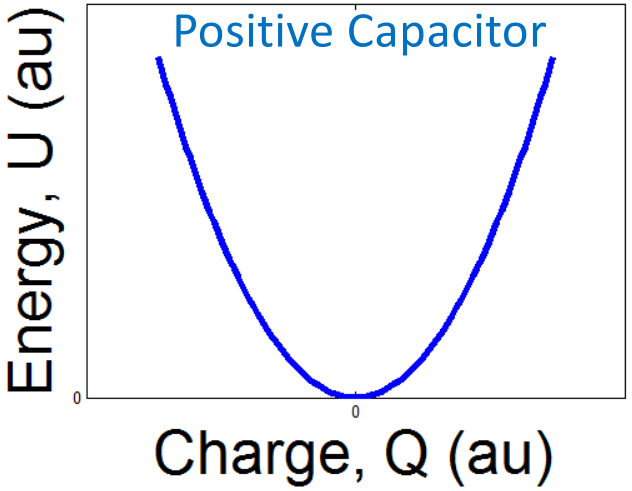
Stored Energy $U = \frac{Q^2}{2C}$

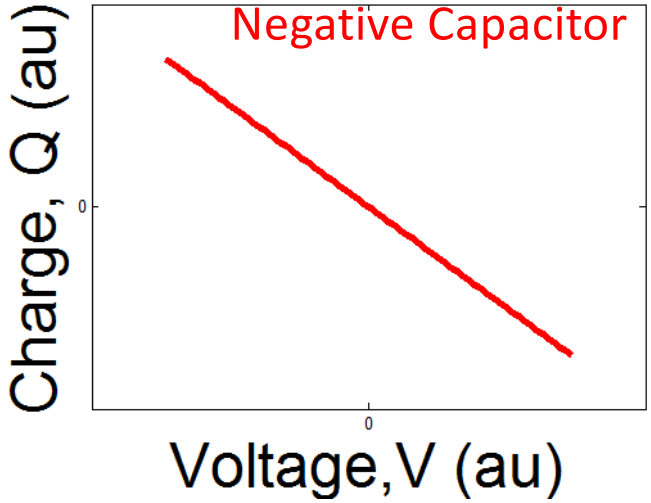
$$C = \left[\frac{d^2U}{dQ^2}\right]^{-1}$$

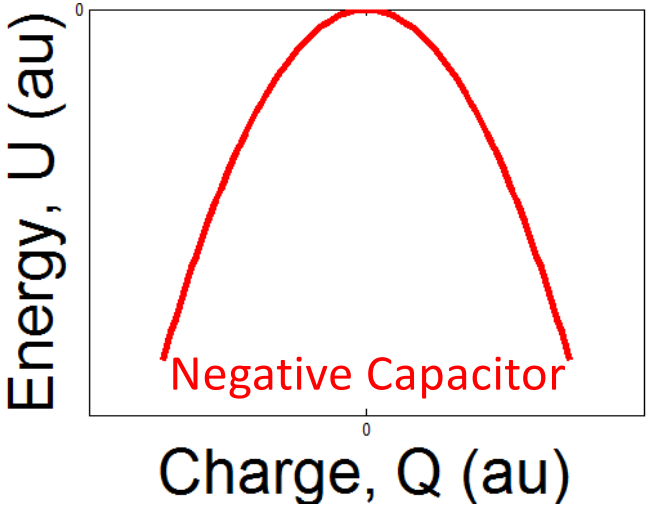
Q-V Characteristics



Q-U Characteristics (Energy Landscape)







C is inverse of radius of curvature of energy landscape

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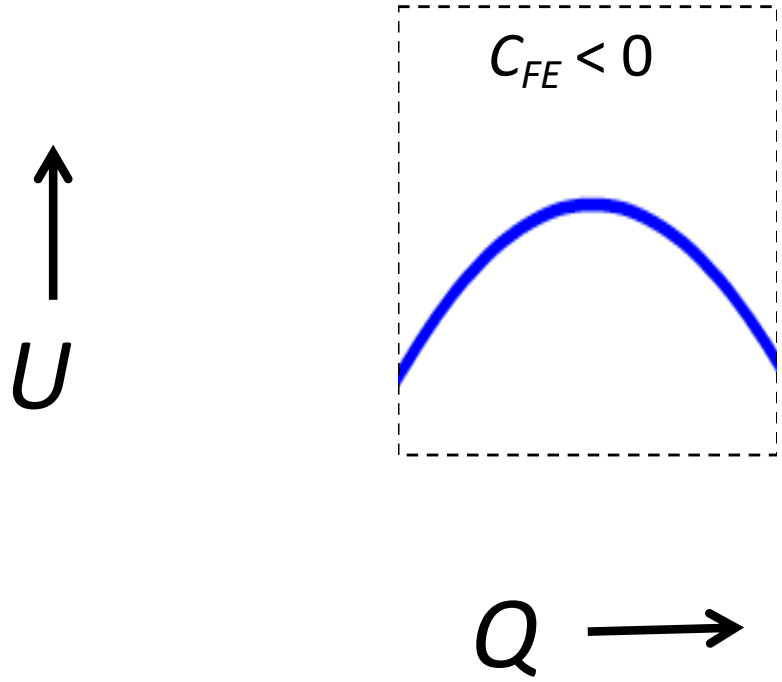
How to get Negative Capacitance Material



Landau Theory of Ferroelectrics

Free energy of a ferroelectric

$$U = \alpha Q^2 + \beta Q^4 + \gamma Q^6; \alpha < 0$$

α, β, γ = Anisotropy Constants
Q = Charge

According to the Landau theory of ferroelectric, ferroelectric oxides could give an effective negative capacitance

Landau & Khalatnikov. Dokl. Akad. Nauk 96, 85 469472 (1954).

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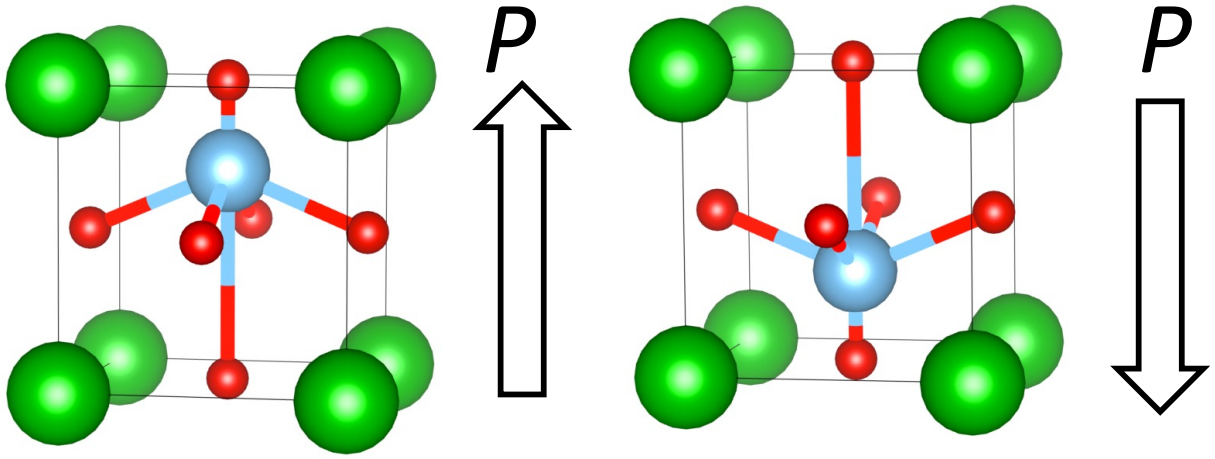
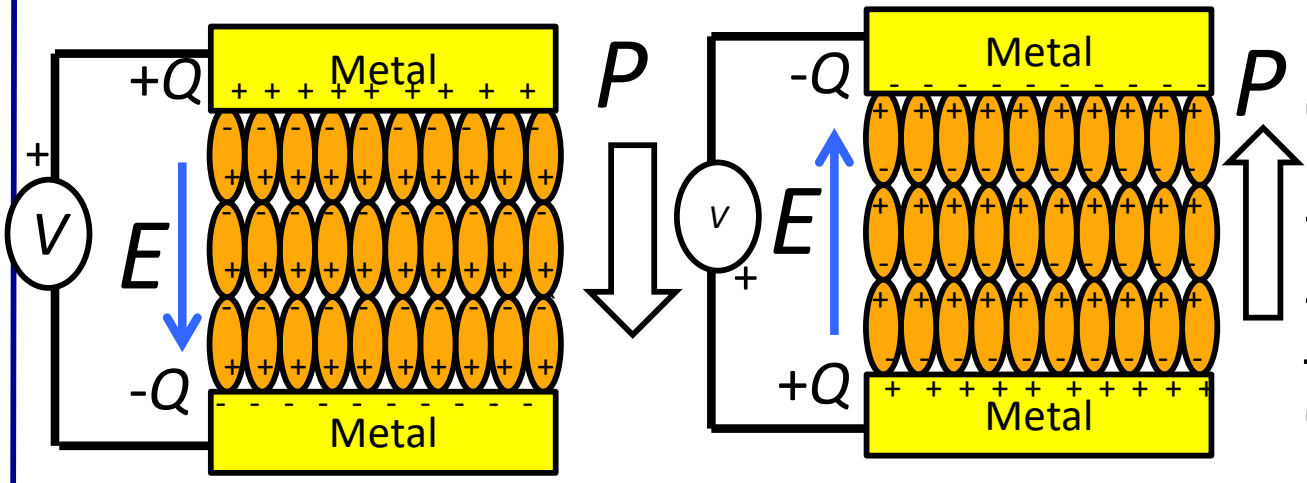
Ferroelectric Oxides

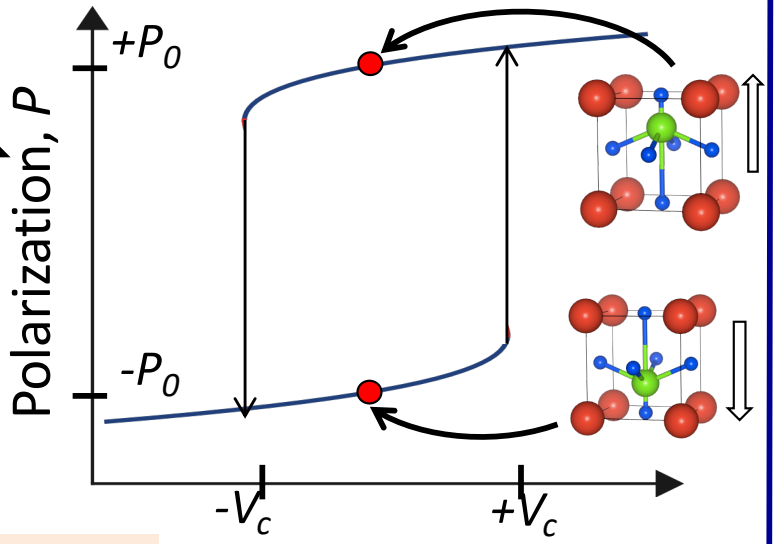
Classical Ferroelectric

$PbTiO_3$ ($Pb^{2+}Ti^{4+}O_3^{6-}$)

Pb^{2+} Ti^{4+} O^{2-}







A ferroelectric is an insulator with a spontaneous polarization, which can be switched by an above coercivity voltage .

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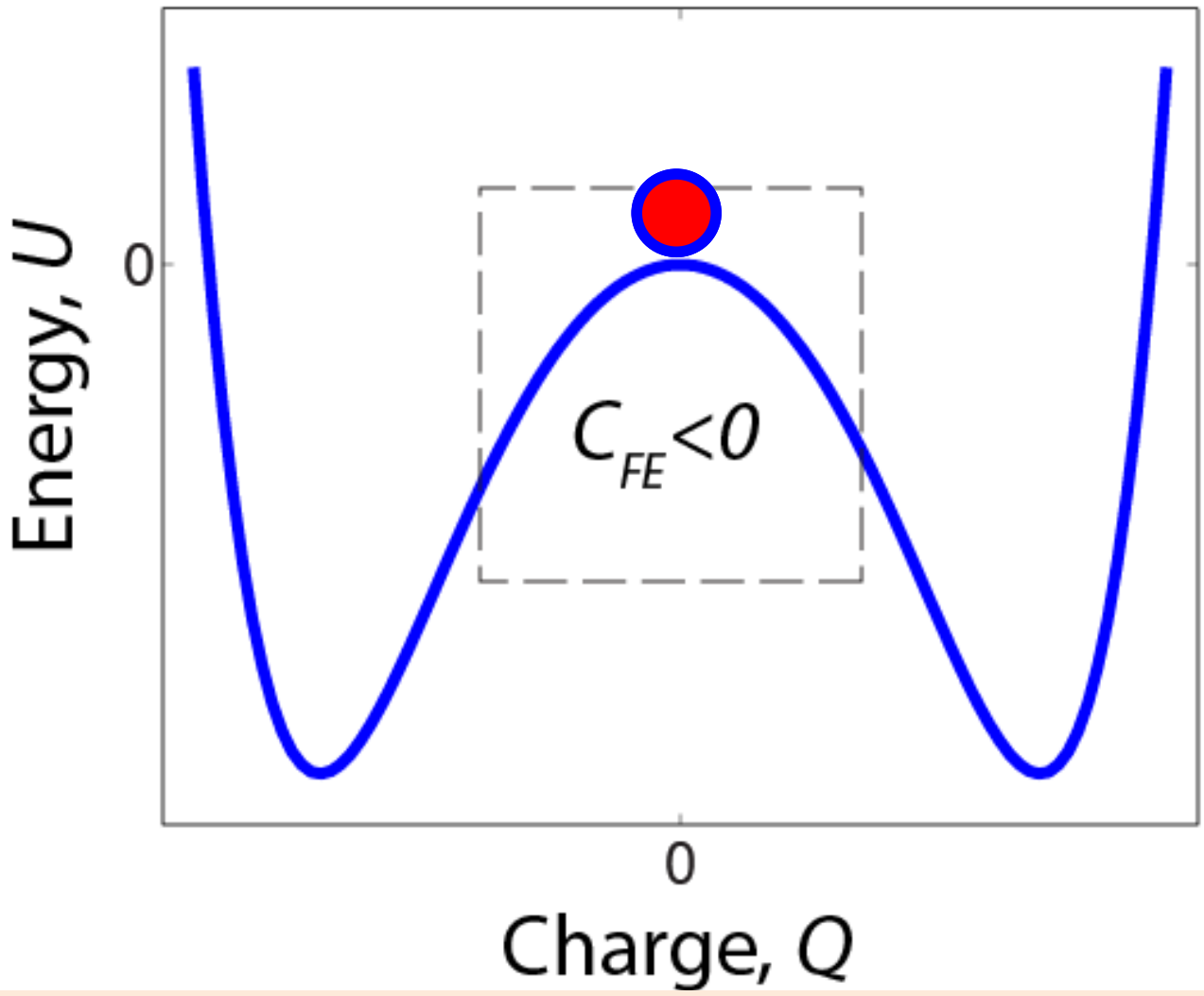
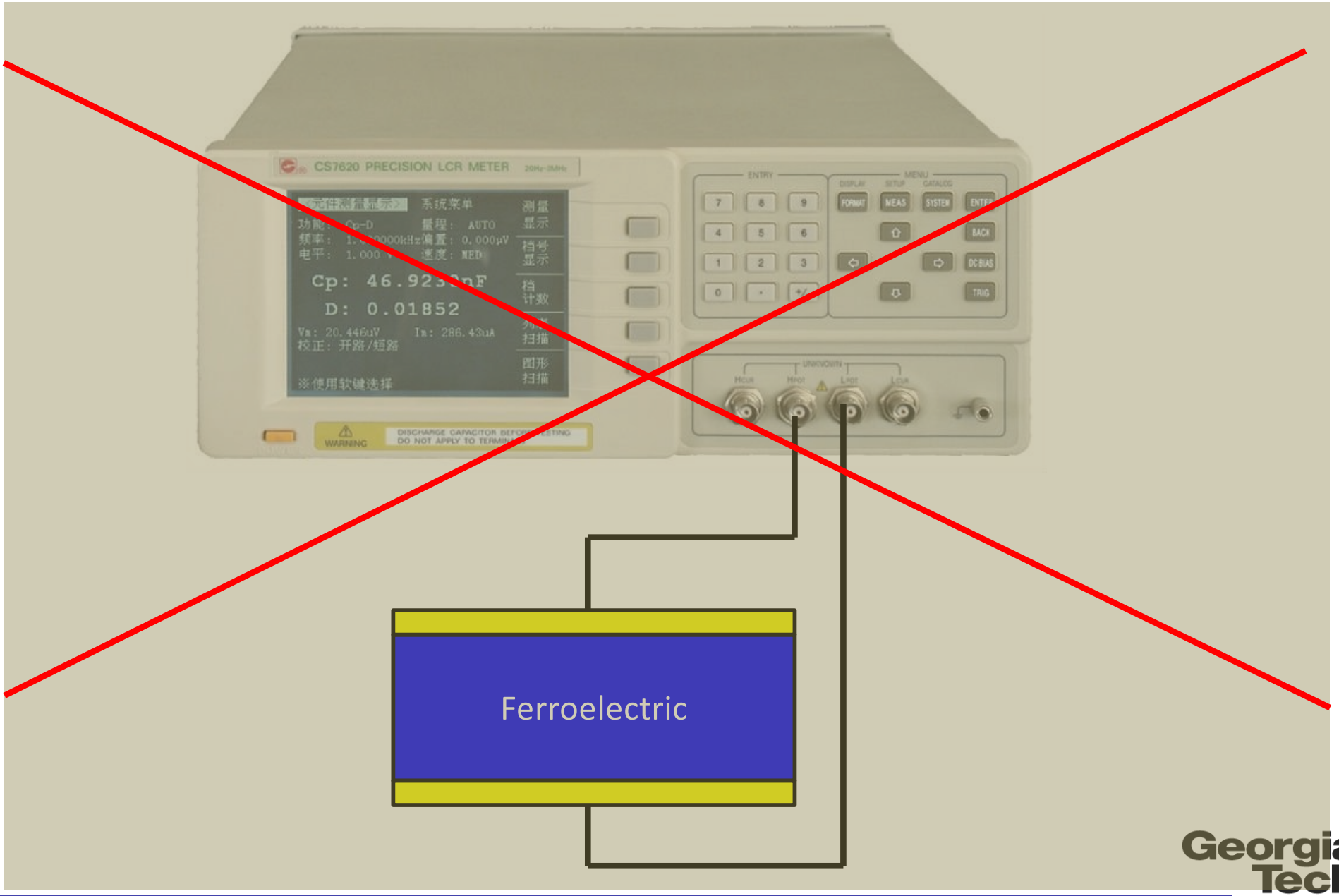
Why is it difficult to measure?

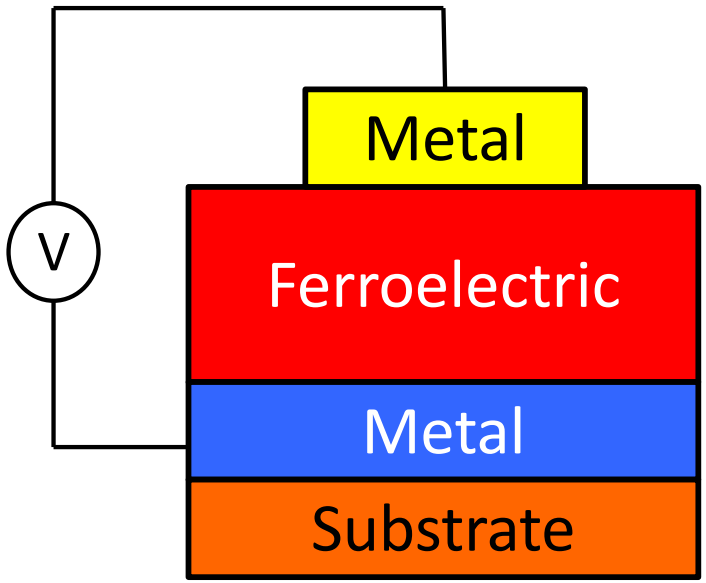


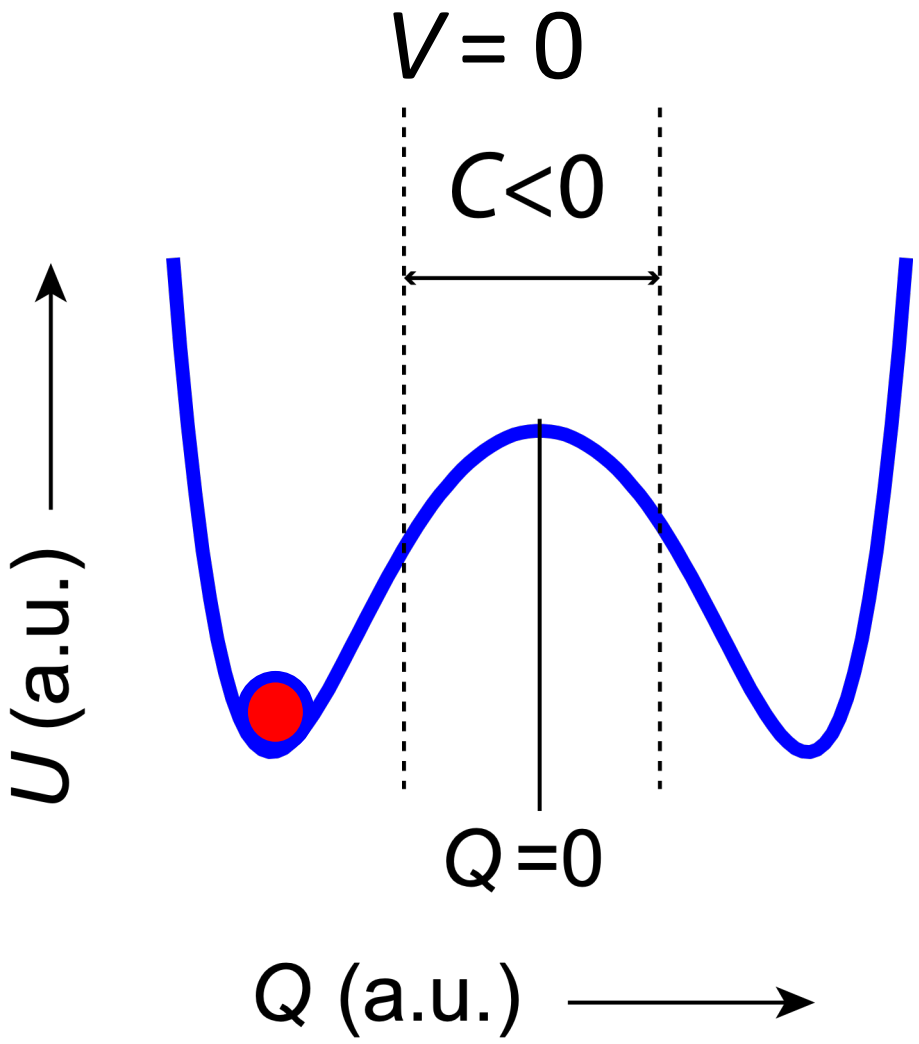
Ferroelectric Negative Capacitance is unstable and cannot be accessed in a time independent equilibrium measurement.

Why is it difficult to measure?



Direct Measurement of Negative Capacitance





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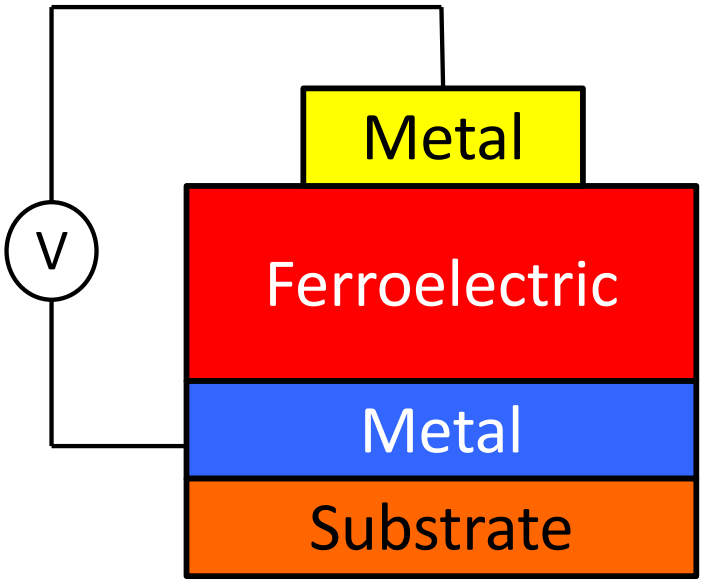
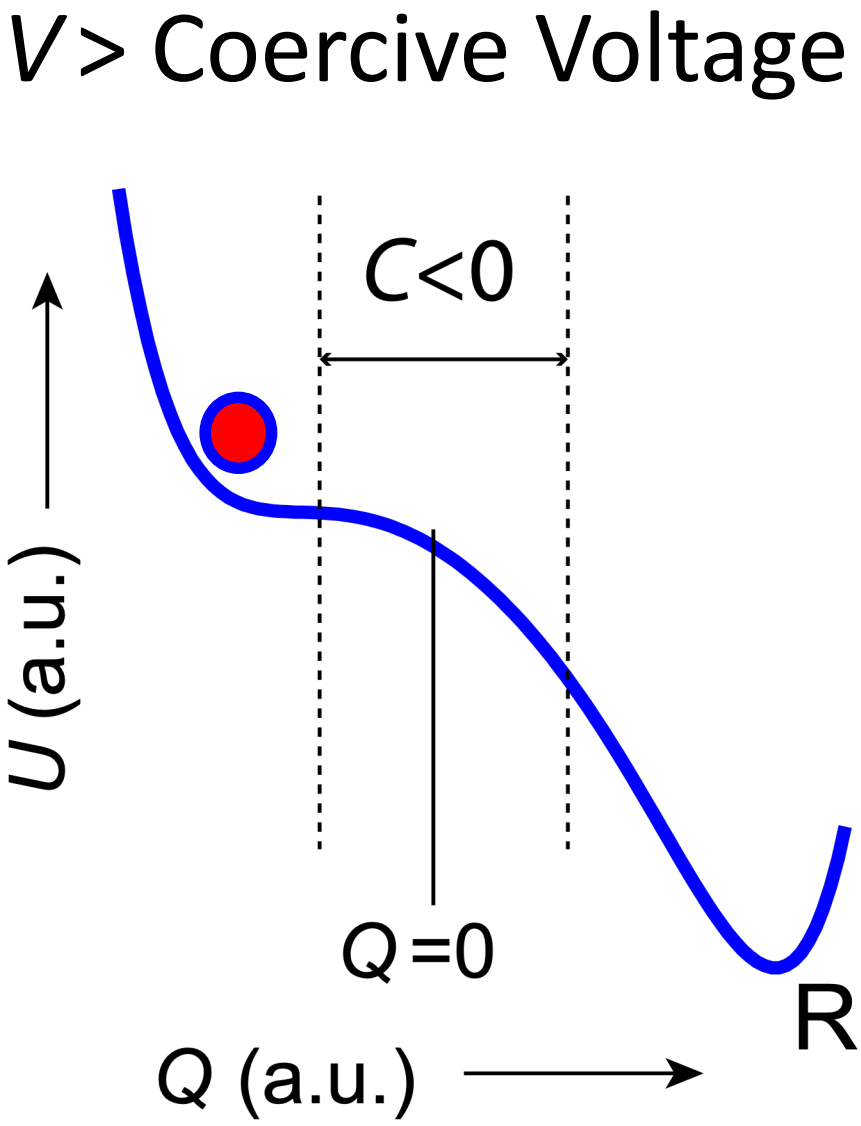
Direct Measurement of Negative Capacitance



A ferroelectric capacitor goes through the unstable negative capacitance states during switching.



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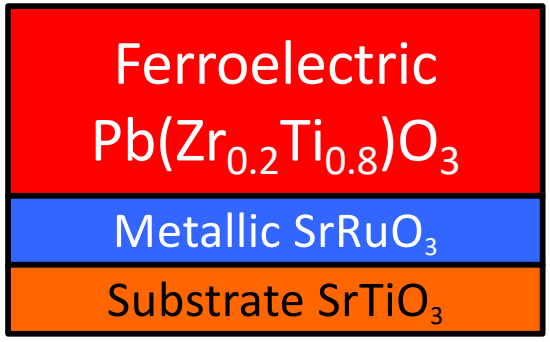
Growth of Ferroelectric Oxides

Experimental Heterostructure



In-plane lattice parameter

a_{PZT}=0.393 nm

a_{SRO}=0.394 nm

a_{STO}=0.3905 nm

Pulsed laser deposition technique

Typical Growth Conditions:

$SrRuO_3$: 720°C, 100 mTorr, 1.2 J/cm^2, 5-15 Hz

$Pb(Zr_{0.2}Ti_{0.8})O_3$: 630 °C, 100 mTorr, 1-1.5 J/cm^2, 5-15 Hz

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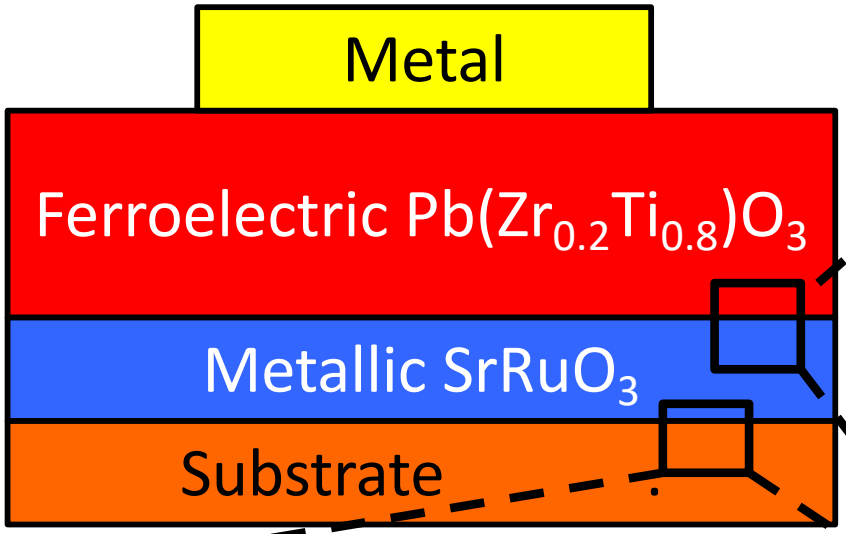
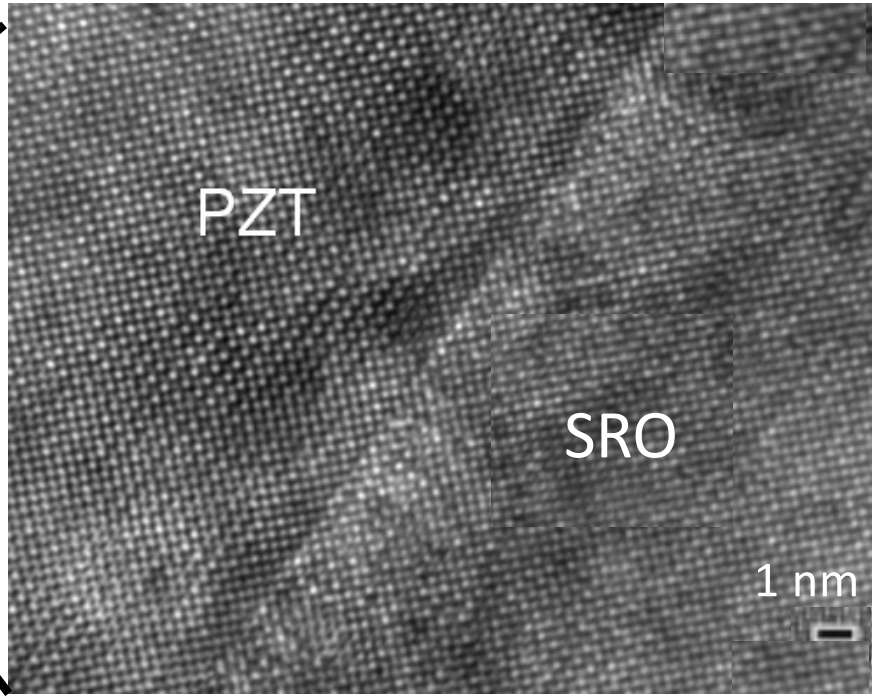
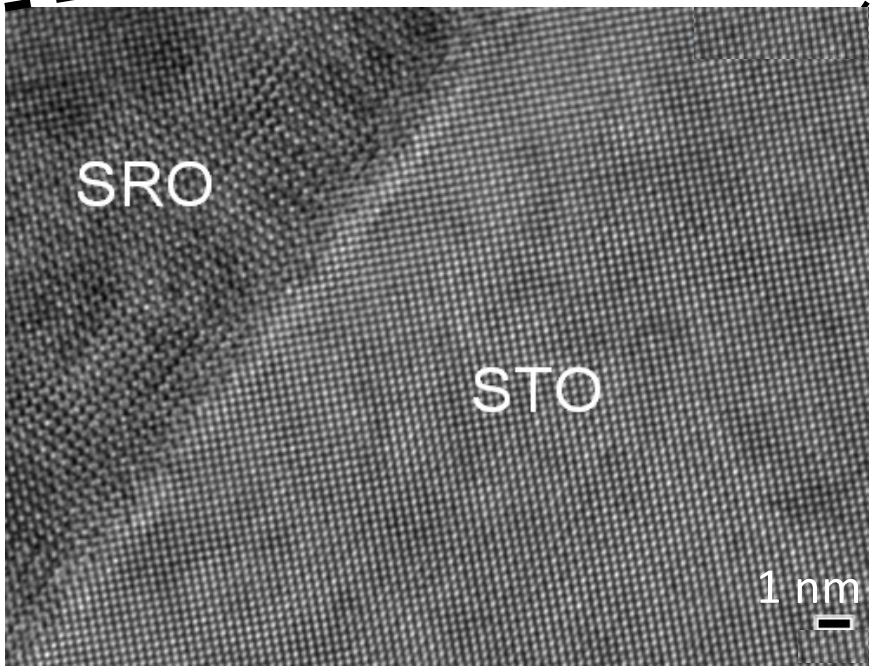
Ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$







Courtesy: Pan group, U. Mich.

Excellent epitaxial quality!

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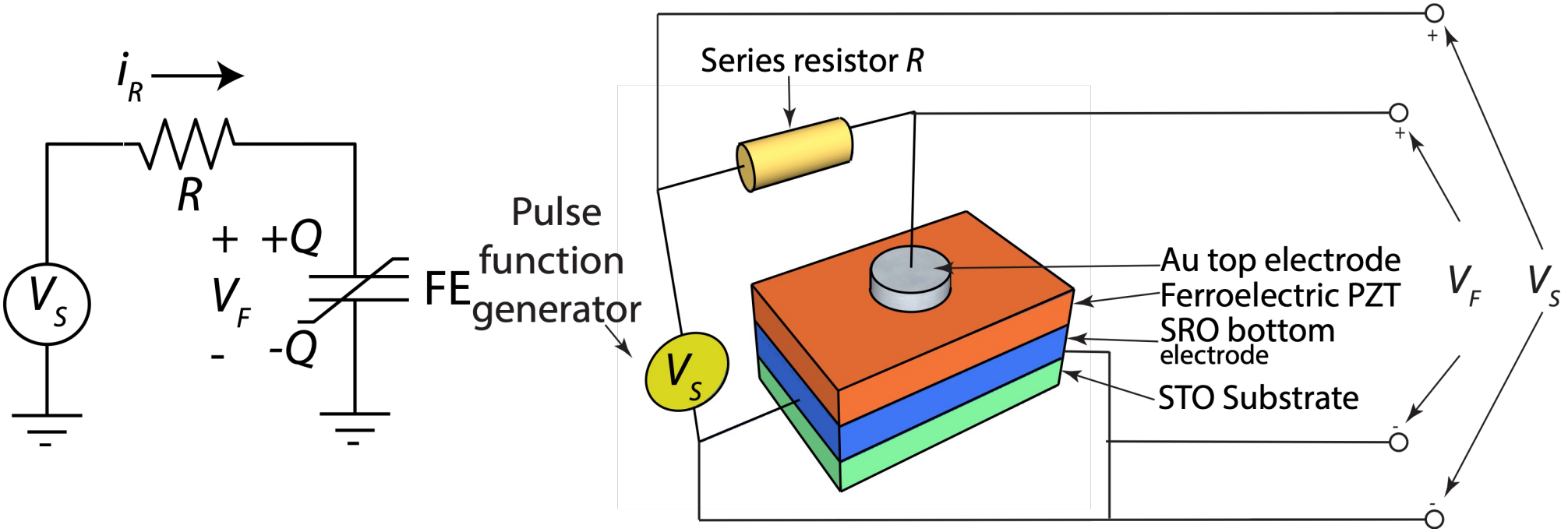
Direct Measurement of Negative Capacitance



A ferroelectric capacitor connected in series with an external resistor.

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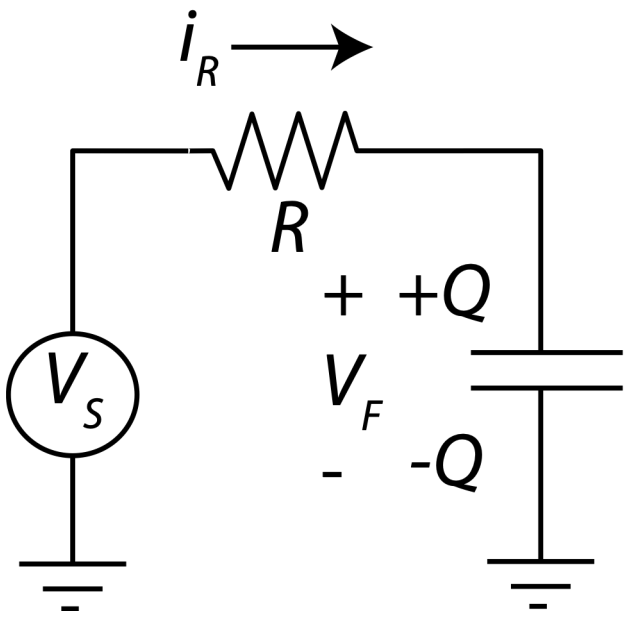
What happens in an *R-C* Series circuit?

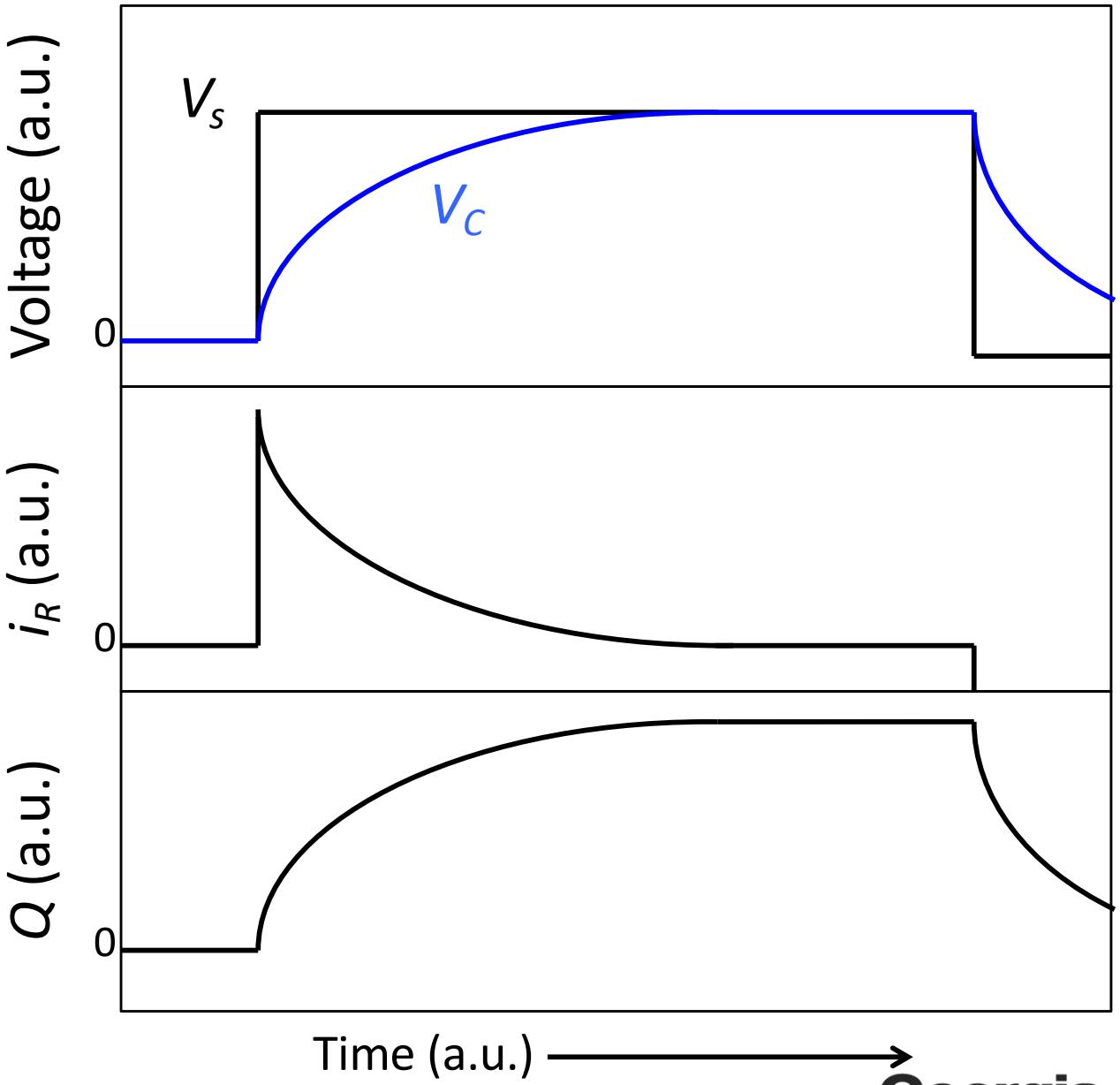


Voltage: $V_C=V_S(1-e^{-t/RC})$

Current: $i_R=V_S e^{-t/RC}/R$

Charge: $Q=CV_S(1-e^{-t/RC})$

At any time t,
$dQ/dV_C=C>0$.



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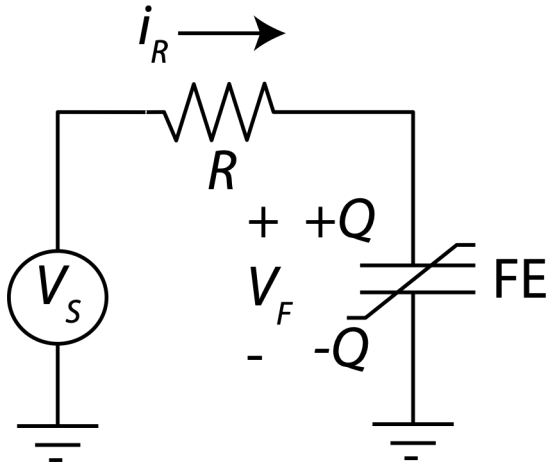
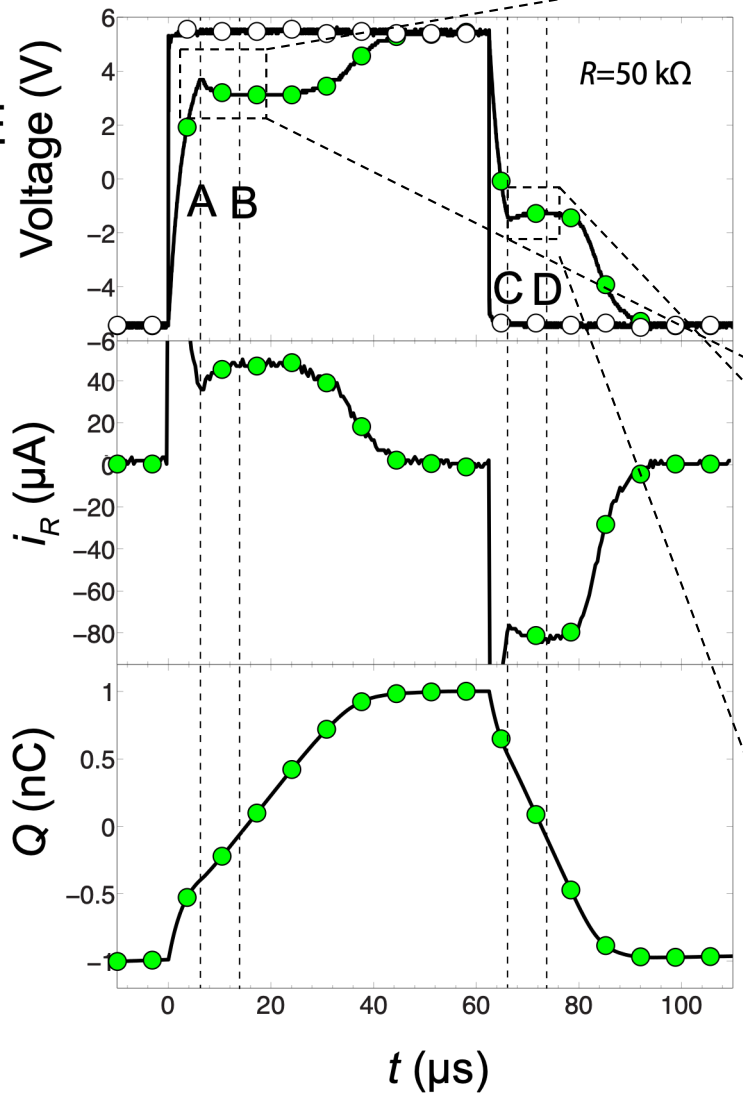
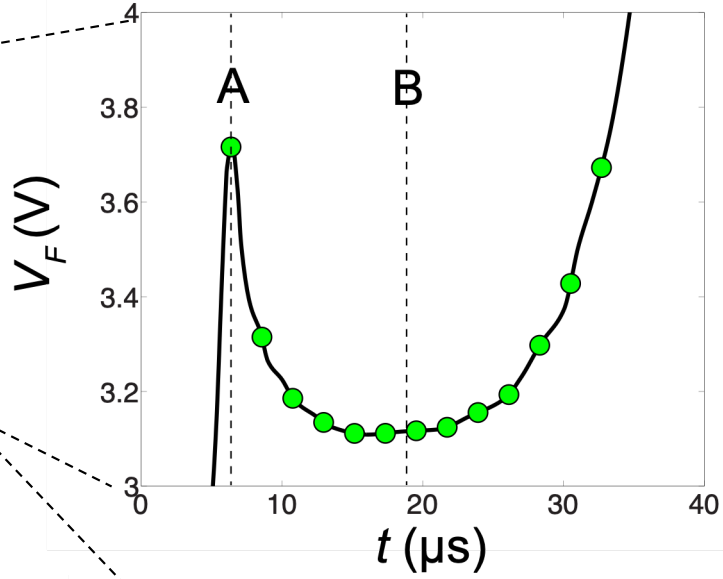
Direct Measurement of Negative Capacitance

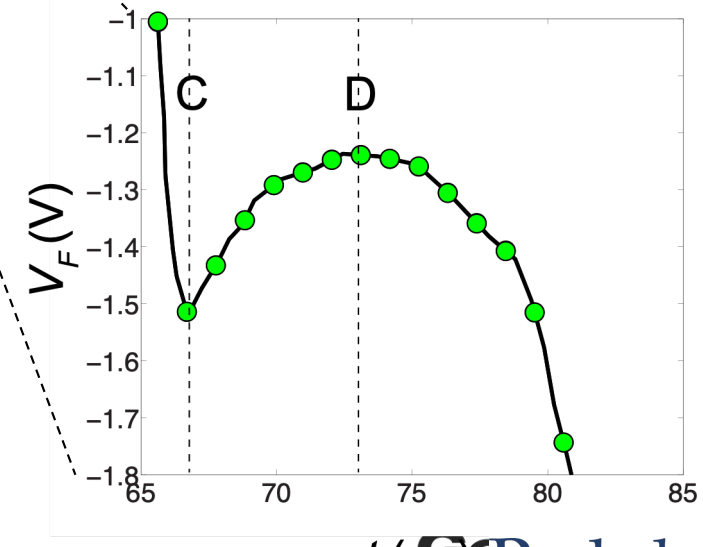
60 nm $Pb(Zr_{0.2}Ti_{0.8})O_3$) (Coercive voltage=~2.5 V)

V_s: -5.4 V → +5.4 V → -5.4 V





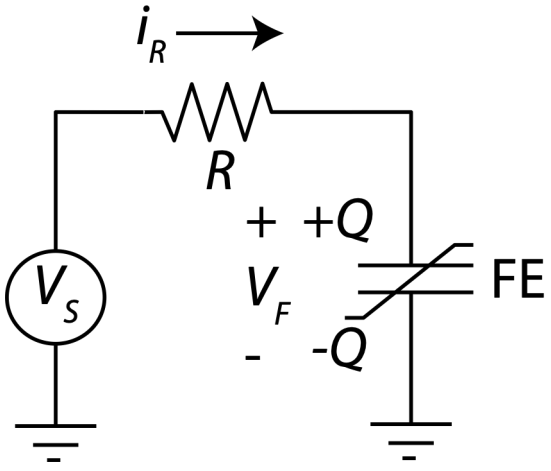




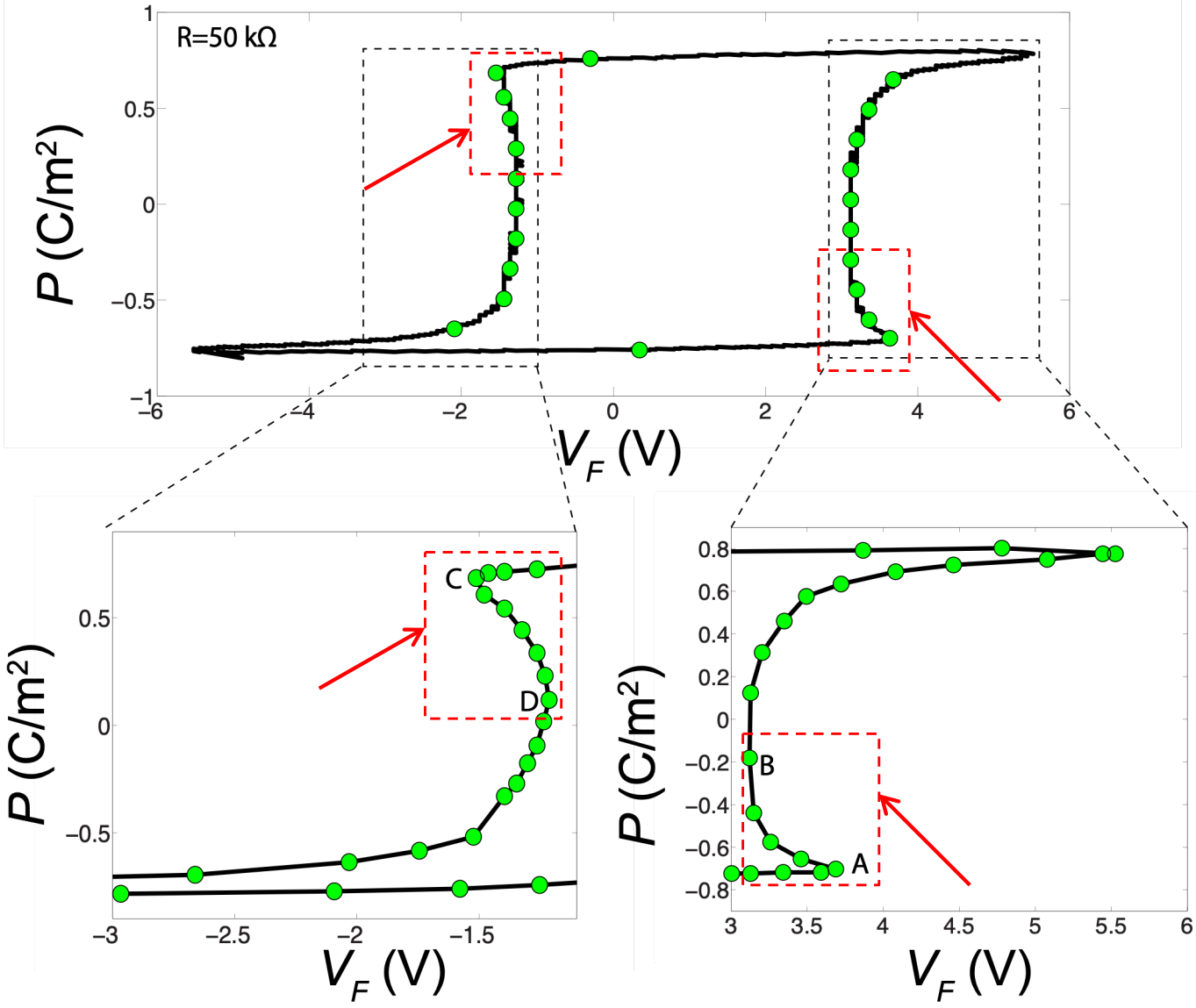
During AB & CD, dQ & dV_F has opposite signs indicating $dQ/dV_F < 0$.

Khan et al. Nature Mater. 14, 182 (2015)

Direct Measurement of Negative Capacitance



60 nm $Pb(Zr_{0.2}Ti_{0.8})O_3$ (Coercive voltage=~2.5 V)



A negative dQ/dV_F directly observed in an isolated ferroelectric.

Khan et al. Nature Mater. 14, 182 (2015)

Perspective

Nature Nanotech. 3, 77 (2008)

NEWS & VIEWS

NANOELECTRONICS

Negative capacitance to the rescue?

Victor V. Zhirnov* and Ralph K. Cavin
are at the Semiconductor Research Corporation, Research Triangle Park, North Carolina 27709, USA.
*e-mail: Victor.Zhirnov@src.org

At this point the proposed negative capacitance mechanism has not been observed in experiments, and it remains

Nature Materials 14, 137 (2015)

news & views

FERROELECTRICS

Negative capacitance detected

The experimental detection of negative capacitance in ferroelectrics rekindles hopes that the phenomenon could be used to further push the miniaturization of conventional transistors.

Gustau Catalan, David Jiménez and Alexei Gruverman

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Negative Capacitance in 1956!

Landauer et al. Polarization reversal in the Barium Titanate hysteresis loops.
J. Appl. Phys. 27, 752 (1956)

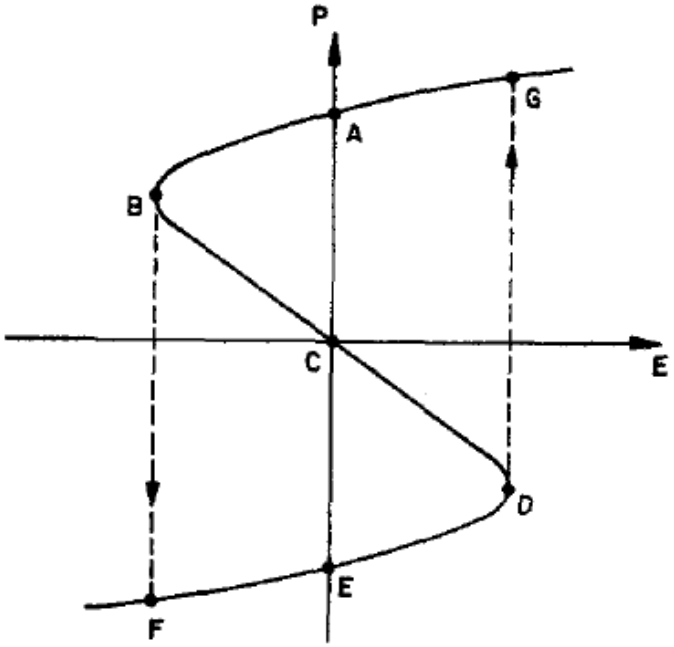

FIG. 1. Plot of polarization against field, at room temperature, as given by Devonshire's theory. P = polarization, E = field. Direction of field and polarization are taken to be the same, and parallel to the "c" axis of a single domain crystal. The solid line $GABCDEF$ gives the theoretical relationship.

Merz. Switching time in BaTiO3 and its dependence on its crystal thickness. **J. Appl. Phys.** 27, 938 (1956)

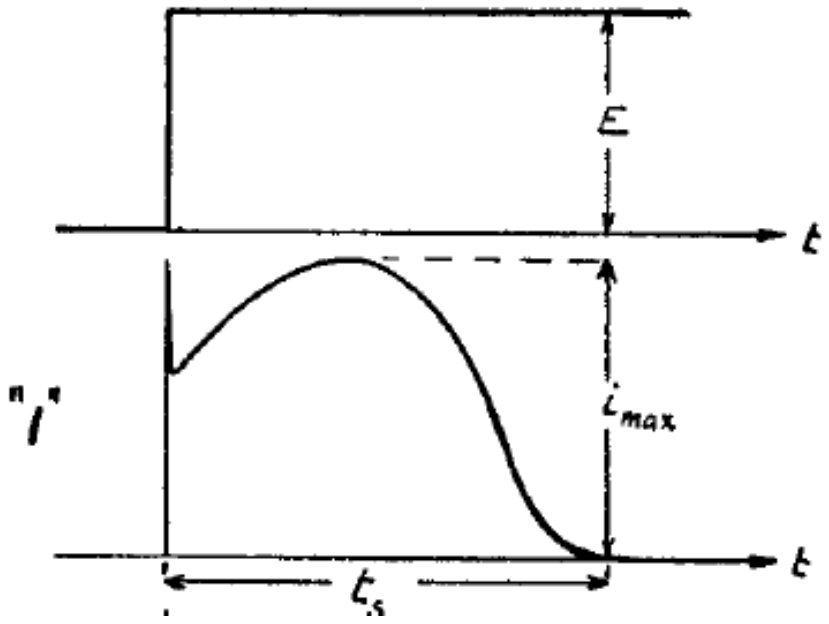

FIG. 1. Pulsing field and pulsing current *versus* time.

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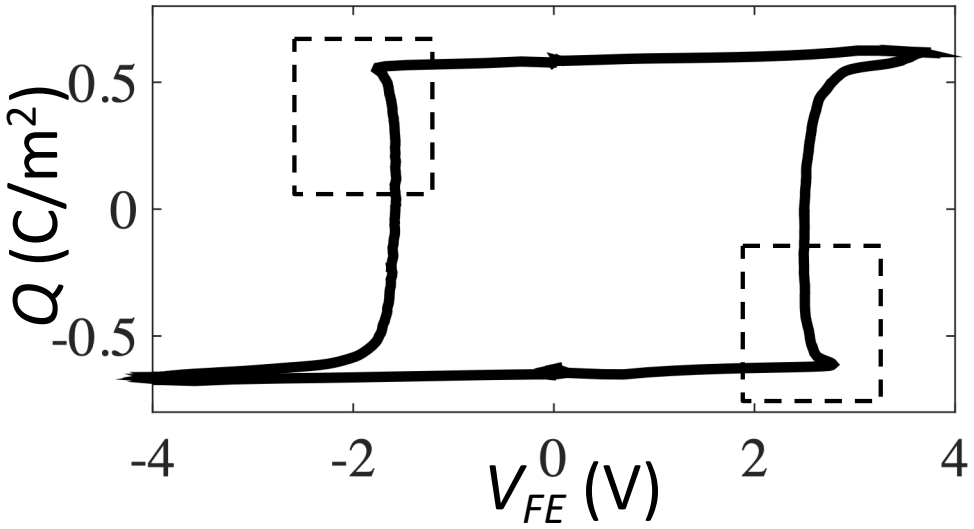
What's next?

Now that negative capacitance has been detected…



1. Can we see capacitance enhancement?

2. Can we see sub-60 mV/decade of subthreshold swing?

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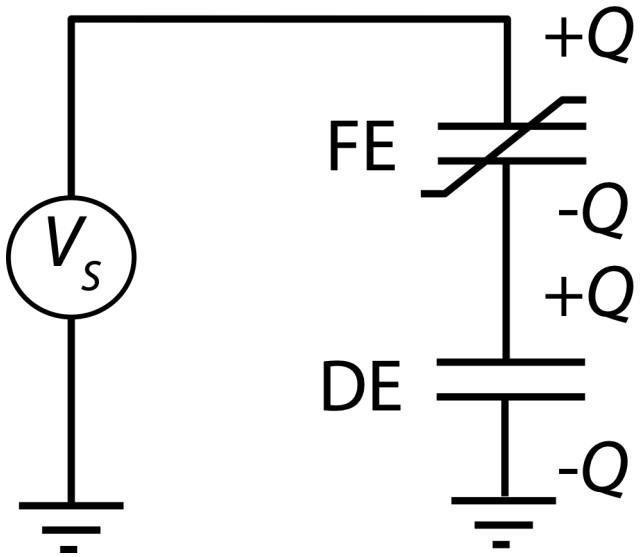
Breaking the Circuit Laws using Neg. Cap.

Ferroelectric-Dielectric
Series Combination



Equivalent Capacitance $C_{FE+DE} = \left[\frac{1}{C_{FE}} + \frac{1}{C_{DE}}\right]^{-1}$

$C_{FE+DE} > C_{DE}$ If $C_{FE} < 0$

Enhancement of capacitance in a FE-DE Series combination!

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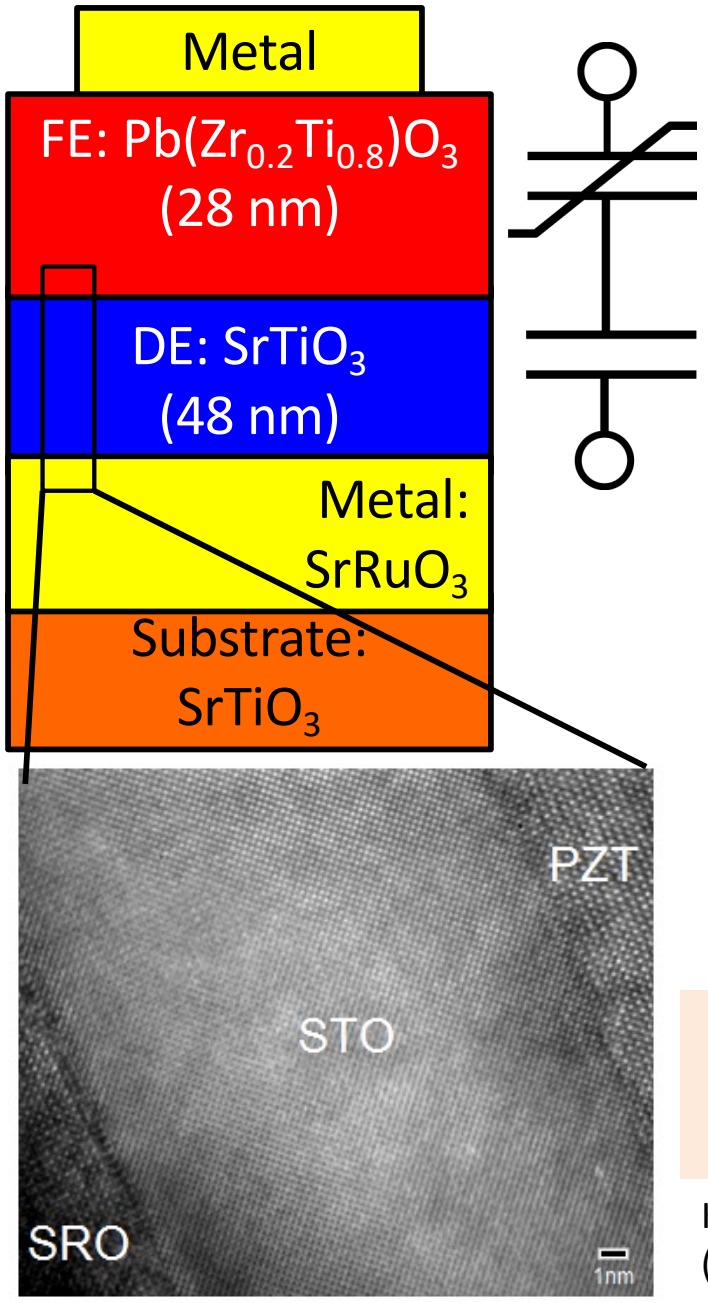
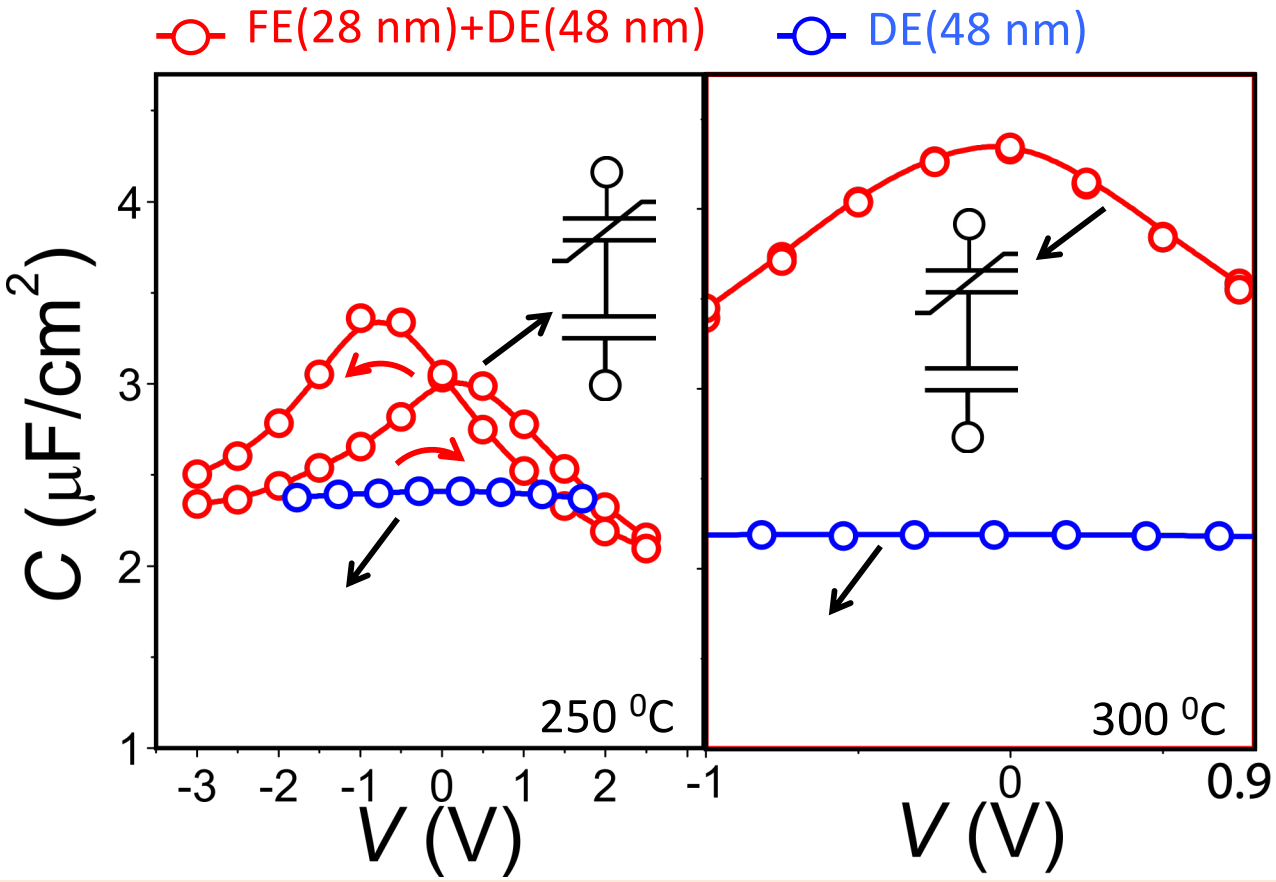
Breaking the Circuit Laws using Neg. Cap.



C-V Characteristics



Capacitance Enhancement in a FE-DE heterostructure experimentally observed!

Khan et al. Appl. Phys. Lett. 100, 113501 (2011) (cover article, most downloaded Aug/Sep 2011).
Gao, Khan et al. Nano Lett. 14, 5814 (2014)

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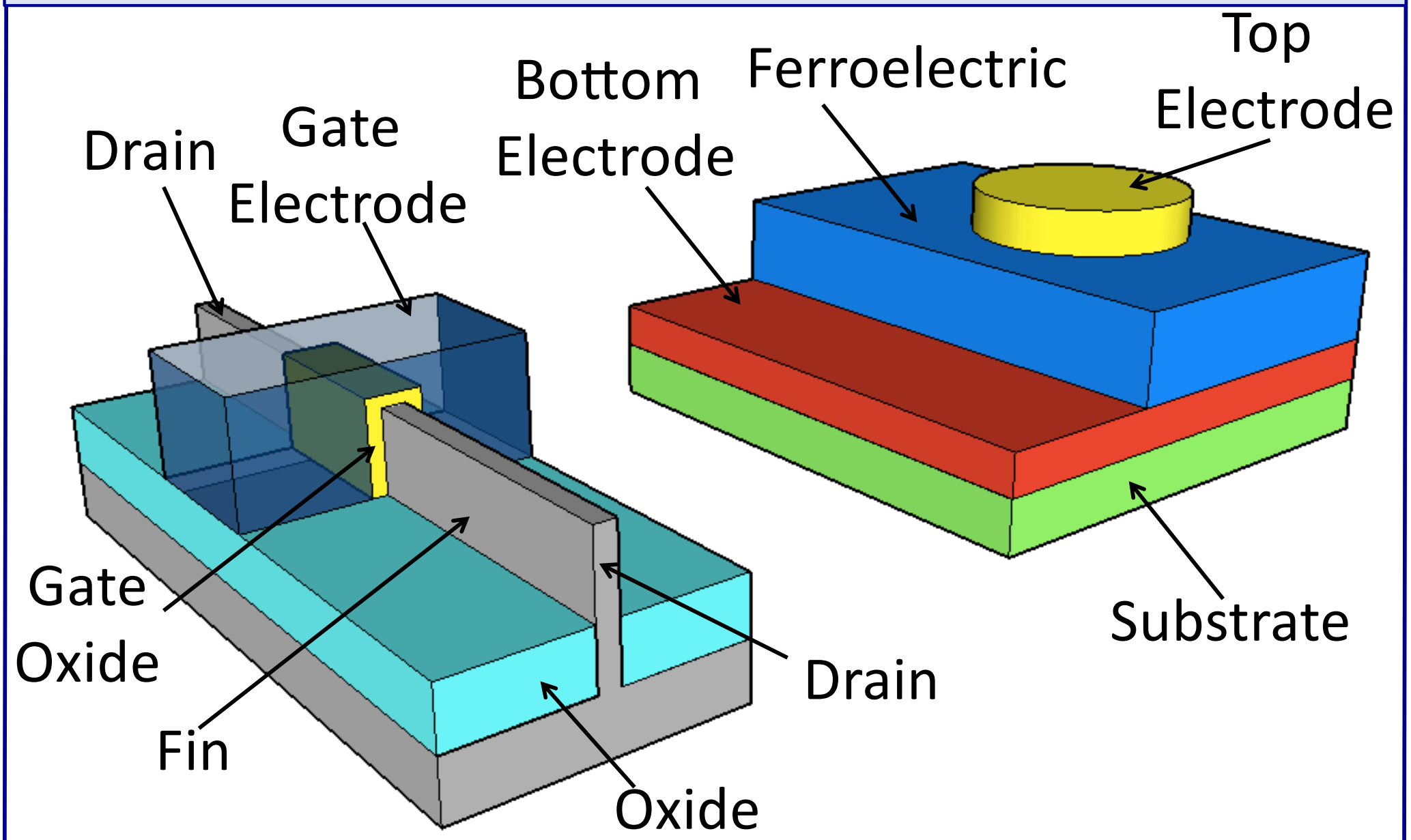
Externally Connected NCFET



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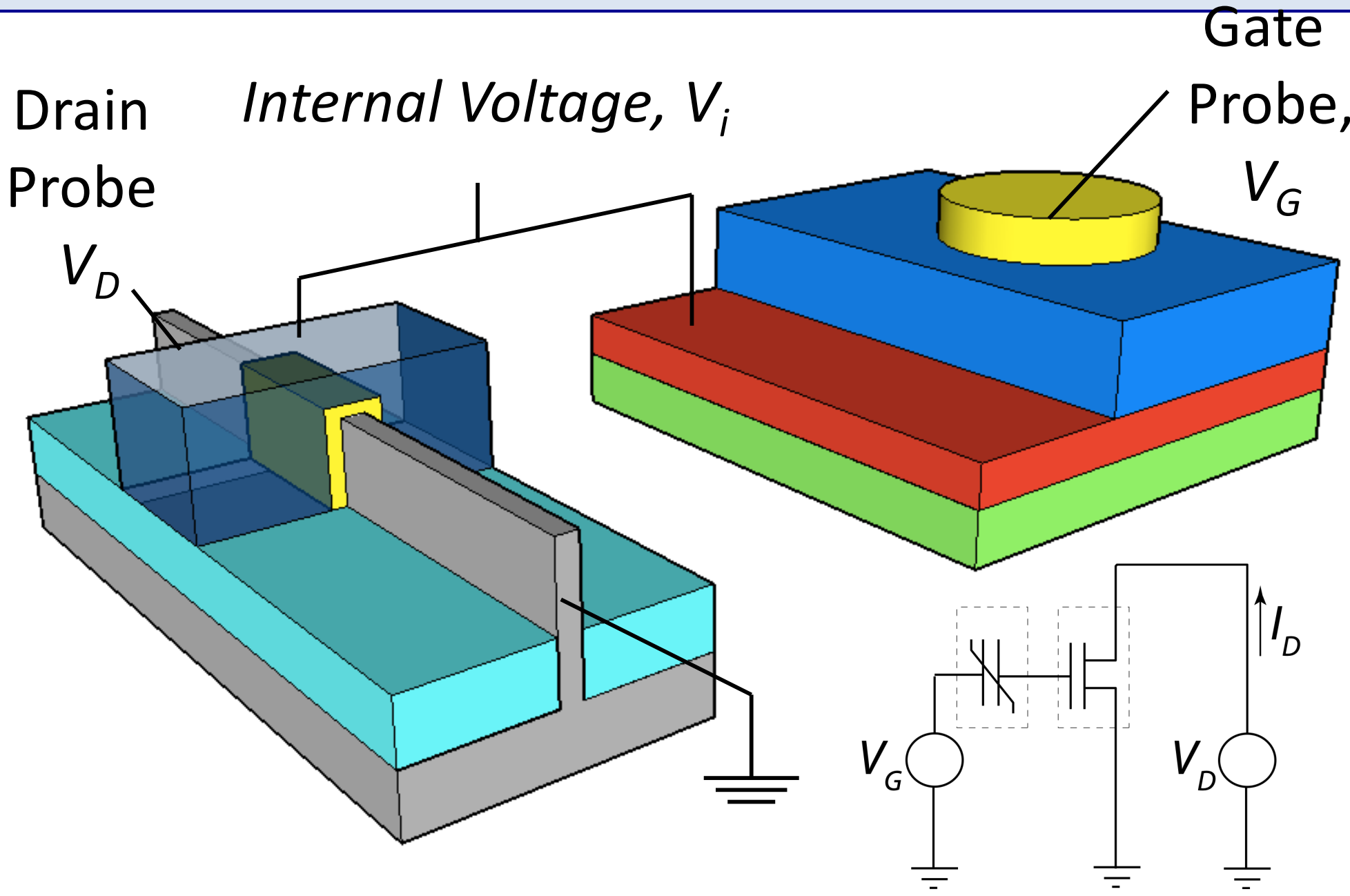
Externally Connected NCFET



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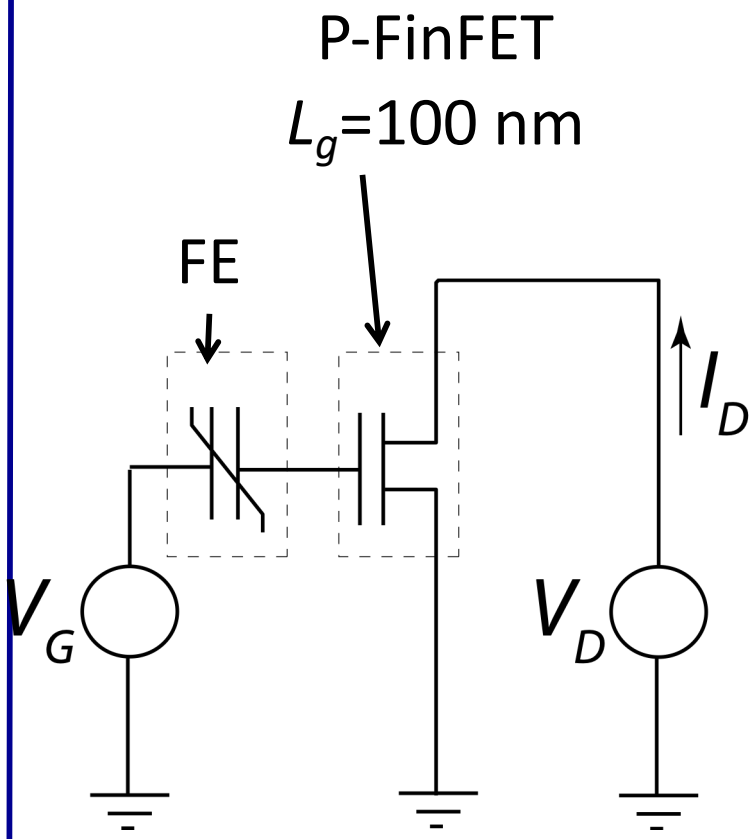
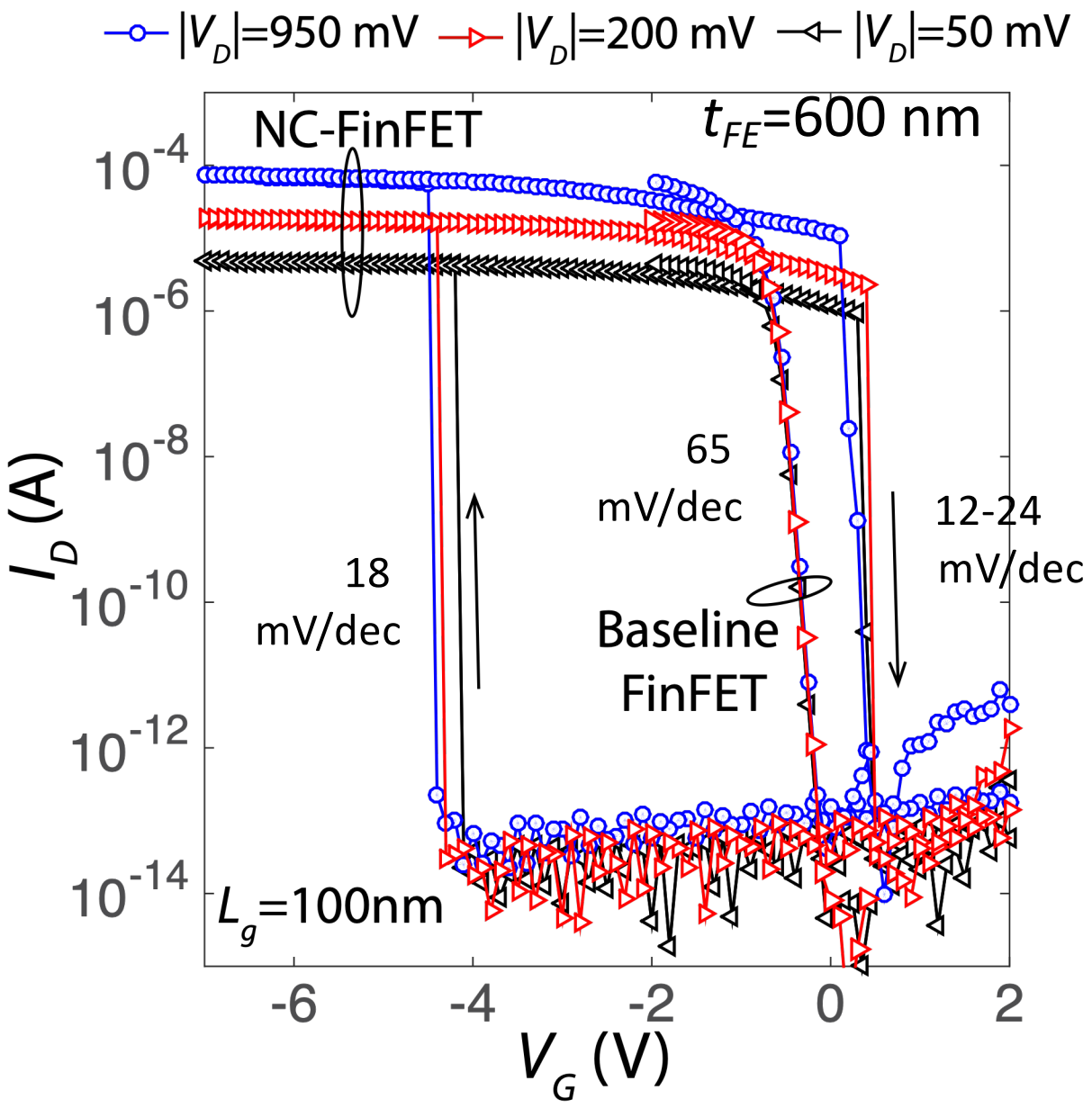
Externally Connected NCFET



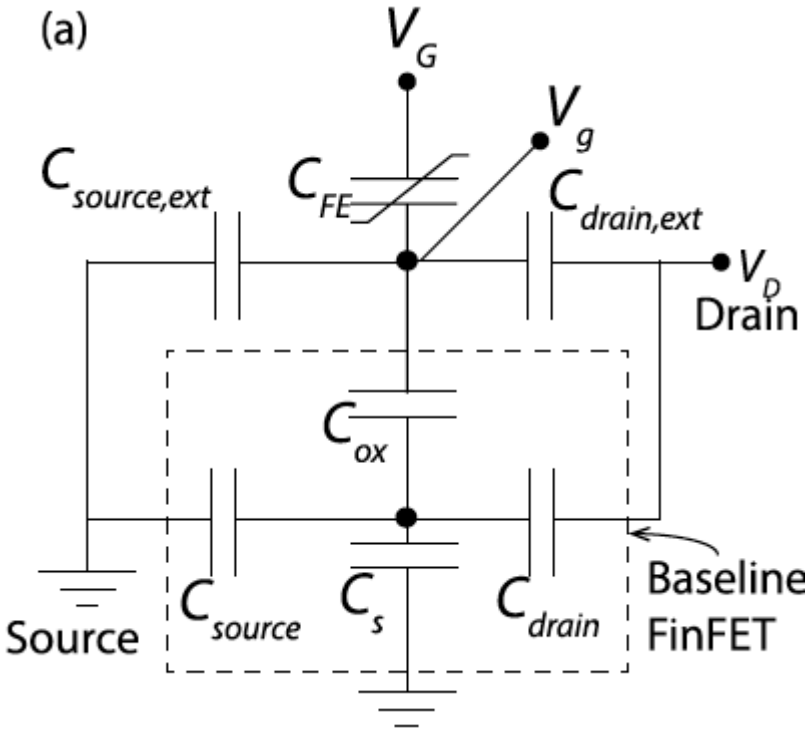
FinFET L_G=100 nm
Fin width=35 nm
Fin height=25 nm
EOT=1.4 nm

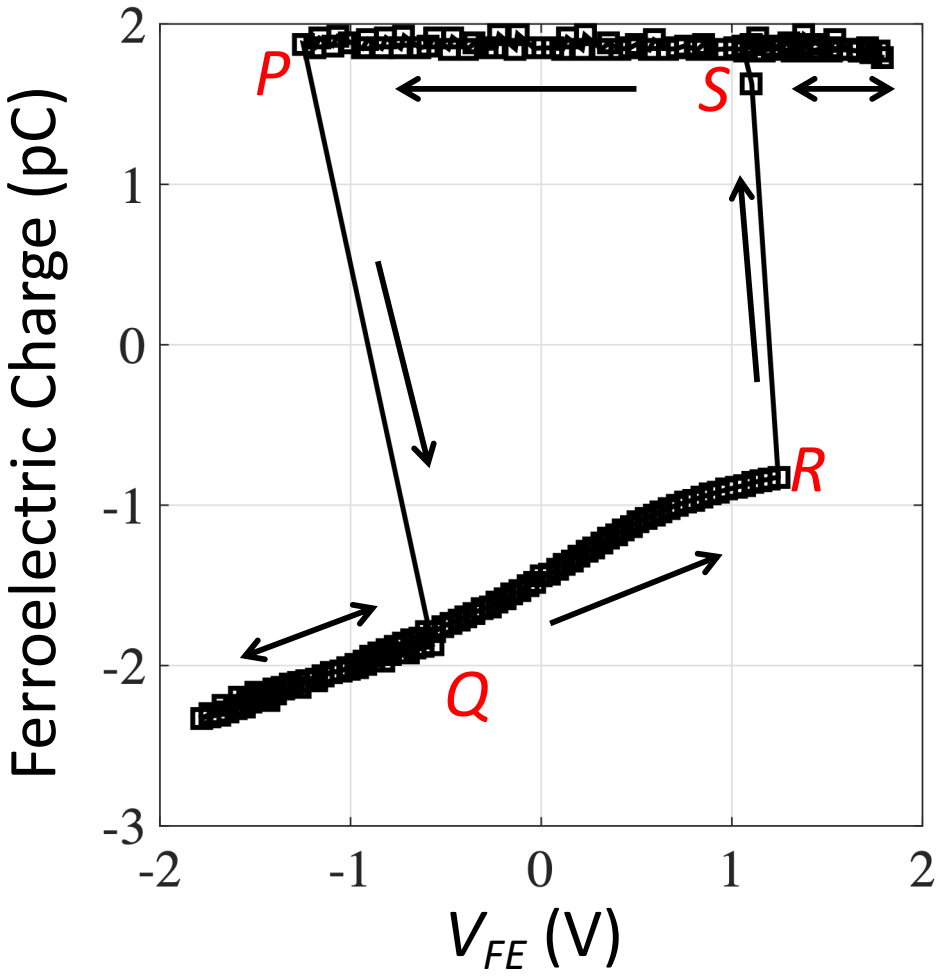


Khan et al. IEEE EDL 37, 111 (2016)

Berkeley
UNIVERSITY OF CALIFORNIA

Externally Connected NC-FET





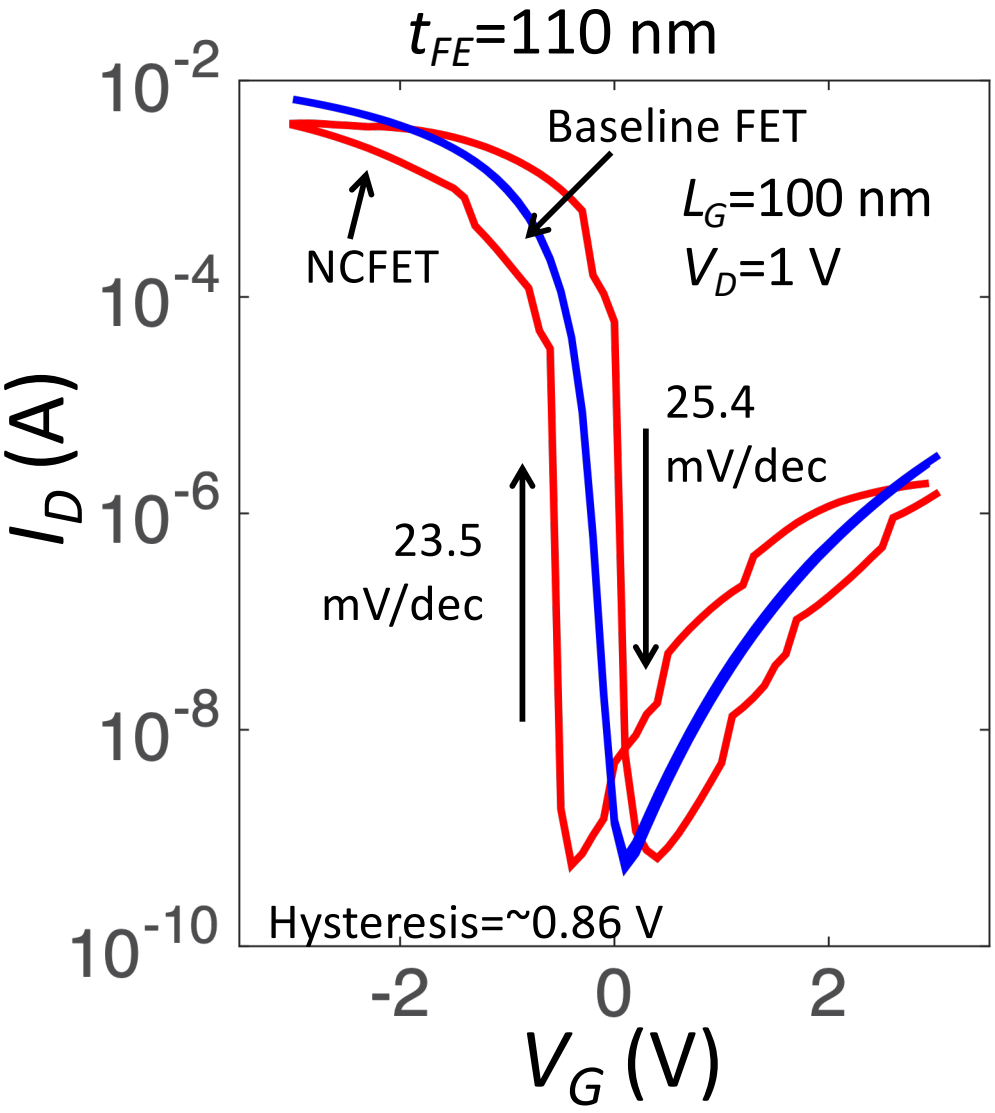
Sharp switching occurs due to ferroelectric negative capacitance!

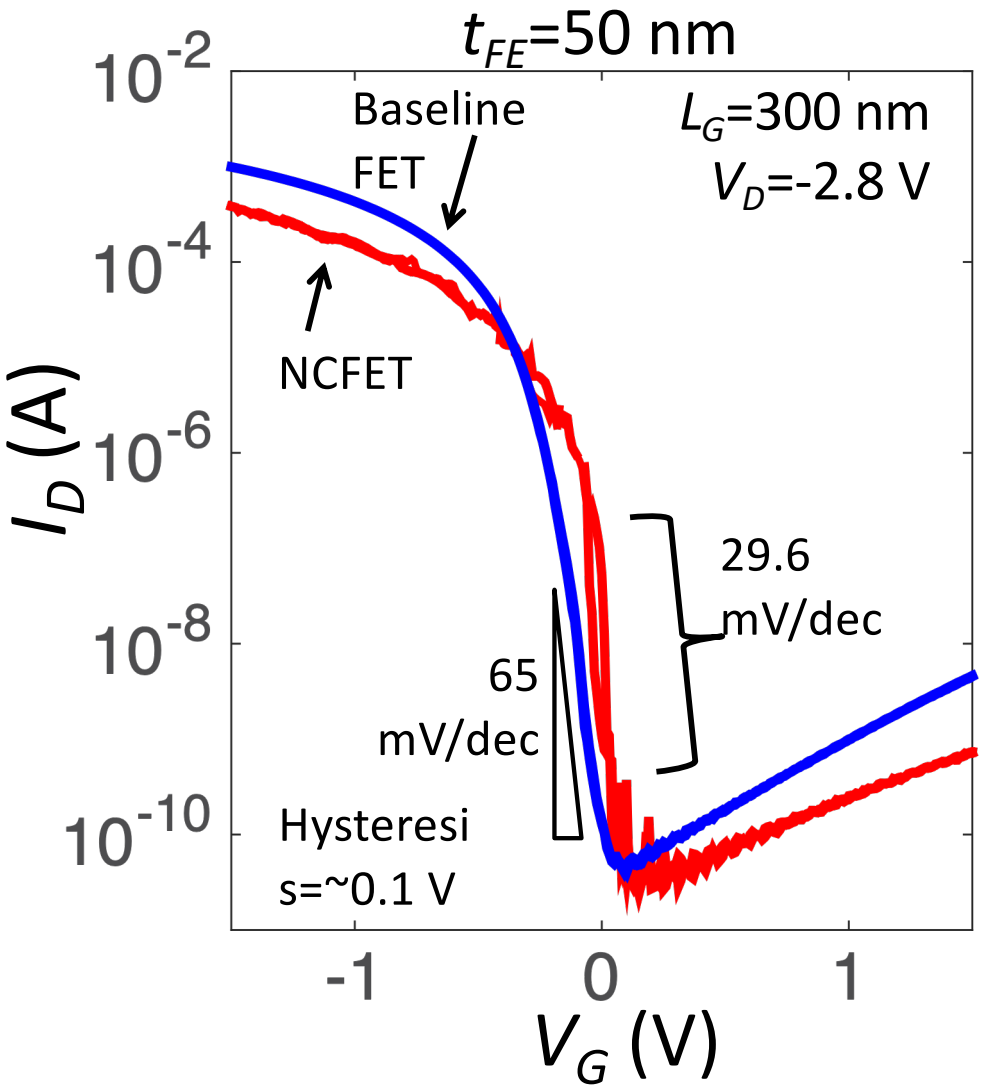
Negative Capacitance Regions: PQ and RS

Khan et al. IEEE EDL 37, 111 (2016)

Berkeley
UNIVERSITY OF CALIFORNIA

Externally Connected NC-FET





Khan, Jo et al.
(unpublished)

Negative capacitance can reduce subthreshold swing below 60 mV/dec!

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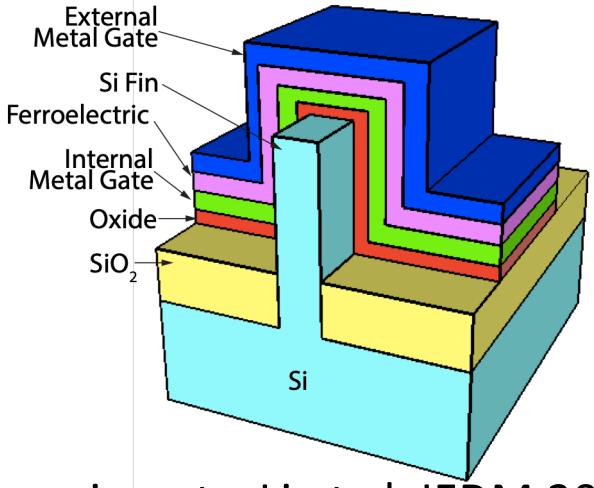
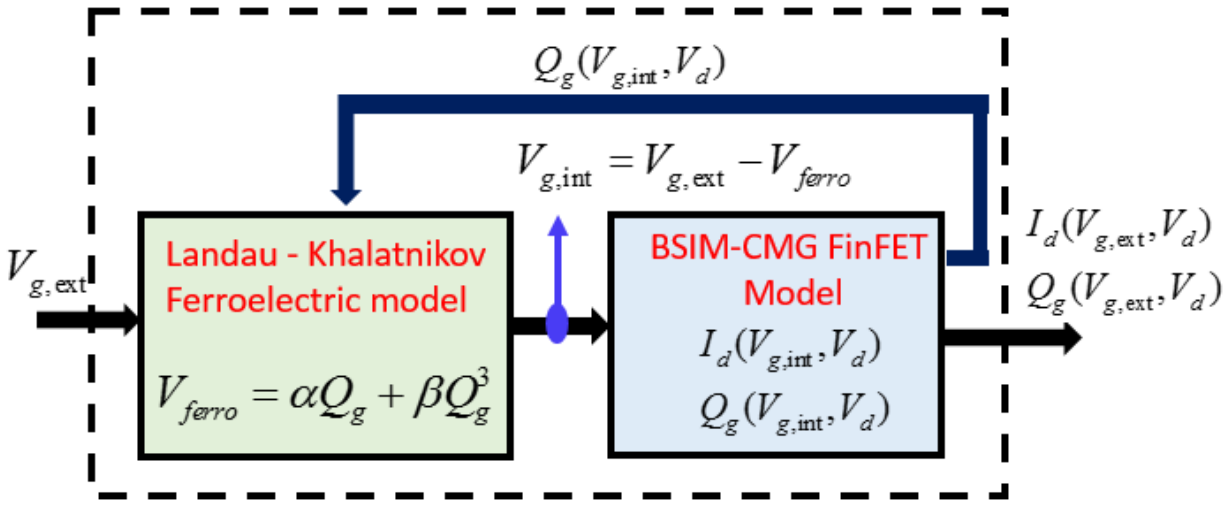
Performance Projection of NCFETs

14 nm FinFET Node

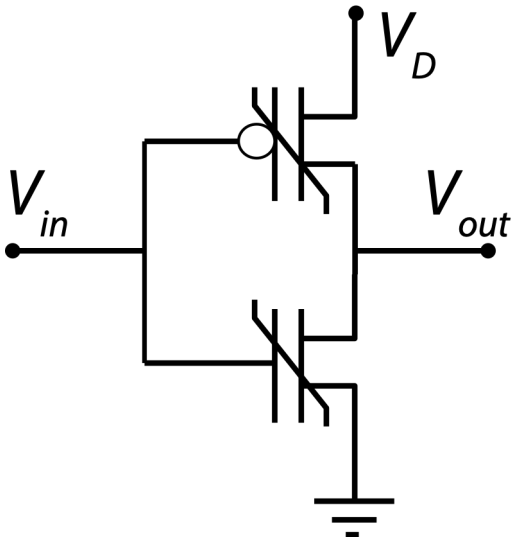


Experiments: Li et al. IEDM 2015

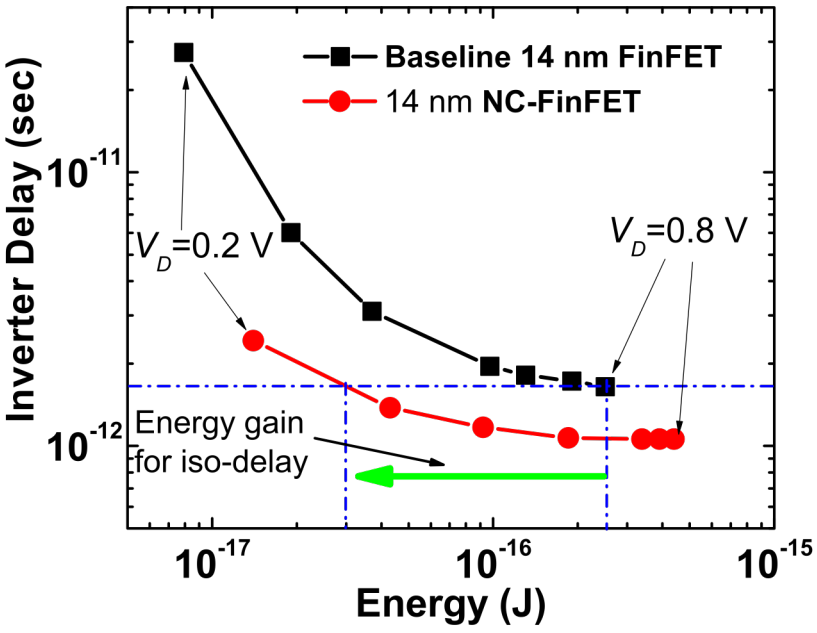
Compact Model



Inverter



Energy-Delay Curve



Significant reduction of energy-delay product is possible with negative capacitance

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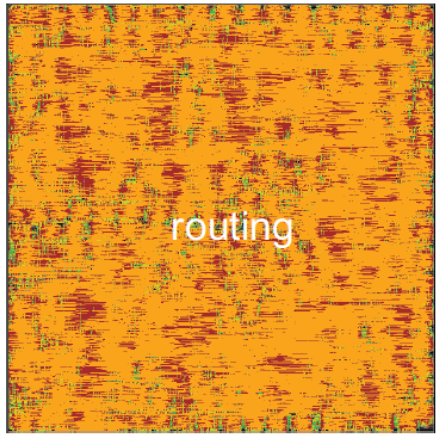
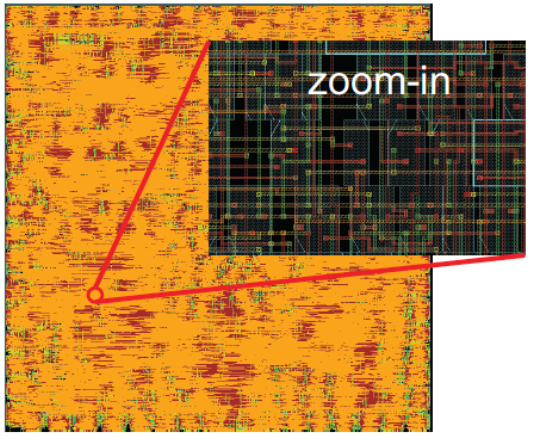
Full Chip Power Benefits of NCFETs

- Advanced Encryption Core (AES) Engine: ~120,000 gates, ~800,000 devices
- Iso-performance analysis (2 GHz)
- Steps:
  - 14 nm NCFET BSIM models based on experimental results (Li et al. IEDM 2015)
  - NCFET-based standard-cell library characterization
  - Full-chip NCFET-based GDSII-level design implementations



baseline FET @ 0.8V



NCFET @ 0.4V

Metric	BaseFET@0.8V	NCFET@0.5V	Δ	NCFET@0.4V	Δ
WNS (ps)	+3.9	+3.4		+9.3	
Wire switching (mW)	16.5	6.5	-61%	4.6	-72%
Cell-pin switching (mW)	98.0	62.5	-36%	38.2	-61%
Cell internal (mW)	182.2	75.8	-58%	46.6	-74%
Leakage (mW)	6.25	0.94	-85%	0.96	-85%
Total (mW)	**303.0**	**145.8**	**-52%**	**90.4**	**-70%**
Clock (mW)	141.8	62.2	-56%	36.8	-74%
Combinational (mW)	122.1	66.1	-46%	42.9	-65%
Registers (mW)	39.1	17.5	-55%	10.6	-73%

- **70% power saving obtained at 0.4V!**

Collaboration with Lim group at Georgia Tech

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Why am I excited
And
Why everyone can/should be excited?

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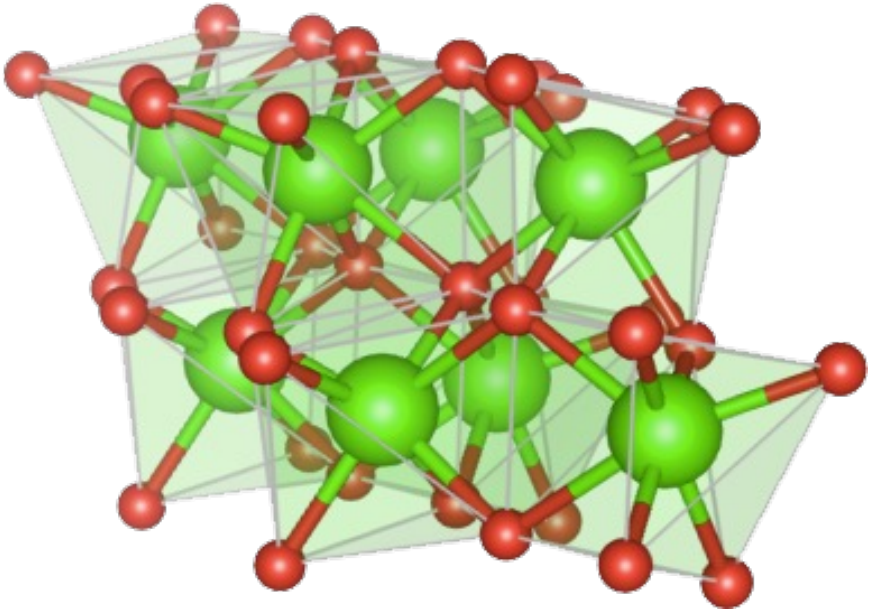
New CMOS Compatible Ferroelectrics

New class of ferroelectric materials have emerged which can be introduced in commercial fabs!



Controlled annealing in **HfO_2** doped with Zr, Al, Si, Sr, Ti, La etc. induces a ferroelectric orthorhombic phase!

Commercial Fabs!

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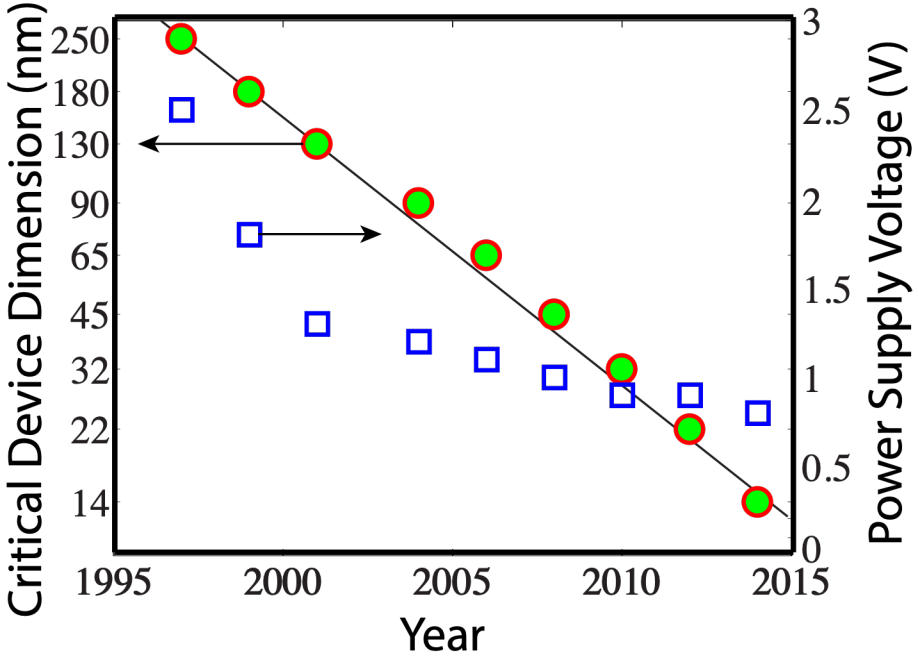
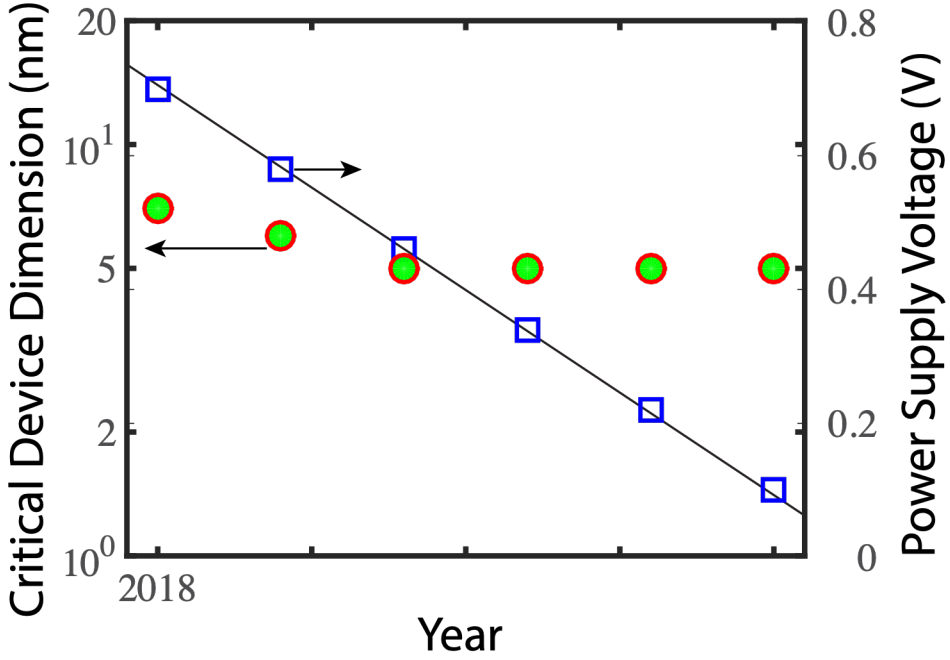
Advanced CMOS with Negative Capacitance

Current CMOS Technology



Beyond CMOS with Negative Capacitance



Negative capacitance technology could continue the performance enhancement after scaling ends!

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THANKS

QUESTIONS
&
COMMENTS

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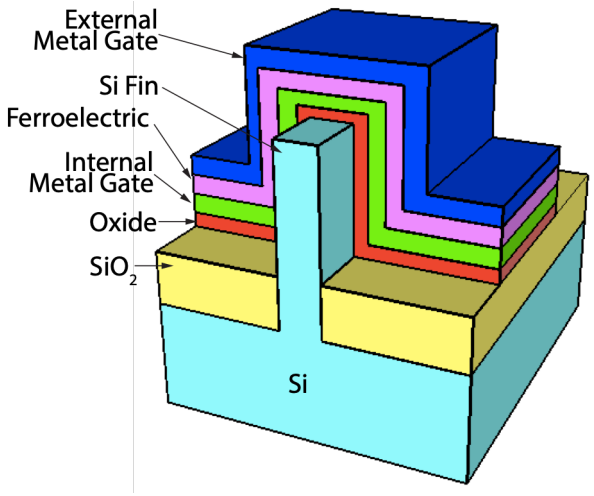
Physics of Negative Capacitance FET

14 nm FinFET Node

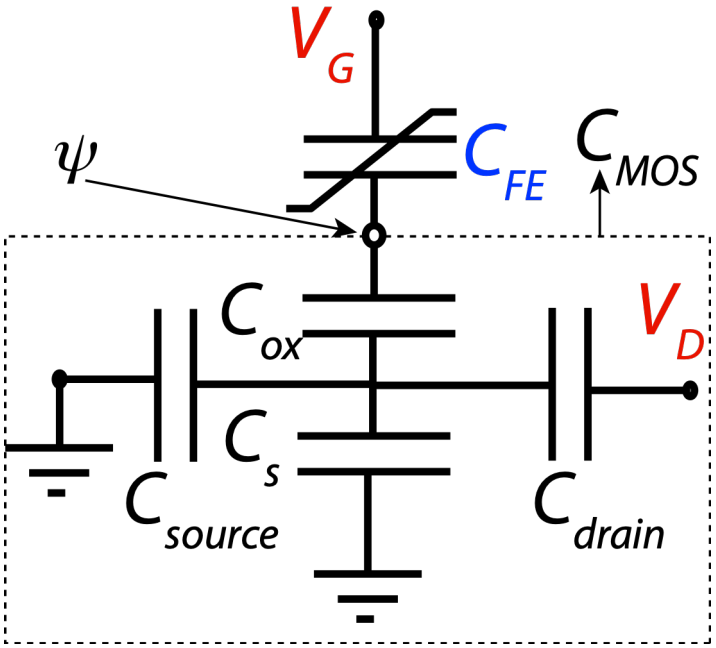


Modified Body Factor $m^o = \frac{dV_G}{d\psi} = 1 - \frac{C_{MOS}}{|C_{FE}|}$ <1

Subthreshold Swing $S = S^{baseline} \times m^o < S^{baseline}$

Input gate capacitance $C_G = \frac{C_{G,baseline}}{m} > C_{G,baseline}$

Power $P = \alpha C_L V_{DD}^2 f$



Where does the power benefits come from?

$C_L \uparrow V_{DD} \downarrow\downarrow P \downarrow\downarrow$

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